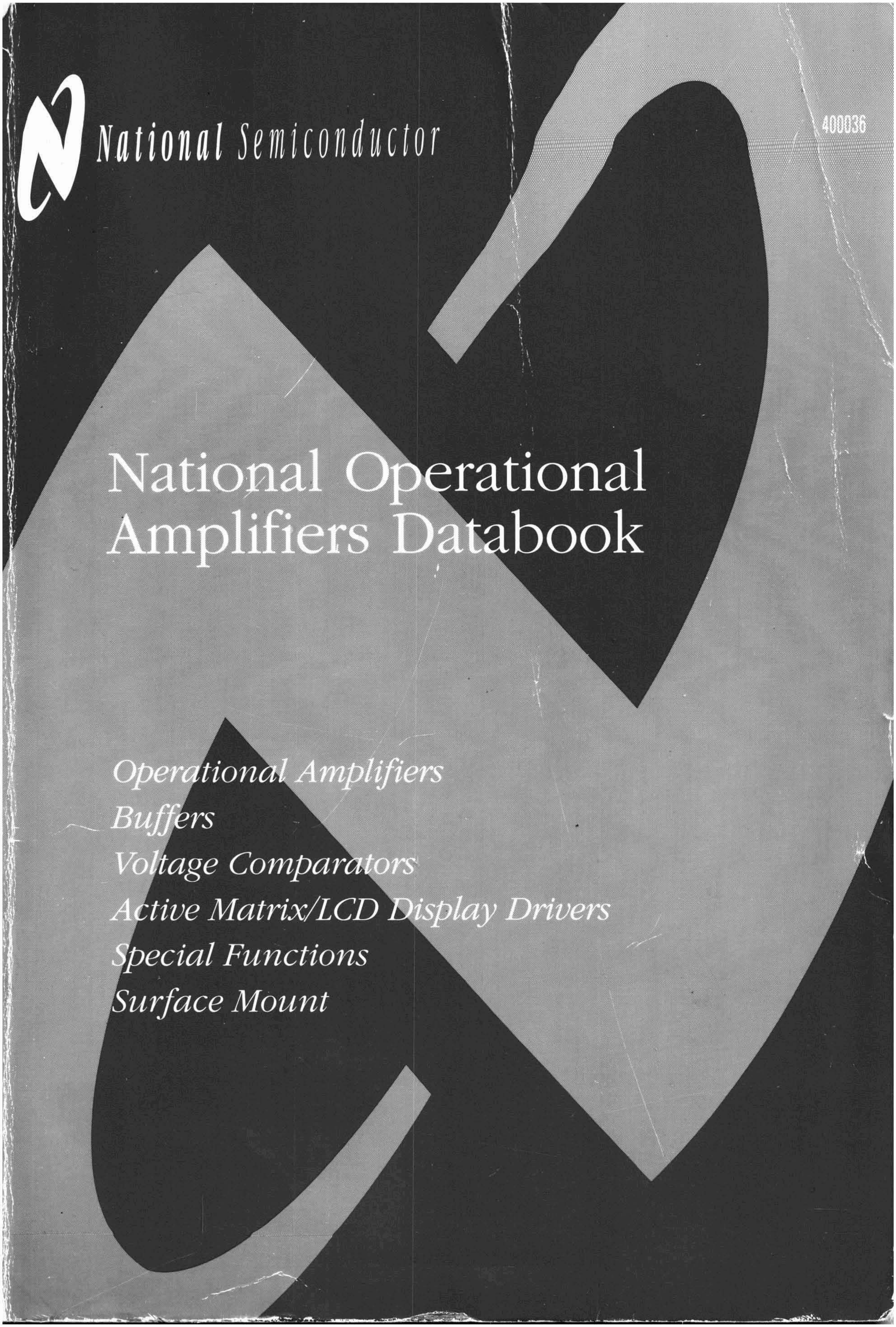

National Semiconductor

400036

National Operational Amplifiers Databook

Operational Amplifiers
Buffers
Voltage Comparators
Active Matrix/LCD Display Drivers
Special Functions
Surface Mount

OPERATIONAL AMPLIFIERS DATABOOK

1995 Edition

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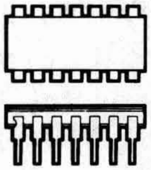
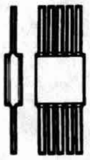
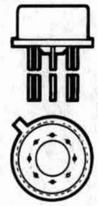
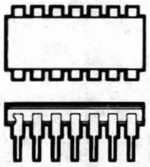
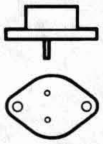
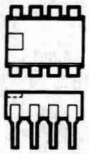
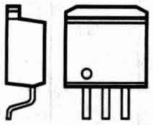
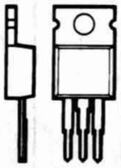
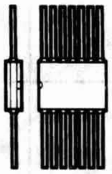
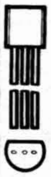
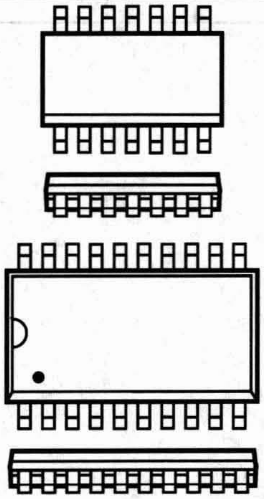
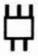
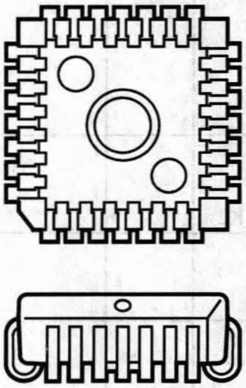
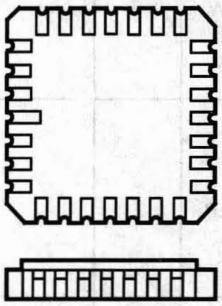
National Semiconductor

Industry Package Cross-Reference Guide

		NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
	4/16 Lead Glass/Metal DIP	D	D	I	L		D	R
	Glass/Metal Flat Pack	F	F	Q	F	F, S	F	
	TO-99, TO-100, TO-5	H	H	T, K, L, DB	G	L	H	
	8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	R, D	F	U	J	D	H
	TO-3 (Steel)	K			KS			
	(Aluminum)	KC	K	DA	K	K		
	8-, 14- and 16-Lead Plastic DIP	N	T, P	N, V	P	P, N	P	A, B, M

		NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
	TO-263 3- & 5-Lead	S						
	TO-220 3- & 5-Lead	T	U	U		KC		
	TO-220 11-, 15- & 23-Lead	T						
	Low Temperature Glass Hermetic Flat Pack	W	F		F	W	F	
	TO-92 (Plastic)	Z	W	S	P	LP		
	SO (Narrow Body)	M	S	S, D	D	D		L
	(Wide Body)	WM				DW		LW
	SOT-23 5-Lead	M5						

		NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
	PCC	V	Q	A	FN	FN	L	EP
	LCC Leadless Ceramic Chip Carrier	E	L1	G	U	FK/ FG/FH	L	EK

Section 1
Operational Amplifiers

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Operational Amplifiers Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

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General Purpose Operational Amplifier Selection Guide

Automotive Temperature Range (−40°C to +85°C) Specs at $T_A = 25°C$ (Note 1)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Specified Supply Voltage		Special Features
						Min V	Max V	
LM6142A	1	250	17	25	0.8	2.7	24	R-R In-Out Dual
LM6144A	1	250	17	25	0.8	2.7	24	R-R In-Out Quad
LM6142B	2.5	300	17	25	0.8	2.7	24	R-R In-Out Dual
LM6144B	2.5	300	17	25	0.8	2.7	24	R-R In-Out Quad
LM833	5	1000	15	7	4	10	30	Dual Low Noise
LP2902	4	20	0.1	0.05	0.031	3	26	Quad
LM2902	7	250	1	0.5	0.75	5	26	Quad
LM2904	7	250	1	0.5	1.0	5	26	Dual
LM2924	7	250	1	0.5	1.0	5	26	Comparator + Op Amp

Industrial Temperature Range (−25°C to +85°C) Specs at $T_A = 25°C$ (Note 1)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Specified Supply Voltage		Special Features
						Min V	Max V	
LM208A	0.5	2		0.3	0.6	10	40	
LM10B(L)	2	20	0.09	0.1	0.4	(Note 4)		Op Amp + Reference
LM201A	2	75	1	0.5	2.5	10	40	
LM207	2	75	1	0.5	2.5	10	40	Compensated LM201A
LM208	2	2	1	0.3	0.6	10	40	
LM224A	3	80	1	0.5	0.75	5	30	Quad
LM258A	3	80	1	0.5	1.0	3	32	Dual
LF255	5	0.1	2.5	5	4	30	40	
LF256	5	0.1	5	12	7	30	40	
LF257	5	0.1	20	50	7	30	40	Minimum Gain of 5
LM224	5	150	1	0.5	0.75	5	30	Quad
LM258	5	150	1	0.5	1.0	5	30	Dual
LM246	6	250	1.2	0.4	0.625	3	30	(Note 5)
LM248	6	200	1	0.5	1.13	10	30	Quad
LH0042C	20	0.05	1	3	4	10	40	
LM6132	0.25	110	7	22	0.4	2.7	24	R-R In-Out Dual
LM6134	0.25	110	7	22	0.4	2.7	24	R-R In-Out Quad

General Purpose Operational Amplifier Selection Guide (Continued)

Commercial Temperature Range (0°C to +70°C) Specs at $T_A = 25°C$ (Notes 1 and 2)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Specified Supply Voltage Min V	Specified Supply Voltage Max V	Special Features
LF411A	0.5	0.2	4	15	2.8	10	40	
LF441A	0.5	0.05	1	1	0.25	10	40	
LM308A	0.5	7	1	0.3	0.8	10	40	
LM11C	0.6	0.1	0.8	0.3	0.8	5	40	
LF412A	1	0.2	4	15	2.8	12	40	Dual
LF442A	1	0.05	1	1	0.2	10	32	Dual
LM604AC	1	50	7	3	9	10	32	Multiplexed Op Amp
LF355A	2	0.05	2.5	5	4	30	36	
LF356A	2	0.05	5	12	10	30	36	
LF357A	2	0.05	20	50	10	30	36	Minimum Gain of 5
LF411	2	0.2	4	15	3.4	10	30	
LF412	3	0.2	4	15	3.3	12	30	Dual
LM324A	3	100	1	0.5	0.75	5	30	Quad
LM358A	3	100	1	0.5	1.0	5	30	Dual
LM604C	3	80	7	7	4.5	10	32	Multiplexed Op Amp
LM741E	3	80	1.5	0.7	2.8	10	40	
LM10C(L)	4	30	0.09	0.1	0.5	(Note 4)		Op Amp + Reference
LP324	4	10	0.1	0.05	0.0375	5	30	
LF347B	5	0.2	4	13	2.8	10	30	Quad
LF355B	5	0.1	2.5	5	4	30	40	
LF356B	5	0.1	5	12	4	30	40	
LF357B	5	0.1	20	50	7	30	40	
LF441	5	0.1	1	1	0.25	10	30	
LF442	5	0.1	1	1	0.25	10	30	Dual
LM11CL	5	0.2	0.8	0.3	0.8	5	40	
LF451	5	0.2	4	13	3.4	10	32	SO Pkg
LF453	5	0.2	4	13	3.25	10	32	SO Pkg Dual
LM611	5	35	0.8	0.7	0.35	2.8	32	Op Amp + Ref
LM613	5	35	0.8	0.7	0.25	2.8	32	2 Op Amps + 2 Comparators + Ref

General Purpose Operational Amplifier Selection Guide (Continued)

Commercial Temperature Range (0°C to +70°C) (Notes 1 and 2) (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Specified Supply Voltage		Special Features
						Min V	Max V	
LM614	5	35	0.8	0.7	0.25	2.8	32	Quad Op Amp + Ref
LM392	5	250	1	0.5	1	5	30	
LM346	6	250	1.2	0.4	0.63	3	30	(Note 5)
LM348	6	200	1	0.5	1.13	10	30	
LM349	6	200	4	2	1.13	10	30	
LM741C	6	500	1.5	0.5	2.8	10	40	
LM1458	6	500	*	*	2.8	30	30	
LM4250C	6	75	0.2	0.2	0.1	3	30	(Note 5)
LM324	7	250	1	0.5	0.75	5	30	Quad, Low Cost
LM358	7	250	1	0.5	1.0	5	30	Dual
LM301A	7.5	250	1	0.5	3	10	30	V_{CM} to V^+
LM307	7.5	250	1	0.5	3	10	30	Compensated LM301A
LM308	7.5	7	1	0.3	0.8	10	36	
LM343	8	40	1	2.5	5	56	68	
LF347	10	0.2	4	13	2.75	10	30	Quad
LF351	10	0.2	4	13	3.4	10	30	
LF353	10	0.2	4	13	5.4	10	30	Dual
LF355	10	0.2	2.5	5	4	30	30	
LF356	10	0.2	5	12	10	30	30	
LF357	10	0.2	20	50	10	30	30	Minimum Gain of 5
LF444	10	0.1	1	1	0.25	10	30	Quad
TL081C	15	0.2	4	13	2.8	10	30	
TL082C	15	0.2	4	13	2.8	12	30	Dual

*Not Specified.

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: Those looking for a commercial part should also look at the Industrial Temp Range guide as many Hybrids are listed there.

Note 3: Supply current is per amplifier.

Note 4: The LM10 has 2 versions: one a high voltage part, good to 45V and a low voltage part, good to 7V. Refer to the datasheet for more information.

Note 5: The LM146 and LM4250 are programmable amplifiers. The data shown is for $V_S = \pm 15V$ and $I_{SET} = 10\ \mu A$. Refer to the datasheets for more information.

General Purpose Operational Amplifier Selection Guide (Continued)

Military Temperature Range (−55°C to +125°C) Specs at T_A = 25°C (Note 1)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Specified Supply Voltage		Special Features
						Min V	Max V	
LF411AM	0.5	0.2	4	15	2.8	10	40	
LF441AM	0.5	0.05	1	1	0.2	10	40	
LM108A	0.5	2	1	0.3	0.6	10	40	
LF412A	1	0.2	4	15	2.8	12	40	Dual
LF442A	1	0.05	1	1	0.2	12	40	Dual
LH0004	1	100	10	*	0.15	10	80	High Voltage
LM604A	1	50	7	2	4.5	10	32	Multiplexed Op Amp
LF155A	2	0.05	2.5	5	4	30	40	
LF156A	2	0.05	5	12	7	30	40	
LF157A	2	0.05	20	50	7	30	40	Minimum Gain of 5
LF411M	2	0.2	4	15	3.4	10	30	
LM10	2	20	0.09	0.1	0.4	1.2	40	Op Amp + Reference
LM101A	2	75	1	0.5	3	10	40	V_{CM} to V^+
LM107	2	100	1	0.5	3	10	40	Compensated LM101A
LM108	2	2	1	0.3	0.6	10	40	
LM124A	2	50	1	0.5	0.75	5	30	Quad
LM158A	2	50	1	0.5	0.5	5	30	Dual
LP124	2	4	0.1	0.05	0.035	5	30	Quad
LF412	3	0.2	4	15	3.25	12	30	Dual
LM741A	3	80	1.5	0.7	2.8	10	40	
LF155	5	0.1	2.5	5	4	30	40	
LF156	5	0.1	5	12	7	30	40	
LF157	5	0.1	20	50	7	30	40	Minimum Gain of 5
LF147	5	0.2	4	13	2.75	10	40	Quad
LF442	5	0.1	1	1	0.25	10	40	Dual
LF444A	5	50	1	1	0.20	10	40	Quad
LM124	5	150	1	0.5	0.75	5	30	Quad

General Purpose Operational Amplifier Selection Guide (Continued)

Military Temperature Range (−55°C to +125°C) Specs at $T_A = 25°C$ (continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Specified Supply Voltage		Special Features
						Min V	Max V	
LM143	5	20	1	2.5	4	56	80	High Voltage
LM146	5	100	1.2	0.4	0.55	3	30	(Note 5)
LM148	5	100	1	0.5	0.9	10	30	Quad
LM149	5	100	4	2	0.9	10	30	Minimum Gain of 5, Quad
LM158	5	150	1	0.5	1	5	30	Dual
LM741	5	500	1	0.5	2.8	10	40	
LM1558	5	500	*	*	2.5	30	30	Dual
LM4250	5	50	0.2	0.2	0.1	3	30	(Note 5)
LH0042	20	0.025	1	3	3.5	10	40	

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Low Input Current Selection Guide

<25 fA	<100 fA	≤5 pA*	≤20 pA	≤50 pA	≤100 pA	≤200 pA	≤500 pA
T_A = 25°C							
LMC6001A**	LMC6001B**	LMC660*	LH0042	LH0032A	LH0032	TL081	LH0032C
		LMC662*	LH0042C	LF155A/156A	LF155/156	LH0032AC	LH4004
		LMC6041*		LF157A	LF157	LF351	
		LMC6042*		LF355A/356A	LF255/256	LF411A/411	
		LMC6044*		LF357A	LF257	LF355/356	
		LMC6062*		LF441A	LF355B/356B	LF357	
		LMC6082*		LF442A	LF357B	LF147/347B/347	
		LPC660*		LF444A	LF441	LF353	
		LPC661*		LM11	LF442	LF412A/412	
		LPC662*			LF444	LM11CL	
		LMC6061*			LM11C	LMC6022*	
		LMC6081*			LH0101	LMC6024*	
		LMC6064*				LMC6032*	
		LMC6084*				LMC6034*	
		LMC6482*				LH4104	
		LMC6484*				LH4104C	
		LMC6001C					
		LMC6462					
		LMC6464					
		LMC6492					
		LMC6494					
		LMC6572					
		LMC6574					
		LMC6584					
		LMC6681					
		LMC6682					
		LMC6684					
		LMC7101					
		LMC7111					

Note: Datasheet should be referred to for conditions and more detailed information.

*Guaranteed over industrial temperature range (−40°C to +85°C). Typical value is ≤ 40 fA.

**100 percent tested and guaranteed.

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High Speed Operational Amplifier Selection Guide

Part #	Slew Rate V/µs (Typ)	GBW MHz (Typ)	V_{OS} mV (Max)	I_S mA (Max) (Note 1)	Notes
GBW ≥ 4 MHz, T_A = 25°C					
LM7171A	4100	200	1	8.5	High Output Current, Voltage Feedback
LM6171A	3600	100	3	4	Low Power, Voltage Feedback
LM7171	4100	200	3	8.5	High Output Current, Voltage Feedback
LM6171	3600	100	6	4	Low Power, Voltage Feedback
LM6172	3600	100	1	4	Dual Low Power, Voltage Feedback
LM6181	2000	100	7.0	10	Current Feedback, VIP
LM7121A	1000	200	3	5	Low Power, Voltage Feedback
LM7121	1000	200	6	5	Low Power, Voltage Feedback
LH0024	500	70	4	15	
LH0032	500	70	5	20	FET Input
LM6161	300	50	7	6.8	Unity Gain Stable, VIP™
LM6162	300	100	5	6.8	Min Gain of 2, VIP
LM6164	300	175	4	6.8	Min Gain of 5, VIP
LM6165	300	725	3	6.8	Min Gain of 25, VIP
LM6313	250	35	20	11.5	Hi Speed Hi Power, Dual
LM6218A	140	17	1	3.5	Fast Settling Dual, VIP
LM6218	140	17	3	3.5	Fast Settling Dual, VIP
LH0003	2–70	10–30	3	3	External Compensation
LM118	70	15	4	7	
LF157A	50	20	2	7	Min Gain of 5, JFET
LM359	30	30	*	11	Dual Current Mode (Norton) Amp
LM6152	30	45	2.5	1.5	R-R In-Out, Dual
LM6154	30	45	2.5	1.5	R-R In-Out, Quad
LM6142A	25	17	1.0	0.8	Low Power, R-R In-Out, Dual
LM6144A	25	17	1.0	0.8	Low Power, R-R In-Out, Quad
LF411A	15	4	0.5	1.4	JFET
LF412A	15	4	1.0	2.8	Dual JFET
LF147	13	4	5	2.75	Quad JFET
LF451	13	4	5	3.4	SO Pkg
LF453	13	4	5	3.25	SO Pkg Dual
LF351	13	4	10	3.4	JFET
LF353	13	4	10	3.3	Dual JFET
LF156A	12	5	2	7	JFET
LM833	7	15	5	4	Dual Low Noise

*Not specified.

Note 1: Supply current is per amplifier in a package.

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Precision Operational Amplifier Selection Guide

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (typ)	Slew Rate V/μs (Typ)	Supply Current (Note 1) mA (Max)	Notes
Singles						
LMC6081A	0.35	0.00001*	1.3	1.5	0.750	Low power
LMC6061A	0.35	0.00001*	0.1	0.035	0.024	Micropower
LM308A	0.5	7	1	0.3	0.8	
LM208A	0.5	2	1	0.3	0.6	
LM108A	0.5	2	1	0.3	0.6	
LF441A	0.5	0.05	1	1	0.2	
LF411A	0.5	0.2	4	15	2.8	
LM11C	0.6	0.1	0.8	0.3	0.8	
LMC6081	0.8	0.00001*	1.3	1.5	0.750	Low power
LMC6061	0.8	0.00001*	0.1	0.035	0.032	Micropower
Duals						
LMC6082A	0.35	0.00001*	1.3	0.75	0.75	Dual LMC6081A
LMC6062A	0.35	0.00001*	0.1	0.019	0.019	Dual LMC6061A
LMC6482A	0.5	0.00002*	1.3	1	0.50	Rail to Rail Input/Output
LMC6082	0.8	0.00001*	1.3	1.5	0.75	Dual LMC6081
LMC6062	0.8	0.00001*	0.1	0.035	0.023	Dual LMC6061
Quads						
LMC6084A	0.35	0.00001*	1.3	1.5	0.75	Quad LMC6081A
LMC6064A	0.35	0.00001*	0.1	0.035	0.019	Quad LMC6061A
LMC6484A	0.5	0.00002*	1.3	1	0.50	Rail to Rail Input/Output
LMC6084	0.8	0.00001*	1.3	1.5	0.75	Quad LMC6081
LMC6064	0.8	0.00001*	0.1	0.35	0.029	Quad LMC6061

*Typical Value

Note 1: Supply current is per amplifier.

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MicroPower/Low Power Operational Amplifier Selection Guide

Part #	I_S μA Typ (per Amp)	V_{OS} mV Max	I_B fA Typ	V_{CM} V Typ	Output Swing V Typ with RL = 100 kΩ	GBW MHz Typ	Specified Supply Voltage	
							Min V	Max V
Specs at T_A = 25°C and Vs = +5V								
Singles								
LMC6041A	14	3	2	−0.4 to 3.1	0.004 to 4.987	0.075	5	15
LMC6041	14	6	2	−0.4 to 3.1	0.004 to 4.987	0.075	5	15
LMC6061A	20	0.35	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LMC6061	20	0.8	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LPC661A	55	3	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LPC661	55	6	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LMC6081A	450	0.35	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6081	450	0.8	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6681A	700	1	80	−0.3 to 5.3	0.05 to 4.9	1.2	1.8	10
LMC6681	700	3	80	−0.3 to 5.3	0.05 to 4.9	1.2	1.8	10
Duals								
LMC6042A	10	3	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15
LMC6042	10	6	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15
LMC6062A	16	0.35	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LMC6062	16	0.8	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LMC6462A	20	0.5	150	−0.2 to 5.3	0.005 to 4.995	0.05	73	15
LMC6462	20	3	150	−0.2 to 5.3	0.005 to 4.995	0.05	3	15
LPC662A	43	3	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LPC662	43	6	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LMC6022	43	9	40	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LMC662A	375	3	2	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC662	375	6	2	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC6032	375	9	40	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC6082A	450	0.35	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6082	450	0.8	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6482A	500	0.5	20	0 to 5	0.03 to 4.97	1.3	3	15
LMC6482	500	3	20	0 to 5	0.03 to 4.97	1.3	3	15
LMC6492A	500	3	150	−0.3 to 5.3	0.02 to 4.98	1.5	2.5	15.5
LMC6492	500	6	150	−0.3 to 5.3	0.02 to 4.98	1.5	2.5	15.5

MicroPower/Low Power Operational Amplifier Selection Guide (Continued)

Part #	I_S μA Typ (per Amp)	V_{OS} mV Max	I_B fA Typ	V_{CM} V Typ	Output Swing V Typ with RL = 100 kΩ	GBW MHz Typ	Specified Supply Voltage	
							Min V	Max V
Specs at T_A = 25°C and Vs = +5V								
Duals Continued								
LMC6582A	700	1	80	−0.3 to 5.3	0.05 to 4.9	1.2	1.8	10
LMC6582	700	3	80	−0.3 to 5.3	0.05 to 4.9	1.2	1.8	10
LMC6682A	700	1	80	−0.3 to 5.3	0.05 to 4.9	1.2	1.8	10
LMC6682	700	3	80	−0.3 to 5.3	0.05 to 4.9	1.2	1.8	10
LMC6142A	650	1	170*		0.005 to 4.995	17	2.7	24
Quads								
LMC6044A	10	3	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15
LMC6044	10	6	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15
LMC6064A	16	0.35	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LMC6064	16	0.8	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LMC6464	20	3	150	−0.2 to 5.3	0.05 to 4.995	0.05	3	15
LMC6464A	20	0.5	150	−0.2 to 5.3	0.05 to 4.995	0.05	3	15
LPC660A	40	3	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LPC660	40	6	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LMC6024	40	9	40	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LMC660A	375	3	2	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC660	375	6	2	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC6034	375	9	40	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC6084A	450	0.35	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6084	450	0.8	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6484A	500	0.5	20	0 to 5	0.03 to 4.97	1.3	3	15
LMC6484	500	3	20	0 to 5	0.03 to 4.97	1.3	3	15
LMC6494A	500	3	150	−0.3 to 5.3	0.02 to 4.98	1.5	5	15
LMC6494	500	3	150	−0.3 to 5.3	0.02 to 4.98	1.5	5	15
LMC6144A	650	1	170*	−0.25 to 5.3	0.005 to 4.995	1.7	2.7	24
LMC6584A	700	1	80	−0.3 to 5.3	0.05 to 4.9	1.2	1.8	10
LMC6584	700	3	80	−0.3 to 5.3	0.05 to 4.9	1.2	1.8	10
LMC6684A	700	1	80	−0.3 to 5.3	0.05 to 4.9	1.2	1.8	10
LMC6684	700	3	80	−0.3 to 5.3	0.05 to 4.9	1.2	1.8	10

*nA

Medium and High Power Operational Amplifier Selection Guide ($\geq$ 0.1A Output) ($T_A = 25°C$, Note 1)

Part #	I_{OUT} A (Typ)	V_{OS} mV (Max)	I_S mA (Max)	Slew Rate V/μS (Typ)	PBW (Typ)
LM6181	0.1	7.0	10	2000	60 MHz
LM6182	0.1 (Dual)	7.0	20	2000	60 MHz
LH0041	0.2	3	3.5	3	20 kHz
LH0101A	2.2	3	35	10	300 kHz
LH0101	2.2	10	35	10	300 kHz
LM675	3	10	50	8	*
LM12(L)	(Note 2)	7	80	9	60 kHz
LM12C(L)	(Note 2)	15	120	9	60 kHz
LM7171A	0.1	1	8.5	4100	33 MHz
LM7171	0.1	3	8.5	4100	33 MHz
LM6171A	0.1	3	4	3600	28 MHz
LM6171	0.1	6	4	3600	28 MHz

*Not Specified

Note 1: Refer to Datasheet for conditions and more detailed information.

Note 2: I_{OUT} for the LM12 is dependent on the amount of power dissipated in the output transistor. The datasheet should be referred to, to determine amount of current available.

Low Voltage Selection Guide

Part #	Minimum Supply Voltage	Typical Supply Current (per Device)	Description
LMC6482	3V	500 μA	Dual 1 MHz Rail-to-Rail Amp
LMC6484	3V	500 μA	Quad 1 MHz Rail-to-Rail Amp
LMC7101	2.7V	500 μA	Tiny Pak™ SOT23 1 MHz Rail-to-Rail Amp
LMC7111	2.2V	25 μA	Tiny Pak SOT23 35 kHz Rail-to-Rail Amp
LMC6582	1.8V	700	Dual Low-Voltage, 1.2 MHz Rail-to-Rail Input and Output CMOS Amplifier
LMC6584	1.8V	700	Quad Low-Voltage, 1.2 MHz Rail-to-Rail Input and Output CMOS Amplifiers
LMC6681	1.8V	700 μA	Single Low-Voltage, 1.2 MHz Rail-to-Rail Input and Output CMOS Amplifier with Powerdown
LMC6682	1.8V	700 μA	Dual Low-Voltage, 1.2 MHz Rail-to-Rail Input and Output CMOS Op Amp with Powerdown
LMC6684	1.8V	700 μA	Quad Low-Voltage, 1.2 MHz Rail-to-Rail Input and Output CMOS Amplifiers with Powerdown
LM6142	1.8V	650 μA	Dual 17 MHz Gain-Bandwidth Rail-to-Rail Amp
LM6144	1.8V	650 μA	Quad 17 MHz Gain-Bandwidth Rail-to-Rail Amp
LM7131	3V	7 mA	Video Amp in SOT23 Tiny Pak, 70 MHz Gain-Bandwidth
LM6132	1.8V	360 μA	Dual 7 MHz Gain-Bandwidth Rail-to-Rail Amplifier
LM6134	1.8V	360 μA	Quad 7 MHz Gain-Bandwidth Rail-to-Rail Amplifier
LM6152	1.8V	1500 μA	Dual 45 MHz Gain-Bandwidth Rail-to-Rail Amplifier
LM6154	1.8V	1500 μA	Dual 45 MHz Gain-Bandwidth Rail-to-Rail Amplifier

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Audio Op Amp Selection Guide

Part #	Description Precision Op Amp	Input Referred Noise Voltage	THD	Slew Rate	GBW	PSRR	Supply Range	Single/ Dual/Quad	Package (Pin Count)
LM833	Dual Audio Amplifier	4.5 nV/√Hz	0.002%	7V/μs	15 MHz	100 dB	± 18V	Dual	SO(8), DIP(8)
LM837	Quad Audio Amplifier	4.5 nV/√Hz	0.0015%	10V/μs	25 MHz	100 dB	± 18V	Quad	SO(14), DIP(14)
LF347	Wide Bandwidth JFET	20 nV/√Hz	0.02%	13V/μs	4 MHz	100 dB	± 18V	Quad	DIP(14), SO(14)
LF351	Wide Bandwidth JFET	25 nV/√Hz	0.02%	13V/μs	4 MHz	100 dB	± 18V	Single	SO(8), DIP(8)
LF353	Dual LF351	16 nV/√Hz	0.02%	13V/μs	4 MHz	100 dB	± 18V	Dual	SO(14), DIP(14)
LF411	Low Offset, Low Drift JFET	25 nV/√Hz	0.02%	15V/μs	3 MHz	100 dB	± 18V	Single	DIP(8)
LF412	Dual LF411	25 nV/√Hz	0.02%	15V/μs	3 MHz	100 dB	± 18V	Dual	DIP(8)
LF444	Low Power JFET Quad	35 nV/√Hz	0.02%	1V/μs	1 MHz	100 dB	± 18V	Quad	DIP(14), SO(14)
LM6142	High-Speed/Low Power Dual	16 nV/√Hz	0.03%	5V/μs	17 MHz	87 dB	± 1.8V to 24V	Dual	DIP(8), SO(8)
LM6144	High-Speed/Low Power Quad	16 nV/√Hz	0.03%	5V/μs	17 MHz	87 dB	± 1.8V to 24V	Quad	DIP(14), SO(14)

National Semiconductor

Audio Power Amp Selection Guide

Users Supply Voltage	Part #	Power [THD ≤ 1% (Typ)] Power Specified as Continuous RMS			Power [THD ≤ 10% (Typ)] Power Specified as Continuous RMS		
		4Ω	8Ω	16Ω	4Ω	8Ω	16Ω
5V $(V_S = 6V)$	LM1896	0.7W	0.45W	NA	1.1W	1.3W	NA
12V	LM1877	1.5W	1.0W	0.55W	1.75W	1.3W	0.75W
	LM2877	1.5W	1.0W	0.55W	1.75W	1.3W	0.75W
	LM2878	1.5W	1.0W	0.55W	2.0W	1.3W	0.75W
14V	LM1877	2.0W	1.3W	0.85W	2.5W	1.75W	1.0W
	LM2877	2.0W	1.3W	0.85W	2.75W	1.75W	1.0W
	LM2878	2.0W	1.3W	0.85W	2.75W	1.75W	1.0W
	LM2879	NA	1.25W	NA	NA	2W	NA
20V and Above							
$(V_S = 20V)$	LM1877	2.0W	2.0W	NA	2.5W	3.0W	NA
$(V_S = 20V)$	LM2877	2.5W	3.0W	1.75W	3.7	4.25W	2.3W
$(V_S = 20V)$	LM2878	NA	4.0W	NA	NA	4.75W	NA
$(V_S = 28V)$	LM2879	NA	7.0W	NA	NA	8W	NA
$(V_S = \pm 25V)$	LM1875	20W	20W	NA	25W	30W	NA
$(V_S = \pm 35V)$	LM3875	45W ($V_S = \pm 25V$	56W	30W	56W ($V_S = \pm 25V$)	70W	39W
$(V_S = \pm 35V)$	LM3876	45W ($V_S = \pm 25V$	56W	30W	56W ($V_S = \pm 25V$)	70W	39W
$(V_S = \pm 35V)$	LM3886	68W ($V_S = \pm 28V$	63W	33W	87W ($V_S = \pm 28V$)	78W	41W

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Typical THD Ratings

Typical THD Ratings	THD Measurements Conditions	Supply Range (V)	Single/ Dual	Package (Pin Count)
0.72%	Po = 1W @ V_S = 5V	2.7V to 5.5V	Single	SO(16)
0.45%	Po = 0.5W @ V_S = 5V	2.7V to 5.5V	Single	SO(8)
0.72%	Po = 1W @ V_S = 5V	2.7V to 5.5V	Single	SO(16)
0.45%	Po = 0.5W @ V_S = 5V	2.7V to 5.5V	Single	SO(8)
0.11%	Po = 0.5W @ V_S = 6V	3V to 10V	Dual	DIP(14)
0.055%	Po = 1W @ V_S = 14V	6V to 24V	Dual	DIP(14), SO(14)
0.07%	Po = 1W @ V_S = 14V	6V to 24V	Dual	SIP(11)
0.14%	Po = 2W @ V_S = 22V	6V to 32V	Dual	SIP(11)
0.14%	Po = 1W @ V_S = 12V	3V to 15V	Dual	SIP(11)
0.055%	Po = 1W @ V_S = 14V	6V to 24V	Dual	DIP(14), SO(14)
0.07%	Po = 1W @ V_S = 1W	6V to 24V	Dual	SIP(11)
0.15%	Po = 2W @ V_S = 22V	6V to 32V	Dual	SIP(11)
0.05%	Po = 1W @ V_S = 12V	6V to 32V	Dual	TO-220(11)
0.02%	Po = 20W @ V_S = ±25V	16V to 60V	Single	TO-220(5)
0.06%	Po = 25W @ V_S = ±30V	20V to 60V	Single	TO-220(11)**
0.06%	Po = 40W @ V_S = ±35V	20V to 84V	Single	TO-220(11)**
0.06%	Po = 40W @ V_S = ±35V	20V to 84V	Single	TO-220(11)**
0.03%	Po = 60W @ V_S = ±28V	20V to 84V	Single	TO-220(11)**

**Isolated packages available.

Special Amplifier Selection Guide

Amplifiers with Added Functions

Featuring the new Super-Block™ family, these amplifiers have additional special functions within their packages which help minimize the number of components required in an application. These devices are often used in control circuits, power supplies, and automatic test systems.

LM10	Op Amp and Adjustable Voltage Reference
LM392	Op Amp and Comparator
LM611	Super-Block Op Amp and Adjustable Voltage Reference
LM613	Super-Block Dual Op Amp, Dual Comparator, and Adjustable Voltage Reference
LM614	Super-Block Quad Op Amp and Adjustable Voltage Reference

Transconductance Amplifiers (Voltage In, Current Out)

These amplifiers provide a transconductance (g_m) proportional to their bias current, which is controlled externally. This programmable gain makes the amplifiers useful in applications such as voltage-controlled amplifiers, current-controlled amplifiers, AGC circuits, and voltage multipliers.

LM3080	Operational Transconductance Amplifier
LM13600	Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers
LM13700	Improved Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers

Transimpedance Amplifiers (Current In, Voltage Out)

Transimpedance amplifiers are widely used to amplify photo-diode signals, and to ground-reference differential voltage signals which have high common-mode voltages. The LH0082 was designed to receive and amplify analog and digital signals transmitted by fiber optics. Like the LM359, the LH0082 can also be used as a video amplifier. The LM2900 series has found popularity in filter applications, as well as general-purpose amplifiers.

LM359	Dual Current Mode (Norton) Amplifier
LM2900 LM3900 LM3301 LM3401	Quad Current Mode (Norton) Amplifier

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LF147/LF347 Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

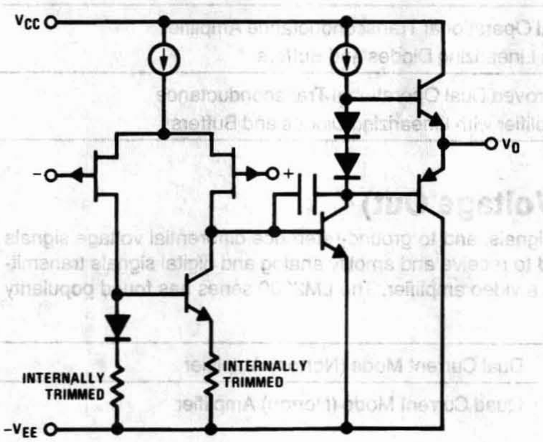
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage	5 mV max
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	7.2 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz − 20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Simplified Schematic

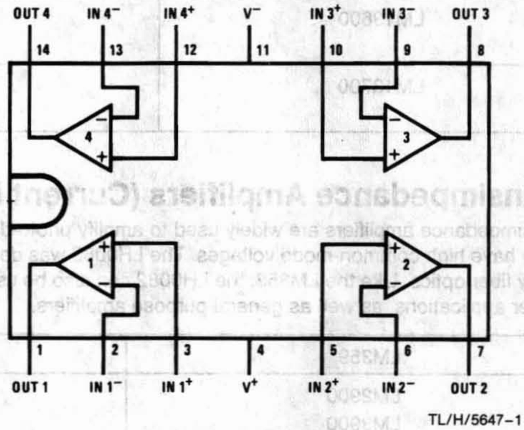
¼ Quad



TL/H/5647–13

Connection Diagram

Dual-In-Line Package



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Top View

Order Number LF147J, LF347M, LF347BN, LF347N, LF147D/883 or LF147J/883*
See NS Package Number D14E, J14A, M14A or N14A

*Available per SMD #8102306, JM38510/11906.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
Power Dissipation (Notes 3 and 9)	900 mW	1000 mW
T_j max	150°C	150°C
θ_{jA}		
Cavity DIP (D) Package		80°C/W
Ceramic DIP (J) Package		70°C/W
Plastic DIP (N) Package		75°C/W
Surface Mount Narrow (M)		100°C/W
Surface Mount Wide (WM)		85°C/W

	LF147	LF347B/LF347
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)		260°C
Small Outline Package		
Vapor Phase (60 seconds)		215°C
Infrared (15 seconds)		220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10) 900V

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$		1	5		3	5		5	10	mV
		Over Temperature			8			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10			10			10		μV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 5, 6)		25	100		25	100		25	100	pA
		Over Temperature			25			4			4	nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 5, 6)		50	200		50	200		50	200	pA
		Over Temperature			50			8			8	nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\ k\Omega$	50	100		50	100		25	100		V/mV
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		±11	+15 −12		±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, $f = 1\ Hz - 20\ kHz$ (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	8	13		8	13		8	13		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	2.2	4		2.2	4		2.2	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, $f = 1000\ Hz$		20			20			20		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, $f = 1000\ Hz$		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF147 is available in the military temperature range $-55°C \le T_A \le 125°C$, while the LF347B and the LF347 are available in the commercial temperature range $0°C \le T_A \le 70°C$. Junction temperature can rise to T_j max = 150°C.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF147 and for $V_S = \pm 15V$ for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5V$ to $\pm 15V$ for the LF347 and LF347B and from $V_S = \pm 20V$ to $\pm 5V$ for the LF147.

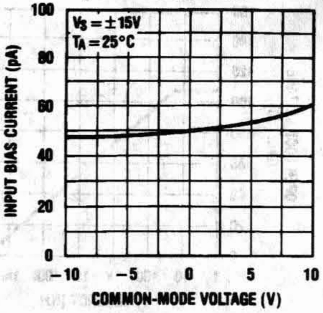
Note 8: Refer to RETS147X for LF147D and LF147J military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

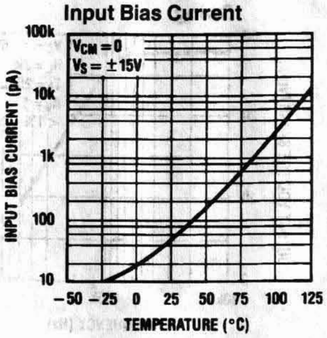
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

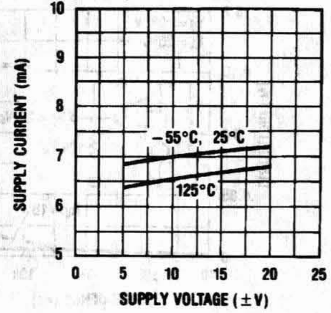
Input Bias Current



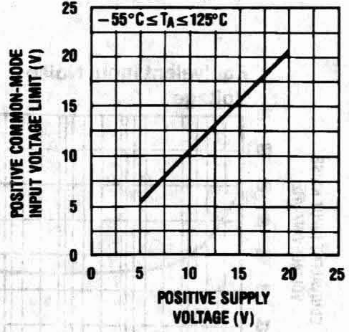
Input Bias Current



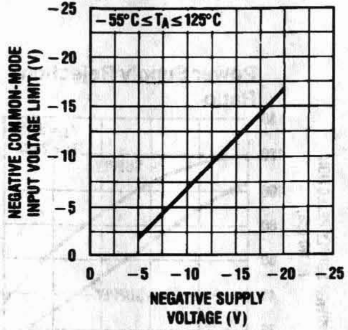
Supply Current



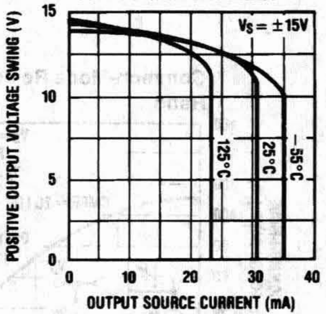
Positive Common-Mode Input Voltage Limit



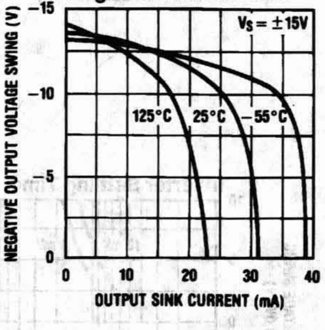
Negative Common-Mode Input Voltage Limit



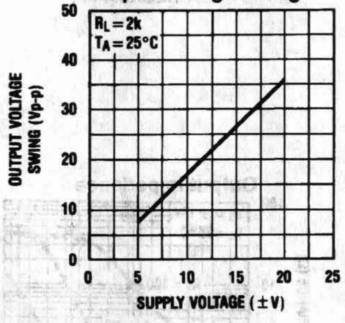
Positive Current Limit



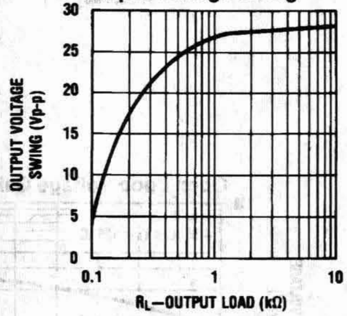
Negative Current Limit



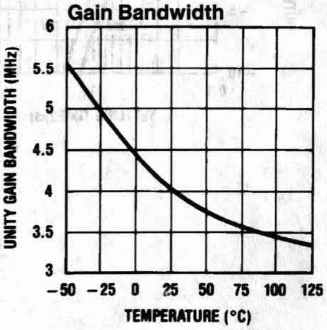
Output Voltage Swing



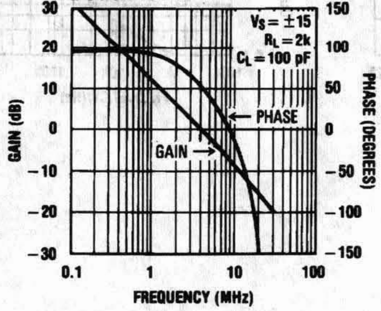
Output Voltage Swing



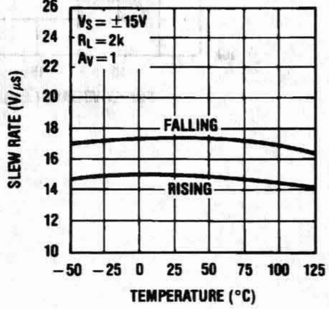
Gain Bandwidth



Bode Plot



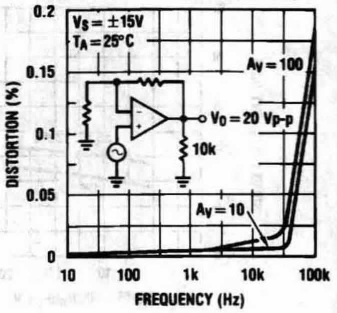
Slew Rate



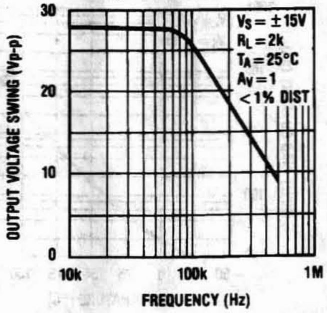
TL/H/5647–2

Typical Performance Characteristics (Continued)

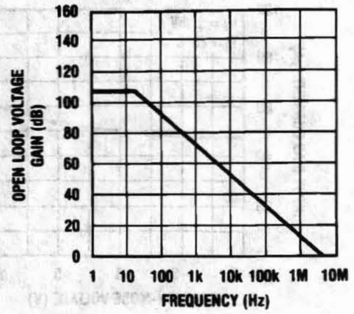
Distortion vs Frequency



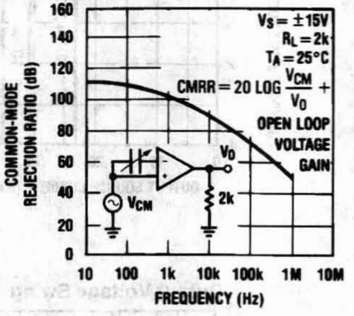
Undistorted Output Voltage Swing



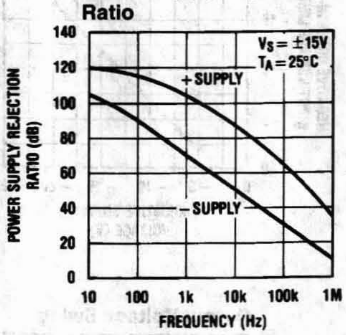
Open Loop Frequency Response



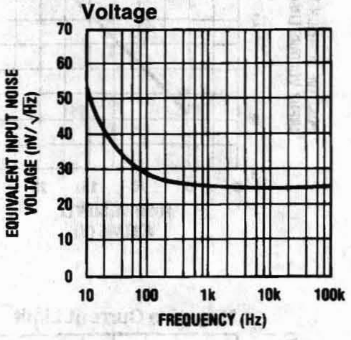
Common-Mode Rejection Ratio



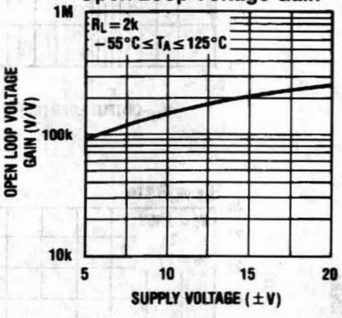
Power Supply Rejection Ratio



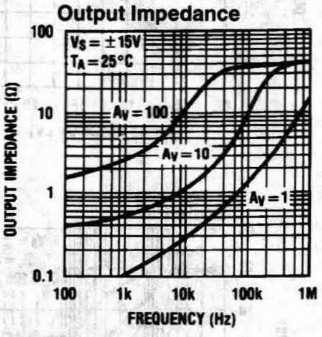
Equivalent Input Noise Voltage



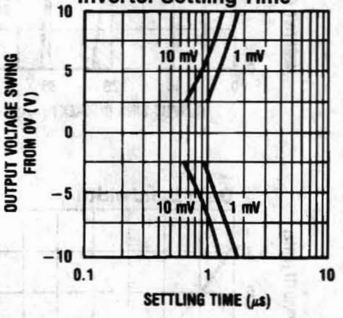
Open Loop Voltage Gain



Output Impedance



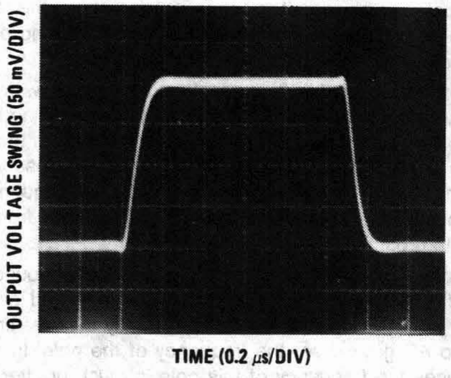
Inverter Settling Time



TL/H/5647–3

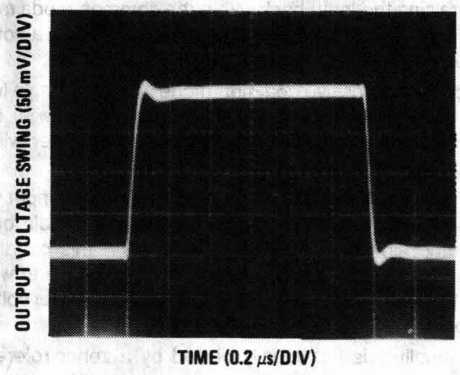
Pulse Response $R_L = 2\ k\Omega$, $C_L = 10\ pF$

Small Signal Inverting



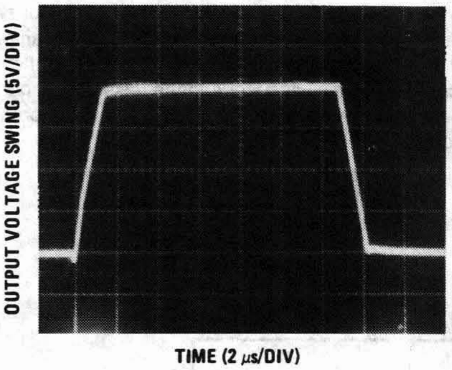
TL/H/5647-4

Small Signal Non-Inverting



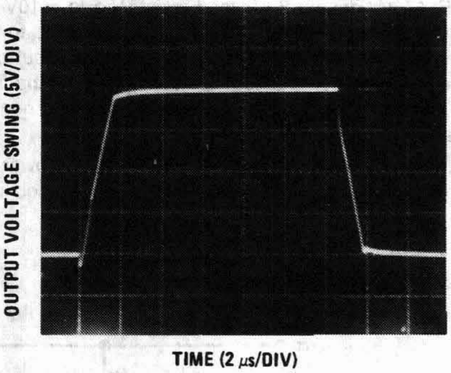
TL/H/5647-5

Large Signal Inverting



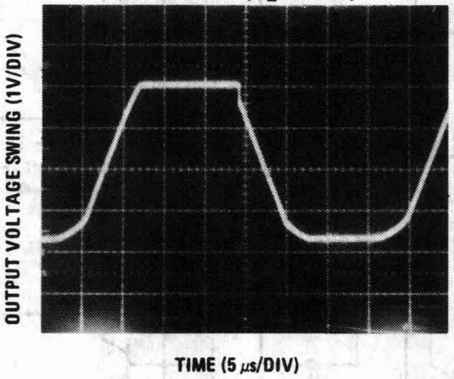
TL/H/5647-6

Large Signal Non-Inverting



TL/H/5647-7

Current Limit ($R_L = 100\Omega$)



TL/H/5647-8

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier

Application Hints (Continued)

output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

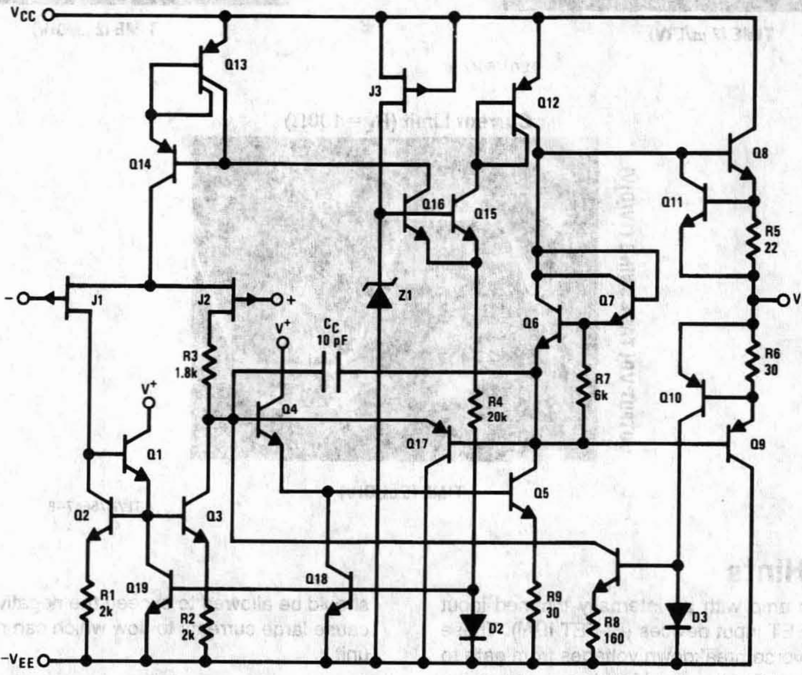
The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

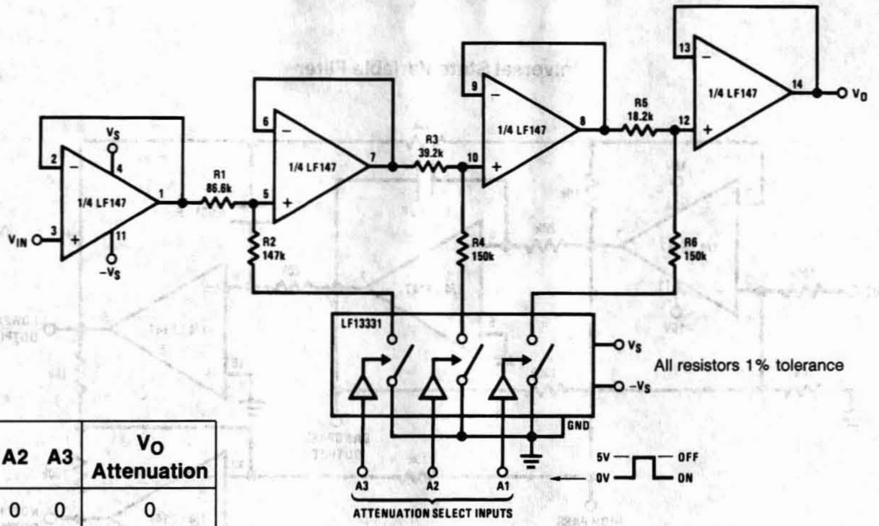
Detailed Schematic



TL/H/5647-9

Typical Applications

Digitally Selectable Precision Attenuator



V_S
2
4
1/4 LF147
1
3
11
V_{IN}
−V_S
R1 86.6k
6
5
1/4 LF147
7
R2 147k
R3 39.2k
9
10
1/4 LF147
8
R4 150k
R5 18.2k
13
12
1/4 LF147
14
V_O
R6 150k
LF13331
V_S
−V_S
GND
A3
A2
A1
ATTENUATION SELECT INPUTS
5V OFF
0V ON

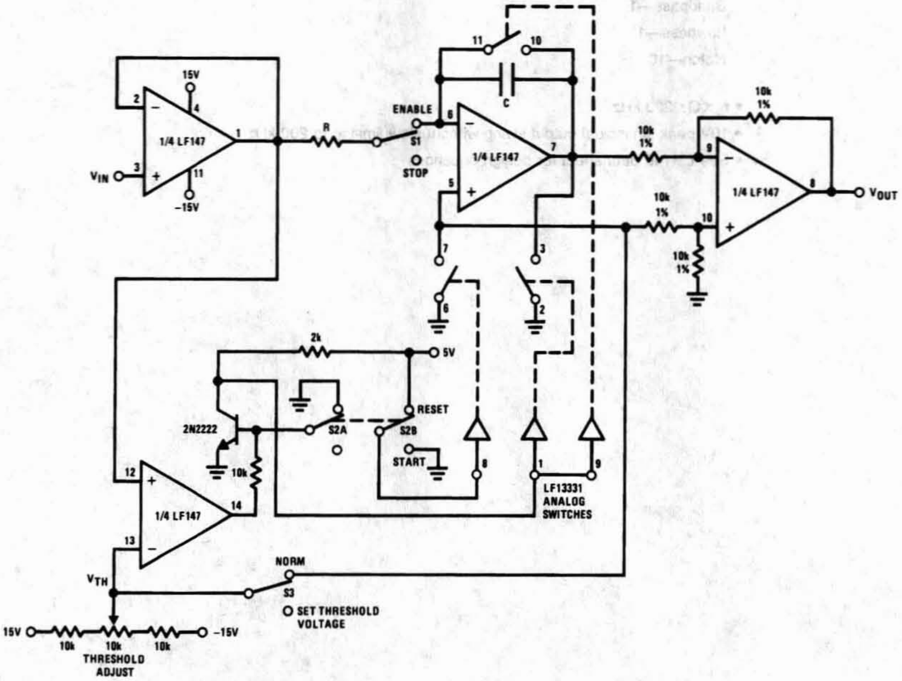
All resistors 1% tolerance

TL/H/5647-10

A1	A2	A3	V_O Attenuation
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



15V
2
4
1/4 LF147
1
V_{IN}
3
11
−15V
R
ENABLE
S1
STOP
11
10
C
6
5
1/4 LF147
7
10k 1%
10k 1%
9
10
1/4 LF147
8
V_{OUT}
10k 1%
10k 1%
7
6
3
2
2k
5V
2N2222
S2A
S2B
RESET
START
10k
8
1
9
LF13331 ANALOG SWITCHES
12
14
1/4 LF147
13
V_{TH}
NORM
S3
SET THRESHOLD VOLTAGE
15V
10k
10k
10k
−15V
THRESHOLD ADJUST

TL/H/5647-11

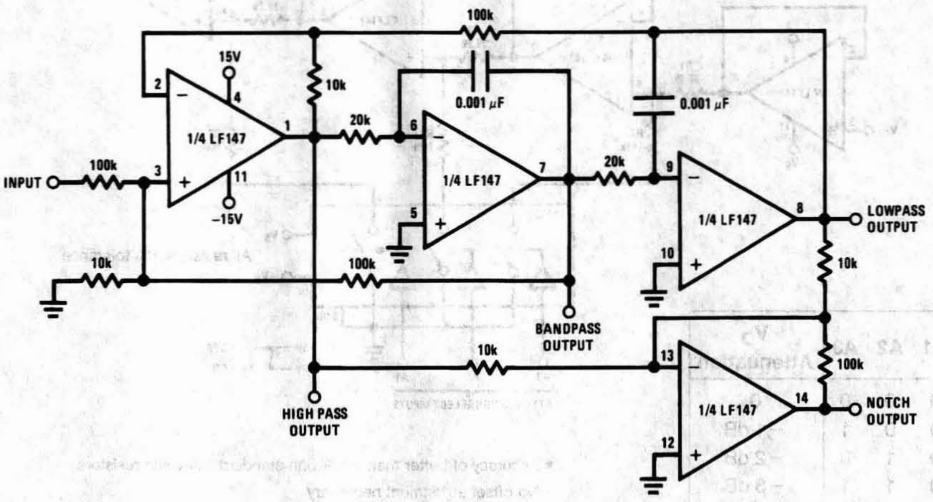
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT}=\frac{1}{RC}\int_0^t (V_{IN}-V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Typical Applications (Continued)

Universal State Variable Filter


100k
15V
10k
0.001 μF
0.001 μF
2
4
1/4 LF147
1
20k
6
INPUT
100k
3
11
−15V
1/4 LF147
7
20k
9
5
1/4 LF147
8
LOWPASS OUTPUT
10
10k
10k
100k
BANDPASS OUTPUT
10k
13
100k
HIGH PASS OUTPUT
1/4 LF147
14
NOTCH OUTPUT
12

TL/H/5647-12

For circuit shown:

$f_o = 3$ kHz, $f_{NOTCH} = 9.5$ kHz

$Q = 3.4$

Passband gain:
  Highpass—0.1
  Bandpass—1
  Lowpass—1
  Notch—10

- $f_o \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

National Semiconductor

LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

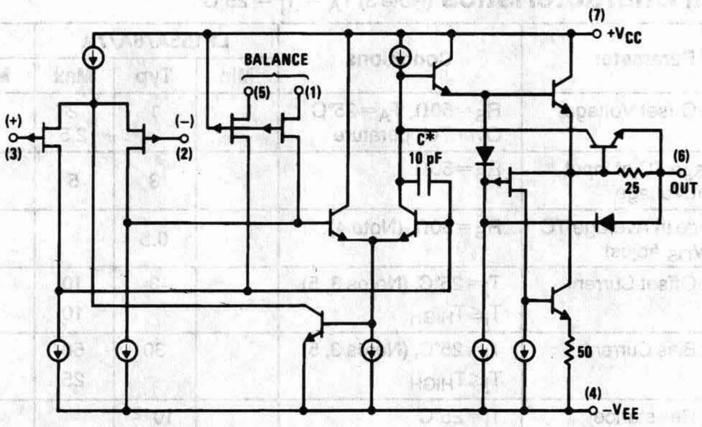
(LF155A, LF156A, LF157A)

■ Low input bias current	30 pA
■ Low Input Offset Current	3 pA
■ High input impedance	$10^{12}\Omega$
■ Low input offset voltage	1 mV
■ Low input offset voltage temp. drift	3 μV/°C
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ High common-mode rejection ratio	100 dB
■ Large dc voltage gain	106 dB

Uncommon Features

	LF155A	LF156A	LF157A ($A_V = 5$)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	V/μs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	nV/$\sqrt{\text{Hz}}$

Simplified Schematic



*3 pF in LF157 series.

TL/H/5646–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 8)

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7	LF355/6/7 LF355A/6A/7A
Supply Voltage	±22V	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
T_{jMAX}				
H-Package	150°C	150°C	115°C	115°C
N-Package			100°C	100°C
M-Package			100°C	100°C
Power Dissipation at $T_A = 25°C$ (Notes 1 and 9)				
H-Package (Still Air)	560 mW	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1200 mW	1000 mW	1000 mW
N-Package			670 mW	670 mW
M-Package			380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}				
H-Package (Still Air)	160°C/W	160°C/W	160°C/W	160°C/W
H-Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W	65°C/W
N-Package			130°C/W	130°C/W
M-Package			195°C/W	195°C/W
(Typical) θ_{JC}				
H-Package	23°C/W	23°C/W	23°C/W	23°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Soldering Information (Lead Temp.)				
Metal Can Package				
Soldering (10 sec.)	300°C	300°C	300°C	300°C
Dual-In-Line Package				
Soldering (10 sec.)		260°C	260°C	260°C
Small Outline Package				
Vapor Phase (60 sec.)			215°C	215°C
Infrared (15 sec.)			220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7	LF355/6/7 LF355A/6A/7A
ESD tolerance				
(100 pF discharged through 1.5 kΩ)	1000V	1000V	1000V	1000V

DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ Over Temperature		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	10 10		3	10 1	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	50 25		30	50 5	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$ $V_O = \pm10V$, $R_L = 2k$ Over Temperature	50 25	200		50 25	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$ $V_S = \pm15V$, $R_L = 2k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V

DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$ (Continued)

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12		±11	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = T_j = 25°C$, $V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155A/355A			LF156A/356A			LF157A/357A			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	LF155A/6A; $A_V = 1$, LF157A; $A_V = 5$	3	5		10	12		40	50		V/μs V/μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		25 20			15 12			15 12		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz f = 1000 Hz		0.01 0.01			0.01 0.01			0.01 0.01		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3			3			3		pF

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ Over Temperature		3	5 7		3	5 6.5		3	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	20 20		3	20 1		3	50 2	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	100 50		30	100 5		30	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2k$ Over Temperature	50 25	200		50 25	200		25 15	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$ $V_S = \pm 15V$, $R_L = 2k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12		±11	±15.1 −12		+10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = T_j = 25°C, V_S = \pm 15V$

Parameter	LF155A/155, LF255, LF355A/355B		LF355		LF156A/156, LF256/356B		LF356A/356		LF157A/157 LF257/357B		LF357A/357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = T_j = 25°C, V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155/255/ 355/355B	LF156/256, LF356B	LF156/256/ 356/356B	LF157/257, LF357B	LF157/257/ 357/357B	Units
			Typ	Min	Typ	Min	Typ	
SR	Slew Rate	LF155/6: $A_V=1$, LF157: $A_V=5$	5	7.5	12	30	50	V/μs V/μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S=100\Omega$ f=100 Hz f=1000 Hz	25 20		15 12		15 12	nV/√Hz nV/√Hz
i_n	Equivalent Input Current Noise	f=100 Hz f=1000 Hz	0.01 0.01		0.01 0.01		0.01 0.01	pA/√Hz pA/√Hz
C_{IN}	Input Capacitance		3		3		3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d=(T_{jMAX}-T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A/6A/7A LF155//6/7	LF255//6/7	LF355A/6A/7A	LF355B/6B/7B	LF355//6/7
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 18V$	$\pm 15V \le V_S \pm 20V$	$V_S = \pm 15V$
T_A	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM}=0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j=T_A+\theta_{jA}$ Pd where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V=-5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit).

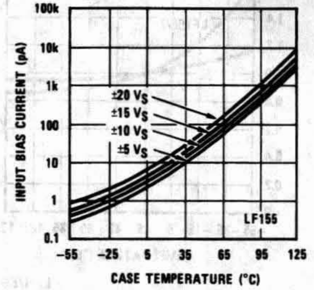
Note 8: Refer to RETS155AX for LF155A, RETS155X for LF155, RETS156AX for LF156A, RETS156X for LF156, RETS157A for LF157A and RETS157X for LF157 military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

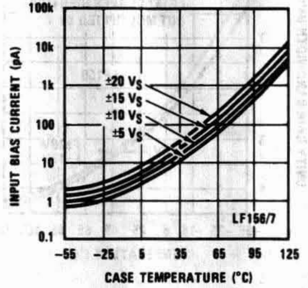
Typical DC Performance Characteristics

Curves are for LF155, LF156 and LF157 unless otherwise specified.

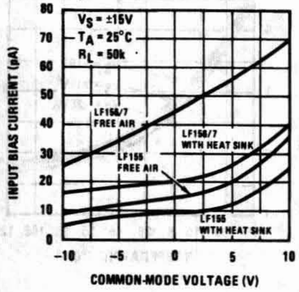
Input Bias Current



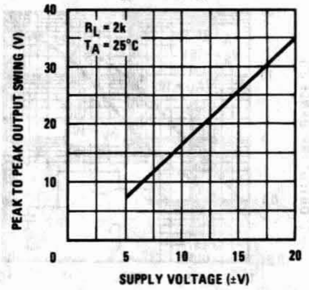
Input Bias Current



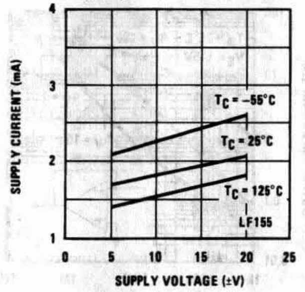
Input Bias Current



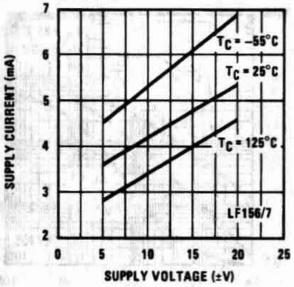
Voltage Swing



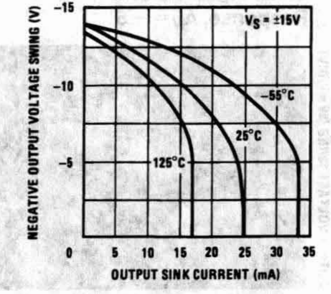
Supply Current



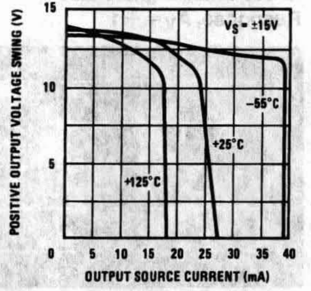
Supply Current



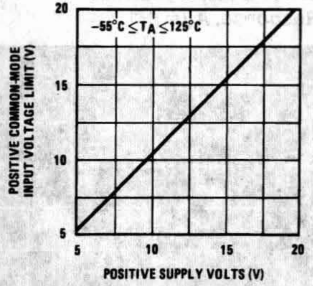
Negative Current Limit



Positive Current Limit

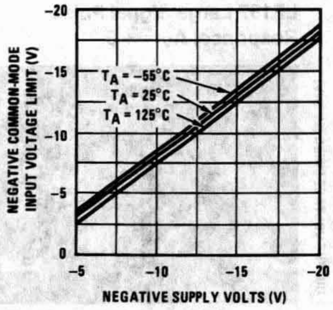


Positive Common-Mode Input Voltage Limit

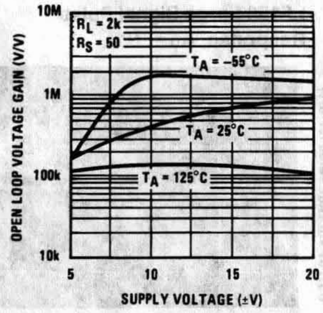


TL/H/5646–2

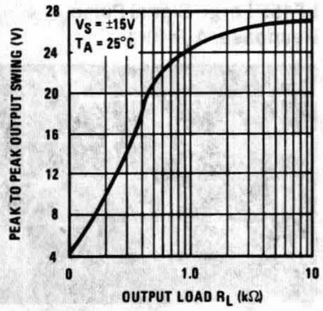
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



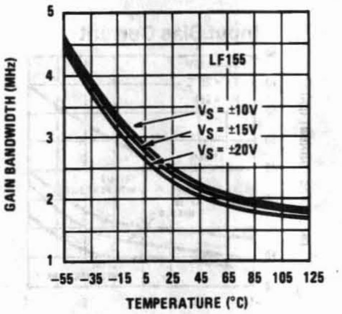
Output Voltage Swing



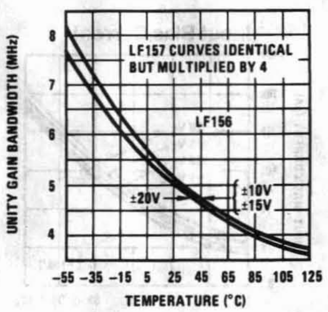
TL/H/5646–3

Typical AC Performance Characteristics

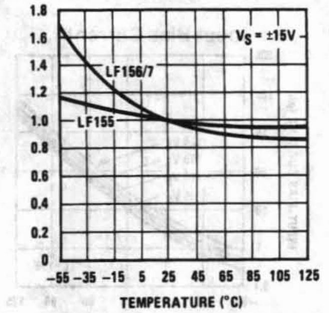
Gain Bandwidth



Gain Bandwidth

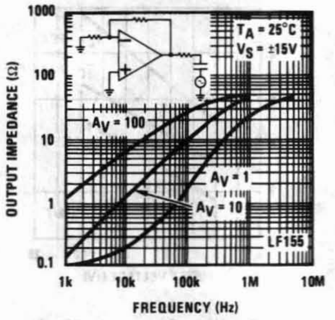


Normalized Slew Rate

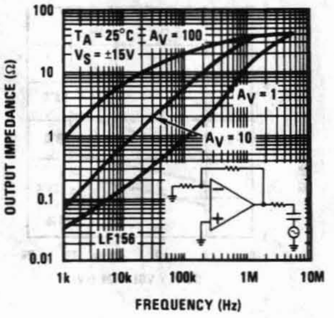


TL/H/5646-4

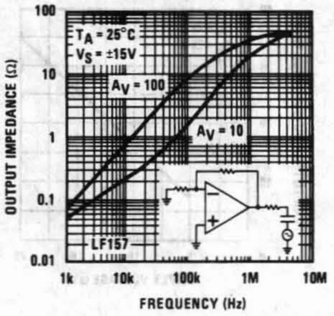
Output Impedance



Output Impedance

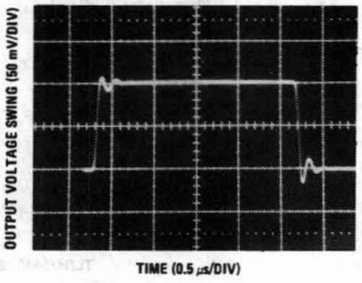


Output Impedance



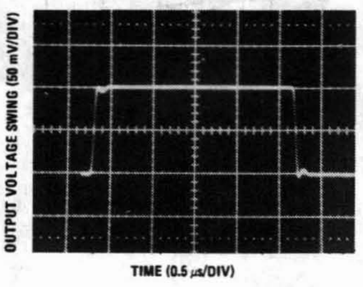
TL/H/5646-12

LF155 Small Signal Pulse Response, $A_V = +1$



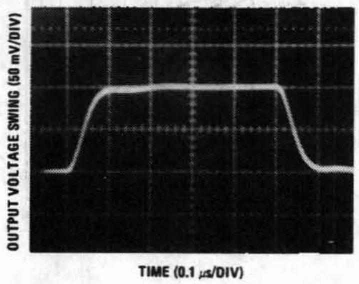
TL/H/5646-5

LF156 Small Signal Pulse Response, $A_V = +1$



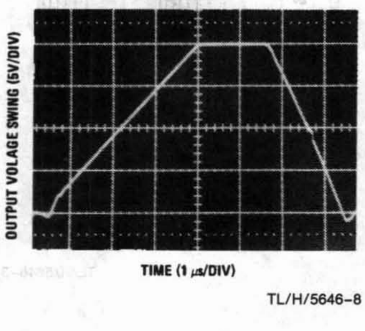
TL/H/5646-6

Small Signal Pulse Response, $A_V = +5$



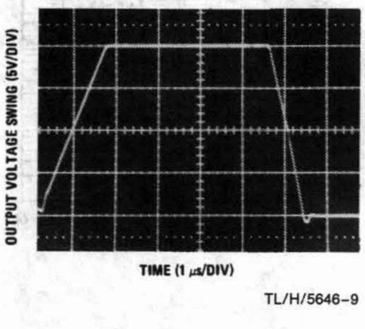
TL/H/5646-7

LF155 Large Signal Pulse Response, $A_V = +1$



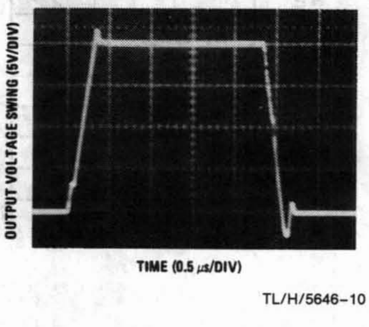
TL/H/5646-8

LF156 Large Signal Pulse Response, $A_V = +1$



TL/H/5646-9

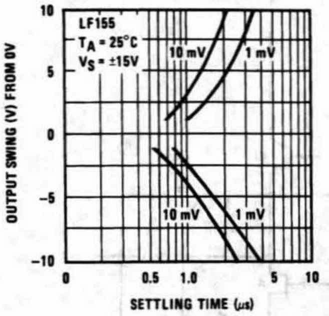
LF157 Large Signal Pulse Response, $A_V = +5$



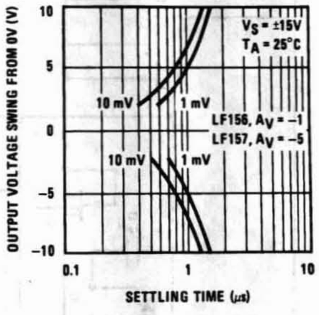
TL/H/5646-10

Typical AC Performance Characteristics (Continued)

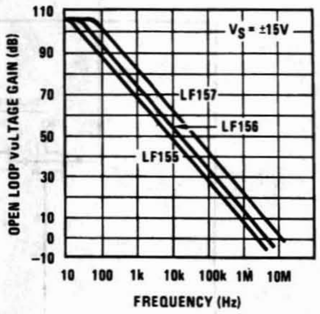
Inverter Settling Time



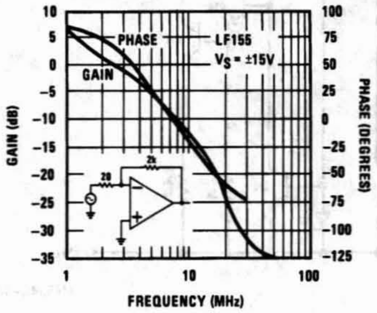
Inverter Settling Time



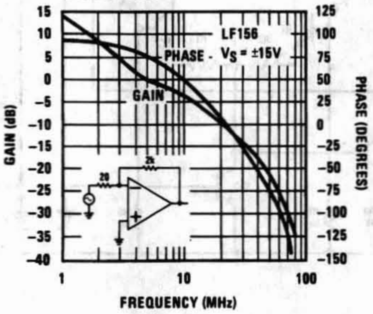
Open Loop Frequency Response



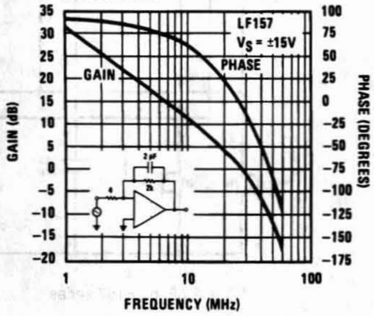
Bode Plot



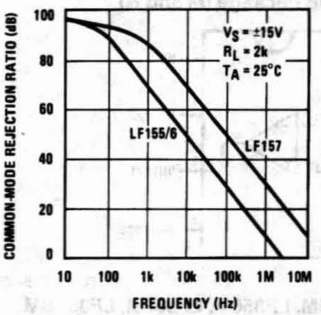
Bode Plot



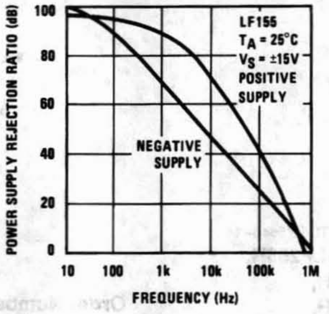
Bode Plot



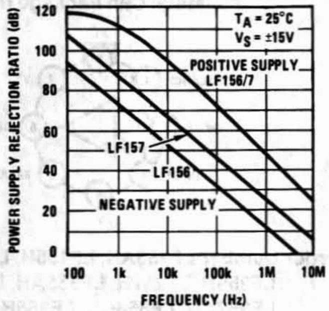
Common-Mode Rejection Ratio



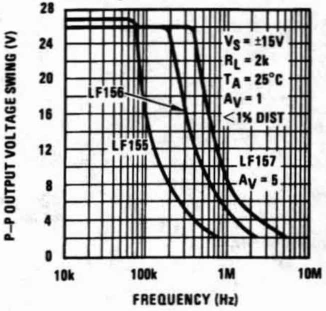
Power Supply Rejection Ratio



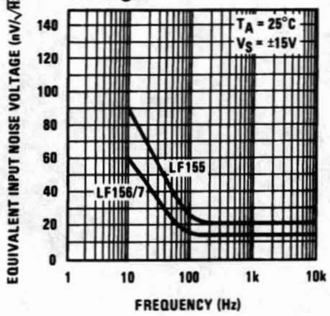
Power Supply Rejection Ratio



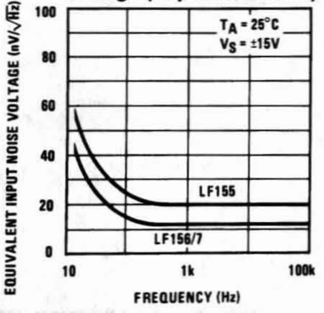
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage

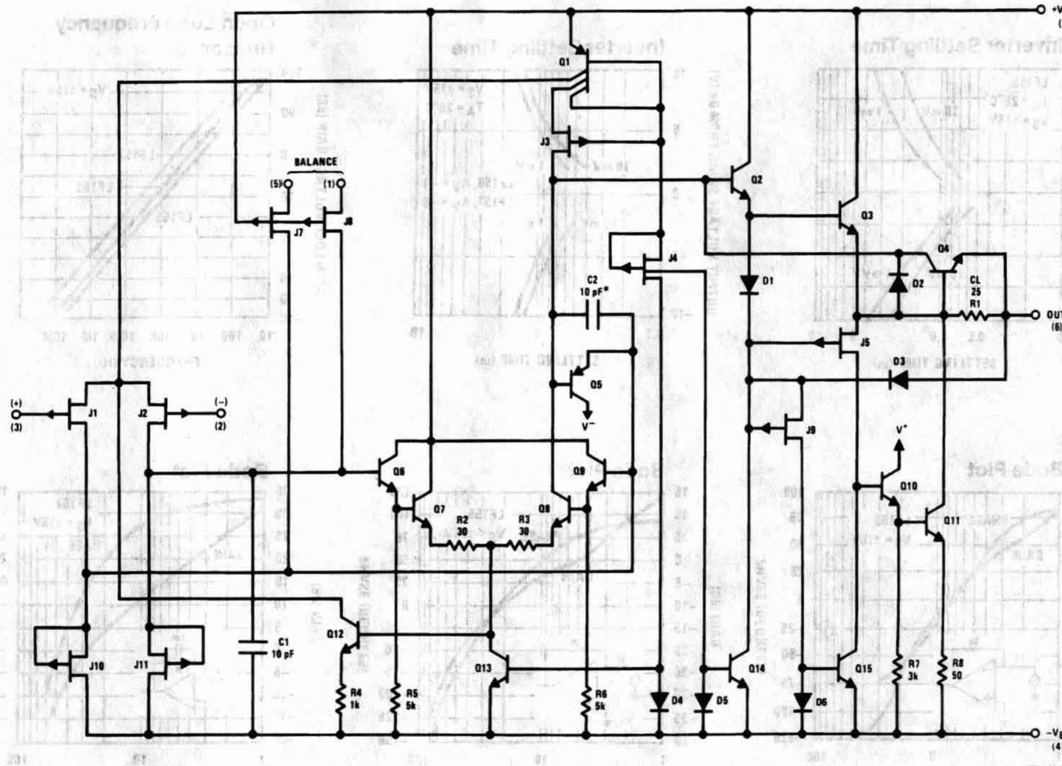


Equivalent Input Noise Voltage (Expanded Scale)



TL/H/5646–11

Detailed Schematic

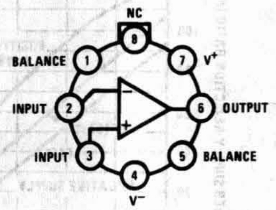

+V_{CC}
(7)
Q1
J3
BALANCE
(5)
(1)
J7
J8
Q2
Q3
Q4
D1
D2
CL
25
R1
OUT
(6)
J4
C2
10 pF*
J5
D3
Q5
V−
(+)
(3)
J1
J2
(−)
(2)
J9
V+
Q10
Q11
Q6
Q7
Q8
Q9
R2
30
R3
30
C1
10 pF
Q12
Q13
Q14
Q15
R4
1k
R5
5k
R6
5k
D4
D5
D6
R7
3k
R8
50
J10
J11
−V_{EE}
(4)

*C = 3 pF in LF157 series.

TL/H/5646-13

Connection Diagrams (Top Views)

Metal Can Package (H)

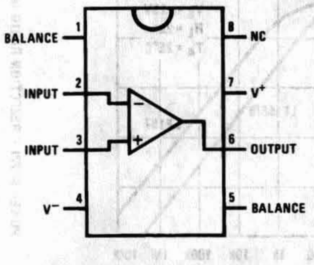

NC
8
7
V+
BALANCE
1
INPUT
2
6
OUTPUT
INPUT
3
5
BALANCE
4
V−

TL/H/5646-14

Order Number LF156AH, LF155H, LF156H, LF255H, LF256H, LF257H, LF355AH, LF356AH, LF357AH, LF356BH, LF355H, LF356H, LF357H, LM155AH/883, LM155H/883, LM156AH/883, LM156H/883, LM157AH/883 or LM157H/883*

See NS Package Number H08C

Dual-In-Line Package (M and N)


BALANCE
1
INPUT
2
INPUT
3
V−
4
8
NC
7
V+
6
OUTPUT
5
BALANCE

TL/H/5646-29

Order Number LF355M, LF356M, LF357M, LF355BM, LF356BM, LF355BN, LF356BN, LF357BN, LF355N, LF356N or LF357N

See NS Package Number M08A or N08E

*Available per JM38510/11401 or JM38510/11402

Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

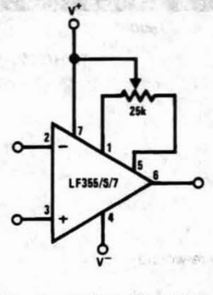
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

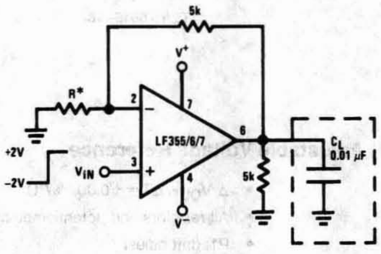
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 µV/°C/mV of adjustment
- Typical overall drift: 5 µV/°C ±(0.5 µV/°C/mV of adj.)

Driving Capacitive Loads



*LF155/6 R = 5k

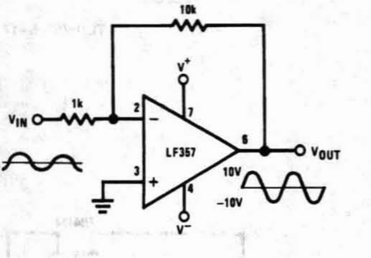
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \cong 0.01$ µF.

Overshoot ≤ 20%

Settling time $(t_s) \cong 5$ µs

LF157. A Large Power BW Amplifier

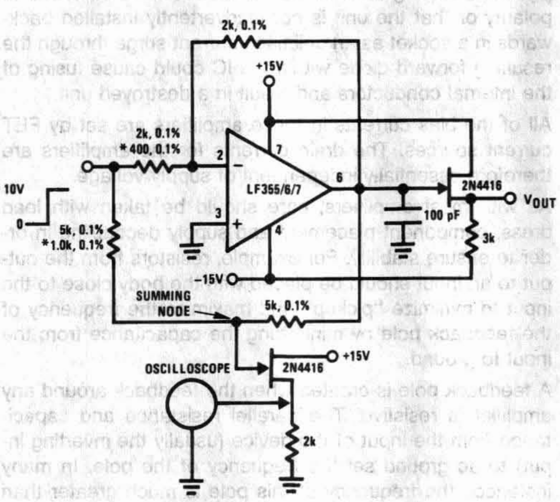


TL/H/5646–15

For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.

Typical Applications

Settling Time Test Circuit

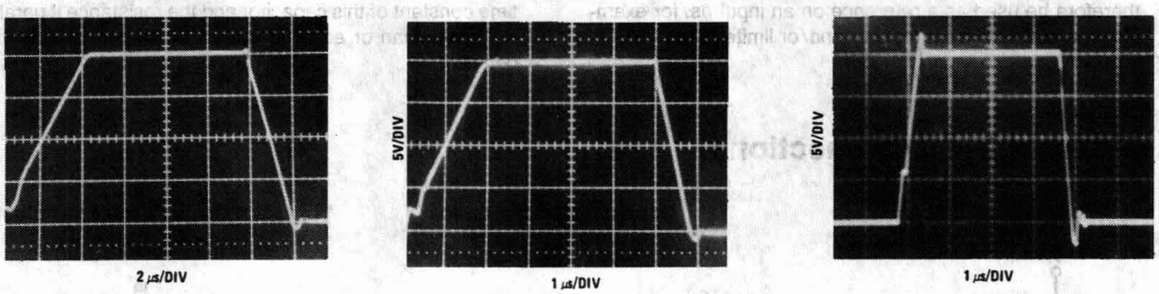


2k, 0.1%
+15V
2k, 0.1%
* 400, 0.1%
2
7
6
LF355/6/7
2N4416
VOUT
10V
0
5k, 0.1%
* 1.0k, 0.1%
3
4
100 pF
3k
−15V
SUMMING NODE
5k, 0.1%
OSCILLOSCOPE
2N4416
+15V
2k

- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

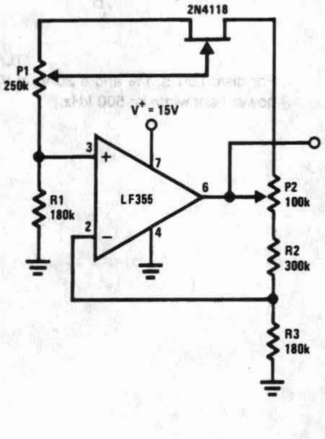
TL/H/5646–16

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



TL/H/5646–17 TL/H/5646–18 TL/H/5646–19

Low Drift Adjustable Voltage Reference



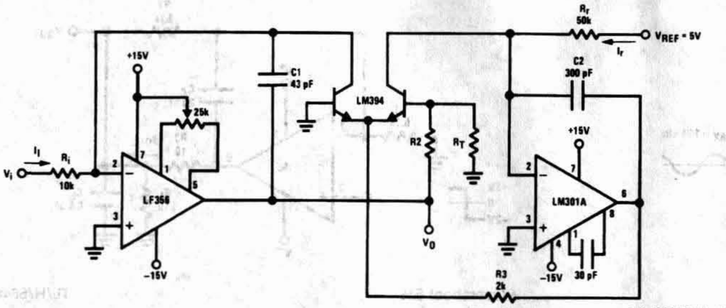
2N4118
P1
250k
V+ = 15V
3
7
6
VOUT = 10V
LF355
R1
180k
2
4
P2
100k
R2
300k
R3
180k

- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

TL/H/5646–20

Typical Applications (Continued)

Fast Logarithmic Converter



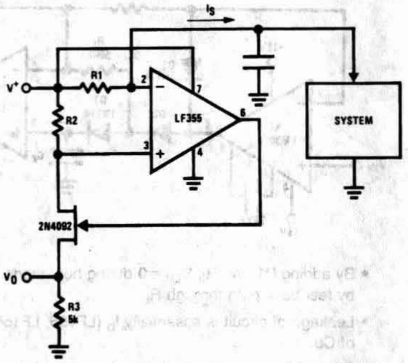
R_r 50k
V_{REF} = 5V
I_r
C1 43 pF
C2 300 pF
LM394
+15V
25k
I_i
R_i 10k
V_i
LF356
−15V
R2
R_T
V_O
LM301A
30 pF
R3 2k
−15V

TL/H/5646-21

- Dynamic range: 100 μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF}\,R_i}\right] = \log V_i \frac{1}{R_i I_r}$$ R2 = 15.7k, R_T = 1k, 0.3%/°C (for temperature compensation)

Precision Current Monitor

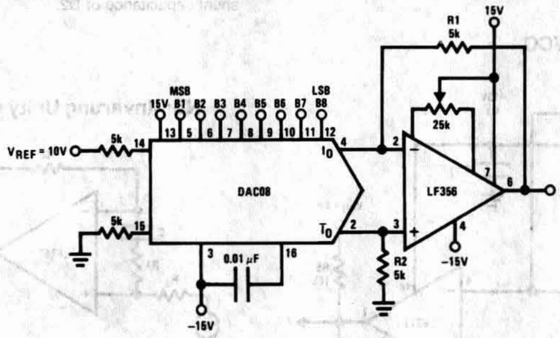


I_S
V⁺
R1
R2
LF355
SYSTEM
2N4092
V_O
R3 5k

TL/H/5646-31

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low Supply Current

8-Bit D/A Converter with Symmetrical Offset Binary Operation



15V
R1 5k
MSB
LSB
15V B1 B2 B3 B4 B5 B6 B7 B8
V_{REF} = 10V
5k
DAC08
I_O
$\overline{I_O}$
0.01 μF
−15V
25k
LF356
E_O
R2 5k
−15V

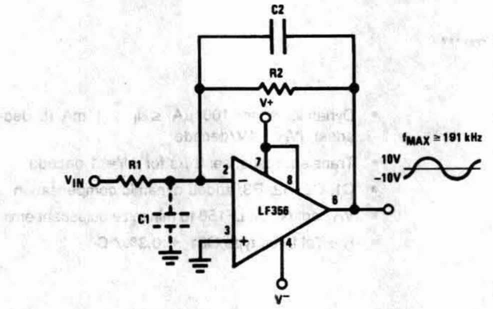
TL/H/5646-32

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

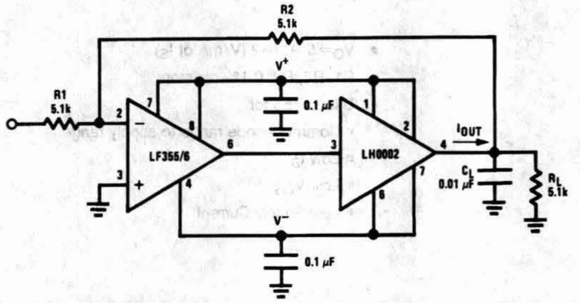
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier


C2
R2
V+
7
8
2
VIN
R1
C1
LF356
6
3
4
V−
fMAX ≅ 191 kHz
10V
−10V

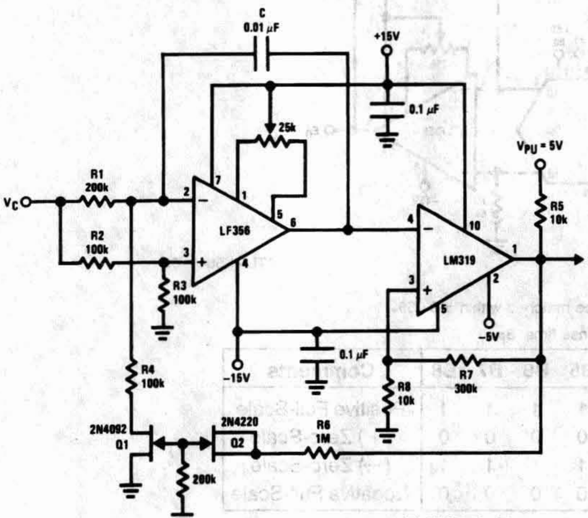
- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 191$ kHz
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156 and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 ≅ R1 C1.

Boosting the LF156 with a Current Amplifier


R2
5.1k
V+
R1
5.1k
2
7
8
0.1 µF
1
2
LF355/6
6
3
LH0002
4
IOUT
CL
0.01 µF
RL
5.1k
3
4
7
6
V−
0.1 µF

- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \ge 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}$ V/µs (with C_L shown)
- No additional phase shift added by the current amplifier

3 Decades VCO

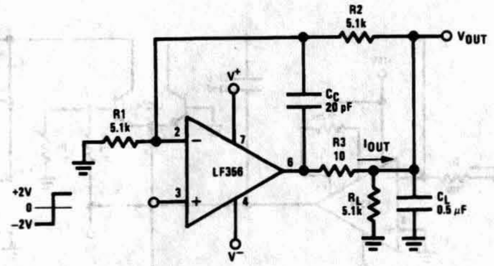

C
0.01 µF
+15V
0.1 µF
25k
VPU = 5V
VC
R1
200k
R2
100k
2
7
1
5
6
3
4
LF356
R5
10k
4
10
LM319
1
f
3
2
5
−5V
R3
100k
0.1 µF
−15V
R4
100k
R8
10k
R7
300k
2N4092
Q1
2N4220
Q2
R6
1M
200k

TL/H/5646-24

$f = \frac{V_C (R8+R7)}{(8\ V_{PU}\ R8\ R1)\ C}$, $0 \le V_C \le 30V$, 10 Hz ≤ f ≤ 10 kHz

R1, R4 matched. Linearity 0.1% over 2 decades.

Isolating Large Capacitive Loads

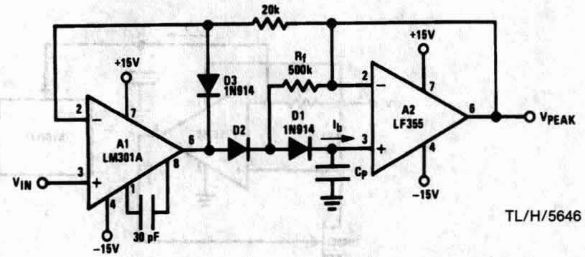

R2
5.1k
VOUT
V+
CC
20 pF
R1
5.1k
2
7
LF356
6
R3
10
IOUT
+2V
0
−2V
3
4
RL
5.1k
CL
0.5 µF
V−

TL/H/5646-22

- Overshoot 6%
- t_s 10 µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}$ V/µs = 0.04 V/µs (with C_L shown)

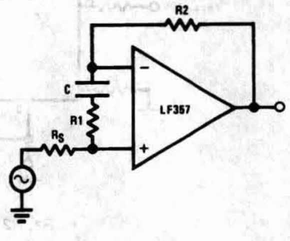
Low Drift Peak Detector


20k
+15V
Rf
500k
+15V
D3
1N914
2
7
A2
LF355
6
VPEAK
2
7
A1
LM301A
6
D2
D1
1N914
Ib
3
Cp
4
−15V
VIN
3
8
4
1
30 pF
−15V

TL/H/5646

- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be << ½π$R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

Non-Inverting Unity Gain Operation for LF157


R2
C
R1
RS
LF357

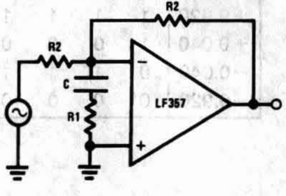
$R1C \ge \frac{1}{(2\pi)\ (5\ MHz)}$

$R1 = \frac{R2 + R_S}{4}$

$A_{V(DC)} = 1$

$f_{-3\ dB} \approx 5$ MHz

Inverting Unity Gain for LF157


R2
R2
C
R1
LF357

$R1C \ge \frac{1}{(2\pi)\ (5\ MHz)}$

$R1 = \frac{R2}{4}$

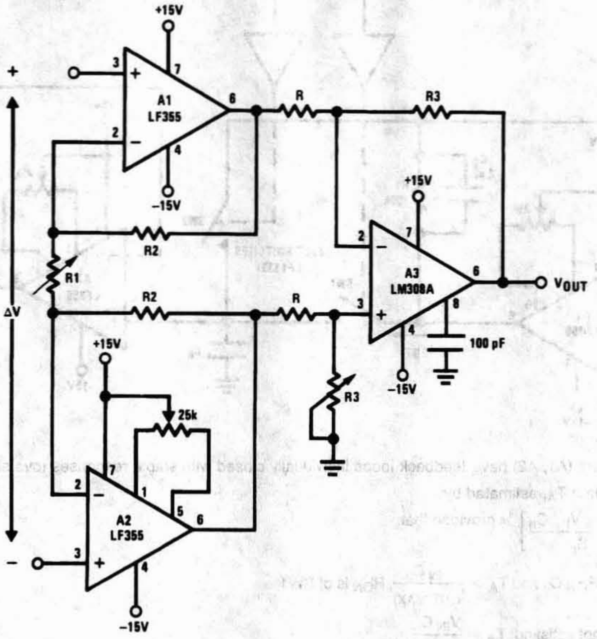
$A_{V(DC)} = -1$

$f_{-3\ dB} \approx 5$ MHz

TL/H/5646-25

Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier

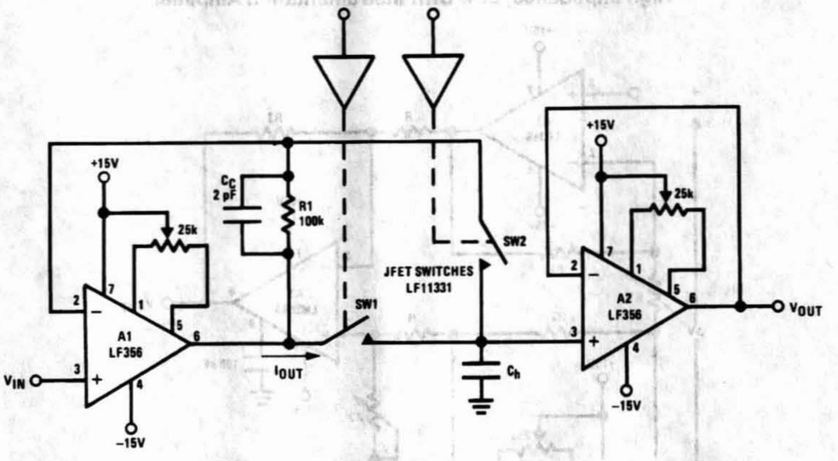

+15V
+
3
7
A1
LF355
6
2
4
−15V
R
R3
+15V
R2
2
7
R1
A3
LM308A
6
VOUT
ΔV
R2
R
3
8
4
100 pF
+15V
−15V
R3
25k
2
7
1
5
A2
LF355
6
−
3
4
−15V

TL/H/5646-26

- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V$, $V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

Typical Applications (Continued)

Fast Sample and Hold


+15V
C_C 2 pF
R1 100k
25k
A1 LF356
V_{IN}
-15V
I_{OUT}
SW1
JFET SWITCHES LF11331
SW2
C_h
+15V
25k
A2 LF356
-15V
V_{OUT}
2
3
7
1
5
6
4

TL/H/5646-33

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

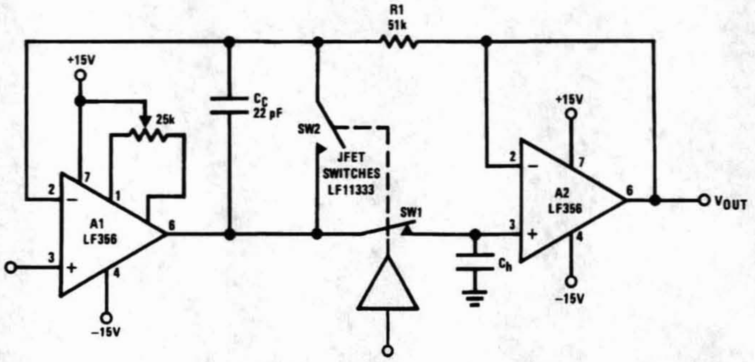
$$T_A \cong \left[\frac{2R_{ON}, V_{IN}, C_h}{S_r}\right]^{1/2} \text{ provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}, R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN} C_h}{20 \text{ mA}}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

High Accuracy Sample and Hold

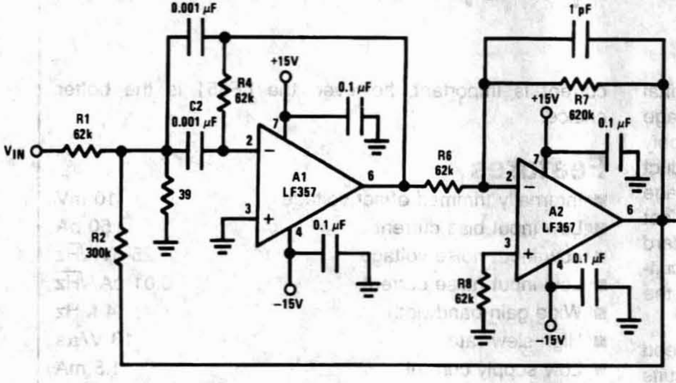

R1 51k
+15V
25k
C_C 22 pF
SW2
JFET SWITCHES LF11333
SW1
A1 LF356
-15V
C_h
+15V
A2 LF356
-15V
V_{OUT}
2
3
7
1
6
4

TL/H/5646-27

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

Typical Applications (Continued)

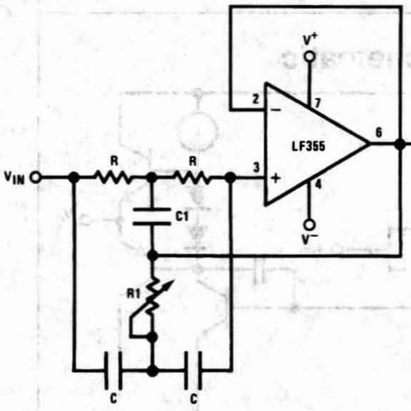
High Q Band Pass Filter


C1
0.001 μF
1 pF
+15V
R4
62k
0.1 μF
C2
0.001 μF
+15V
R7
620k
0.1 μF
R1
62k
V_IN
2
7
A1
LF357
6
R6
62k
2
7
A2
LF357
6
V_OUT
39
3
4
0.1 μF
3
4
0.1 μF
R2
300k
R8
62k
−15V
−15V

- By adding positive feedback (R2) Q increases to 40
- $f_{BP} = 100$ kHz
- $\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$
- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 μs

TL/H/5646–28

High Q Notch Filter


V+
2
7
LF355
6
V_OUT
V_IN
R
R
3
4
V−
C1
R1
C
C

- 2R1 = R = 10 MΩ
  2C = C1 = 300 pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - Low I_B
  - Low supply current

TL/H/5646–34

National Semiconductor

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

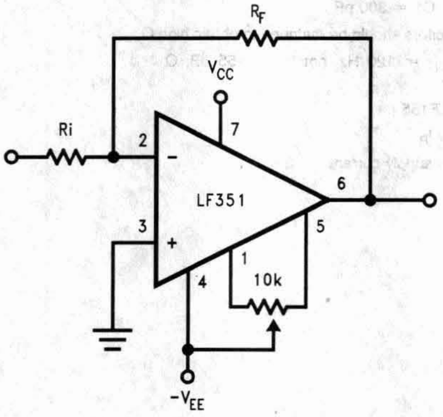
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

Features

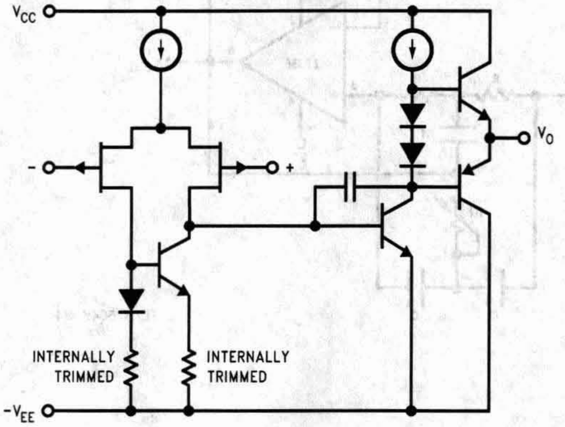
■ Internally trimmed offset voltage	10 mV
■ Low input bias current	50 pA
■ Low input noise voltage	$25\ nV/\sqrt{Hz}$
■ Low input noise current	$0.01\ pA/\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	$13\ V/\mu s$
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	$<0.02\%$
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	$2\ \mu s$

Typical Connection



TL/H/5648-11

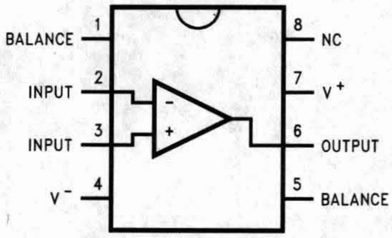
Simplified Schematic



TL/H/5648-12

Connection Diagrams

Dual-In-Line Package



TL/H/5648-13

Order Number LF351M or LF351N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	
Metal Can	300°C
DIP	260°C

θ_{jA}

N Package	120°C/W
M Package	TBD

Soldering Information

Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$ Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10		µV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 4) $T_j \leq 70°C$		25	100 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 4) $T_j \leq \pm 70°C$		50	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\ k\Omega$ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		V/μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{JA}.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

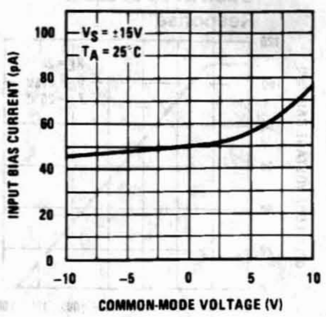
Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \le T_A \le +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

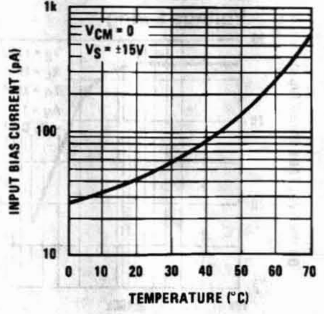
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

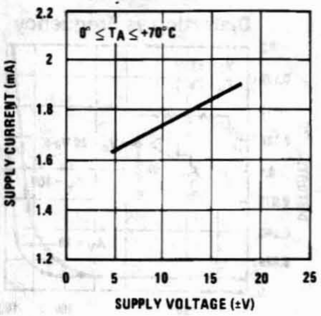
Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V.

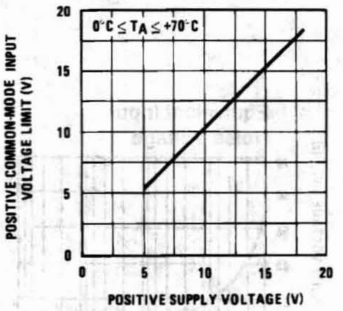
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

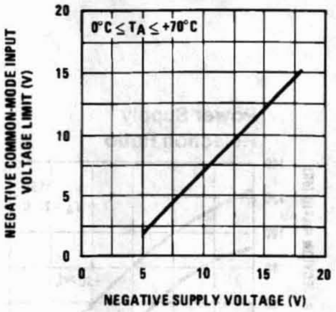
Typical Performance Characteristics

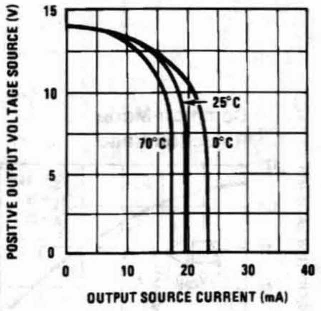

Input Bias Current

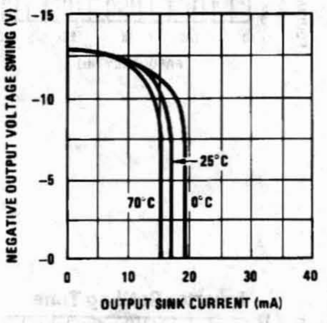

Input Bias Current

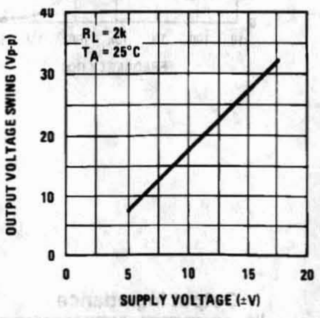

Supply Current

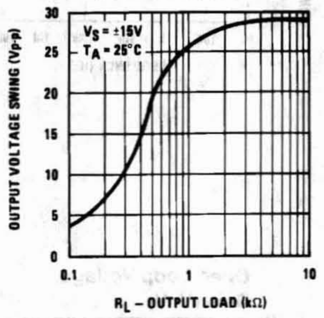

Positive Common-Mode Input Voltage Limit

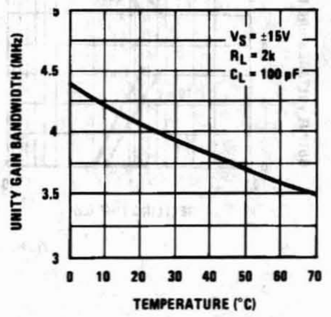

Negative Common-Mode Input Voltage Limit

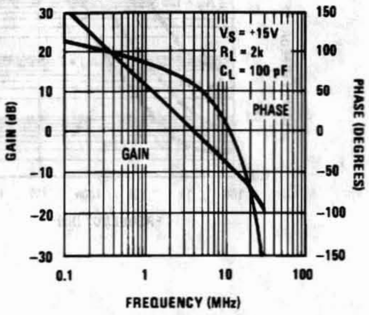

Positive Current Limit

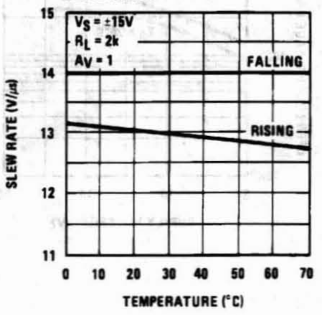

Negative Current Limit


Voltage Swing


Output Voltage Swing


Gain Bandwidth

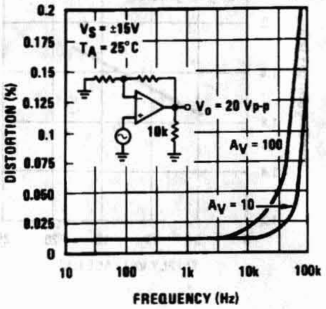

Bode Plot


Slew Rate

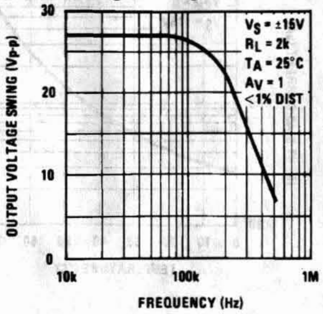
TL/H/5648–2

Typical Performance Characteristics (Continued)

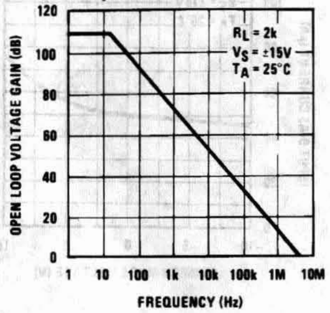
Distortion vs Frequency



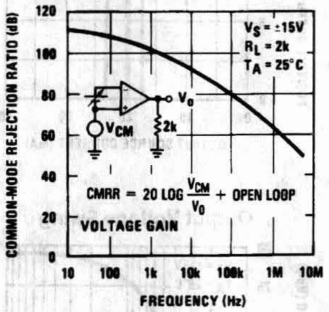
Undistorted Output Voltage Swing



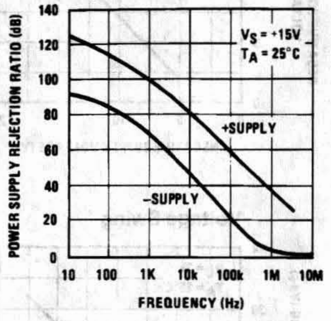
Open Loop Frequency Response



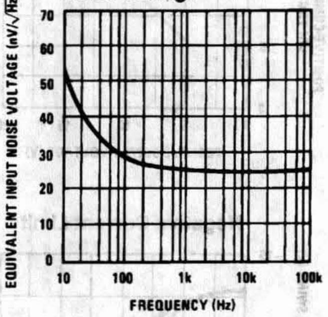
Common-Mode Rejection Ratio



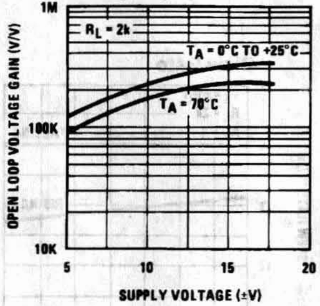
Power Supply Rejection Ratio



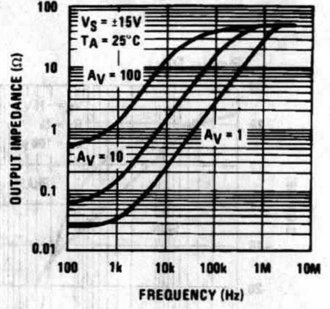
Equivalent Input Noise Voltage



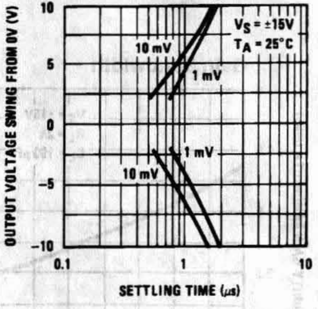
Open Loop Voltage Gain (V/V)



Output Impedance



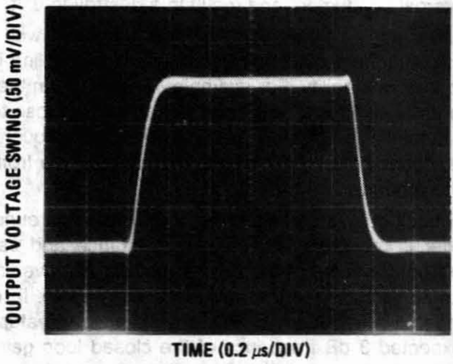
Inverter Settling Time



TL/H/5648–3

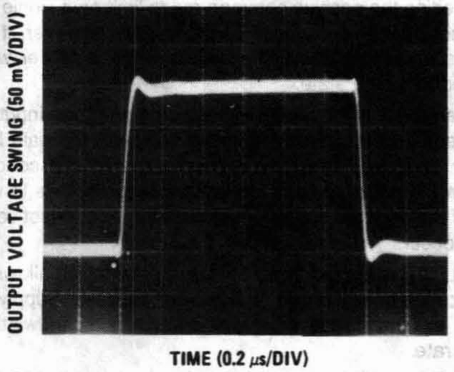
Pulse Response

Small Signal Inverting



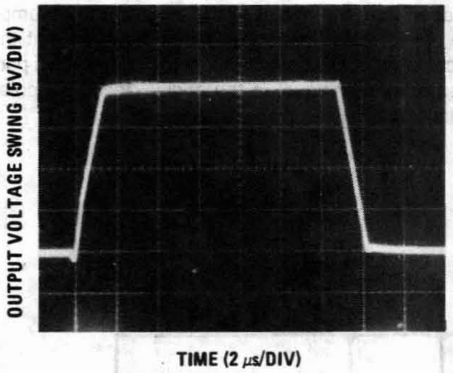
TL/H/5648–4

Small Signal Non-Inverting



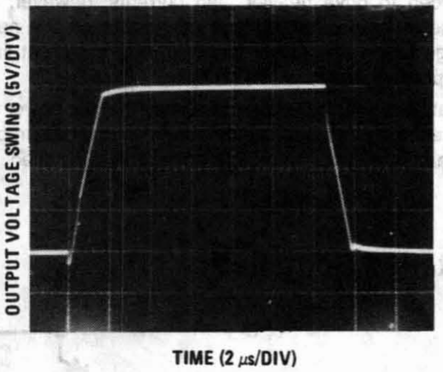
TL/H/5648–5

Large Signal Inverting



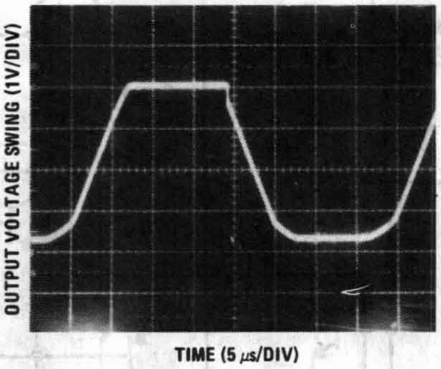
TL/H/5648–6

Large Signal Non-Inverting



TL/H/5648–7

Current Limit ($R_L = 100\Omega$)



TL/H/5648–8

Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

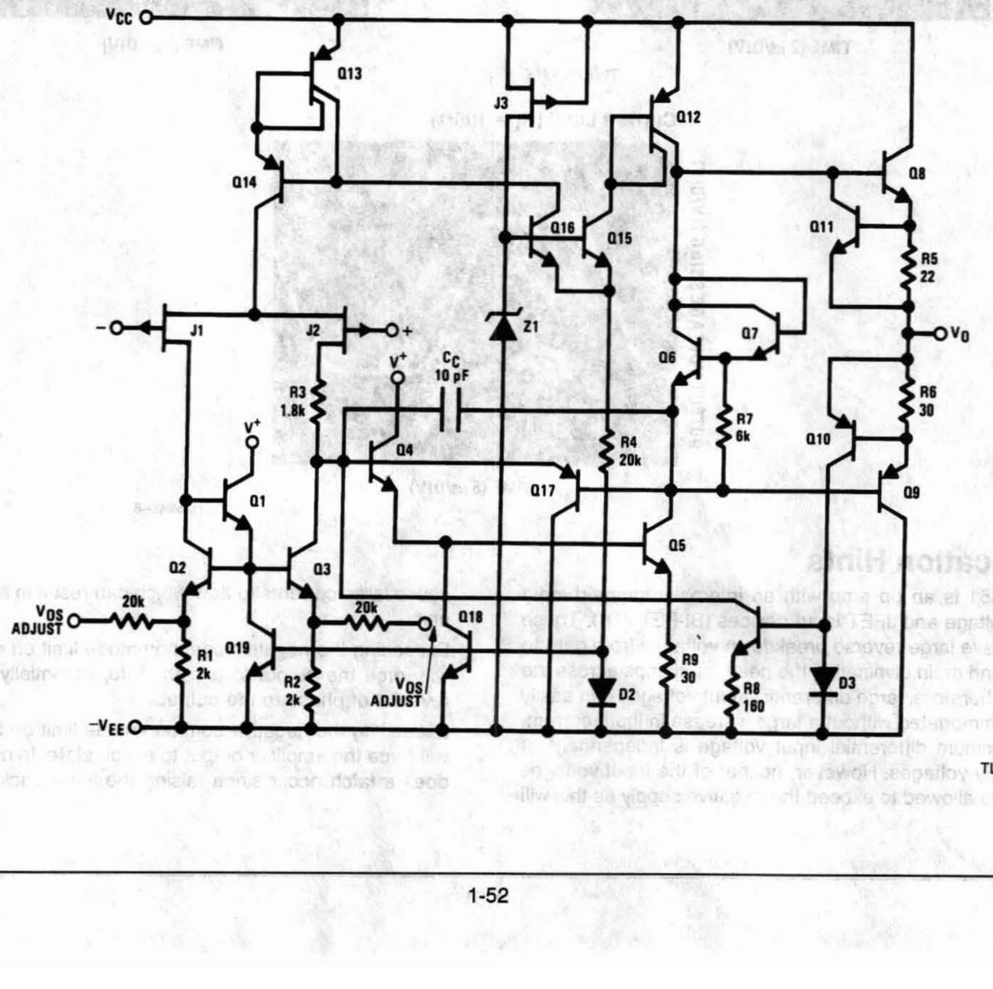
The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

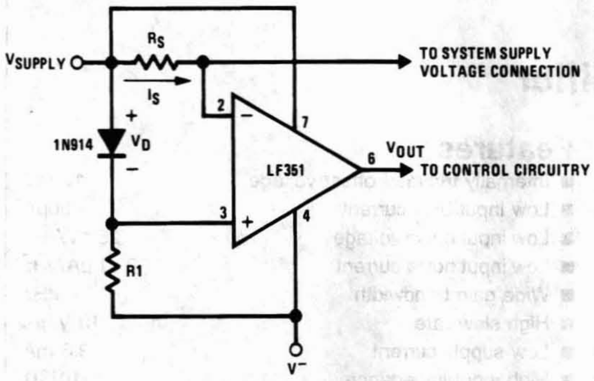
Detailed Schematic



TL/H/5648–9

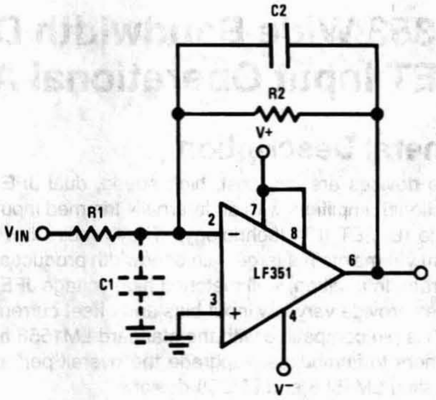
Typical Applications

Supply Current Indicator/Limiter


R$_S$
V$_{SUPPLY}$
I$_S$
TO SYSTEM SUPPLY VOLTAGE CONNECTION
+
1N914
V$_D$
−
2
7
LF351
6
V$_{OUT}$
TO CONTROL CIRCUITRY
3
4
R1
V$^-$

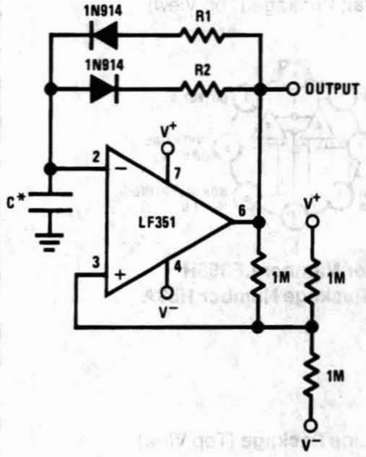
- V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z$_{IN}$ Inverting Amplifier


C2
R2
V+
7
R1
V$_{IN}$
2
8
LF351
6
C1
3
4
V$^-$

Parasitic input capacitance C1 ≅ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator

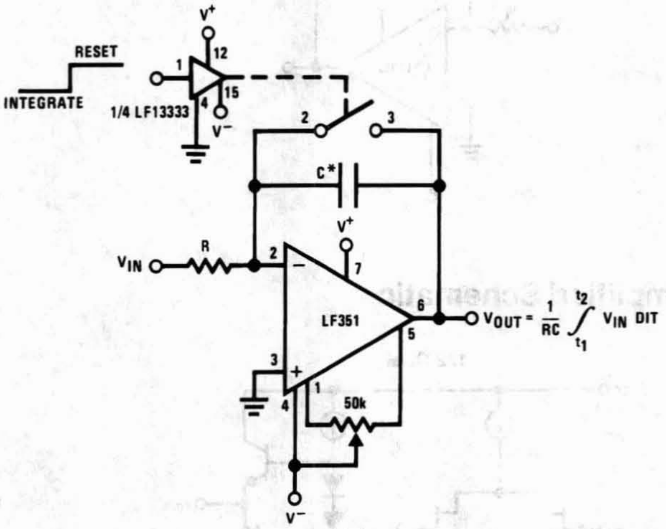

1N914
R1
1N914
R2
OUTPUT
V$^+$
2
7
C*
LF351
6
V$^+$
3
4
1M
1M
V$^-$
1M
V$^-$

- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator


RESET
INTEGRATE
V$^+$
1
12
15
1/4 LF13333
4
V$^-$
2
3
C*
V$^+$
R
V$_{IN}$
2
7
LF351
6
$V_{OUT} = \frac{1}{RC} \int_{t_1}^{t_2} V_{IN}\ DT$
5
3
1
4
50k
V$^-$

TL/H/5648-10

*Low leakage capacitor

- 50k pot used for less sensitive V_{OS} adjust

National Semiconductor

LF353 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

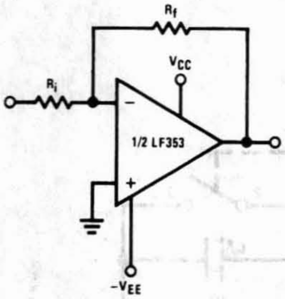
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

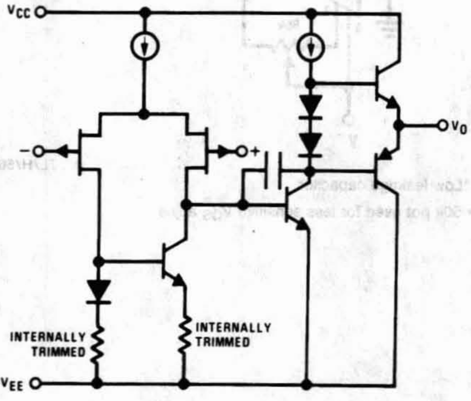
■ Internally trimmed offset voltage	10 mV
■ Low input bias current	50pA
■ Low input noise voltage	25 nV/$\sqrt{Hz}$
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	3.6 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, RL = 10k, V_O = 20Vp−p, BW = 20 Hz-20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection


R_f
R_i
V_{CC}
1/2 LF353
−V_{EE}

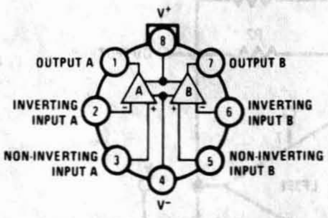
Simplified Schematic

1/2 Dual


V_{CC}
−
+
V_O
INTERNALLY TRIMMED
INTERNALLY TRIMMED
−V_{EE}

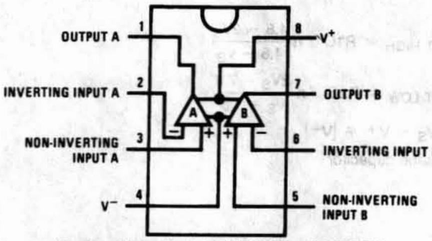
Connection Diagrams

Metal Can Package (Top View)


V+
OUTPUT A
OUTPUT B
INVERTING INPUT A
INVERTING INPUT B
NON-INVERTING INPUT A
NON-INVERTING INPUT B
V−
A
B
1
2
3
4
5
6
7
8

Order Number LF353H
See NS Package Number H08A

Dual-In-Line Package (Top View)


OUTPUT A
INVERTING INPUT A
NON-INVERTING INPUT A
V−
V+
OUTPUT B
INVERTING INPUT B
NON-INVERTING INPUT B
A
B
1
2
3
4
5
6
7
8

Order Number LF353M or LF353N
See NS Package Number M08A or N08E

TL/H/5649–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 1)
Operating Temperature Range	0°C to +70°C
T_j(MAX)	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 7)	1700V
θ_{JA} M Package	TBD

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S=10k\Omega$, $T_A=25°C$		5	10	mV
		Over Temperature			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S=10\ k\Omega$		10		μV/°C
I_{OS}	Input Offset Current	$T_j=25°C$, (Notes 4, 5)		25	100	pA
		$T_j \leq 70°C$			4	nA
I_B	Input Bias Current	$T_j=25°C$, (Notes 4, 5)		50	200	pA
		$T_j \leq 70°C$			8	nA
R_{IN}	Input Resistance	$T_j=25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S=\pm15V$, $T_A=25°C$ $V_O=\pm10V$, $R_L=2\ k\Omega$	25	100		V/mV
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	$V_S=\pm15V$, $R_L=10k\Omega$	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S=\pm15V$	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A=25°C$, f=1 Hz−20 kHz (Input Referred)		−120		dB
SR	Slew Rate	$V_S=\pm15V$, $T_A=25°C$	8.0	13		V/μs
GBW	Gain Bandwidth Product	$V_S=\pm15V$, $T_A=25°C$	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A=25°C$, $R_S=100\Omega$, f=1000 Hz		16		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j=25°C$, f=1000 Hz		0.01		pA/$\sqrt{Hz}$

Note 1: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 115°C/W typ junction to ambient for the N package, and 158°C/W typ junction to ambient for the H package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

Note 4: These specifications apply for $V_S=\pm15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM}=0$.

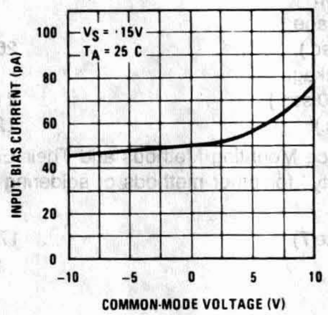
Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j=T_A+\theta_{jA}\ P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm6V$ to $\pm15V$.

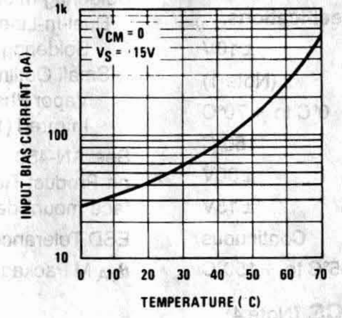
Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

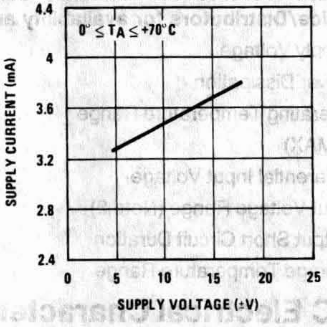
Input Bias Current



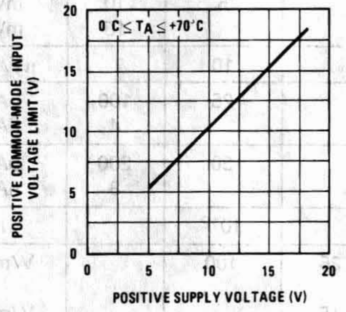
Input Bias Current



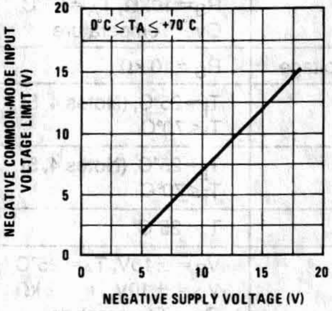
Supply Current



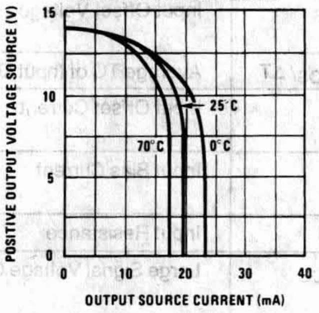
Positive Common-Mode Input Voltage Limit



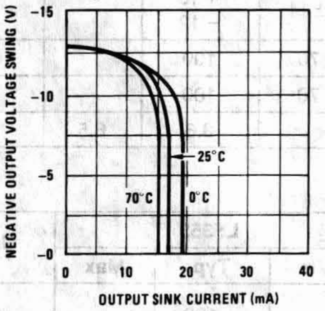
Negative Common-Mode Input Voltage Limit



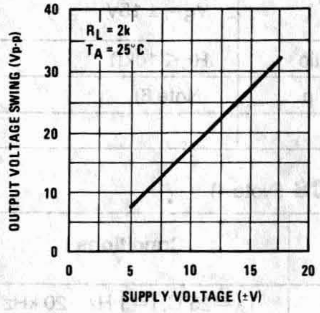
Positive Current Limit



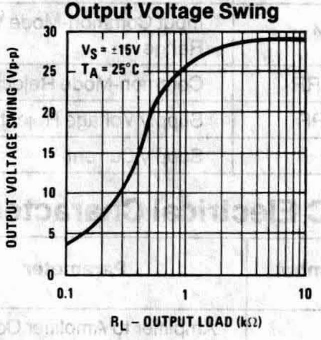
Negative Current Limit



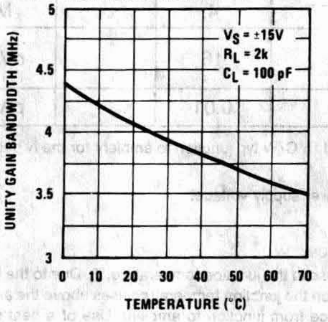
Voltage Swing



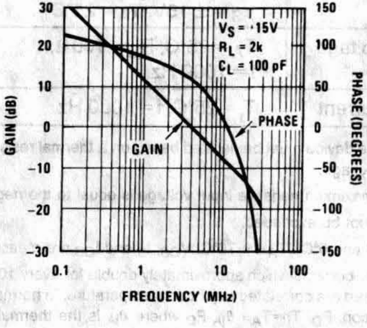
Output Voltage Swing



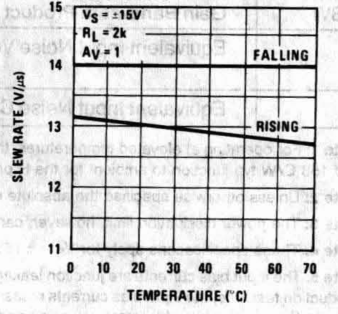
Gain Bandwidth



Bode Plot



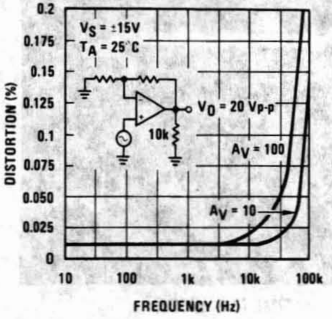
Slew Rate



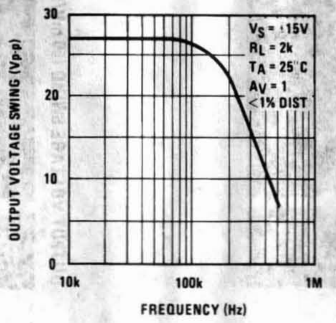
TL/H/5649–2

Typical Performance Characteristics (Continued)

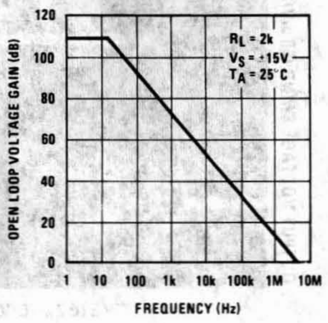
Distortion vs Frequency



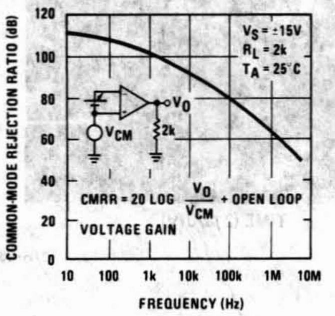
Undistorted Output Voltage Swing



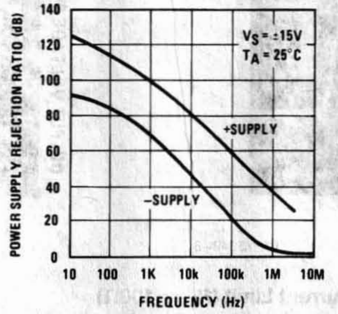
Open Loop Frequency Response



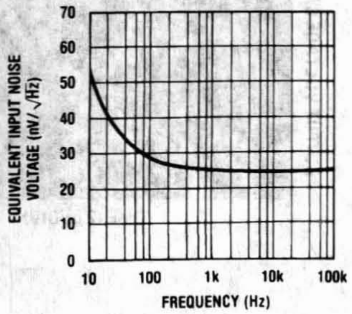
Common-Mode Rejection Ratio



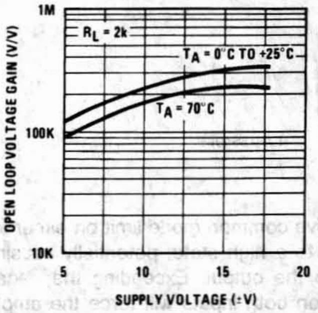
Power Supply Rejection Ratio



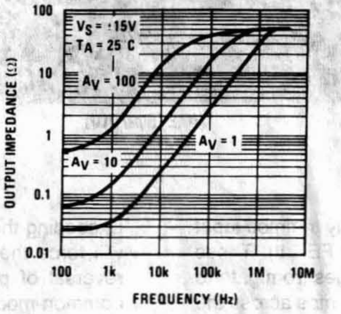
Equivalent Input Noise Voltage



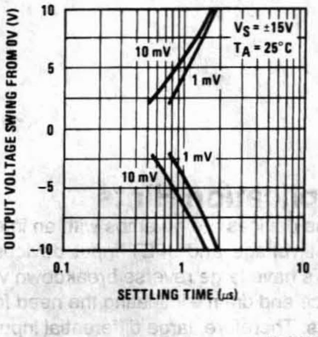
Open Loop Voltage Gain (V/V)



Output Impedance

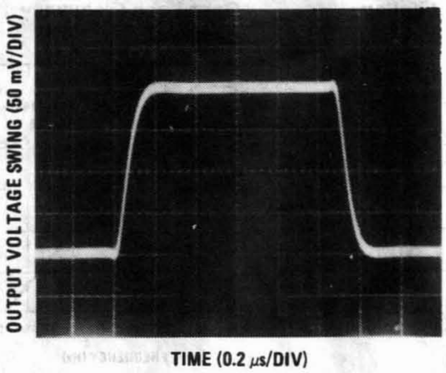


Inverter Settling Time

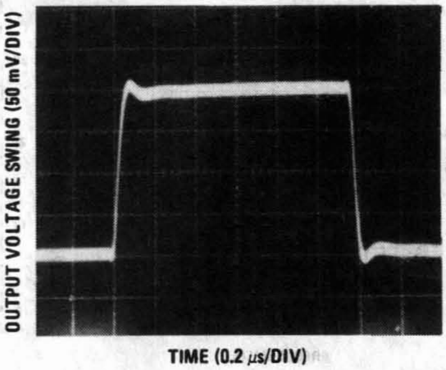


TL/H/5649–3

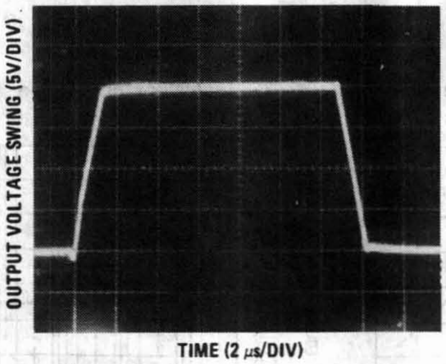
Pulse Response


Small Signaling Inverting

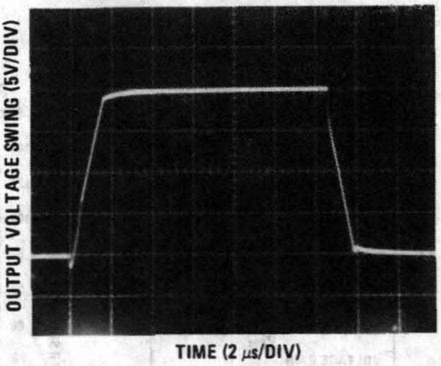
TL/H/5649–4


Small Signal Non-Inverting

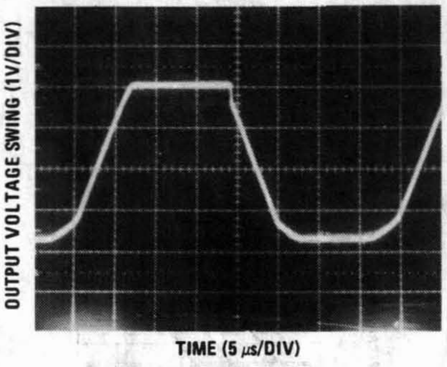
TL/H/5649–5


Large Signal Inverting

TL/H/5649–6


Large Signal Non-Inverting

TL/H/5649–7


Current Limit ($R_L = 100\Omega$)

TL/H/5649–8

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

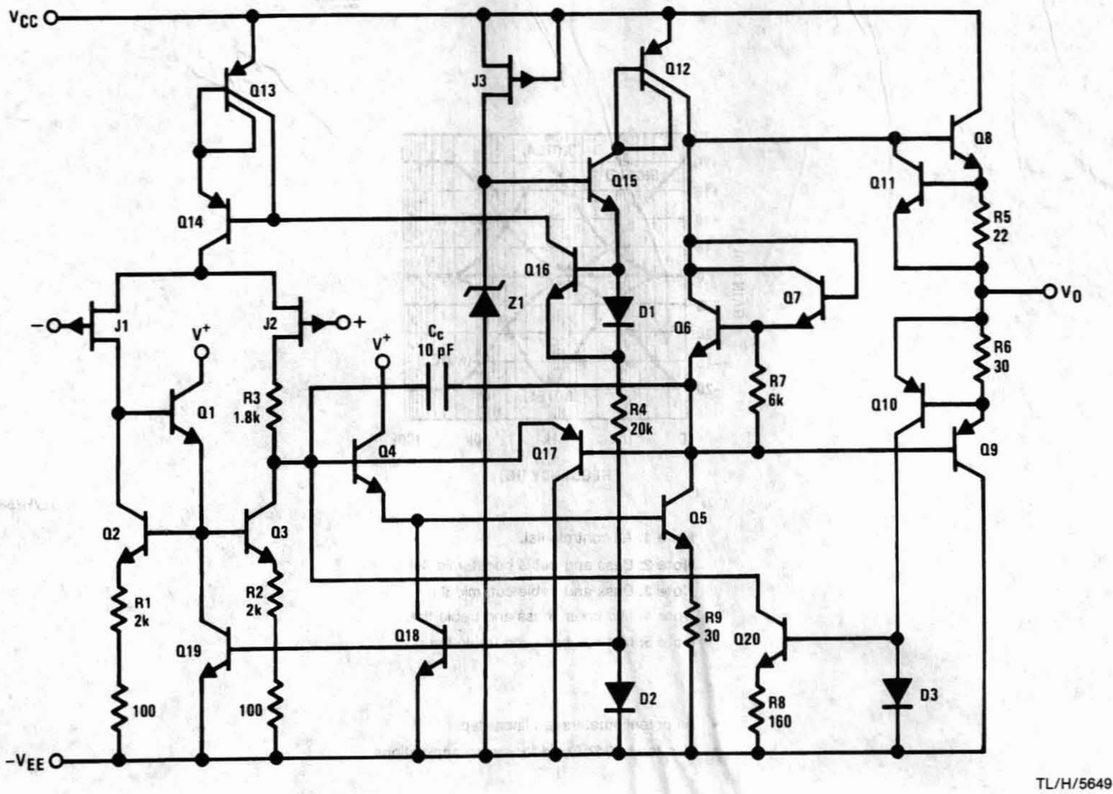
The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

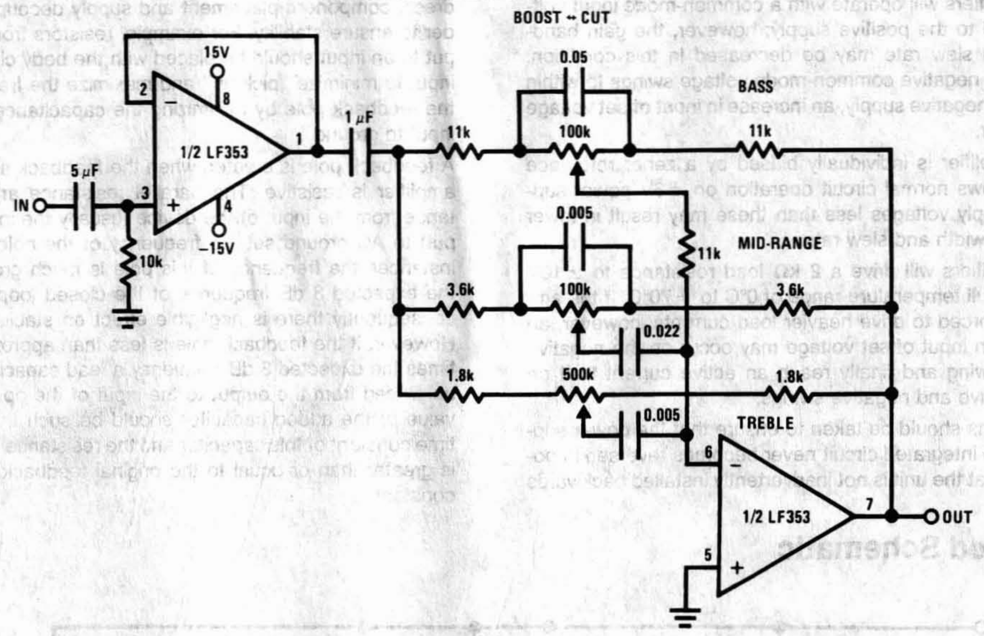
Detailed Schematic

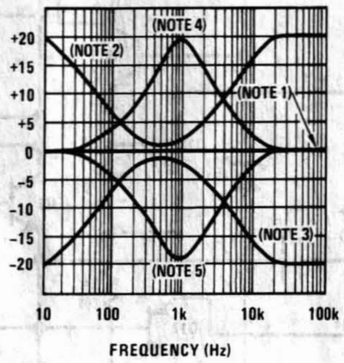


TL/H/5649-9

Typical Applications

Three-Band Active Tone Control


BOOST ↔ CUT
15V
2
8
−
1 μF
11k
0.05
100k
BASS
11k
1/2 LF353
1
5 μF
IN
3
+
4
−15V
10k
0.005
11k
MID-RANGE
3.6k
100k
3.6k
0.022
1.8k
500k
1.8k
0.005
TREBLE
6
−
1/2 LF353
7
OUT
5
+



TL/H/5649–10

Note 1: All controls flat.

Note 2: Bass and treble boost, mid flat.

Note 3: Bass and treble cut, mid flat.

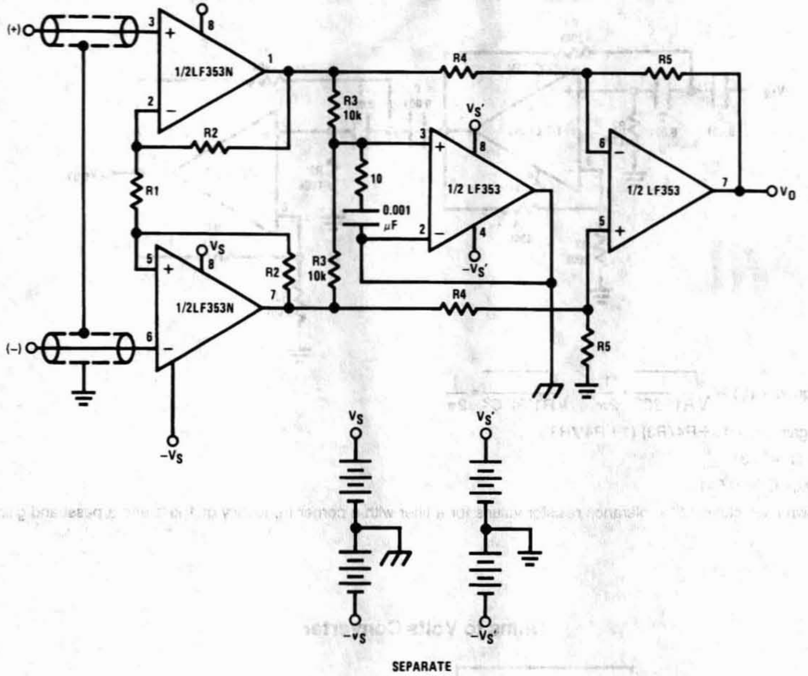
Note 4: Mid boost, bass and treble flat.

Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier


(+)
(−)
Vs
−Vs
1/2LF353N
1/2LF353N
1/2 LF353
1/2 LF353
R1
R2
R2
R3 10k
R3 10k
R4
R4
R5
R5
10
0.001 µF
Vs'
−Vs'
VO
Vs
−Vs
Vs'
−Vs'
SEPARATE

$$A_V = \left(\frac{2R2}{R1} + 1\right) \frac{R5}{R4}$$

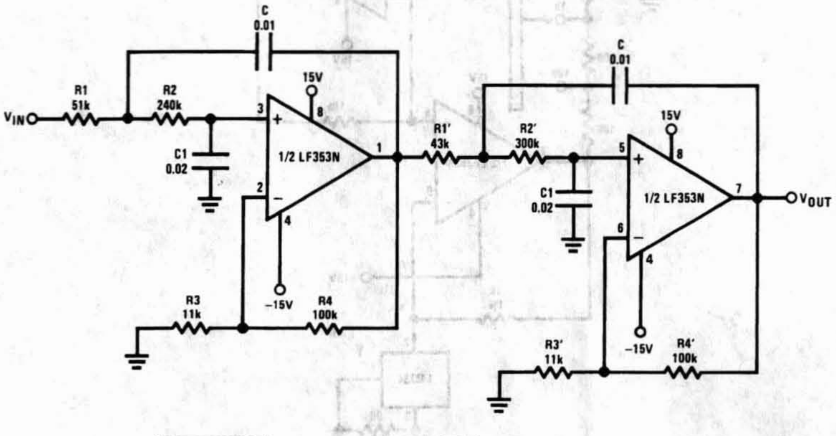
⫫ and ⏚ are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

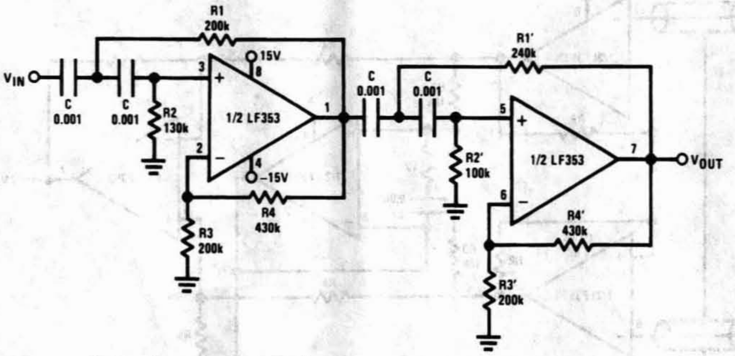

VIN
R1 51k
R2 240k
C 0.01
C1 0.02
15V
1/2 LF353N
−15V
R3 11k
R4 100k
R1' 43k
R2' 300k
C 0.01
C1 0.02
15V
1/2 LF353N
VOUT
−15V
R3' 11k
R4' 100k

- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

TL/H/5649–11

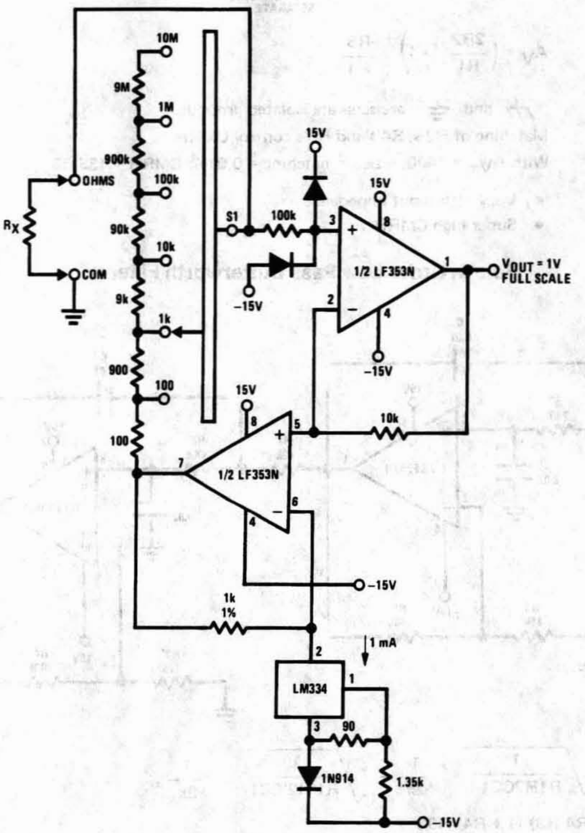
Typical Applications (Continued)

Fourth Order High Pass Butterworth Filter


R1
200k
R1'
240k
V_IN
C
0.001
C
0.001
C
0.001
C
0.001
R2
130k
15V
1/2 LF353
−15V
R4
430k
R3
200k
R2'
100k
1/2 LF353
R4'
430k
R3'
200k
V_OUT
3
8
1
2
4
5
7
6

- Corner frequency $(f_c) = \sqrt{\frac{1}{R1R2C^2}} \bullet \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \bullet \frac{1}{2\pi}$
- Passband gain $(H_O = (1 + R4/R3)\ (1 + R4'/R3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10.

Ohms to Volts Converter


10M
9M
1M
900k
100k
90k
10k
9k
1k
900
100
100
OHMS
COM
R_X
S1
100k
15V
15V
−15V
3
8
1
2
4
1/2 LF353N
V_OUT = 1V FULL SCALE
−15V
15V
8
5
7
6
4
1/2 LF353N
10k
−15V
1k
1%
1 mA
2
1
3
LM334
90
1N914
1.35k
−15V

TL/H/5649-13

$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the LF353.

National Semiconductor

LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description

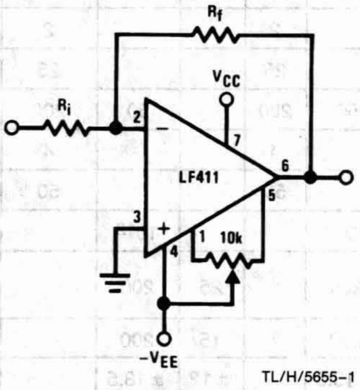
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

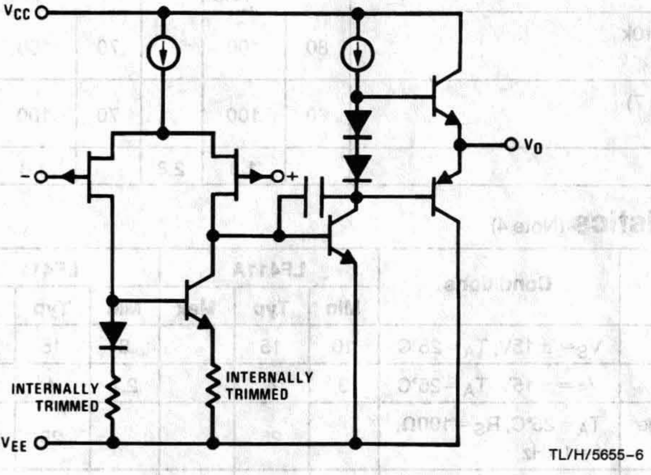
■ Internally trimmed offset voltage	0.5 mV(max)
■ Input offset voltage drift	10 μV/°C(max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ Wide gain bandwidth	3 MHz(min)
■ High slew rate	10V/μs(min)
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V=10$, $R_L=10k$, $V_O=20$ Vp-p, BW=20 Hz−20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



R_f
R_i
V_{CC}
2
7
6
LF411
5
3
1
10k
4
$-V_{EE}$
TL/H/5655–1

Simplified Schematic



V_{CC}
V_O
−
+
INTERNALLY TRIMMED
INTERNALLY TRIMMED
$-V_{EE}$
TL/H/5655–6

Ordering Information

LF411XYZ

X indicates electrical grade

Y indicates temperature range

"M" for military

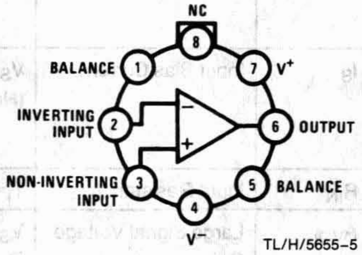
"C" for commercial

Z indicates package type

"H" or "N"

Connection Diagrams

Metal Can Package



NC
8
BALANCE
1
7
V+
INVERTING INPUT
2
6
OUTPUT
NON-INVERTING INPUT
3
5
BALANCE
4
V−
TL/H/5655–5

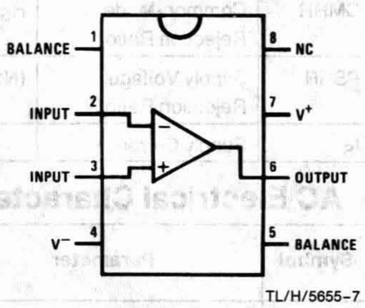
Top View

Note: Pin 4 connected to case.

Order Number LF411ACH or LF411MH/883*

See NS Package Number H08A

Dual-In-Line Package



BALANCE
1
8
NC
INPUT
2
7
V+
INPUT
3
6
OUTPUT
V−
4
5
BALANCE
TL/H/5655–7

Top View

Order Number LF411ACN, LF411CN or LF411MJ/883*

See NS Package Number N08E or J08A

*Available per JM38510/11904

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 8)

	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package
Power Dissipation (Notes 2 and 9)	670 mW	670 mW
$T_j$max	150°C	115°C
θ_jA	162°C/W (Still Air) 65°C/W (400 LF/min Air Flow)	120°C/W
θ_jC	20°C/W	
Operating Temp. Range	(Note 3)	(Note 3)
Storage Temp. Range	$-65°C \leq T_A \leq 150°C$	$-65°C \leq T_A \leq 150°C$
Lead Temp. (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance		Rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF411A			LF411			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 5)			7	10		7	20 (Note 5)	μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 4, 6)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 4, 6)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_jA.

Note 3: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

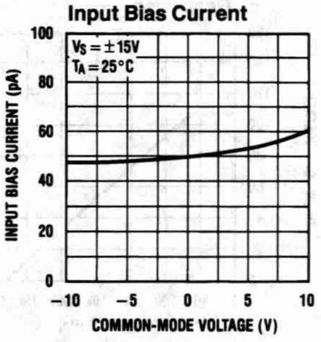
Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

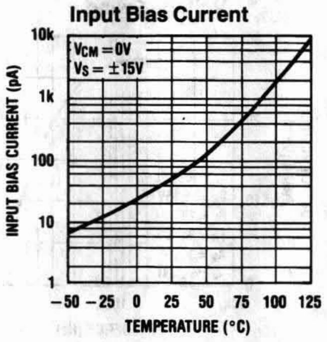
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from ±15V to ±5V for the LF411 and from ±20V to ±5V for the LF411A.

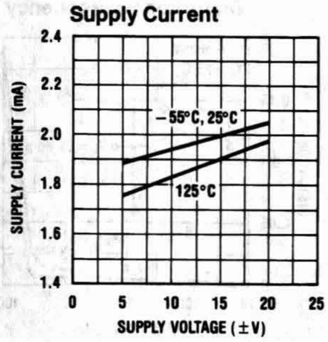
Note 8: RETS 411X for LF411MH and LF411MJ military specifications.

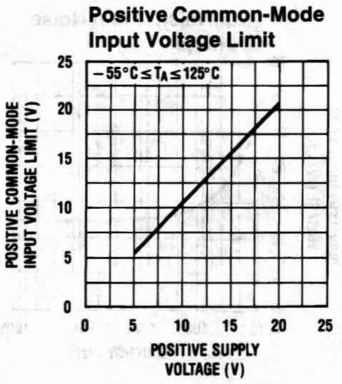
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

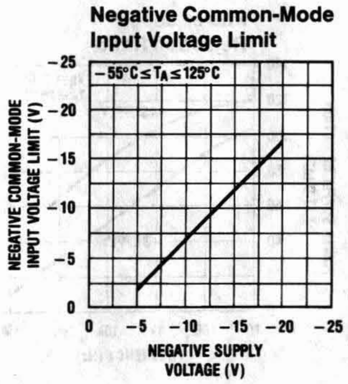
Typical Performance Characteristics

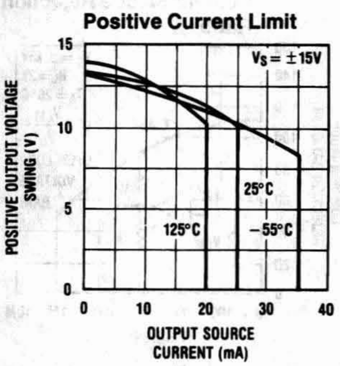

Input Bias Current

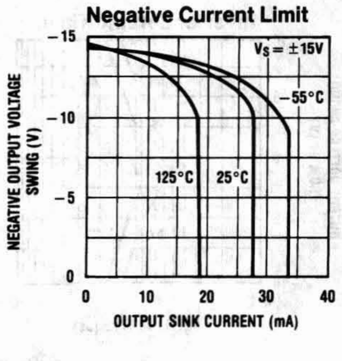

Input Bias Current

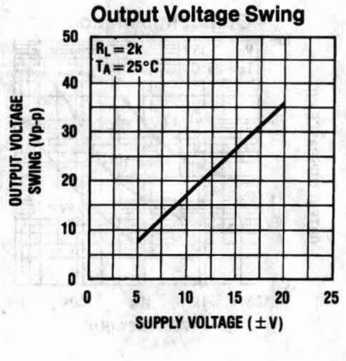

Supply Current

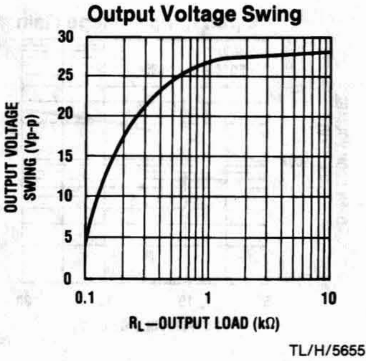

Positive Common-Mode Input Voltage Limit


Negative Common-Mode Input Voltage Limit


Positive Current Limit


Negative Current Limit


Output Voltage Swing

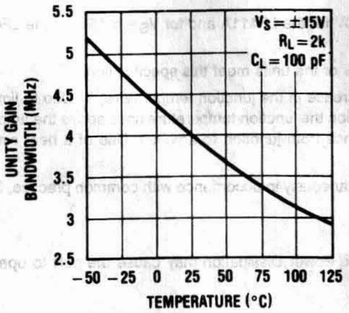

Output Voltage Swing

TL/H/5655–2

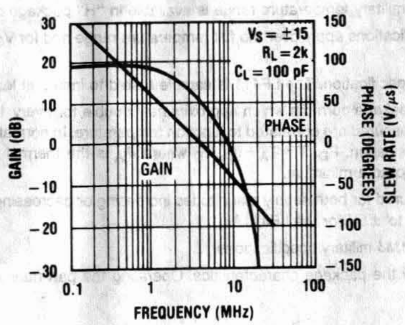
1

Typical Performance Characteristics (Continued)

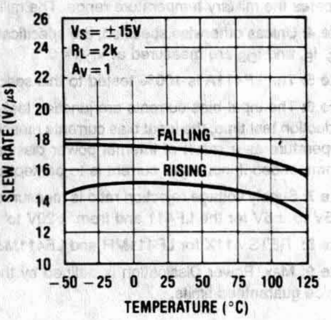
Gain Bandwidth



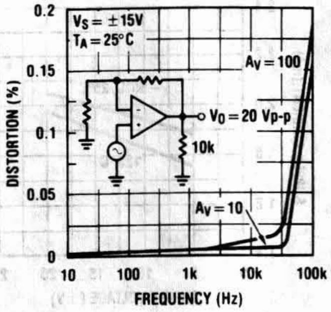
Bode Plot



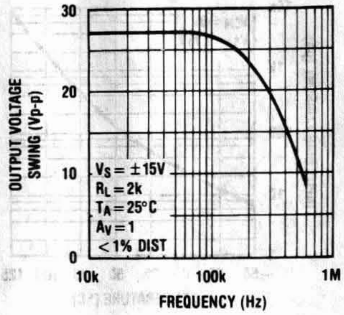
Slew Rate



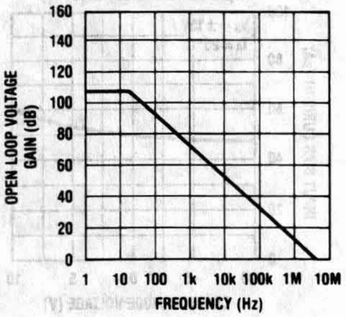
Distortion vs Frequency



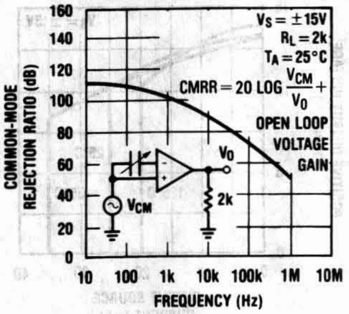
Undistorted Output Voltage Swing



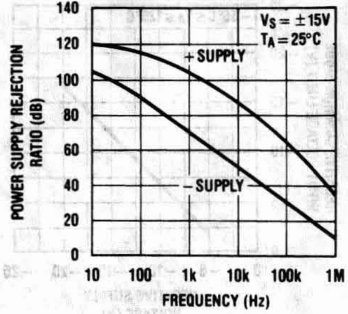
Open Loop Frequency Response



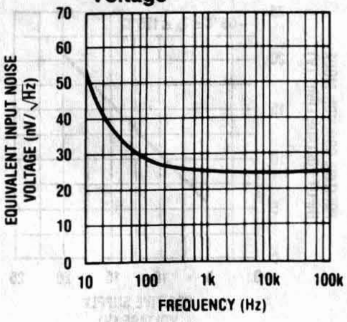
Common-Mode Rejection Ratio



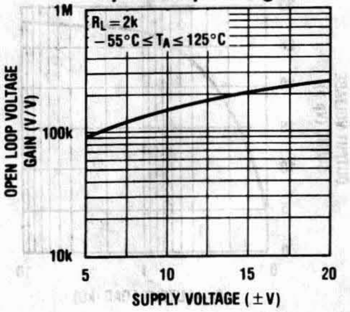
Power Supply Rejection Ratio



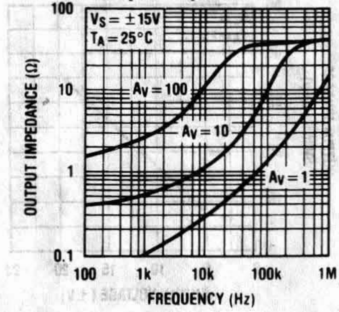
Equivalent Input Noise Voltage



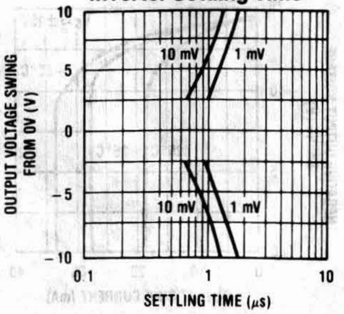
Open Loop Voltage Gain



Output Impedance



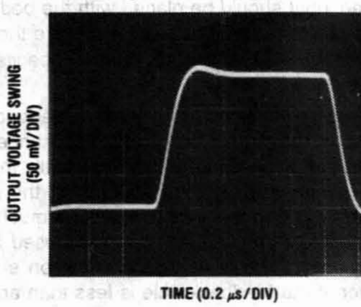
Inverter Settling Time



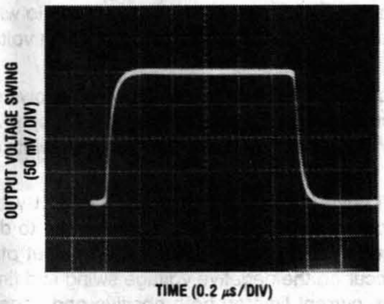
TL/H/5655–3

Pulse Response $R_L = 2\ k\Omega$, $C_L 10\ pF$

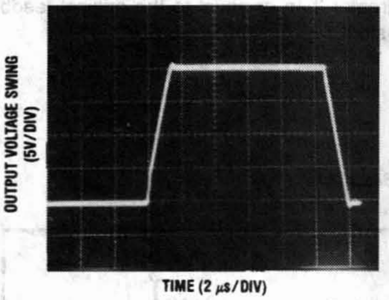
Small Signal Inverting



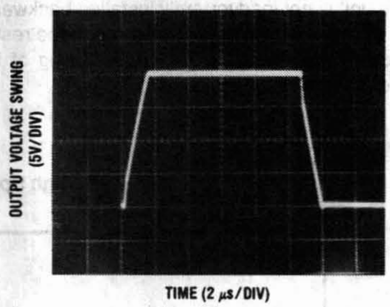
Small Signal Non-Inverting



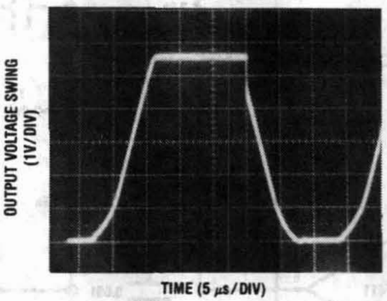
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



TL/H/5655–4

Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

Application Hints (Continued)

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

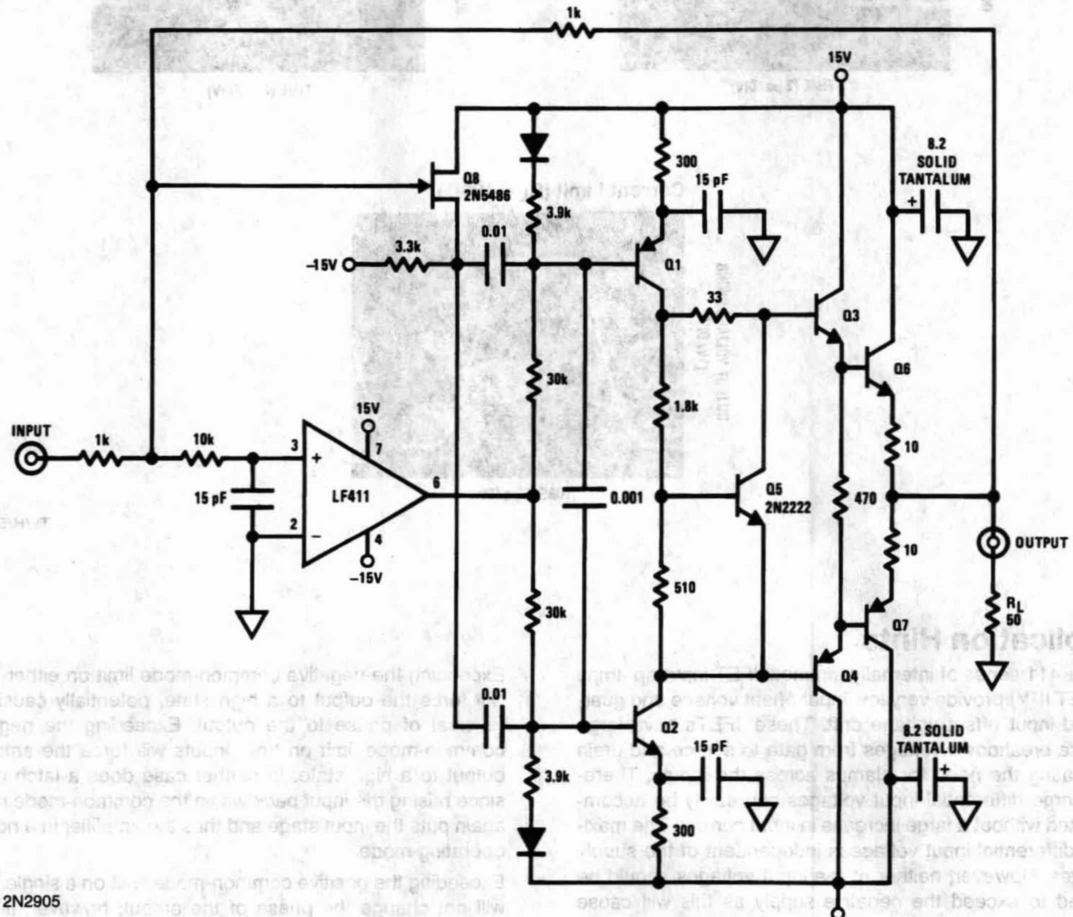
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

High Speed Current Booster



PNP = 2N2905

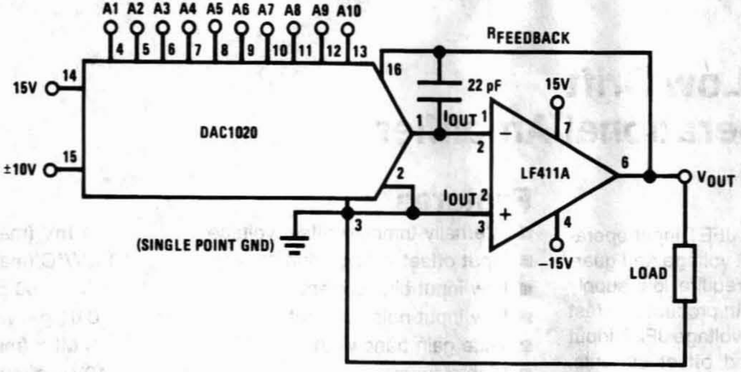
NPN = 2N2219 unless noted

TO-5 heat sinks for Q6-Q7

TL/H/5655–9

Typical Applications (Continued)

10-Bit Linear DAC with No V_{OS} Adjust


MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
15V
14
±10V
15
DAC1020
16
RFEEDBACK
22 pF
15V
7
1
IOUT 1
2
IOUT 2
3
LF411A
6
VOUT
4
−15V
LOAD
(SINGLE POINT GND)

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

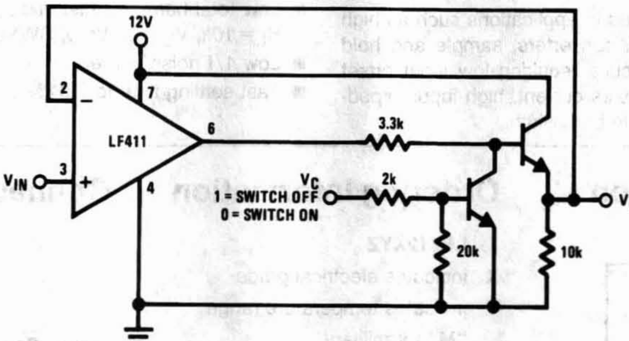
$$-10V \leq V_{REF} \leq 10V$$

$$0 \leq V_{OUT} \leq -\frac{1023}{1024} V_{REF}$$

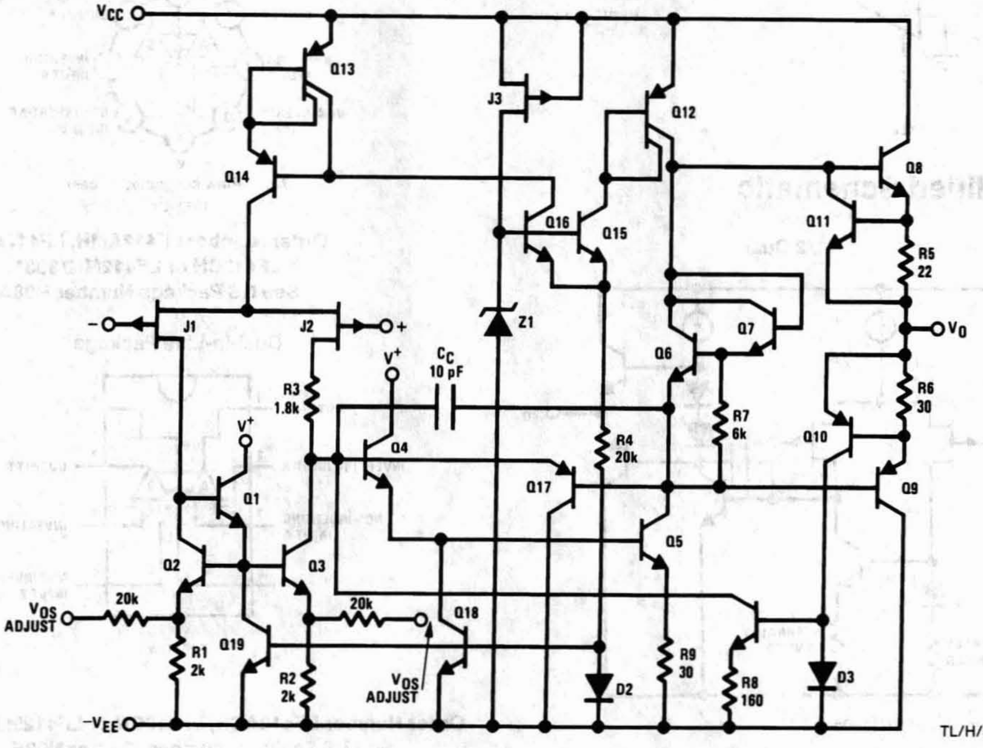
where $A_N = 1$ if the A_N digital input is high

$A_N = 0$ if the A_N digital input is low

Single Supply Analog Switch with Buffered Output


12V
2
7
LF411
6
VIN
3
4
3.3k
VC
2k
1 = SWITCH OFF
0 = SWITCH ON
20k
10k
VO

Detailed Schematic


VCC
Q13
J3
Q12
Q14
Q8
Q16
Q15
Q11
R5
22
−
J1
J2
+
Z1
Q7
VO
V+
CC
10 pF
Q6
R3
1.8k
R6
30
V+
Q4
R4
20k
R7
6k
Q10
Q1
Q17
Q9
Q5
Q2
Q3
VOS
ADJUST
20k
20k
Q18
R1
2k
Q19
R2
2k
VOS
ADJUST
R9
30
R8
160
D2
D3
−VEE

TL/H/5655-10

National Semiconductor

LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

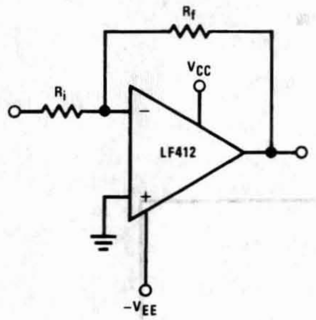
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	1 mV (max)
■ Input offset voltage drift	10 μV/°C (max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ Wide gain bandwidth	3 MHz (min)
■ High slew rate	10V/μs (min)
■ Low supply current	1.8 mA/Amplifier
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz	≤0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

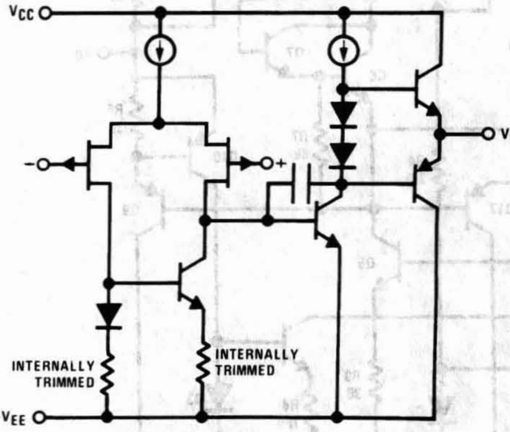
Typical Connection



R_f
V_CC
R_i
−
LF412
+
−V_EE

Simplified Schematic

1/2 Dual



V_CC
V_O
−
+
INTERNALLY TRIMMED
INTERNALLY TRIMMED
−V_EE

Ordering Information

LF412XYZ

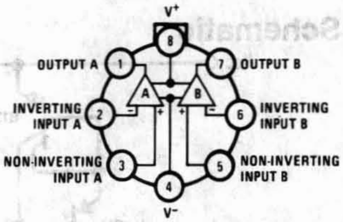
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



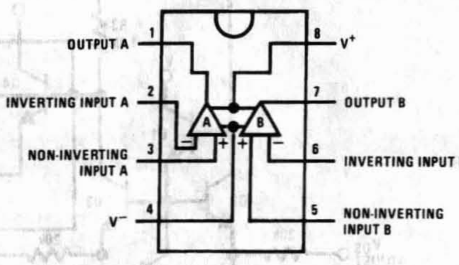
V+
8
OUTPUT A
1
7
OUTPUT B
INVERTING INPUT A
2
A
B
6
INVERTING INPUT B
NON-INVERTING INPUT A
3
5
NON-INVERTING INPUT B
4
V−

Note. Pin 4 connected to case.

TOP VIEW

Order Number LF412AMH, LF412MH, LF412CH or LF412MH/883*
See NS Package Number H08A

Dual-In-Line Package



OUTPUT A
1
8
V+
INVERTING INPUT A
2
7
OUTPUT B
A
B
NON-INVERTING INPUT A
3
6
INVERTING INPUT B
V−
4
5
NON-INVERTING INPUT B

TOP VIEW

TL/H/5656–1

Order Number LF412ACN, LF412CN or LF412MJ/883*
See NS Package Number J08A or N08E

*Available per JM38510/11905

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 9)

	LF412A	LF412
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	H Package	N Package
Power Dissipation (Note 10)	(Note 3)	670 mW
T_j max	150°C	115°C
θ_{jA} (Typical)	152°C/W	115°C/W
Operating Temp. Range	(Note 4)	(Note 4)
Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temp. (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance (Note 11)	1700V	1700V

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF412A			LF412			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.5	1.0		1.0	3.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 6)			7	10		7	20	μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current	$V_O = 0V$, $R_L = \infty$			3.6	5.6		3.6	6.5	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF412A			LF412			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefintely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only. In all cases the maximum operating temperature is limited by internal junction temperature T_j max.

Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF412A and for $V_S = \pm 15V$ for the LF412. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 85% of the amplifiers meet this specification.

Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

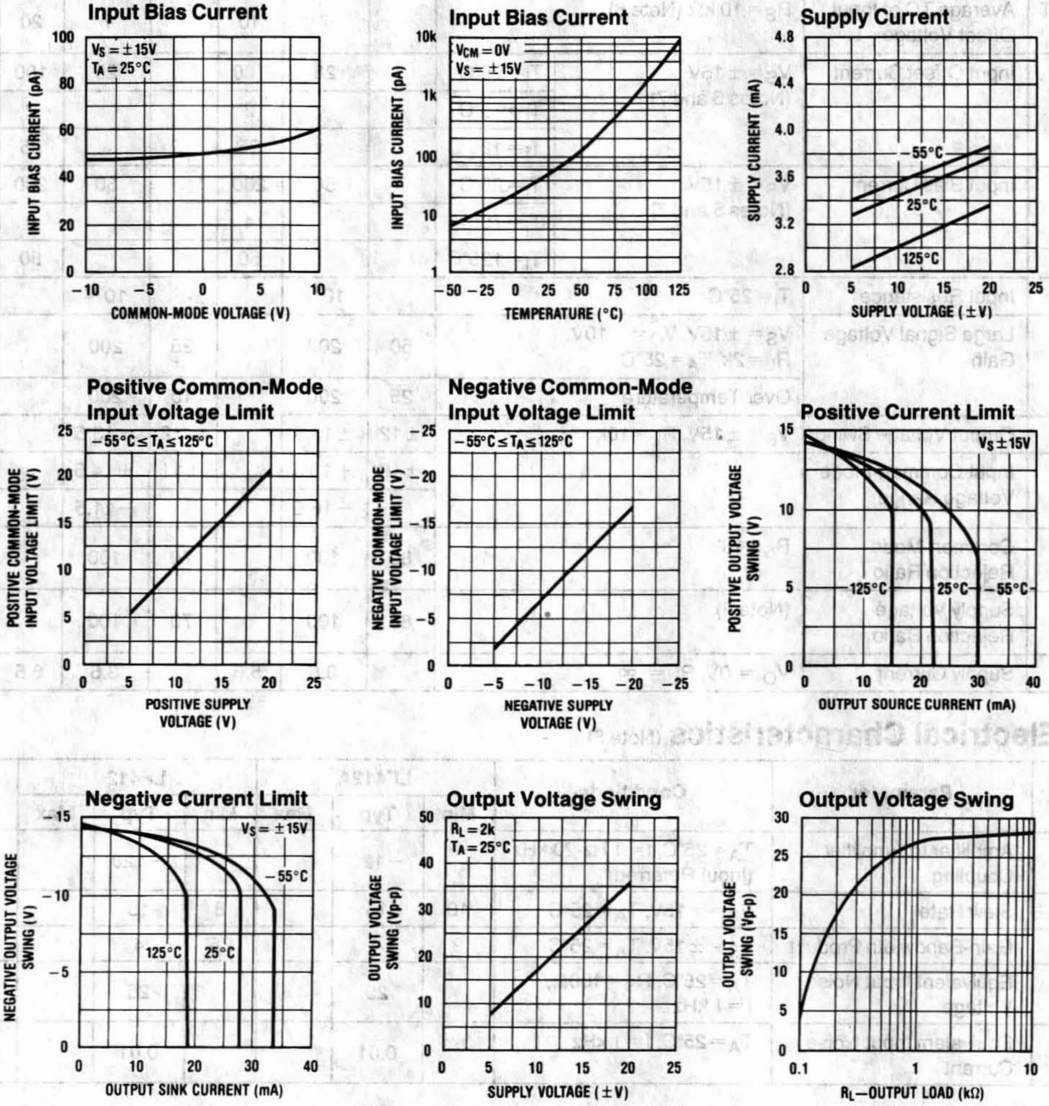
Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm 6V$ to $\pm 15V$.

Note 9: Refer to RETS412X for LF412MH and LF412MJ military specifications.

Note 10: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 11: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics


Input Bias Current

Input Bias Current

Supply Current

Positive Common-Mode Input Voltage Limit

Negative Common-Mode Input Voltage Limit

Positive Current Limit

Negative Current Limit

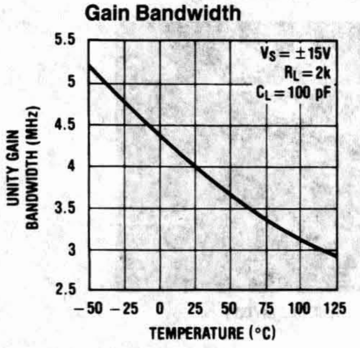
Output Voltage Swing

Output Voltage Swing

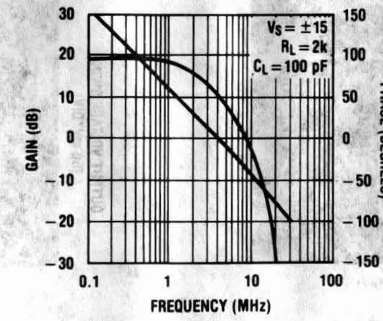
TL/H/5656–2

Typical Performance Characteristics (Continued)

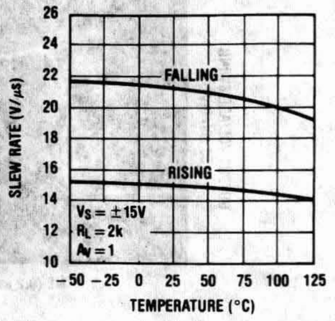
Gain Bandwidth



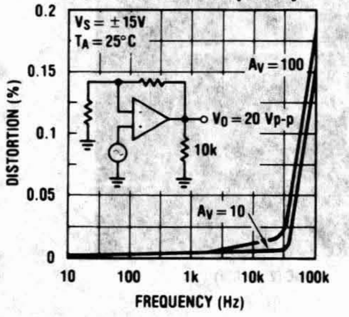
Bode Plot



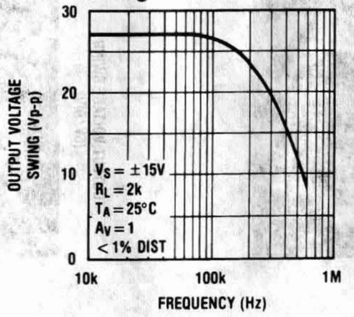
Slew Rate



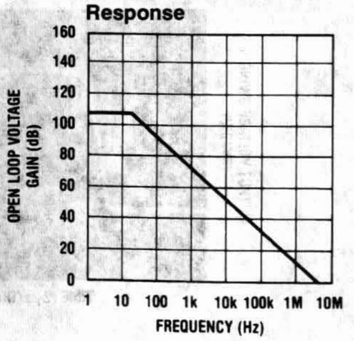
Distortion vs Frequency



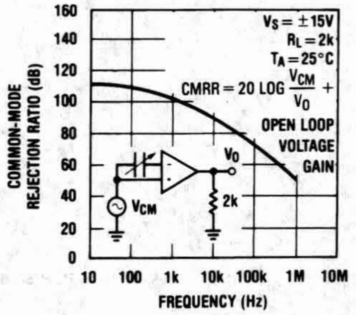
Undistorted Output Voltage Swing



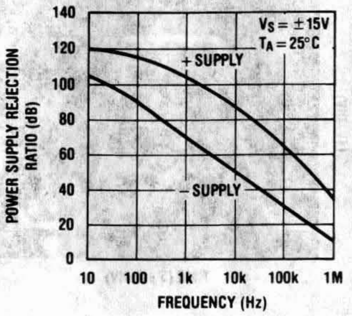
Open Loop Frequency Response



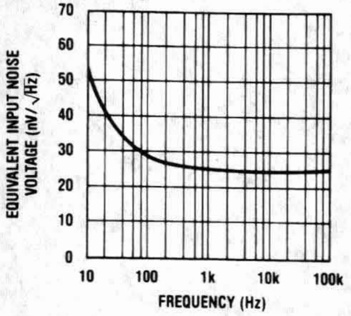
Common-Mode Rejection Ratio



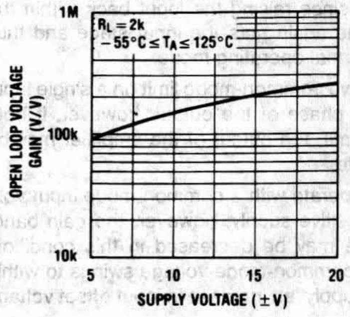
Power Supply Rejection Ratio



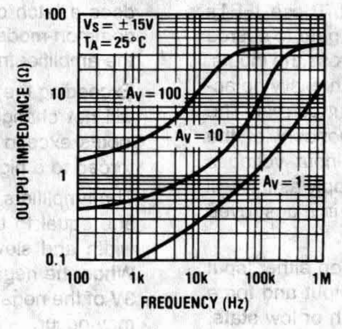
Equivalent Input Noise Voltage



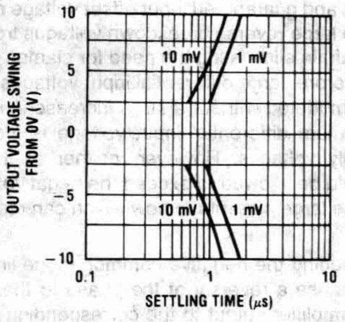
Open Loop Voltage Gain



Output Impedance



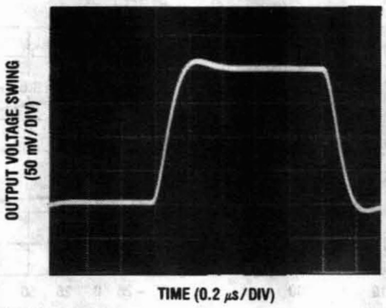
Inverter Settling Time



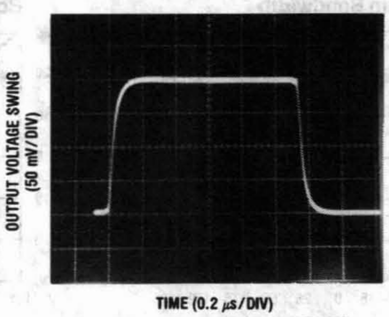
TL/H/5656–3

Pulse Response $R_L = 2\ k\Omega$, $C_L = 10\ pF$

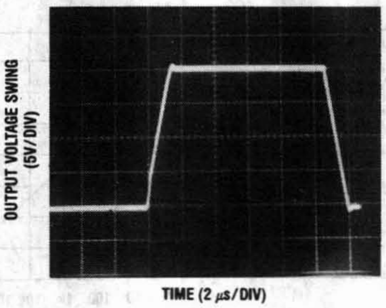
Small Signal Inverting



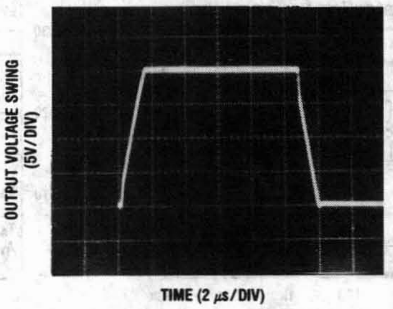
Small Signal Non-Inverting



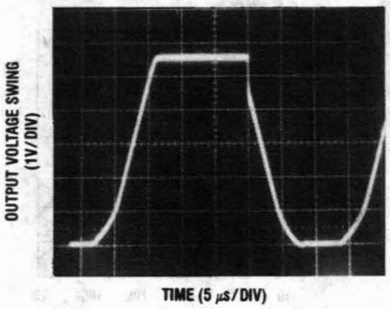
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



TL/H/5656–4

Application Hints

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Application Hints (Continued)

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6.0V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

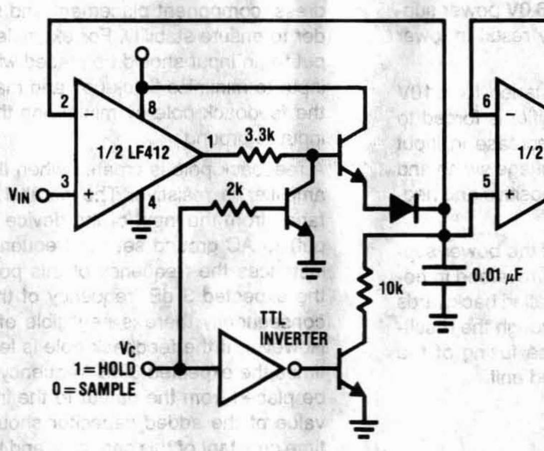
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

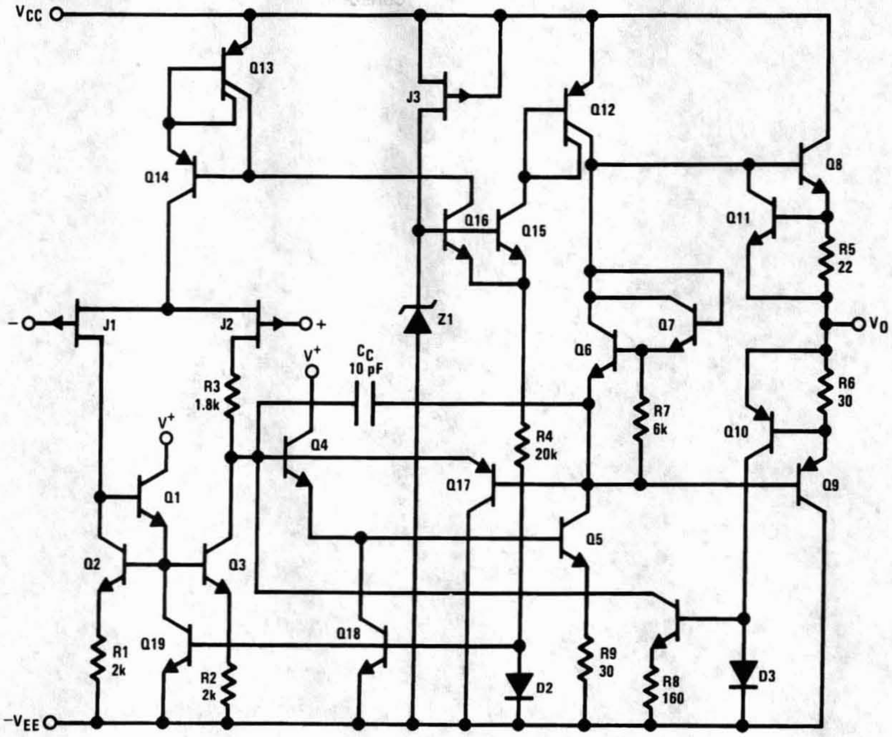
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

Single Supply Sample and Hold


2
8
3
4
1/2 LF412
1
3.3k
2k
V_IN
10k
TTL
INVERTER
V_C
1 = HOLD
0 = SAMPLE
0.01 μF
6
5
7
1/2 LF412
V_O

Detailed Schematic


V_CC
Q13
J3
Q12
Q8
Q14
Q16
Q15
Q11
R5
22
−
J1
J2
+
Z1
Q7
V_O
Q6
V⁺
C_C
10 pF
R3
1.8k
R6
30
V⁺
R7
6k
Q10
Q4
R4
20k
Q17
Q9
Q1
Q5
Q2
Q3
Q18
R1
2k
Q19
R2
2k
D2
R9
30
R8
160
D3
−V_EE

TL/H/5656-9

National Semiconductor

LF441 Low Power JFET Input Operational Amplifier

General Description

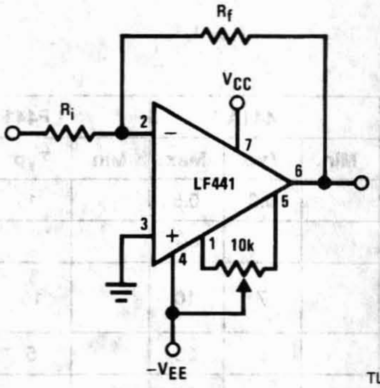
The LF441 low power operational amplifier provides many of the same AC characteristics as the industry standard LM741 while greatly improving the DC characteristics of the LM741. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM741 and only draws one tenth the supply current of the LM741. In addition, the well matched high voltage JFET input devices of the LF441 reduce the input bias and offset currents by a factor of 10,000 over the LM741. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF441 also has a very low equivalent input noise voltage for a low power amplifier.

The LF441 is pin compatible with the LM741, allowing an immediate 10 times reduction in power drain in many applications. The LF441 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/10 supply current of a LM741	200 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	0.5 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection



TL/H/9297-1

Ordering Information

LF441XYZ

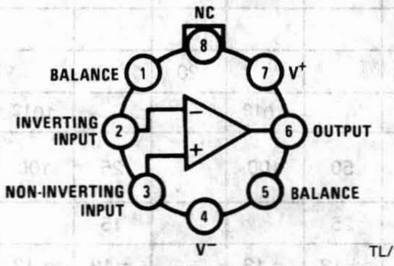
X indicates electrical grade

Y indicates temperature range
"M" for military,
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



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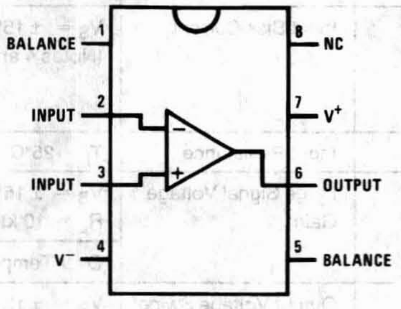
Top View

Note: Pin 4 connected to case.

Order Number LF441MH/883
See NS Package Number H08A

Dual-In-Line Package



TL/H/9297-4

Top View
Order Number LF441ACN,
LF441CM or LF441CN
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF441A	LF441
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package	M Package
Power Dissipation (Notes 2 and 9)	670 mW	670 mW	
$T_{j\,max}$	150°C	115°C	
θ_{jA}(Typical)		130°C/W	185°C/W
Board Mount in still air	165°C/W		
Board Mount in 400 LF/min air flow	65°C/W		
θ_{jC}	25°C/W		
Operating Temp. Range	(Note 3)	(Note 3)	
Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 seconds)	300°C	260°C	

	LF441A	LF441
Soldering Information		
Dual-In-Line Package		
Soldering (10 sec.)	260°C	260°C
Small Outline Package		
Vapor Phase (60 sec.)	215°C	215°C
Infrared (15 sec.)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10) Rating to be Determined

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF441A			LF441			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.3	0.5		1	5	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 5)			7	10		10		μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 4 and 6)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 4 and 6)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\ k\Omega$, $T_A = 25°C$		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18, −17		±11	+14, −12		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$		80	100		70	95		dB

DC Electrical Characteristics (Note 4) (Continued)

Symbol	Parameter	Conditions	LF441A			LF441			Units
			Min	Typ	Max	Min	Typ	Max	
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		70	90		dB
I_S	Supply Current			150	200		150	250	μA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF441A			LF441			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	$V_S = \pm15V$, $T_A = 25°C$	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm15V$, $T_A = 25°C$	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 3: The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm20V$ for the LF441A and for $V_S = \pm15V$ for the LF441. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The LF441A is 100% tested to this specification.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V for the LF441 and from ±20V to ±5V for the LF441A.

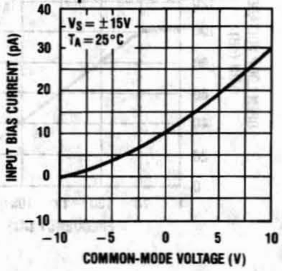
Note 8: Refer to RETS441X for LF441MH military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

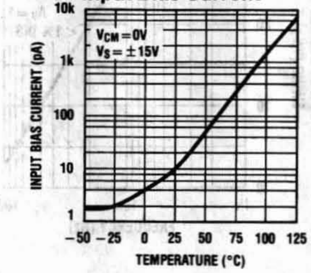
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

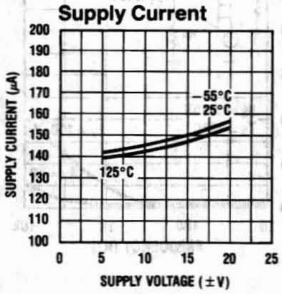
Input Bias Current



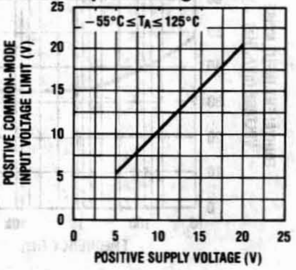
Input Bias Current



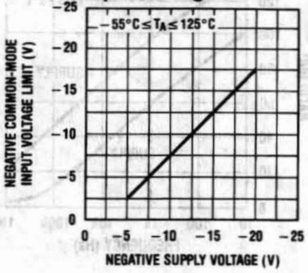
Supply Current



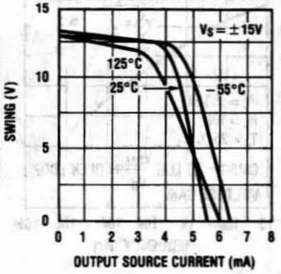
Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit



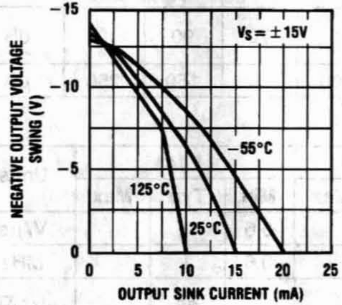
Positive Current Limit



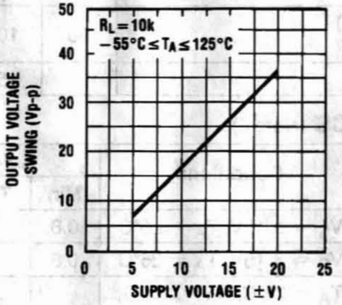
TL/H/9297-5

Typical Performance Characteristics (Continued)

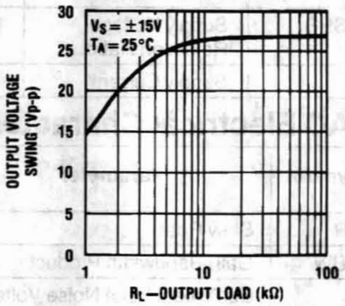
Negative Current Limit



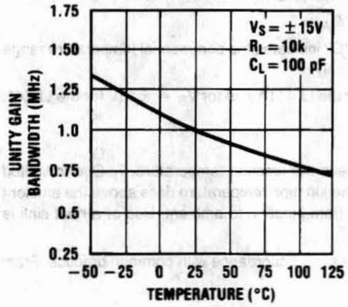
Output Voltage Swing



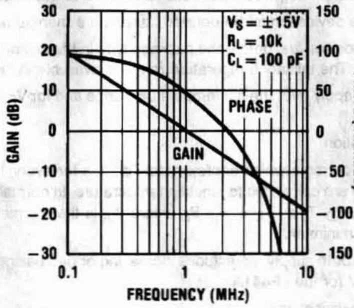
Output Voltage Swing



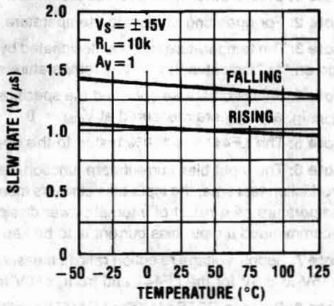
Gain Bandwidth



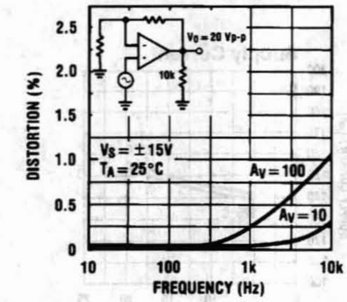
Bode Plot



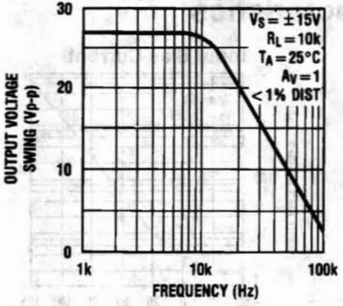
Slew Rate



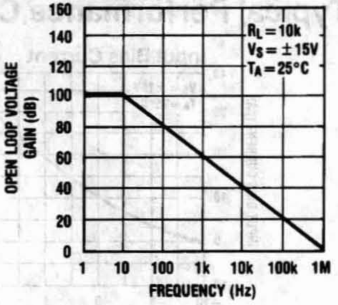
Distortion vs Frequency



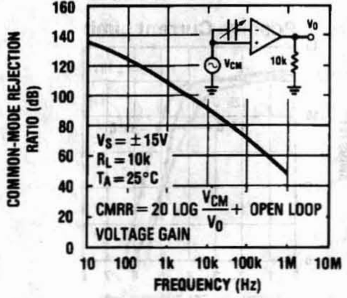
Undistorted Output Voltage Swing



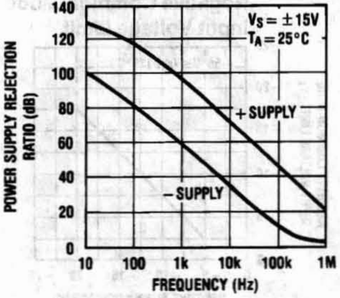
Open Loop Frequency Response



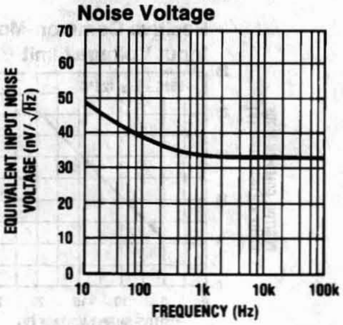
Common-Mode Rejection Ratio



Power Supply Rejection Ratio



Equivalent Input Noise Voltage



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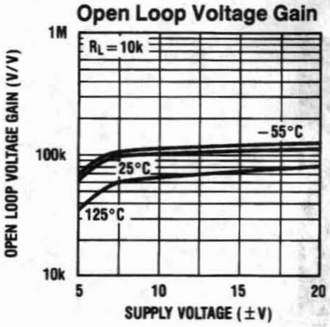
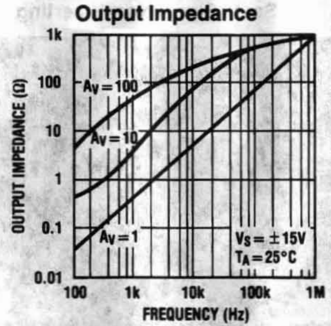
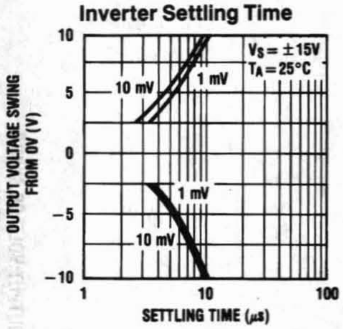
Typical Performance Characteristics (Continued)

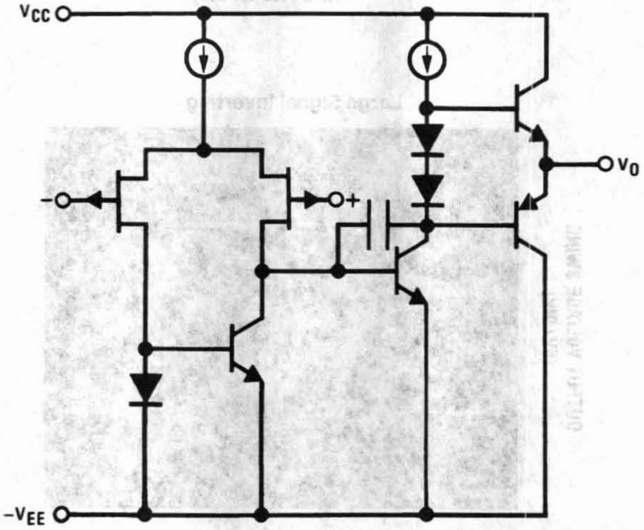

Open Loop Voltage Gain


Output Impedance


Inverter Settling Time

TL/H/9297-7

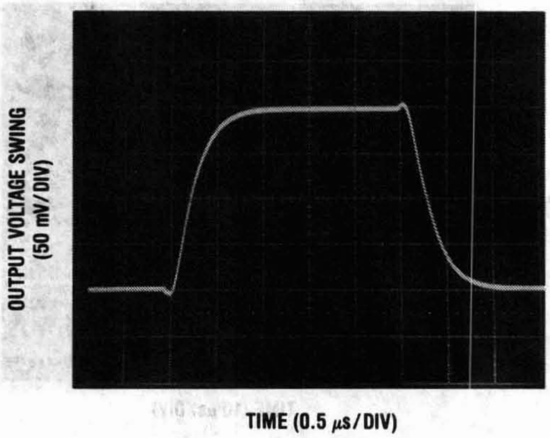
Simplified Schematic



TL/H/9297-3

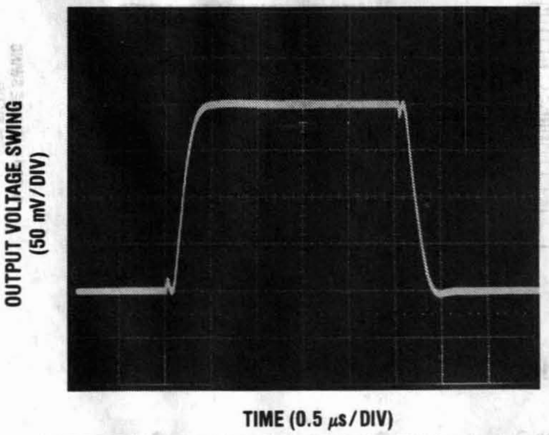
Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

Small Signal Inverting

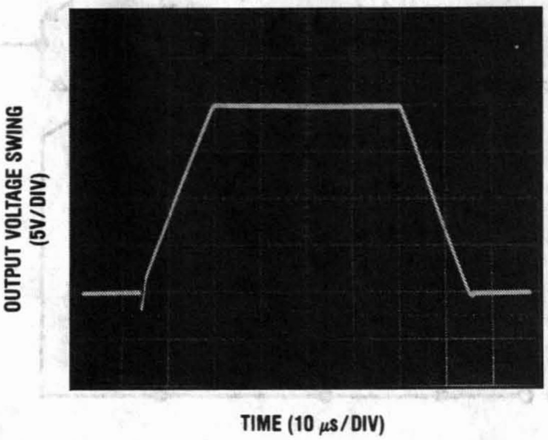


TL/H/9297-8

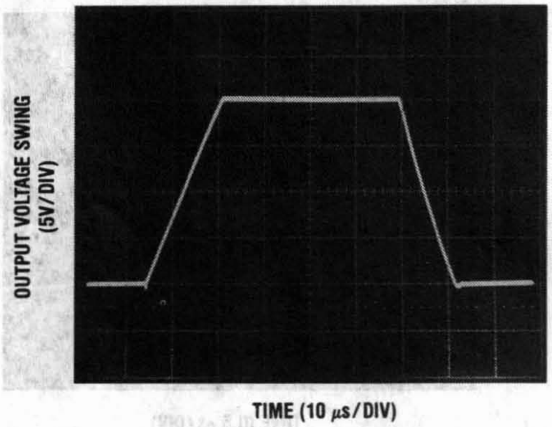
Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$ (Continued)



TL/H/9297–9



TL/H/9297–10



TL/H/9297–11

Application Hints

This device is a low power op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain, eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The amplifier is biased to allow normal circuit operation with power supplies of ±3V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

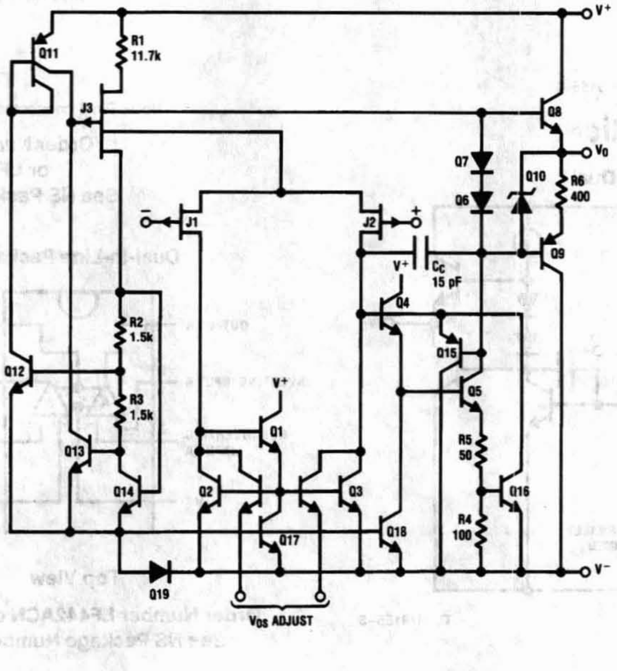
The amplifier will drive a 10 kΩ load resistance to ±10V over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket, as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input to AC ground) set the frequency of this pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency, of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



TL/H/9297-13

National Semiconductor

LF442 Dual Low Power JFET Input Operational Amplifier

General Description

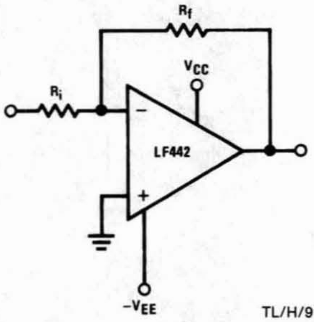
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/10 supply current of a LM1458	400 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	1 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/$\sqrt{Hz}$
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection



Rf
VCC
Ri
LF442
−VEE

TL/H/9155–1

Ordering Information

LF442XYZ

X indicates electrical grade

Y indicates temperature range

"M" for military

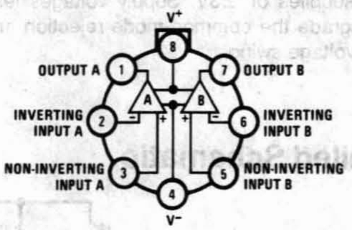
"C" for commercial

Z indicates package type

"H" or "N"

Connection Diagrams

Metal Can Package



V+
8
OUTPUT A
1
7
OUTPUT B
A
B
INVERTING INPUT A
2
6
INVERTING INPUT B
NON-INVERTING INPUT A
3
5
NON-INVERTING INPUT B
4
V−

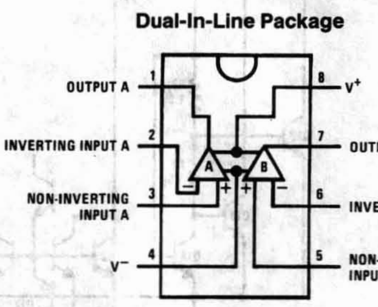
TL/H/9155–2

Top View

Note: Pin 4 connected to case

Order Number LF442AMH or LF442MH/883
See NS Package Number H08A

Dual-In-Line Package



OUTPUT A
1
8
V+
INVERTING INPUT A
2
7
OUTPUT B
A
B
NON-INVERTING INPUT A
3
6
INVERTING INPUT B
V−
4
5
NON-INVERTING INPUT B

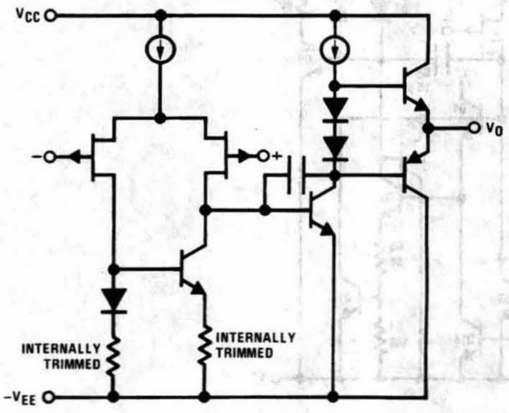
TL/H/9155–4

Top View

Order Number LF442ACN or LF442CN
See NS Package Number N08E

Simplified Schematic

½ Dual



VCC
VO
−
+
INTERNALLY TRIMMED
INTERNALLY TRIMMED
−VEE

TL/H/9155–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LF442A	LF442
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	H Package	N Package
T_j max	150°C	115°C
θ_{JA} (Typical)		
(Note 3)	65°C/W	114°C/W
(Note 4)	165°C/W	152°C/W
θ_{JC} (Typical)	21°C/W	
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \leq T_A \leq 150°C$	$-65°C \leq T_A \leq 150°C$
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance	Rating to be determined	

DC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions		LF442A			LF442			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.5	1.0		1.0	5.0	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$			7	10		7		μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 6 and 7)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 6 and 7)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\ k\Omega$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18 −17		±11	+14 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	90		dB
I_S	Supply Current				300	400		400	500	μA

AC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions	LF442A			LF442			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		nV/√Hz
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/√Hz

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: The value given is in 400 linear feet/min air flow.

Note 4: The value given is in static air.

Note 5: These devices are available in both the commercial temperature range 0°C ≤ T_A ≤ 70°C and the military temperature range −55°C ≤ T_A ≤ 125°C. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 6: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF442A and for $V_S = \pm 15V$ for the LF442. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

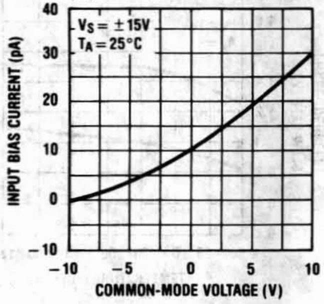
Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF442 and ±20V to ±5V for the LF442A.

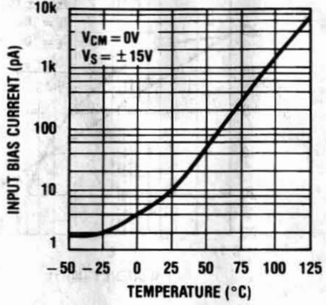
Note 9: Refer to RETS442X for LF442MH military specifications.

Typical Performance Characteristics

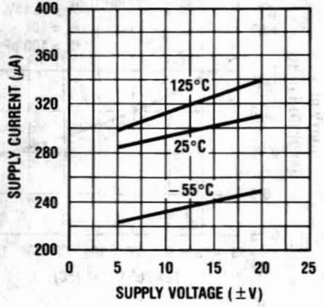
Input Bias Current



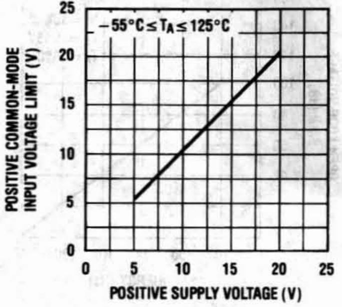
Input Bias Current



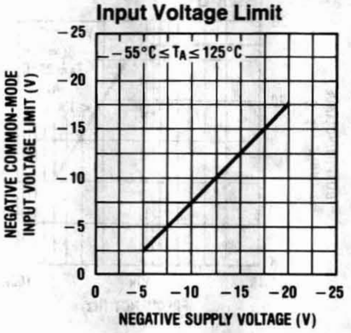
Supply Current



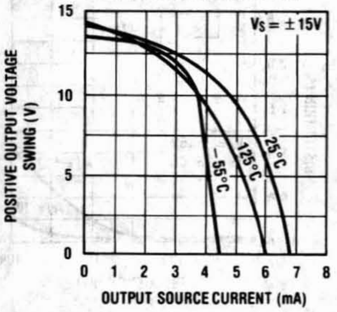
Positive Common-Mode Input Voltage Limit



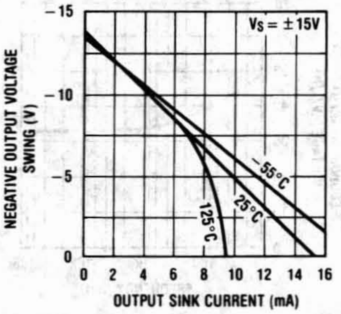
Negative Common-Mode Input Voltage Limit



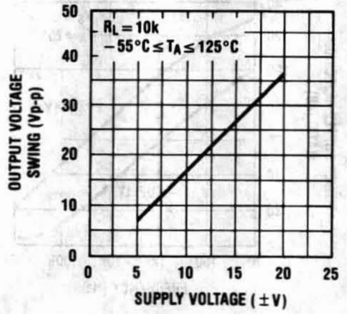
Positive Current Limit



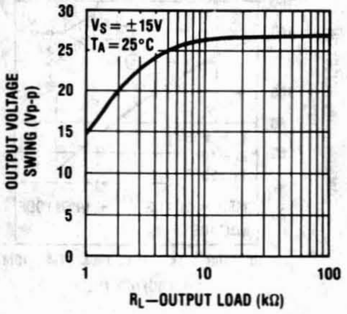
Negative Current Limit



Output Voltage Swing

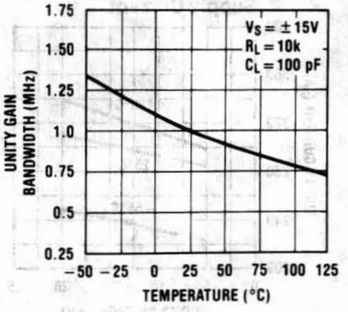


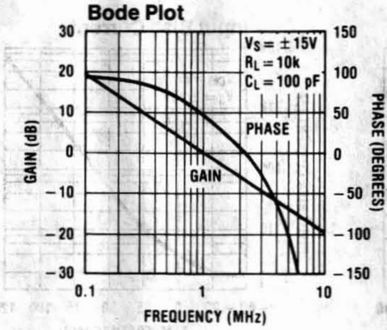
Output Voltage Swing

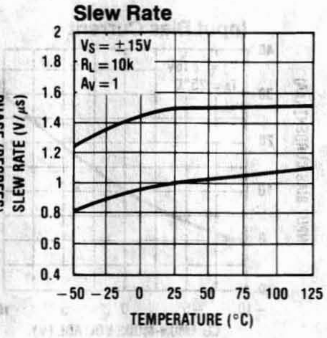


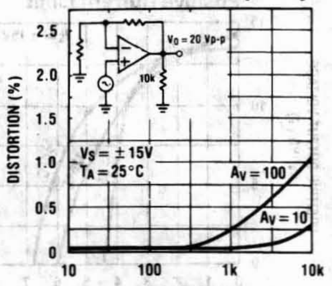
TL/H/9155–5

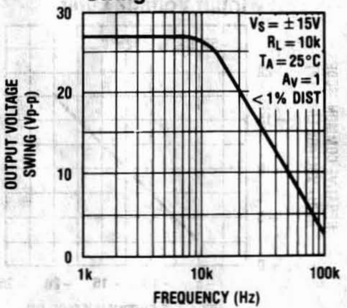
Typical Performance Characteristics (Continued)

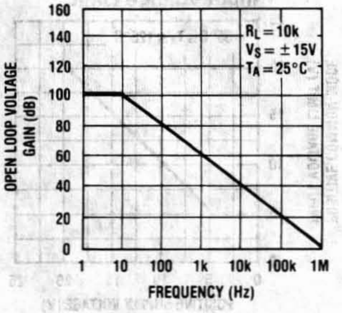

Gain Bandwidth

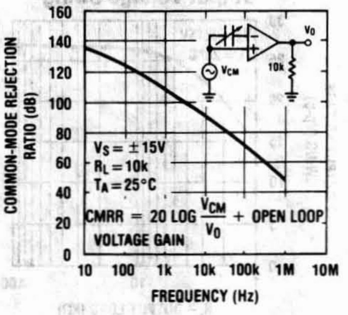

Bode Plot

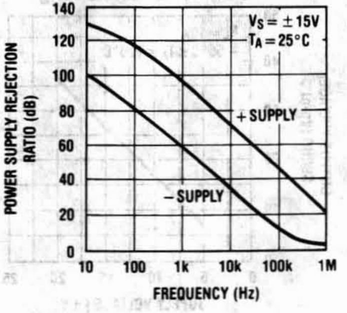

Slew Rate

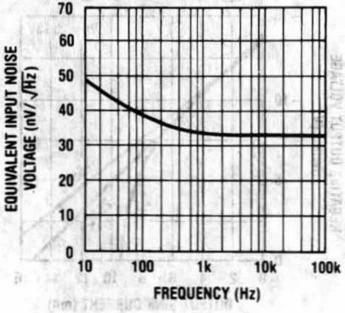

Distortion vs Frequency

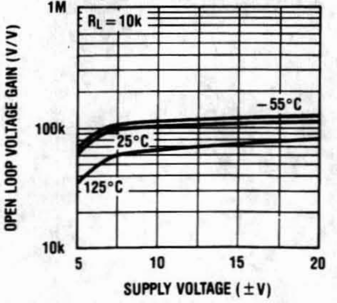

Undistorted Output Voltage Swing

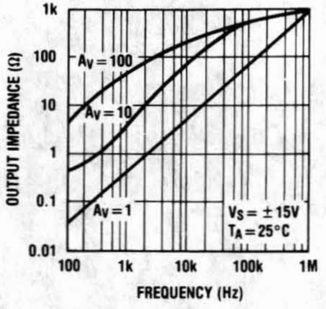

Open Loop Frequency Response

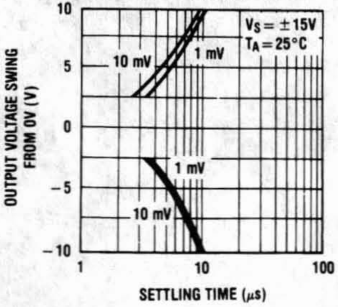

Common-Mode Rejection Ratio


Power Supply Rejection Ratio


Equivalent Input Noise Voltage


Open Loop Voltage Gain

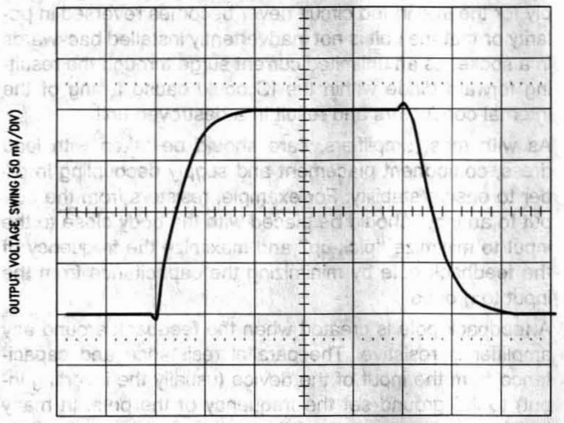

Output Impedance


Inverter Settling Time

TL/H/9155-6

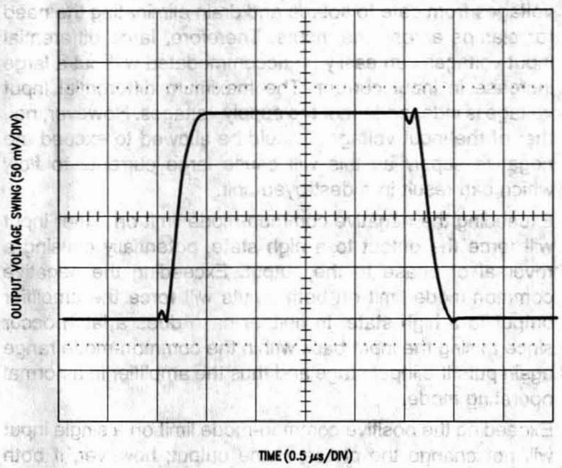
Pulse Response $R_L = 10\ k\Omega, C_L = 10\ pF$

Small Signal Inverting



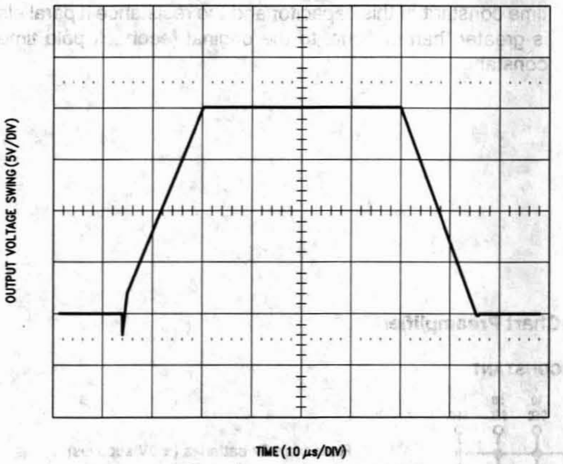
TL/H/9155–7

Small Signal Non-Inverting



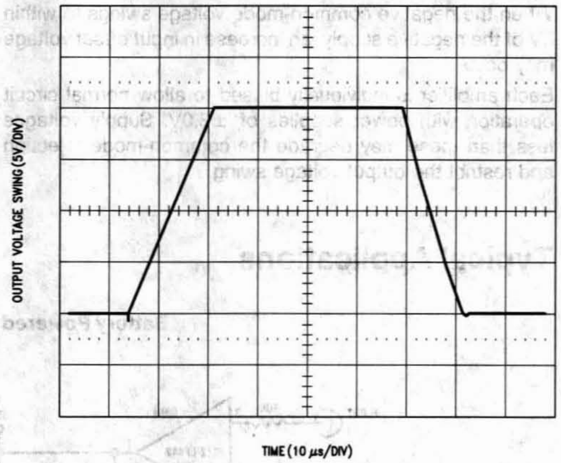
TL/H/9155–8

Large Signal Inverting



TL/H/9155–9

Large Signal Non-Inverting



TL/H/9155–10

Application Hints

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

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Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ± 10V over the full temperature range.

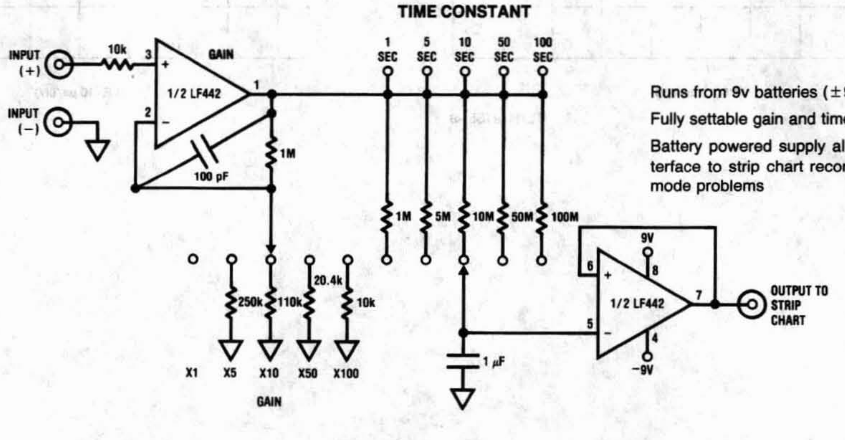
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequenty there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

Battery Powered Strip Chart Preamplifier



Runs from 9v batteries (±9V supplies)

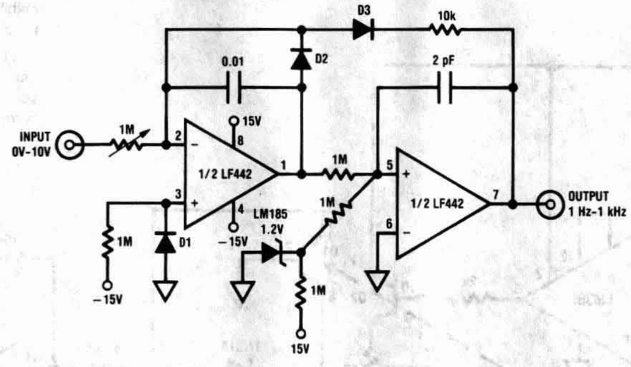
Fully settable gain and time constant

Battery powered supply allows direct plug-in interface to strip chart recorder without common-mode problems

TL/H/9155–11

Typical Applications (Continued)

"No FET" Low Power V → F Converter


D3
10k
0.01
D2
2 pF
15V
INPUT
0V-10V
1M
2
8
1/2 LF442
1
1M
5
1/2 LF442
7
OUTPUT
1 Hz-1 kHz
3
4
LM185
1.2V
1M
6
1M
D1
−15V
−15V
1M
15V

Trim 1M pot for 1 kHz full-scale output

15 mW power drain

No integrator reset FET required

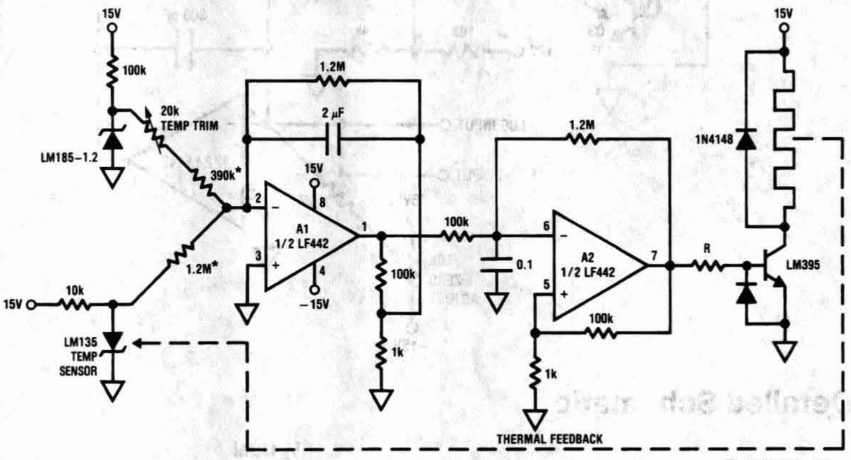
Mount D1 and D2 in close proximity

1% linearity to 1 kHz

TL/H/9155-12

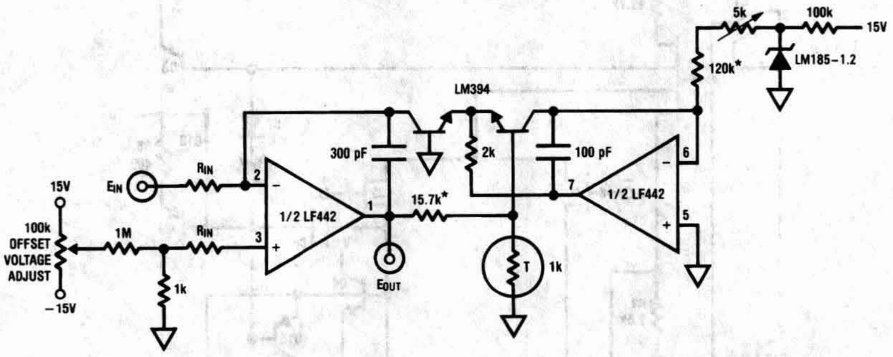
High Efficiency Crystal Oven Controller

- $T_{control}$ = 75°C
- A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature
- A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop
- Switched mode operation yields high efficiency
- 1% metal film resistor


15V
100k
20k
TEMP TRIM
LM185-1.2
390k*
1.2M
2 μF
15V
2
8
A1
1/2 LF442
1
3
4
−15V
1.2M*
15V
10k
LM135
TEMP
SENSOR
100k
100k
1k
1.2M
0.1
6
A2
1/2 LF442
7
5
100k
1k
R
15V
1N4148
LM395
THERMAL FEEDBACK

TL/H/9155-13

Conventional Log Amplifier


5k
100k
15V
120k*
LM185-1.2
LM394
300 pF
2k
100 pF
6
15V
E_{IN}
R_{IN}
2
1/2 LF442
1
15.7k*
7
1/2 LF442
5
100k
OFFSET
VOLTAGE
ADJUST
1M
R_{IN}
3
E_{OUT}
T
1k
1k
−15V

TL/H/9155-14

$$E_{OUT} = -\left[\log 10\left(\frac{E_{IN}}{R_{IN}}\right) + 5\right]$$

R_T = Tel Labs type Q81

Trim 5k for 10 μA through the 5k–120k combination

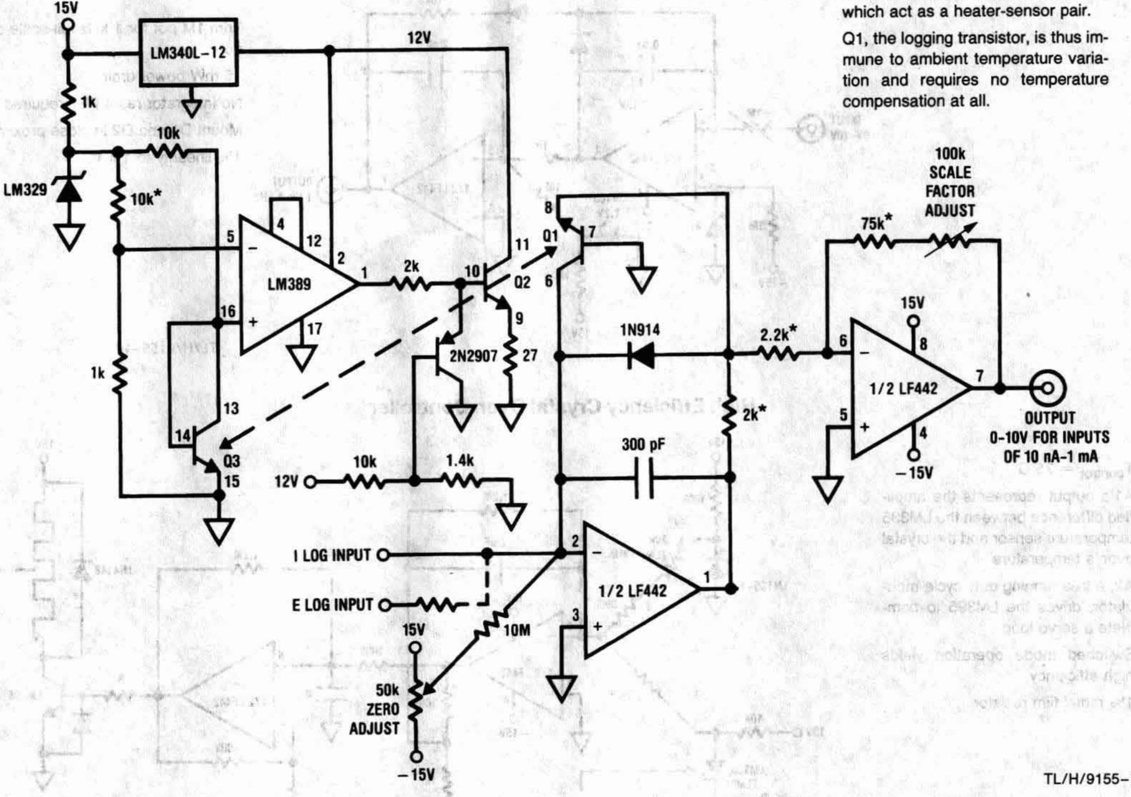
*1% film resistor

Typical Applications (Continued)

Unconventional Log Amplifier

Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair.

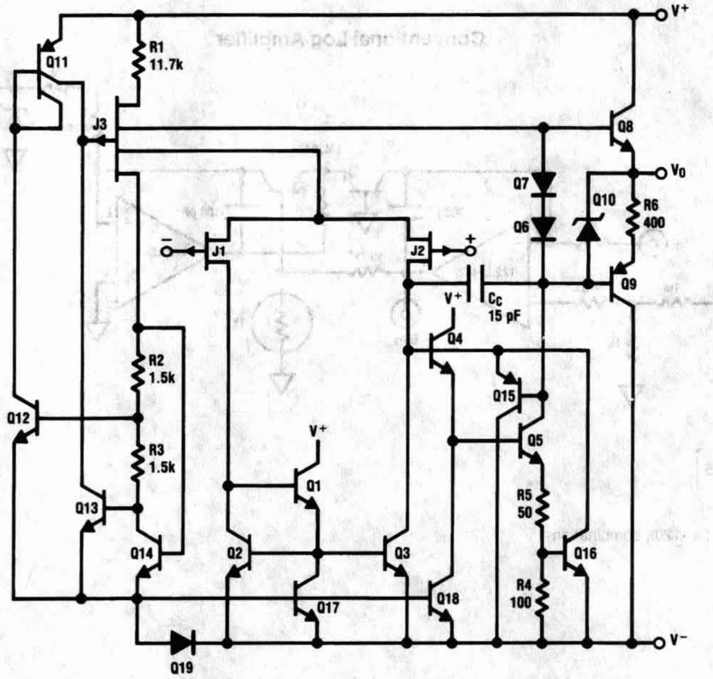
Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.


15V
LM340L-12
12V
1k
10k
LM329
10k*
5
4
12
2
LM389
1
2k
10
11
Q1
8
7
Q2
6
16
17
9
2N2907
27
1N914
1k
13
14
Q3
15
12V
10k
1.4k
300 pF
2k*
2.2k*
75k*
100k
SCALE
FACTOR
ADJUST
15V
6
8
1/2 LF442
7
5
4
−15V
OUTPUT
0–10V FOR INPUTS
OF 10 nA–1 mA
I LOG INPUT
E LOG INPUT
2
1/2 LF442
1
3
15V
10M
50k
ZERO
ADJUST
−15V

TL/H/9155–15

Detailed Schematic

½ Dual


V+
Q11
R1
11.7k
J3
Q8
Vo
Q7
Q10
R6
400
Q6
−
J1
J2
+
Q9
V+
Cc
15 pF
Q4
R2
1.5k
Q15
Q12
R3
1.5k
V+
Q5
Q1
R5
50
Q13
Q14
Q2
Q3
Q16
Q17
Q18
R4
100
Q19
V−

TL/H/9155–16

National Semiconductor

LF444 Quad Low Power JFET Input Operational Amplifier

General Description

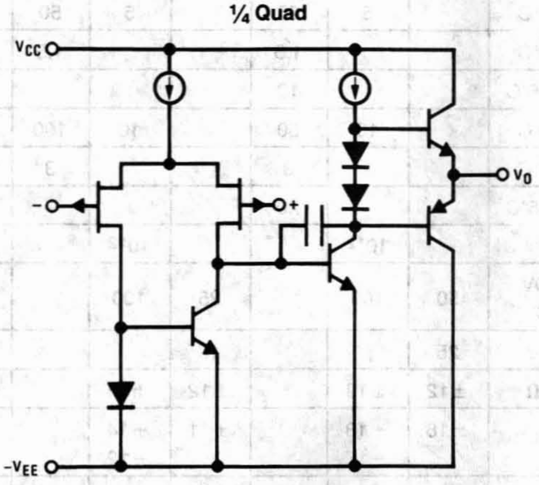
The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Features

■ ¼ supply current of a LM148	200 µA/Amplifier (max)
■ Low input bias current	50 pA (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/µs
■ Low noise voltage for low power	35 nV/$\sqrt{\text{Hz}}$
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

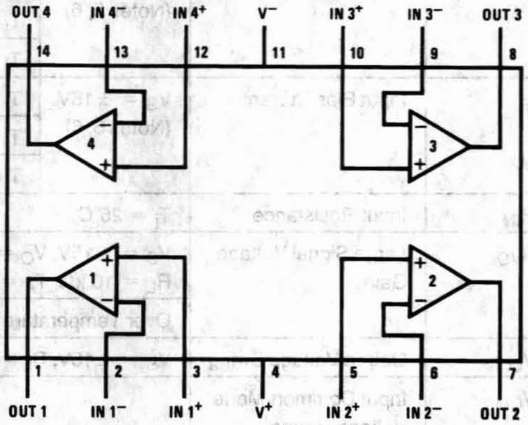
Simplified Schematic



TL/H/9156-1

Connection Diagram

Dual-In-Line Package



TL/H/9156-2

Top View

Order Number LF444AMD, LF444CM, LF444ACN, LF444CN or LF444MD/883
See NS Package Number D14E, M14A or N14A

Ordering Information

LF444XYZ

X indicates electrical grade

Y indicates temperature range
"M" for military, "C" for commercial

Z indicates package type "D", "M" or "N"

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF444A	LF444
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
	D Package	**N, M Packages**
Power Dissipation (Notes 3 and 9)	900 mW	670 mW
T_j max	150°C	115°C
θ_{jA} (Typical)	100°C/W	85°C/W

	LF444A/LF444
Operating Temperature Range	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$
ESD Tolerance (Note 10)	Rating to be determined
Soldering Information	
Dual-In-Line Packages (Soldering, 10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF444A Min	LF444A Typ	LF444A Max	LF444 Min	LF444 Typ	LF444 Max	Units
V_{OS}	Input Offset Voltage	$R_S = 10k, T_A = 25°C$			2	5		3	10	mV
		$0°C \le T_A \le +70°C$				6.5			12	mV
		$-55°C \le T_A \le +125°C$				8				mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$			10			10		μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5, 6)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5, 6)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 10\ k\Omega, T_A = 25°C$		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V, R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18 −17		±11	+14 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	90		dB
I_S	Supply Current				0.6	0.8		0.6	1.0	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF444A			LF444			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier-to-Amplifier Coupling			−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		1			1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		1			1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/$\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF444A is available in both the commercial temperature range 0°C ≤ T_A ≤ 70°C and the military temperature range −55°C ≤ T_A ≤ 125°C. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "D" package only.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF444A and for $V_S = \pm 15V$ for the LF444. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF444 and from ±20V to ±5V for the LF444A.

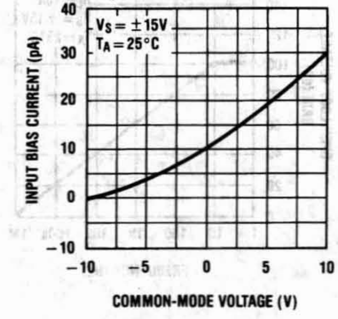
Note 8: Refer to RETS444X for LF444MD military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

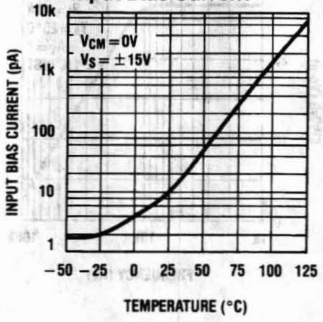
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

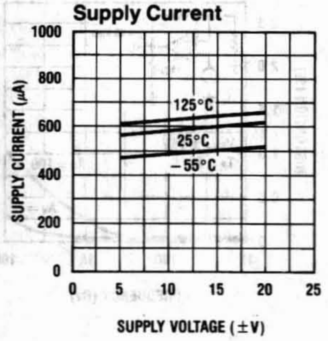
Input Bias Current



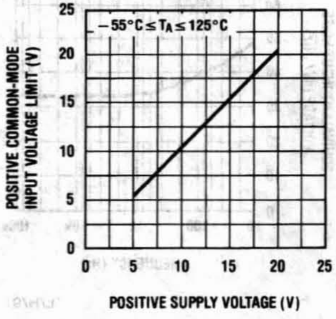
Input Bias Current



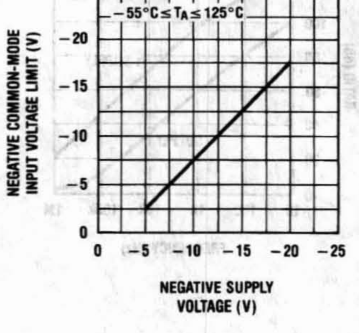
Supply Current



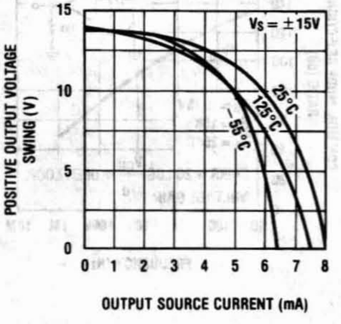
Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit



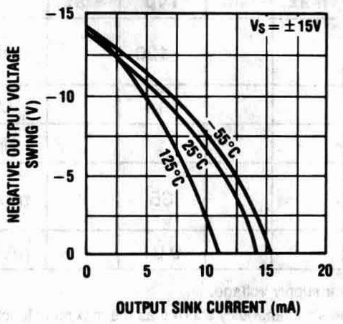
Positive Current Limit



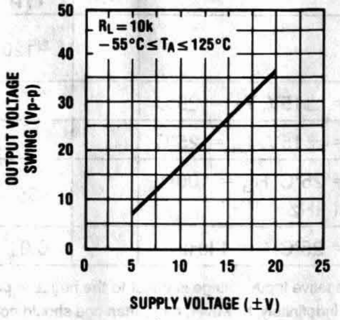
TL/H/9156–3

Typical Performance Characteristics (Continued)

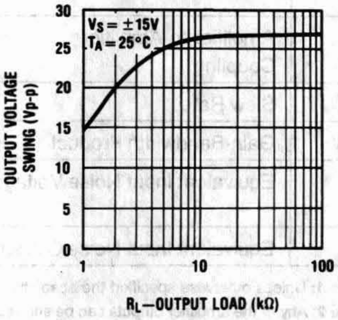
Negative Current Limit



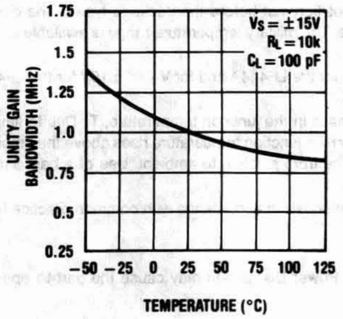
Output Voltage Swing



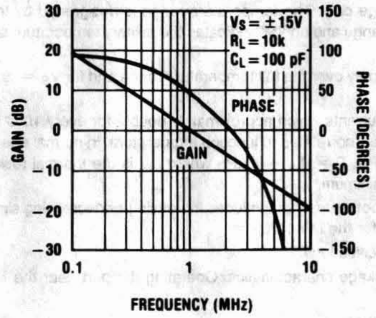
Output Voltage Swing



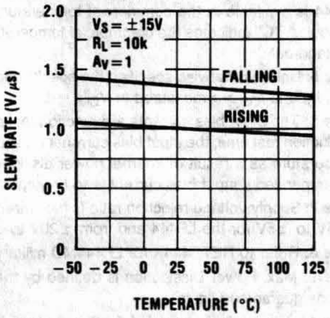
Gain Bandwidth



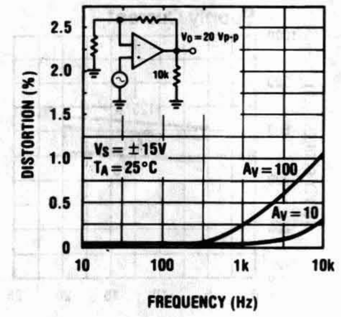
Bode Plot



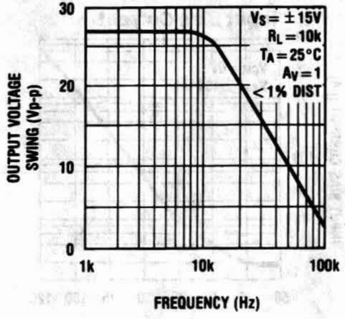
Slew Rate



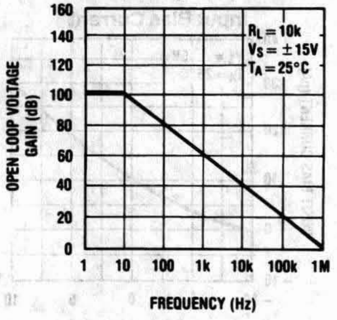
Distortion vs Frequency



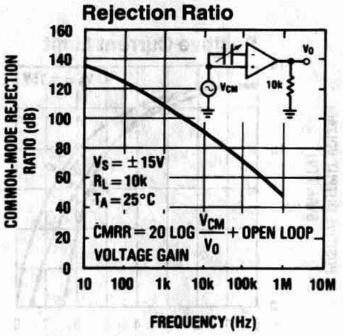
Undistorted Output Voltage Swing



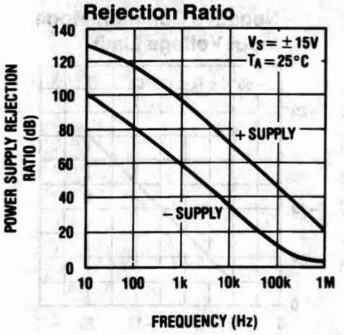
Open Loop Frequency Response



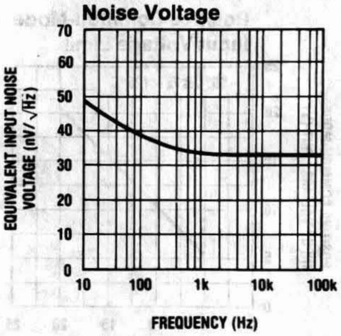
Common-Mode Rejection Ratio



Power Supply Rejection Ratio

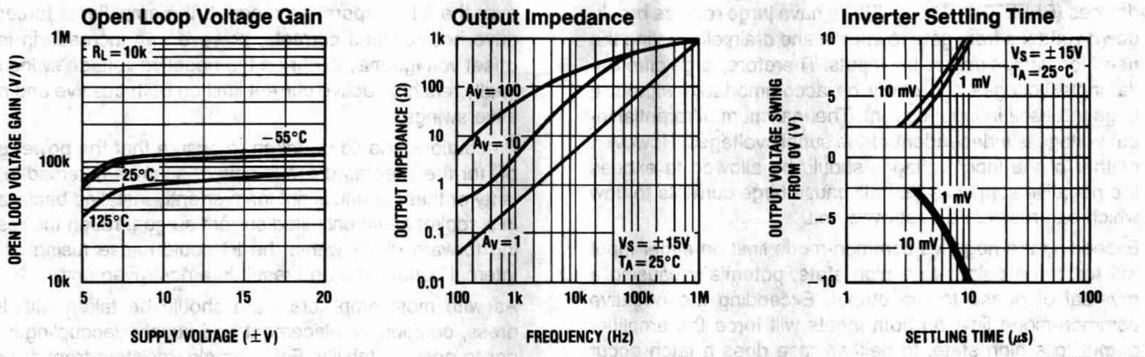


Equivalent Input Noise Voltage



TL/H/9156–4

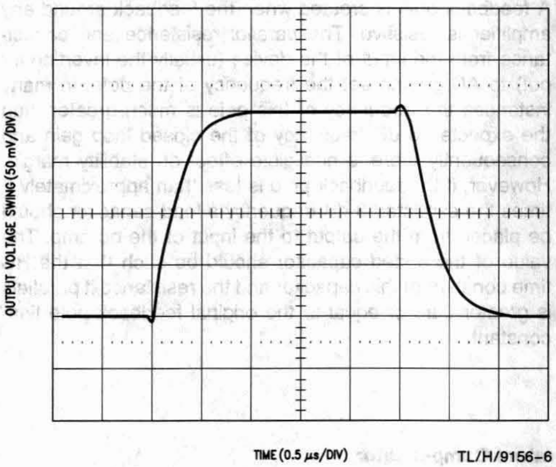
Typical Performance Characteristics (Continued)


Open Loop Voltage Gain
Output Impedance
Inverter Settling Time

TL/H/9156–5

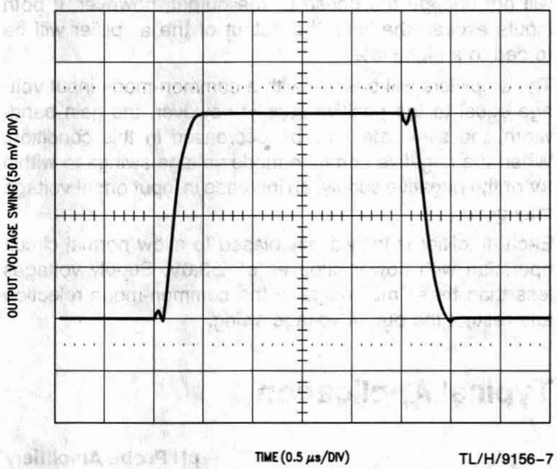
Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

Small Signal Inverting



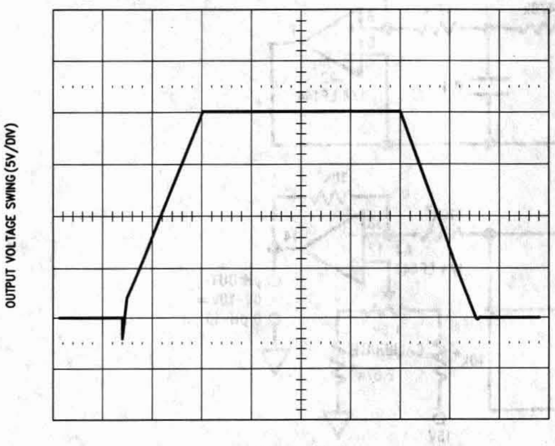
TL/H/9156–6

Small Signal Non-Inverting



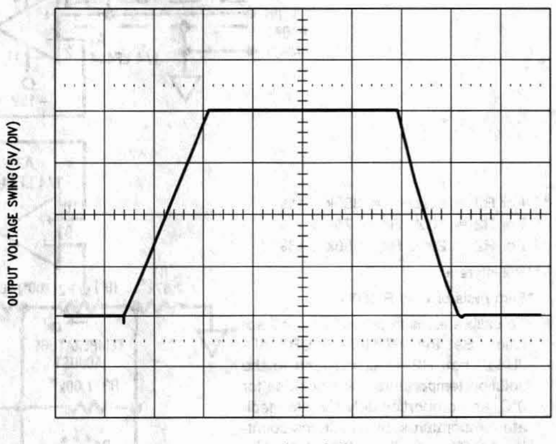
TL/H/9156–7

Large Signal Inverting



TL/H/9156–8

Large Signal Non-Inverting



TL/H/9156–9

Application Hints

This device is a quad low power op amp with JFET input devices (BI-FET™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

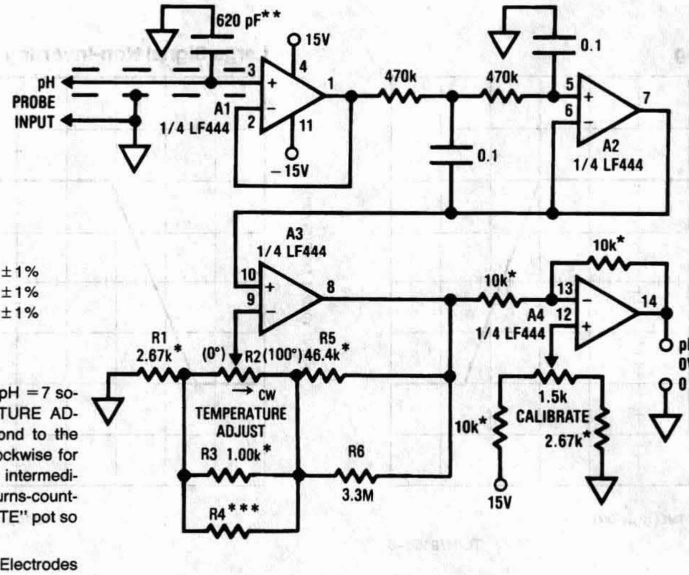
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

pH Probe Amplifier/Temperature Compensator



***For R2 = 50k, R4 = 330k ±1%
For R2 = 100k, R4 = 75k ±1%
For R2 = 200k, R4 = 56k ±1%

**Polystyrene

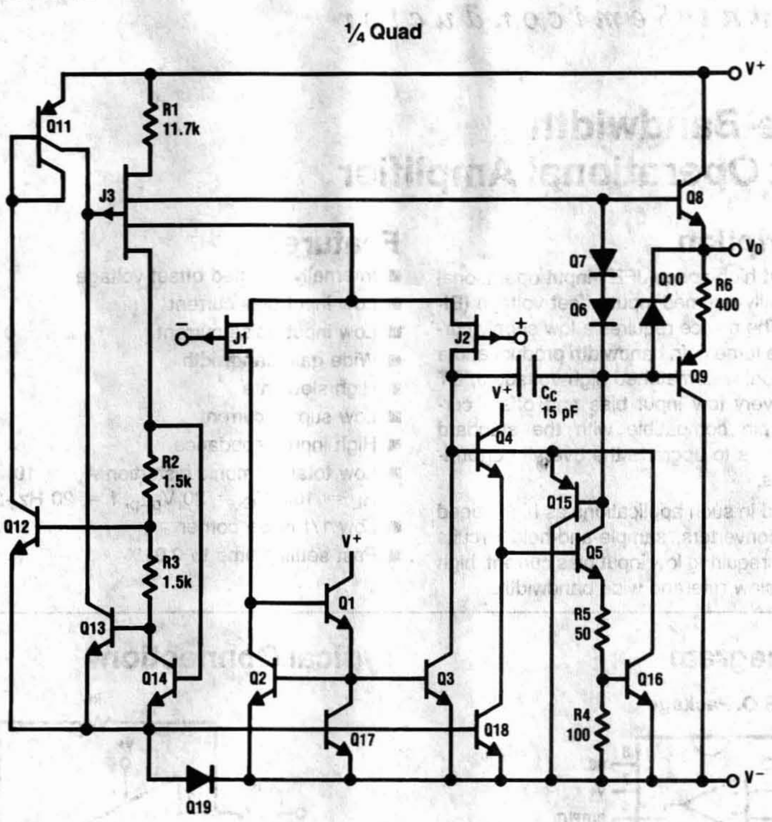
*Film resistor type RN60C

To calibrate, insert probe in pH = 7 solution. Set the "TEMPERATURE ADJUST" pot, R2, to correspond to the solution temperature: full clockwise for 0°C, and proportionately for intermediate temperatures, using a turns-counting dial. Then set "CALIBRATE" pot so output reads 7V.

Typical probe = Ingold Electrodes #465-35

TL/H/9156–10

Detailed Schematic


¼ Quad
V+
Q11
R1
11.7k
J3
Q8
Q7
Q6
Q10
R6
400
V0
−
J1
J2
+
Cc
15 pF
Q9
V+
Q4
R2
1.5k
Q15
Q12
Q5
R3
1.5k
V+
Q1
R5
50
Q13
Q14
Q2
Q3
Q16
R4
100
Q18
Q17
V−
Q19

TL/H/9156–11

National Semiconductor

LF451 Wide-Bandwidth JFET-Input Operational Amplifier

General Description

The LF451 is a low-cost high-speed JFET-input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF451 is pin compatible with the standard LM741, allowing designers to upgrade the overall performance of existing designs.

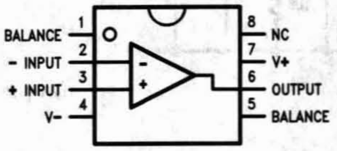
The LF451 may be used in such applications as high-speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	5.0 mV (max)
■ Low input bias current	50 pA (typ)
■ Low input noise current	$0.01\ \text{pA}/\sqrt{\text{Hz}}$ (typ)
■ Wide gain bandwidth	4 MHz (typ)
■ High slew rate	13 V/μs (typ)
■ Low supply current	3.4 mA (max)
■ High input impedance	$10^{12}\Omega$ (typ)
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20\ V_{p-p}$, f = 20 Hz–20 kHz	<0.02% (typ)
■ Low 1/f noise corner	50 Hz (typ)
■ Fast settling time to 0.01%	2 μs (typ)

Connection Diagram

S.O. Package

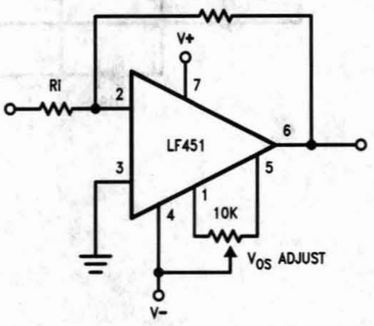


TL/H/9660-2

Top View

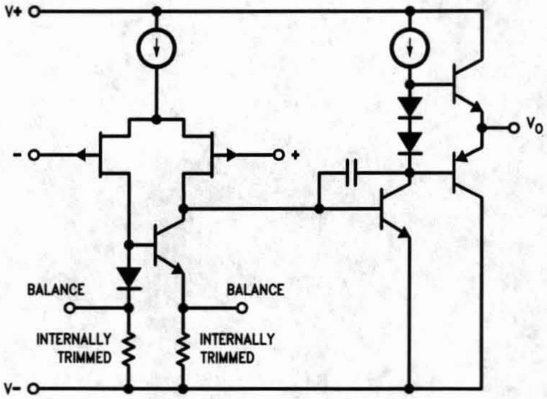
Order Number LF451CM
See NS Package Number M08A

Typical Connection



TL/H/9660-1

Simplified Schematic



TL/H/9660-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Input Voltage Range	$V^- \le V_{IN} \le V^+$
Differential Input Voltage (Note 2)	±30V
Junction Temperature (T_J MAX)	150°C
Output Short Circuit Duration	Continuous
Power Dissipation (Note 3)	500 mW
ESD Tolerance	TBD
Soldering Information (Note 5)	
SO Package: Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF451CM	$0°C \le T_A \le +70°C$
Junction Temperature ($T_{J\ max}$)	125°C
Supply Voltage ($V^+ - V^-$)	10V to 32V

DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF451CM			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
V_{OS}	Maximum Input Offset Voltage	$R_S = 10\ k\Omega$, (Note 10)	0.3	5		mV
I_{OS}	Maximum Input Offset Current	(Notes 9, 10) $T_J = 25°C$ $T_J = 70°C$	25	100	 **2**	pA nA
I_B	Maximum Input Bias Current	(Notes 9, 10) $T_J = 25°C$ $T_J = 70°C$	50	200	 **4**	pA nA
R_{IN}	Input Resistance	$T_J = 25°C$	10^{12}			Ω
AVOL	Minimum Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2\ k\Omega$ (Note 10)	200	50	**25**	V/mV
V_O	Minimum Output Voltage Swing	$R_L = 10k$	±13.5	±12	**±12**	V
V_{CM}	Minimum Input Common Mode Voltage Range		+14.5 −11.5	+11 −11	**+11** **−11**	V V
CMRR	Minimum Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	100	80	**80**	dB
PSRR	Minimum Supply Voltage Rejection Ratio	(Note 11)	100	80	**80**	dB
I_S	Maximum Supply Current			3.4	**3.4**	mA

AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF451CM			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
SR	Slew Rate	$A_V = +1$	13	8		V/μs
GBW	Minimum Gain-Bandwidth Product	f = 100 kHz	4	2.7		MHz
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 1 kHz	25			$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$R_S = 100\Omega$, f = 1 kHz	0.01			$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: When the input voltage exceeds the power supplies, the current should be limited to 1 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J\ MAX - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation $T_{J\ max} = 125°C$. The typical thermal resistance (θ_{JA}) of the LF451CM when board-mounted is 170°C/W.

Note 5: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Note 6: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed to National's AOQL, but not 100% tested.

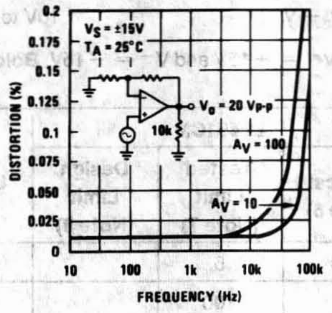
Note 9: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, the input bias currents are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA}P_D$ where θ_{JA} is the thermal resistance from junction to ambient.

Note 10: V_{OS}, I_B, AVOL, and I_{OS} are measured at $V_{CM} = 0V$.

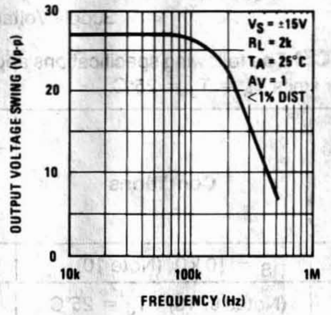
Note 11: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

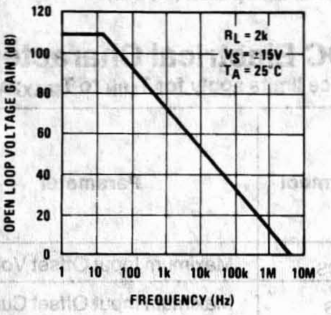
Distortion vs Frequency



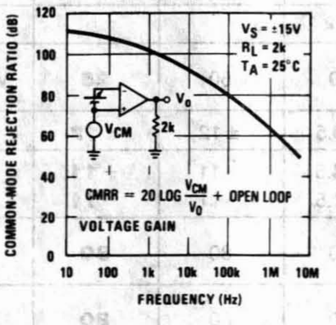
Undistorted Output Voltage Swing



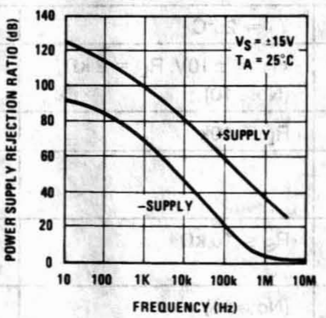
Open Loop Frequency Response



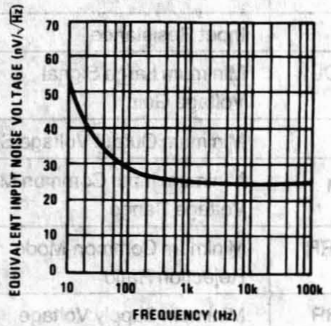
Common-Mode Rejection Ratio



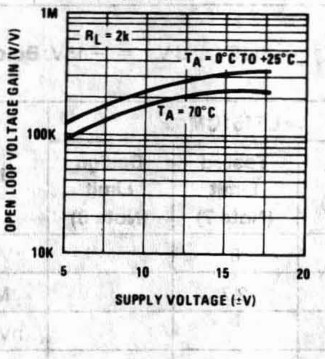
Power Supply Rejection Ratio



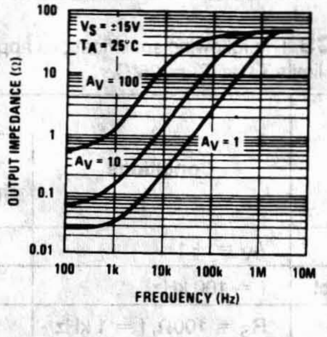
Equivalent Input Noise Voltage



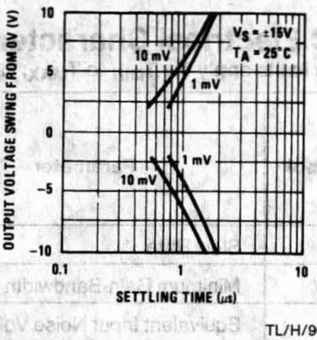
Open Loop Voltage Gain (V/V)



Output Impedance



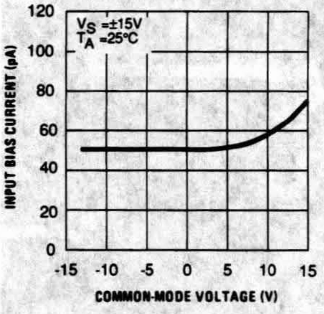
Inverter Settling Time



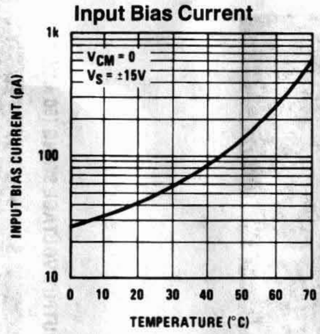
TL/H/9660–5

Typical Performance Characteristics (Continued)

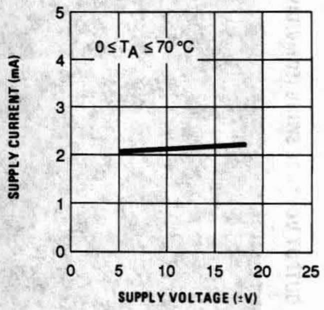
Input Bias Current



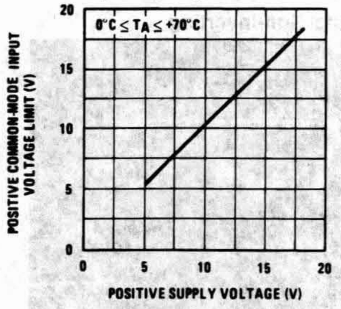
Input Bias Current



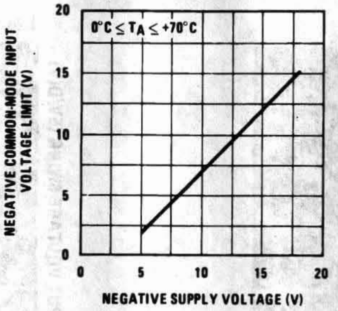
Supply Current



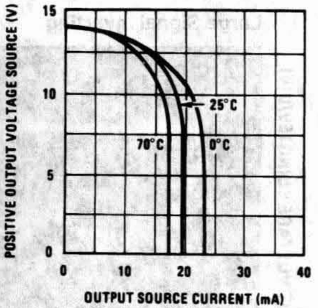
Positive Common-Mode Input Voltage Limit



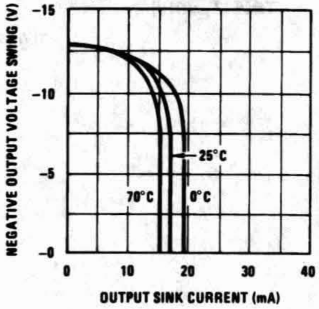
Negative Common-Mode Input Voltage Limit



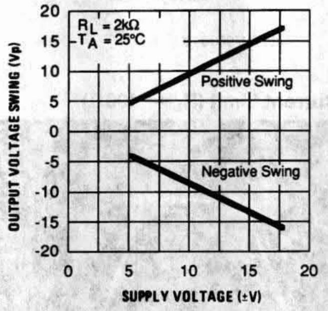
Positive Current Limit



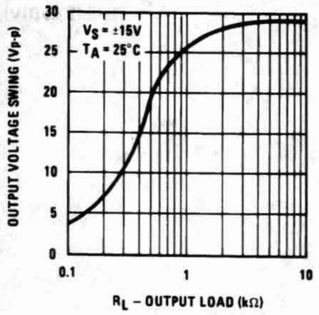
Negative Current Limit



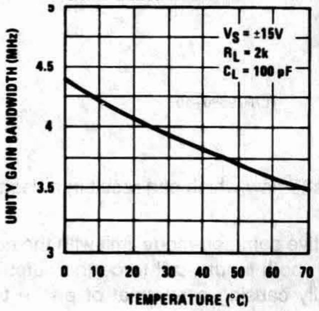
Voltage Swing



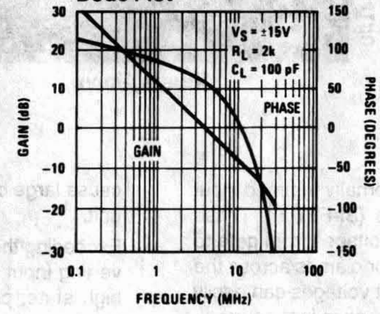
Output Voltage Swing



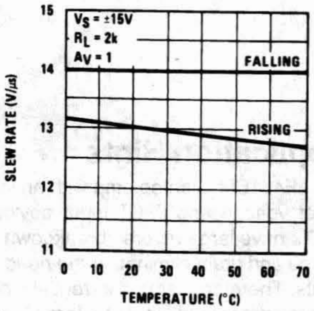
Gain Bandwidth



Bode Plot



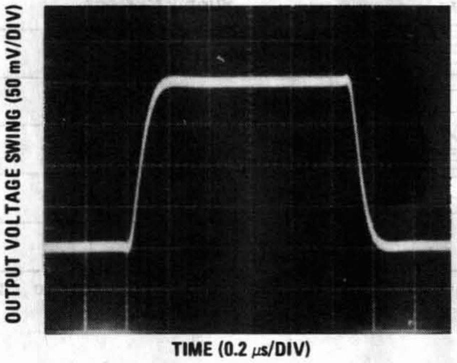
Slew Rate



TL/H/9660–4

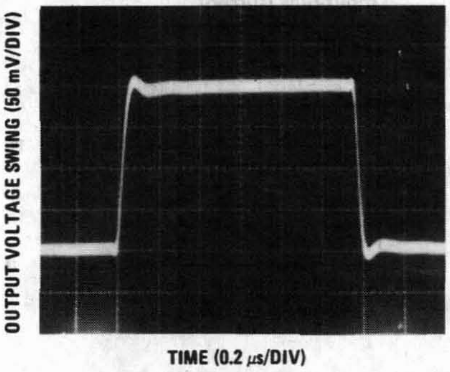
Pulse Response

Small Signal Inverting



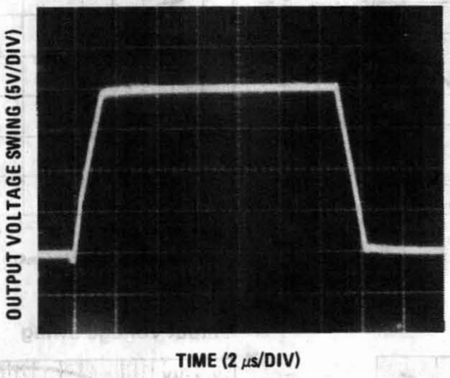
TL/H/9660–6

Small Signal Non-Inverting



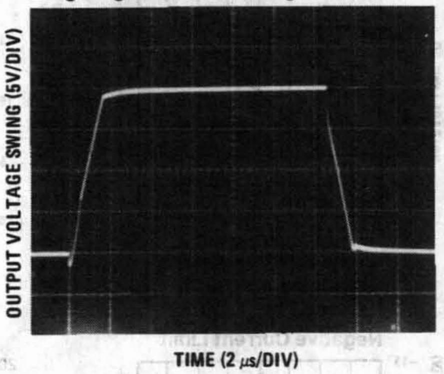
TL/H/9660–7

Large Signal Inverting



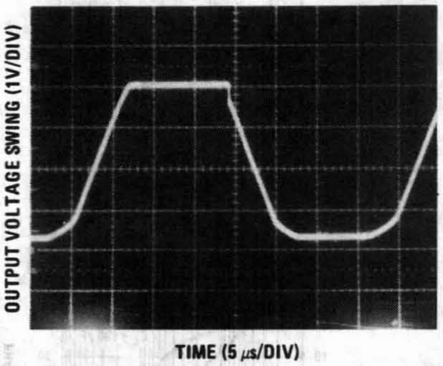
TL/H/9660–8

Large Signal Non-Inverting



TL/H/9660–9

Current Limit ($R_L = 100\Omega$)



TL/H/9660–10

Application Hints

The LF451CM is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit with the non-inverting input, or with both inputs, will force the output to a high state, potentially causing a reversal of phase to the output.

In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF451 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF451 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

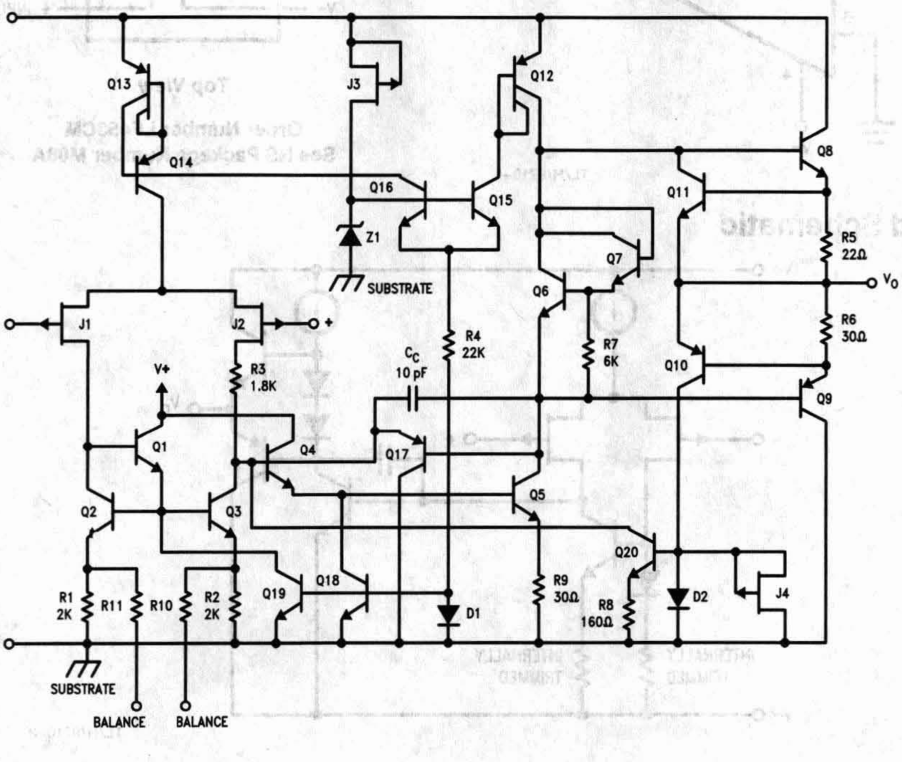
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

The benefit of the S.O. package results from its very small size. It follows, however, that the die inside the S.O. package is less protected from external physical forces than a die in a standard DIP would be, because there is so much less plastic in the S.O. Therefore, not following certain precautions when board mounting the LF451CM can put mechanical stress on the die, lead frame, and/or bond wires. This can cause shifts in the LF451CM's parameters, even causing them to exceed limits specified in the Electrical Characteristics. For recommended practices in LF451CM surface mounting refer to Application Note AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" and to Section 6 "Surface Mount" found in any Rev. 1 Linear Databook volume.

Detailed Schematic



TL/H/9660-11

National Semiconductor

LF453 Wide-Bandwidth Dual JFET-Input Operational Amplifiers

General Description

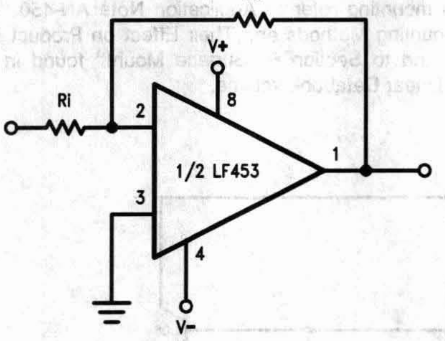
The LF453 is a low-cost, high-speed, dual JFET-input operational amplifier with an internally trimmed input offset voltage (BI-FET II technology). The device requires a low supply current and yet the amplifiers maintain a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF453 is pin compatible with the standard LM1558, allowing designers to upgrade the overall performance of existing designs.

The LF453 may be used in such applications as high-speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	5.0 mV (max)
■ Low input bias current	50 pA (typ)
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$ (typ)
■ Wide gain bandwidth	4 MHz (typ)
■ High slew rate	13 V/µs (typ)
■ Low supply current	6.5 mA (max)
■ High input impedance	$10^{12}\Omega$ (typ)
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20\ V_{p-p}$, f = 20 Hz–20 kHz	<0.02% (typ)
■ Low 1/f noise corner	50 Hz (typ)
■ Fast settling time to 0.01%	2 µs (typ)

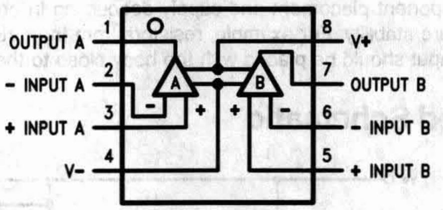
Typical Connection



TL/H/9710–1

Connection Diagram

SO Package

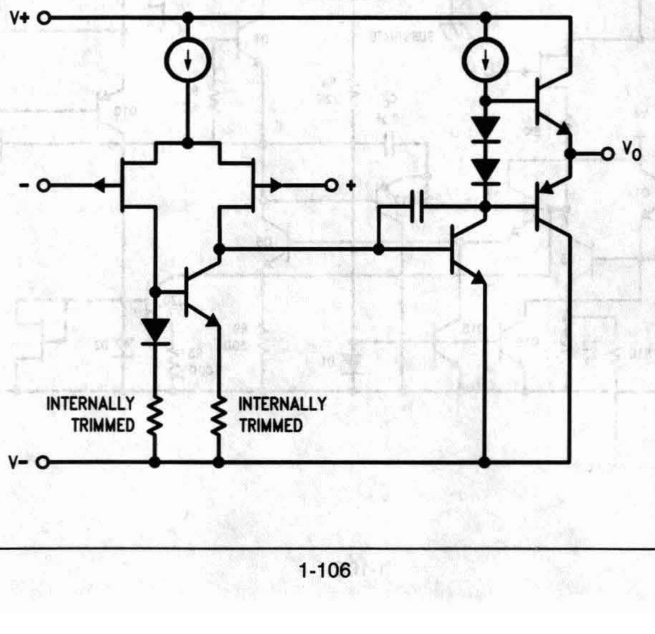


TL/H/9710–2

Top View

Order Number LF453CM
See NS Package Number M08A

Simplified Schematic



TL/H/9710–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Input Voltage Range	$V^- \leq V_{IN} \leq V^+$
Differential Input Voltage (Note 2)	±30V
Junction Temperature (T_J MAX)	150°C
Output Short Circuit Duration	Continuous
Power Dissipation (Note 3)	500 mW
ESD Tolerance	TBD

Soldering Information (Note 4)

SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
LF453CM	$0°C \leq T_A + 70°C$
Junction Temperature ($T_{J\ max}$)	125°C
Supply Voltage ($V^+ - V^-$)	10V to 32V

DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Boldface limits apply for T_{MIN} to T_{MAX}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF453CM			Units
			Typical (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
V_{OS}	Maximum Input Offset Voltage	$R_S = 10\ k\Omega$, (Note 9)		5		mV
I_{OS}	Maximum Input Offset Current	(Notes 8, 9) $T_J = 25°C$ $T_J = 70°C$	25	100	 **2**	pA nA
I_B	Maximum Input Bias Current	(Notes 8, 9) $T_J = 25°C$ $T_J = 70°C$	50	200	 **4**	pA nA
R_{IN}	Input Resistance	$T_J = 25°C$	10^{12}			Ω
AVOL	Minimum Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2\ k\Omega$ (Note 9)	200	50	**25**	V/mV
V_O	Minimum Output Voltage Swing	$R_L = 10k$	±13.5	±12	**±12**	V
V_{CM}	Minimum Input Common Mode Voltage Range		+14.5 −11.5	+11 −11	**+11** **−11**	V V
CMRR	Minimum Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	100	80	**80**	dB
PSRR	Minimum Supply Voltage Rejection Ratio	(Note 10)	100	80	**80**	dB
I_S	Maximum Supply Current			6.5	**6.5**	mA

AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. Limits apply for $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF453CM			Units
			Typical (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
SR	Slew Rate	$A_V = +1$	13	8		V/µs
GBW	Minimum Gain-Bandwidth Product	f = 100 kHz	4	2.7		MHz
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 1 kHz	25			$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$R_S = 100\Omega$, f = 1 kHz	0.01			$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: When the input voltage exceeds the power supplies, the current should be limited to 1 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J\ MAX - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation $T_{J\ max} = 125°C$. The typical thermal resistance (Θ_{JA}) of the LF453CM when board-mounted is 160°C/W.

Note 4: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (section titled "Surface Mount") for other methods of soldering surface mount devices.

Note 5: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Design limits are guaranteed to National's AOQL, but not 100% tested.

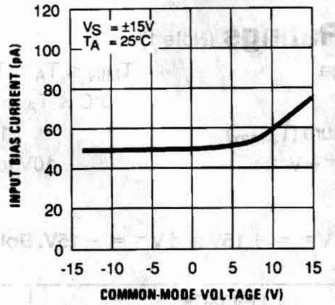
Note 8: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, the input bias currents are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \Theta_{JA} P_D$ where Θ_{JA} is the thermal resistance from junction to ambient.

Note 9: V_{OS}, I_B, AVOL and I_{OS} are measured at $V_{CM} = 0V$.

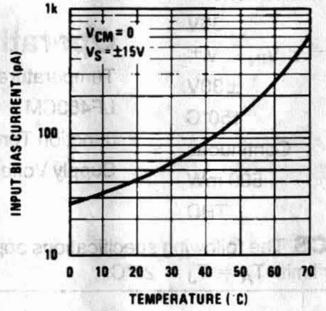
Note 10: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

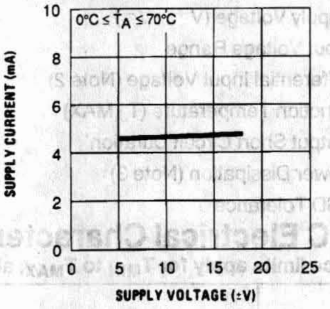
Input Bias Current



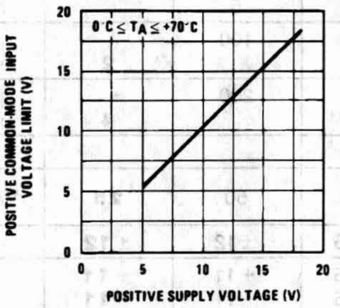
Input Bias Current



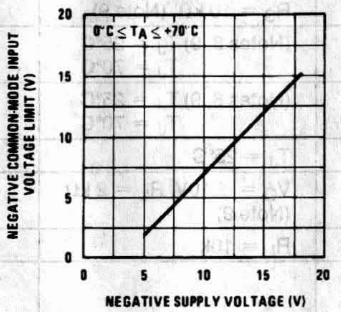
Supply Current



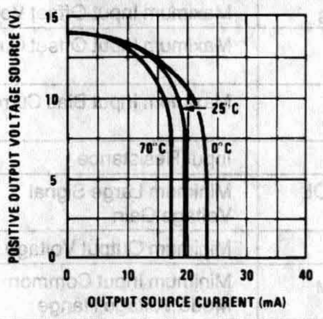
Positive Common-Mode Input Voltage Limit



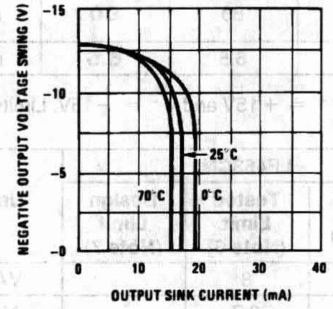
Negative Common-Mode Input Voltage Limit



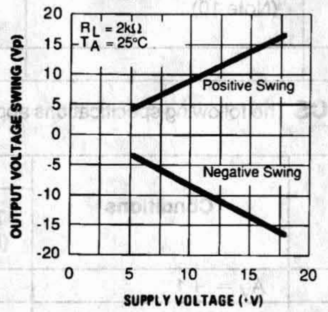
Positive Current Limit



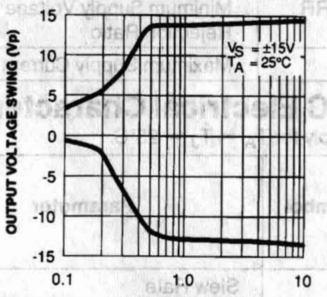
Negative Current Limit



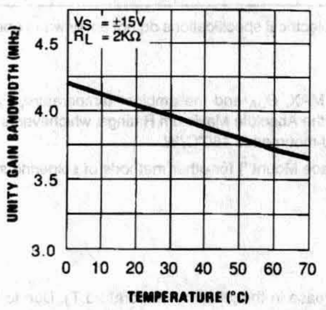
Voltage Swing



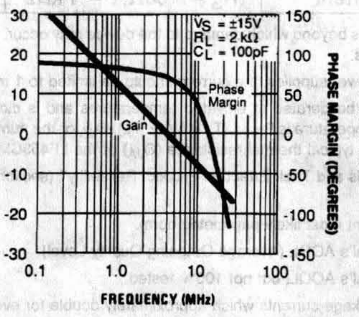
Output Voltage Swing



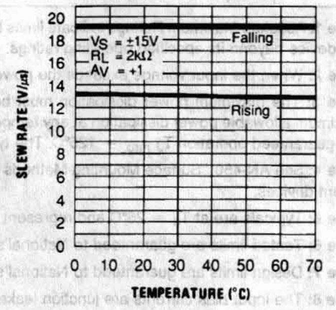
Gain Bandwidth



Bode Plot



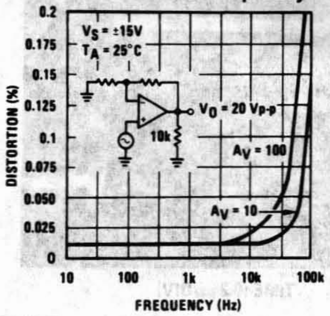
Slew Rate



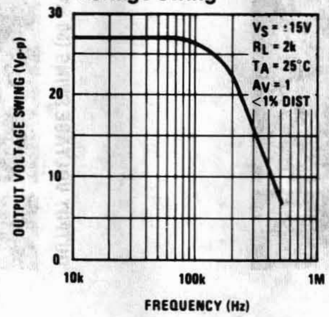
TL/H/9710–4

Typical Performance Characteristics (Continued)

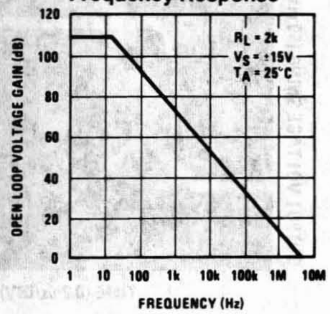
Distortion vs Frequency



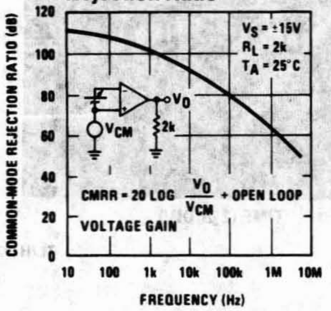
Undistorted Output Voltage Swing



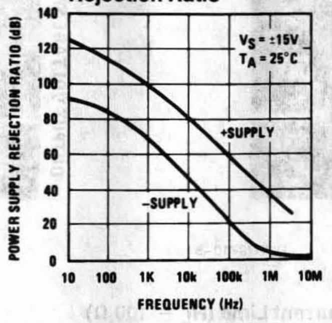
Open Loop Frequency Response



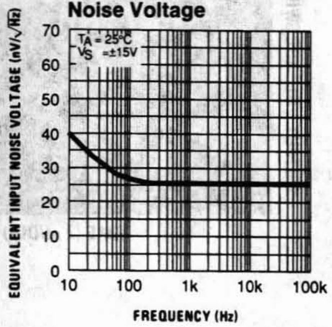
Common-Mode Rejection Ratio



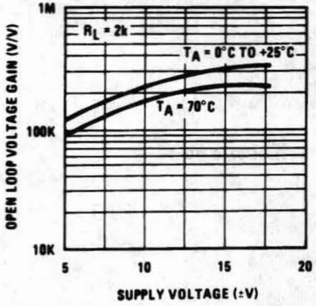
Power Supply Rejection Ratio



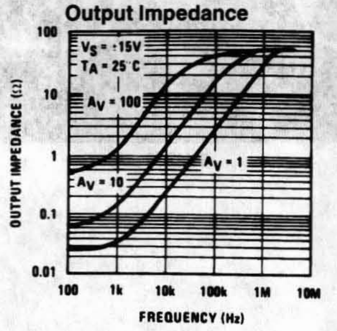
Equivalent Input Noise Voltage



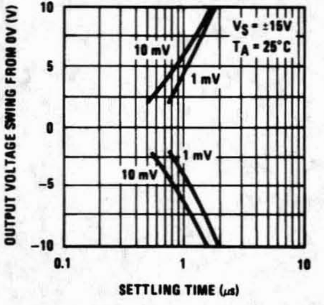
Open Loop Voltage Gain (V/V)



Output Impedance



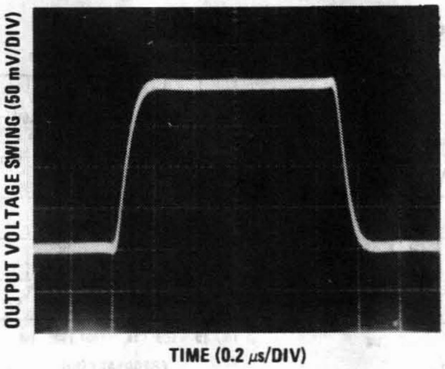
Inverter Settling Time



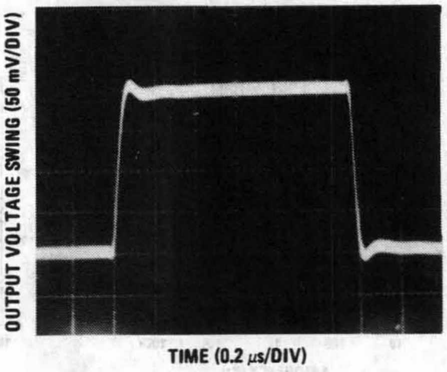
TL/H/9710–5

Pulse Response

Small Signal Inverting



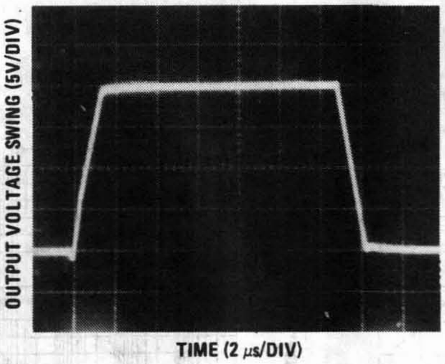
Small Signal Non-Inverting



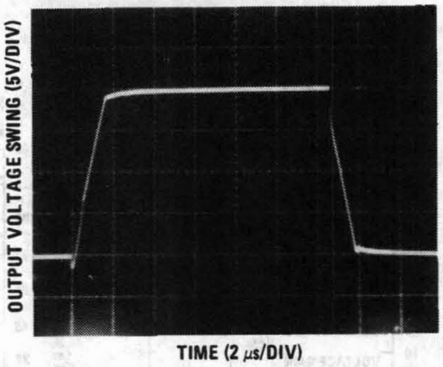
TL/H/9710-6

TL/H/9710-7

Large Signal Inverting



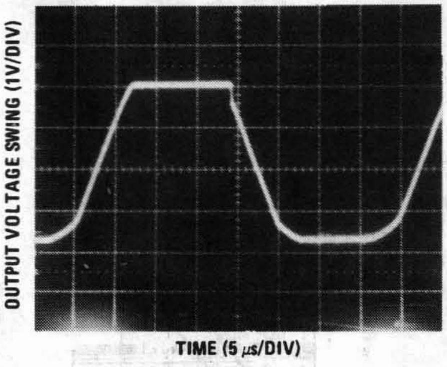
Large Signal Non-Inverting



TL/H/9710-8

TL/H/9710-9

Current Limit ($R_L = 100\ \Omega$)



TL/H/9710-10

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit with the non-inverting input, or with both inputs, will force the output to a high state, potentially causing a reversal of phase to the output. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

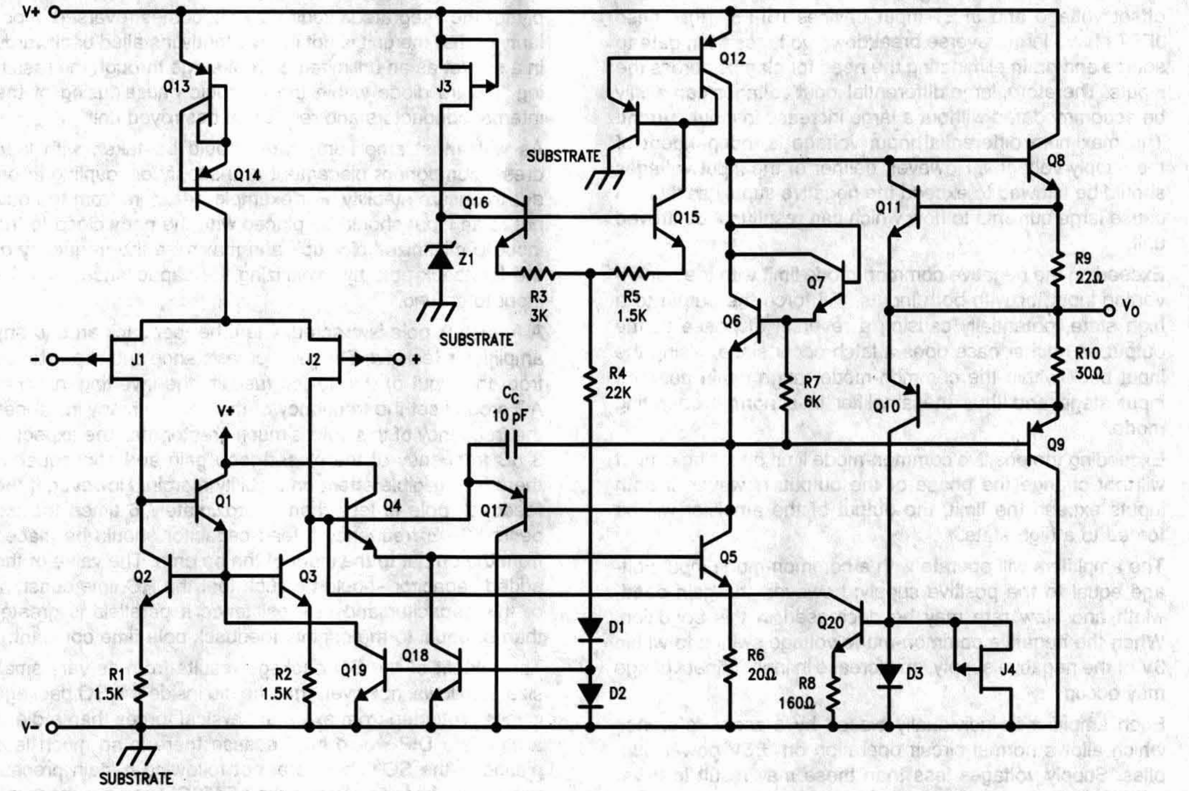
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive.The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

The benefit of the SO package results from its very small size. It follows, however, that the die inside the SO package is less protected from external physical forces than a die in a standard DIP would be, because there is so much less plastic in the SO. Therefore, not following certain precautions when board mounting the LF453CM can put mechanical stress on the die, lead frame, and/or bond wires. This can cause shifts in the LF453CM's parameters, even causing them to exceed limits specified in the Electrical Characteristics. For recommended practices in LF453CM surface mounting refer to Application Note AN450 "Surface Mounting Methods and Their Effect on Product Reliability" and to the section titled "Surface Mount" found in any Rev 1. Linear Databook volume.

Detailed Schematic


V+
Q13
J3
Q12
SUBSTRATE
Q8
Q14
Q16
Q15
Q11
Z1
R3
3K
R5
1.5K
R9
22Ω
Q7
V_O
SUBSTRATE
Q6
-
J1
J2
+
R10
30Ω
R4
22K
R7
6K
Q10
C_C
10 pF
V+
Q9
Q1
Q4
Q17
Q5
Q2
Q3
Q20
D1
R6
20Ω
D3
J4
Q19
Q18
R1
1.5K
R2
1.5K
D2
R8
160Ω
V-
SUBSTRATE

TL/H/9710-11

National Semiconductor

LH0003
Wide Bandwidth Operational Amplifier

General Description

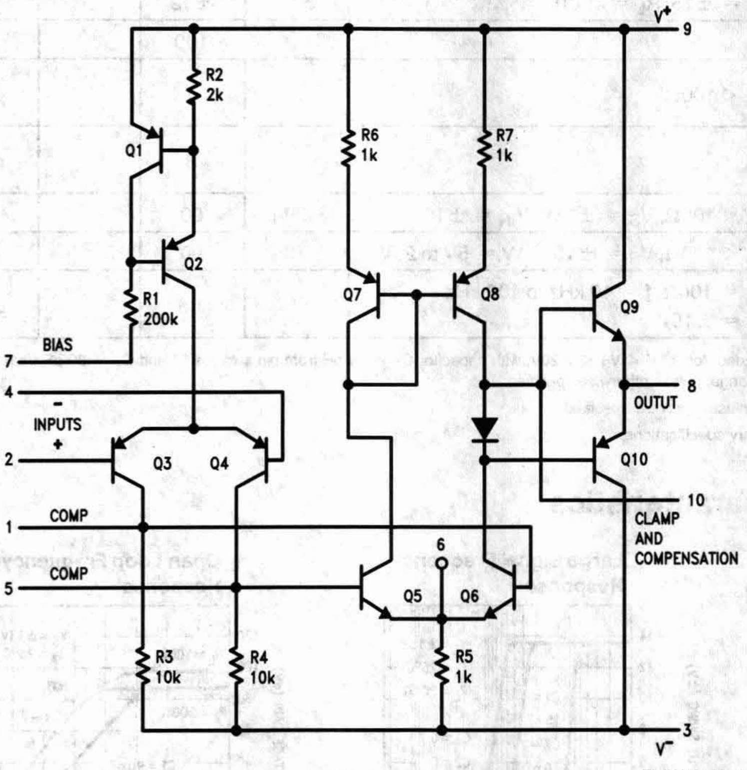
The LH0003/LH0003C is a general purpose operational amplifier which features: slewing rate up to 70 V/μs, a gain bandwidth of up to 30 MHz, and high output currents. Other features are:

Features

■ Very low offset voltage	Typically 0.4 mV
■ Large output swing	> ±10V into 100Ω load
■ High CMRR	Typically > 90 dB
■ Good large signal frequency response	50 kHz to 400 kHz depending on compensation

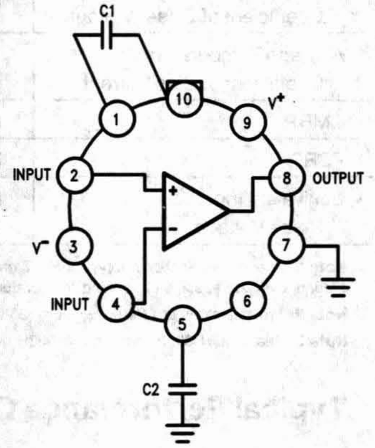
The LH0003 is specified for operation over the −55°C to +125°C military temperature range. The LH0003C is specified for operation over the 0°C to +85°C temperature range.

Schematic and Connection Diagrams



V+
9
R2
2k
Q1
R6
1k
R7
1k
Q2
R1
200k
Q7
Q8
Q9
BIAS
7
4
−
INPUTS
+
2
Q3
Q4
8
OUTUT
Q10
10
CLAMP
AND
COMPENSATION
1
COMP
5
COMP
6
Q5
Q6
R3
10k
R4
10k
R5
1k
3
V−

TL/K/10123-1



C1
10
1
9
V+
INPUT
2
8
OUTPUT
+
−
V−
3
7
INPUT
4
6
5
C2

TL/K/10123-2

Top View

Order Number LH0003H, LH0003H-MIL or LH0003CH
See NS Package Number H10G

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±20V
Power Dissipation	See curve
Differential Input Voltage	±7V
Input Voltage	Equal to supply
Load Current	120 mA
Operating Temperature Range LH0003	−55°C to +125°C
LH0003C	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (Notes 1 & 2)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S < 100\Omega$		0.4	3.0	mV
Input Offset Current			0.02	0.2	μA
Input Bias Current			0.4	2.0	μA
Supply Current	$V_S = \pm 20V$		1.2	3	mA
Voltage Gain	$R_L = 100k, V_S = \pm 15V, V_{OUT} = \pm 10V$	20	70		V/mV
Voltage Gain	$R_L = 2k, V_S = \pm 15V, V_{OUT} = \pm 10V$	15	40		V/mV
Output Voltage Swing	$V_S = \pm 15, R_L = 100\Omega$	±10	±12		V
Input Resistance			100		kΩ
Average Temperature Coefficient of Offset Voltage	$R_S < 100\Omega$		4		μV/°C
Average Temperature Coefficient of Bias Current			8		nA/°C
CMRR	$R_S < 100\Omega, V_S = \pm 15V, V_{IN} = \pm 10V$	70	90		dB
PSRR	$R_S < 100\Omega, V_S = \pm 15V, \Delta V = 5V$ to $20V$	70	90		dB
Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 10 kHz to 100 kHz $V_S = \pm 15V$		1.8		μVrms

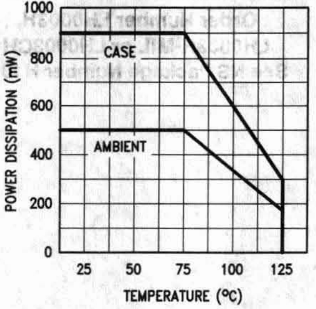
Note 1: These specifications apply for Pin 7 grounded, for $\pm 5V < V_S < \pm 20V$, with capacitor $C_1 = 90$ pF from pin 1 to pin 10 and $C_2 = 90$ pF from pin 5 to ground, over the specified operating temperature range, unless otherwise specified.

Note 2: Typical values are for $t_{AMBIENT} = 25°C$ unless otherwise specified.

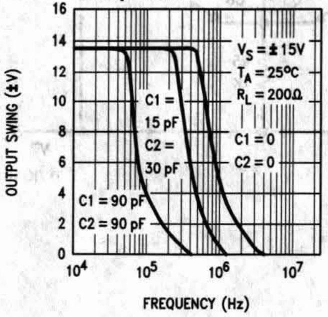
Note 3: See #RETS0003X for the LM0003H military specifications.

Typical Performance Characteristics

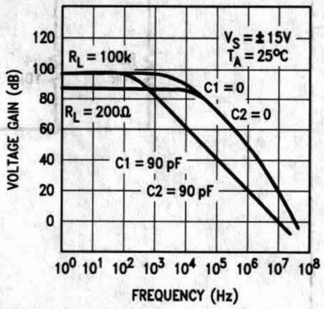
Maximum Power Dissipation



Large Signal Frequency Response



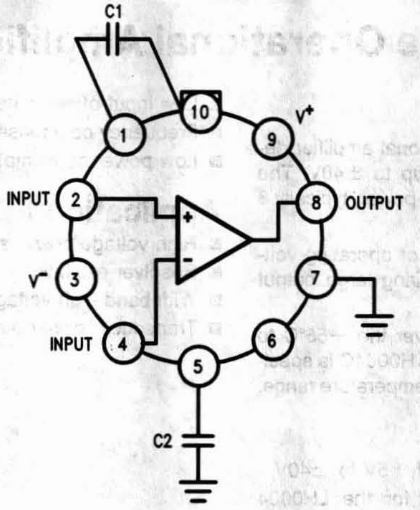
Open Loop Frequency Response



TL/K/10123-5

Typical Applications

High Slew Rate Unity Gain Inverting Amplifier


C1
10
1
9
V+
INPUT
2
8
OUTPUT
V−
3
7
INPUT
4
5
6
C2

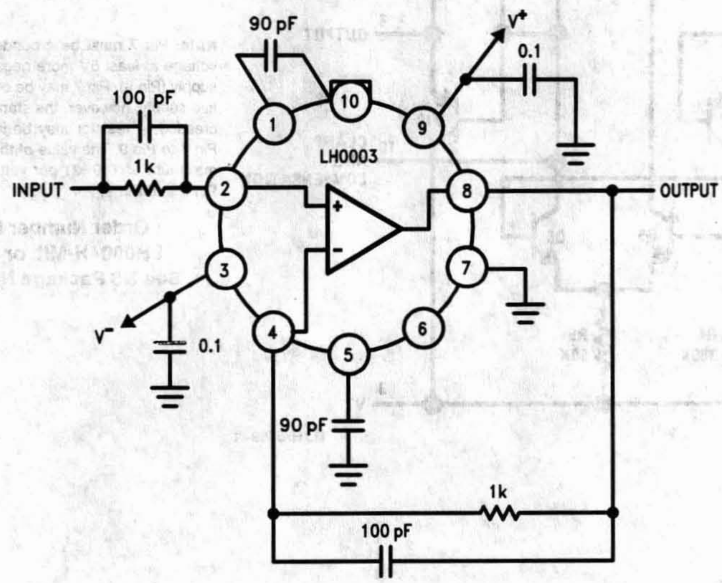
*Previously called NH0003/NH0003C

TL/K/10123-2

Typical Compensation

Circuit Gain	C_1 pF	C_2 pF	Slew Rate $R_L > 200\Omega$, V/µs	Full Output Frequency $R_L = 200\Omega$ $V_{OUT} = \pm 10V$
≥40	0	0	70	400 kHz
≥10	5	30	30	350 kHz
≥5	15	30	15	250 kHz
≥2	50	50	5	100 kHz
≥1	90	90	2	50 kHz

Unity Gain Follower


90 pF
V+
0.1
100 pF
1k
10
1
9
LH0003
INPUT
2
8
OUTPUT
3
7
V−
0.1
4
5
6
90 pF
1k
100 pF

TL/K/10123-4

National Semiconductor

LH0004 High Voltage Operational Amplifier

General Description

The LH0004 is a general purpose operational amplifier designed to operate from supply voltages up to ±40V. The device dissipates extremely low quiescent power, typically 8 mW at 25°C and $V_S = \pm 40V$.

The LH0004's high gain and wide range of operating voltages make it ideal for applications requiring large output swing and low power dissipation.

The LH0004 is specified for operation over the −55°C to +125°C military temperature range. The LH0004C is specified for operation over the 0°C to +85°C temperature range.

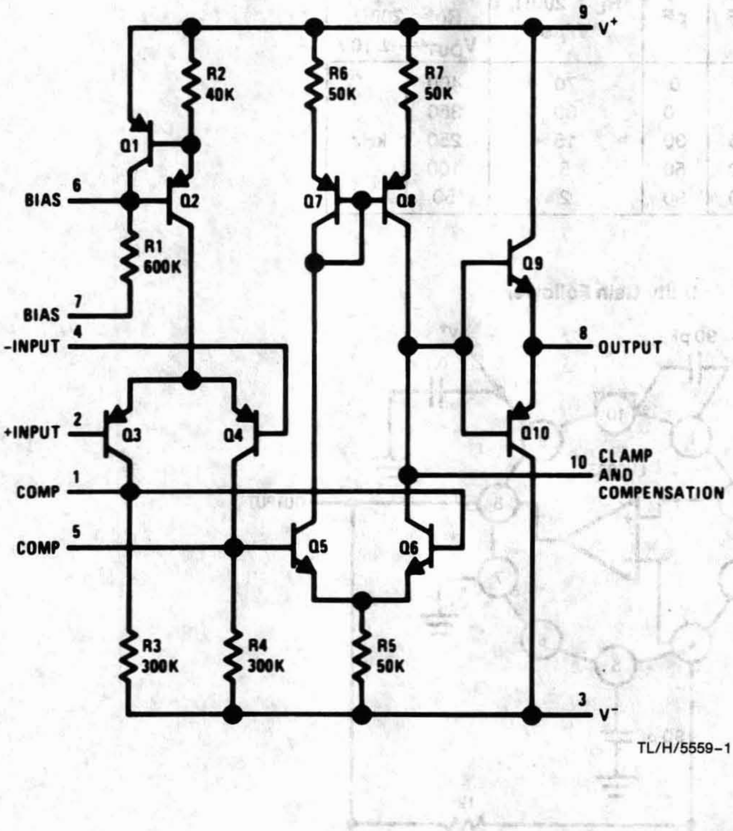
Features

- Capable of operation over the range of ±5V to ±40V
- Large output voltage typically ±35V for the LH0004 and ±33V for the LH0004C into a 2 kΩ load with ±40V supplies
- Low input offset voltage typically 0.3 mV
- Frequency compensation with 2 small capacitors
- Low power consumption 8 mW at ±40V

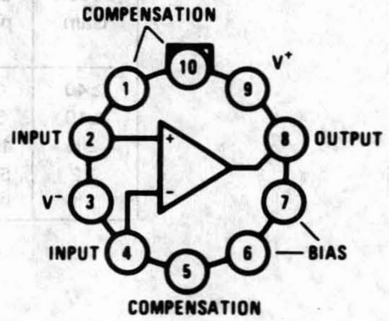
Applications

- High voltage power supply
- Resolver excitation
- Wideband high voltage amplifier
- Transducer power supply

Schematic and Connection Diagrams


9
V+
R2
40K
R6
50K
R7
50K
Q1
BIAS
6
Q2
Q7
Q8
R1
600K
Q9
BIAS
7
-INPUT
4
8
OUTPUT
+INPUT
2
Q3
Q4
Q10
10
CLAMP
AND
COMPENSATION
COMP
1
COMP
5
Q5
Q6
R3
300K
R4
300K
R5
50K
3
V-

TL/H/5559-1


COMPENSATION
10
V+
1
9
INPUT
2
8
OUTPUT
V-
3
7
INPUT
4
6
BIAS
5
COMPENSATION

TL/H/5559-2

Note: Pin 7 must be grounded or connected to a voltage at least 5V more negative than the positive supply (Pin 9). Pin 7 may be connected to the negative supply; however, the standby current will be increased. A resistor may be inserted in series with Pin 7 to Pin 9. The value of the resistor should be a maximum of 100 kΩ per volt of potential between Pin 3 and Pin 9.

Order Number LH0004H, LH0004H-MIL or LH0004CH
See NS Package Number H10G

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Supply Voltage	±45V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±7V
Input Voltage	Equal to Supply
Short Circuit Duration	3 sec
Operating Temperature Range	
LH0004	−55°C to +125°C
LH0004C	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

Electrical Characteristics (Note 1)

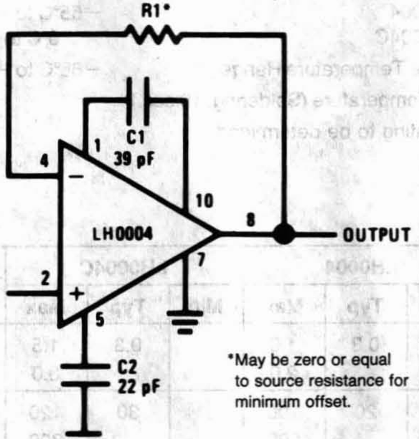
Parameter	Conditions	LH0004			LH0004C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$ $R_S \leq 100\Omega$		0.3	1.0 2.0		0.3	1.5 3.0	mV
Input Bias Current	$T_A = 25°C$		20	100 300		30	120 300	nA
Input Offset Current	$T_A = 25°C$		3	20 100		10	45 150	nA
Positive Supply Current	$V_S = \pm 40V$, $T_A = 25°C$ $V_S = \pm 40V$		110	150 175		110	150 175	μA
Negative Supply Current	$V_S = \pm 40V$, $T_A = 25°C$ $V_S = \pm 40V$		80	100 135		80	100 135	μA
Voltage Gain	$V_S = \pm 40V$, $R_L = 100k$, $T_A = 25°C$ $V_{OUT} = \pm 30V$	30	60		30	60		V/mV
	$V_S = \pm 40V$, $R_L = 100k$ $V_{OUT} = \pm 30V$	10			10			V/mV
Output Voltage	$V_S = \pm 40V$, $R_L = 10k$		±35	±30		±33	±30	V
CMRR	$V_S = \pm 40V$, $R_S \leq 5k$ $V_{IN} = \pm 33V$	70	90		70	90		dB
PSRR	$V_S = \pm 40V$, $R_S \leq 5k$ $\Delta V = 20V$ to $40V$	70	90		70	90		dB
Average Temperature Coefficient Offset Voltage	$R_S \leq 100\Omega$		4.0			4.0		μV/°C
Average Temperature Coefficient of Offset Current			0.4			0.4		nA/°C
Equivalent Input Noise Voltage	$R_S = 100\Omega$, $V_S = \pm 40V$ f = 500 Hz to 5 kHz, $T_A = 25°C$		3.0			3.0		μVrms

Note 1: These specifications apply for $\pm 5V \leq V_S \leq \pm 40V$, Pin 7 grounded, with capacitors C1 = 39 pF between Pin 1 and Pin 10, C2 = 22 pF between Pin 5 and ground, −55°C to +125°C for the LH0004, and 0°C to +85°C for the LH0004C unless otherwise specified.

Note 2: Refer to RETS0004X for LH0004H military specifications.

Typical Applications

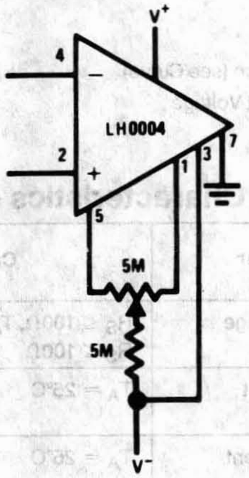
Voltage Follower


R1*
C1
39 pF
1
4
10
8
OUTPUT
LH0004
2
7
5
C2
22 pF

*May be zero or equal to source resistance for minimum offset.

TL/H/5559-3

Input Offset Voltage Adjust


V+
4
2
LH0004
7
1
3
5
5M
5M
V-

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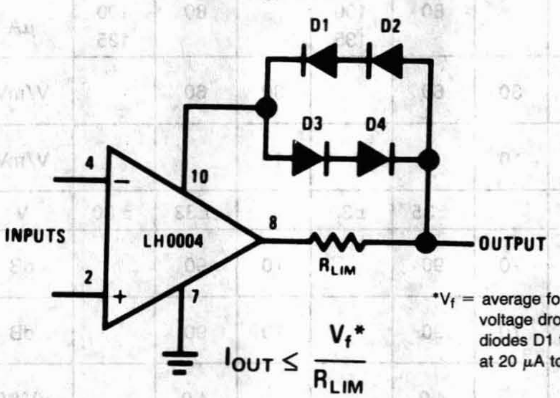
External Current Limiting Method


D1
D2
D3
D4
4
10
INPUTS
LH0004
8
2
7
RLIM
OUTPUT

$$I_{OUT} \leq \frac{V_f^*}{R_{LIM}}$$

*V_f = average forward voltage drop of diodes D1 to D4 at 20 μA to 50 μA.

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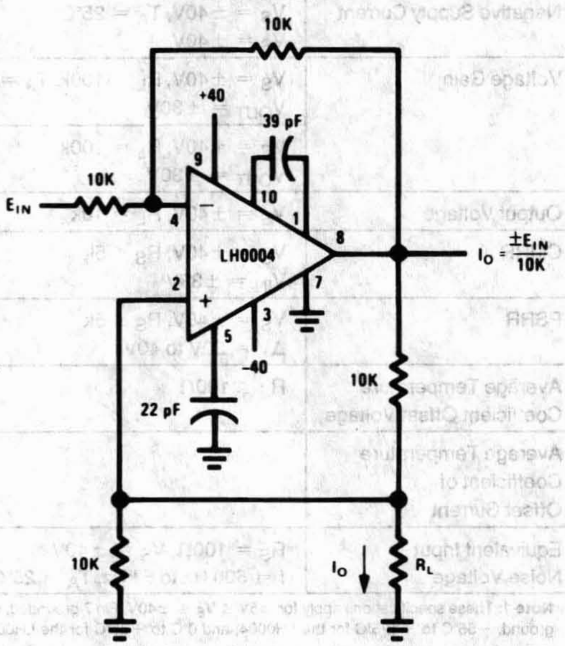
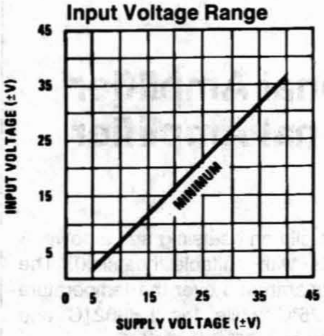
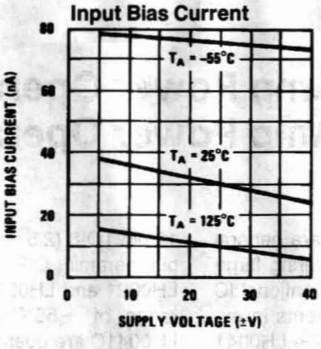
High Compliance Current Source

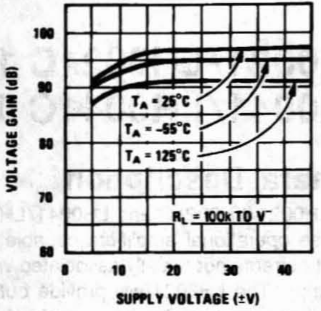

10K
+40
39 pF
9
10K
EIN
10
4
1
8
LH0004
$I_O = \frac{\pm E_{IN}}{10K}$
2
7
3
5
-40
10K
22 pF
10K
IO
RL

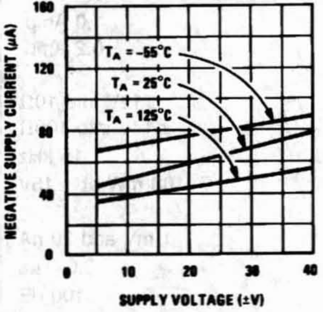
TL/H/5559-6

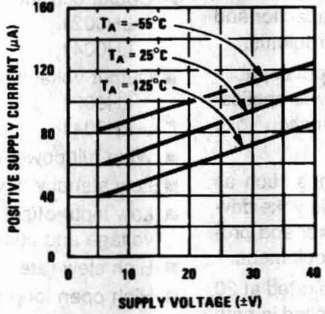
Typical Performance Characteristics

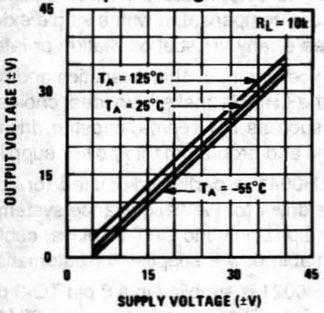

Input Voltage Range

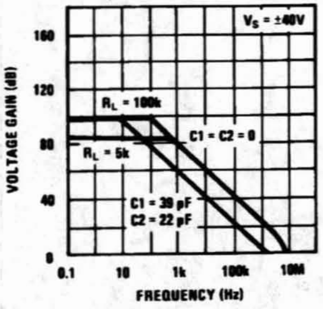

Input Bias Current

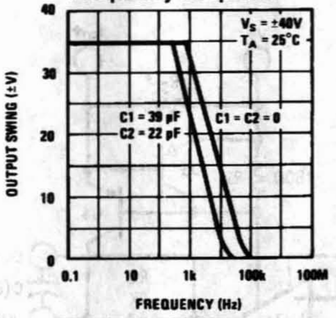

Voltage Gain

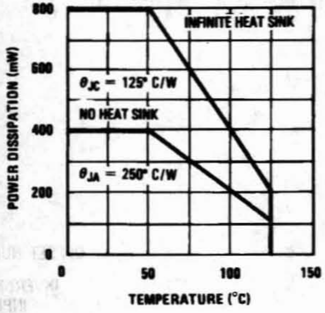

Negative Supply Current


Positive Supply Current


Output Voltage


Open Loop Frequency Response


Large Signal Frequency Response


Package Power Dissipation

TL/H/5559-7

National Semiconductor

LH0021/LH0021C 1.0 Amp Power Operational Amplifier
LH0041/LH0041C 0.2 Amp Power Operational Amplifier

General Description

The LH0021/LH0021C and LH0041/LH0041C are general purpose operational amplifiers capable of delivering large output currents not usually associated with conventional IC Op Amps. The LH0021 will provide output currents in excess of one ampere at voltage levels of ±12V; the LH0041 delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload. the devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

The excellent input characteristics and high output capability of the LH0021 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

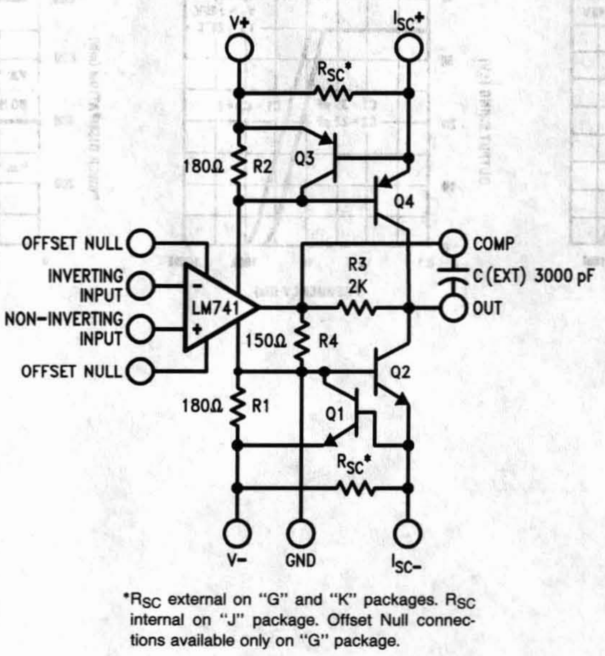
The LH0041 is particularly suited for applications such as torque driver for inertial guidance systems, diddle yoke driver for alpha-numeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

The LH0021 is supplied in a 8 pin TO-3 package rated at 20 watts with suitable heatsink. The LH0041 is supplied in both 12 pin TO-8 (2.5 watts with clip on heatsink) and a power 8 pin ceramic DIP (2 watts with suitable heatsink). The LH0021 and LH0041 are guaranteed over the temperature range of −55°C to +125°C while the LH0021C and LH0041C are guaranteed from −25°C to +85°C.

Features

■ Output current	
LH0021	1.0 Amp
LH0041	0.2 Amp
■ Output voltage swing	
LH0021	±12V into 10Ω
LH0041	±14V into 100Ω
■ Wide full power bandwidth	15 kHz
■ Low standby power	100 mW at ±15V
■ Low input offset voltage and current	1 mV and 20 nA
■ High slew rate	3.0V/μs
■ High open loop gain	100 dB

Schematic Diagram



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*R_{SC} external on "G" and "K" packages. R_{SC} internal on "J" package. Offset Null connections available only on "G" package.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	See Curves
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Peak Output Current (Note 2)	
LH0021/LH0021C	2.0 Amps
LH0041/LH0041C	0.5 Amps
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range	
LH0021/LH0041	−55°C to +125°C
LH0021C/LH0041C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

DC Electrical Characteristics for LH0021/LH0021C (Note 4)

Parameter	Conditions	Limits						Units
		LH0021			LH0021C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S < 100\Omega$, $T_C = 25°C$ $R_S < 100\Omega$		1.0	3.0 5.0		3.0	6.0 7.5	mV mV
Voltage Drift with Temperature	$R_S < 100\Omega$		3	25		5	30	μV/°C
Offset Voltage Drift with Time			5			5		μV/week
Offset Voltage Change with Output Power			5	15		5	20	μV/W
Input Offset Current	$T_C = 25°C$		30	100 300		50	200 500	nA nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_C = 25°C$		100	300 1.0		200	500 1.0	nA μA
Input Resistance	$T_C = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	R_S 100Ω, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S \le 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 1\ k\Omega$, $T_C = 25°C$	100	200		100	200		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$ $V_S = \pm 15V$, $R_L = 10\Omega$, $T_C = 25°C$	±13.5 ±11.0	14 ±12		±13 ±10	±14 ±12		V V
Output Short Circuit Current	$V_S = \pm 15V$, $T_C = 25°C$, $R_{SC} = 0.5\Omega$	0.8	1.2	1.6	0.8	1.2	1.6	Amps
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

AC Electrical Characteristics for LH0021/LH0021C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000\ pF$)

Parameter	Conditions	Limits						Units
		LH0021			LH0021C			
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	$A_V = +1$, $R_L = 100\Omega$	0.8	3.0		1.0	3.0		V/μs
Power Bandwidth	$R_L = 100\Omega$		20			20		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	μs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		μs
Overload Recovery Time			3			3		μs
Harmonic Distortion	f = 1 kHz, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_s = 50\Omega$, B.W. = 10 Hz to 10 kHz		5			5		μV/rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA/rms

DC Electrical Characteristics for LH0041/LH0041C (Note 4)

Parameter	Conditions	Limits						Units
		LH0041			LH0041C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S < 100\Omega$, $T_A = 25°C$ $R_S < 100\Omega$		1.0	3.0 5.0		3.0	6.0 7.5	mV mV
Voltage Drift with Temperature	$R_S < 100\Omega$		3			5		μV/°C
Offset Voltage Drift with Time			5			5		μV/week
Offset Voltage Change with Output Power			15			15		μV/W
Offset Voltage Adjustment Range	(Note 5)		20			20		mV
Input Offset Current	$T_A = 25°C$		30	100 300		50	200 500	nA nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_A = 25°C$		100	300 1.0		200	500 1.0	nA μA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	R_S 100Ω, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	+12			+12			V
Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 1\ k\Omega$, $T_A = 25°C$	100	200		100	200		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$	±13	14		±13	±14		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_A = 25°C$ (Note 6)		200	300		200	300	mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

AC Electrical Characteristics for LH0041/LH0041C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000\ pF$)

Parameter	Conditions	Limits						Units
		LH0041			LH0041C			
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	$A_V = +1$, $R_L = 100\Omega$	1.5	3.0		1.0	3.0		V/μs
Power Bandwidth	$R_L = 100\Omega$		20			20		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	μs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		μs
Overload Recovery Time			3			3		μs
Harmonic Distortion	$f = 1\ kHz$, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_s = 50\Omega$, B.W. = 10 Hz to 10 kHz		5			5		μV/rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA/rms

Note 1: Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.

Note 2: Rating applies for LH0041G and LH0021K with $R_{SC} = 0\Omega$.

Note 3: Rating applies as long as package power rating is not exceeded.

Note 4: Specifications apply for $\pm 5V \leq V_S \pm 18V$, and $-55°C \leq T_C = \leq 125°C$ for LH0021K and LH0041G, and $-25°C \leq T_C \leq +85°C$ for LH0021CK, LH0041CG and LH0041CJ unless otherwise specified. Typical values are for 25°C only.

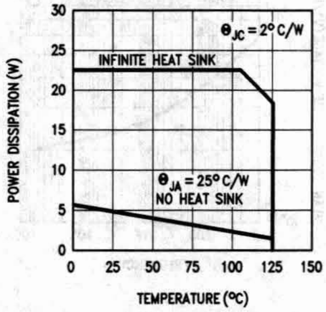
Note 5: TO-8 "G" packages only.

Note 6: Rating applies for "J" DIP package and for TO-8 "G" package with $R_{SC} = 3.3$ ohms.

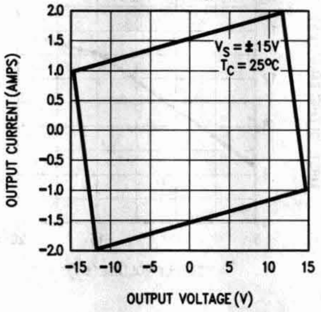
Note 7: See Typical Performance Characteristics.

Typical Performance Characteristics

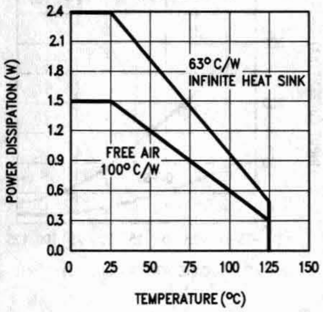
Power Derating-LH0021



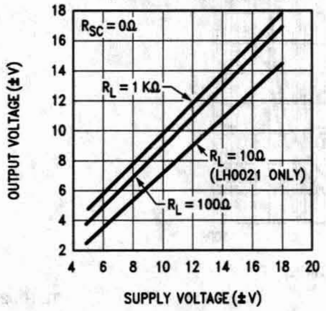
Safe Operating Area—LH0021



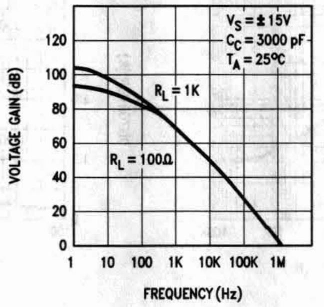
Package Power Dissipation LH0041/LH0041C



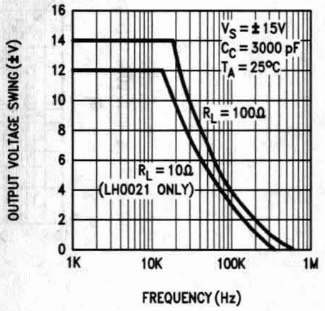
Output Voltage Swing



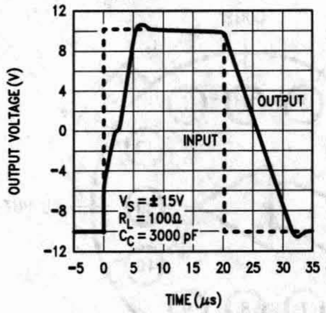
Open Loop Frequency Response



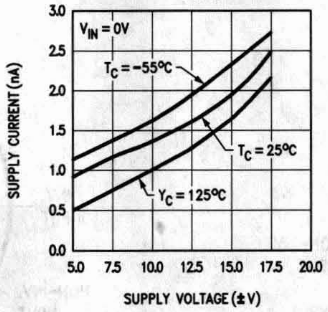
Large Signal Frequency Response



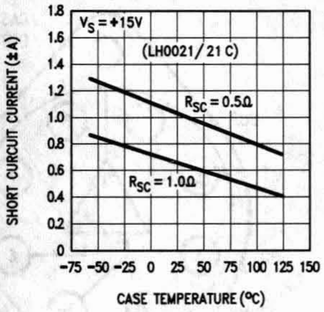
Voltage Follower Pulse Response



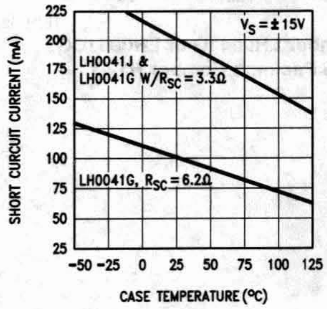
No Load Supply Current



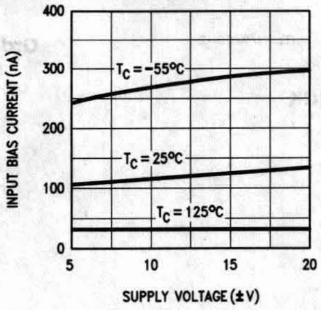
Short Circuit Current vs Temperature LH0021/LH0021C



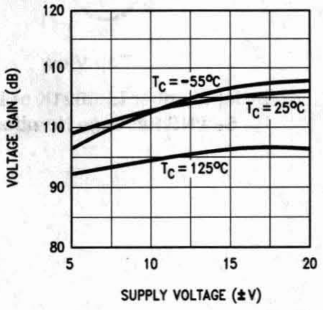
Short Circuit Current vs Temperature LH0041/LH0041C



Input Bias Current

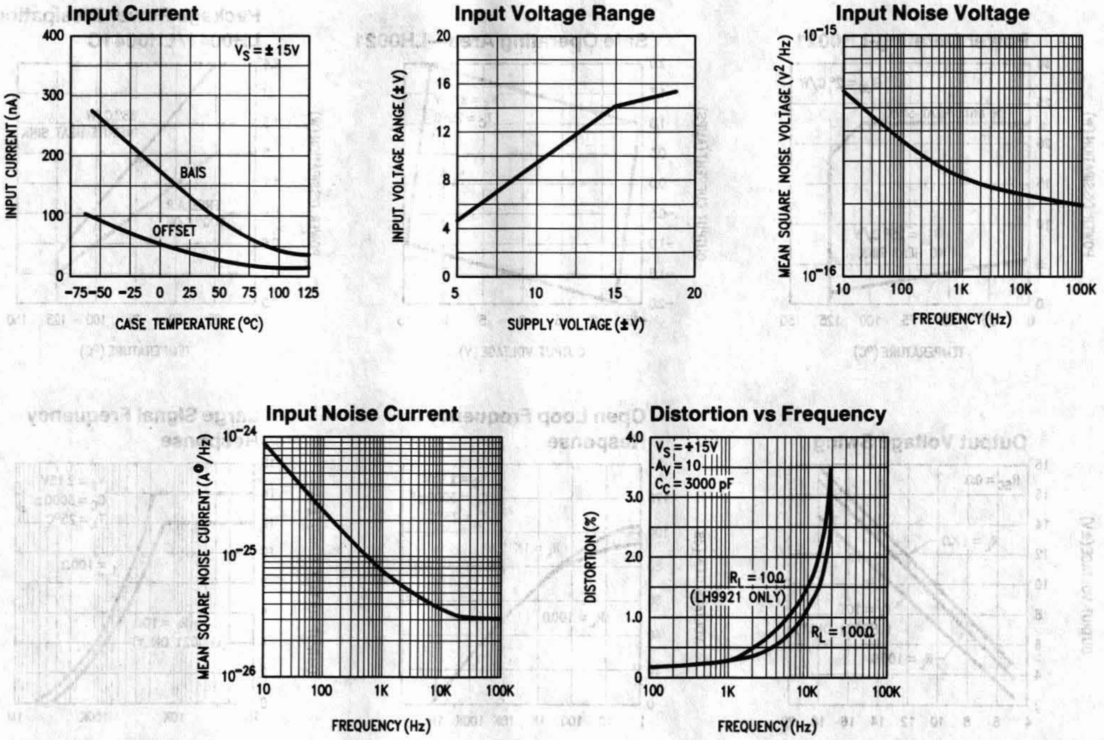


Voltage Gain



TL/H/9298–6

Typical Performance Characteristics (Continued)



Input Current

Input Voltage Range

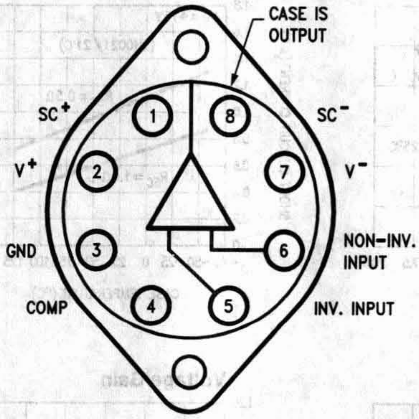
Input Noise Voltage

Input Noise Current

Distortion vs Frequency

TL/H/9298-7

Connections Diagrams

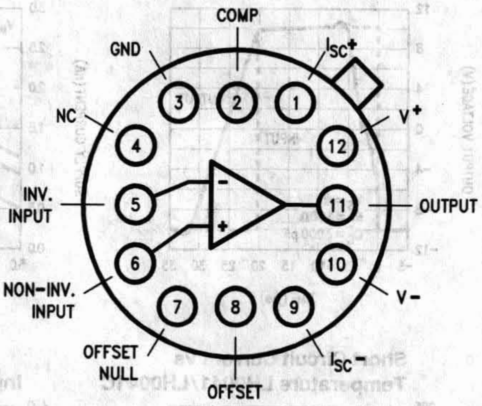


CASE IS OUTPUT
1
2
3
4
5
6
7
8
SC^+
V^+
GND
COMP
SC^-
V^-
NON-INV. INPUT
INV. INPUT

TL/H/9298-2

Top View

Order Number LH0021K or LH0021CK
See NS Package Number K08A

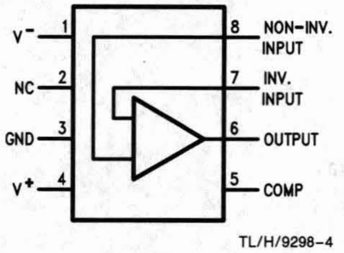


COMP
GND
I_{SC}^+
NC
V^+
INV. INPUT
OUTPUT
NON-INV. INPUT
V−
OFFSET NULL
I_{SC}^-
OFFSET
1
2
3
4
5
6
7
8
9
10
11
12
−
+

TL/H/9298-3

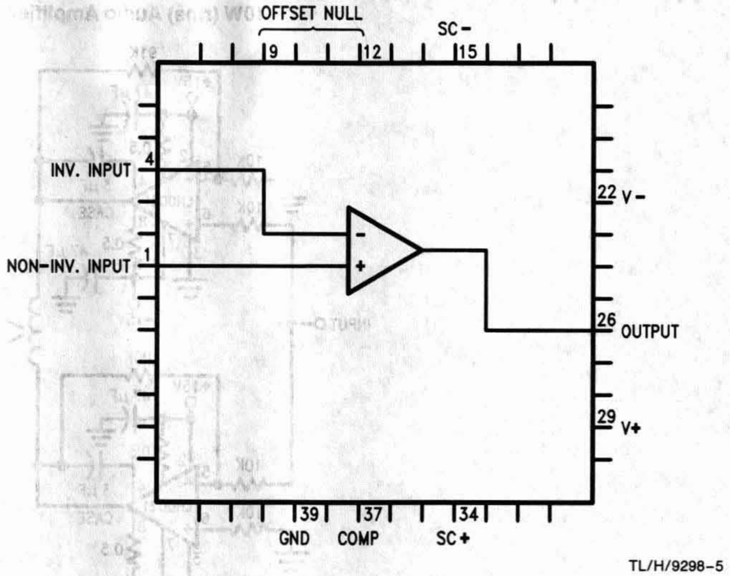
Order Number LH0041G or LH0041CG
See NS Package Number H12B

Connection Diagrams (Continued)


V⁻
1
NC
2
GND
3
V⁺
4
8
NON-INV. INPUT
7
INV. INPUT
6
OUTPUT
5
COMP
TL/H/9298-4

Top View

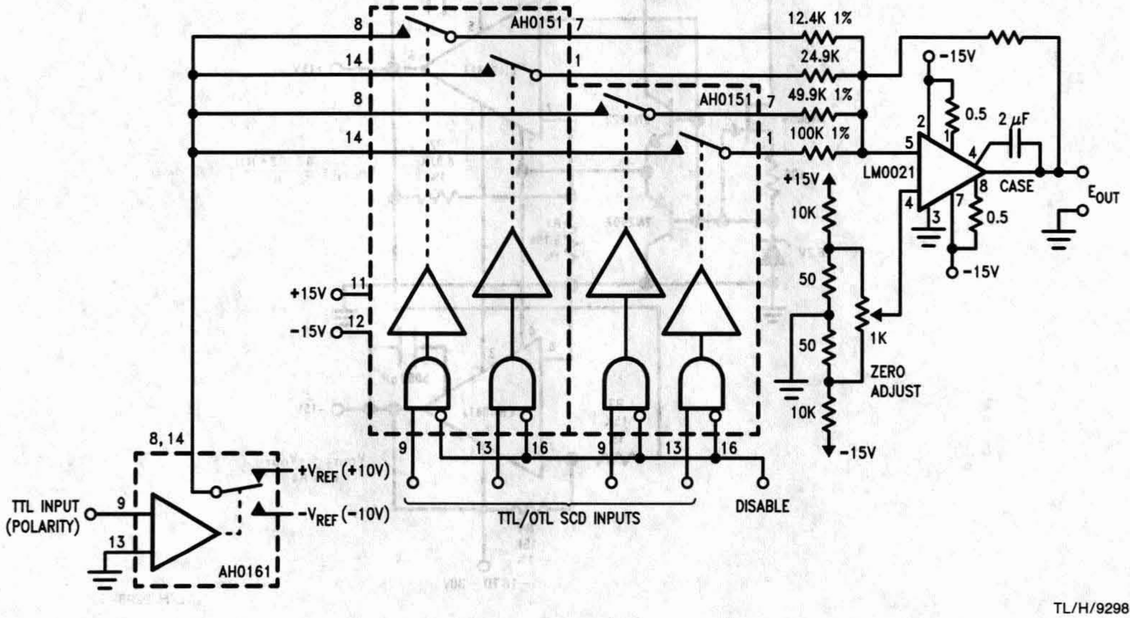
Order Number LH0041CJ
See NS Package Number HY08A


OFFSET NULL
9
12
SC−
15
4
INV. INPUT
1
NON-INV. INPUT
22
V−
26
OUTPUT
29
V+
39
GND
37
COMP
34
SC+
TL/H/9298-5

Order Number LH0041E
See NS Package Number E48A

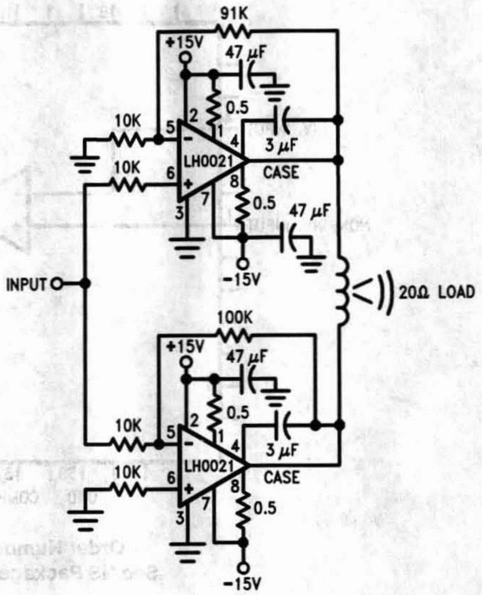
Typical Applications

Programmable One Amp Power Supply


8
14
8
14
AH0151
7
1
AH0151
7
1
12.4K 1%
24.9K
49.9K 1%
100K 1%
−15V
2
1
0.5
2 μF
5
4
LM0021
7
8
CASE
0.5
3
E_OUT
−15V
+15V
10K
50
50
1K
ZERO ADJUST
10K
−15V
+15V
11
−15V
12
9
13
16
9
13
16
DISABLE
TTL/DTL SCD INPUTS
8, 14
+V_REF (+10V)
−V_REF (−10V)
TTL INPUT (POLARITY)
9
13
AH0161
TL/H/9298-8

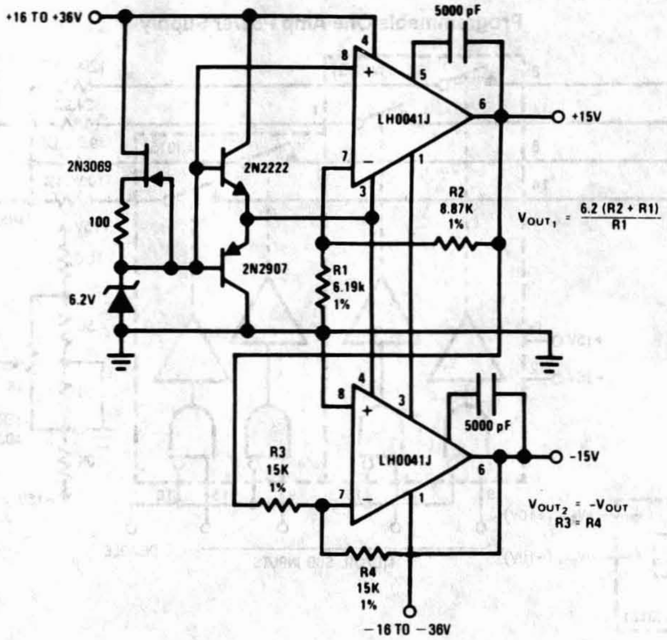
Typical Applications (Continued)

10W (rms) Audio Amplifier


91K
+15V
47 μF
0.5
3 μF
10K
10K
5
6
2
1
4
3
7
8
LH0021
CASE
0.5
47 μF
−15V
INPUT
20Ω LOAD
100K
+15V
47 μF
0.5
10K
10K
LH0021
3 μF
CASE
0.5
−15V

TL/H/9298-9

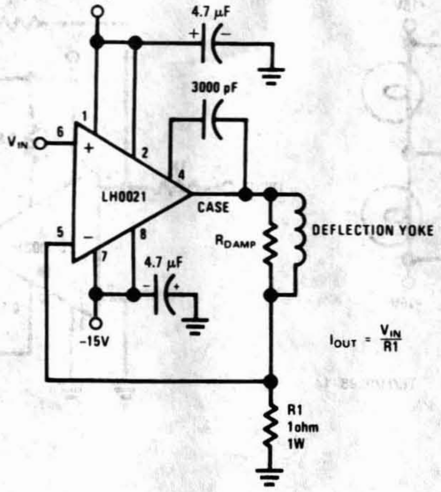
Dual Tracking One Amp Power Supply


+16 TO +36V
5000 pF
LH0041J
+15V
2N3069
2N2222
100
2N2907
6.2V
R2
8.87K
1%
R1
6.19k
1%
$V_{OUT_1} = \frac{6.2\,(R2 + R1)}{R1}$
LH0041J
5000 pF
−15V
R3
15K
1%
R4
15K
1%
$V_{OUT_2} = -V_{OUT}$
R3 = R4
−16 TO −36V

TL/H/9298-10

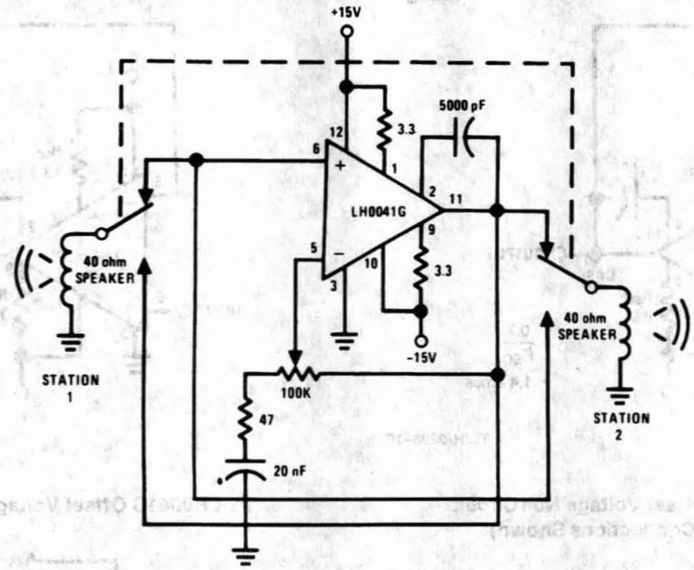
Typical Applications (Continued)

CRT Deflection Yoke Driver


+15V
4.7 μF
3000 pF
V_{IN}
6
1
2
4
LH0021
CASE
5
8
7
4.7 μF
−15V
DEFLECTION YOKE
R_{DAMP}
$I_{OUT} = \frac{V_{IN}}{R1}$
R1
1ohm
1W

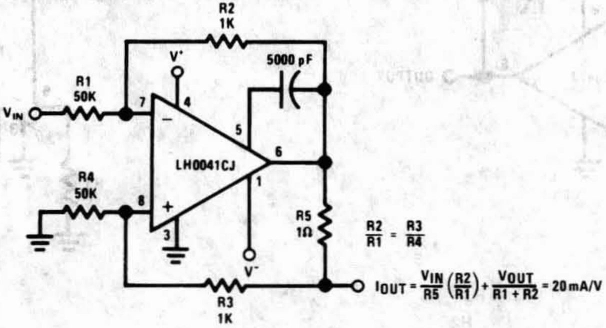
TL/H/9298–11

Two Way Intercom


+15V
3.3
5000 pF
12
6
1
LH0041G
2
11
9
5
10
3
3.3
−15V
40 ohm
SPEAKER
STATION
1
100K
47
20 nF
40 ohm
SPEAKER
STATION
2

TL/H/9298–12

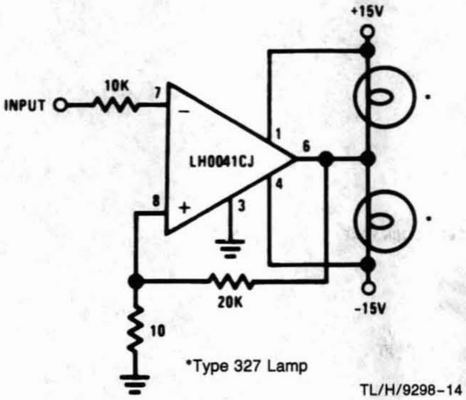
Programmable High Current Source/Sink


R2
1K
V+
5000 pF
R1
50K
V_{IN}
7
4
5
LH0041CJ
6
1
R4
50K
8
3
V−
R5
1Ω
$\frac{R2}{R1} = \frac{R3}{R4}$
R3
1K
$I_{OUT} = \frac{V_{IN}}{R5}\left(\frac{R2}{R1}\right) + \frac{V_{OUT}}{R1 + R2} = 20\,mA/V$

TL/H/9298–13

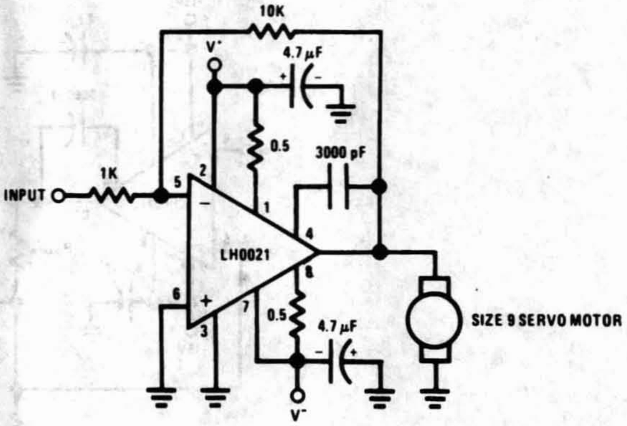
Typical Applications (Continued)

Power Comparator


+15V
INPUT
10K
7
LH0041CJ
1
6
4
8
3
20K
10
-15V
*Type 327 Lamp

TL/H/9298-14

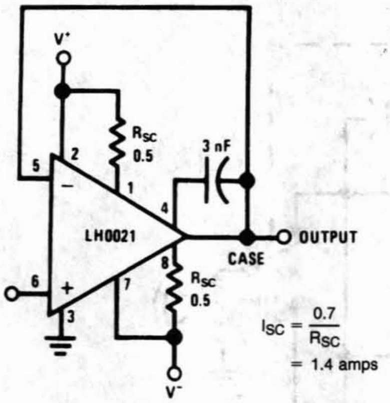
DC Servo Amplifier


10K
V+
4.7 μF
0.5
3000 pF
INPUT
1K
5
2
1
4
LH0021
8
6
7
3
0.5
4.7 μF
V-
SIZE 9 SERVO MOTOR

TL/H/9298-15

Auxiliary Circuits

LH0021 Unity Gain Circuit with Short Circuit Limiting

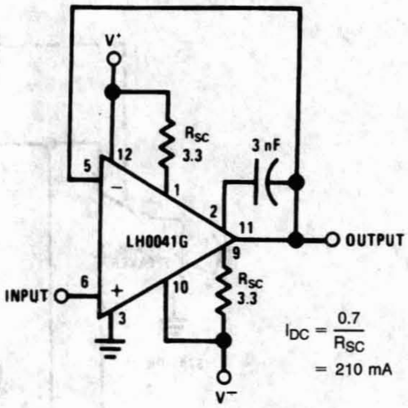

V+
R_SC
0.5
3 nF
5
2
1
4
LH0021
OUTPUT
CASE
6
8
7
3
R_SC
0.5
V-

$$I_{SC} = \frac{0.7}{R_{SC}}$$

$= 1.4$ amps

TL/H/9298-16

LH0041G Unity Gain with Short Circuit Limiting

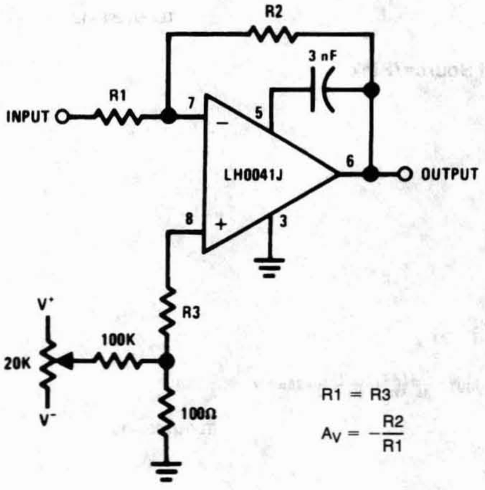

V+
R_SC
3.3
3 nF
5
12
1
2
11
LH0041G
OUTPUT
INPUT
6
9
10
3
R_SC
3.3
V-

$$I_{DC} = \frac{0.7}{R_{SC}}$$

$= 210$ mA

TL/H/9298-17

LH0041/LH0021 Offset Voltage Null Circuit (LH0041CJ Pin Connections Shown)*

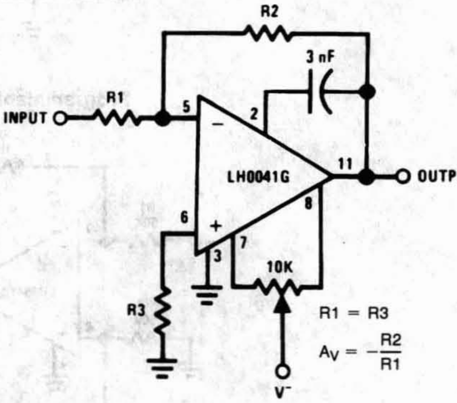

R2
3 nF
INPUT
R1
7
5
LH0041J
6
OUTPUT
8
3
V+
R3
20K
100K
V-
100Ω

R1 = R3

$$A_V = -\frac{R2}{R1}$$

TL/H/9298-18

LH0041G Offset Voltage Null Circuit*


R2
3 nF
R1
INPUT
5
2
LH0041G
11
OUTPUT
6
8
7
3
10K
R3
V-

R1 = R3

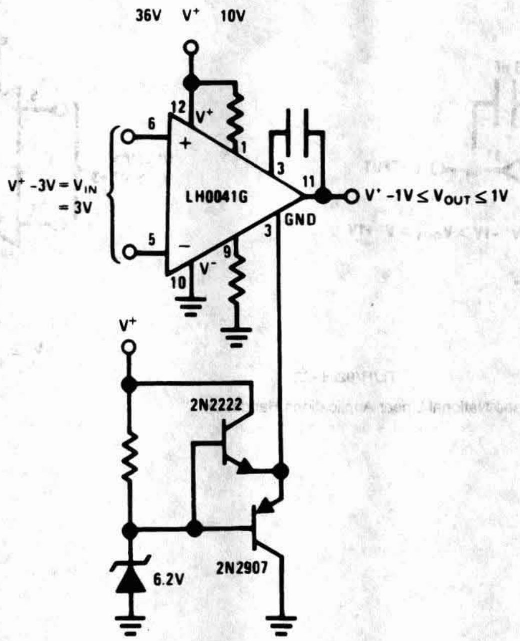
$$A_V = -\frac{R2}{R1}$$

TL/H/9298-19

Auxiliary Circuits (Continued)

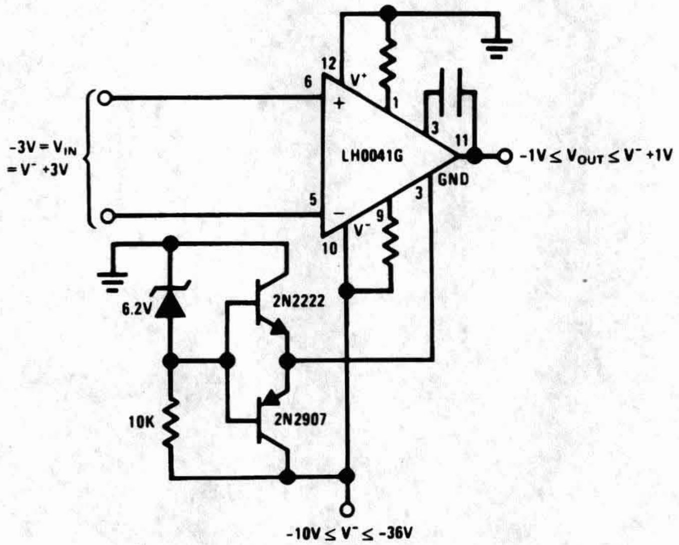
Operation from Single Supplies

POSITIVE


36V V+ 10V
12
V+
6
+
1
3
11
V+ -3V = VIN = 3V
LH0041G
V+ -1V ≤ VOUT ≤ 1V
GND
3
5
−
9
V-
10
V+
2N2222
6.2V
2N2907

TL/H/9298-20

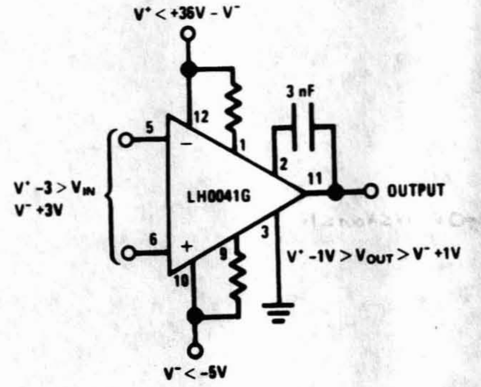
NEGATIVE


12
V+
6
+
1
3
11
-3V = VIN = V- +3V
LH0041G
-1V ≤ VOUT ≤ V- +1V
GND
3
5
−
9
V-
10
6.2V
2N2222
10K
2N2907
-10V ≤ V- ≤ -36V

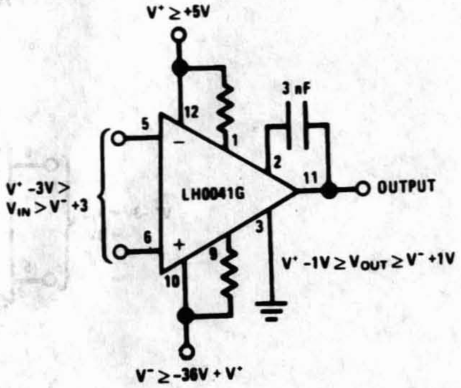
TL/H/9298-21

Auxiliary Circuits (Continued)

Operation from Non-Symmetrical Supplies


$V^+ < +36V - V^-$
12
5
1
3 nF
2
11
OUTPUT
$V^+ -3 > V_{IN}$
$V^- +3V$
LH0041G
−
+
6
3
9
10
$V^+ -1V > V_{OUT} > V^- +1V$
$V^- < -5V$

TL/H/9298–22


$V^+ \geq +5V$
12
5
1
3 nF
2
11
OUTPUT
$V^+ -3V >$
$V_{IN} > V^- +3$
LH0041G
−
+
6
3
9
10
$V^+ -1V \geq V_{OUT} \geq V^- +1V$
$V^- \geq -36V + V^+$

TL/H/9298–23

*For additional offset null circuit techniques see National Linear Applications Handbook.

National Semiconductor

LH0024 High Slew Rate Operational Amplifier

General Description

The LH0024/LH0024C is a very wide bandwidth, high slew rate operational amplifier intended to fulfill a wide variety of high speed applications such as buffers to A to D and D to A converters and high speed comparators. The device exhibits useful gain in excess of 50 MHz making it possible to use in video applications requiring higher gain accuracy than is usually associated with such amplifiers.

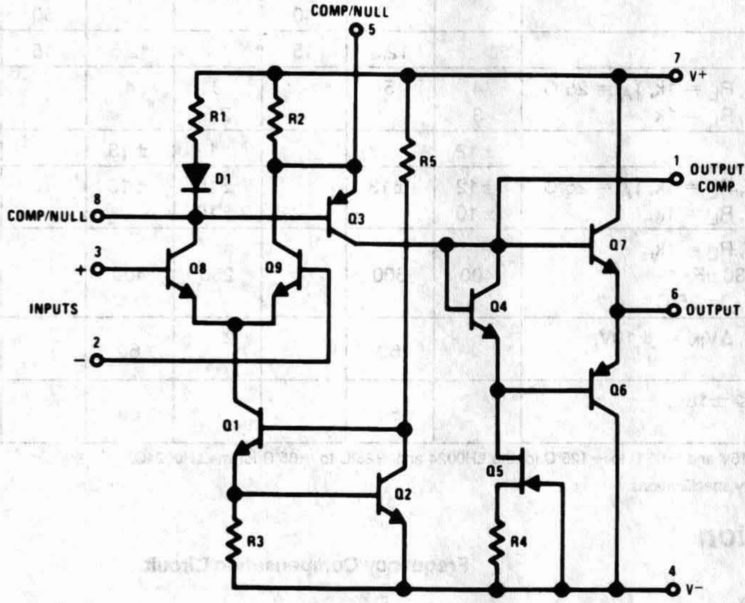
The LH0024/LH0024C's combination of wide bandwidth and high slew rate make it an ideal choice for a variety of high speed applications including active filters, oscillators, and comparators as well as many high speed general purpose applications.

The LH0024 is guaranteed over the temperature range −55°C to +125°C, whereas the LH0024C is guaranteed −25°C to +85°C.

Features

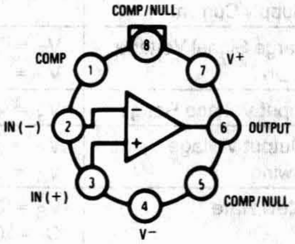
- Very high slew rate—500 V/µs at $A_V = +1$
- Wide small signal bandwidth—70 MHz
- Wide large signal bandwidth—15 MHz
- High output swing—±12V into 1k
- Low input offset—2 mV
- Pin compatible with standard IC op amps

Schematic and Connection Diagrams


COMP/NULL
5
7
V+
R1
R2
R5
D1
1
OUTPUT COMP
8
COMP/NULL
Q3
3
+
Q8
Q9
Q7
INPUTS
Q4
6
OUTPUT
2
−
Q6
Q1
Q5
Q2
R3
R4
4
V−

TL/K/5552-1

Metal Can Package


COMP/NULL
8
COMP
1
V+
7
IN (−)
2
−
+
6
OUTPUT
IN (+)
3
5
COMP/NULL
4
V−

TL/K/5552-2

Top View

Note: For heat sink use Thermalloy 2230-5 series.

Order Number LH0024H, LH0024H-MIL or LH0024CH
See NS Package Number H08B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Supply Voltage	±18V
Input Voltage	Equal to Supply
Differential Input Voltage	±5V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

Operating Temperature Range

LH0024	−55°C to +125°C
LH0024C	−25°C to +85°C

DC Electrical Characteristics (Note 1)

Parameter	Conditions	LH0024			LH0024C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		2.0	4.0		5.0	8.0	mV
	$R_S = 50\Omega$			6.0			10.0	mV
Average Temperature Coefficient of Input Offset Voltage	$V_S = \pm 15V$, $R_S = 50\Omega$ −55°C to 125°C		−20			−25		μV/°C
Input Offset Current	$T_A = 25°C$		2.0	5.0		4.0	15.0	μA
				10.0			20.0	μA
Input Bias Current	$T_A = 25°C$		15	30		18	40	μA
				40			50	μA
Supply Current			12.5	15		12.5	15	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $R_L = 1k$, $T_A = 25°C$	4	5		3	4		V/mV
	$V_S = \pm 15V$, $R_L = 1k$	3			2.5			V/mV
Input Voltage Range	$V_S = \pm 15V$	±12	±13		±12	±13		V
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 1k$, $T_A = 25°C$	±12	±13		±10	±13		V
	$V_S = \pm 15V$, $R_L = 1k$	±10			±10			V
Slew Rate	$V_S = \pm 15V$, $R_L = 1k$, $C_1 = C_2 = 30$ pF, $A_V = +1$, $T_A = 25°C$	400	500		250	400		V/μs
Common-Mode Rejection Ratio	$V_S = \pm 15V$, $\Delta V_{IN} = \pm 10V$, $R_S = 50\Omega$		60			60		dB
Power Supply Rejection Ratio	$\pm 5V \leq V_S \leq \pm 18V$, $R_S = 50\Omega$		60			60		dB

Note 1: These specifications apply for $V_S = \pm 15V$ and −55°C to +125°C for the LH0024 and −25°C to +85°C for the LH0024C.

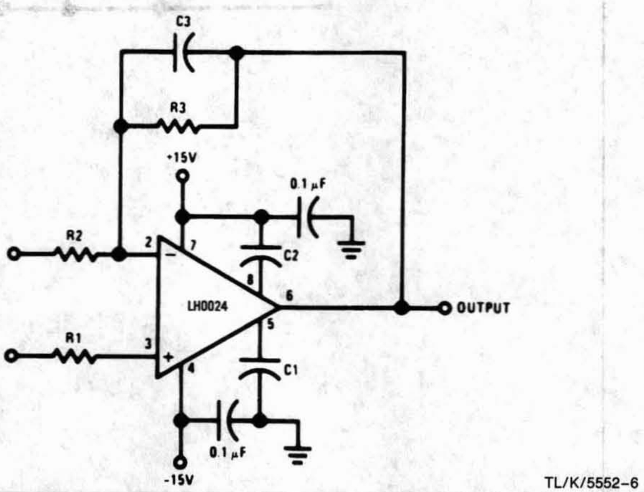
Note 2: Refer to RETS0024 for LH0024H military specifications.

Frequency Compensation

TABLE I

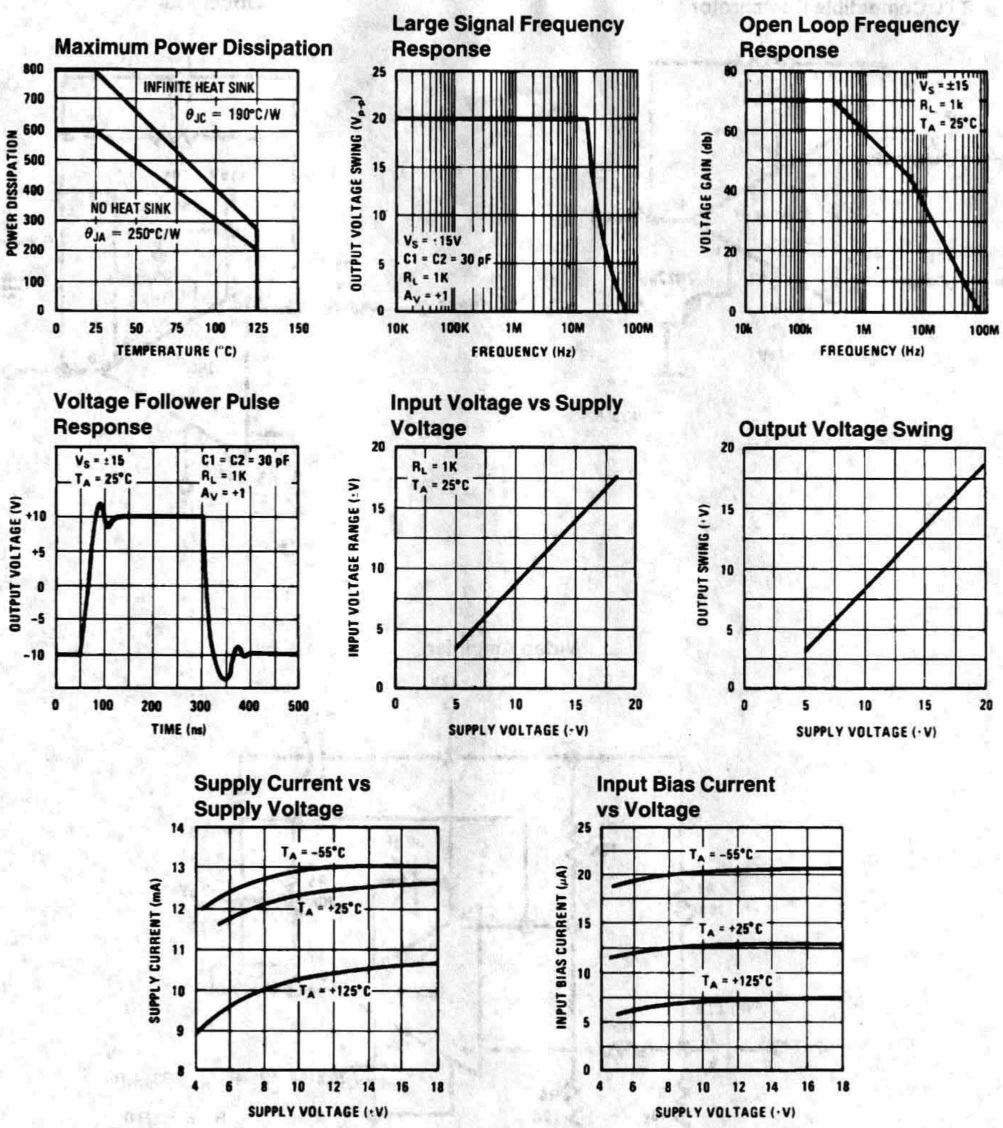
Closed Loop Gain	C_1	C_2	C_3
100	0	0	0
20	0	0	0
10	0	20 pF	1 pF
1	30 pF	30 pF	3 pF

Frequency Compensation Circuit



TL/K/5552-6

Typical Performance Characteristics


Maximum Power Dissipation

Large Signal Frequency Response

Open Loop Frequency Response

Voltage Follower Pulse Response

Input Voltage vs Supply Voltage

Output Voltage Swing

Supply Current vs Supply Voltage

Input Bias Current vs Voltage

TL/K/5552–7

Applications Information

LAYOUT CONSIDERATIONS

The LH0024/LH0024C, like most high speed circuitry, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near the device as is practicable with at least 0.01 µF disc type capacitors. Compensating capacitors should also be placed as close to device as possible.

COMPENSATION RECOMMENDATIONS

Compensation schemes recommended in Table 1 work well under typical conditions. However, poor layout and long lead lengths can degrade the performance of the LH0024 or cause the device to oscillate. Slight adjustments in the values for C1, C2, and C3 may be necessary for a given layout. In particular, when operating at a gain of −1, C3 may require adjustment in order to perfectly cancel the input capacitance of the device.

When operating the LH0024/LH0024C at a gain of +1, the value of R1 should be at least 1 kΩ.

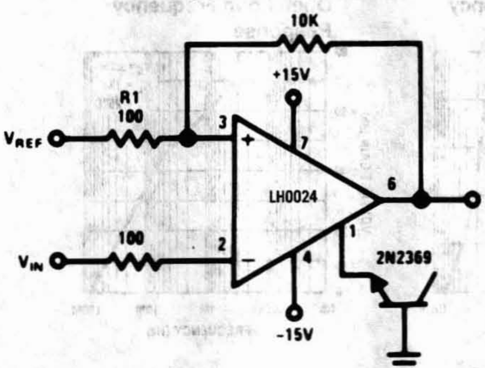
The case of the LH0024 is electrically isolated from the circuit; hence, it may be advantageous to drive the case in order to minimize stray capacitances.

HEAT SINKING

The LH0024/LH0024C is specified for operation without the use of an explicit heat sink. However, internal power dissipation does cause a significant temperature rise. Improved offset voltage drift can be obtained by limiting the temperature rise with a clip-on heat sink such as the Thermalloy 2228B or equivalent.

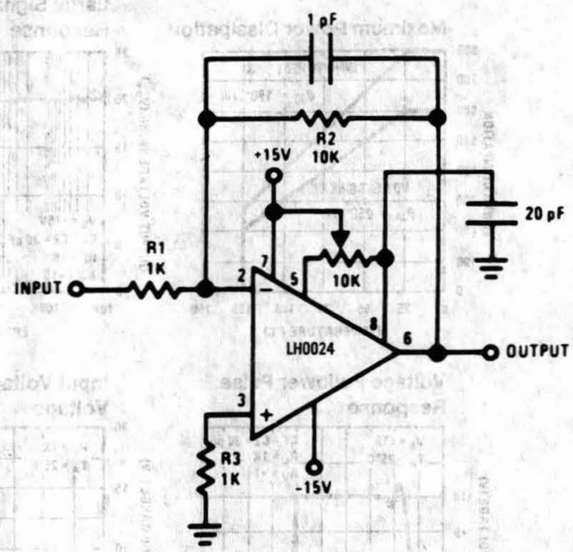
Typical Applications

TTL Compatible Comparator


10K
+15V
R1
100
VREF
3
7
6
LH0024
1
2N2369
100
VIN
2
4
-15V

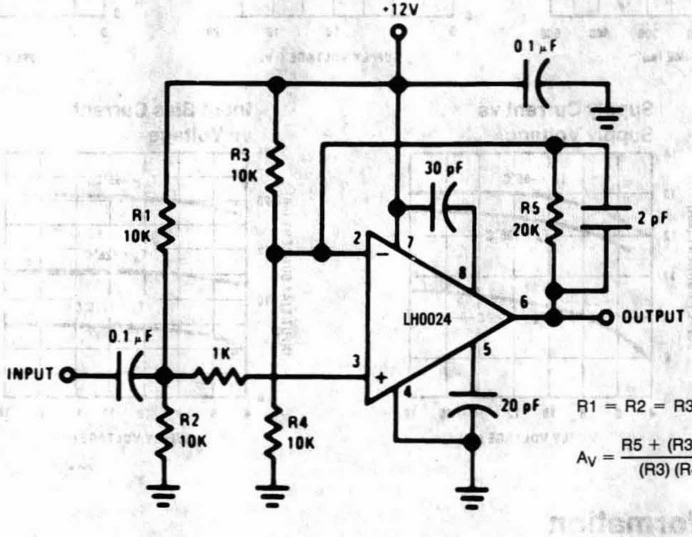
TL/K/5552-3

Offset Null


1 pF
R2
10K
+15V
20 pF
R1
1K
INPUT
7
2
5
10K
8
6
OUTPUT
LH0024
3
R3
1K
-15V

TL/K/5552-4

Video Amplifier


+12V
0.1 µF
R3
10K
30 pF
R5
20K
2 pF
R1
10K
2
7
8
6
LH0024
OUTPUT
0.1 µF
1K
INPUT
3
5
4
20 pF
R2
10K
R4
10K

R1 = R2 = R3 = R4

$$A_V = \frac{R5 + (R3\ R4)}{(R3)\ (R4)} = 5$$

TL/K/5552-5

National Semiconductor

LH0032
Ultra Fast FET-Input Operational Amplifier

General Description

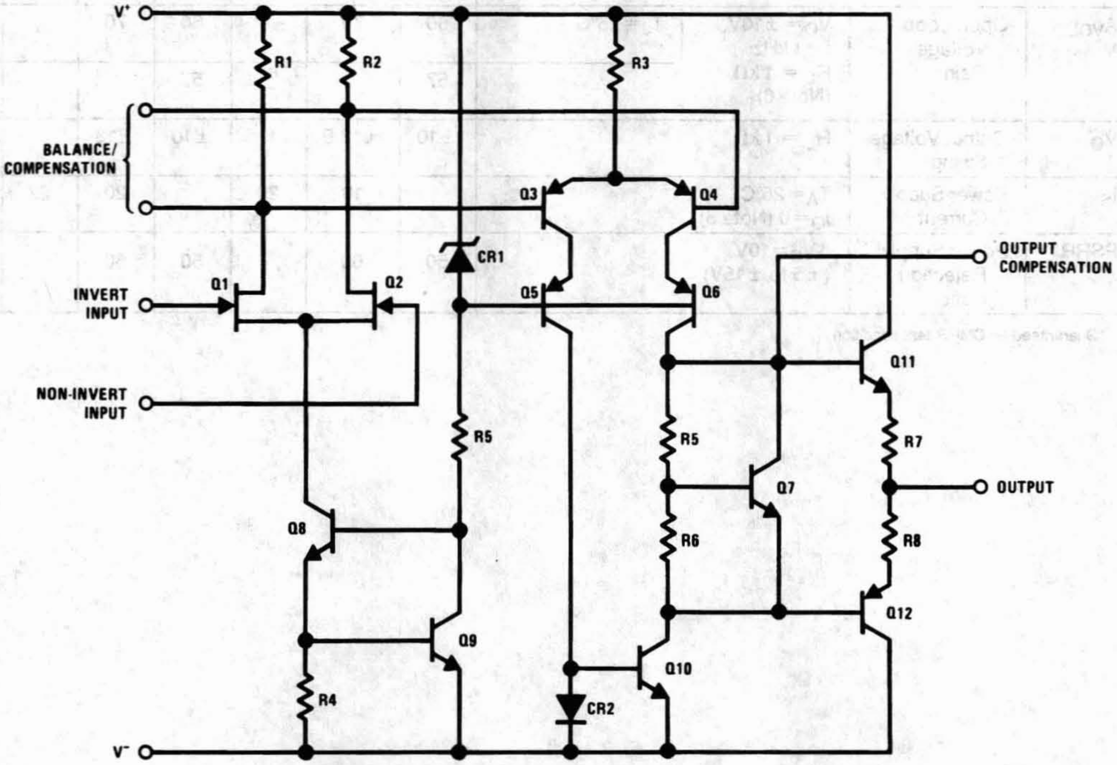
The LH0032 is a high slew rate, high input impedance differential operational amplifier suitable for diverse applications in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A converters, buffers in data acquisition systems and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed for operation over the temperature range −55°C to +125°C, the LH0032C is guaranteed for −25°C to +85°C.

Features

- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- As low as 2 mV max input offset voltage
- FET input
- Peak output current to 100 mA

Schematic



V⁺
R1
R2
R3
BALANCE/ COMPENSATION
Q3
Q4
CR1
OUTPUT COMPENSATION
Q1
Q2
INVERT INPUT
Q5
Q6
NON-INVERT INPUT
Q11
R5
R5
R7
Q7
OUTPUT
Q8
R6
R8
Q12
Q9
Q10
R4
CR2
V⁻

TL/K/5265–1

Absolute Maximum Ratings (Note 9)

Supply Voltage, V_S	±18V
Input Voltage, V_{IN}	$\pm V_S$
Differential Input Voltage	±30V or $\pm 2V_S$
Power Dissipation, P_D	(Note 10)
Steady State Output Current	±100 mA
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range, T_A	
LH0032G	−55°C to +125°C
LH0032CG	−25°C to +85°C
Junction Temperature, T_J	
LH0032G	+175°C
Thermal Resistance (Note 8)	
θ_{JA} G Package	100°C/W
θ_{JC} G Package	70°C/W

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted (Note 2) ($T_A = T_J$)

Symbol	Parameter	Test Conditions		LH0032			LH0032C			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$V_{IN} = 0$	$T_A = T_J = 25°C$ (Note 3)		2	5 10		2	15 20	mV
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift		(Note 4)		15	50		15	50	µV/°C
I_{OS}	Input Offset Current		$T_J = 25°C$ (Note 3) $T_A = 25°C$ (Note 5)			25 250 25			50 500 5	pA pA nA
I_B	Input Bias Current		$T_J = 25°C$ (Note 3) $T_A = 25°C$ (Note 5)			100 1 50			500 5 15	pA nA nA
*V_{INCM}	Input Voltage Range			±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = \pm 10V$		50	60		50	60		dB
A_{VOL}	Open-Loop Voltage Gain	$V_O = \pm 10V$, f = 1 kHz $R_L = 1 k\Omega$ (Note 6)	$T_J = 25°C$	60	70		60	70		dB
				57			57			
V_O	Output Voltage Swing	$R_L = 1 k\Omega$		±10	±13.5		±10	±13		V
I_S	Power Supply Current	$T_A = 25°C$, $I_O = 0$ (Note 5)			18	20		20	22	mA
PSRR	Power Supply Rejection Ratio	$\Delta V_S = 10V$ (±5 to ±15V)		50	60		50	60		dB

*Guaranteed by CMRR test condition.

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1k\Omega$, $T_J = 25°C$ (Note 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
S_R	Slew Rate	$A_V = +1$	$\Delta V_{IN} = 20V$	350	500		V/μs
t_s	Settling Time to 1% of Final Value	$A_V = -1$,			100		ns
t_s	Settling Time to 0.1% of Final Value				300		ns
t_R	Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$			8	20	
t_D	Small Signal Delay Time				10	25	

Note 1: In order to limit maximum junction temperature to +175°C, it may be necessary to operate with VS $< \pm 15V$ when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See applications notes AN-277, "Applications of Wide-Band Buffer Amplifiers" and AN-253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2: LH0032G is 100% production tested as specified at 25°C, 125°C, and −55°C. LH0032CG is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 3: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25$ C. When supply voltages are ± 15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 4: LH0032G is 100% production tested for this parameter. LH0032CG is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 5: Measured in still air 7 minutes after application of power. Guaranteed thru correlated automatic pulse testing.

Note 6: Guaranteed thru correlated automatic pulse testing at $T_J = 25°C$.

Note 7: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

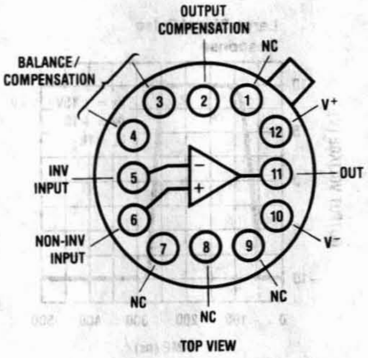
Note 8: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} and T_J max. $T_J = T_A + P_D\theta_{JA}$.

Note 9: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 10: The maximum power dissipation is a function of maximum junction temperature T_J max, total thermal resistance θ_{JA}, and ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J \text{ max} - T_A)/\theta_{JA}$.

Note 11: See RETS0032X for LH0032G military specifications.

Connection Diagram

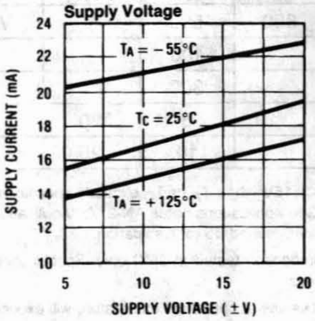


TL/K/5265-23

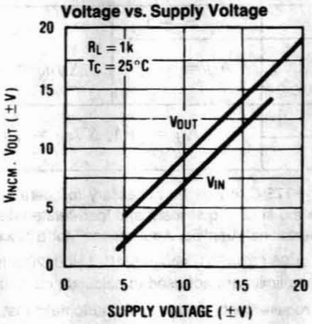
Order Number LH0032G,
LH0032G/883 or LH0032CG
See NS Package Number G12B

Typical Performance Characteristics

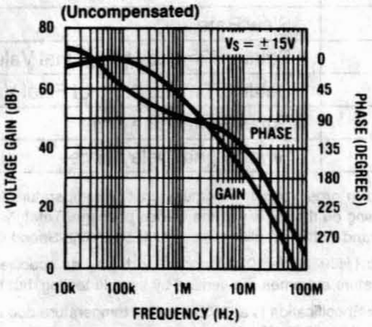
Supply Current vs. Supply Voltage



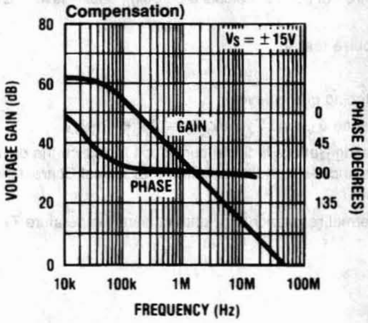
Input Voltage Range and Output Voltage vs. Supply Voltage



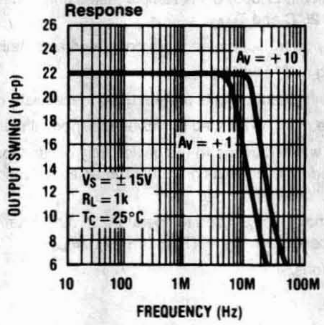
Bode Plot (Uncompensated)



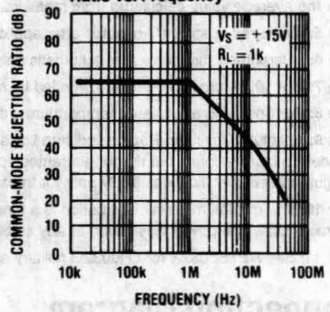
Bode Plot (Unity Gain Compensation)



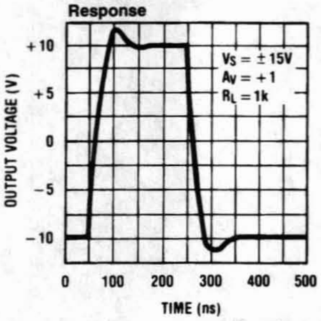
Large Signal Frequency Response



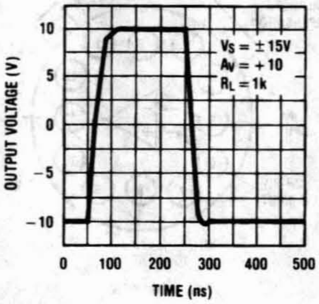
Common Mode Rejection Ratio vs. Frequency



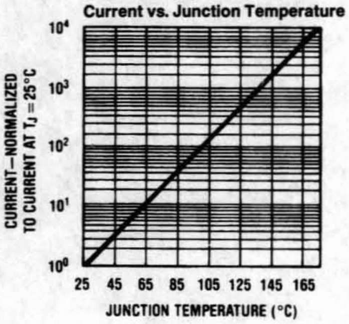
Large Signal Pulse Response



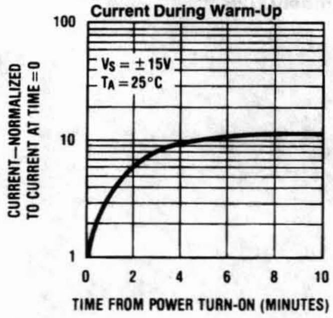
Large Signal Pulse Response



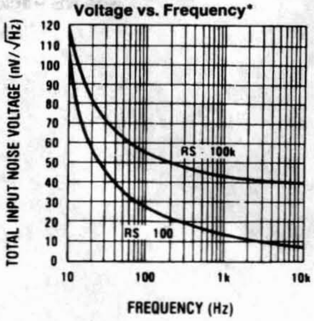
Normalized Input Bias and Offset Current vs. Junction Temperature



Normalized Input Bias Current During Warm-Up



Total Input Noise Voltage vs. Frequency*



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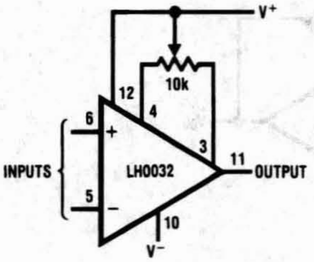
*Noise voltage includes contribution from source resistance.

Auxiliary Circuits

Offset Null


V+
10k
12
4
6
+
INPUTS
LH0032
3
11
OUTPUT
5
−
10
V−

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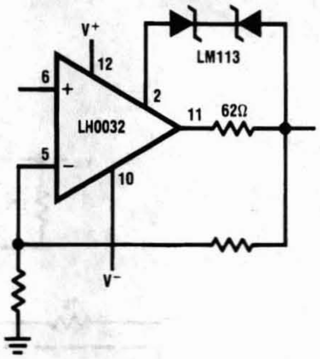
Output Short Circuit Protection


V+
12
LM113
6
+
2
LH0032
11
62Ω
5
−
10
V−

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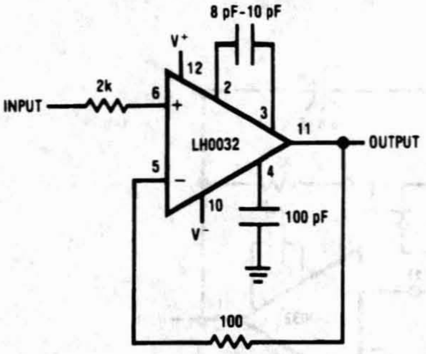
Typical Applications

Unity Gain Amplifier


8 pF-10 pF
V+
12
2
INPUT
2k
6
+
3
11
LH0032
OUTPUT
5
−
4
10
100 pF
V−
100

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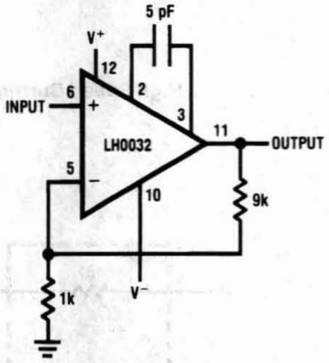
10X Buffer Amplifier


5 pF
V+
12
2
INPUT
6
+
3
11
LH0032
OUTPUT
5
−
10
9k
V−
1k

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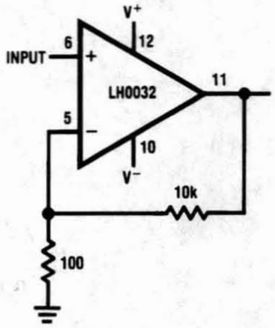
100X Buffer Amplifier


V+
INPUT
6
+
12
11
LH0032
5
−
10
V−
10k
100

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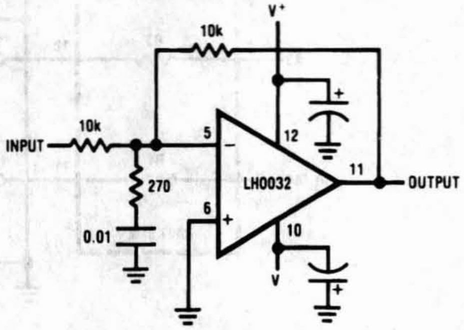
Non-Compensated Unity Gain Inverter


V+
10k
+
10k
5
INPUT
−
12
11
270
LH0032
OUTPUT
6
0.01
+
10
V
+

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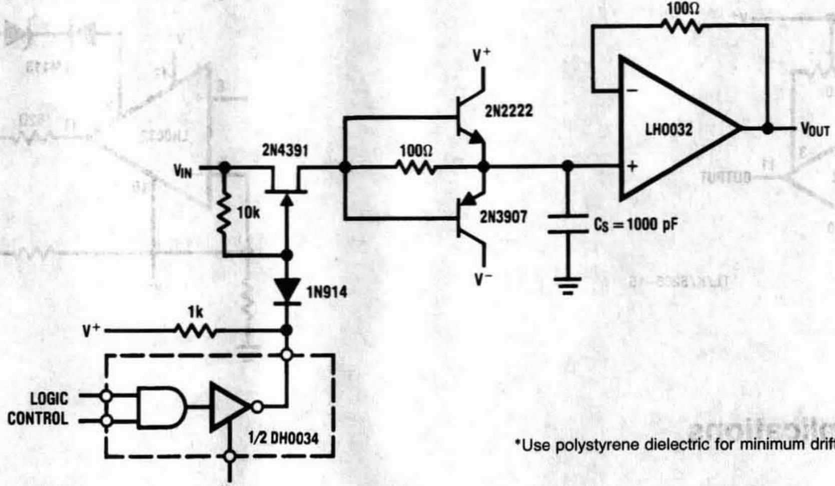
Typical Applications (Continued)

High Speed Sample and Hold


100Ω
V+
2N2222
LH0032
VOUT
2N4391
VIN
100Ω
10k
2N3907
CS = 1000 pF
V−
1N914
1k
V+
LOGIC
CONTROL
1/2 DH0034
V−

*Use polystyrene dielectric for minimum drift

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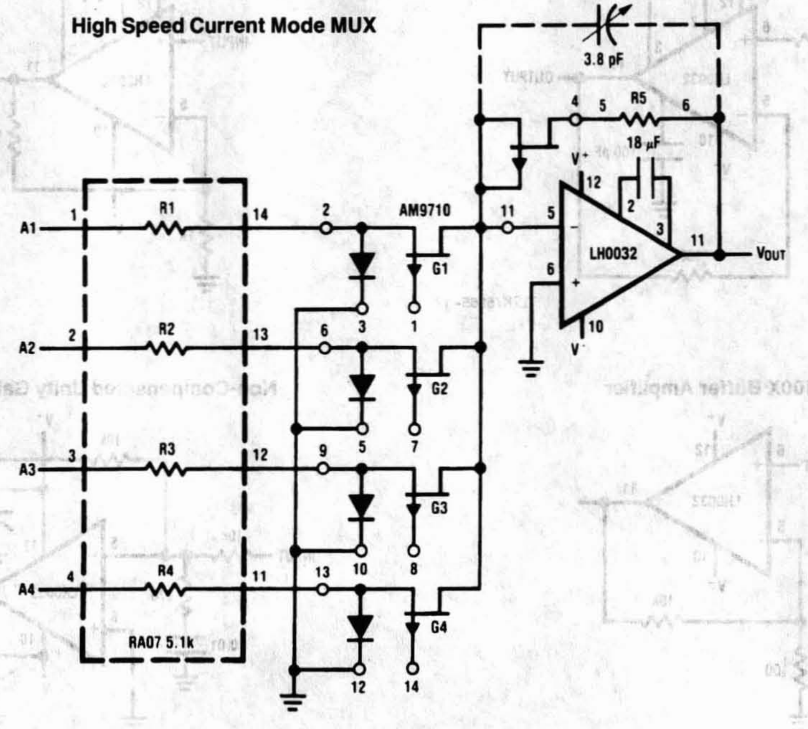
High Speed Current Mode MUX


3.8 pF
4
5
R5
6
18 μF
V+
12
2
3
AM9710
11
5
11
VOUT
LH0032
6
10
V−
A1
1
R1
14
2
G1
1
3
A2
2
R2
13
6
G2
7
5
A3
3
R3
12
9
G3
8
10
A4
4
R4
11
13
G4
RA07 5.1k
12
14

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Applications Information

POWER SUPPLY DECOUPLING

The LH0032/LH0032A, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be by passed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

INPUT CURRENT

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40–60°C above free-air ambient temperature when supplies are ±15V. The de-

Applications Information (Continued)

vice temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

INPUT CAPACITANCE

The input capacitance to the LH0032/LH0032C is typically 5pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

HEAT SINKING

While the LH0032/LH0032A is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information request Application Note AN-253.

Compensating the LH0032

With the LH0032, two compensation schemes may be used, depending on the designer's specific needs.

The first technique is shown in *Figure 14*. It offers the best 0.1% settling time for a ±10V square wave input. The compensation capacitors C_C and C_A should be selected from *Figure 15* for various closed-loop gains. *Figure 16* shows how the LH0032 frequency response is modified for different value compensation capacitors.

Although this approach offers the shortest settling time, the falling edge exhibits overshoot up to 30% lasting 200 to 300 ns. *Figure 17* shows the typical pulse response.

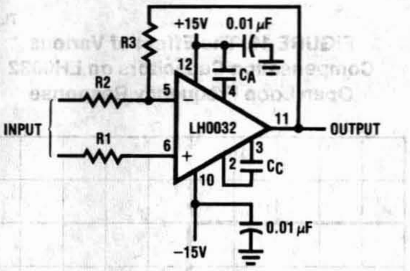

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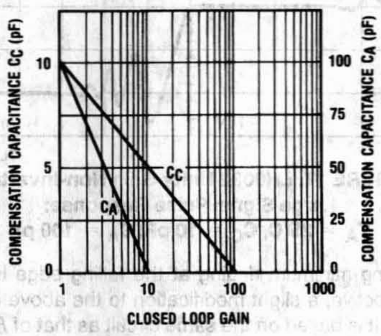
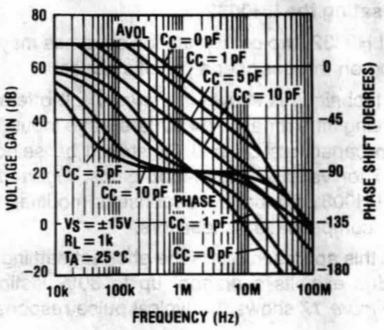
FIGURE 14. LH0032 Frequency Compensation Circuit



TL/K/5265–28

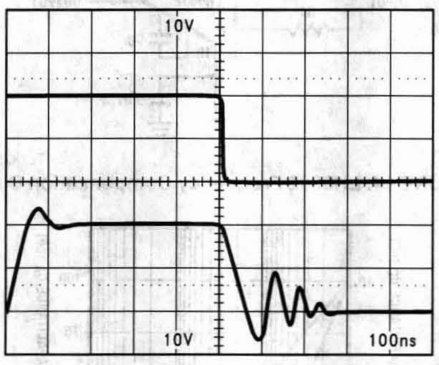
FIGURE 15. Recommended Value of Compensation Capacitor vs. Closed-Loop Gain for Optimum Settling Time

Applications Information (Continued)



TL/K/5265–29

FIGURE 16. The Effect of Various Compensation Capacitors on LH0032 Open Loop Frequency Response



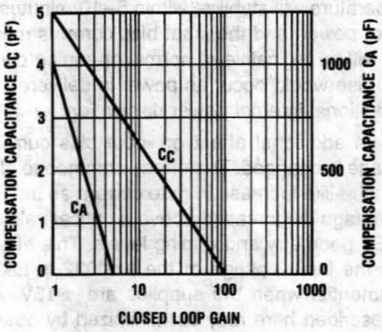
TL/K/5265–30

FIGURE 17. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response: $T_A = 25°C, C_C = 10\ pF, C_A = 100\ pF$

If obtaining minimum ringing at the falling edge is the primary objective, a slight modification to the above is recommended. It is based on the same circuit as that of *Figure 14*.

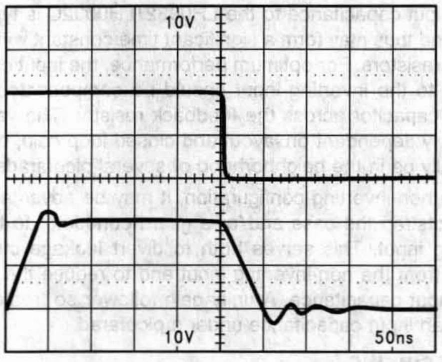
The values of the unity gain compensation capacitors C_C and C_A should be modified to 5 pF and 1000 pF, respectively. *Figure 18* shows the suitable capacitance to use for various closed-loop gains. The resulting unity gain pulse response waveform is shown in *Figure 19*. The settling time to 1% final value is actually superior to the first method of compensation. However, the LH0032 suffers slow settling thereafter to 0.1% accuracy at the falling edge, and nearly four times as much at the rising edge, compared to the previous scheme. Note, however, that the falling edge ringing is considerably reduced. Furthermore, the slew rate is consistently superior using this compensation because of the smaller value of Miller capacitance C_C required. Typical improvement is as much as 50%. A more detailed discussion of this effect is provided in the Slew Response section of this Application Note.

The second compensation scheme works well with both inverting or non-inverting modes. *Figure 20* shows the circuit schematic, in which a 270Ω resistor and a 0.01 μF capacitor are shunted across the inputs of the device. This lag compensation introduces a zero in the loop modifying the response such that adequate phase margin is preserved at unity gain crossover frequency. Note that the circuit requires no additional compensation.



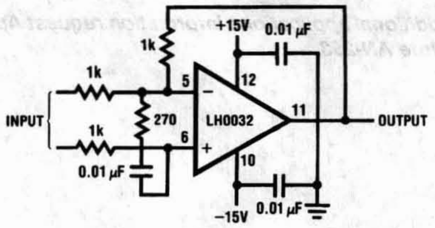
TL/K/5265–31

FIGURE 18. Recommended Value of Compensation Capacitor vs. Closed-Loop Gain for Optimum Slew Rate



TL/K/5265–32

FIGURE 19. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response: $C_C = 5\ pF, C_A = 1000\ pF$



TL/K/5265–33

FIGURE 20. LH0032 Non-Compensated Unity Gain Compensation

National Semiconductor

LH0042
Low Cost FET Op Amp

General Description

The LH0042 is a FET input operational amplifier with very high input impedance and low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The LH0042 is internally compensated and is free of latch-up.

The LH0042 is specified for operation over the −55°C to +125°C military temperature range. The LH0042C is specified for operation over the −25°C to +85°C temperature range.

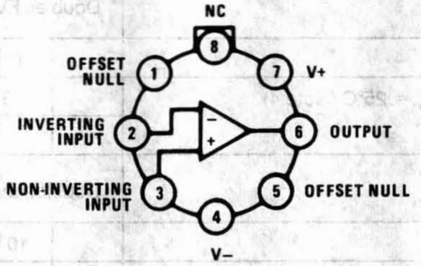
The LH0042 op amp is intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents. The LH0042 provides low cost high performance for such applications as electrometer and photocell amplification, picoammeters, and high input impedance buffers.

Features

- High open loop gain—100 dB typ
- Internal compensation
- Pin compatible with standard IC op amps (TO-99 package)

Connection Diagram

Metal Can Package



TL/K/5557–3

Top View

Order Number LH0042H-MIL, LH0042H or LH0042CH
See NS Package Number H08D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Power Dissipation (see Graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V

Short Circuit Duration	Continuous
Operating Temperature Range	
LH0022, LH0042, LH0052	−55°C to +125°C
LH0022C, LH0042C, LH0052C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics for LH0022/LH0022C (Note 3) $T_A = T_J(Max)$

Parameter	Conditions	Limits						Units
		LH0022			LH0022C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 100\ k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$		2.0	4.0		3.5	6.0	mV
	$R_S \le 100\ k\Omega$, $V_S = \pm 15V$			5.0			7.0	mV
Temperature Coefficient of Input Offset Voltage	$R_S \le 100\ k\Omega$		10			15		μV/°C
Offset Voltage Drift with Time			3			4		μV/week
Input Offset Current	$T_A = 25°C$ (Note 4)		0.2	2.0		1.0	5.0	pA
				2.0			0.5	nA
Temperature Coefficient of Input Offset Current		Doubles Every 10°C			Doubles Every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	$T_A = 25°C$ (Note 4)		5	10		10	25	pA
				10			2.5	nA
Temperature Coefficient of Input Bias Current		Doubles Every 10°C			Doubles Every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm 15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$, $V_{IN} = \pm 10V$	74	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$, $\pm 5V \le V_S \le \pm 15V$	74	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$ $T_A = 25°C$, $V_S = \pm 15V$	75	100		75	100		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$ $V_S = \pm 15V$	30			30			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm 15V$		2.0	2.5		2.4	2.8	mA
Power Consumption	$V_S = \pm 15V$			75			85	mW

DC Electrical Characteristics for LH0042/LH0042C (Note 3)

Parameter	Conditions	Limits						Units
		LH0042			LH0042C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 100\ k\Omega$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \le 100\ k\Omega$		10			15		μV/°C
Offset Voltage Drift with Time			7.0			10		μV/week
Input Offset Current	$T_A = 25°C$ (Note 4)		1.0	5.0		2.0	10	pA
Input Bias Current	$T_A = 25°C$ (Note 4)		10	25		15	50	pA
Temperature Coefficient of Input Bias Current		Doubles Every 10°C			Doubles Every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$, $V_{IN} = \pm 10V$	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$, $\pm 5V \le V_S \le \pm 15V$	70	86		70	86		dB
Large Signal Voltage Gain	$R_S \le 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$	50	100		25	100		V/mV
	$R_S \le 2\ k\Omega$, $V_{OUT} = \pm 10V$	30			25			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current	$V_S = \pm 15V$		2.5	3.5		2.8	4.0	mA
Power Consumption	$V_S = \pm 15V$			105			120	mW

DC Electrical Characteristics for LH0052/LH0052C (Note 3) (Continued)

Parameter	Conditions	Limits						Units
		LH0052			LH0052C			
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	$T_A = 25°C$ (Note 4)		0.5	2.5		1.0	5.0	pA
				2.5			0.5	nA
Temperature Coefficient of Input Bias Current		Doubles Every 10°C			Doubles Every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm10V$	74	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm5V \leq V_S \leq \pm15V$	74	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm10V$ $V_S = \pm15V$, $T_A = 25°C$	75	100		75	100		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm10V$ $V_S = \pm15V$	30			30			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$ $V_S = \pm15V$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$, $V_S = \pm15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm15V$		3.0	3.5		3.0	3.8	mA
Power Consumption	$V_S = \pm15V$			105			114	mW

AC Electrical Characteristics for all amplifiers ($T_A = 25°C$, $V_S = \pm15V$)

Parameter	Conditions	Limits						Units
		LH0022/42/52			LH0022C/42C/52C			
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/μs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	μs
Overshoot			10	30		15	40	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$		4.5			4.5		μs
Overload Recovery			4.0			4.0		μs

AC Electrical Characteristics for all amplifiers (T_A = 25°C, V_S = ±15V) (Continued)

Parameter	Conditions	Limits						Units
		LH0042			LH0042C			
		Min	Typ	Max	Min	Typ	Max	
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		nV/√Hz
	R_S = 10 kΩ, f_o = 100 Hz		55			55		nV/√Hz
	R_S = 10 kΩ, f_o = 1 kHz		35			35		nV/√Hz
	R_S = 10 kΩ, f_o = 10 kHz		30			30		nV/√Hz
	BW = 10 Hz to 10kHz, R_S = 10 kΩ		12			12		μVrms

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.

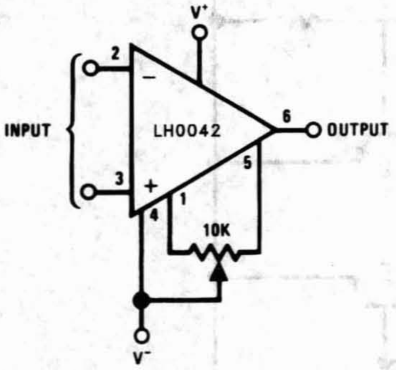
Note 3: Unless otherwise specified, these specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C for the LH0042 and −25°C ≤ T_A ≤ +85°C for the LH0042C. Typical values are given for T_A = 25°C.

Note 4: Input currents are a strong function of temperature. Due to high speed testing they are specified at a junction temperature T_j = 25°C. Self heating will cause an increase in current in manual tests. 25°C spec is guaranteed by testing at 125°C.

Note 5: See RETS0042X for the LH0042H military specifications.

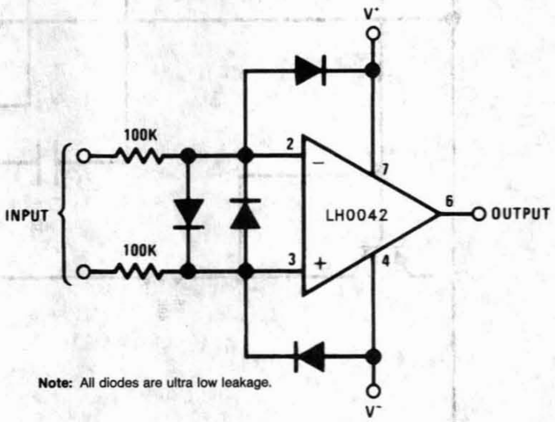
Auxiliary Circuits (Shown for TO-99 pin out)

Offset Null



TL/K/5557-5

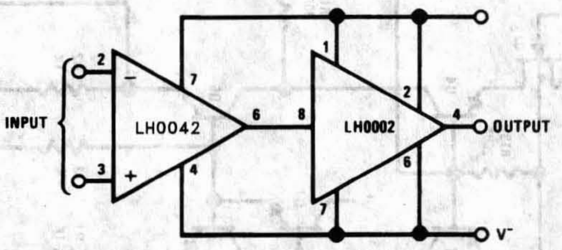
Protecting Inputs from ±150V Transients



Note: All diodes are ultra low leakage.

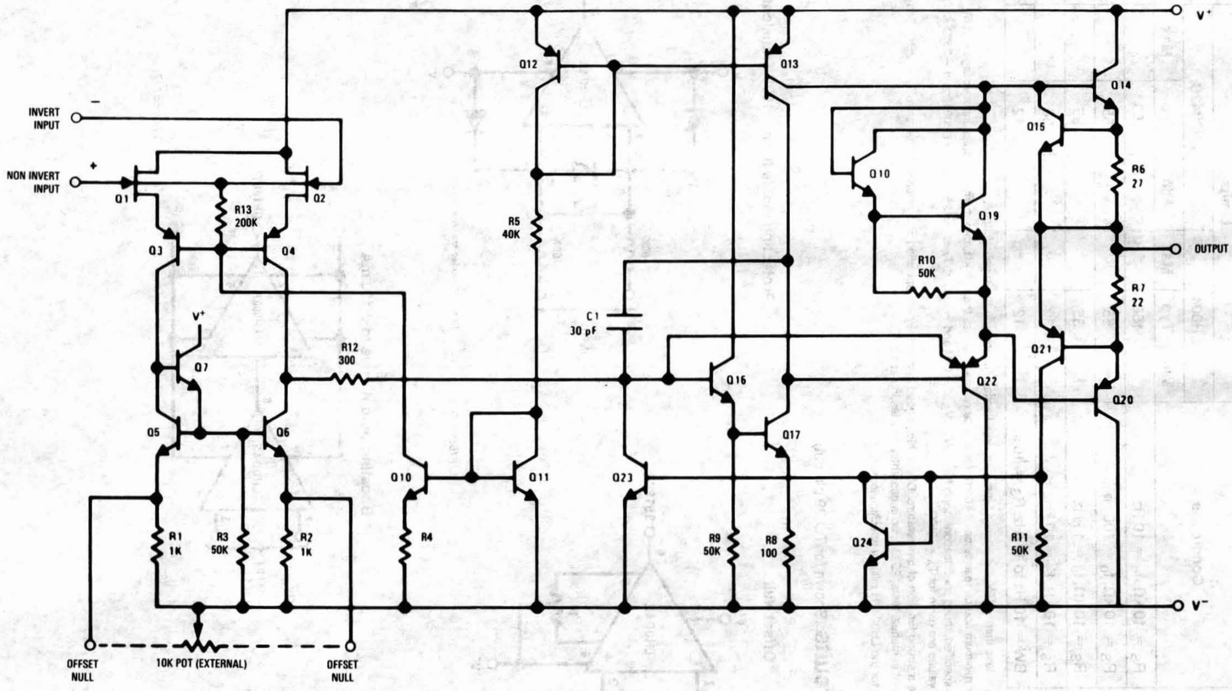
TL/K/5557-6

Boosting Output Drive to ±100 mA



TL/K/5557-7

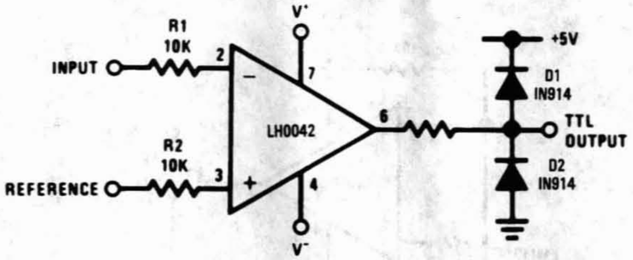
Schematic Diagram


V⁺
INVERT INPUT
−
NON INVERT INPUT
+
Q1
Q2
R13 200K
Q3
Q4
V⁺
Q7
Q5
Q6
R1 1K
R3 50K
R2 1K
OFFSET NULL
10K POT (EXTERNAL)
OFFSET NULL
R12 300
Q12
R5 40K
Q10
R4
Q11
C1 30 pF
Q23
Q13
Q16
Q17
R9 50K
R8 100
Q24
Q10
Q19
R10 50K
Q22
Q14
Q15
R6 27
OUTPUT
R7 22
Q21
Q20
R11 50K
V⁻

TL/K/5557–1

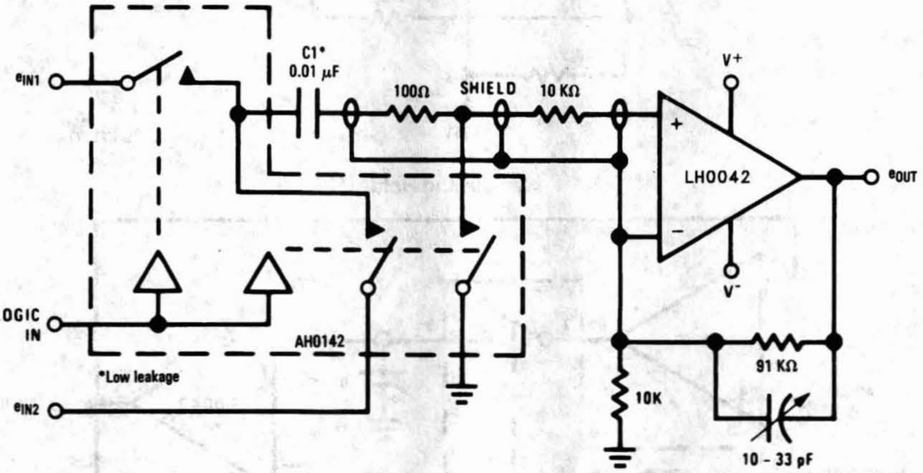
Typical Applications

Precision Voltage Comparator


V⁺
R1
10K
INPUT
2
7
−
6
LH0042
R2
10K
REFERENCE
3
+
4
V⁻
+5V
D1
IN914
TTL
OUTPUT
D2
IN914

TL/K/5557-9

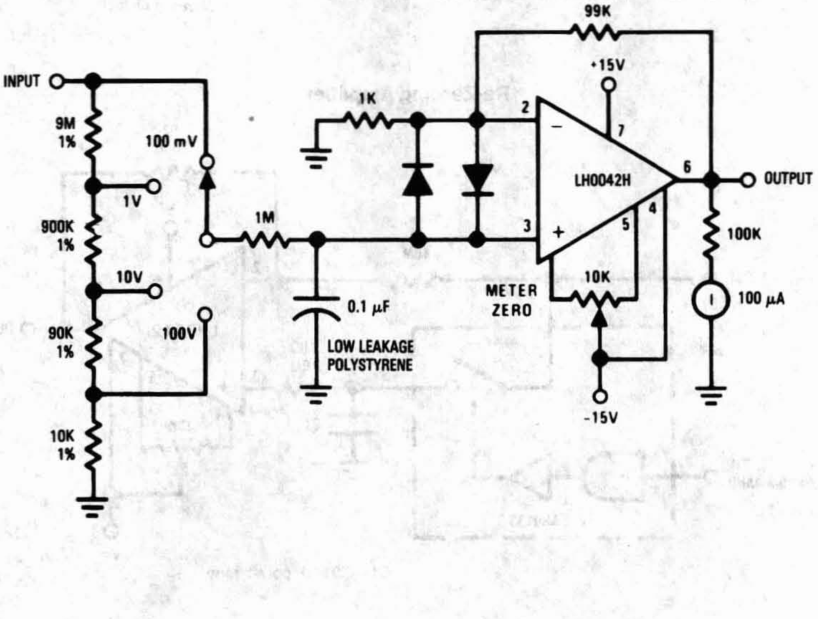
Subtractor for Automatic Test Gear


C1*
0.01 μF
e_{IN1}
100Ω
SHIELD
10 KΩ
V+
+
LH0042
e_{OUT}
−
V⁻
LOGIC
IN
AH0142
*Low leakage
e_{IN2}
91 KΩ
10K
10 - 33 pF

TL/K/5557-11

$e_{OUT} = 10 \times (e_{IN1} - e_{IN2})$

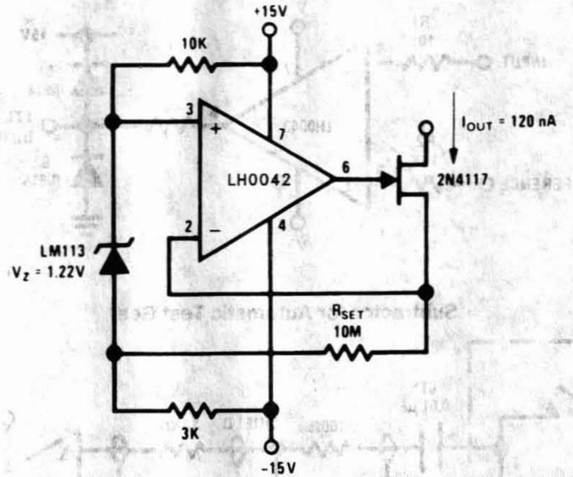
Sensitive Low Cost "VTVM"


99K
+15V
INPUT
1K
2
9M
1%
100 mV
−
7
LH0042H
6
OUTPUT
1V
1M
4
900K
1%
3
+
5
100K
10V
METER
ZERO
10K
0.1 μF
100 μA
90K
1%
100V
LOW LEAKAGE
POLYSTYRENE
-15V
10K
1%

TL/K/5777-12

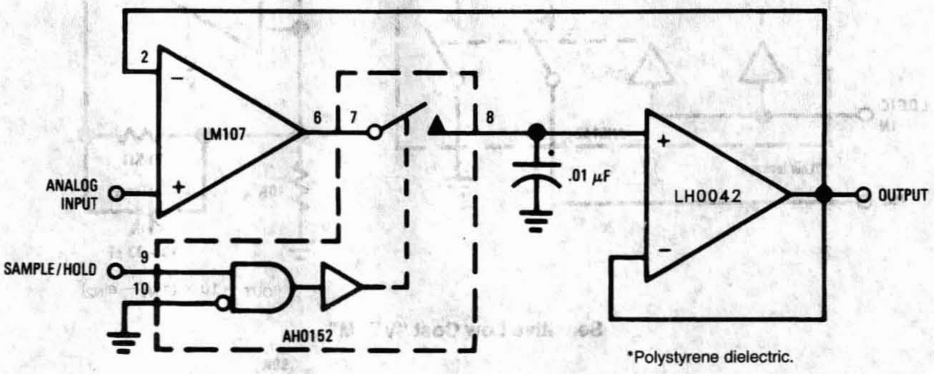
Typical Applications (Continued)

Ultra Low Level Current Source


+15V
10K
3
+
7
LH0042
6
2N4117
I_{OUT} = 120 nA
2
−
4
LM113
V_Z = 1.22V
R_{SET}
10M
3K
-15V

TL/K/5777-13

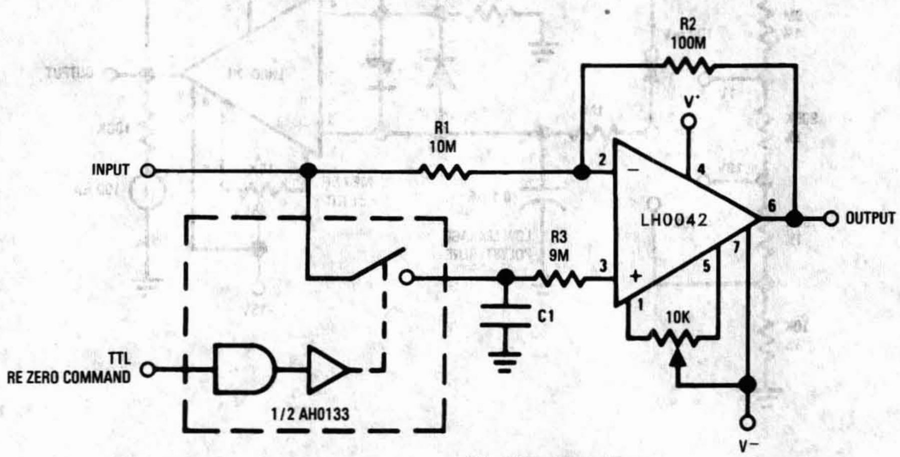
Sample and Hold


2
−
LM107
+
6
7
8
ANALOG INPUT
.01 µF
+
LH0042
−
OUTPUT
SAMPLE/HOLD
9
10
AH0152

*Polystyrene dielectric.

TL/K/5557-16

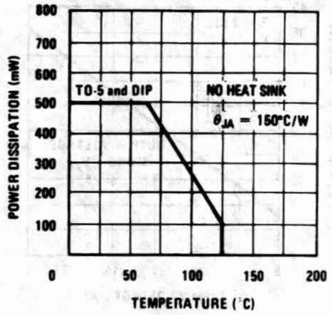
Re-Zeroing Amplifier


R2
100M
V+
R1
10M
INPUT
2
−
4
LH0042
6
OUTPUT
7
R3
9M
3
+
5
C1
1
10K
TTL
RE ZERO COMMAND
1/2 AH0133
V−

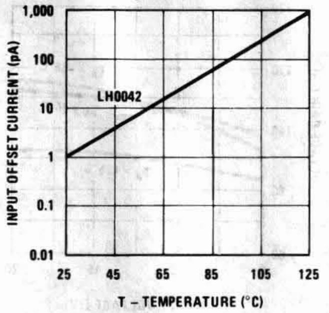
C1—0.01 µF polystyrene.

TL/K/5557-17

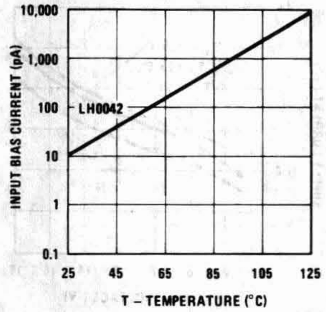
Typical Performance Characteristics



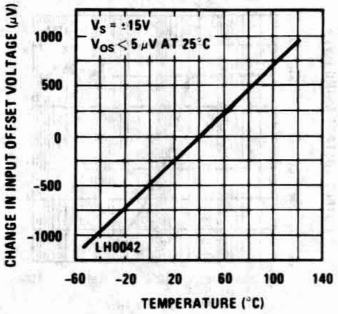
Maximum Power Dissipation



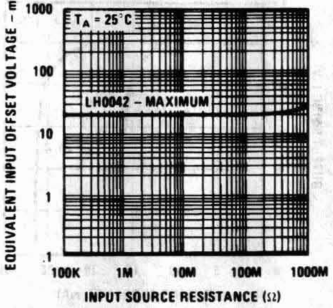
Input Offset Current vs Temperature



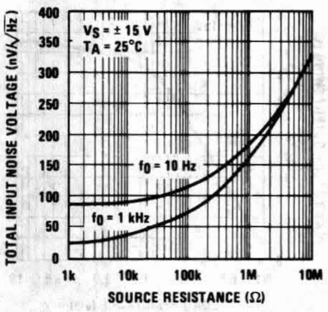
Input Bias Current vs Temperature



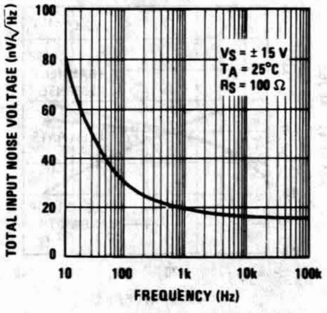
Input Offset Voltage vs Temperature



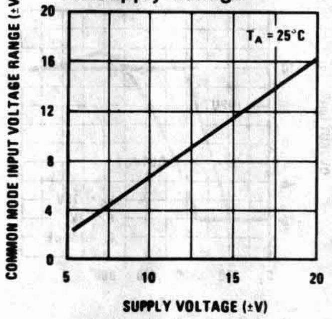
Offset Error (without V_{OS} Null)



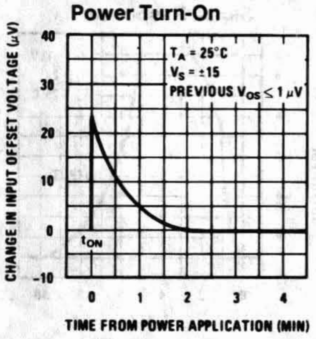
Total Input Noise Voltage* vs Source Resistance



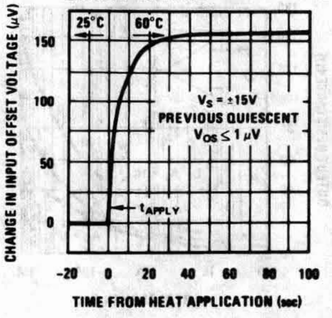
Total Input Noise Voltage* vs Frequency



Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On

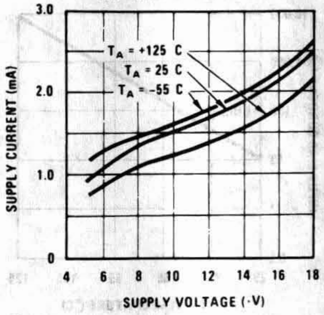


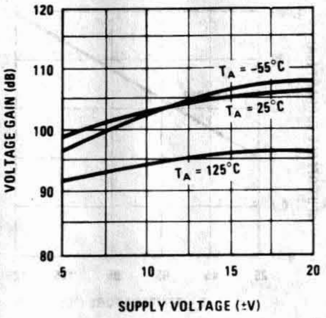
Change in Input Offset Voltage Due to Thermal Shock vs Time

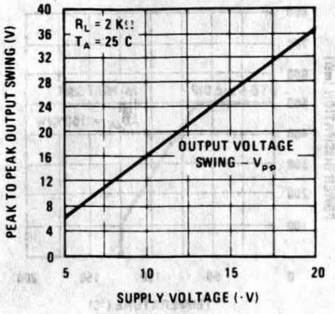
TL/K/5557–18

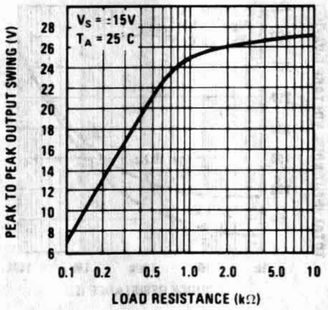
*Noise voltage includes contribution from source resistance.

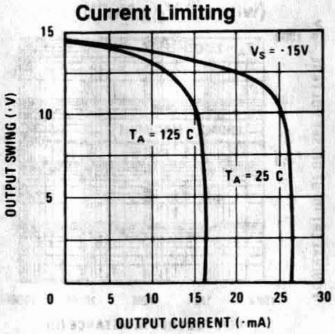
Typical Performance Characteristics (Continued)

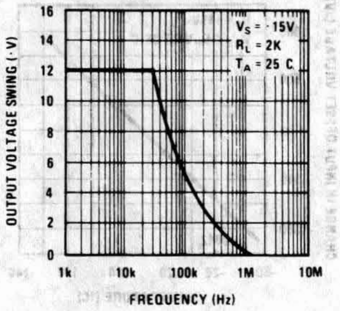

Supply Voltage vs Supply Current

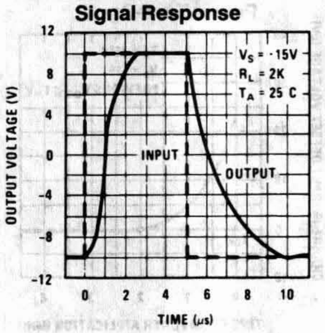

Voltage Gain

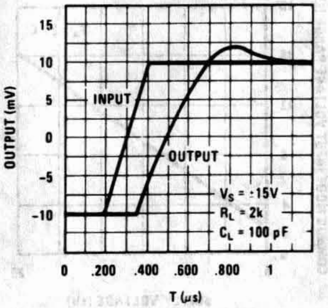

Output Swing vs Supply Voltage

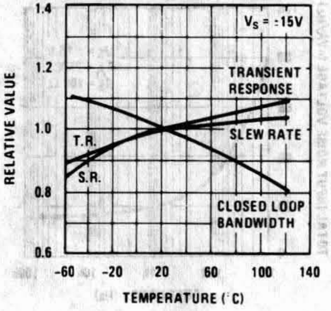

Output Voltage Swing vs Load Resistance

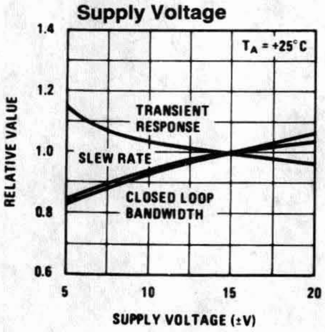

Current Limiting

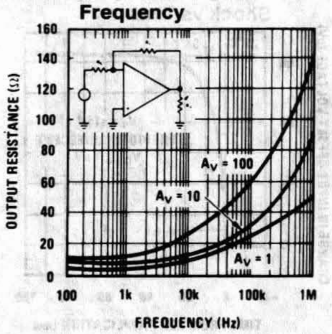

Output Voltage Swing vs Frequency

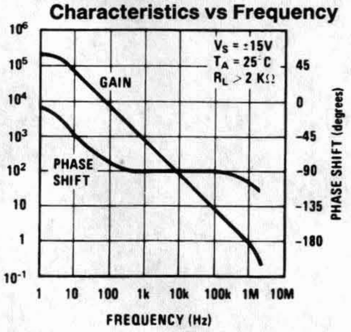

Voltage Follower Large Signal Response


Transient Response


Frequency Characteristics vs Ambient Temperature


Frequency Characteristics vs Supply Voltage


Output Resistance vs Frequency


Open Loop Transfer Characteristics vs Frequency

TL/K/5557–19

National Semiconductor

LH0101 Power Operational Amplifier

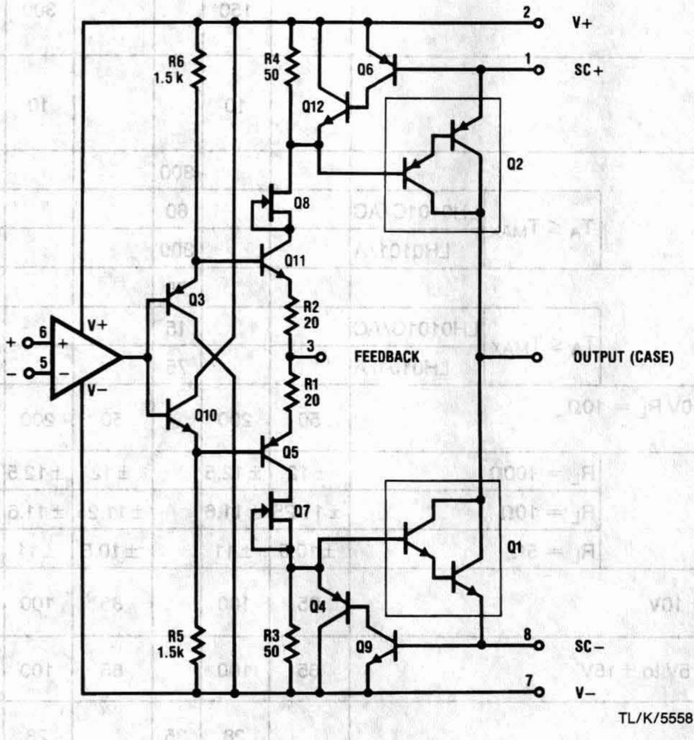
General Description

The LH0101 is a wideband power operational amplifier featuring FET inputs, internal compensation, virtually no crossover distortion, and rapid settling time. These features make the LH0101 an ideal choice for DC or AC servo amplifiers, deflection yoke drives, programmable power supplies, and disk head positioner amplifiers. The LH0101 is packaged in an 8 pin TO-3 hermetic package, rated at 60 watts with a suitable heat sink.

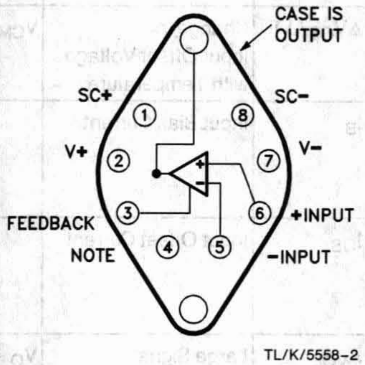
Features

- 5 Amp peak, 2 Amp continuous output current
- 300 kHz power bandwidth
- 850 mW standby power (±15V supplies)
- 300 pA input bias current
- 10 V/μs slew rate
- Virtually no crossover distortion
- 2 μs settling time to 0.01%
- 5 MHz gain bandwidth

Schematic and Connection Diagrams


2
V+
1
SC+
R6
1.5 k
R4
50
Q6
Q12
Q2
Q8
Q11
Q3
R2
20
3
FEEDBACK
OUTPUT (CASE)
+
6
−
5
V+
V−
R1
20
Q10
Q5
Q7
Q1
Q4
R5
1.5k
R3
50
Q9
8
SC−
7
V−

TL/K/5558-1


CASE IS OUTPUT
SC+
SC−
V+
V−
FEEDBACK
NOTE
+INPUT
−INPUT
1
2
3
4
5
6
7
8

TL/K/5558-2

Top View

Order Numbers LH0101K, LH0101K-MIL, LH0101CK, LH0101AK, LH0101AK-MIL or LH0101ACK
See NS Package Number K08A

Note: Electrically connected internally, no connection should be made to pin.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Supply Voltage, V_S	±22V
Power Dissipation at $T_A = 25°C$, P_D	5W
Derate linearly at 25°C/W to zero at 150°C,	
Power Dissipation at $T_C = 25°C$	62W
Derate linearly at 2°C/W to zero at 150°C	
Differential Input Voltage, V_{IN}	$\pm 40V$ but $< \pm V_S$
Input Voltage Range, V_{CM}	$\pm 20V$ but $< \pm V_S$
Thermal Resistance— See Typical Performance Characteristics	
Peak Output Current (50 ms pulse), $I_{O(PK)}$	5A
Output Short Circuit Duration (within rated power dissipation, $R_{SC} = 0.35\Omega$, $T_A = 25°C$)	Continuous
Operating Temperature Range, T_A	
LH0101AC, LH0101C	−25°C to +85°C
LH0101A, LH0101	−55°C to +125°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_J	150°C
Lead Temperature (Soldering <10 sec.)	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 1) $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Conditions			LH0101AC LH0101A			LH0101C LH0101			Units
					Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage					1	3		5	10	mV
		$T_{MIN} \le T_A \le T_{MAX}$					7			15	
$\Delta V_{OS}/\Delta P_D$	Change in Input Offset Voltage with Dissipated Power	(Note 2)				150			300		μV/W
$\Delta V_{OS}/\Delta T$	Change in Input Offset Voltage with Temperature	$V_{CM} = 0$				10			10		μV/°C
I_B	Input Bias Current						300			1000	pA
			$T_A \le T_{MAX}$	LH0101C/AC			60			60	nA
				LH0101/A			300			1000	
I_{OS}	Input Offset Current						75			250	pA
			$T_A \le T_{MAX}$	LH0101C/AC			15			15	nA
				LH0101/A			75			250	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 10\Omega$			50	200		50	200		V/mV
V_O	Output Voltage Swing	$R_{SC} = 0$	$R_L = 100\Omega$		±12	±12.5		±12	±12.5		V
		$A_V = +1$	$R_L = 10\Omega$		±11.25	±11.6		±11.25	±11.6		
		Note 3	$R_L = 5\Omega$		±10.5	±11		±10.5	±11		
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = \pm 10V$			85	100		85	100		dB
PSRR	Power Supply Rejection Ratio	$\Delta V_S = \pm 5V$ to $\pm 15V$			85	100		85	100		
I_S	Quiescent Supply Current					28	35		28	35	mA

AC Electrical Characteristics (Note 1), $V_S = \pm 15V$, $T_A = 25°C$

Symbol	Parameter	Conditions		LH0101 LH0101A			LH0101C LH0101AC			Units
				Min	Typ	Max	Min	Typ	Max	
e_n	Equivalent Input Noise Voltage	f = 1 kHz			25			25		nV√Hz
C_{IN}	Input Capacitance	f = 1 MHz			3.0			3.0		pF
	Power Bandwidth, −3 dB	$R_L = 10\Omega$	$A_V = +1$		300			300		kHz
SR	Slew Rate			7.5 (Note 4)	10			10		V/μs
t_r, t_f	Small Signal Rise or Fall Time				200			200		ns
	Small Signal Overshoot				10			10		%
GBW	Gain-Bandwidth Product	$R_L = \infty$		4.0 (Note 4)	5.0			5.0		MHz
t_s	Large Signal Settling Time to 0.01%				2.0			2.0		μs
THD	Total Harmonic Distortion	$P_O = 10W$, f = 1 kHz $R_L = 10\Omega$			0.008			0.008		%

Note 1: Specification is at $T_A = 25°C$. Actual values at operating temperature may differ from the $T_A = 25°C$ value. When supply voltages are ±15V, quiescent operating junction temperature will rise approximately 20°C without heat sinking. Accordingly, V_{OS} may change 0.5 mV and I_B and I_{OS} will change significantly during warm-ups. Refer to the I_B vs. temperature and power dissipation graphs for expected values. Power supply voltage is ±15V. Temperature tests are made only at extremes.

Note 2: Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heat sink.

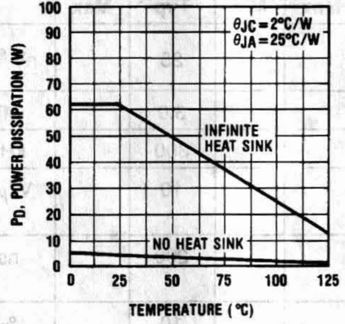
Note 3: At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation.

Note 4: These parameters are sample tested to 10% LTPD.

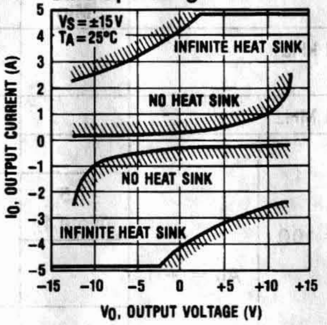
Note 5: Refer to RETS0101AK for the LH0101AK military specifications and RETS0101K for the LH0101K military specifications.

Typical Performance Characteristics

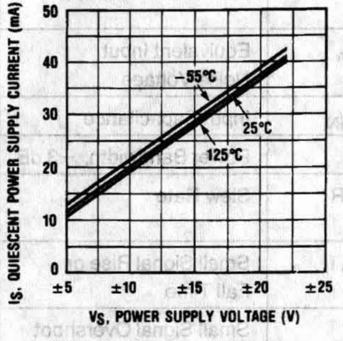
Maximum Power Dissipation



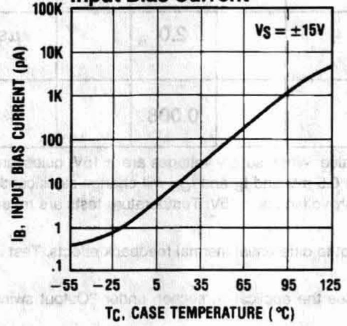
Safe Operating Area



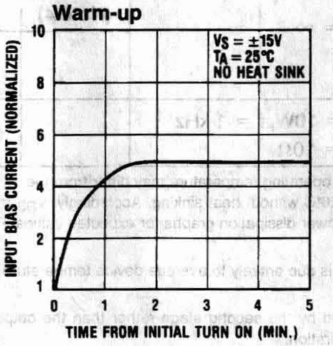
Quiescent Power Supply Current



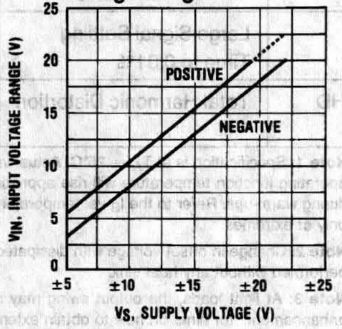
Input Bias Current



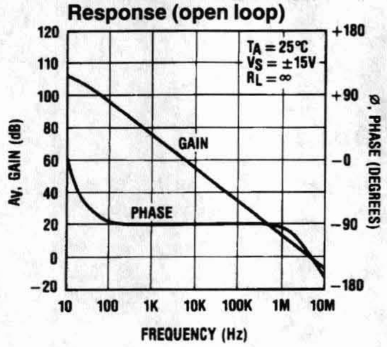
Input Bias Current after Warm-up



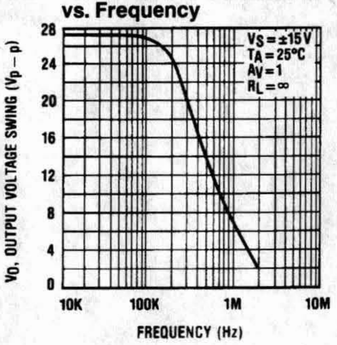
Input Common-Mode Voltage Range



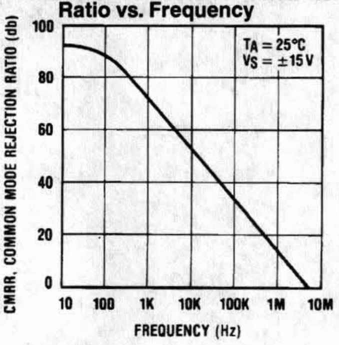
Small Signal Frequency Response (open loop)



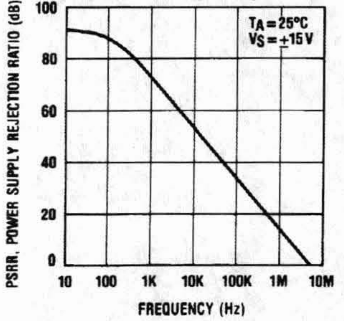
Output Voltage Swing vs. Frequency



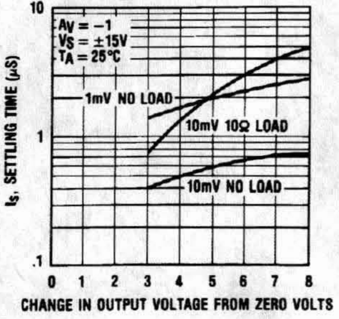
Common-Mode Rejection Ratio vs. Frequency



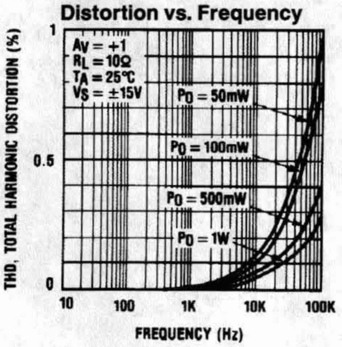
Power Supply Rejection Ratio vs. Frequency



Settling Time



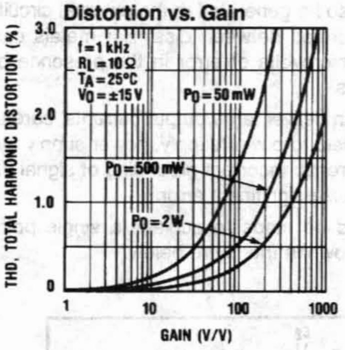
Total Harmonic Distortion vs. Frequency



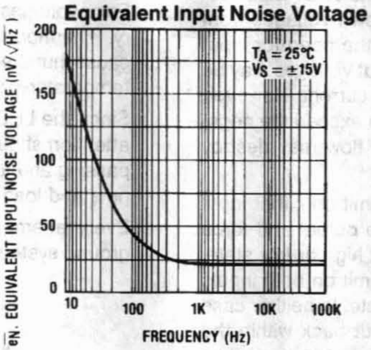
TL/K/5558–3

Typical Performance Characteristics (Continued)

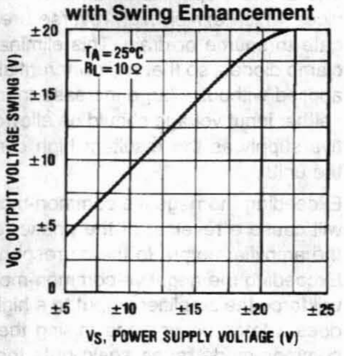
Total Harmonic Distortion vs. Gain



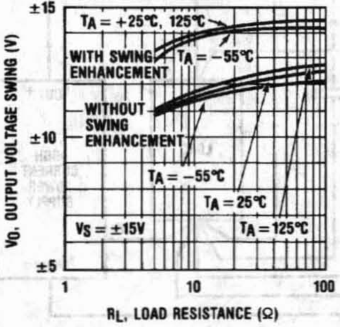
Equivalent Input Noise Voltage



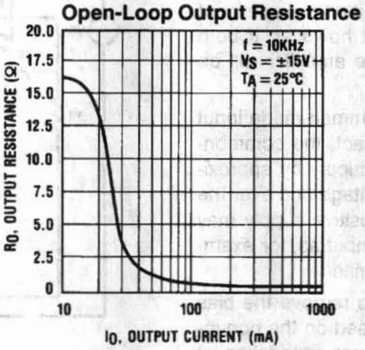
Output Voltage Swing with Swing Enhancement



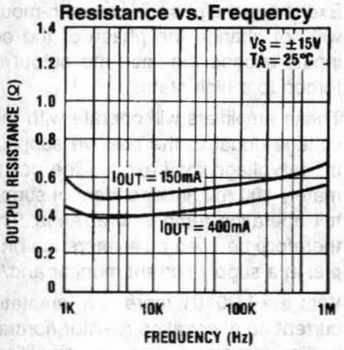
Output Voltage Swing vs. Load Resistance



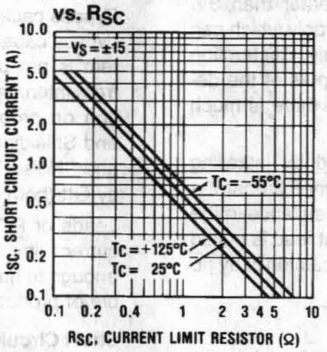
Open-Loop Output Resistance



Open-Loop Output Resistance vs. Frequency

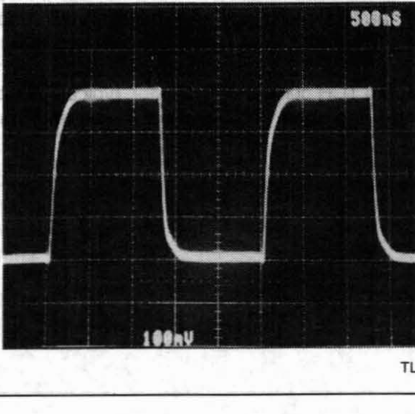


Short Circuit Current vs. R_{SC}



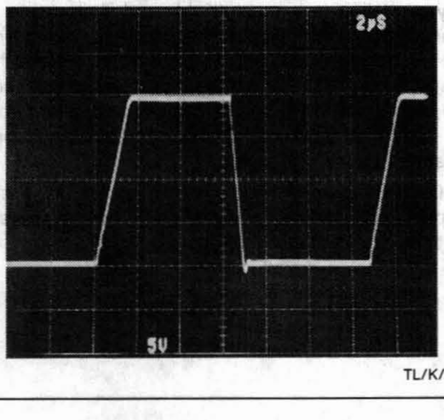
TL/K/5558–4

Small Signal Pulse Response (No Load)



TL/K/5558–5

Large Signal Pulse Response (R_L = 10Ω)



TL/K/5558–6

Application Hints

Input Voltages

The LH0101 operational amplifier contains JFET input devices which exhibit high reverse breakdown voltages from gate to source or drain. This eliminates the need for input clamp diodes, so that high differential input voltages may be applied without a large increase in input current. However, neither input voltage should be allowed to exceed the negative supply as the resultant high current flow may destroy the unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage may exceed the positive supply by approximately 100 mV, independent of supply voltage and over the full operating temperature range. The positive supply may therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

With the LH0101 there is a temptation to remove the bias current compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than 3V. The potential problem involves loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the inputs of the device is not limited to less than 100 mA or if there is much more than 1 μF bypass on the supply buss.

Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LH0101.

Layout Considerations

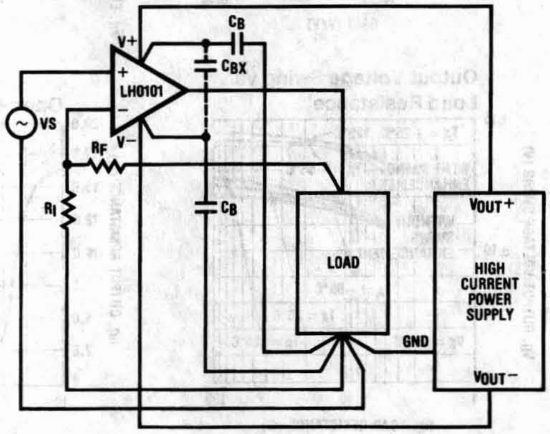
When working with circuitry capable of resolving pico-ampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs. Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients.

Since the LH0101 can deliver large output currents, careful attention should be paid to power supply, power supply bypassing and load currents. Incorrect grounding of signal inputs and load can cause significant errors.

Every attempt should be made to achieve a single point ground system as shown in the figure below.



TL/K/5558-7

FIGURE 1. Single-Point Grounding

Bypass capacitor C_{BX} should be used if the lead lengths of bypass capacitors C_B are long. If a single point ground system is not possible, keep signal, load, and power supply from intermingling as much as possible. For further information on proper grounding techniques refer to "Grounding and Shielding Techniques in Instrumentation" by Morrison, and "Noise Reduction Techniques in Electronic Systems" by Ott (both published by John Wiley and Sons).

Leads or PC board traces to the supply pins, short-circuit current limit pins, and the output pin must be substantial enough to handle the high currents that the LH0101 is capable of producing.

Short Circuit Current Limiting

Should current limiting of the output not be necessary, SC+ should be shorted to V+ and SC− should be shorted to V−. Remember that the short circuit current limit is dependent upon the total resistance seen between the supply and current limit pins. This total resistance includes the desired resistor plus leads, PC Board traces, and solder joints.* Assuming a zero TCR current limit resistor, typical temperature coefficient of the short circuit current will be approximately .3%/°C.

*Short circuit current will be limited to approximately $\frac{0.6}{RSC}$.

Application Hints (Continued)

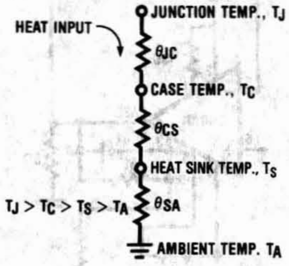
Thermal Resistance

The thermal resistance between two points of a conductive system is expressed as:

$$\theta_{12} = \frac{T_1 - T_2}{P_D}\ ^\circ\text{C/W}$$

where subscript order indicates the direction of heat flow. A simplified heat transfer circuit for a cased semiconductor and heat sink system is shown in the figure below.

The circuit is valid only if the system is in thermal equilibrium (constant heat flow) and there are, indeed, single specific temperatures T_J, T_C and T_S (no temperature distribution in junction, case, or heat sink). Nevertheless, this is a reasonable approximation of actual performance.



TL/K/5558–8

FIGURE 2. Semiconductor-Heat Sink Thermal Circuit

The junction-to-case thermal resistance θ_{JC} specified in the data sheet depends upon the material and size of the package, die size and thickness, and quality of the die bond to the case or lead frame. The case-to-heat sink thermal resistance θ_{CS} depends on the mounting of the device to the heat sink and upon the area and quality of the contact surface. Typical θ_{CS} for a TO-3 package is 0.5 to 0.7°C/W, and 0.3 to 0.5°C/W using silicone grease.

The heat sink to ambient thermal resistance θ_{SA} depends on the quality of the heat sink and the ambient conditions.

Cooling is normally required to maintain the worst case operating junction temperature T_J of the device below the specified maximum value $T_{J(MAX)}$. T_J can be calculated from known operating conditions. Rewriting the above equation, we find:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}\ ^\circ\text{C/W}$$

$$T_J = T_A + P_D\theta_{JA}\ ^\circ\text{C}$$

Where: $P_D\ (V_S - V_{OUT})I_{OUT} + |V+ - (V-)|I_Q$
for a DC Signal

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ and V_S = Supply Voltage

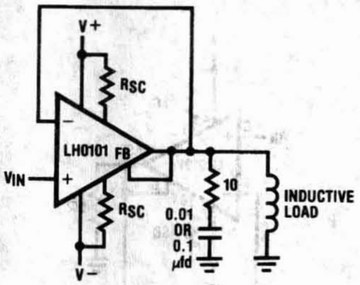
θ_{JC} for the LH0101 is about 2°C/W.

Stability and Compensation

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time consistant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

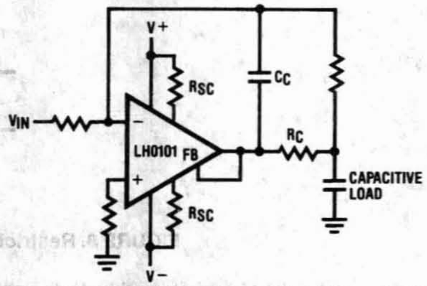
Some inductive loads may cause output stage oscillation. A .01 μF ceramic capacitor in series with a 10Ω resistor from the output to ground will usually remedy this situation.



TL/K/5558–9

FIGURE 3. Driving Inductive Loads

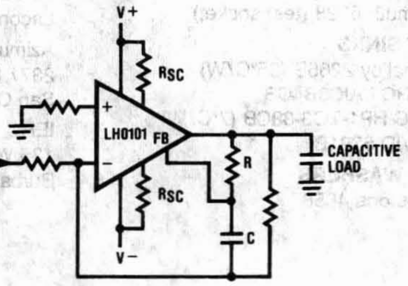
Capacitive loads may be compensated for by traditional techniques. (See "Operational Amplifiers: Theory and Practice" by Roberge, published by Wiley):



TL/K/5558–10

FIGURE 4. R_C and C_C Selected to Compensate for Capacitive Load

A similar but alternative technique may be used for the LH0101:



TL/K/5558–11

FIGURE 5. Alternate Compensation for Capacitive Load

Application Hints (Continued)

Output Swing Enhancement

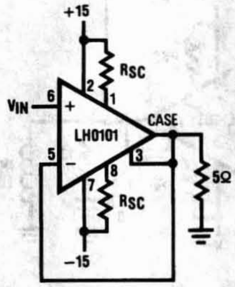
When the feedback pin is connected directly to the output, the output voltage swing is limited by the driver stage and not by output saturation. Output swing can be increased as shown by taking gain in the output stage as shown in High Power Voltage Follower with Swing Enhancement below. Whenever gain is taken in the output stage, as in swing enhancement, either the output stage, or the entire op amp must be appropriately compensated to account for the additional loop gain.

Output Resistance

The open loop output resistance of the LH0101 is a function of the load current. No load output resistance is approximately 10Ω. This decreases to under 1Ω for load currents exceeding 100 mA.

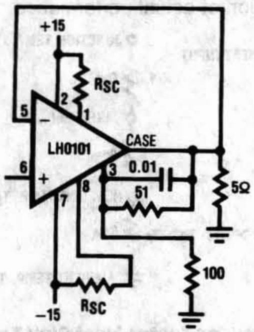
Typical Applications

See AN261 for more information.



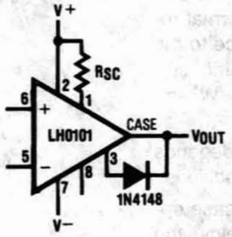
TL/K/5558–12

FIGURE 6. High Power Voltage Follower



TL/K/5558–13

FIGURE 7. High Power Voltage Follower with Swing Enhancement



TL/K/5558–14

FIGURE 8. Restricting Outputs to Positive Voltages Only

Following is a partial list of sockets and heat dissipators for use with the LH0101. National assumes no responsibility for their quality or availability.

8-Lead TO-3 Hardware

SOCKETS

Keystone 4626 or 4627
Robinson Nugent 0002011
Azimuth 6028 (test socket)

HEAT SINKS

Thermalloy 2266B (35°C/W)
IERC LAIC3B4CB
IERC HP1-TO3-33CB (7°C/W)
AAVID 5791B

MICA WASHERS

Keystone 4658

AAVID Engineering
30 Cook Court
Laconia, New Hampshire 03246

Azimuth Electronics
2377 S. El Camino Real
San Clemente, CA 92572

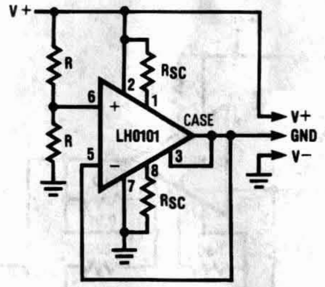
IERC
135 W. Magnolia Blvd.
Burbank, CA 91502

Keystone Electronics Corp.
49 Bleecker St.
New York, NY 10012

Robinson Nugent Inc.
800 E. 8th St.
New Albany, IN 47150

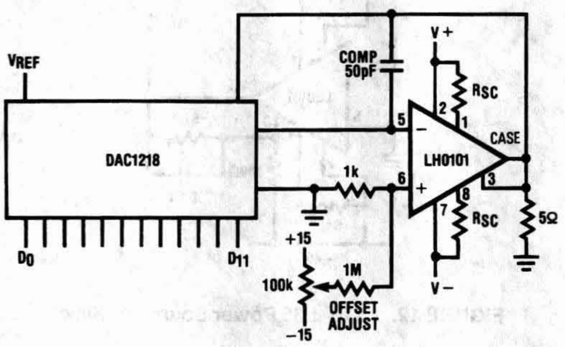
Thermalloy
P.O. Box 34829
Dallas, TX 75234

Typical Applications (Continued)


V+
R
R
RSC
RSC
2
1
6
5
7
8
3
+
−
LH0101
CASE
V+
GND
V−

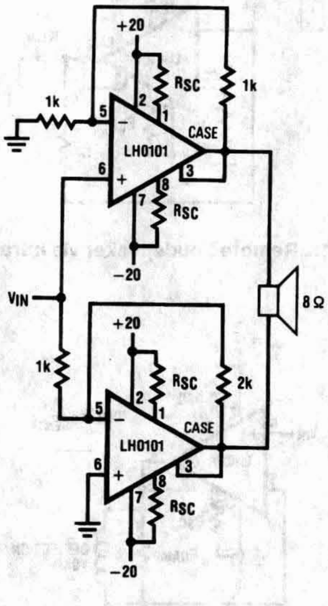
TL/K/5558-15

FIGURE 9. Generating a Split Supply from a Single Voltage Supply


VREF
DAC1218
D0
D11
COMP
50pF
V+
RSC
RSC
2
1
5
6
7
8
3
−
+
LH0101
CASE
1k
5Ω
+15
100k
1M
OFFSET
ADJUST
−15
V−

TL/K/5558-16

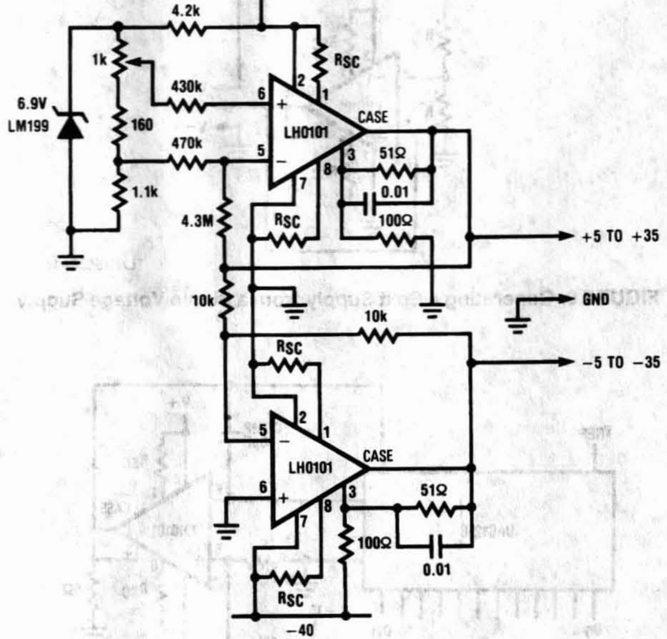
FIGURE 10. Power DAC


+20
RSC
1k
1k
2
1
5
6
7
8
3
−
+
LH0101
CASE
RSC
−20
VIN
8Ω
+20
1k
RSC
2k
2
1
5
6
7
8
3
−
+
LH0101
CASE
RSC
−20

TL/K/5558-17

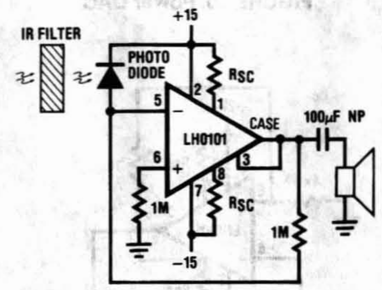
FIGURE 11. Bridge Audio Amplifier

Typical Applications (Continued)


+40
4.2k
1k
RSC
430k
6.9V
LM199
160
470k
1.1k
6
2
1
+
LH0101
CASE
5
−
3
51Ω
8
7
0.01
4.3M
RSC
100Ω
+5 TO +35
10k
GND
10k
RSC
−5 TO −35
2
5
1
LH0101
CASE
6
+
3
51Ω
8
7
100Ω
0.01
RSC
−40

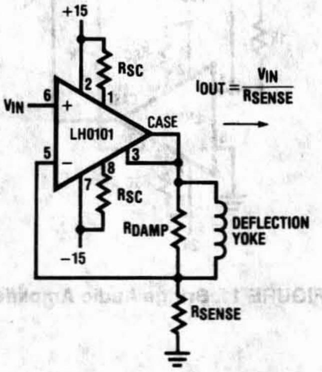
TL/K/5558–18

FIGURE 12. ±5 to ±35 Power Source or Sink


IR FILTER
+15
PHOTO DIODE
RSC
2
5
1
LH0101
CASE
100μF NP
6
+
3
8
7
RSC
1M
1M
−15

TL/K/5558–19

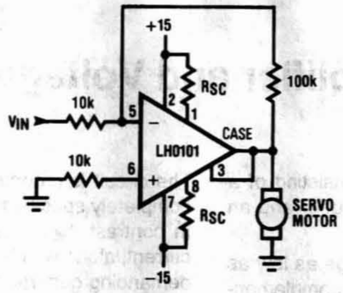
FIGURE 13. Remote Loudspeaker via Infrared Link


+15
RSC
2
1
6
VIN
+
$I_{OUT} = \frac{V_{IN}}{R_{SENSE}}$
LH0101
CASE
5
−
3
8
7
RSC
RDAMP
DEFLECTION YOKE
−15
RSENSE

TL/K/5558–20

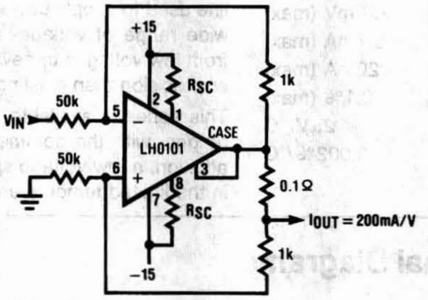
FIGURE 14. CRT Deflection Yoke Driver

Typical Applications (Continued)


+15
RSC
100k
2
1
VIN
10k
5
−
LH0101
CASE
10k
6
+
3
7
8
RSC
SERVO
MOTOR
−15

TL/K/5558-21

FIGURE 15. DC Servo Amplifier


+15
RSC
1k
2
50k
VIN
5
1
−
LH0101
CASE
50k
6
+
3
8
0.1Ω
IOUT = 200mA/V
7
RSC
1k
−15

TL/K/5558-22

FIGURE 16. High Current Source/Sink

National Semiconductor

LM10 Operational Amplifier and Voltage Reference

General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV. Some other characteristics of the LM10 are

■ input offset voltage	2.0 mV (max)
■ input offset current	0.7 nA (max)
■ input bias current	20 nA (max)
■ reference regulation	0.1% (max)
■ offset voltage drift	2μV/°C
■ reference drift	0.002%/°C

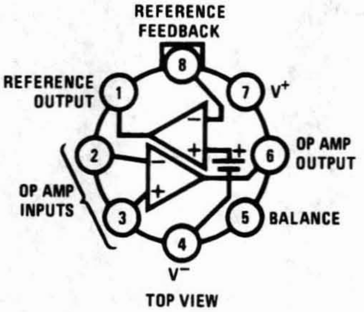
The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

Connection and Functional Diagrams

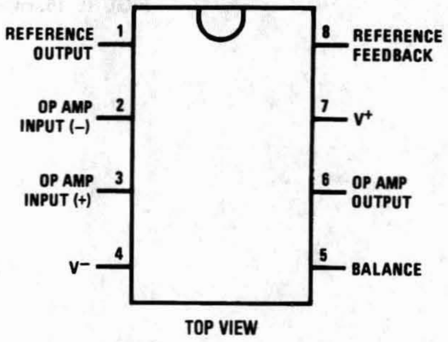
Metal Can Package (H)


REFERENCE FEEDBACK
8
REFERENCE OUTPUT
1
7
V+
2
6
OP AMP OUTPUT
OP AMP INPUTS
3
5
BALANCE
4
V−
TOP VIEW

TL/H/5652–1

Order Number LM10BH, LM10CH, LM10CLH or LM10H/883 available per SMA# 5962-8760401 See NS Package Number H08A

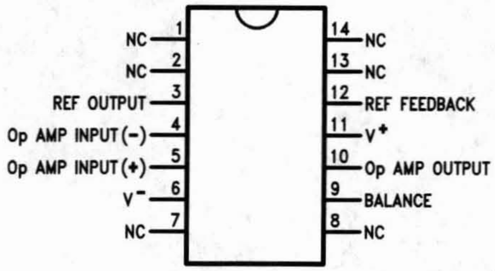
Dual-In-Line Package (N)


REFERENCE OUTPUT
1
8
REFERENCE FEEDBACK
OP AMP INPUT (−)
2
7
V+
OP AMP INPUT (+)
3
6
OP AMP OUTPUT
V−
4
5
BALANCE
TOP VIEW

TL/H/5652–15

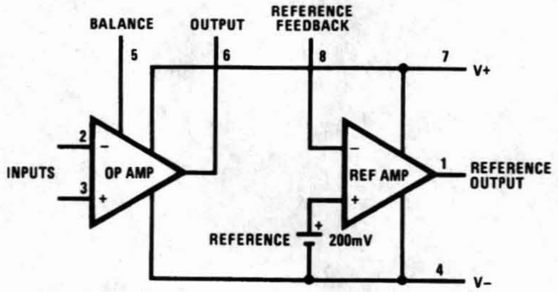
Order Number LM10CN or LM10CLN See NS Package Number N08E

Small Outline Package (WM)


NC 1
NC 2
REF OUTPUT 3
Op AMP INPUT(−) 4
Op AMP INPUT(+) 5
V− 6
NC 7
14 NC
13 NC
12 REF FEEDBACK
11 V+
10 Op AMP OUTPUT
9 BALANCE
8 NC

TL/H/5652–17

Order Number LM10CWM See NS Package Number M14B


BALANCE
OUTPUT
REFERENCE FEEDBACK
5
6
8
7
V+
2
3
INPUTS
OP AMP
REF AMP
1
REFERENCE OUTPUT
REFERENCE
200mV
4
V−

TL/H/5652–16

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

	LM10/LM10B/ LM10C	LM10BL/ LM10CL
Total Supply Voltage	45V	7V
Differential Input Voltage (note 1)	±40V	±7V
Power Dissipation (note 2)	internally limited	
Output Short-circuit Duration (note 3)	continuous	
Storage-Temp. Range	−55°C to +150°C	
Lead Temp. (Soldering, 10 seconds)		
Metal Can	300°C	
Lead Temp. (Soldering, 10 seconds) DIP	260°C	
Vapor Phase (60 seconds)	215°C	
Infrared (15 seconds)	220°C	

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

Maximum Junction Temperature	
LM10	150°C
LM10B	100°C
LM10C	85°C

Operating Ratings

Package Thermal Resistance	
θ_{JA}	
H Package	150°C/W
N Package	87°C/W
WM Package	90°C/W
θ_{JC}	
H Package	45°C/W

Electrical Characteristics

$T_J = 25°C$, $\mathbf{T_{MIN} \le T_J \le T_{MAX}}$ (note 4) **(Boldface type refers to limits over temperature range)**

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0		0.5	4.0	mV
				3.0			**5.0**	mV
Input offset current (note 5)			0.25	0.7		0.4	2.0	nA
				1.5			**3.0**	nA
Input bias current			10	20		12	30	nA
				30			**40**	nA
Input resistance		250	500		150	400		kΩ
		150			**115**			kΩ
Large signal voltage gain	$V_S = \pm 20V$, $I_{OUT} = 0$	120	400		80	400		V/mV
	$V_{OUT} = \pm 19.95V$	**80**			**50**			V/mV
	$V_S = \pm 20V$, $V_{OUT} = \pm 19.4V$	50	130		25	130		V/mV
	$I_{OUT} = \pm 20$ mA **(±15 mA)**	**20**			**15**			V/mV
	$V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA	1.5	3.0		1.0	3.0		V/mV
	$V_{OUT} = \pm 0.4V$ **(±0.3V), $\mathbf{V_{CM} = -0.4V}$**	**0.5**			**0.75**			V/mV
Shunt gain (note 6)	1.2V **(1.3V)** $\le V_{OUT} \le 40V$,	14	33		10	33		V/mV
	$R_L = 1.1$ kΩ							
	0.1 mA $\le I_{OUT} \le$ 5 mA	**6**			**6**			V/mV
	$1.5V \le V^+ \le 40V$, $R_L = 250\Omega$	8	25		6	25		V/mV
	0.1 mA $\le I_{OUT} \le$ 20 mA	**4**			**4**			V/mV
Common-mode rejection	$-20V \le V_{CM} \le 19.15V$ **(19V)**	93	102		90	102		dB
	$V_S = \pm 20V$	**87**			**87**			dB
Supply-voltage rejection	$-0.2V \ge V^- \ge -39V$	90	96		87	96		dB
	$V^+ = 1.0V$ **(1.1V)**	**84**			**84**			dB
	1.0V **(1.1V)** $\le V^+ \le 39.8V$	96	106		93	106		dB
	$V^- = -0.2V$	**90**			**90**			dB
Offset voltage drift			2.0			5.0		µV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift	$T_C < 100°C$		60			90		pA/°C
Line regulation	1.2V **(1.3V)** $\le V_S \le 40V$		0.001	0.003		0.001	0.008	%/V
	$0 \le I_{REF} \le 1.0$ mA, $V_{REF} = 200$ mV			**0.006**			**0.01**	%/V
Load regulation	$0 \le I_{REF} \le 1.0$ mA		0.01	0.1		0.01	0.15	%
	$V^+ - V_{REF} \ge 1.0V$ **(1.1V)**			**0.15**			**0.2**	%

Electrical Characteristics

$T_J = 25°C$, $\mathbf{T_{MIN} \leq T_J \leq T_{MAX}}$, (note 4) **(Boldface type refers to limits over temperature range)** (Continued)

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Amplifier gain	$0.2V \leq V_{REF} \leq 35V$	50 **23**	75		25 **15**	70		V/mV V/mV
Feedback sense voltage		195 **194**	200	205 **206**	190 **189**	200	210 **211**	mV mV
Feedback current			20	50 **65**		22	75 **90**	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			270	400 **500**		300	500 **570**	μA μA
Supply current change	1.2V (**1.3V**) $\leq V_S \leq$ 40V		15	**75**		15	**75**	μA

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0 **3.0**		0.5	4.0 **5.0**	mV mV
Input offset current (note 5)			0.1	0.7 **1.5**		0.2	2.0 **3.0**	nA nA
Input bias current			10	20 **30**		12	30 **40**	nA nA
Input resistance		250 **150**	500		150 **115**	400		kΩ kΩ
Large signal voltage gain	$V_S = \pm 3.25V$, $I_{OUT} = 0$ $V_{OUT} = \pm 3.2V$ $V_S = \pm 3.25V$, $I_{OUT} = 10$ mA $V_{OUT} = \pm 2.75$ V $V_S = \pm 0.6V$ (**0.65V**), $I_{OUT} = \pm 2$ mA $V_{OUT} = \pm 0.4V$ (**±0.3V**), $V_{CM} = -0.4V$	60 **40** 10 **4** 1.5 **0.5**	300 25 3.0		40 **25** 5 **3** 1.0 **0.75**	300 25 3.0		V/mV V/mV V/mV V/mV V/mV V/mV
Shunt gain (note 6)	$1.5V \leq V^+ \leq 6.5V$, $R_L = 500\Omega$ 0.1 mA $\leq I_{OUT} \leq 10$ mA	8 **4**	30		6 **4**	30		V/mV V/mV
Common-mode rejection	$-3.25V \leq V_{CM} \leq 2.4V$ (**2.25V**) $V_S = \pm 3.25V$	89 **83**	102		80 **74**	102		dB dB
Supply-voltage rejection	$-0.2V \geq V^- \geq -5.4V$ $V^+ = 1.0V$ (**1.2V**) 1.0V (**1.1V**) $\leq V^+ \leq 6.3V$ $V^- = 0.2V$	86 **80** 94 **88**	96 106		80 **74** 80 **74**	96 106		dB dB dB dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift			60			90		pA/°C
Line regulation	1.2V (**1.3V**) $\leq V_S \leq 6.5V$ $0 \leq I_{REF} \leq 0.5$ mA, $V_{REF} = 200$ mV		0.001	0.01 **0.02**		0.001	0.02 **0.03**	%/V %/V
Load regulation	$0 \leq I_{REF} \leq 0.5$ mA $V^+ - V_{REF} \geq 1.0V$ (**1.1V**)		0.01	0.1 **0.15**		0.01	0.15 **0.2**	% %
Amplifier gain	$0.2V \leq V_{REF} \leq 5.5V$	30 **20**	70		20 **15**	70		V/mV V/mV

Electrical Characteristics

$T_J = 25°C$, $\mathbf{T_{MIN} \leq T_J \leq T_{MAX}}$, (note 4) **(Boldface type refers to limits over temperature range)** (Continued)

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Feedback sense voltage		195 **194**	200	205 **206**	190 **189**	200	210 **211**	mV mV
Feedback current			20	50 **65**		22	75 **90**	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			260	400 **500**		280	500 **570**	μA μA

Note 1: The input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.

Note 2: The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.

Note 3: Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

Note 4: These specifications apply for $V^- \leq V_{CM} \leq V^+ - 0.85V$ **(1.0V)**, 1.2V **(1.3V)** $< V_S \leq V_{MAX}$, $V_{REF} = 0.2V$ and $0 \leq I_{REF} \leq 1.0$ mA, unless otherwise specified: $V_{MAX} = 40V$ for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation;** this is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \cong 20$ ms), die heating ($\tau_2 \cong 0.2$s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

Note 5: For $T_J > 90°C$, I_{OS} may exceed 1.5 nA for $V_{CM} = V^-$. With $T_J = 125°C$ and $V^- \leq V_{CM} \leq V^- + 0.1V$, $I_{OS} \leq 5$ nA.

Note 6: This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see typical applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Note 7: Refer to RETS10X for LM10H military specifications.

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the unloaded output is in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V^+ terminal of the IC. The load and power source are connected between the V^+ and V^- terminals, and input common-mode is referred to the V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^-, on the reference feedback terminal while operating in regulation.

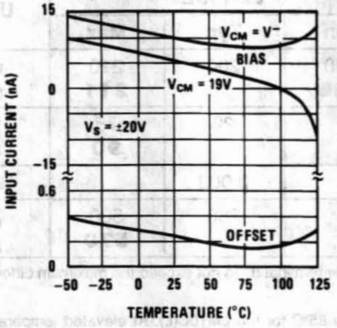
Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

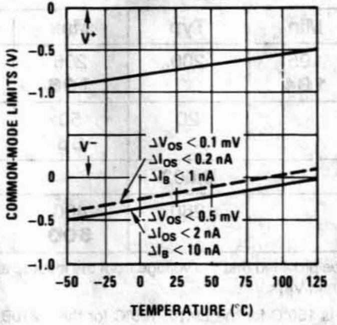
Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

Typical Performance Characteristics (Op Amp)

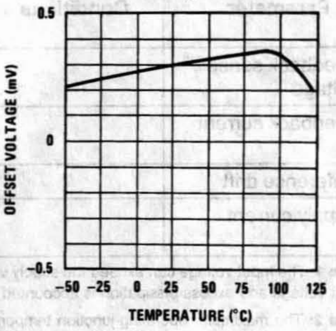
Input Current



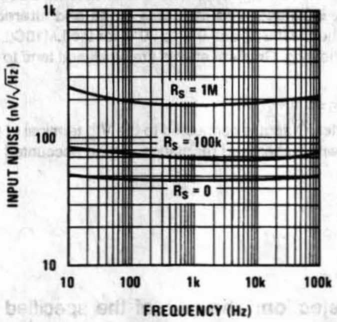
Common Mode Limits



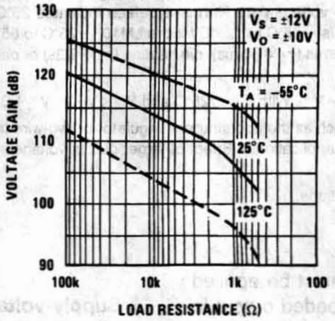
Offset Voltage Drift



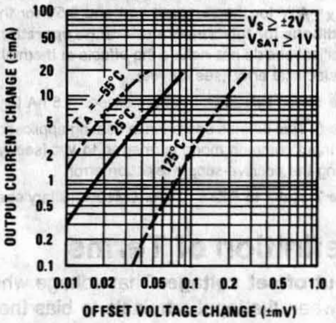
Input Noise Voltage



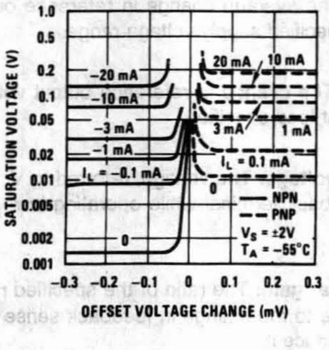
DC Voltage Gain



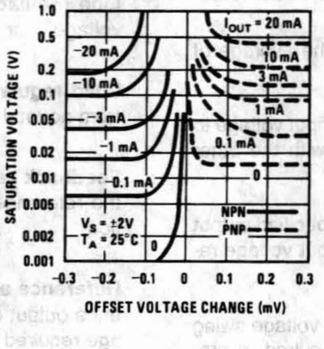
Transconductance



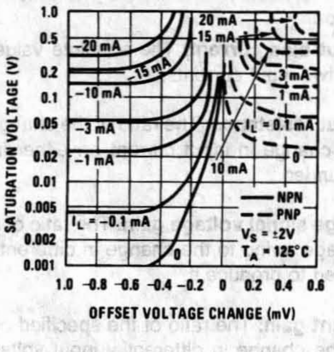
Output Saturation Characteristics



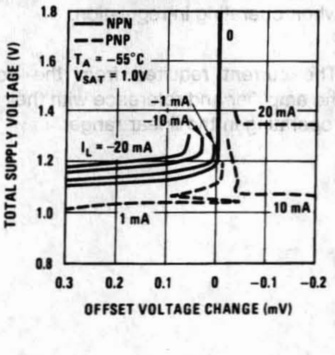
Output Saturation Characteristics



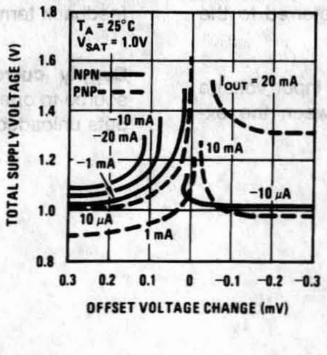
Output Saturation Characteristics



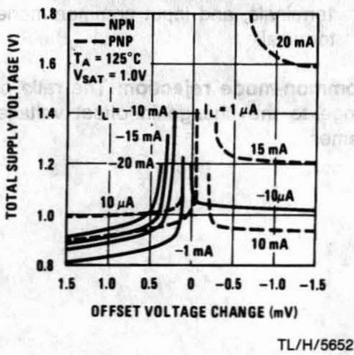
Minimum Supply Voltage



Minimum Supply Voltage



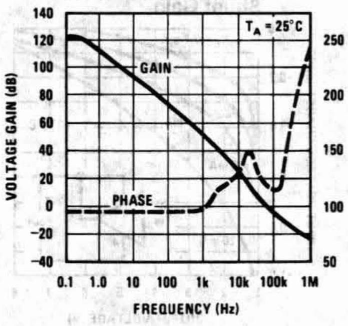
Minimum Supply Voltage



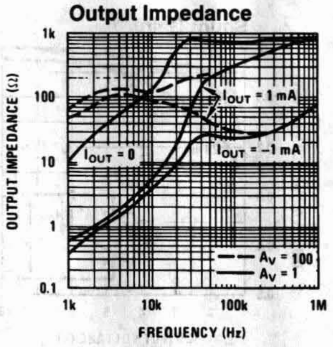
TL/H/5652–2

Typical Performance Characteristics (Op Amp) (Continued)

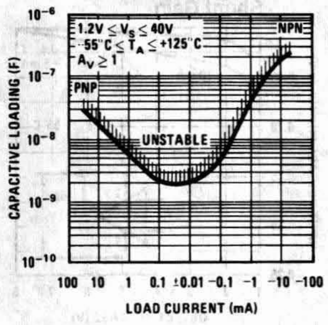
Frequency Response



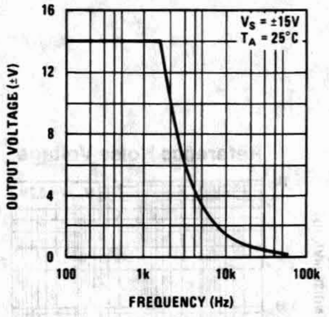
Output Impedance



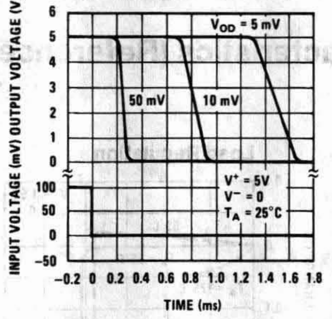
Typical Stability Range



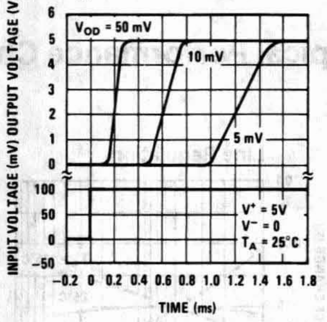
Large Signal Response



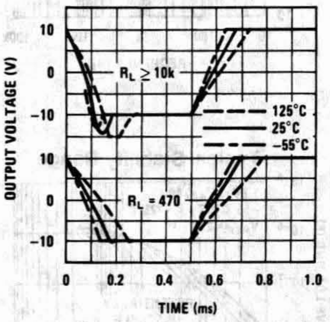
Comparator Response Time For Various Input Overdrives



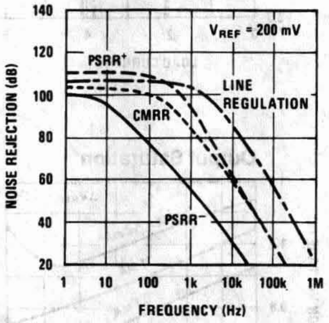
Comparator Response Time For Various Input Overdrives



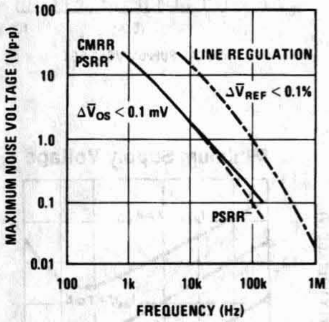
Follower Pulse Response



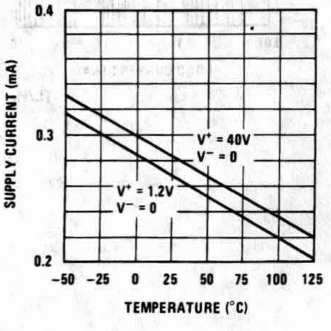
Noise Rejection



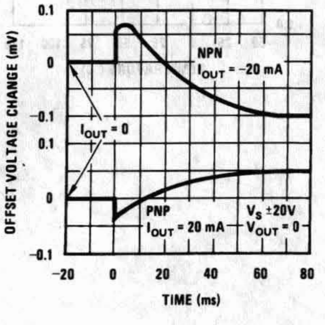
Rejection Slew Limiting



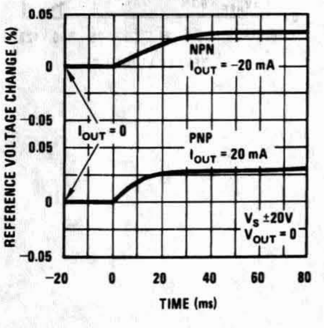
Supply Current



Thermal Gradient Feedback



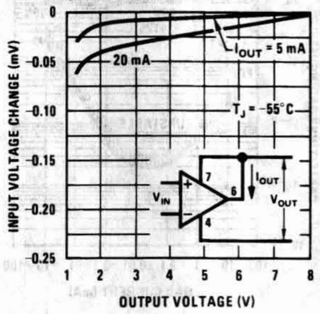
Thermal Gradient Cross-coupling



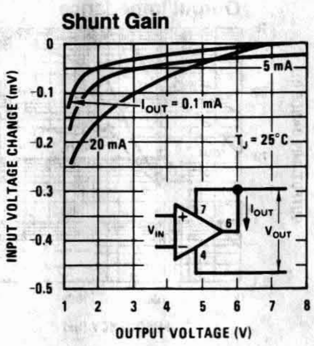
TL/H/5652–3

Typical Performance Characteristics (Op Amp) (Continued)

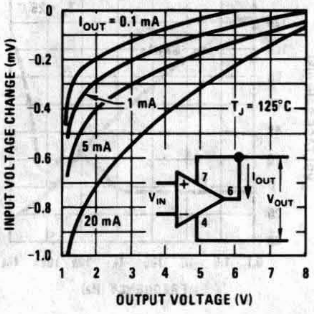
Shunt Gain



Shunt Gain



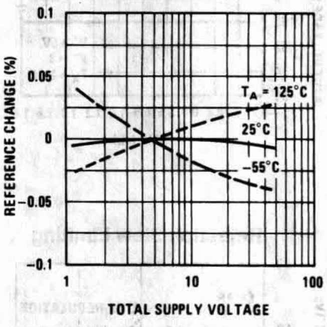
Shunt Gain



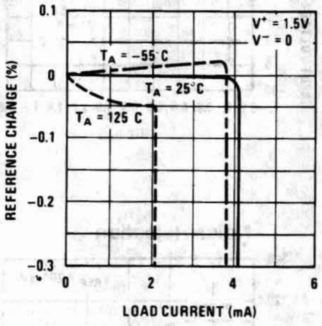
TL/H/5652-4

Typical Performance Characteristics (Reference)

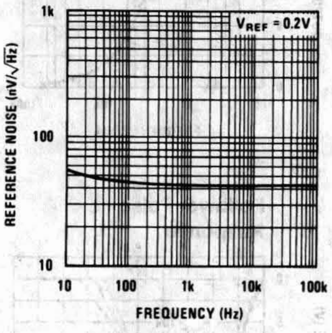
Line Regulation



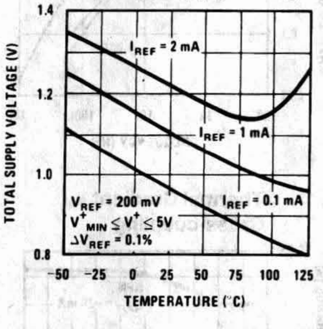
Load Regulation



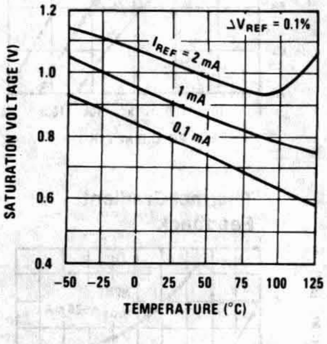
Reference Noise Voltage



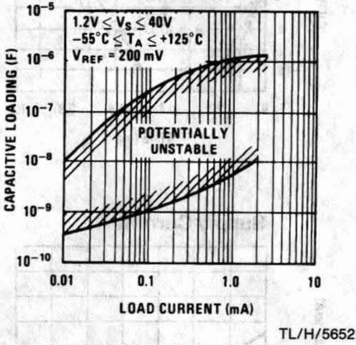
Minimum Supply Voltage



Output Saturation



Typical Stability Range

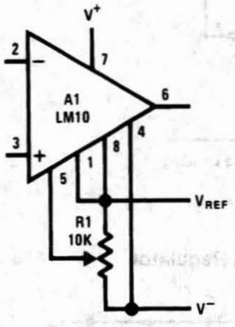


TL/H/5652-5

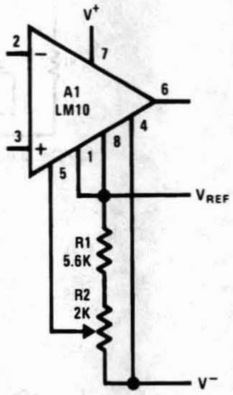
Typical Applications[††] (Pin numbers are for devices in 8-pin packages)

Op Amp Offset Adjustment

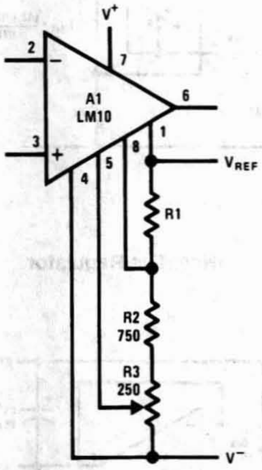
Standard


V+
2
7
A1
LM10
6
3
4
8
1
5
VREF
R1
10K
V−

Limited Range

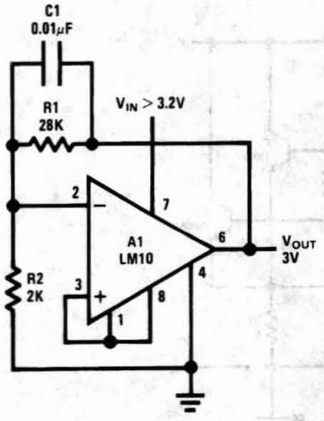

V+
2
7
A1
LM10
6
3
4
8
1
5
VREF
R1
5.6K
R2
2K
V−

Limited Range With Boosted Reference

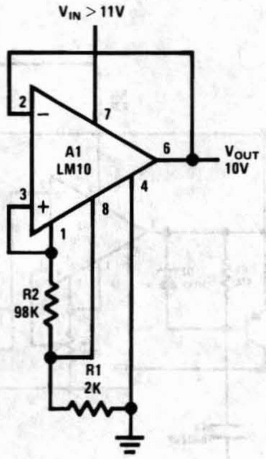

V+
2
7
A1
LM10
6
1
3
8
5
4
VREF
R1
R2
750
R3
250
V−

Positive Regulators[†]

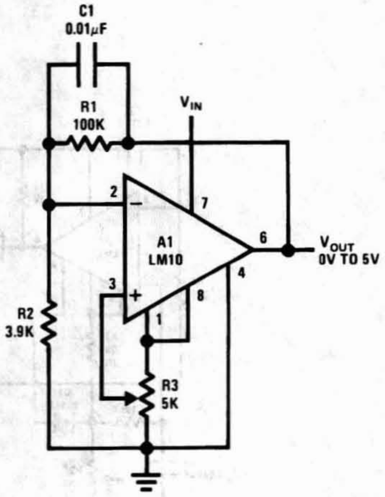
Low Voltage


C1
0.01μF
R1
28K
VIN > 3.2V
2
7
A1
LM10
6
VOUT
3V
R2
2K
3
4
8
1

Best Regulation


VIN > 11V
2
7
A1
LM10
6
VOUT
10V
4
3
8
1
R2
98K
R1
2K

Zero Output


C1
0.01μF
R1
100K
VIN
2
7
A1
LM10
6
VOUT
0V TO 5V
4
3
8
1
R2
3.9K
R3
5K

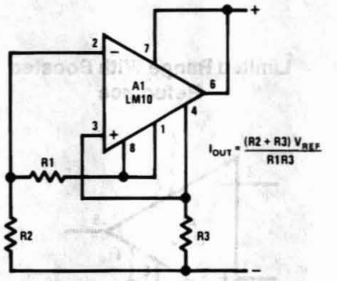
TL/H/5652–6

[†] Use only electrolytic output capacitors.

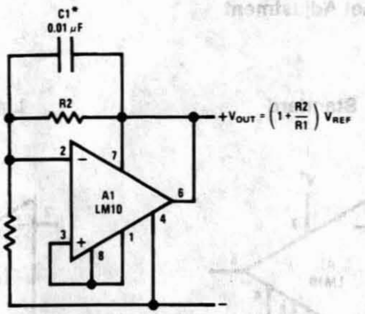
[††] Circuit descriptions available in application note AN-211.

Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

Current Regulator

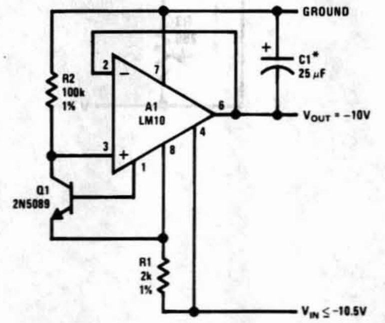

+
2
7
A1
LM10
6
4
3
1
8
R1
$I_{OUT} = \frac{(R2 + R3)\, V_{REF}}{R1R3}$
R2
R3
−

Shunt Regulator


C1*
0.01 μF
R2
$+V_{OUT} = \left(1 + \frac{R2}{R1}\right) V_{REF}$
2
7
A1
LM10
6
4
R1
3
1
8
−

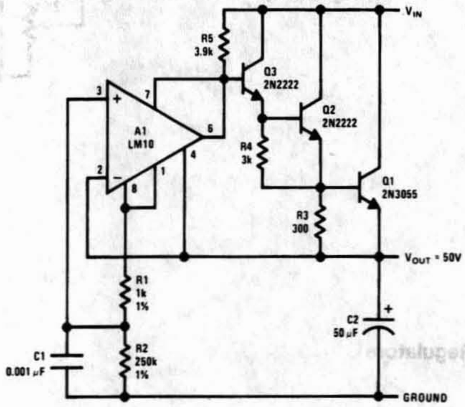
*Required For Capacitive Loading

Negative Regulator

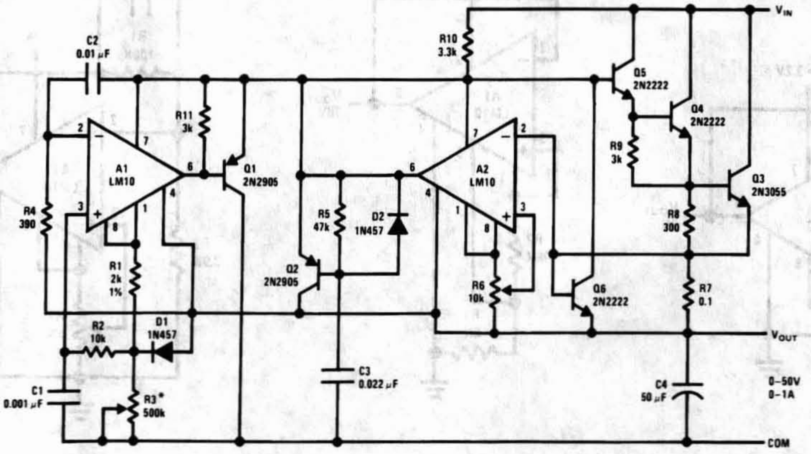

GROUND
C1*
25 μF
R2
100k
1%
2
7
A1
LM10
6
$V_{OUT} = -10V$
4
3
8
1
Q1
2N5089
R1
2k
1%
$V_{IN} \leq -10.5V$

*Electrolytic

Precision Regulator


V_{IN}
R5
3.9k
Q3
2N2222
Q2
2N2222
3
7
A1
LM10
6
4
R4
3k
2
1
8
Q1
2N3055
R3
300
$V_{OUT} = 50V$
R1
1k
1%
C2
50 μF
C1
0.001 μF
R2
250k
1%
GROUND

Laboratory Power Supply


V_{IN}
R10
3.3k
C2
0.01 μF
Q5
2N2222
R11
3k
Q4
2N2222
2
7
A1
LM10
6
Q1
2N2905
6
A2
LM10
7
2
R9
3k
Q3
2N3055
R4
390
3
4
1
8
R5
47k
D2
1N457
4
1
3
8
R8
300
R1
2k
1%
Q2
2N2905
R6
10k
Q6
2N2222
R7
0.1
R2
10k
D1
1N457
V_{OUT}
C3
0.022 μF
C1
0.001 μF
R3*
500k
C4
50 μF
0–50V
0–1A
COM

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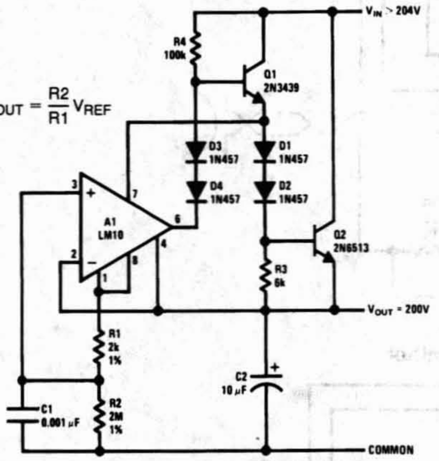
*$V_{OUT} = 10^{-4}$ R3

††Circuit descriptions available in application note AN-211.

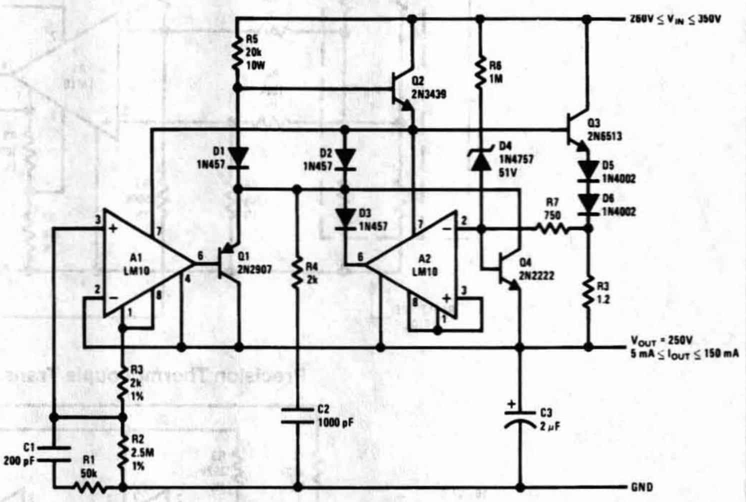
Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

HV Regulator

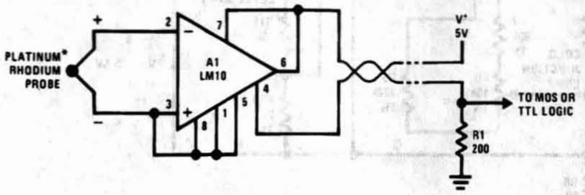
$$V_{OUT} = \frac{R2}{R1} V_{REF}$$


VIN > 204V
R4
100k
Q1
2N3439
D3
1N457
D1
1N457
D4
1N457
D2
1N457
3
+
7
6
A1
LM10
4
2
−
8
1
Q2
2N6513
R3
6k
VOUT = 200V
R1
2k
1%
C2
10 µF
+
C1
0.001 µF
R2
2M
1%
COMMON

Protected HV Regulator

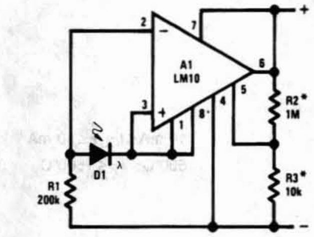

260V ≤ VIN ≤ 350V
R5
20k
10W
Q2
2N3439
R6
1M
Q3
2N6513
D1
1N457
D2
1N457
D4
1N4757
51V
D5
1N4002
D6
1N4002
R7
750
D3
1N457
3
+
7
A1
LM10
6
4
2
−
8
1
Q1
2N2907
R4
2k
6
A2
LM10
7
2
−
+
3
8
1
Q4
2N2222
R3
1.2
VOUT = 250V
5 mA ≤ IOUT ≤ 150 mA
R3
2k
1%
R2
2.5M
1%
C1
200 pF
R1
50k
C2
1000 pF
C3
2 µF
+
GND

Flame Detector


+
PLATINUM*
RHODIUM
PROBE
−
2
−
3
+
7
A1
LM10
6
4
8
1
5
V+
5V
TO MOS OR
TTL LOGIC
R1
200

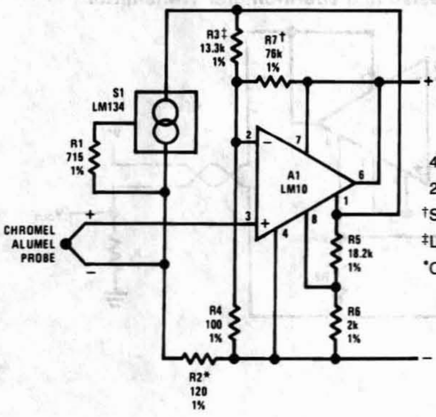
*800°C Threshold Is Established By Connecting Balance To V_{REF}.

Light Level Sensor


+
2
−
7
A1
LM10
6
3
+
1
8
4
5
R2*
1M
R3*
10k
D1
λ
R1
200k
−

*Provides Hysteresis

Remote Thermocouple Amplifier


R3‡
13.3k
1%
R7†
76k
1%
+
S1
LM134
R1
715
1%
2
−
7
A1
LM10
6
1
3
+
4
8
CHROMEL
ALUMEL
PROBE
+
−
R5
18.2k
1%
R4
100
1%
R6
2k
1%
R2*
120
1%
−

4V ≤ V_{OUT} ≤ 20V

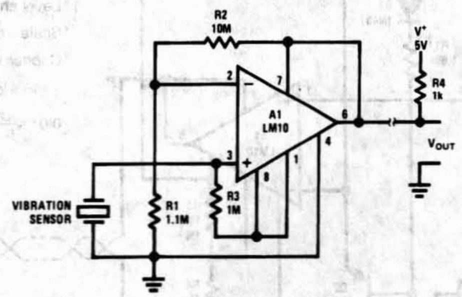
200°C ≤ T_P ≤ 700°C

†Span Trim

‡Level-shift Trim

*Cold-junction Trim

Remote Amplifier


R2
10M
2
−
7
A1
LM10
6
4
3
+
8
1
V+
5V
R4
1k
VOUT
VIBRATION
SENSOR
R1
1.1M
R3
1M

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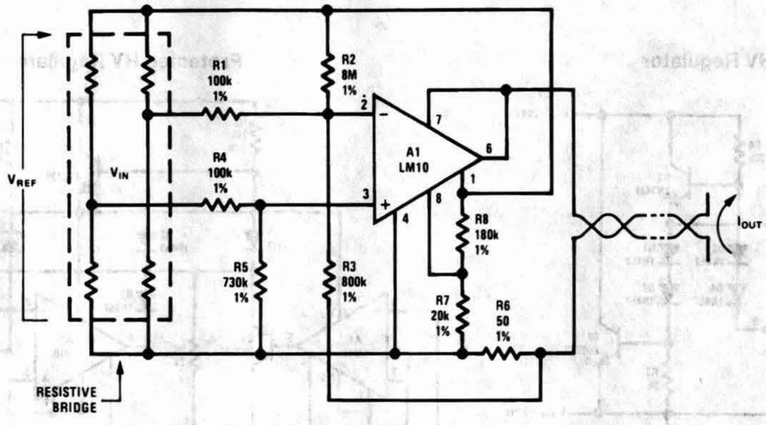
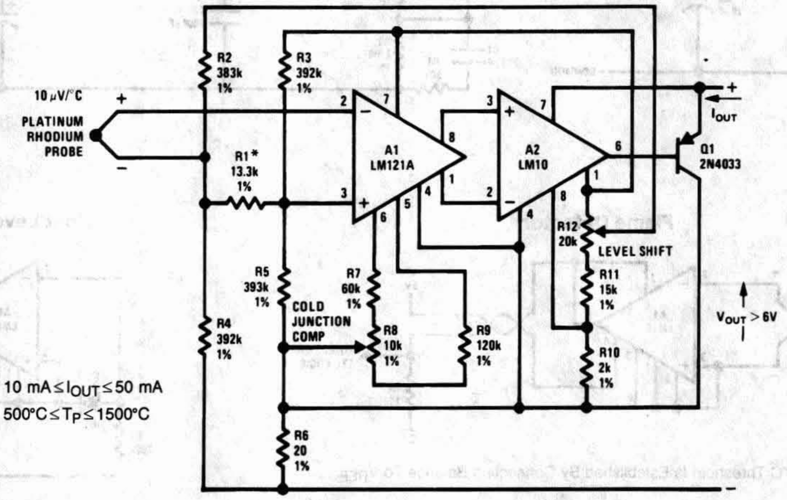
††Circuit descriptions available in application note AN-211.

Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

Transmitter for Bridge Sensor


R1
100k
1%
R2
8M
1%
R4
100k
1%
A1
LM10
V_{REF}
V_{IN}
R5
730k
1%
R3
800k
1%
R8
180k
1%
R7
20k
1%
R6
50
1%
I_{OUT}
RESISTIVE
BRIDGE
2
3
4
6
7
8
1

Precision Thermocouple Transmitter

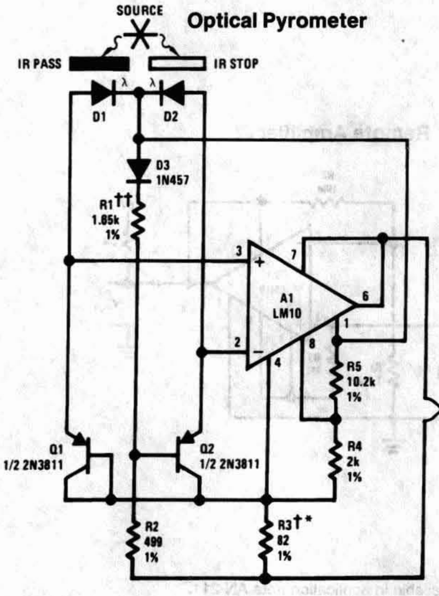

10 μV/°C
+
PLATINUM
RHODIUM
PROBE
−
R2
383k
1%
R3
392k
1%
R1*
13.3k
1%
A1
LM121A
A2
LM10
Q1
2N4033
I_{OUT}
+
−
R12
20k
LEVEL SHIFT
R11
15k
1%
R10
2k
1%
R5
393k
1%
COLD
JUNCTION
COMP
R7
60k
1%
R8
10k
1%
R9
120k
1%
R4
392k
1%
R6
20
1%
V_{OUT} > 6V

10 mA ≤ I_{OUT} ≤ 50 mA

500°C ≤ T_P ≤ 1500°C

*Gain Trim

Optical Pyrometer


SOURCE
IR PASS
IR STOP
λ
λ
D1
D2
D3
1N457
R1††
1.05k
1%
A1
LM10
R5
10.2k
1%
R4
2k
1%
Q1
1/2 2N3811
Q2
1/2 2N3811
R2
499
1%
R3†*
82
1%
I_{OUT}
2
3
4
6
7
8
1

††Level-shift Trim

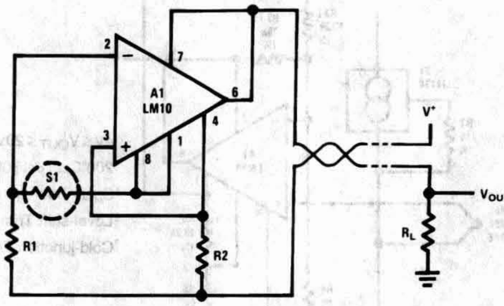
*Scale Factor Trim

†Copper Wire Wound

1 mA ≤ I_{OUT} ≤ 5 mA

$0.01 \le \frac{I_{D2}}{I_{D1}} \le 100$

Resistance Thermometer Transmitter

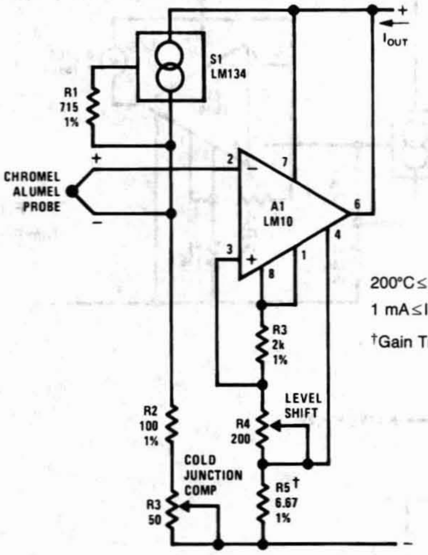

A1
LM10
S1
R1
R2
V+
V_{OUT}
R_L
2
3
4
6
7
8
1

††Circuit descriptions available in application note AN-211.

TL/H/5652–9

Typical Applications[††] (Pin numbers are for devices in 8-pin packages) (Continued)

Thermocouple Transmitter

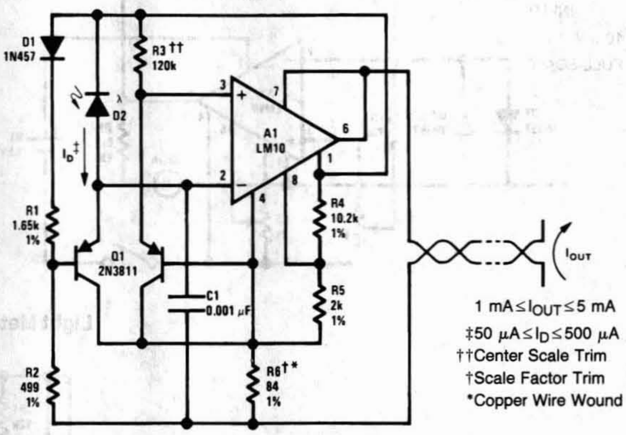

+
I_{OUT}
S1
LM134
R1
715
1%
CHROMEL
ALUMEL
PROBE
+
−
2
7
A1
LM10
6
4
3
8
1
R3
2k
1%
LEVEL
SHIFT
R4
200
R2
100
1%
COLD
JUNCTION
COMP
R3
50
R5†
6.67
1%
−

200°C ≤ T_P ≤ 700°C

1 mA ≤ I_{OUT} ≤ 5 mA

†Gain Trim

Logarithmic Light Sensor


D1
1N457
R3 ††
120k
λ
D2
I_D‡
3
7
A1
LM10
6
1
2
8
4
R4
10.2k
1%
R1
1.65k
1%
Q1
2N3811
C1
0.001 μF
R5
2k
1%
R2
499
1%
R6†*
84
1%
I_{OUT}

1 mA ≤ I_{OUT} ≤ 5 mA

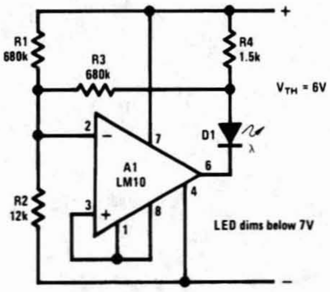
‡50 μA ≤ I_D ≤ 500 μA

††Center Scale Trim

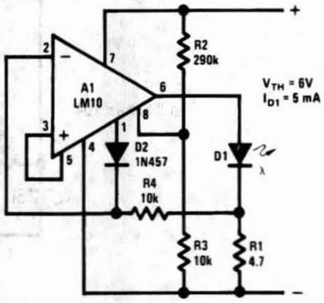
†Scale Factor Trim

*Copper Wire Wound

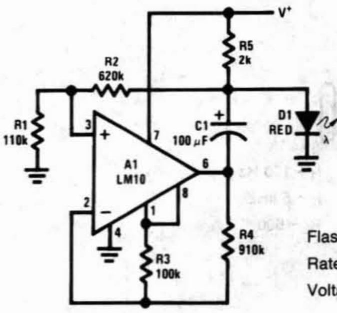
Battery-level Indicator


+
R1
680k
R3
680k
R4
1.5k
V_{TH} = 6V
2
7
D1
λ
A1
LM10
6
4
R2
12k
3
8
1
LED dims below 7V
−

Battery-threshold Indicator

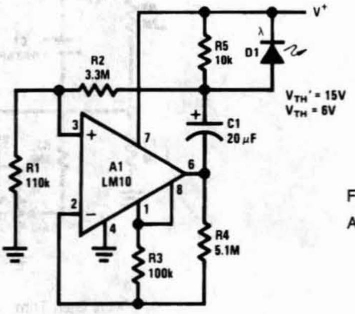

+
R2
290k
2
7
A1
LM10
6
V_{TH} = 6V
I_{D1} = 5 mA
8
3
1
4
5
D2
1N457
D1
λ
R4
10k
R3
10k
R1
4.7
−

Single-cell Voltage Monitor


V⁺
R5
2k
R2
620k
R1
110k
3
7
C1
100 μF
D1
RED
λ
A1
LM10
6
2
8
1
4
R4
910k
R3
100k

Flashes Above 1.2V Rate Increases With Voltage

Double-ended Voltage Monitor


V⁺
λ
R5
10k
D1
R2
3.3M
V_{TH}' = 15V
V_{TH} = 6V
3
7
C1
20 μF
R1
110k
A1
LM10
6
2
8
1
4
R4
5.1M
R3
100k

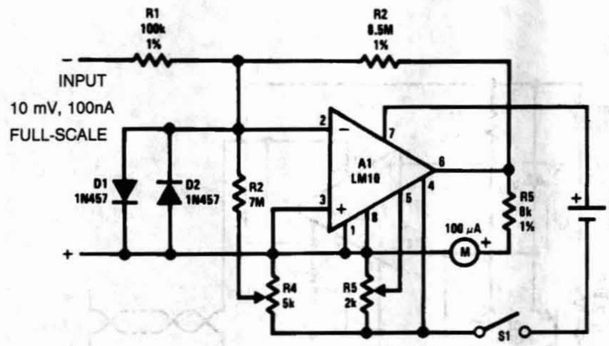
Flash Rate Increases Above 6V and Below 15V

TL/H/5652–10

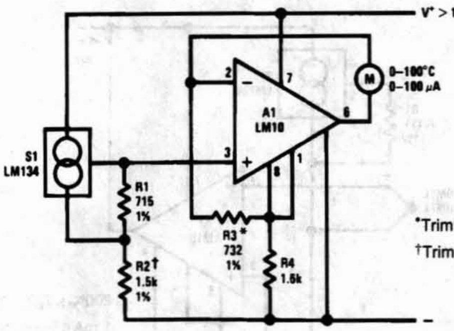
[††] Circuit descriptions available in application note AN-211.

Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

Meter Amplifier


R1
100k
1%
R2
8.5M
1%
–
INPUT
10 mV, 100nA
FULL-SCALE
D1
1N457
D2
1N457
R2
7M
2
3
7
6
5
4
1
8
A1
LM10
R5
8k
1%
B1
1.5V
100 μA
M
+
R4
5k
R5
2k
S1

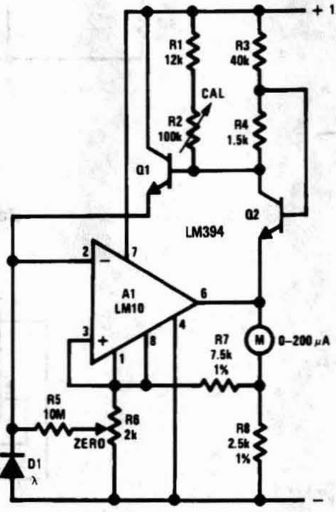
Thermometer


V⁺ > 1V
S1
LM134
2
3
7
6
8
1
A1
LM10
M
0–100°C
0–100 μA
R1
715
1%
R2†
1.5k
1%
R3*
732
1%
R4
1.6k
–

*Trim For Span

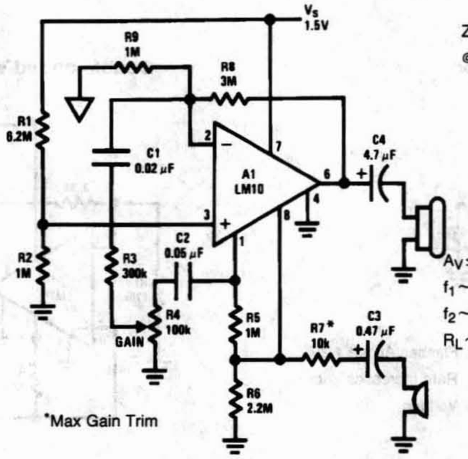
†Trim For Zero

Light Meter


+ 1.1V ≤ V⁺ ≤ 2V
R1
12k
R3
40k
CAL
R2
100k
R4
1.5k
Q1
Q2
LM394
2
7
3
6
4
8
1
A1
LM10
M
0–200 μA
R7
7.5k
1%
R5
10M
R6
2k
ZERO
R8
2.5k
1%
D1
λ
–

$1 \leq \lambda/\lambda_0 \leq 10^5$

Microphone Amplifier


V_S
1.5V
R9
1M
R8
3M
R1
6.2M
C1
0.02 μF
2
3
7
6
4
8
1
A1
LM10
C4
4.7 μF
R2
1M
R3
300k
C2
0.05 μF
R4
100k
GAIN
R5
1M
R7*
10k
C3
0.47 μF
R6
2.2M

$Z_{OUT} \sim 680\Omega$
@ 5 kHz

$A_V \leq 1k$
$f_1 \sim 100$ Hz
$f_2 \sim 5$ kHz
$R_L \sim 500$

*Max Gain Trim

TL/H/5652–11

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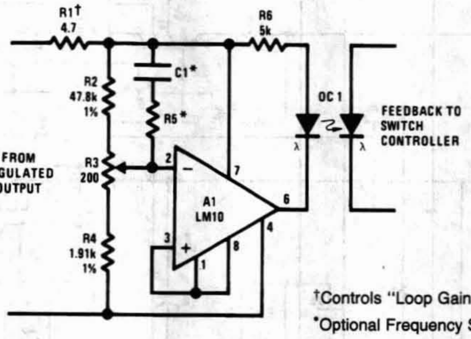
††Circuit descriptions available in application note AN-211.

Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

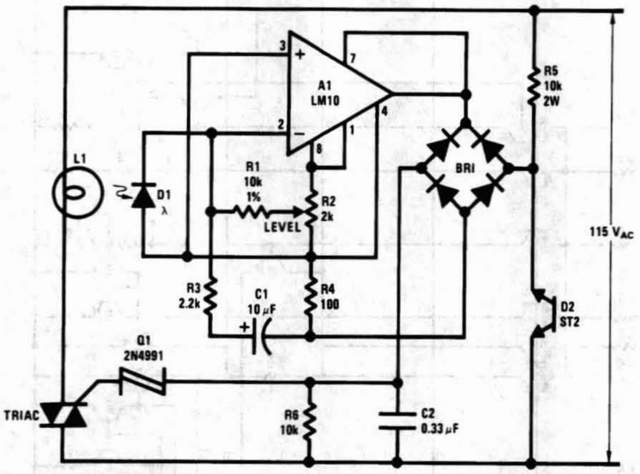
Isolated Voltage Sensor


R1†
4.7
R6
5k
C1*
R2
47.8k
1%
R5*
OC 1
FEEDBACK TO
SWITCH
CONTROLLER
λ
λ
FROM
REGULATED
OUTPUT
R3
200
2
7
A1
LM10
6
3
8
4
1
R4
1.91k
1%

†Controls "Loop Gain"

*Optional Frequency Shaping

Light-level Controller


3
7
A1
LM10
4
2
8
1
R5
10k
2W
L1
D1
λ
R1
10k
1%
R2
2k
LEVEL
BRI
115 V_{AC}
R3
2.2k
C1
10 μF
R4
100
D2
ST2
Q1
2N4991
TRIAC
R6
10k
C2
0.33 μF

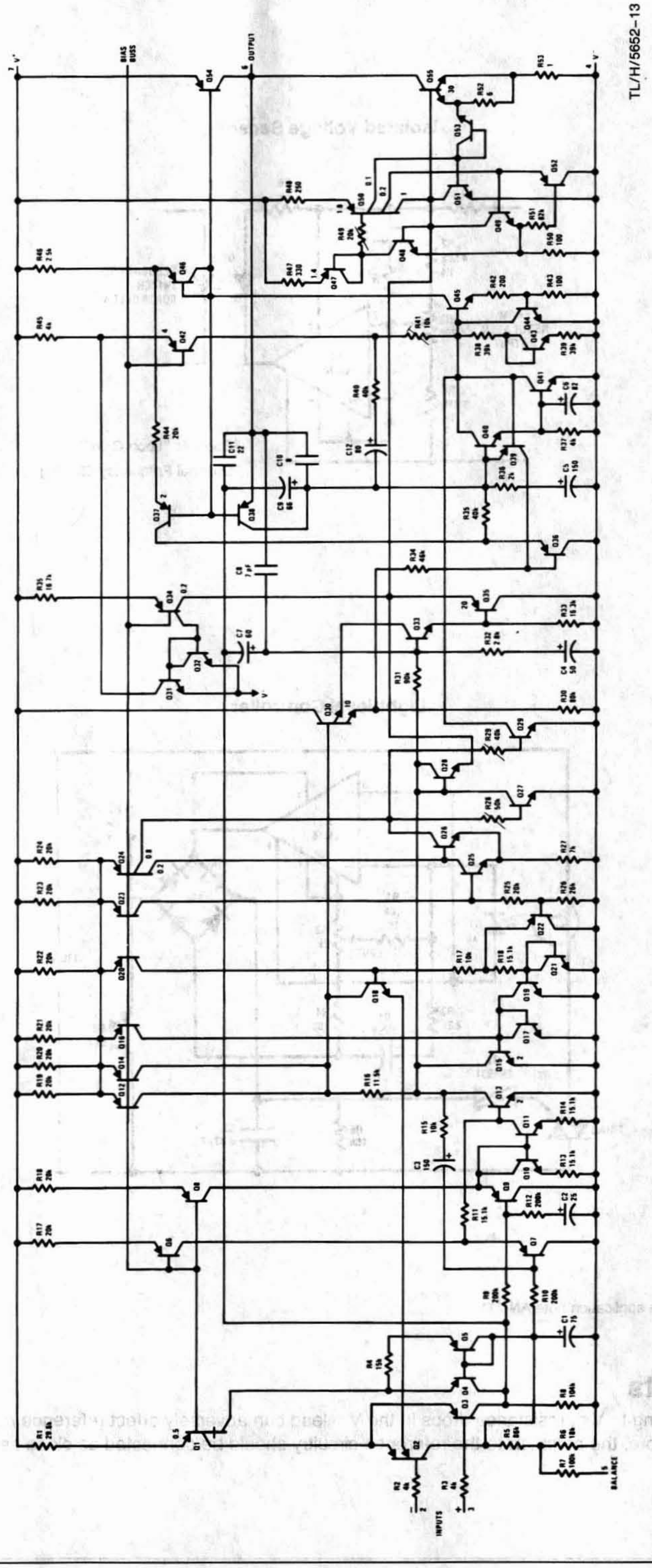
TL/H/5652–12

††Circuit descriptions available in application note AN-211.

Application Hints

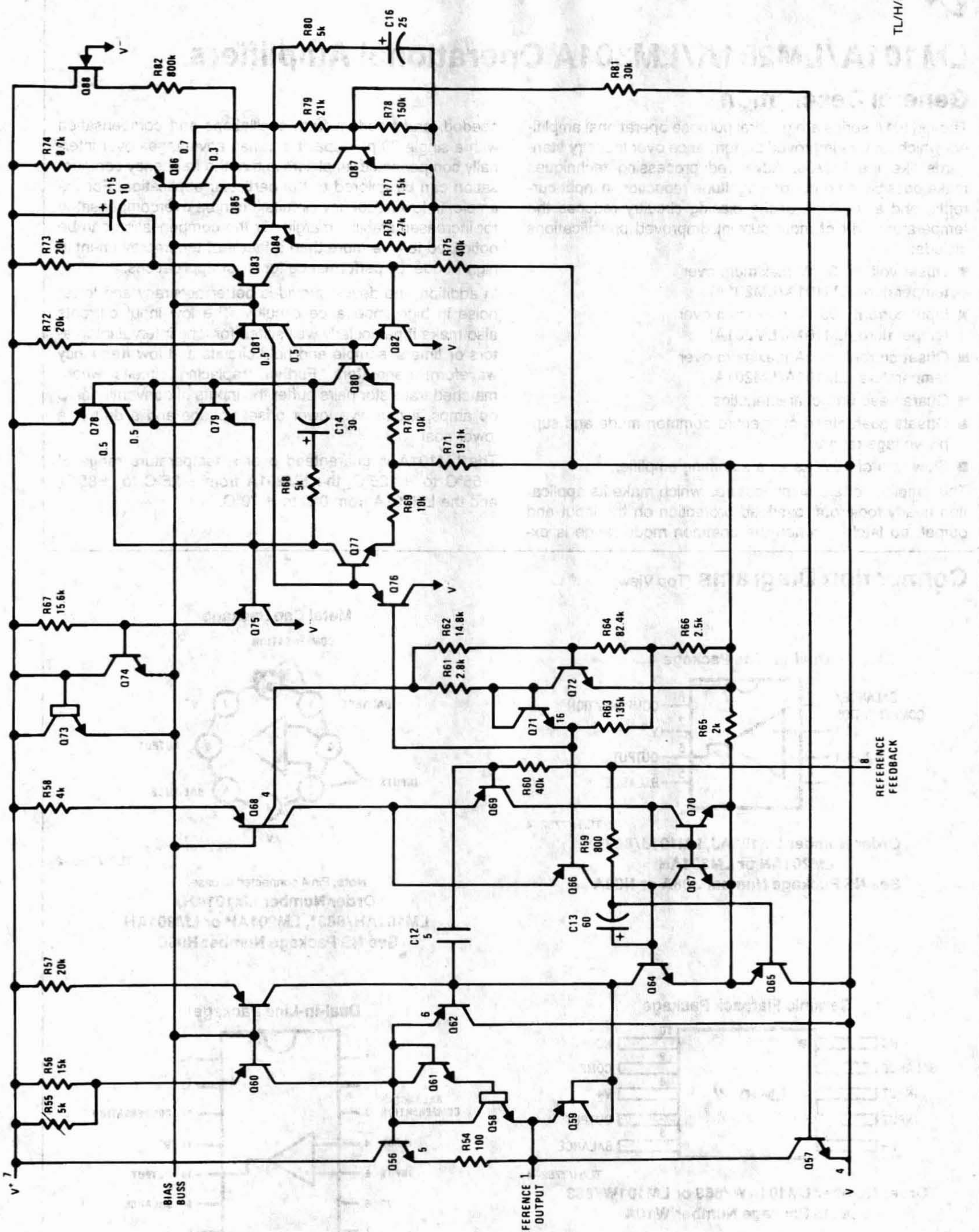
With heavy amplifier loading to V^-, resistance drops in the V^- lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

Operational Amplifier Schematic (Pin numbers are for 8-pin packages)


7 V+
BIAS BUSS
6 OUTPUT
4 V−
INPUTS
2
3
5 BALANCE

TL/H/5652-13

Reference and Internal Regulator (Pin numbers are for 8-pin packages)


R80 5k
C16 25
R82 800k
Q88
V−
R79 21k
R78 150k
R81 30k
R74 8.7k
Q86
0.7
Q87
0.3
C15 10
Q85
R77 1.5k
R73 20k
Q84
R76 2.7k
Q83
R75 40k
R72 20k
Q81
0.5
0.5
Q82
V−
Q80
Q78
0.5
0.5
Q79
C14 30
R70 10k
R71 19.1k
R68 5k
R69 10k
Q77
Q76
V−
R67 15.6k
Q75
V−
R62 14.8k
R64 82.4k
R66 2.5k
Q74
R61 2.8k
Q72
Q73
Q71
16
R63 135k
R65 2k
R58 4k
Q68
4
Q69
R60 40k
8
REFERENCE FEEDBACK
Q70
R59 800
Q66
Q67
C13 60
C12 5
R57 20k
Q64
Q65
6
Q62
R56 15k
Q60
Q61
R55 5k
Q58
Q59
R54 100
Q56
5
Q57
4
V−
V+ 7
BIAS BUSS
REFERENCE OUTPUT 1

TL/H/5652-14

National Semiconductor

LM101A/LM201A/LM301A Operational Amplifiers

General Description

The LM101A series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

- Offset voltage 3 mV maximum over temperature (LM101A/LM201A)
- Input current 100 nA maximum over temperature (LM101A/LM201A)
- Offset current 20 nA maximum over temperature (LM101A/LM201A)
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

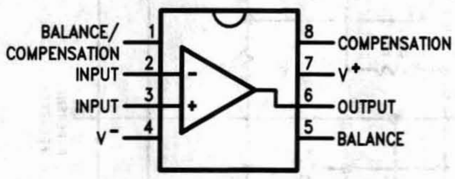
This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.

The LM101A is guaranteed over a temperature range of −55°C to +125°C, the LM201A from −25°C to +85°C, and the LM301A from 0°C to +70°C.

Connection Diagrams (Top View)

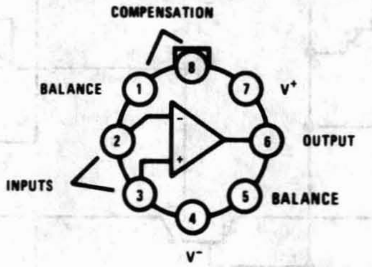
Dual-In-Line Package


BALANCE/ COMPENSATION
INPUT
INPUT
V−
1
2
3
4
8
7
6
5
COMPENSATION
V+
OUTPUT
BALANCE
−
+

TL/H/7752-4

Order Number LM101AJ, LM101J/883*, LM201AN or LM301AN
See NS Package Number J08A or N08A

Metal Can Package

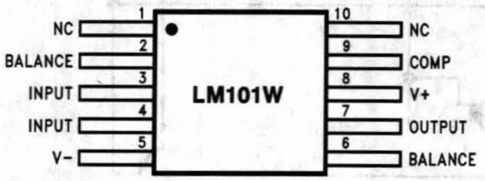

COMPENSATION
BALANCE
V+
OUTPUT
INPUTS
BALANCE
V−
1
2
3
4
5
6
7
8
−
+

TL/H/7752-2

Note: Pin 4 connected to case.

Order Number LM101AH, LM101AH/883*, LM201AH or LM301AH
See NS Package Number H08C

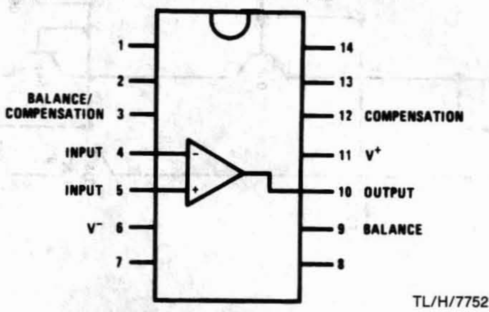
Ceramic Flatpack Package


NC
BALANCE
INPUT
INPUT
V−
1
2
3
4
5
10
9
8
7
6
NC
COMP
V+
OUTPUT
BALANCE
LM101W

TL/H/7752-4

Order Number LM101AW/883 or LM101W/883
See NS Package Number W10A

Dual-In-Line Package


1
2
BALANCE/ COMPENSATION 3
INPUT 4
INPUT 5
V− 6
7
14
13
12 COMPENSATION
11 V+
10 OUTPUT
9 BALANCE
8
−
+

TL/H/7752-3

Order Number LM101AJ-14/883*
See NS Package Number J14A

*Available per JM38510/10103.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LM101A/LM201A	LM301A
Supply Voltage	±22V	±18V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
Operating Ambient Temp. Range	−55°C to +125°C (LM101A) −25°C to +85°C (LM201A)	0°C to +70°C
T_J Max		
H-Package	150°C	100°C
N-Package	150°C	100°C
J-Package	150°C	100°C
Power Dissipation at $T_A = 25°C$		
H-Package (Still Air)	500 mW	300 mW
(400 LF/Min Air Flow)	1200 mW	700 mW
N-Package	900 mW	500 mW
J-Package	1000 mW	650 mW
Thermal Resistance (Typical) θ_{jA}		
H-Package (Still Air)	165°C/W	165°C/W
(400 LF/Min Air Flow)	67°C/W	67°C/W
N Package	135°C/W	135°C/W
J-Package	110°C/W	110°CmW
(Typical) θ_{jC}		
H-Package	25°C/W	25°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		
Metal Can or Ceramic	300°C	300°C
Plastic	260°C	260°C
ESD Tolerance (Note 5)	2000V	2000V

Electrical Characteristics (Note 3) $T_A = T_J$

Parameter	Conditions		LM101A/LM201A			LM301A			Units
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\ k\Omega$			0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$			1.5	10		3.0	50	nA
Input Bias Current	$T_A = 25°C$			30	75		70	250	nA
Input Resistance	$T_A = 25°C$		1.5	4.0		0.5	2.0		MΩ
Supply Current	$T_A = 25°C$	$V_S = \pm 20V$		1.8	3.0				mA
		$V_S = \pm 15V$					1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$		50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50\ k\Omega$				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0	15		6.0	30	μV/°C
Input Offset Current					20			70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{MAX}$			0.01	0.1		0.01	0.3	nA/°C
	$T_{MIN} \leq T_A \leq 25°C$			0.02	0.2		0.02	0.6	nA/°C

Electrical Characteristics (Note 3) $T_A = T_J$ (Continued)

Parameter	Conditions		LM101A/LM201A			LM301A			Units
			Min	Typ	Max	Min	Typ	Max	
Input Bias Current					0.1			0.3	μA
Supply Current	$T_A = T_{MAX}$, $V_S = \pm 20V$			1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k$		25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$	$R_L = 10\ k\Omega$	±12	±14		±12	±14		V
		$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 20V$		±15						V
	$V_S = \pm 15V$			+15, −13		±12	+15, −13		V
Common-Mode Rejection Ratio	$R_S \leq 50\ k\Omega$		80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		80	96		70	96		dB

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 75°C for LM101A/LM201A, and 70°C and 55°C respectively for LM301A.

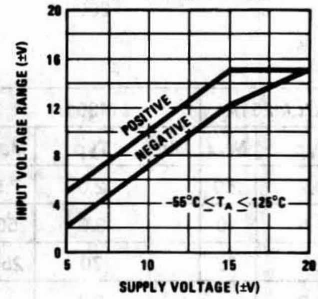
Note 3: Unless otherwise specified, these specifications apply for C1 = 30 pF, $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM101A), $\pm 5V \leq V_S \leq \pm 20V$ and $-25°C \leq T_A \leq +85°C$ (LM201A), $\pm 5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq +70°C$ (LM301A).

Note 4: Refer to RETS101AX for LM101A military specifications and RETS101X for LM101 military specifications.

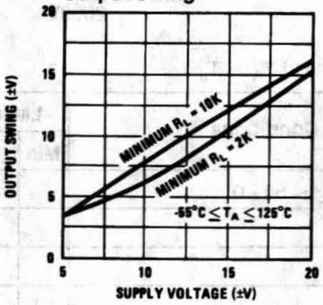
Note 5: Human body model, 100 pF discharged through 1.5 kΩ.

Guaranteed Performance Characteristics LM101A/LM201A

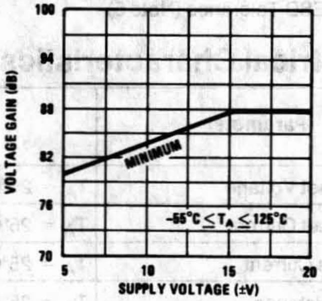
Input Voltage Range



Output Swing



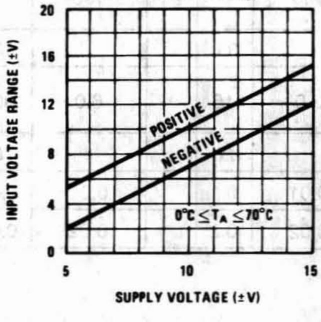
Voltage Gain



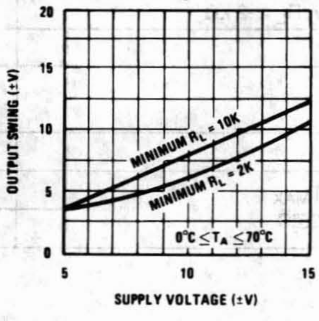
TL/H/7752–5

Guaranteed Performance Characteristics LM301A

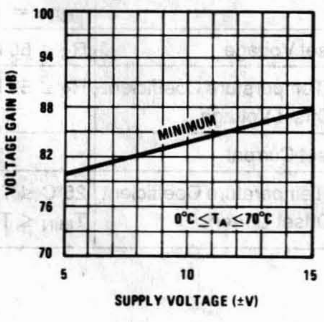
Input Voltage Range



Output Swing

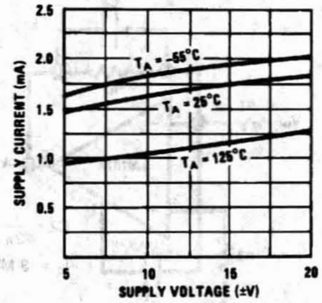


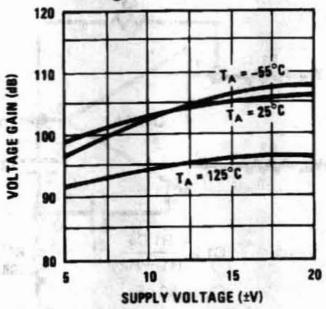
Voltage Gain

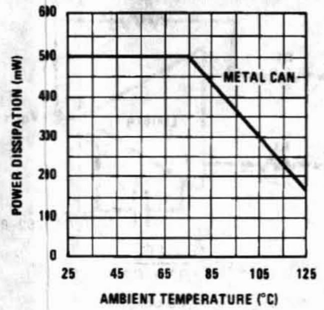


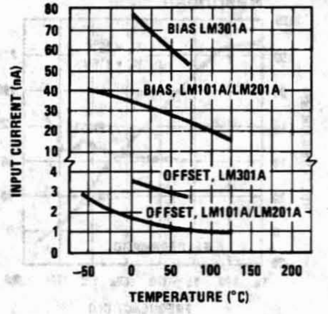
TL/H/7752–6

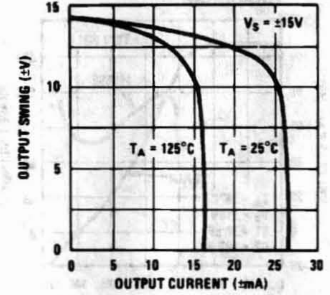
Typical Performance Characteristics

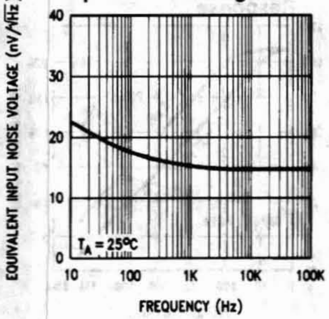

Supply Current

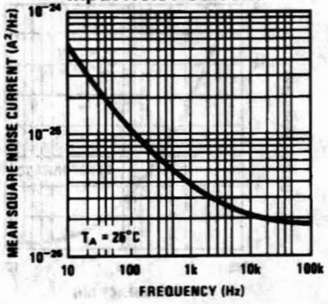

Voltage Gain

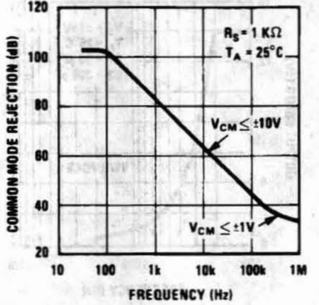

Maximum Power Dissipation

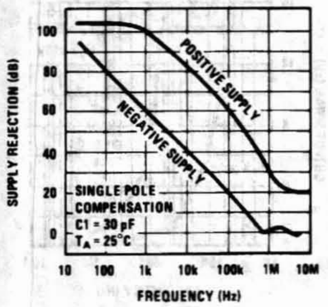

Input Current, LM101A/LM201A/LM301A

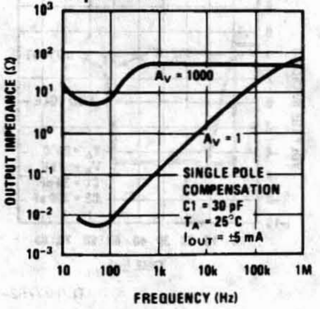

Current Limiting


Input Noise Voltage


Input Noise Current


Common Mode Rejection

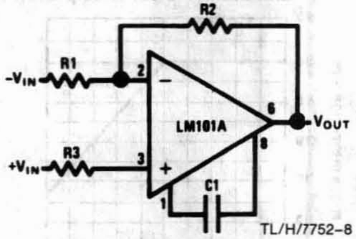

Power Supply Rejection


Closed Loop Output Impedance

TL/H/7752–7

Typical Performance Characteristics for Various Compensation Circuits**

Single Pole Compensation

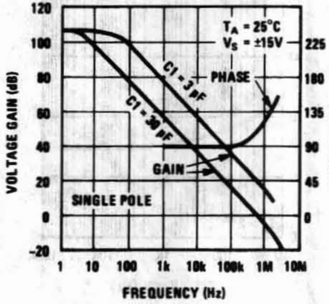

R2
R1
$-V_{IN}$
2
LM101A
6
V_{OUT}
8
R3
$+V_{IN}$
3
1
C1

TL/H/7752-8

$$C1 \geq \frac{R1\,C_S}{R1 + R2}$$

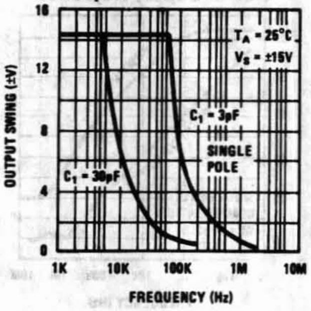
C_S = 30 pF

Open Loop Frequency Response



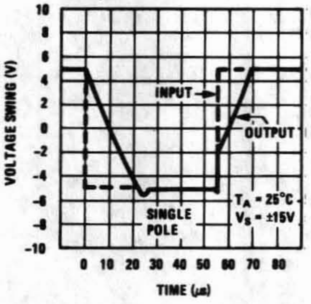
TL/H/7752-9

Large Signal Frequency Response



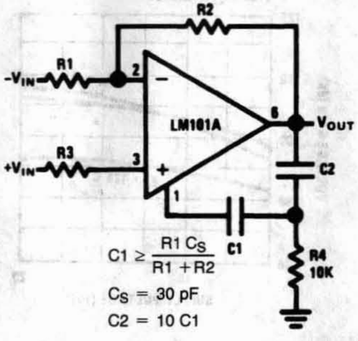
TL/H/7752-10

Voltage Follower Pulse Response



TL/H/7752-11

Two Pole Compensation


R2
R1
$-V_{IN}$
2
LM101A
6
V_{OUT}
R3
$+V_{IN}$
3
1
C1
C2
R4
10K

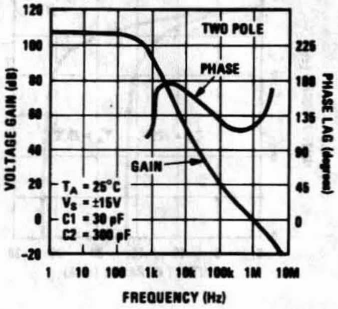
$$C1 \geq \frac{R1\,C_S}{R1 + R2}$$

C_S = 30 pF

C2 = 10 C1

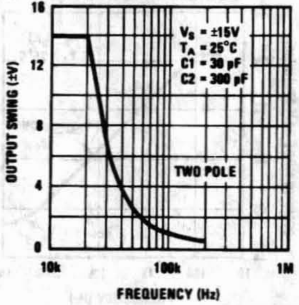
TL/H/7752-12

Open Loop Frequency Response



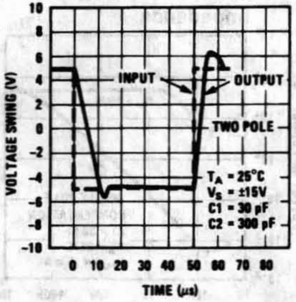
TL/H/7752-13

Large Signal Frequency Response



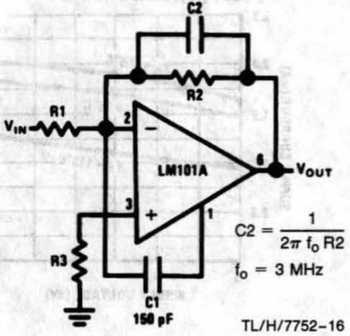
TL/H/7752-14

Voltage Follower Pulse Response



TL/H/7752-15

Feedforward Compensation

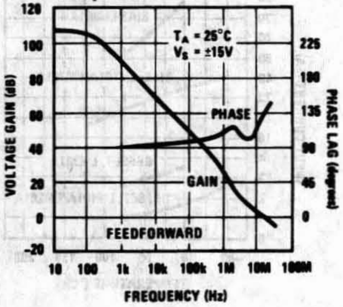

C2
R2
R1
V_{IN}
2
LM101A
6
V_{OUT}
3
1
R3
C1
150 pF

$$C2 = \frac{1}{2\pi\, f_o\, R2}$$

f_o = 3 MHz

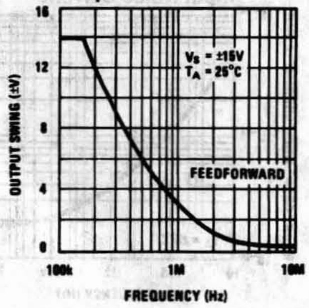
TL/H/7752-16

Open Loop Frequency Response



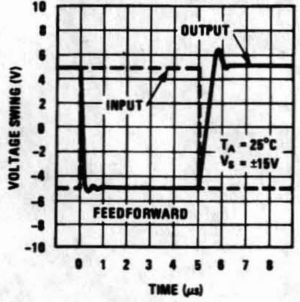
TL/H/7752-17

Large Signal Frequency Response



TL/H/7752-18

Inverter Pulse Response



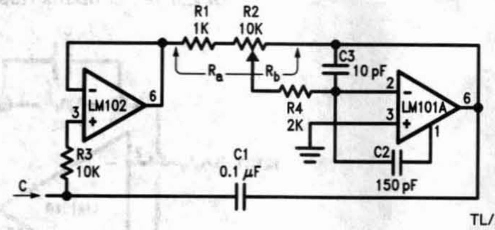
TL/H/7752-19

**Pin connections shown are for 8-pin packages.

Typical Applications**

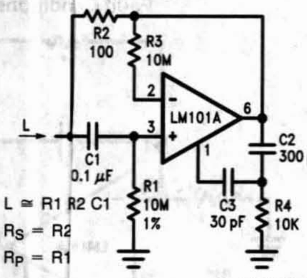
Variable Capacitance Multiplier

$C = 1 + \frac{R_b}{R_a} C1$


R1
1K
R2
10K
C3
10 pF
R_a
R_b
R4
2K
LM102
LM101A
R3
10K
C1
0.1 µF
C2
150 pF
C
2
3
6
1

TL/H/7752-20

Simulated Inductor


R2
100
R3
10M
LM101A
L
C1
0.1 µF
R1
10M
1%
C2
300 pF
C3
30 pF
R4
10K
2
3
6
1

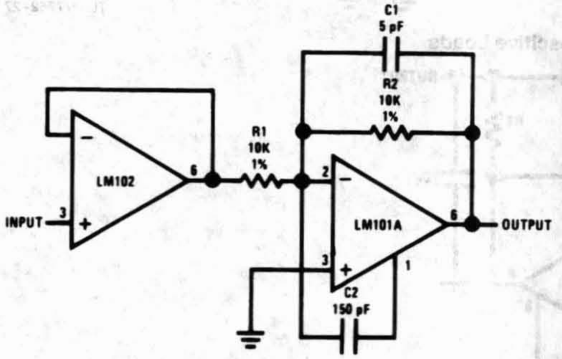
$L \cong R1\,R2\,C1$

$R_S = R2$

$R_P = R1$

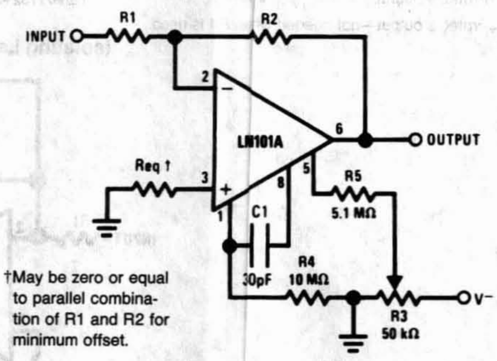
TL/H/7752-21

Fast Inverting Amplifier with High Input Impedance


C1
5 pF
R2
10K
1%
R1
10K
1%
LM102
LM101A
INPUT
OUTPUT
C2
150 pF
2
3
6
1

TL/H/7752-22

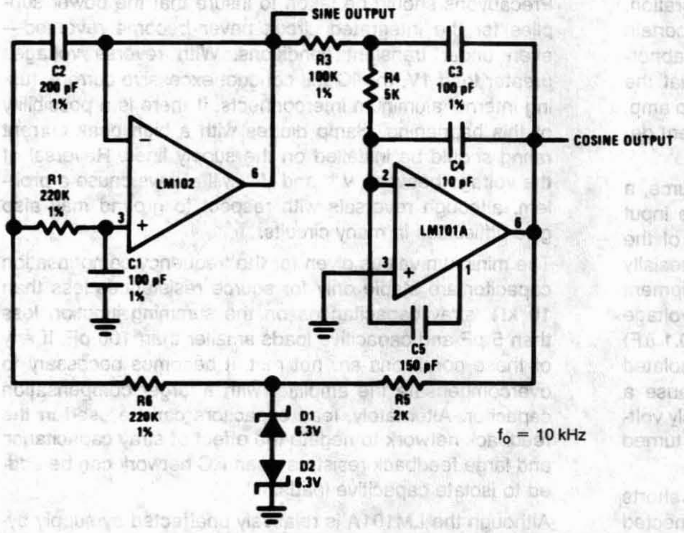
Inverting Amplifier with Balancing Circuit


INPUT
R1
R2
LM101A
OUTPUT
Req †
C1
30pF
R5
5.1 MΩ
R4
10 MΩ
R3
50 kΩ
V−
2
3
5
6
8
1

†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

TL/H/7752-23

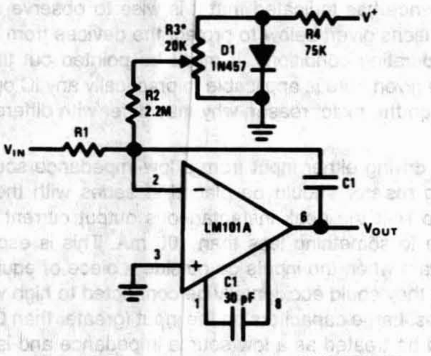
Sine Wave Oscillator


SINE OUTPUT
C2
200 pF
1%
R3
100K
1%
R4
5K
C3
100 pF
1%
COSINE OUTPUT
C4
10 pF
R1
220K
1%
LM102
LM101A
C1
100 pF
1%
C5
150 pF
R6
220K
1%
R5
2K
D1
6.3V
D2
6.3V
2
3
6
1

$f_o = 10$ kHz

TL/H/7752-24

Integrator with Bias Current Compensation


R3*
20K
D1
1N457
R4
75K
V+
R2
2.2M
R1
V_{IN}
C1
LM101A
V_{OUT}
C1
30 pF
2
3
6
1
8

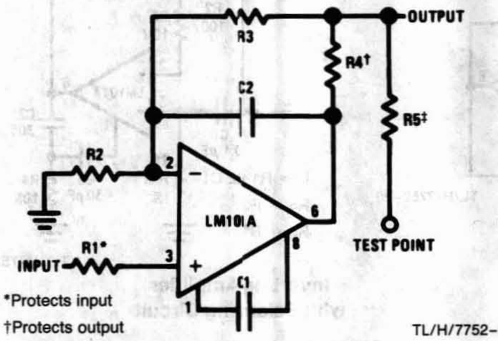
TL/H/7752-25

*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over −55°C to +125°C temperature range.

**Pin connections shown are for 8-pin packages.

Application Hints**

Protecting Against Gross Fault Conditions



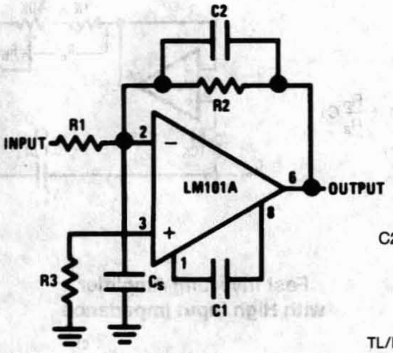
*Protects input

†Protects output

‡Protects output—not needed when R4 is used.

TL/H/7752-26

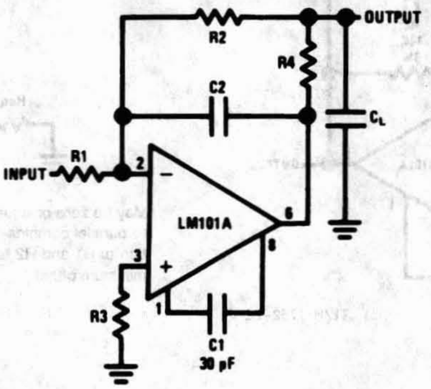
Compensating for Stray Input Capacitances or Large Feedback Resistor



$$C2 = \frac{R1\ C_S}{R2}$$

TL/H/7752-27

Isolating Large Capacitive Loads



TL/H/7752-28

Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifer drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fusing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

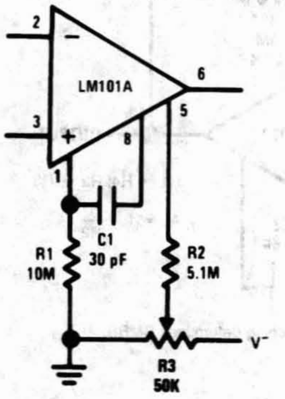
The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

**Pin connections shown are for 8-pin packages.

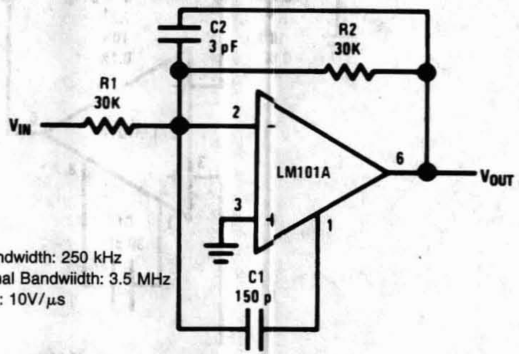
Typical Applications** (Continued)

Standard Compensation and Offset Balancing Circuit


2
3
LM101A
6
5
8
1
C1
30 pF
R1
10M
R2
5.1M
R3
50K
V⁻

TL/H/7752-29

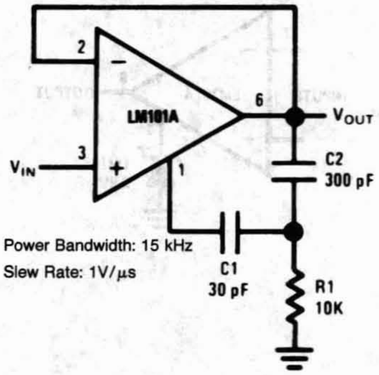
Fast Summing Amplifier


C2
3 pF
R2
30K
R1
30K
V_IN
2
3
LM101A
6
1
V_OUT
C1
150 p

Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

TL/H/7752-30

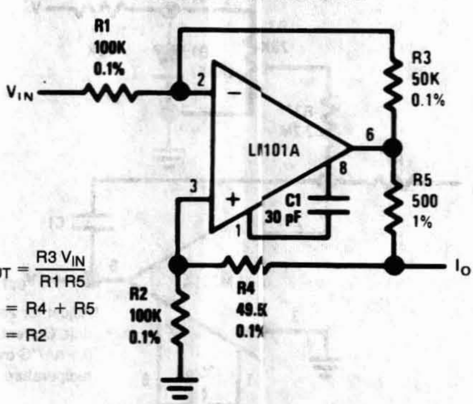
Fast Voltage Follower


2
3
V_IN
LM101A
6
1
V_OUT
C2
300 pF
C1
30 pF
R1
10K

Power Bandwidth: 15 kHz
Slew Rate: 1V/μs

TL/H/7752-31

Bilateral Current Source


R1
100K
0.1%
V_IN
2
3
LM101A
6
8
1
C1
30 pF
R3
50K
0.1%
R5
500
1%
R4
49.5K
0.1%
R2
100K
0.1%
I_OUT

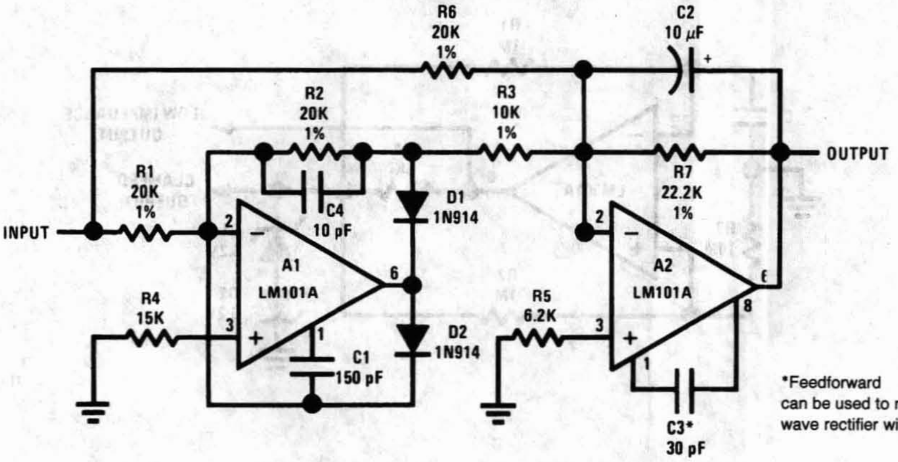
$$I_{OUT} = \frac{R3\,V_{IN}}{R1\,R5}$$

$R3 = R4 + R5$

$R1 = R2$

TL/H/7752-32

Fast AC/DC Converter*


R6
20K
1%
C2
10 μF
+
R2
20K
1%
R3
10K
1%
R1
20K
1%
INPUT
C4
10 pF
D1
1N914
R7
22.2K
1%
OUTPUT
2
A1
LM101A
6
3
1
R4
15K
C1
150 pF
D2
1N914
R5
6.2K
2
3
A2
LM101A
6
8
1
C3*
30 pF

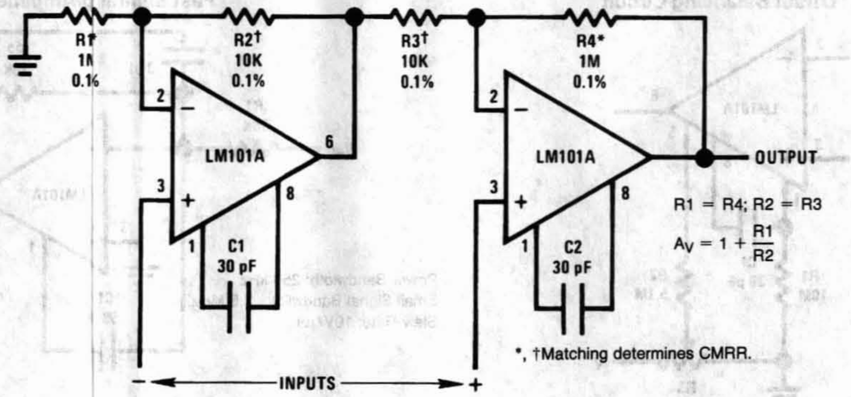
*Feedforward compensation can be used to make a fast full wave rectifier without a filter.

TL/H/7752-33

**Pin connections shown are for 8-pin packages.

Typical Applications** (Continued)

Instrumentation Amplifier


R1†
1M
0.1%
R2†
10K
0.1%
R3†
10K
0.1%
R4*
1M
0.1%
2
3
6
8
1
LM101A
C1
30 pF
2
3
8
1
LM101A
C2
30 pF
OUTPUT
− INPUTS +

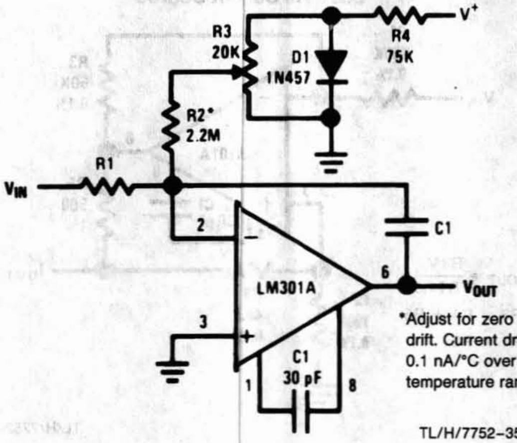
R1 = R4; R2 = R3

$A_V = 1 + \frac{R1}{R2}$

*, †Matching determines CMRR.

TL/H/7752–34

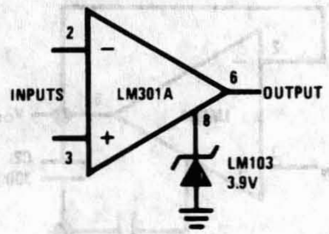
Integrator with Bias Current Compensation


V+
R3
20K
D1
1N457
R4
75K
R2*
2.2M
R1
VIN
C1
2
3
6
LM301A
VOUT
C1
30 pF
1
8

*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over 0°C to +70°C temperature range.

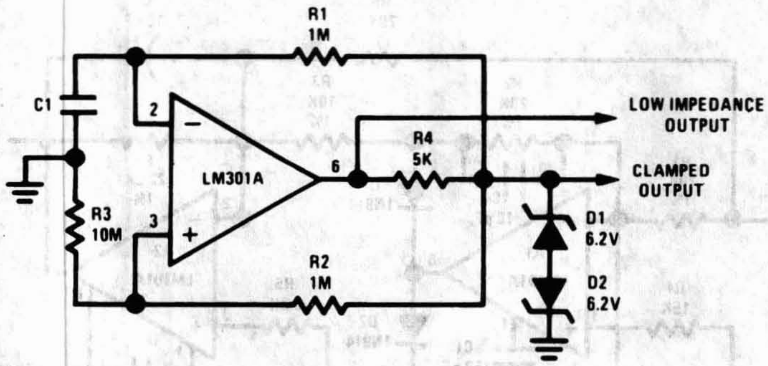
TL/H/7752–35

Voltage Comparator for Driving RTL Logic or High Current Driver


2
INPUTS
3
LM301A
6
OUTPUT
8
LM103
3.9V

TL/H/7752–37

Low Frequency Square Wave Generator

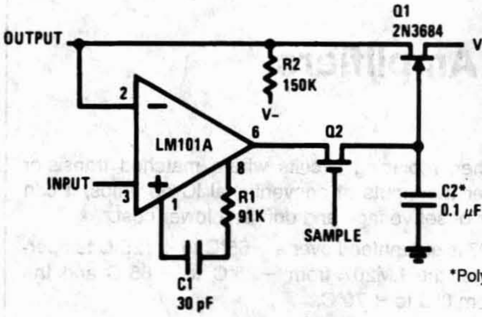

R1
1M
C1
2
3
LM301A
6
R4
5K
R3
10M
R2
1M
LOW IMPEDANCE OUTPUT
CLAMPED OUTPUT
D1
6.2V
D2
6.2V

TL/H/7752–36

**Pin connections shown are for 8-pin packages.

Typical Applications** (Continued)

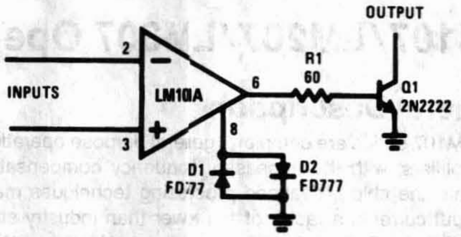
Low Drift Sample and Hold


OUTPUT
Q1
2N3684
V+
R2
150K
V−
2
LM101A
6
Q2
INPUT
3
8
1
R1
91K
SAMPLE
C2*
0.1 μF
C1
30 pF

*Polycarbonate-dielectric capacitor

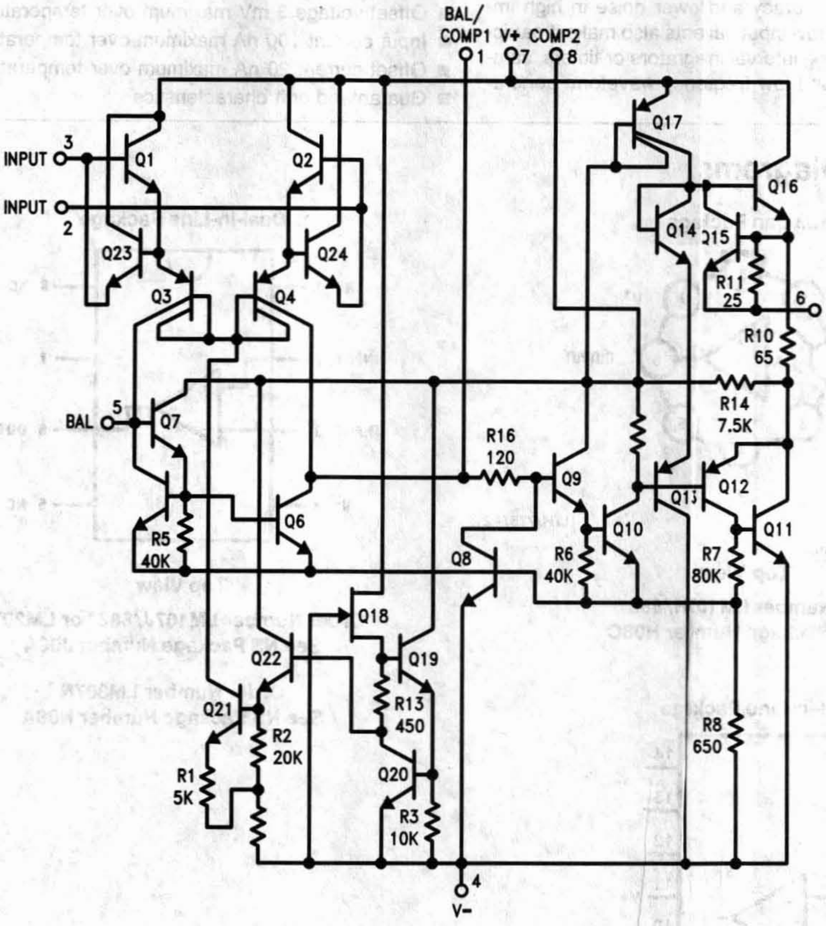
TL/H/7752–38

Voltage Conparator for Driving DTL or TTLIntegrated Circuits


OUTPUT
2
INPUTS
LM101A
3
6
8
R1
60
Q1
2N2222
D1
FD777
D2
FD777

TL/H/7752–39

Schematic**


BAL/
COMP1
V+
COMP2
1
7
8
INPUT
3
INPUT
2
Q1
Q2
Q23
Q24
Q3
Q4
BAL
5
Q7
R5
40K
Q6
R16
120
Q9
Q8
Q18
Q22
Q19
Q21
R13
450
R2
20K
R1
5K
Q20
R3
10K
4
V−
Q17
Q16
Q14
Q15
R11
25
6
OUT
R10
65
R14
7.5K
Q13
Q12
Q10
Q11
R6
40K
R7
80K
R8
650

TL/H/7752–1

**Pin connections shown are for 8-pin packages.

National Semiconductor

LM107/LM207/LM307 Operational Amplifiers

General Description

The LM107 series are complete, general purpose operational amplifiers, with the necessary frequency compensation built into the chip. Advanced processing techniques make the input currents a factor of ten lower than industry standards like the 709. Yet, they are a direct, plug-in replacement for the 709, LM101A and 741

The LM107 series offers the features of the LM101A, which makes its application nearly foolproof. In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at a lower cost.

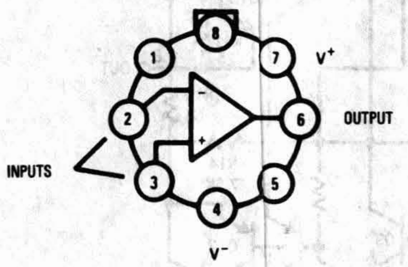
The LM107 is guaranteed over a −55°C to +125°C temperature range, the LM207 from −25°C to +85°C and the LM307 from 0°C to +70°C.

Features

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics

Connection Diagrams

Metal Can Package



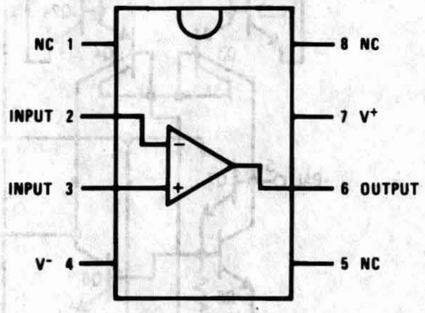
TL/H/7757-2

Note: Pin 4 connected to case.

Top View

Order Number LM107H/883*
See NS Package Number H08C

Dual-in-Line Package



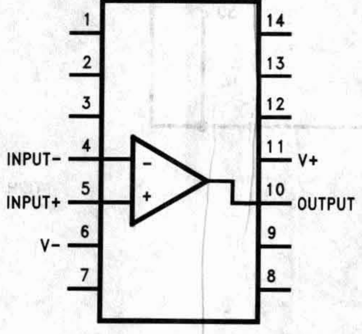
TL/H/7757-3

Top View

Order Number LM107J/883* or LM207J
See NS Package Number J08A

Order Number LM307N
See NS Package Number N08A

Dual-in-Line Package



TL/H/7757-13

Order Number LM107J-14/883*
See NS Package Number J14A

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*Available per SMD# 5962-8958901.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM107/LM207	LM307
Supply Voltage	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Voltage	±30V	±30V
Input Voltage (Note 2)	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous
Operating Temperature Range (T_A)		
(LM107)	−55°C to +125°C	0°C to +70°C
(LM207)	−25°C to +85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	260°C	260°C

	T_{MIN}	T_{MAX}
LM107	−55°C	+125°C
LM207	−25°C	+85°C
LM307	0°C	+70°C

ESD rating to be determined.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM107/LM207			LM307			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C, R_S \leq 50\ k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3.0	50	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4.0		0.5	2.0		MΩ
Supply Current	$T_A = 25°C$							
	$V_S = \pm 20V$		1.8	3.0				mA
	$V_S = \pm 15V$					1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C, V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 2\ k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{MAX}$ $T_{MIN} \leq T_A \leq 25°C$		0.01 0.02	0.1 0.2		0.01 0.02	0.3 0.6	nA/°C nA/°C
Input Bias Current				100			300	nA
Supply Current	$T_A = +125°C, V_S = \pm 20V$		1.2	2.5				mA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM107/LM207			LM307			Units
		Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$							
	$R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 20V$	±15						V
	$V_S = \pm 15V$		+15 −13		±12	+15 −13		V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	96		dB

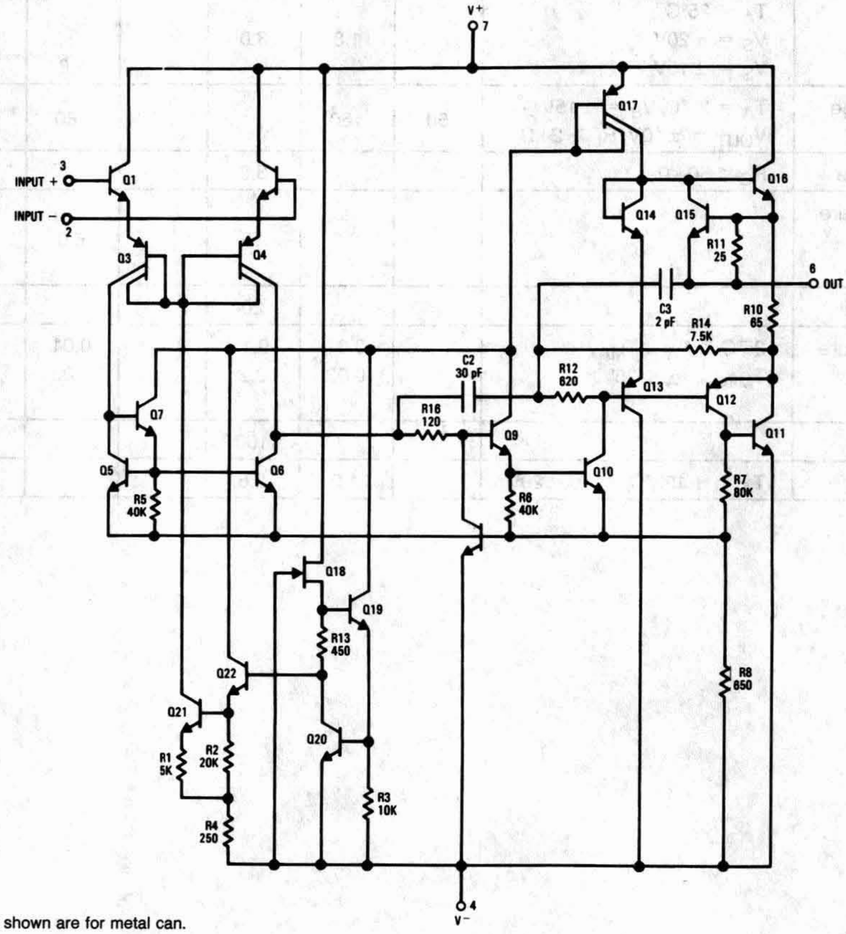
Note 1: The maximum junction temperature of the LM107 is 150°C, and the LM207/LM307 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 30°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq +20V$ and $-55°C \leq T_A \leq +125°C$ for the LM107 or $-25°C \leq T_A + 85°C$ for the LM207, and $0°C \leq T_A \leq +70°C$ and $\pm 5V \leq V_S \leq \pm 15V$ for the LM307 unless otherwise specified.

Note 4: Refer to RETS107X for LM107H and LM107J military specifications.

Schematic Diagram*



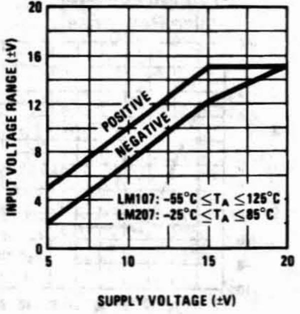
V+
7
INPUT +
3
INPUT −
2
Q1
Q3
Q4
Q5
Q6
Q7
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
R1 5K
R2 20K
R3 10K
R4 250
R5 40K
R6 40K
R7 80K
R8 650
R10 65
R11 25
R12 620
R13 450
R14 7.5K
R16 120
C2 30 pF
C3 2 pF
6
OUT
4
V−

*Pin connections shown are for metal can.

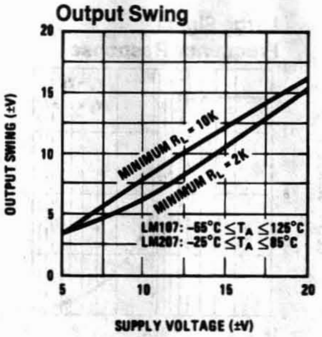
TL/H/7757–1

Guaranteed Performance Characteristics LM107/LM207

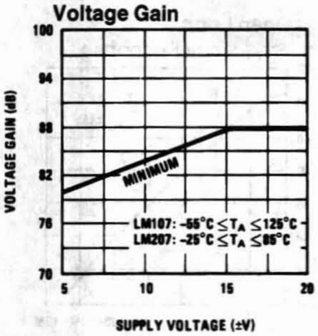
Input Voltage Range



Output Swing



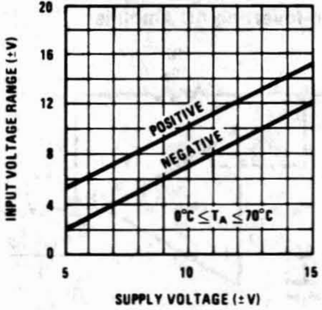
Voltage Gain



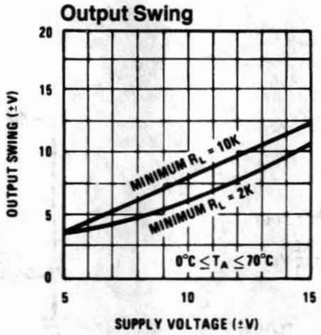
TL/H/7757–4

Guaranteed Performance Characteristics LM307

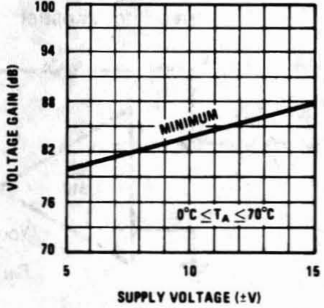
Input Voltage Range



Output Swing



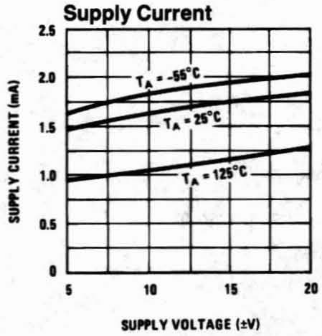
Voltage Gain



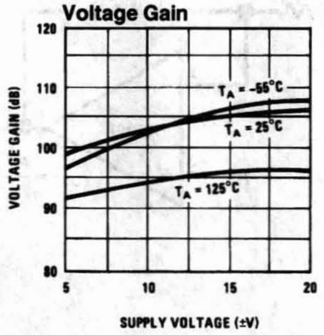
TL/H/7757–5

Typical Performance Characteristics

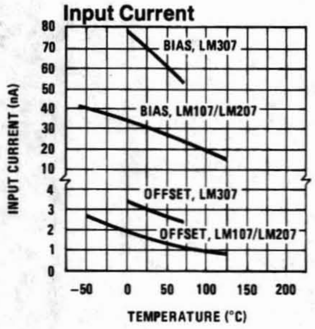
Supply Current



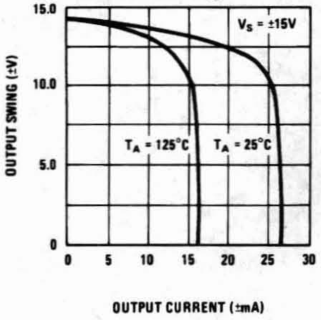
Voltage Gain



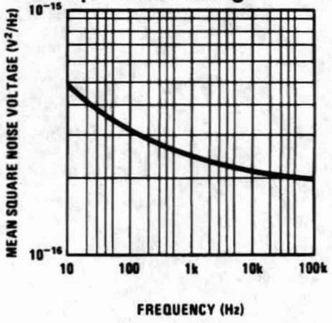
Input Current



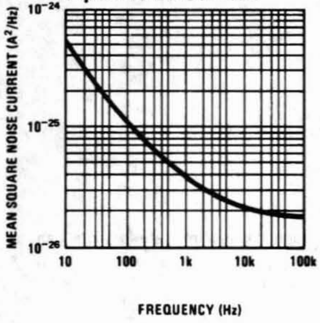
Current Limiting



Input Noise Voltage

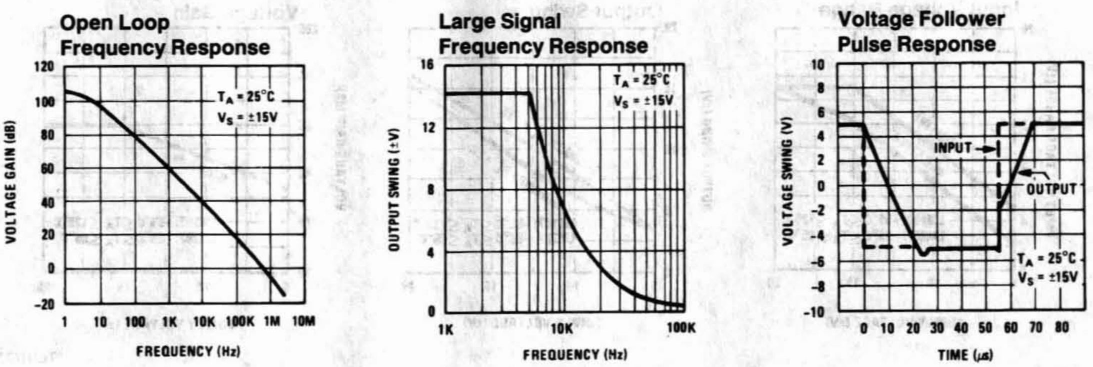


Input Noise Current



TL/H/7757–6

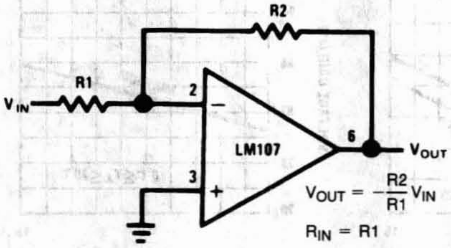
Typical Performance Characteristics (Continued)



TL/H/7757-7

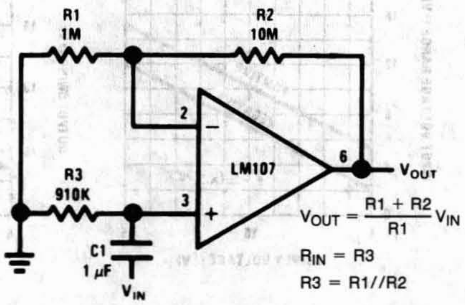
Typical Applications**

Inverting Amplifier


R2
R1
V_IN
2
3
LM107
6
V_OUT
V_OUT = -R2/R1 V_IN
R_IN = R1

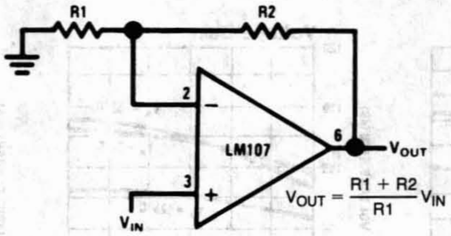
TL/H/7757-8

Non-Inverting AC Amplifier


R1
1M
R2
10M
2
LM107
6
V_OUT
R3
910K
3
C1
1 μF
V_IN
V_OUT = (R1 + R2)/R1 V_IN
R_IN = R3
R3 = R1//R2

TL/H/7757-9

Non-Inverting Amplifier

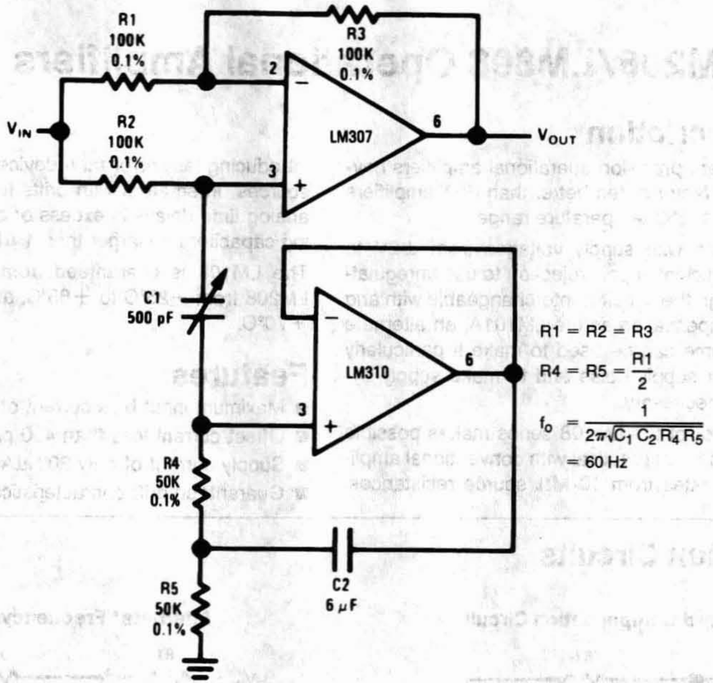

R1
R2
2
LM107
6
V_OUT
3
V_IN
V_OUT = (R1 + R2)/R1 V_IN

TL/H/7757-10

**Pin connections shown are for metal can.

Typical Applications** (Continued)

Turntable Notch Filter


R1
100K
0.1%
R3
100K
0.1%
R2
100K
0.1%
V_IN
V_OUT
LM307
2
3
6
C1
500 pF
LM310
2
3
6
R4
50K
0.1%
R5
50K
0.1%
C2
6 μF

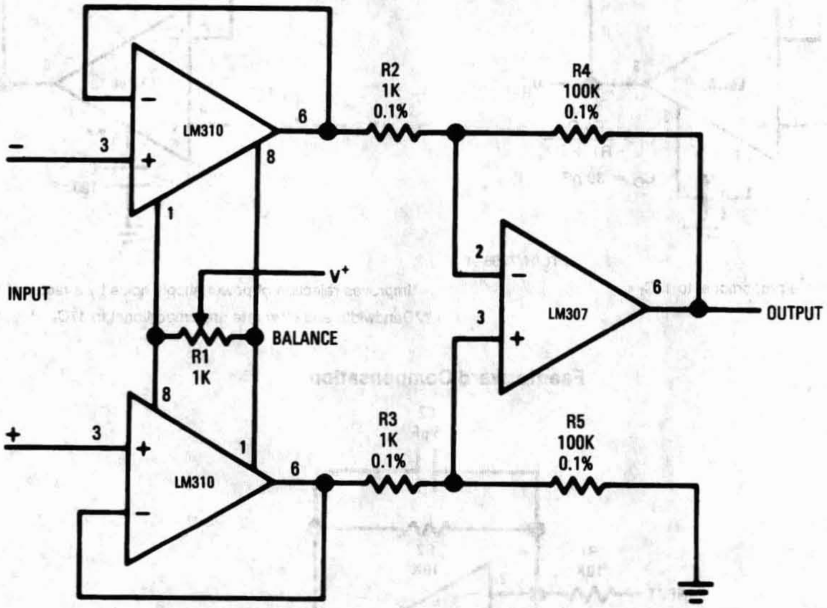
$$R1 = R2 = R3$$

$$R4 = R5 = \frac{R1}{2}$$

$$f_o = \frac{1}{2\pi\sqrt{C_1\, C_2\, R_4\, R_5}} = 60\ \text{Hz}$$

TL/H/7757-11

Differential Input Instrumentation Amplifier


LM310
−
3
+
6
8
1
R2
1K
0.1%
R4
100K
0.1%
V⁺
INPUT
R1
1K
BALANCE
LM307
2
3
6
OUTPUT
+
3
8
1
LM310
6
R3
1K
0.1%
R5
100K
0.1%

TL/H/7757-12

**Pin connections shown are for metal can.

National Semiconductor

LM108/LM208/LM308 Operational Amplifiers

General Description

The LM108 series are precision operational amplifiers having specifications a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range.

The devices operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108 series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

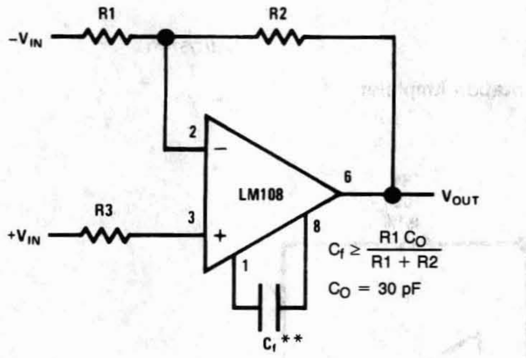
The LM108 is guaranteed from −55°C to +125°C, the LM208 from −25°C to +85°C, and the LM308 from 0°C to +70°C.

Features

- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed drift characteristics

Compensation Circuits

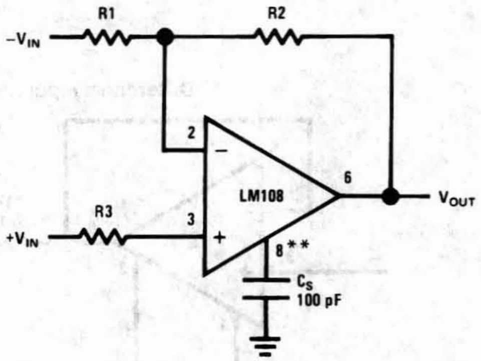
Standard Compensation Circuit



TL/H/7758-1

**Bandwidth and slew rate are proportional to 1/C_f

Alternate* Frequency Compensation

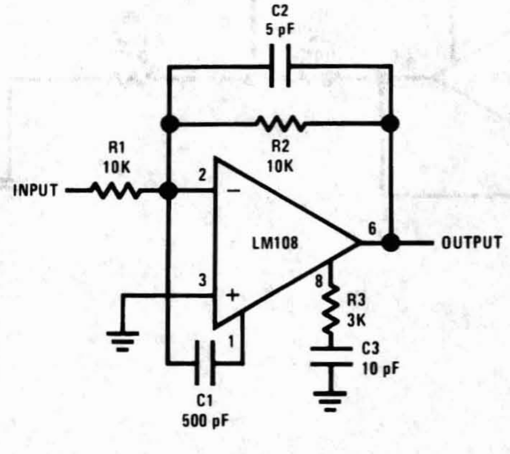


TL/H/7758-2

*Improves rejection of power supply noise by a factor of ten.

**Bandwidth and slew rate are proportional to 1/C_S

Feedforward Compensation



TL/H/7758-3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 5)

	LM108/LM208	LM308
Supply Voltage	±20V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Current (Note 2)	±10 mA	±10 mA
Input Voltage (Note 3)	±15V	±15V
Output Short-Circuit Duration	Continuous	Continuous
Operating Temperature Range (LM108)	−55°C to +125°C	0°C to +70°C
(LM208)	−25°C to + 85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		
DIP	260°C	260°C
H Package Lead Temp		
(Soldering 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	
Small Outline Package		
Vapor Phase (60 seconds)	215°C	
Infrared (15 seconds)	220°C	

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 6)	2000V	

Electrical Characteristics (Note 4)

Parameter	Condition	LM108/LM208			LM308			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		0.05	0.2		0.2	1	nA
Input Bias Current	$T_A = 25°C$		0.8	2.0		1.5	7	nA
Input Resistance	$T_A = 25°C$	30	70		10	40		MΩ
Supply Current	$T_A = 25°C$		0.3	0.6		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C, V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 10\ k\Omega$	50	300		25	300		V/mV
Input Offset Voltage				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				0.4			1.5	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5		2.0	10	pA/°C
Input Bias Current				3.0			10	nA
Supply Current	$T_A = +125°C$		0.15	0.4				mA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \geq 10\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V, R_L = 10\ k\Omega$	±13	±14		±13	±14		V

Electrical Characteristics (Note 4) (Continued)

Parameter	Condition	LM108/LM208			LM308			Units
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	$V_S = \pm 15V$	±13.5			±14			V
Common Mode Rejection Ratio		85	100		80	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

Note 1: The maximum junction temperature of the LM108 is 150°C, for the LM208, 100°C and for the LM308, 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

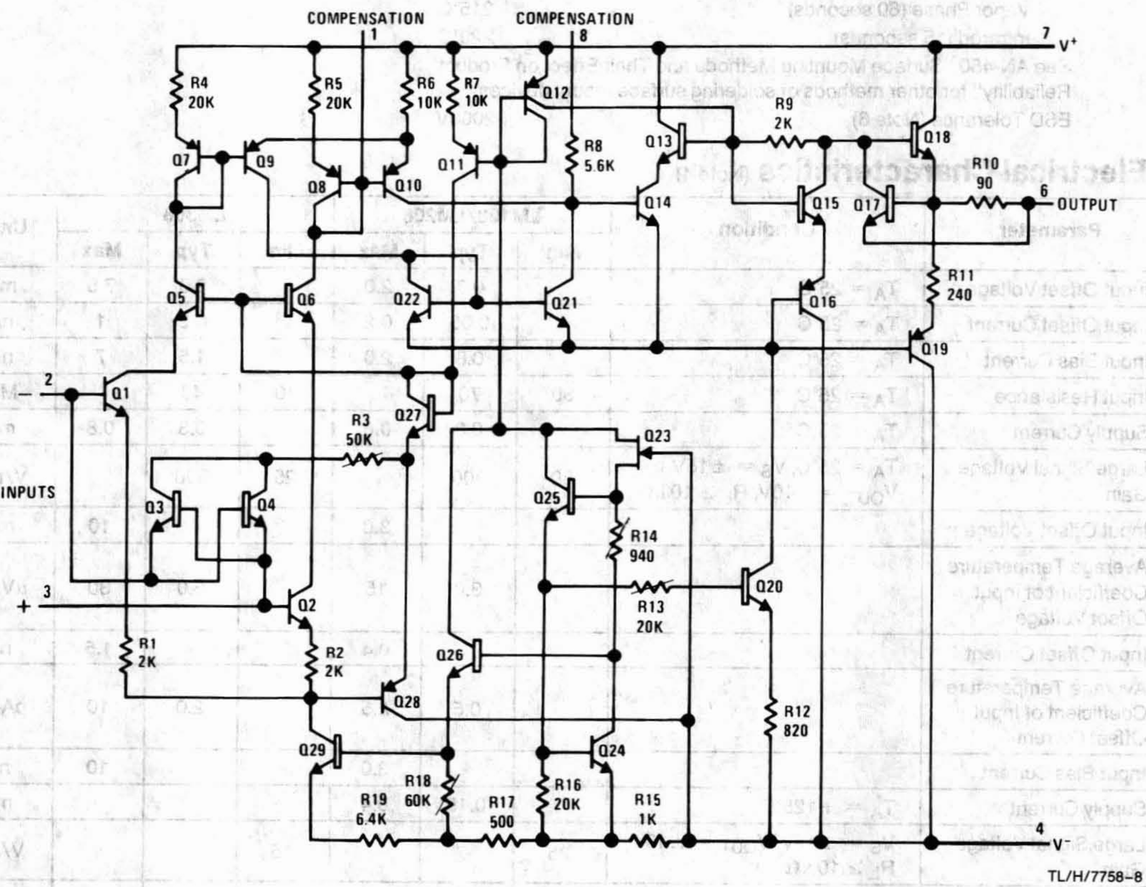
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise specified. With the LM208, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$, and for the LM308 they are limited to $0°C \leq T_A \leq 70°C$.

Note 5: Refer to RETS108X for LM108 military specifications and RETs 108AX for LM108A military specifications.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

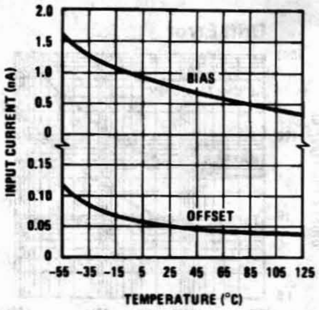
Schematic Diagram



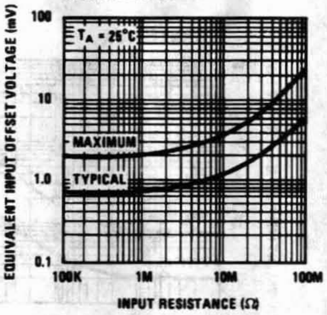
COMPENSATION
1
COMPENSATION
8
7
V+
R4
20K
R5
20K
R6
10K
R7
10K
Q12
R8
5.6K
R9
2K
Q18
Q7
Q9
Q8
Q10
Q11
Q13
Q14
Q15
Q17
R10
90
6
OUTPUT
Q5
Q6
Q22
Q21
Q16
R11
240
Q19
2
−
Q1
Q27
R3
50K
Q23
INPUTS
Q3
Q4
Q25
R14
940
3
+
Q20
R13
20K
Q2
R1
2K
R2
2K
Q26
Q28
R12
820
Q29
Q24
R18
60K
R19
6.4K
R17
500
R16
20K
R15
1K
4
V−

TL/H/7758-8

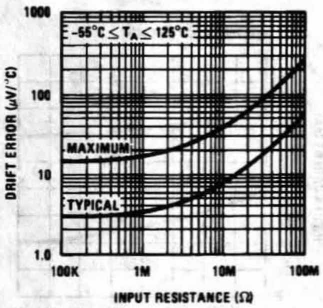
Typical Performance Characteristics LM108/LM208



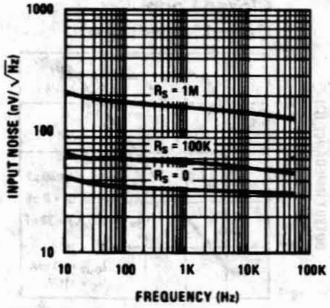
Input Currents



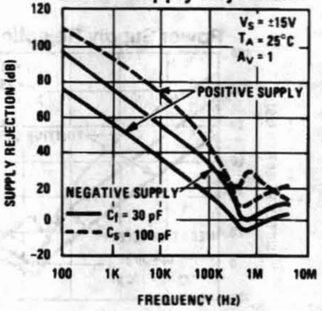
Offset Error



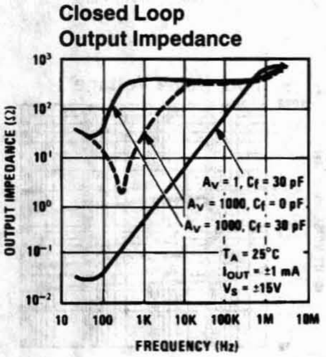
Drift Error



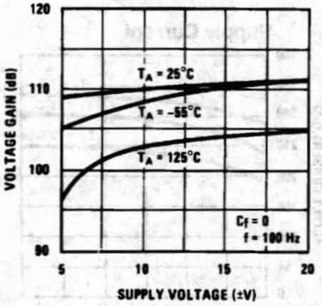
Input Noise Voltage



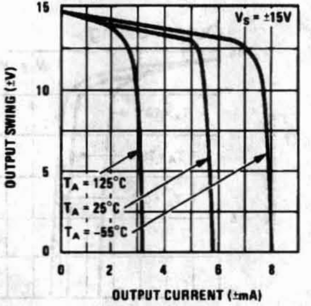
Power Supply Rejection



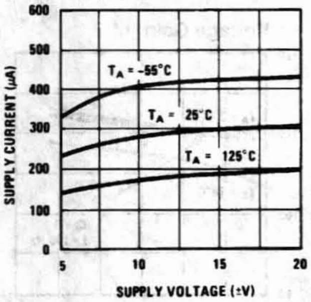
Closed Loop Output Impedance



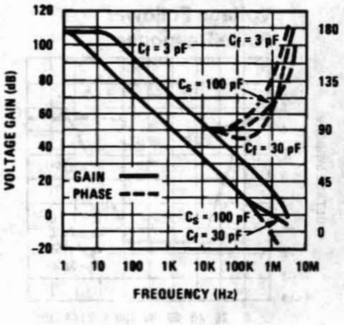
Voltage Gain



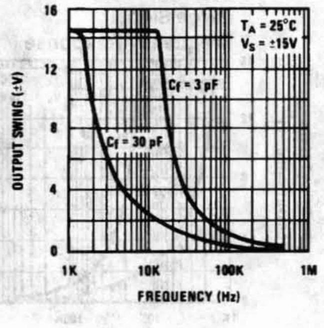
Output Swing



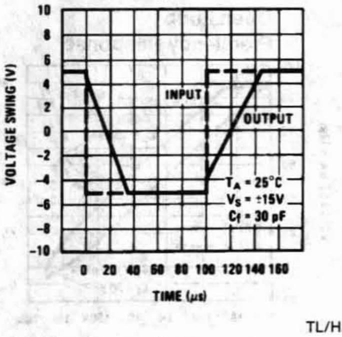
Supply Current



Open Loop Frequency Response



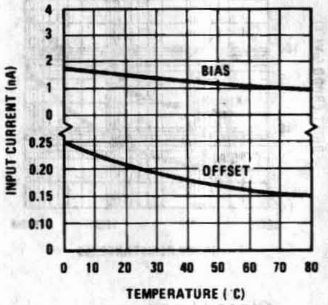
Large Signal Frequency Response



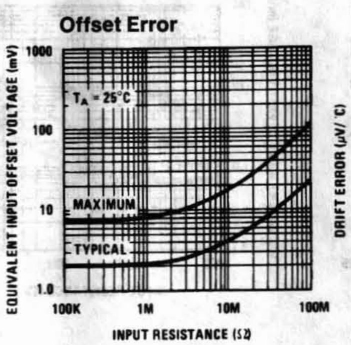
Voltage Follower Pulse Response

TL/H/7758–6

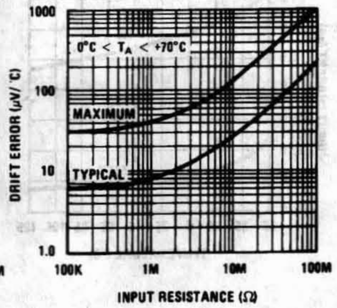
Typical Performance Characteristics LM308



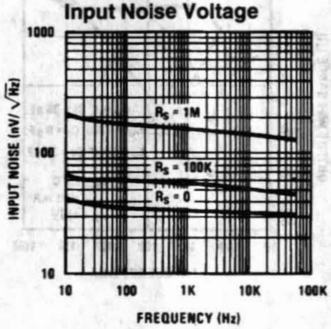
Input Currents



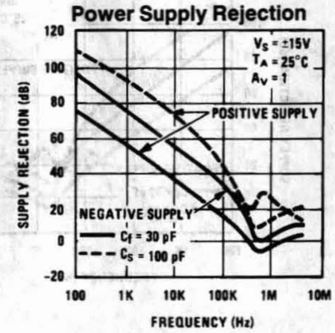
Offset Error



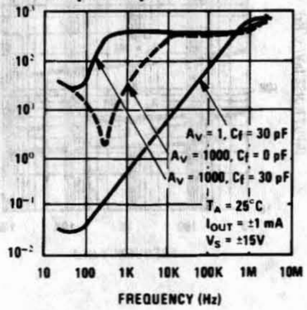
Drift Error



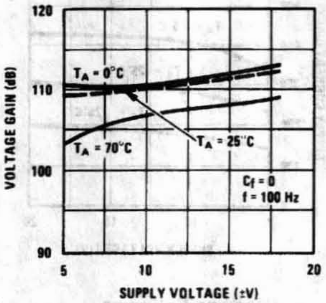
Input Noise Voltage



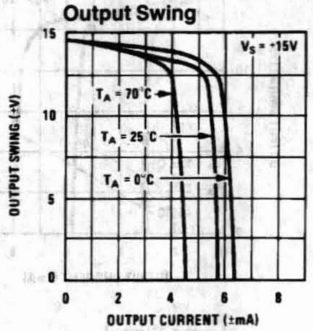
Power Supply Rejection



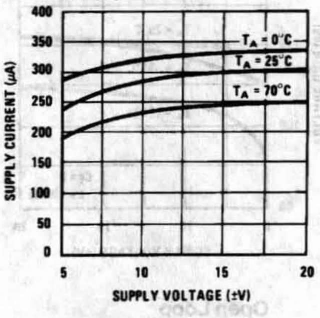
Closed Loop Output Impedance



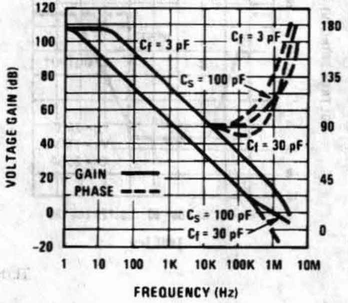
Voltage Gain



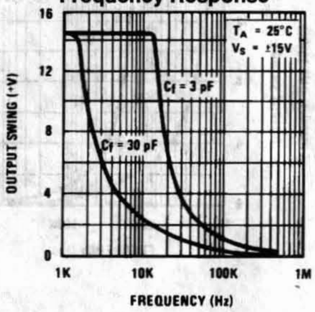
Output Swing



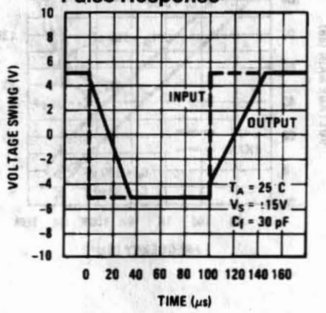
Supply Current



Open Loop Frequency Response



Large Signal Frequency Response

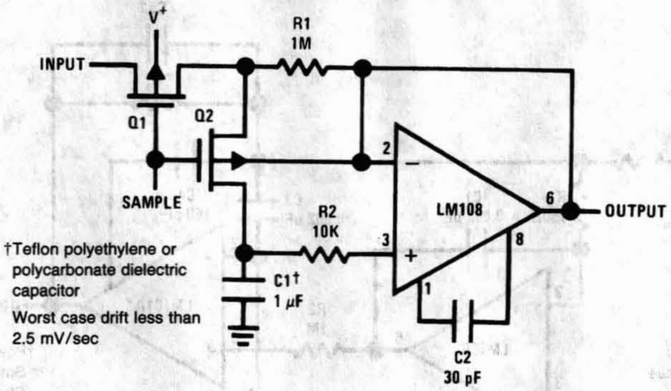


Voltage Follower Pulse Response

TL/H/7758–7

Typical Applications

Sample and Hold

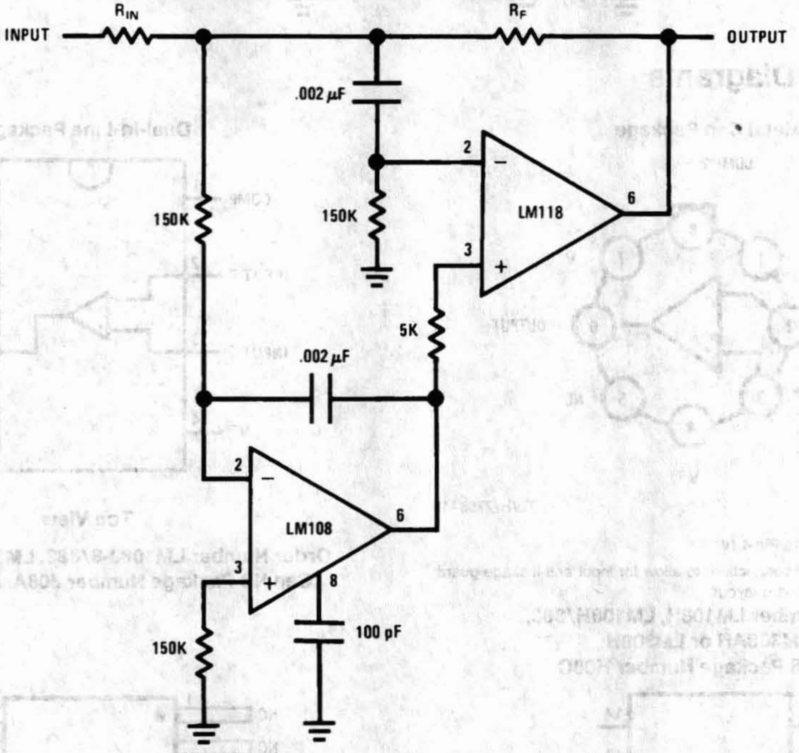

V+
R1
1M
INPUT
Q1
Q2
2
−
SAMPLE
LM108
6
OUTPUT
R2
10K
3
+
8
C1†
1 µF
1
C2
30 pF

†Teflon polyethylene or polycarbonate dielectric capacitor

Worst case drift less than 2.5 mV/sec

TL/H/7758–4

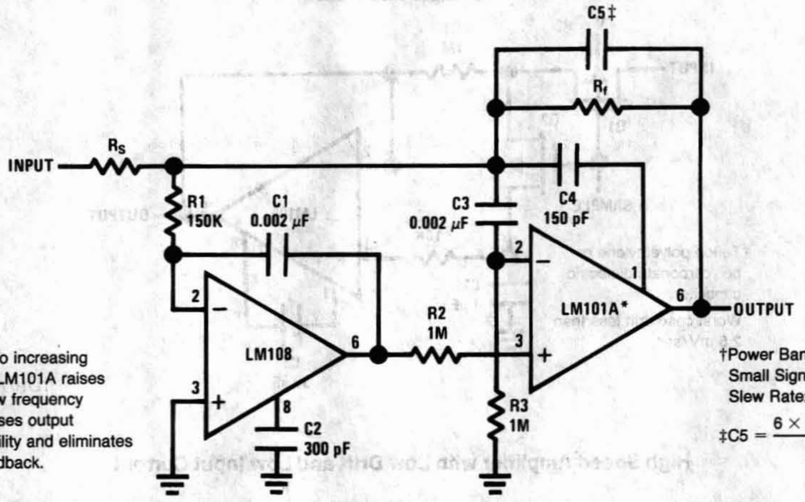
High Speed Amplifier with Low Drift and Low Input Current


INPUT
R_{IN}
R_F
OUTPUT
.002 µF
2
−
150K
150K
LM118
6
3
+
5K
.002 µF
2
−
LM108
6
3
+
8
100 pF
150K

TL/H/7758–5

Typical Applications (Continued)

Fast† Summing Amplifier


C5‡
R_f
INPUT
R_S
R1
150K
C1
0.002 μF
C3
0.002 μF
C4
150 pF
2
1
LM101A*
6
OUTPUT
2
3
LM108
6
8
C2
300 pF
R2
1M
3
R3
1M

*In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

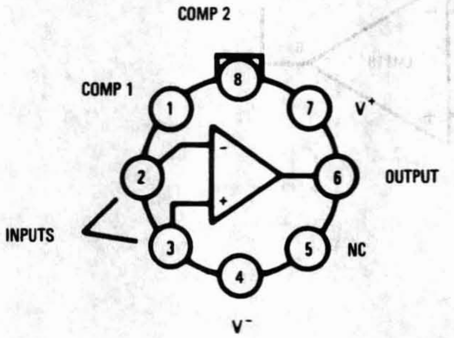
†Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μS

$$‡C5 = \frac{6 \times 10^{-8}}{R_f}$$

TL/H/7758–12

Connection Diagrams

Metal Can Package


COMP 2
COMP 1
8
1
7
V+
2
6
OUTPUT
INPUTS
3
5
NC
4
V−

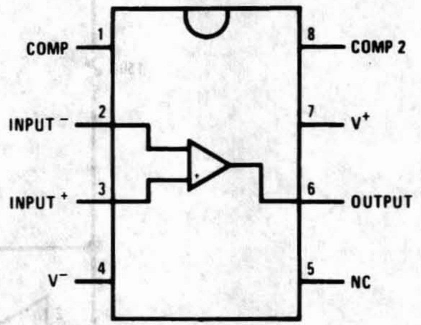
TL/H/7758–13

*Package is connected to Pin 4 (V−)

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

Order Number LM108H, LM108H/883, LM308AH or LM308H
See NS Package Number H08C

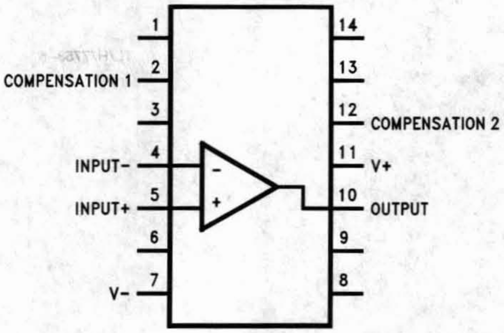
Dual-In-Line Package


COMP
1
8
COMP 2
INPUT −
2
7
V+
INPUT +
3
6
OUTPUT
V−
4
5
NC

TL/H/7758–15

Top View

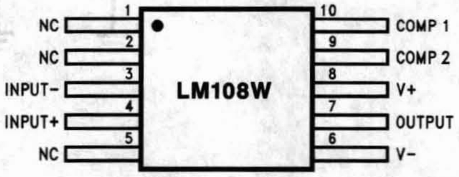
Order Number LM108J-8/883, LM308M or LM308N
See NS Package Number J08A, M08A or N08E


1
14
COMPENSATION 1
2
13
3
12
COMPENSATION 2
INPUT−
4
11
V+
INPUT+
5
10
OUTPUT
6
9
V−
7
8

TL/H/7758–16

Top View

Order Number LM108J/883
See NS Package Number J14A


NC
1
10
COMP 1
NC
2
9
COMP 2
INPUT−
3
8
V+
INPUT+
4
LM108W
7
OUTPUT
NC
5
6
V−

TL/H/7758–17

Order Number LM108W/883
See NS Package Number W10A

†Also available per JM38510/10104

National Semiconductor

LM118/LM218/LM318 Operational Amplifiers

General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

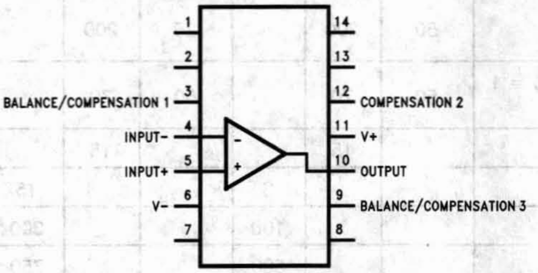
The LM218 is identical to the LM118 except that the LM218 has its performance specified over a −25°C to +85°C temperature range. The LM318 is specified from 0°C to +70°C.

Features

- 15 MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 250 nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

Connection Diagrams

Dual-In-Line Package

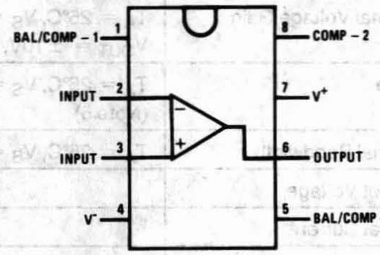

1
2
3
4
5
6
7
8
9
10
11
12
13
14
BALANCE/COMPENSATION 1
INPUT−
INPUT+
V−
COMPENSATION 2
V+
OUTPUT
BALANCE/COMPENSATION 3

TL/H/7766-24

Top View

Order Number LM118J/883*
See NS Package Number J14A

Dual-In-Line Package

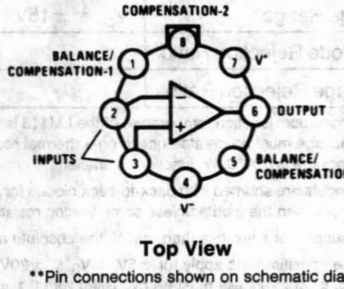

BAL/COMP − 1
INPUT
INPUT
V−
COMP − 2
V+
OUTPUT
BAL/COMP − 3
1
2
3
4
5
6
7
8

TL/H/7766-3

Top View

Order Number LM118J-8/883*,
LM318M or LM318N
See NS Package Number J08A, M08A or N08B

Metal Can Package**


COMPENSATION-2
BALANCE/
COMPENSATION-1
V+
OUTPUT
INPUTS
BALANCE/
COMPENSATION-3
V−
1
2
3
4
5
6
7
8

TL/H/7766-2

Top View

**Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Order Number LM118H, LM118H/883*,
LM218H or LM318H
See NS Package Number H08C

*Available per JM38510/10107.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LM118	−55°C to +125°C
LM218	−25°C to +85°C
LM318	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
Hermetic Package	300°C
Plastic Package	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 7)	2000V

Electrical Characteristics (Note 4)

Parameter	Conditions	LM118/LM218 Min	LM118/LM218 Typ	LM118/LM218 Max	LM318 Min	LM318 Typ	LM318 Max	Units
Input Offset Voltage	$T_A = 25°C$		2	4		4	10	mV
Input Offset Current	$T_A = 25°C$		6	50		30	200	nA
Input Bias Current	$T_A = 25°C$		120	250		150	500	nA
Input Resistance	$T_A = 25°C$	1	3		0.5	3		MΩ
Supply Current	$T_A = 25°C$		5	8		5	10	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	200		25	200		V/mV
Slew Rate	$T_A = 25°C$, $V_S = \pm 15V$, $A_V = 1$ (Note 5)	50	70		50	70		V/μs
Small Signal Bandwidth	$T_A = 25°C$, $V_S = \pm 15V$		15			15		MHz
Input Offset Voltage				6			15	mV
Input Offset Current				100			300	nA
Input Bias Current				500			750	nA
Supply Current	$T_A = 125°C$		4.5	7				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2\ k\Omega$	±12	±13		±12	±13		V
Input Voltage Range	$V_S = \pm 15V$	±11.5			±11.5			V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

Note 1: The maximum junction temperature of the LM118 is 150°C, the LM218 is 110°C, and the LM318 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM118), $-25°C \leq T_A \leq +85°C$ (LM218), and $0°C \leq T_A \leq +70°C$ (LM318). Also, power supplies must be bypassed with 0.1 μF disc capacitors.

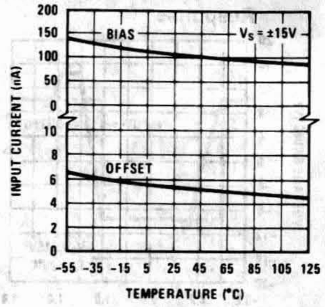
Note 5: Slew rate is tested with $V_S = \pm 15V$. The LM118 is in a unity-gain non-inverting configuration. V_{IN} is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and guaranteed to exceed 50V/μs.

Note 6: Refer to RETS118X for LM118H and LM118J military specifications.

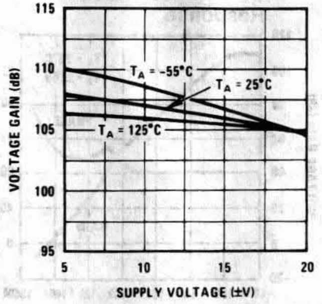
Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics LM118, LM218

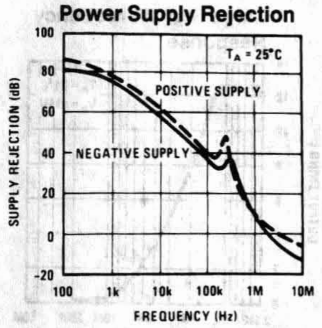
Input Current



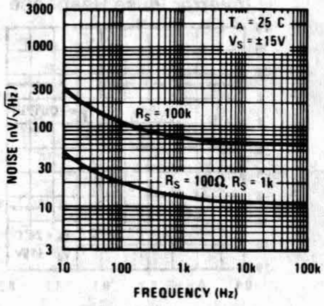
Voltage Gain



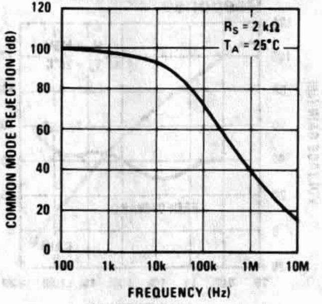
Power Supply Rejection



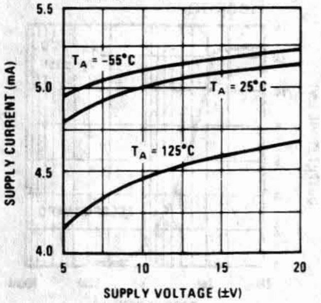
Input Noise Voltage



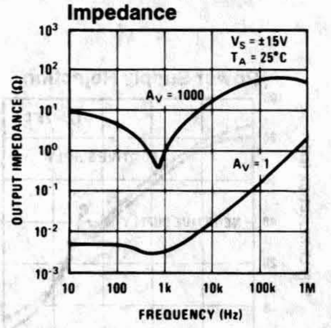
Common Mode Rejection



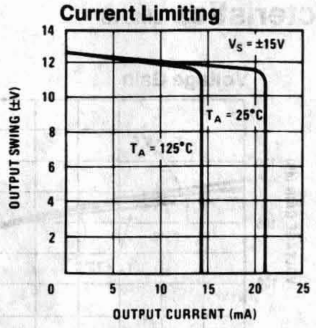
Supply Current



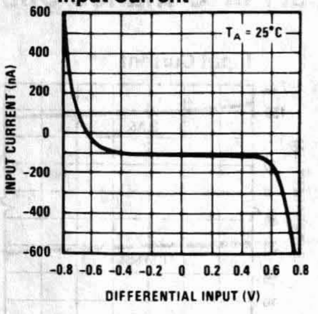
Closed Loop Output Impedance



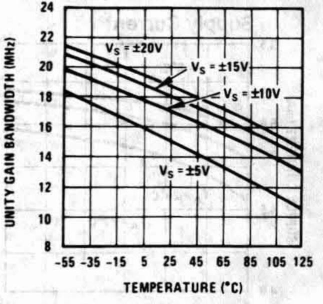
Current Limiting



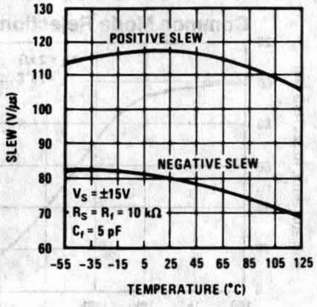
Input Current



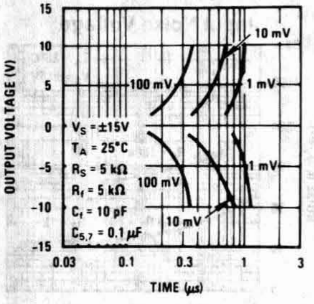
Unity Gain Bandwidth



Voltage Follower Slew Rate



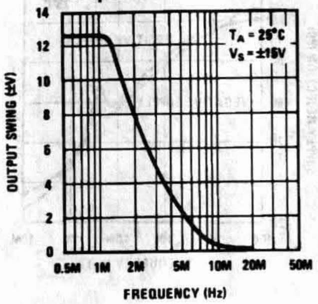
Inverter Settling Time



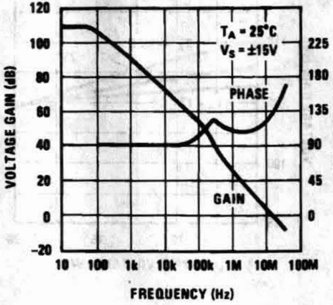
TL/H/7766–4

Typical Performance Characteristics LM118, LM218 (Continued)

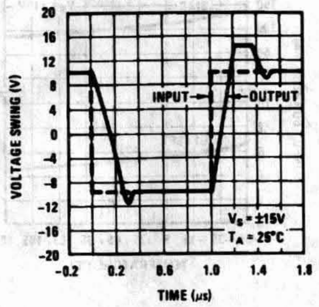
Large Signal Frequency Response



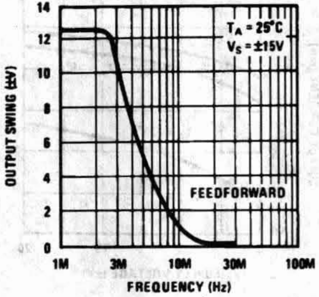
Open Loop Frequency Response



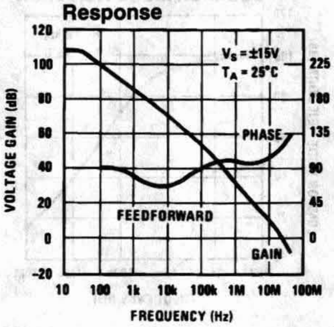
Voltage Follower Pulse Response



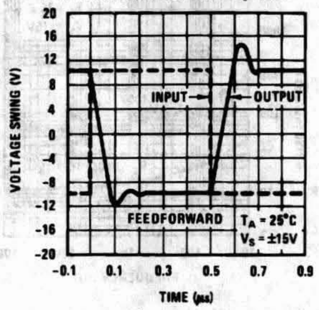
Large Signal Frequency Response



Open Loop Frequency Response



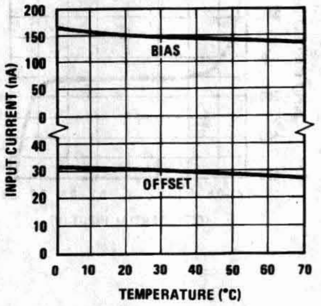
Inverter Pulse Response



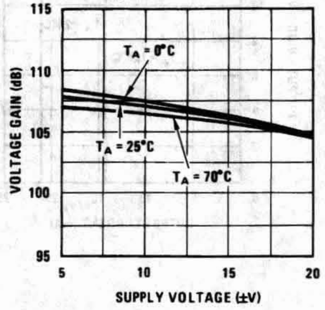
TL/H/7766–5

Typical Performance Characteristics LM318

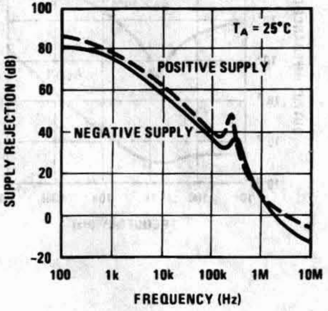
Input Current



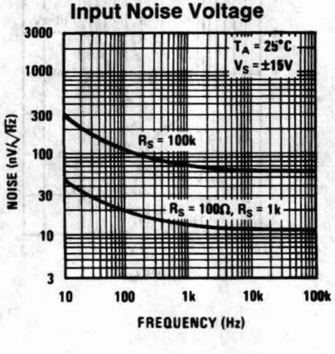
Voltage Gain



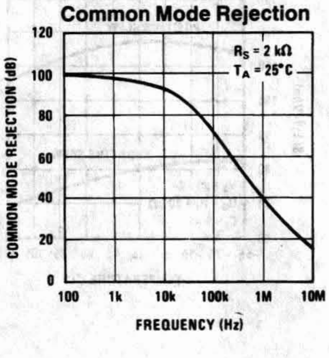
Power Supply Rejection



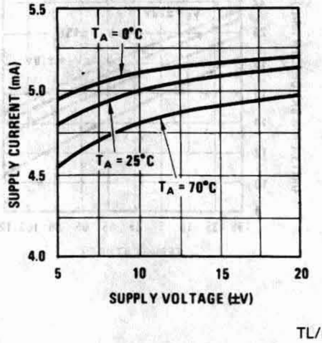
Input Noise Voltage



Common Mode Rejection



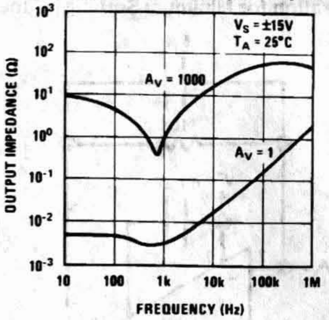
Supply Current



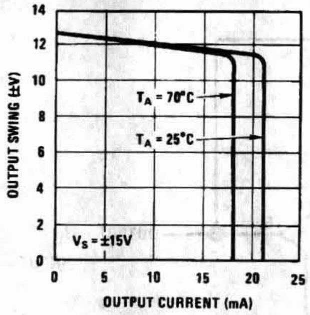
TL/H/7766–6

Typical Performance Characteristics LM318 (Continued)

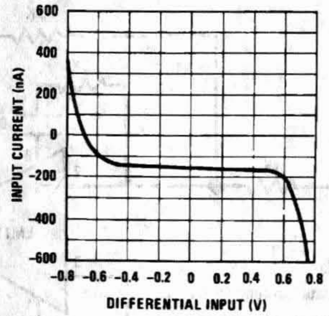
Closed Loop Output Impedance



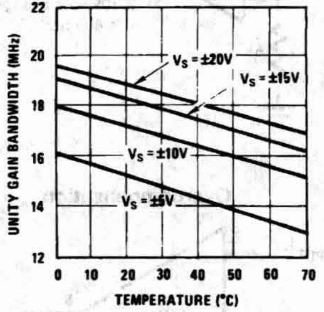
Current Limiting



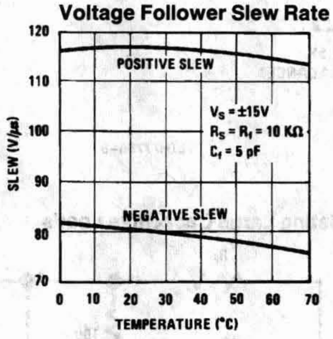
Input Current



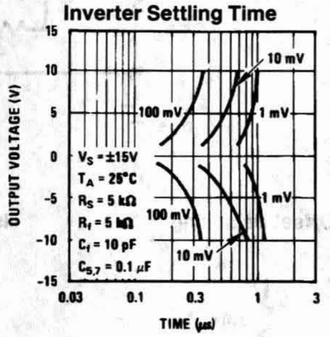
Unity Gain Bandwidth



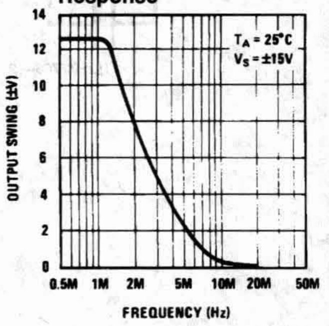
Voltage Follower Slew Rate



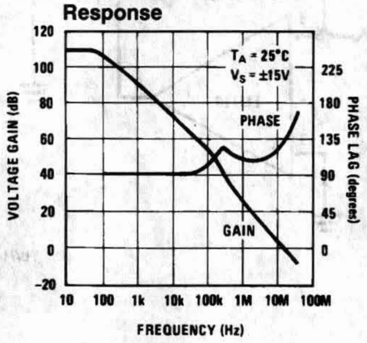
Inverter Settling Time



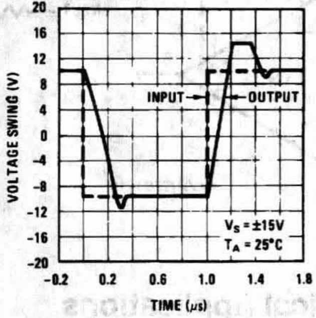
Large Signal Frequency Response



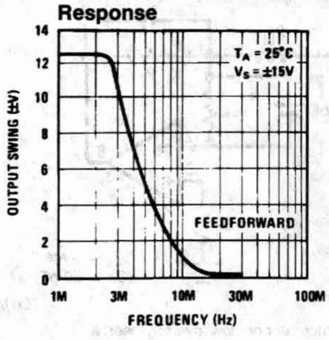
Open Loop Frequency Response



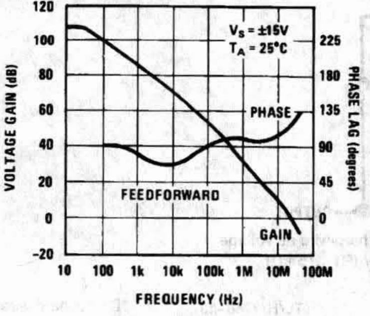
Voltage Follower Pulse Response



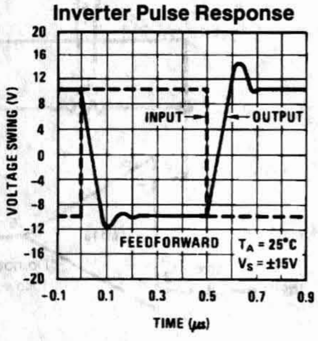
Large Signal Frequency Response



Open Loop Frequency Response



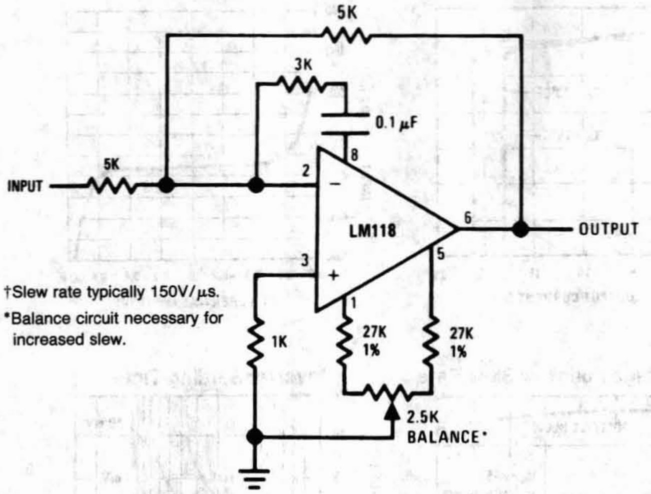
Inverter Pulse Response



TL/H/7766–7

Auxiliary Circuits

Feedforward Compensation for Greater Inverting Slew Rate†

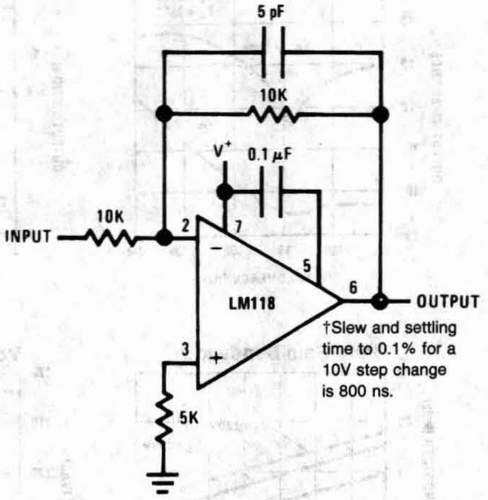

5K
3K
0.1 µF
INPUT
5K
2
8
LM118
6
OUTPUT
3
5
1
1K
27K 1%
27K 1%
2.5K
BALANCE*

†Slew rate typically 150V/µs.

*Balance circuit necessary for increased slew.

TL/H/7766-8

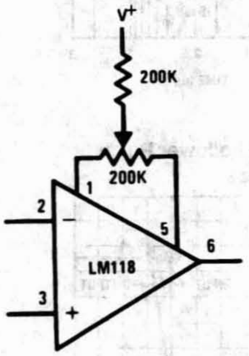
Compensation for Minimum Settling† Time


5 pF
10K
V+
0.1 µF
INPUT
10K
2
7
5
LM118
6
OUTPUT
3
5K

†Slew and settling time to 0.1% for a 10V step change is 800 ns.

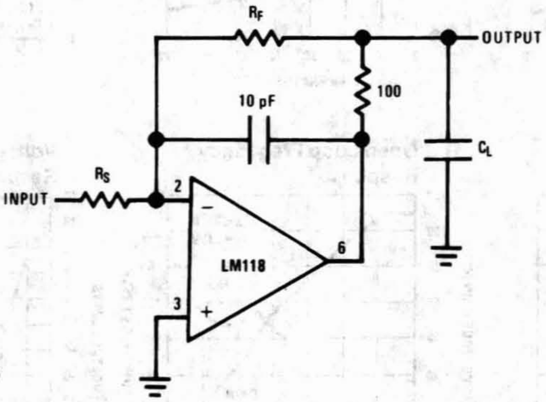
TL/H/7766-9

Offset Balancing


V+
200K
200K
1
2
5
6
LM118
3

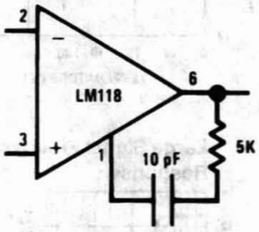
TL/H/7766-10

Isolating Large Capacitive Loads


RF
OUTPUT
100
10 pF
CL
RS
INPUT
2
LM118
6
3

TL/H/7766-11

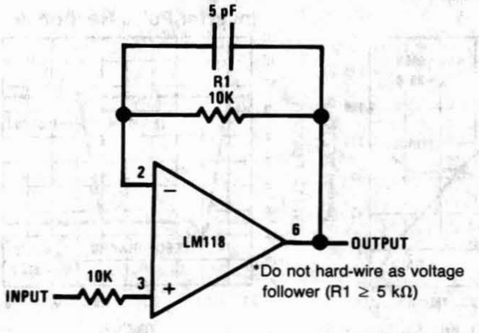
Overcompensation


2
LM118
6
3
1
10 pF
5K

TL/H/7766-12

Typical Applications

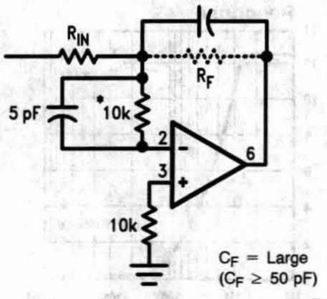
Fast Voltage Follower*


5 pF
R1
10K
2
LM118
6
OUTPUT
10K
3
INPUT

*Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

TL/H/7766-13

Integrator or Slow Inverter


RIN
RF
5 pF
*10k
2
6
3
10k

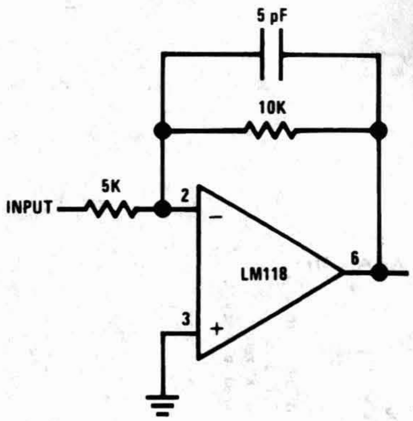
C_F = Large
($C_F \geq 50$ pF)

TL/H/7766-14

*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

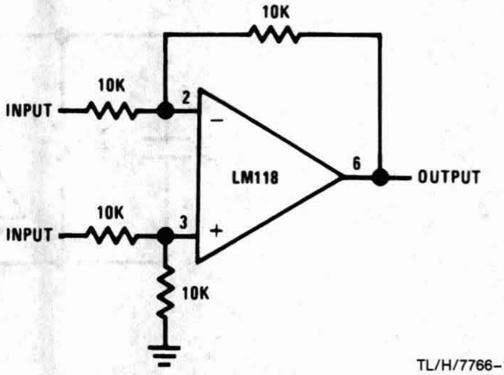
Typical Applications (Continued)

Fast Summing Amplifier


5 pF
10K
5K
INPUT
2
3
LM118
6
OUTPUT

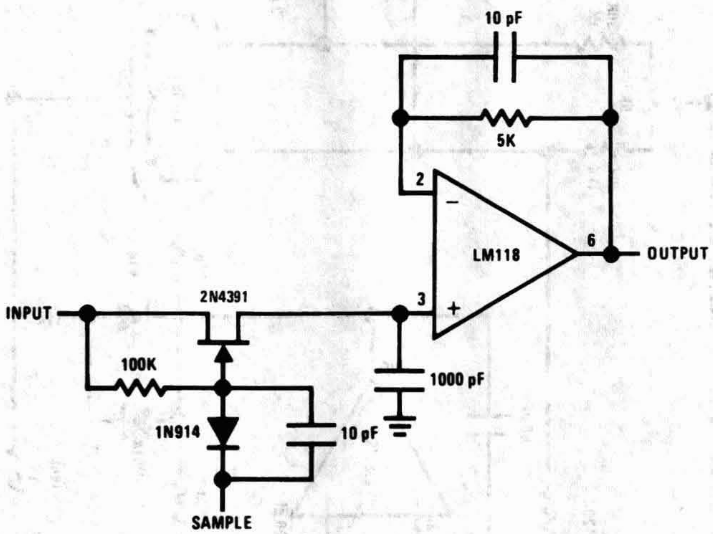
TL/H/7766–15

Differential Amplifier


10K
10K
INPUT
2
LM118
6
OUTPUT
10K
INPUT
3
10K

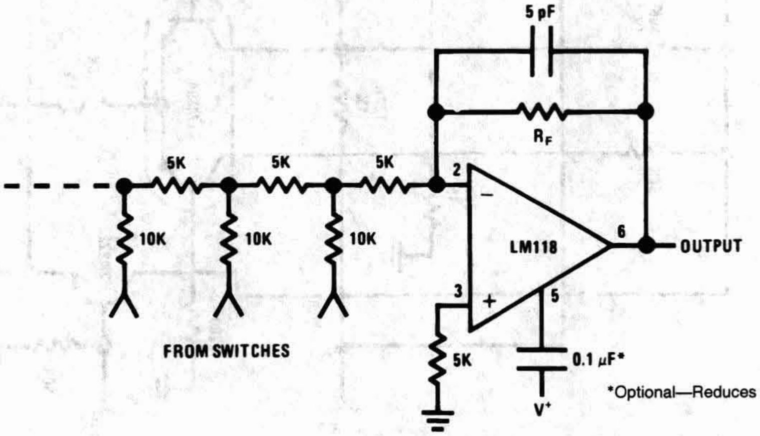
TL/H/7766–16

Fast Sample and Hold


10 pF
5K
2
LM118
6
OUTPUT
INPUT
2N4391
3
100K
1000 pF
1N914
10 pF
SAMPLE

TL/H/7766–18

D/A Converter Using Ladder Network

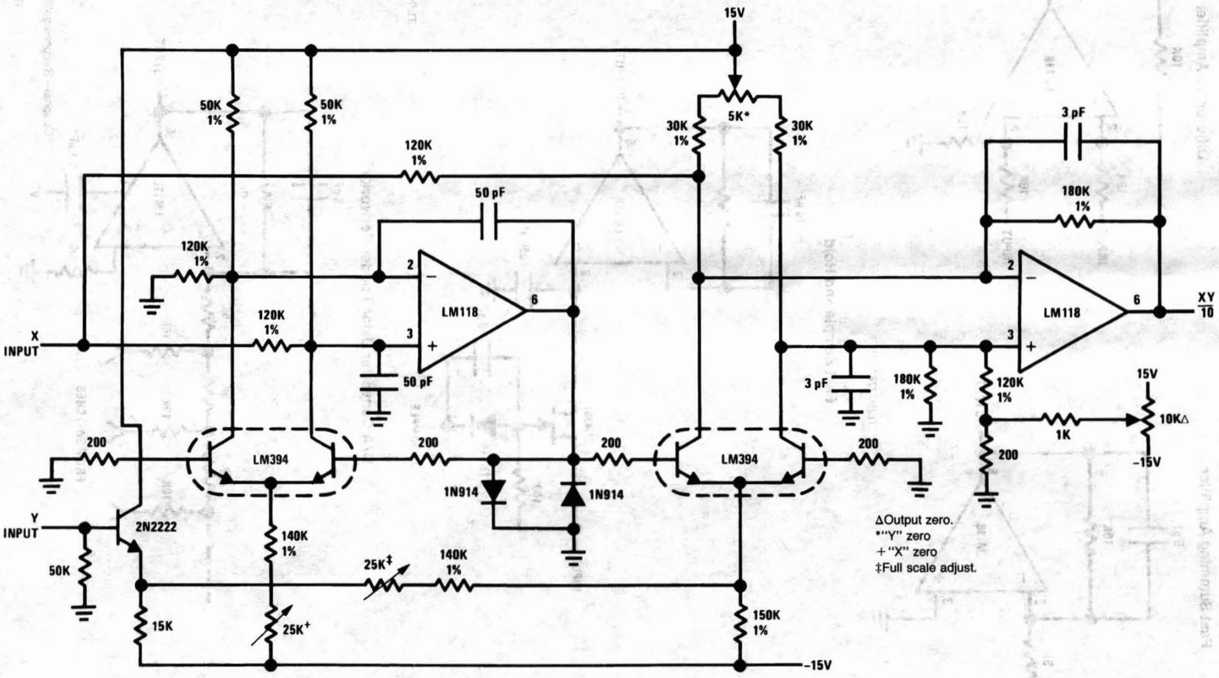

5 pF
R$_F$
5K
5K
5K
2
10K
10K
10K
LM118
6
OUTPUT
3
5
FROM SWITCHES
5K
0.1 µF*
V$^+$

*Optional—Reduces settling time.

TL/H/7766–19

Typical Applications (Continued)

Four Quadrant Multiplier

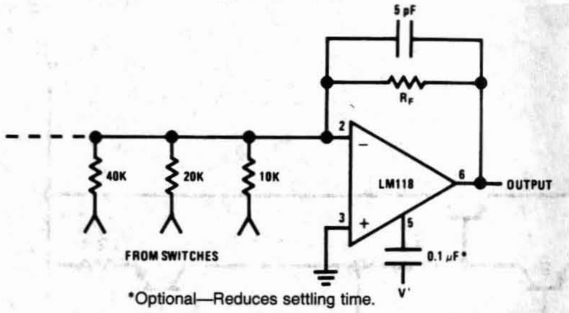

15V
5K*
30K 1%
30K 1%
50K 1%
50K 1%
120K 1%
50 pF
120K 1%
120K 1%
X INPUT
LM118
2
3
6
50 pF
200
LM394
200
1N914
1N914
200
LM394
200
Y INPUT
2N2222
50K
140K 1%
25K‡
140K 1%
15K
25K+
150K 1%
−15V
3 pF
180K 1%
LM118
2
3
6
XY/10
3 pF
180K 1%
120K 1%
200
1K
15V
10KΔ
−15V

ΔOutput zero.
*"Y" zero
+"X" zero
‡Full scale adjust.

TL/H/7766–17

Typical Applications (Continued)

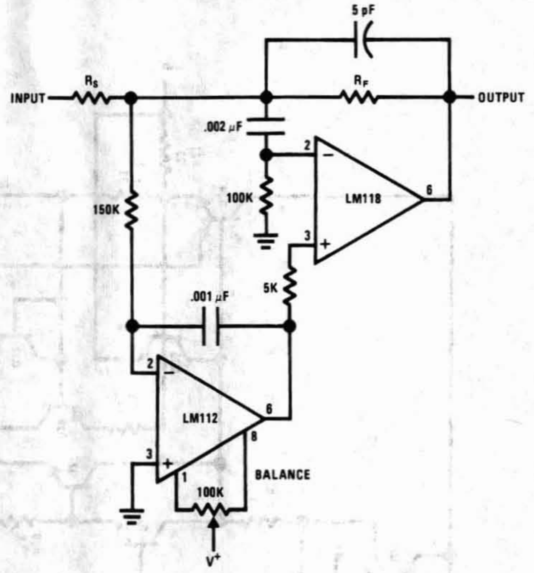
D/A Converter Using Binary Weighted Network


5 pF
R_F
2
40K
20K
10K
LM118
6
OUTPUT
3
5
FROM SWITCHES
0.1 μF*
V⁻

*Optional—Reduces settling time.

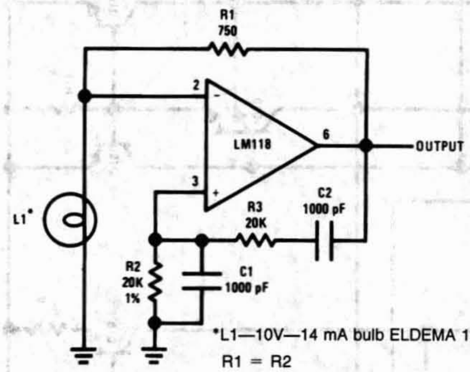
TL/H/7766-20

Fast Summing Amplifier with Low Input Current


5 pF
R_S
R_F
INPUT
OUTPUT
.002 μF
2
100K
LM118
6
150K
3
5K
.001 μF
2
LM112
6
8
3
1
100K
BALANCE
V⁺

TL/H/7766-21

Wein Bridge Sine Wave Oscillator


R1
750
2
LM118
6
OUTPUT
3
L1*
R3
20K
C2
1000 pF
R2
20K
1%
C1
1000 pF

*L1—10V—14 mA bulb ELDEMA 1869

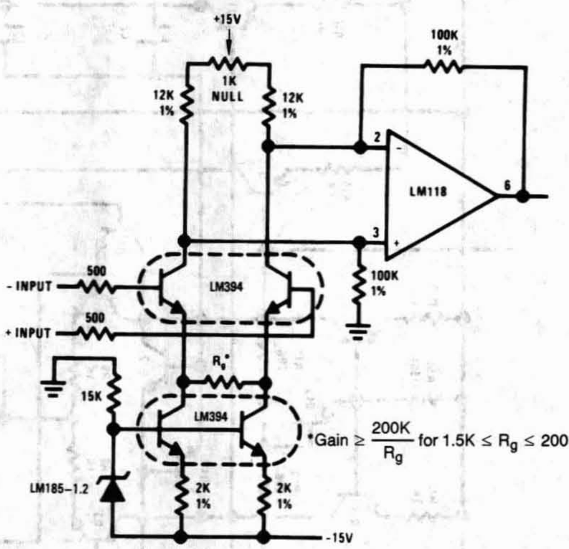
R1 = R2

C1 = C2

$$f = \frac{1}{2\pi R2\, C1}$$

TL/H/7766-22

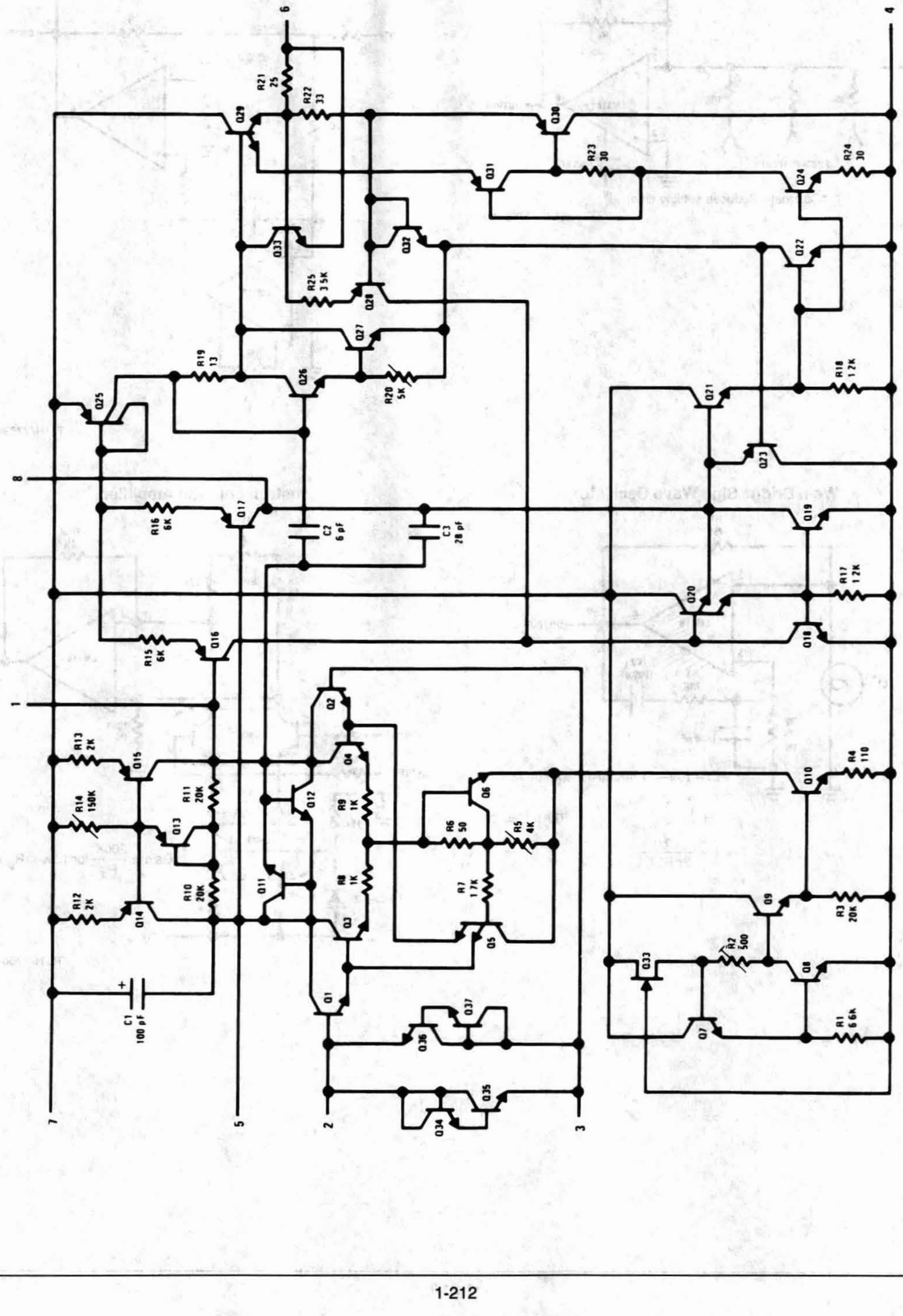
Instrumentation Amplifier


+15V
1K
NULL
12K
1%
12K
1%
100K
1%
2
LM118
6
3
100K
1%
500
- INPUT
LM394
500
+ INPUT
R_g*
15K
LM394
LM185-1.2
2K
1%
2K
1%
-15V

$*\text{Gain} \geq \frac{200K}{R_g}$ for $1.5K \leq R_g \leq 200K$

TL/H/7766-23

Schematic Diagram


6
4
8
1
7
5
2
3
Q29
R21 25
R22 33
Q30
R23 30
Q31
Q24
R24 30
Q33
Q32
Q22
R25 3.5K
Q28
Q27
R19 13
Q26
R20 5K
R18 1.2K
Q21
Q25
Q23
R16 6K
Q17
C2 6 pF
C3 28 pF
Q19
R17 1.2K
Q20
Q18
R15 6K
Q16
Q2
R13 2K
Q15
Q4
R14 150K
Q12
R11 20K
Q13
R9 1K
Q6
R6 50
R5 4K
R4 110
Q10
R12 2K
R10 20K
Q11
R8 1K
R7 1.7K
Q14
Q3
Q5
Q9
R3 20K
R2 500
Q33
Q8
C1 100 pF
Q1
Q37
Q36
Q7
R1 6.6k
Q35
Q34

TL/H/7766–1

National Semiconductor

LM124/LM224/LM324/LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

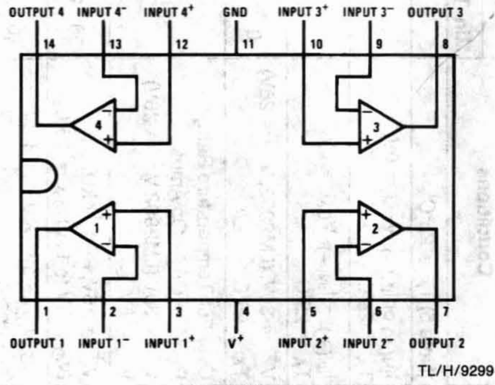
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3V to 32V
  - or dual supplies ±1.5V to ±16V
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current 45 nA (temperature compensated)
- Low input offset voltage 2 mV and offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to $V^+ - 1.5V$

Connection Diagram

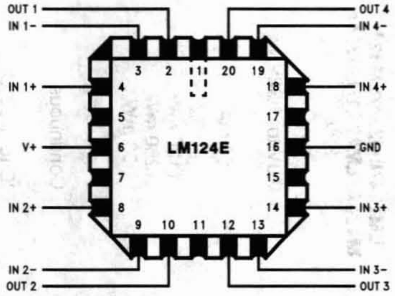
Dual-In-Line Package


OUTPUT 4
INPUT 4⁻
INPUT 4⁺
GND
INPUT 3⁺
INPUT 3⁻
OUTPUT 3
14
13
12
11
10
9
8
4
3
1
2
1
2
3
4
5
6
7
OUTPUT 1
INPUT 1⁻
INPUT 1⁺
V⁺
INPUT 2⁺
INPUT 2⁻
OUTPUT 2

TL/H/9299-1

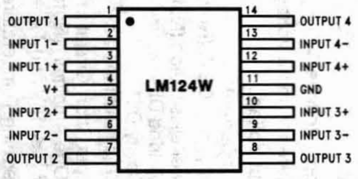
Top View

Order Number LM124J, LM124AJ, LM124J/883, LM124AJ/883*, LM224J, LM224AJ, LM324J, LM324M, LM324AM, LM2902M, LM324N, LM324AN or LM2902N See NS Package Number J14A, M14A or N14A**


OUT 1
IN 1−
IN 1+
V+
IN 2+
IN 2−
OUT 2
OUT 4
IN 4−
IN 4+
GND
IN 3+
IN 3−
OUT 3
3
2
1
20
19
4
18
5
17
6
LM124E
16
7
15
8
14
9
10
11
12
13

TL/H/9299-32

Order Number LM124AE/883 or LM124E/883 See NS Package Number E20A


OUTPUT 1
INPUT 1−
INPUT 1+
V+
INPUT 2+
INPUT 2−
OUTPUT 2
1
2
3
4
5
6
7
LM124W
14
13
12
11
10
9
8
OUTPUT 4
INPUT 4−
INPUT 4+
GND
INPUT 3+
INPUT 3−
OUTPUT 3

TL/H/9299-33

Order Number LM124AW/883 or LM124W/883 See NS Package Number W14B

*LM124A available per JM38510/11006
**LM124 available per JM38510/11005

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0V$, (Note 4), unless otherwise stated

Parameter	Conditions	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5) $T_A = 25°C$		1	2		1	3		2	3		2	5		2	7		2	7	mV
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		2	15		5	30		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30V$, (LM2902, $V^+ = 26V$), $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps $V^+ = 30V$ (LM2902 $V^+ = 26V$) $V^+ = 5V$		1.5 0.7	3 1.2		1.5 0.7	3 1.2		1.5 0.7	3 1.2		1.5 0.7	3 1.2		1.5 0.7	3 1.2		1.5 0.7	3 1.2	mA
Large Signal Voltage Gain	$V^+ = 15V$, $R_L \geq 2\ k\Omega$, ($V_O = 1V$ to $11V$), $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5V$, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	85		50	70		dB
Power Supply Rejection Ratio	$V^+ = 5V$ to $30V$ (LM2902, $V^+ = 5V$ to $26V$), $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB

Electrical Characteristics $V^+ = +5.0V$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions		LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Amplifier-to-Amplifier Coupling (Note 8)		f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)			−120			−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1V, V_{IN}^- = 0V,$ $V^+ = 15V, V_O = 2V, T_A = 25°C$		20	40		20	40		20	40		20	40		20	40		20	40		mA
	Sink	$V_{IN}^- = 1V, V_{IN}^+ = 0V,$ $V^+ = 15V, V_O = 2V, T_A = 25°C$		10	20		10	20		10	20		10	20		10	20		10	20		
		$V_{IN}^- = 1V, V_{IN}^+ = 0V,$ $V^+ = 15V, V_O = 200\ mV, T_A = 25°C$		12	50		12	50		12	50		12	50		12	50		12	50		μA
Short Circuit to Ground		(Note 2) $V^+ = 15V, T_A = 25°C$			40	60		40	60		40	60		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 5)				4			4			5			7			9			10	mV
Input Offset Voltage Drift		$R_S = 0\Omega$			7	20		7	20		7	30		7			7			7		μV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}, V_{CM} = 0V$				30			30			75			100			150		45	200	nA
Input Offset Current Drift		$R_S = 0\Omega$			10	200		10	200		10	300		10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	100		40	100		40	200		40	300		40	500		40	500	nA
Input Common-Mode Voltage Range (Note 7)		$V^+ = +30V$ (LM2902, $V^+ = 26V$)		0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V
Large Signal Voltage Gain		$V^+ = +15V$ (V_O Swing = 1V to 11V) $R_L \geq 2\ k\Omega$		25			25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = 30V$ (LM2902, $V^+ = 26V$)	$R_L = 2\ k\Omega$	26			26			26			26			26			22			V
			$R_L = 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		
	V_{OL}	$V^+ = 5V, R_L = 10\ k\Omega$			5	20		5	20		5	20		5	20		5	20		5	100	mV

Electrical Characteristics $V^+ = +5.0V$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions		LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Current	Source	$V_O = 2V$	$V_{IN}^+ = +1V$, $V_{IN}^- = 0V, V^+ = 15V$	10	20		10	20		10	20		10	20		10	20		10	20		mA
	Sink		$V_{IN}^- = +1V$, $V_{IN}^+ = 0V, V^+ = 15V$	10	15		5	8		5	8		5	8		5	8		5	8		

Note 1: For operating at high temperatures, the LM324/LM324A/LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2902 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$) for LM2902, V^+ from 5V to 26V.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

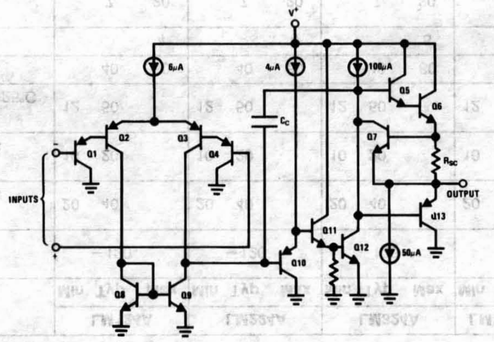
Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2902), independent of the magnitude of V^+.

Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

Note 10: Human body model, 1.5 kΩ in series with 100 pF.

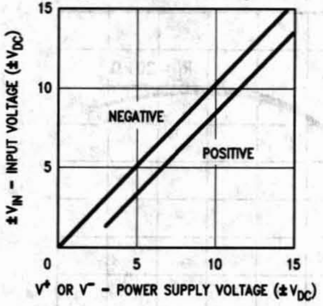
Schematic Diagram (Each Amplifier)



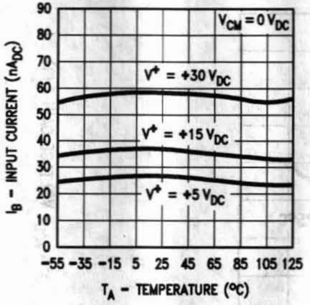
TL/H/9299-2

Typical Performance Characteristics

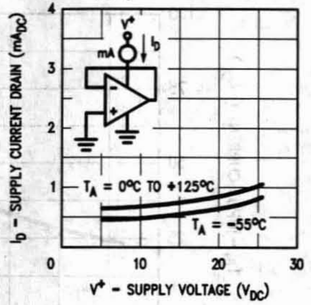
Input Voltage Range



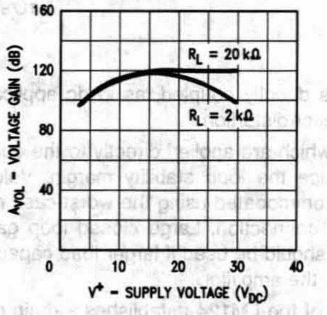
Input Current



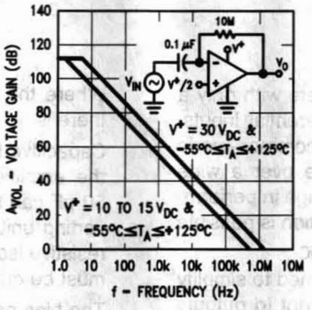
Supply Current



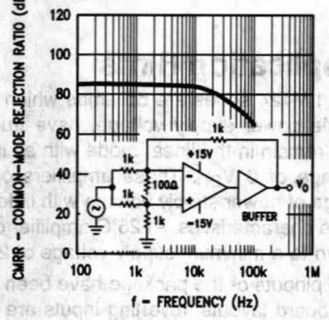
Voltage Gain



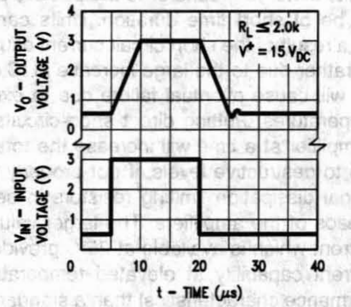
Open Loop Frequency Response



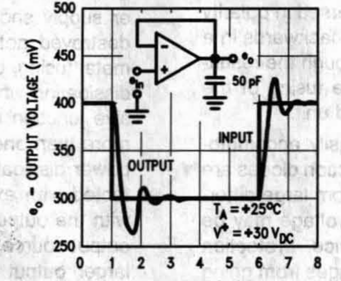
Common Mode Rejection Ratio



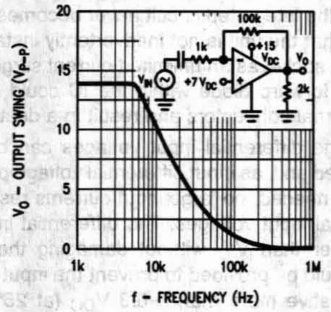
Voltage Follower Pulse Response



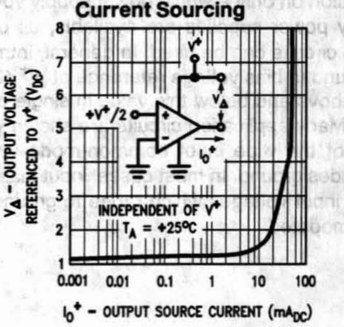
Voltage Follower Pulse Response (Small Signal)



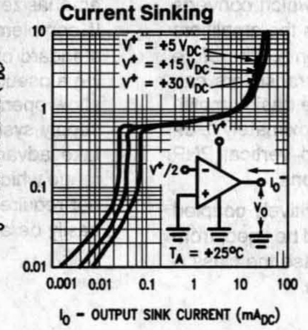
Large Signal Frequency Response



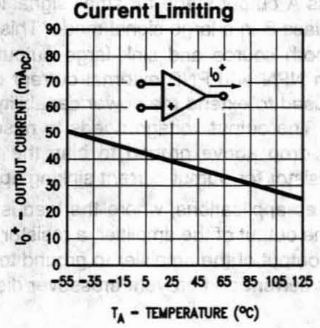
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

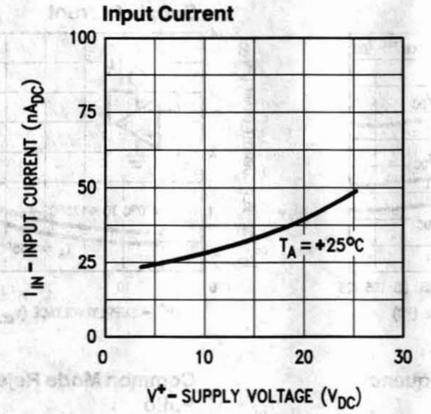


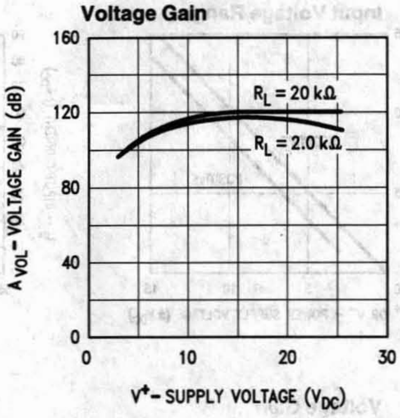
Current Limiting



TL/H/9299–3

Typical Performance Characteristics (LM2902 only)


Input Current


Voltage Gain

TL/H/9299–4

Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

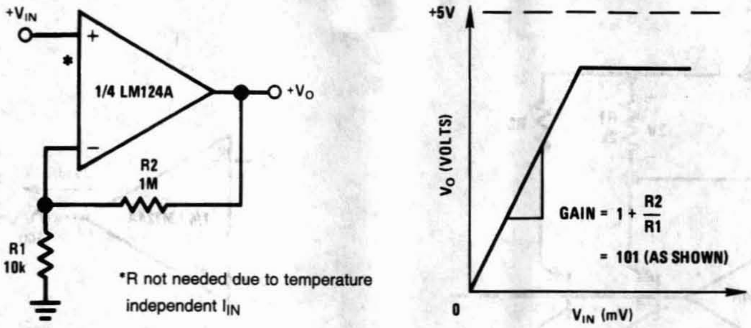
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

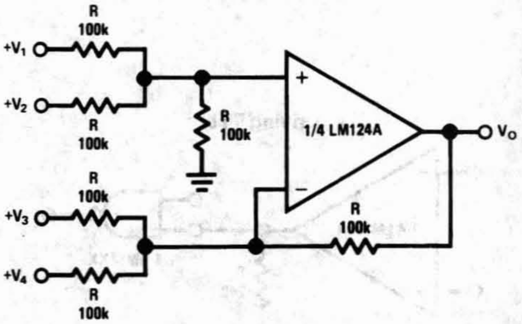


$+V_{IN}$
*
1/4 LM124A
$+V_O$
R2
1M
R1
10k
+5V
V_O (VOLTS)
0
V_{IN} (mV)
GAIN = $1 + \frac{R2}{R1}$
= 101 (AS SHOWN)

*R not needed due to temperature independent I_{IN}

TL/H/9299–5

DC Summing Amplifier
(V_{IN}'S ≥ 0 V_{DC} and V_O ≥ V_{DC})

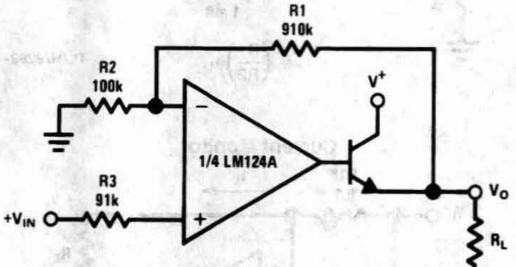


R
100k
$+V_1$
$+V_2$
R
100k
R
100k
R
100k
$+V_3$
$+V_4$
R
100k
1/4 LM124A
V_O
R
100k

TL/H/9299–6

Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier

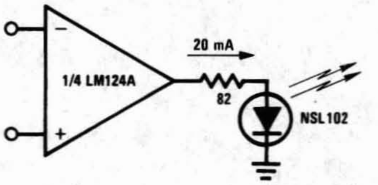


R1
910k
R2
100k
V^+
1/4 LM124A
R3
91k
$+V_{IN}$
V_O
R_L

$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$
$A_V = 10$

TL/H/9299–7

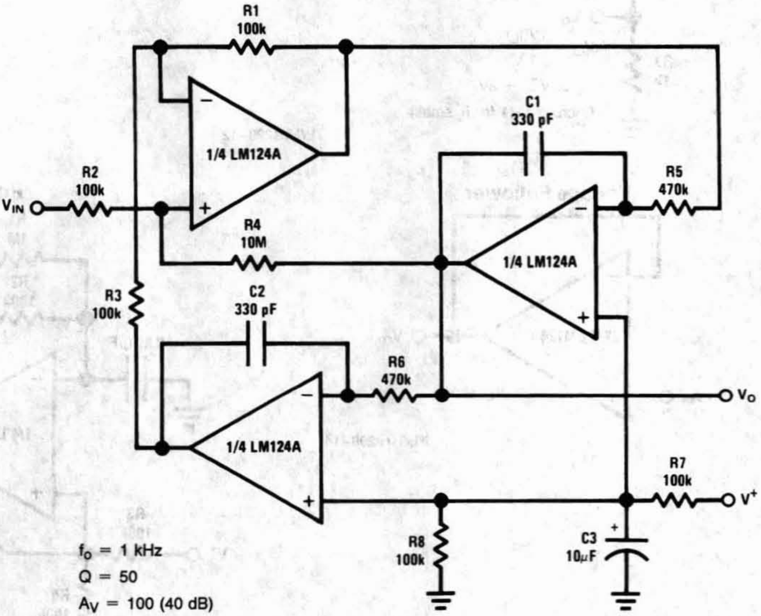
LED Driver



1/4 LM124A
20 mA
82
NSL102

TL/H/9299–8

"BI-QUAD" RC Active Bandpass Filter



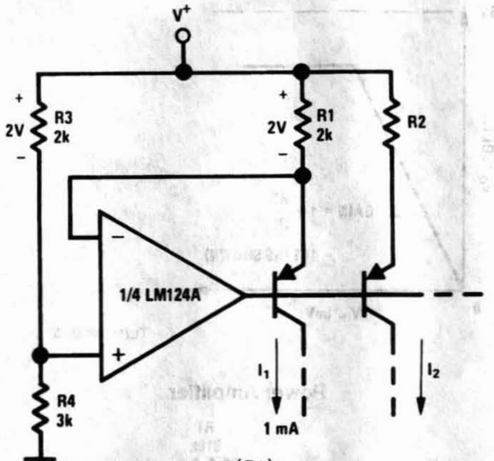
R1
100k
1/4 LM124A
C1
330 pF
R5
470k
R2
100k
V_{IN}
R4
10M
1/4 LM124A
R3
100k
C2
330 pF
R6
470k
V_O
1/4 LM124A
R7
100k
V^+
R8
100k
C3
10µF

f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

TL/H/9299–9

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

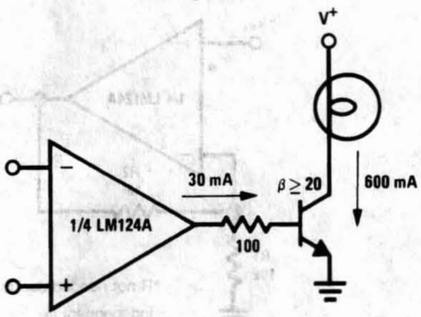
Fixed Current Sources


V+
+
R3
2k
2V
–
+
R1
2k
2V
–
R2
1/4 LM124A
–
+
R4
3k
I1
1 mA
I2

$I_2 = \left(\frac{R1}{R2}\right) I_1$

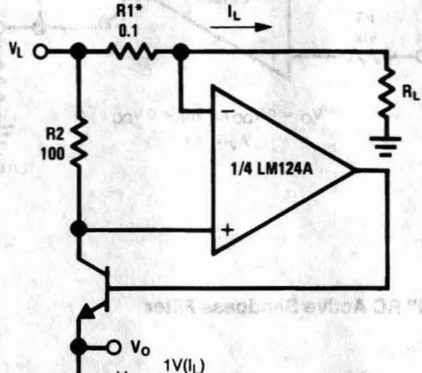
TL/H/9299–10

Lamp Driver


V+
–
+
1/4 LM124A
30 mA
100
β ≥ 20
600 mA

TL/H/9299–11

Current Monitor


R1*
0.1
IL
VL
RL
R2
100
1/4 LM124A
–
+
VO
R3
1k

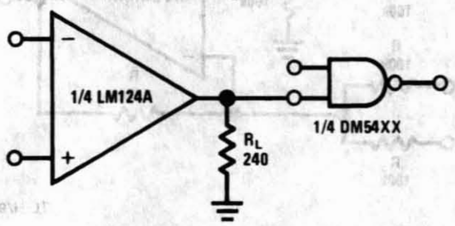
$V_O = \frac{1V(I_L)}{1A}$

$V_L \leq V^+ - 2V$

*(Increase R1 for I_L small)

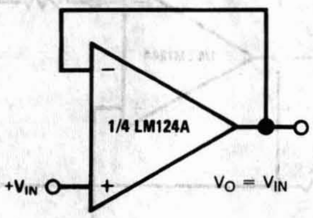
TL/H/9299–12

Driving TTL


–
+
1/4 LM124A
RL
240
1/4 DM54XX

TL/H/9299–13

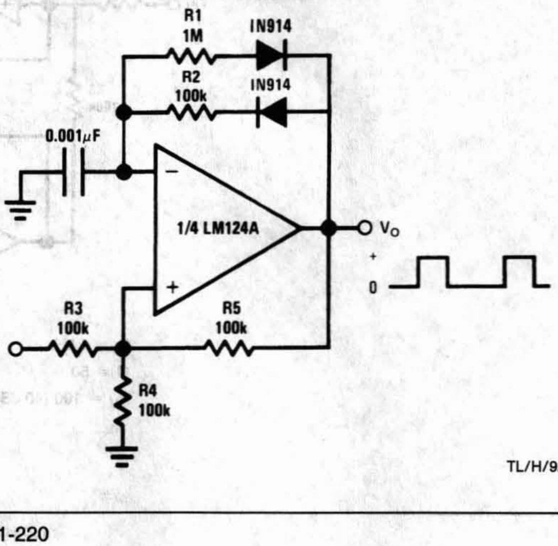
Voltage Follower


–
+
1/4 LM124A
VO
+VIN

$V_O = V_{IN}$

TL/H/9299–14

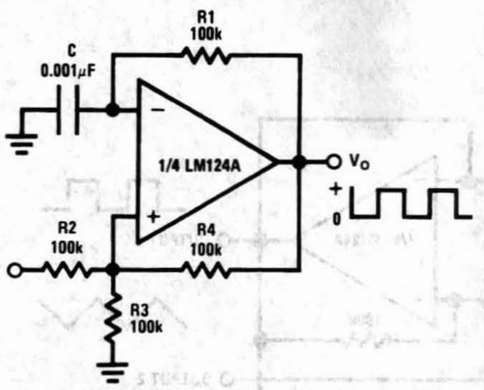
Pulse Generator


R1
1M
IN914
R2
100k
IN914
0.001µF
–
+
1/4 LM124A
VO
+
0
R3
100k
V+
R5
100k
R4
100k

TL/H/9299–15

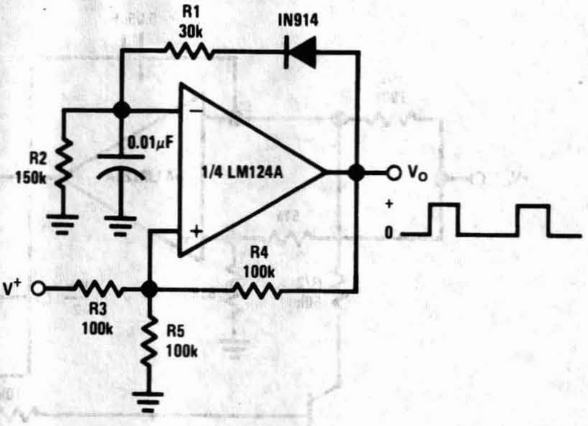
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Squarewave Oscillator


R1
100k
C
0.001μF
1/4 LM124A
V_O
+
0
R2
100k
R4
100k
V+
R3
100k

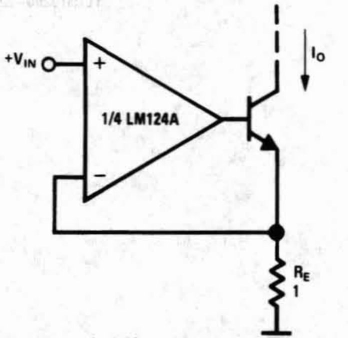
TL/H/9299-16

Pulse Generator


R1
30k
IN914
R2
150k
0.01μF
1/4 LM124A
V_O
+
0
R4
100k
V+
R3
100k
R5
100k

TL/H/9299-17

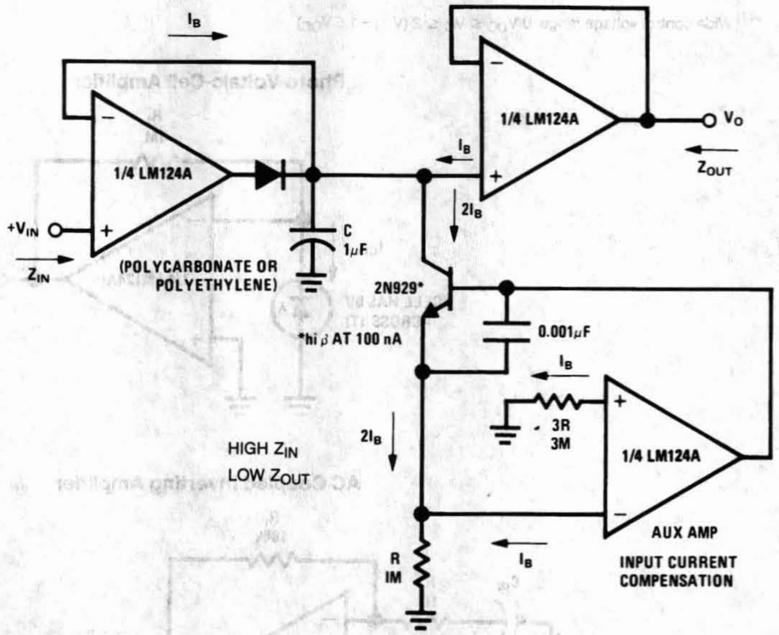
High Compliance Current Sink


I_O
$+V_{IN}$
1/4 LM124A
R_E
1

I_O = 1 amp/volt V_{IN}
(Increase R_E for I_o small)

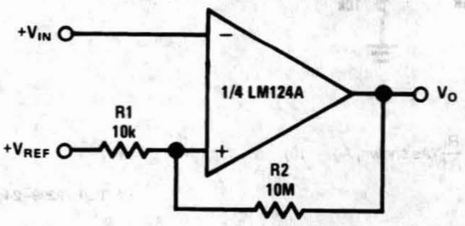
TL/H/9299-18

Low Drift Peak Detector


I_B
1/4 LM124A
V_O
I_B
Z_{OUT}
1/4 LM124A
$+V_{IN}$
Z_{IN}
$2I_B$
C
1μF
(POLYCARBONATE OR
POLYETHYLENE)
2N929*
*hi β AT 100 nA
0.001μF
I_B
3R
3M
1/4 LM124A
HIGH Z_{IN}
LOW Z_{OUT}
$2I_B$
R
IM
I_B
AUX AMP
INPUT CURRENT
COMPENSATION

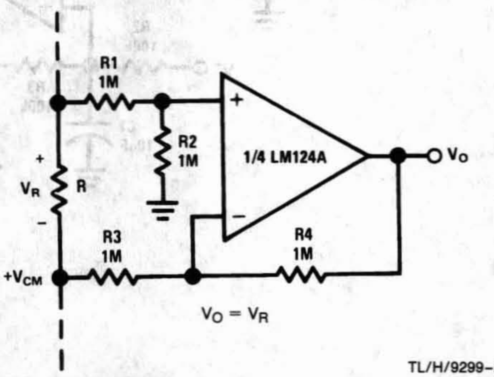
TL/H/9299-19

Comparator with Hysteresis


$+V_{IN}$
1/4 LM124A
V_O
R1
10k
$+V_{REF}$
R2
10M

TL/H/9299-20

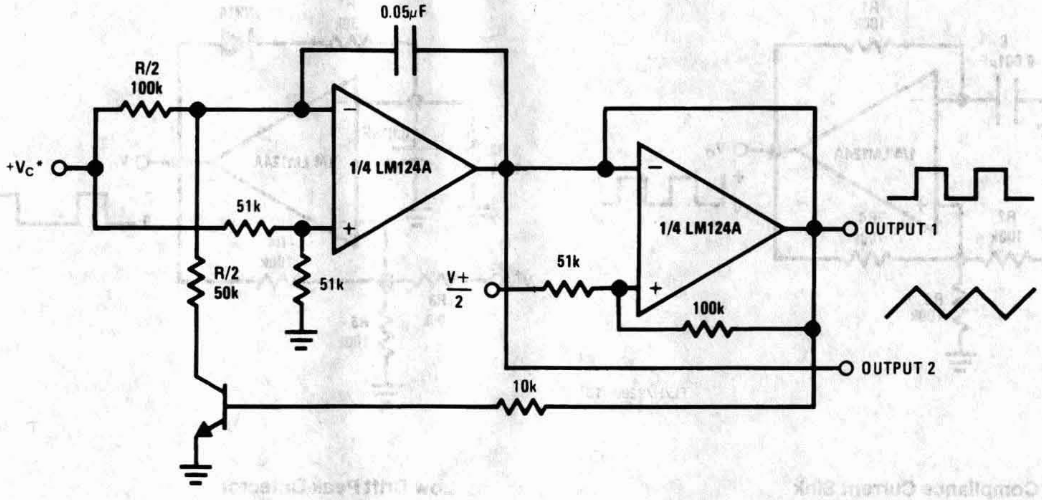
Ground Referencing a Differential Input Signal


R1
1M
R2
1M
1/4 LM124A
V_O
+
V_R
R
−
R3
1M
R4
1M
$+V_{CM}$
$V_O = V_R$

TL/H/9299-21

Typical Single-Supply Applications ($V^{+} = 5.0\ V_{DC}$) (Continued)

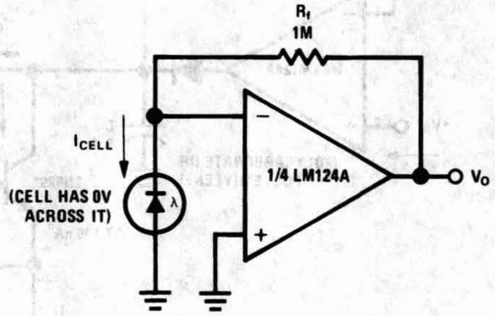
Voltage Controlled Oscillator Circuit


0.05μF
R/2
100k
+V_C*
51k
1/4 LM124A
R/2
50k
51k
V+/2
51k
1/4 LM124A
100k
OUTPUT 1
OUTPUT 2
10k

TL/H/9299-22

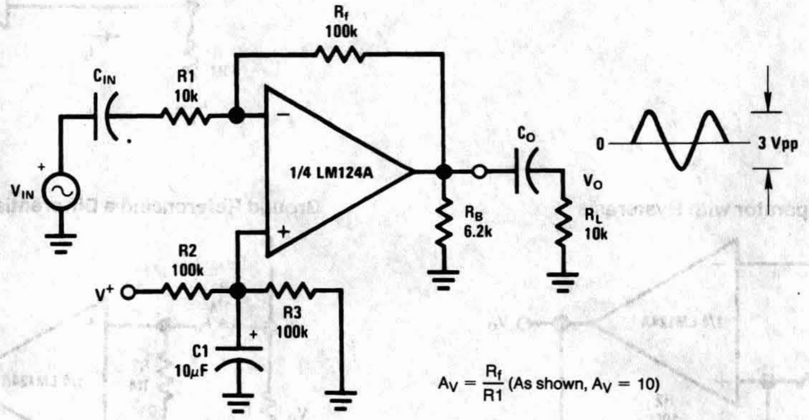
*Wide control voltage range: $0\ V_{DC} \leq V_C \leq 2\ (V^{+} - 1.5\ V_{DC})$

Photo Voltaic-Cell Amplifier


R_f
1M
I_CELL
(CELL HAS 0V ACROSS IT)
λ
1/4 LM124A
V_O

TL/H/9299-23

AC Coupled Inverting Amplifier

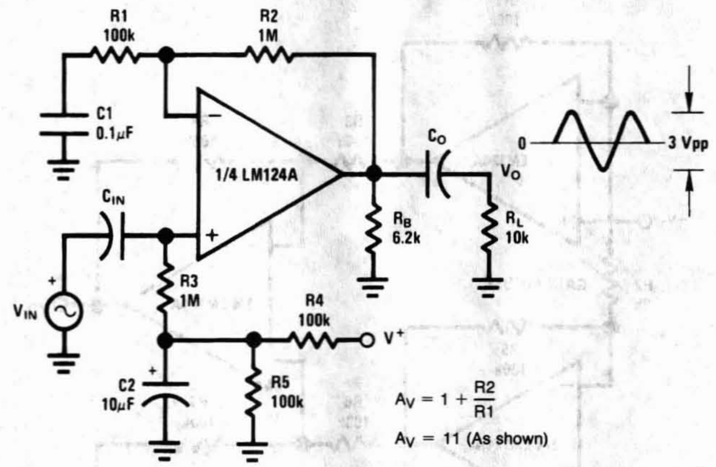

R_f
100k
C_IN
R1
10k
V_IN
1/4 LM124A
C_O
V_O
R_B
6.2k
R_L
10k
0
3 Vpp
R2
100k
V+
R3
100k
C1
10μF

$A_V = \frac{R_f}{R1}$ (As shown, $A_V = 10$)

TL/H/9299-24

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

AC Coupled Non-Inverting Amplifier

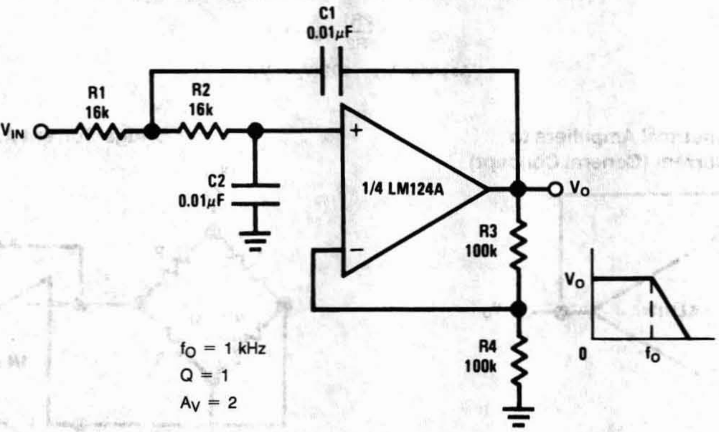

R1
100k
R2
1M
C1
0.1μF
1/4 LM124A
C_O
0
3 Vpp
V_O
C_{IN}
R_B
6.2k
R_L
10k
R3
1M
V_{IN}
R4
100k
V^+
C2
10μF
R5
100k

$A_V = 1 + \frac{R2}{R1}$

$A_V = 11$ (As shown)

TL/H/9299–25

DC Coupled Low-Pass RC Active Filter


C1
0.01μF
R1
16k
R2
16k
V_{IN}
C2
0.01μF
1/4 LM124A
V_O
R3
100k
R4
100k
V_O
0
f_O

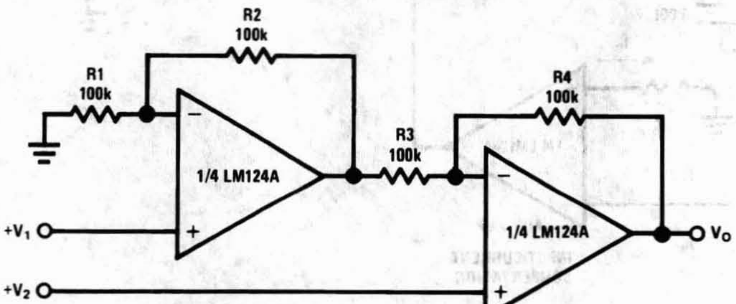
$f_O = 1$ kHz

$Q = 1$

$A_V = 2$

TL/H/9299–26

High Input Z, DC Differential Amplifier


R2
100k
R1
100k
1/4 LM124A
R3
100k
R4
100k
1/4 LM124A
$+V_1$
$+V_2$
V_O

For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

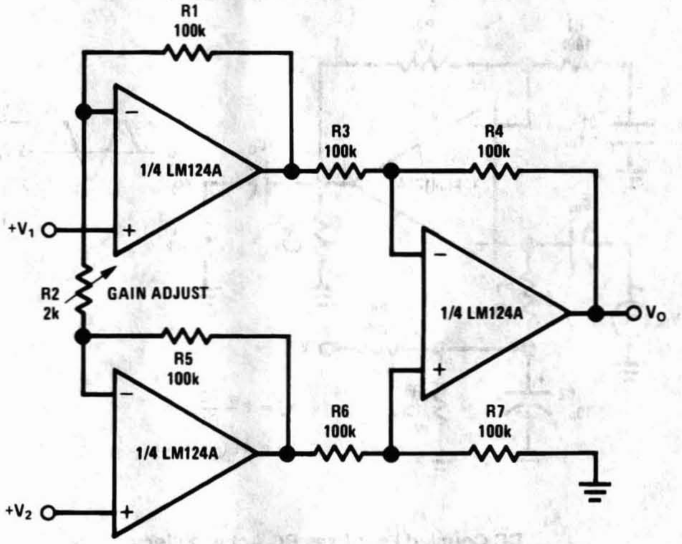
$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

TL/H/9299–27

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

High Input Z Adjustable-Gain DC Instrumentation Amplifier


R1
100k
1/4 LM124A
+V1
R2
2k
GAIN ADJUST
R5
100k
1/4 LM124A
+V2
R3
100k
R4
100k
1/4 LM124A
VO
R6
100k
R7
100k

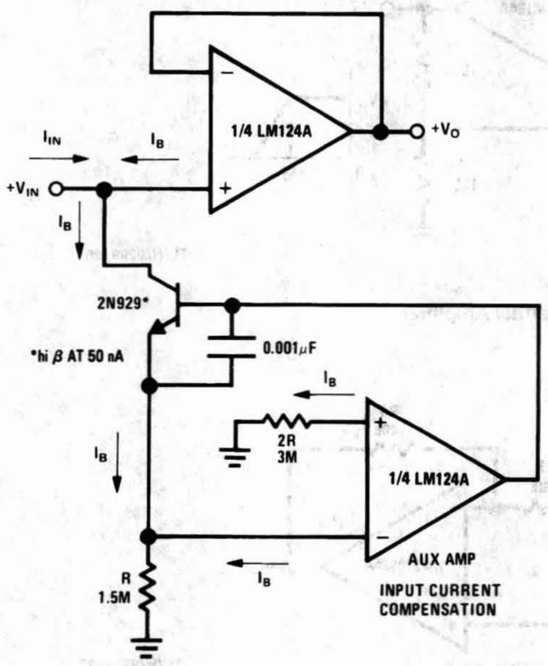
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101\ (V_2 - V_1)$

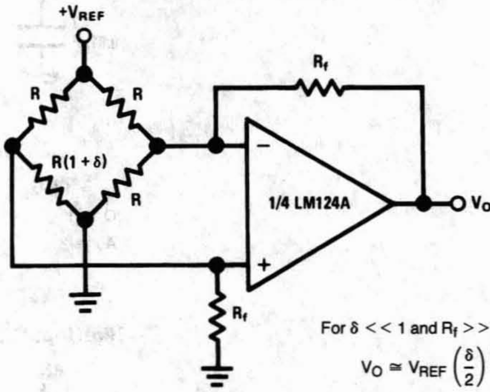
TL/H/9299-28

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)


1/4 LM124A
+VO
IIN
IB
+VIN
IB
2N929*
*hi β AT 50 nA
0.001μF
IB
2R
3M
1/4 LM124A
IB
R
1.5M
IB
AUX AMP
INPUT CURRENT COMPENSATION

TL/H/9299-29

Bridge Current Amplifier


+VREF
R
R
R(1 + δ)
R
Rf
1/4 LM124A
VO
Rf

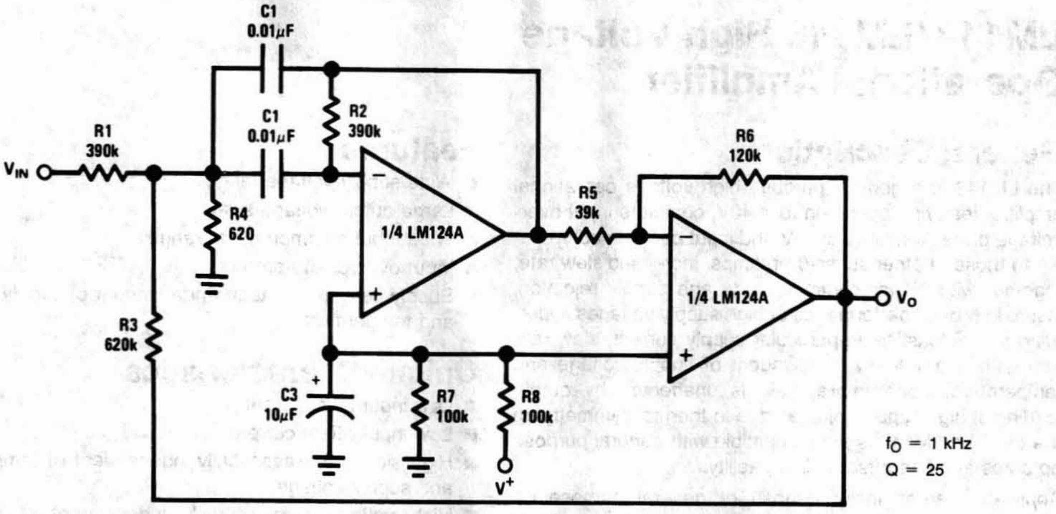
For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

TL/H/9299-30

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Bandpass Active Filter


C1
0.01μF
C1
0.01μF
R2
390k
R1
390k
V_{IN}
R4
620
1/4 LM124A
R5
39k
R6
120k
1/4 LM124A
V_O
R3
620k
C3
10μF
R7
100k
R8
100k
V^+
f_O = 1 kHz
Q = 25

TL/H/9299–31

National Semiconductor

LM143/LM343 High Voltage Operational Amplifier

General Description

The LM143 is a general purpose high voltage operational amplifier featuring operation to ±40V, complete input overvoltage protection up to ±40V and input currents comparable to those of other super-β op amps. Increased slew rate, together with higher common-mode and supply rejection, insure improved performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, gain is unaffected by output loading at high supply voltages due to thermal symmetry on the die. The LM143 is pin compatible with general purpose op amps and has offset null capability.

Application areas include those of general purpose op amps, but can be extended to higher voltages and higher output power when externally boosted. For example, when used in audio power applications, the LM143 provides a power bandwidth that covers the entire audio spectrum. In addition, the LM143 can be reliably operated in environments with large overvoltage spikes on the power supplies, where other internally-compensated op amps would suffer catastrophic failure.

The LM343 is similar to the LM143 for applications in less severe supply voltage and temperature environments.

Features

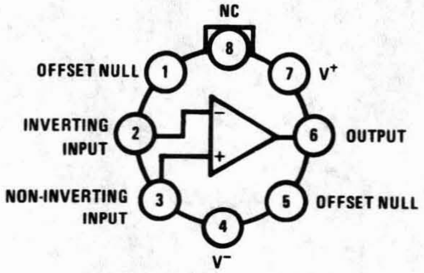
■ Wide supply voltage range	±4.0V to ±40V
■ Large output voltage swing	±37V
■ Wide input common-mode range	±38V
■ Input overvoltage protection	Full ±40V
■ Supply current is virtually independent of supply voltage and temperature	

Unique Characteristics

■ Low input bias current	8.0 nA
■ Low input offset current	1.0 nA
■ High slew rate—essentially independent of temperature and supply voltage	2.5V/μs
■ High voltage gain—virtually independent of resistive loading, temperature, and supply voltage	100k min
■ Internally compensated for unity gain	
■ Output short circuit protection	
■ Pin compatible with general purpose op amps	

Connection Diagram

Metal Can Package
Top View



TL/H/7783–1

Order Number LM143H, LM143H/883* or LM343H
See NS Package Number H08C

*Available per SMD# 7800303

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM143	LM343
Supply Voltage	±40V	±34V
Power Dissipation (Note 1)	680 mW	680 mW
Differential Input Voltage (Note 2)	80V	68V
Input Voltage (Note 2)	±40V	±34V
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Output Short Circuit Duration	5 seconds	5 seconds
Lead Temperature (Soldering, 10 sec.)	300°C	300°C
ESD rating to be determined.		

Electrical Characteristics (Note 3)

Parameter	Conditions	LM143			LM343			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C		2.0	5.0		2.0	8.0	mV
Input Offset Current	T_A = 25°C		1.0	3.0		1.0	10	nA
Input Bias Current	T_A = 25°C		8.0	20		8.0	40	nA
Supply Voltage Rejection Ratio	T_A = 25°C		10	100		10	200	μV/V
Output Voltage Swing	T_A = 25°C, $R_L \geq 5\ k\Omega$	22	25		20	25		V
Large Signal Voltage Gain	T_A = 25°C, $V_{OUT} = \pm 10V$, $R_L \geq 100\ k\Omega$	100k	180k		70k	180k		V/V
Common-Mode Rejection Ratio	T_A = 25°C	80	90		70	90		dB
Input Voltage Range	T_A = 25°C	±24	±26		±22	±26		V
Supply Current (Note 5)	T_A = 25°C		2.0	4.0		2.0	5.0	mA
Short Circuit Current	T_A = 25°C		20			20		mA
Slew Rate	T_A = 25°C, A_V = 1		2.5			2.5		V/μs
Power Bandwidth	T_A = 25°C, V_{OUT} = 40 $V_{p\text{-}p}$, $R_L = 5\ k\Omega$, THD ≤ 1%		20k			20k		Hz
Unity Gain Frequency	T_A = 25°C		1.0M			1.0M		Hz
Input Offset Voltage	T_A = Max T_A = Min			6.0 6.0			10 10	mV
Input Offset Current	T_A = Max T_A = Min		0.8 1.8	4.5 7.0		0.8 1.8	14 14	nA
Input Bias Current	T_A = Max T_A = Min		5.0 16	35 35		5.0 16	55 55	nA
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, T_A = Max $R_L \geq 100\ k\Omega$, T_A = Min	50k 50k	150k 220k		50k 50k	150k 220k		V/V
Output Voltage Swing	$R_L \geq 5.0\ k\Omega$, T_A = Max $R_L \geq 5.0\ k\Omega$, T_A = Min	22 22	26 25		20 20	26 25		V

Note 1: Absolute maximum ratings are not necessarily concurrent, and care must be taken not to exceed the maximum junction temperature of the LM143 (150°C) or the LM343 (100°C). For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 155°C/W, junction to ambient, or 20°C/W, junction to case.

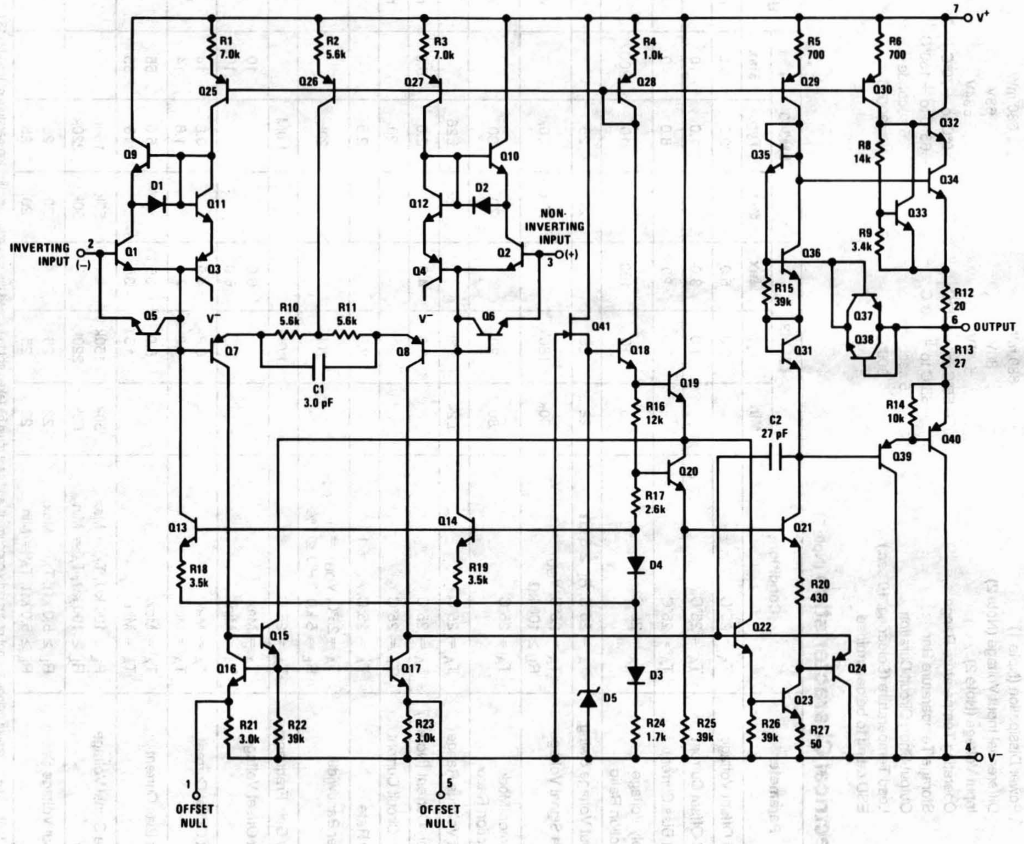
Note 2: For supply voltage less than ±40V for the LM143 and less than ±34V for the LM343, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for V_S = ±28V. For LM143, T_A = max = 125°C and T_A = min = −55°C. For LM343, T_A = max = 70°C and T_A = min = 0°C.

Note 4: Refer to RETS143X for LM143H and LM1536H military specifications.

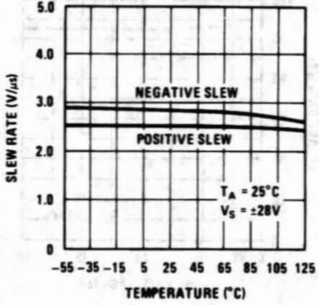
Note 5: The maximum supply currents are guaranteed at V_S = ±40V for the LM143 and V_S = ±34V for the LM343.

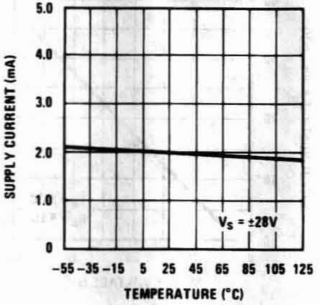
Schematic Diagram

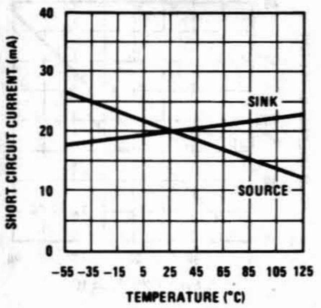

7 V⁺
R1 7.0k
R2 5.6k
R3 7.0k
R4 1.0k
R5 700
R6 700
Q25
Q26
Q27
Q28
Q29
Q30
Q32
Q9
D1
Q11
Q10
D2
Q12
R8 14k
Q35
Q34
Q33
R9 3.4k
INVERTING INPUT 2 (−)
Q1
Q3
NON-INVERTING INPUT 3 (+)
Q2
Q4
Q36
R15 39k
R12 20
6 OUTPUT
Q37
Q38
R13 27
Q5
V⁻
R10 5.6k
R11 5.6k
V⁻
Q6
Q41
Q7
Q8
C1 3.0 pF
Q18
Q31
Q19
R16 12k
R14 10k
C2 27 pF
Q40
Q39
Q20
R17 2.6k
Q13
Q14
Q21
R18 3.5k
R19 3.5k
D4
R20 430
Q22
Q15
Q24
Q16
Q17
D3
Q23
D5
R21 3.0k
R22 39k
R23 3.0k
R24 1.7k
R25 39k
R26 39k
R27 50
4 V⁻
1 OFFSET NULL
5 OFFSET NULL

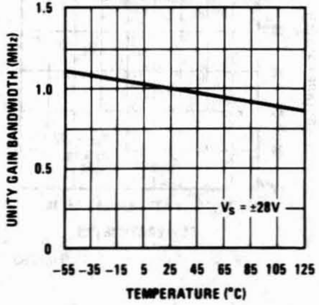
TL/H/7783–2

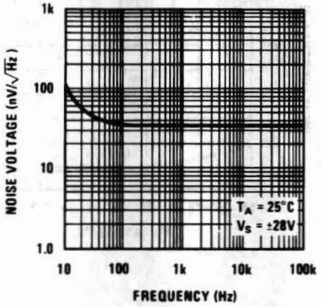
Typical Performance Characteristics

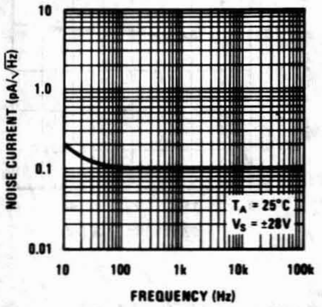

Voltage Follower Slew Rate

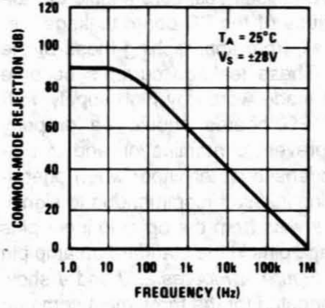

Supply Current

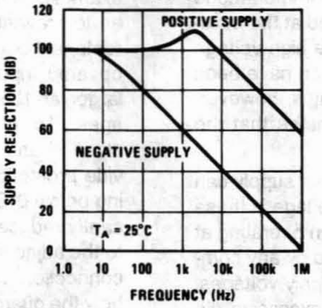

Short Circuit Current

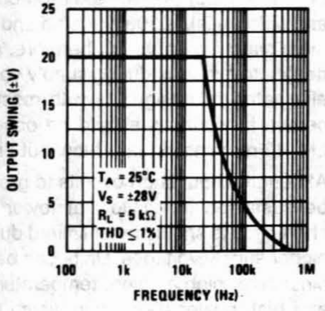

Unity Gain Bandwidth

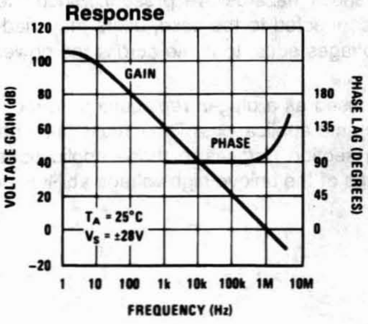

Input Noise Voltage

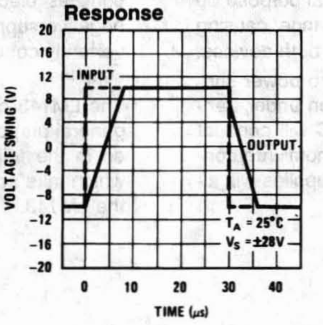

Input Noise Current

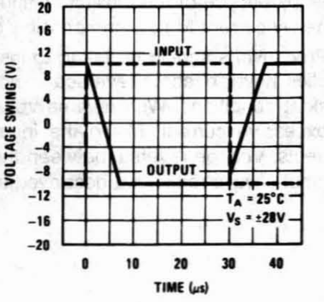

Common-Mode Rejection


Power Supply Rejection


Large Signal Frequency Response


Open Loop Frequency Response

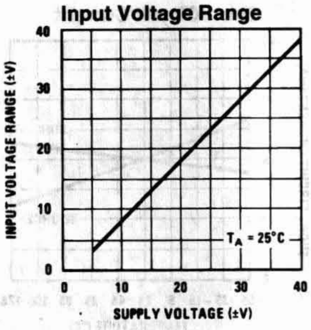

Voltage Follower Pulse Response


Inverter Pulse Response

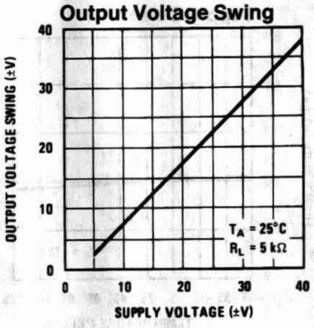
TL/H/7783–4

Typical Performance Characteristics (Continued)

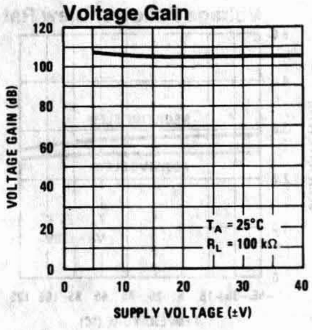
Input Voltage Range



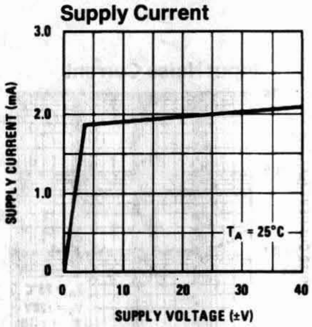
Output Voltage Swing



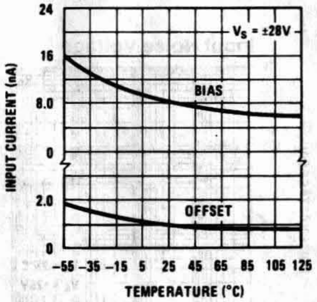
Voltage Gain



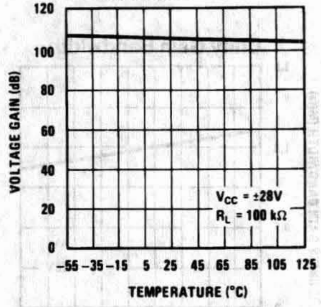
Supply Current



Input Current



Voltage Gain



TL/H/7783–3

Application Hints (See AN-127)

The LM143 is designed for trouble free operation at any supply voltage up to and including the guaranteed maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM143 remains virtually blow-out proof.

Although output short circuits to ground or either supply can be sustained indefinitely at lower supply voltages, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of the maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

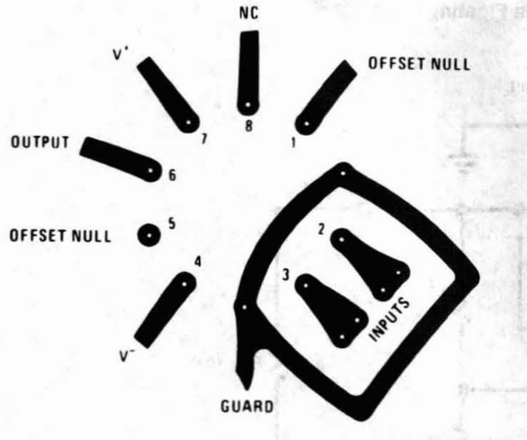
Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltage pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3* and *4* show how the guard ring is connected for the three most common op amp configurations.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.

The LM143 can be used as a plug-in replacement in most general purpose op amp applications. The circuits presented in the following section emphasize those applications which take advantage of the unique high voltage abilities of the LM143.

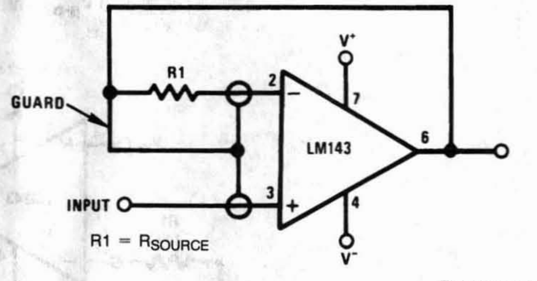
Application Hints (See AN-127) (Continued)


NC
V+
OFFSET NULL
OUTPUT
OFFSET NULL
V-
GUARD
INPUTS
8
7
1
6
5
4
2
3

TL/H/7783-5

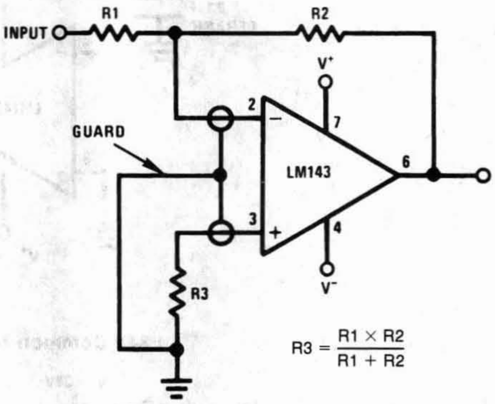
Bottom View

FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package


GUARD
R1
V+
LM143
INPUT
R1 = R_SOURCE
V-
2
3
4
6
7

TL/H/7783-6

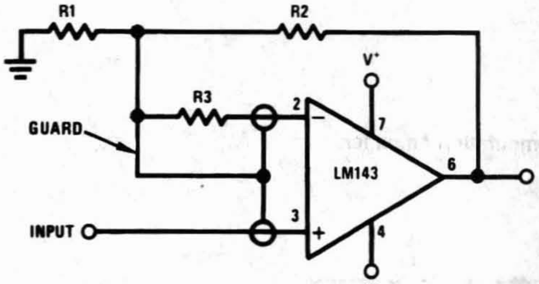
FIGURE 2. Guarded Voltage Follower


INPUT
R1
R2
V+
GUARD
LM143
R3
V-
2
3
4
6
7

$$R3 = \frac{R1 \times R2}{R1 + R2}$$

TL/H/7783-8

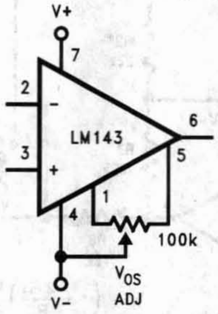
FIGURE 4. Guarded Inverting Amplifier


R1
R2
V+
R3
GUARD
LM143
INPUT
V-
2
3
4
6
7

$$R3 + \frac{R1 \times R2}{R1 + R2} = R_{SOURCE}$$

TL/H/7783-7

FIGURE 3. Guarded Non-Inverting Amplifier

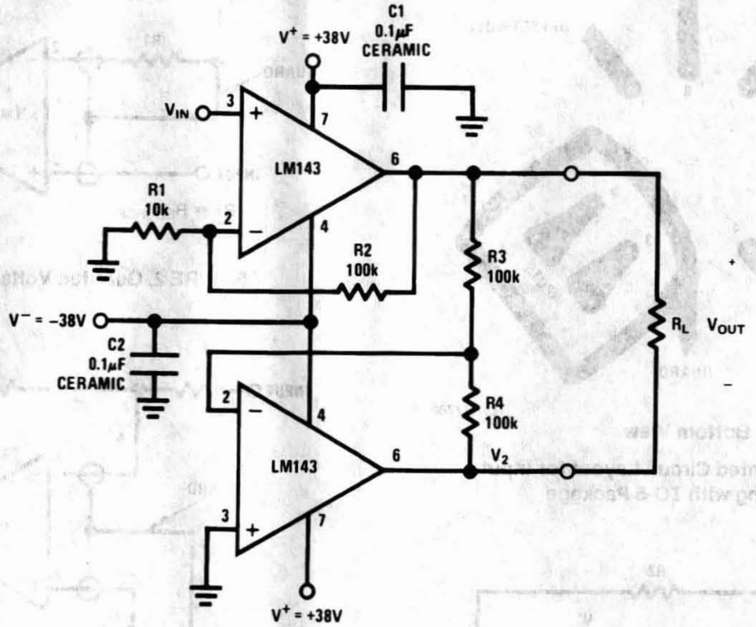

V+
7
2
3
LM143
6
5
1
4
100k
V_OS ADJ
V-

TL/H/7783-14

FIGURE 5. Offset Voltage Adjustment

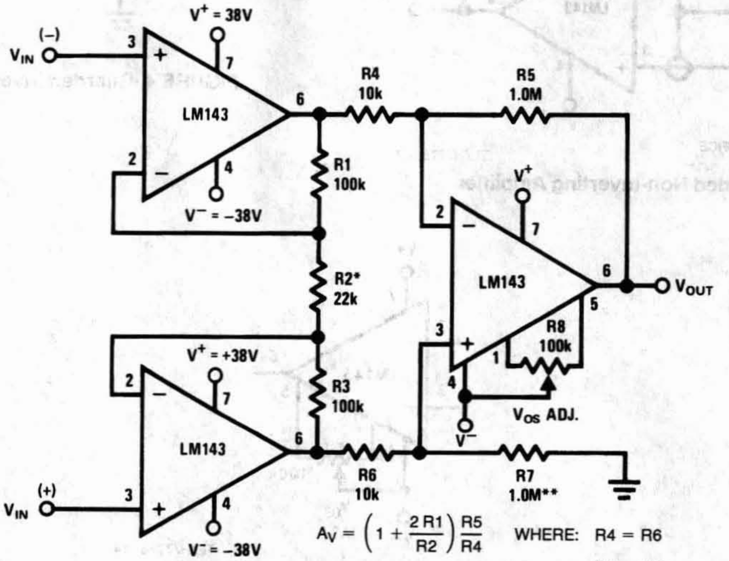
Typical Applications ‡ (For more detail see AN-127)

130 $V_{p\text{-}p}$ Drive Across a Floating Load


C1
0.1µF
CERAMIC
V+ = +38V
VIN
3
7
LM143
6
R1
10k
2
4
R2
100k
R3
100k
V− = −38V
C2
0.1µF
CERAMIC
RL
VOUT
−
R4
100k
2
4
LM143
6
V2
3
7
V+ = +38V

TL/H/7783-9

±34V Common-Mode Instrumentation Amplifier


V+ = 38V
(−)
VIN
3
7
LM143
6
2
4
V− = −38V
R4
10k
R5
1.0M
R1
100k
V+
2
7
LM143
6
VOUT
5
R2*
22k
3
R8
100k
1
V+ = +38V
4
2
7
R3
100k
VOS ADJ.
V−
LM143
6
R6
10k
R7
1.0M**
(+)
VIN
3
4
V− = −38V

$$A_V = \left(1 + \frac{2\,R1}{R2}\right)\frac{R5}{R4} \qquad \text{WHERE: } R4 = R6$$

$$R5 = R7$$

TL/H/7783-10

*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4–R7 for best CMR.

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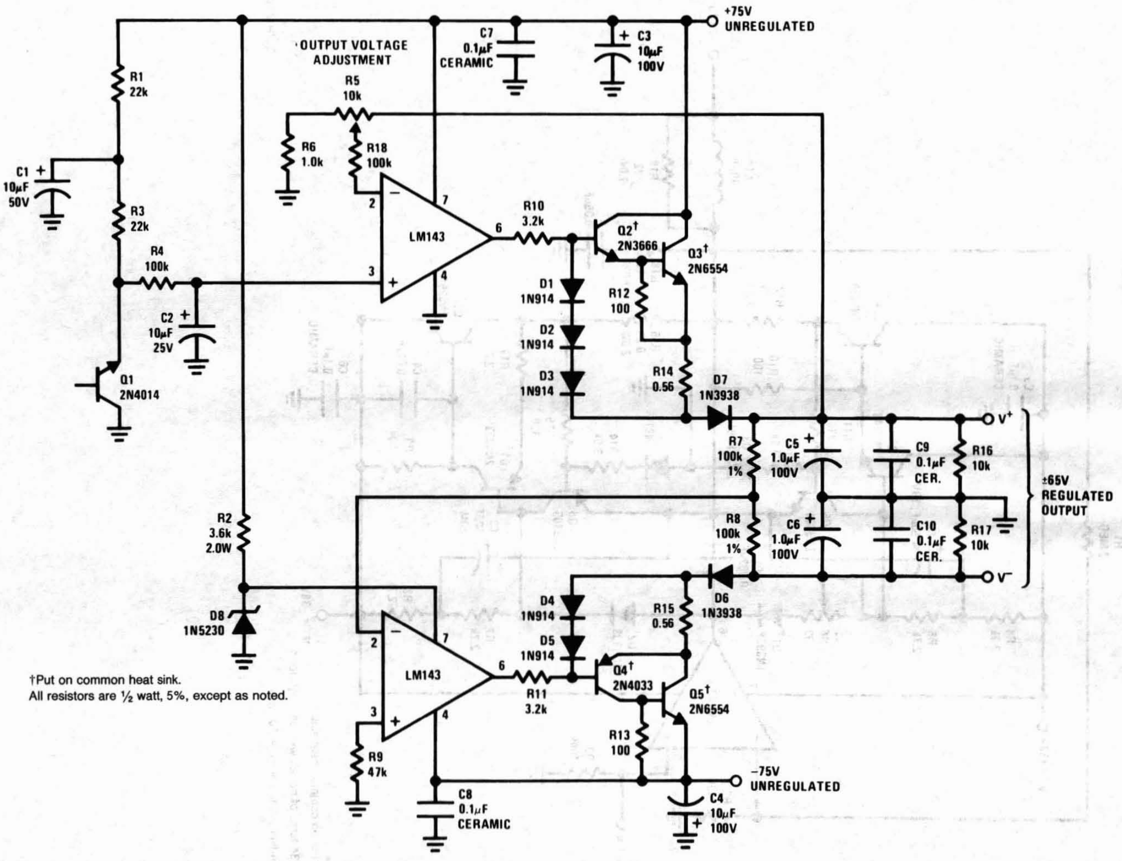
‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

Tracking ±65V, 1 Amp Power Supply with Short Circuit Protection


+75V UNREGULATED
OUTPUT VOLTAGE ADJUSTMENT
C7 0.1μF CERAMIC
C3 10μF 100V
R1 22k
R5 10k
R6 1.0k
R18 100k
C1 10μF 50V
R3 22k
R4 100k
C2 10μF 25V
Q1 2N4014
LM143
R10 3.2k
Q2† 2N3666
Q3† 2N6554
D1 1N914
D2 1N914
D3 1N914
R12 100
R14 0.56
D7 1N3938
V+
R7 100k 1%
C5 1.0μF 100V
C9 0.1μF CER.
R16 10k
±65V REGULATED OUTPUT
R8 100k 1%
C6 1.0μF 100V
C10 0.1μF CER.
R17 10k
V−
R2 3.6k 2.0W
D8 1N5230
D4 1N914
D5 1N914
R15 0.56
D6 1N3938
LM143
R11 3.2k
Q4† 2N4033
Q5† 2N6554
R13 100
R9 47k
C8 0.1μF CERAMIC
−75V UNREGULATED
C4 10μF 100V
2
3
4
6
7

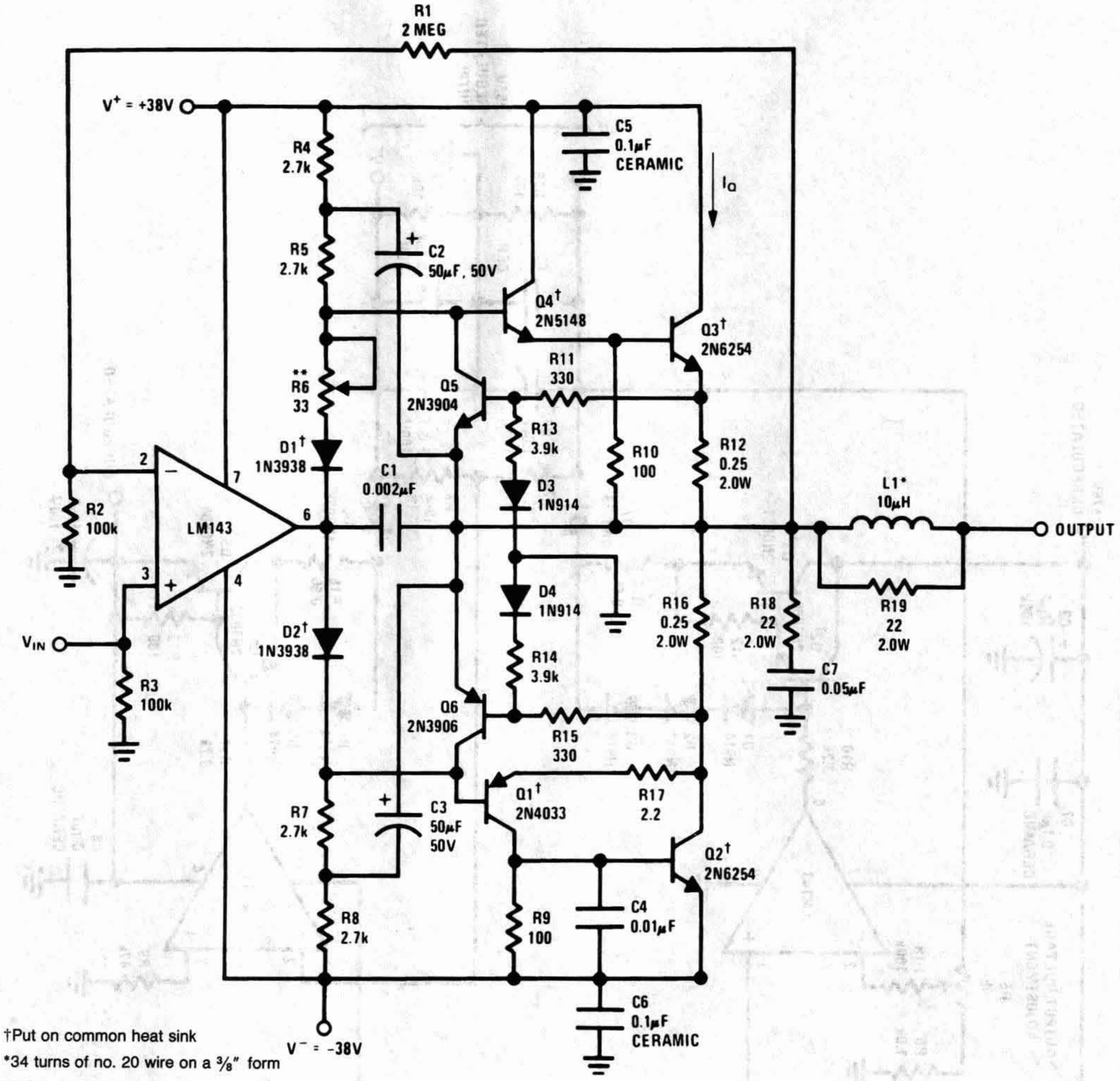
†Put on common heat sink.
All resistors are ½ watt, 5%, except as noted.

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

TL/H/7783–11

Typical Applications ‡ (Continued) (For more detail see AN-127)

90W Audio Power Amplifier with Safe Area Protection


R1
2 MEG
V+ = +38V
R4
2.7k
C5
0.1μF
CERAMIC
IQ
R5
2.7k
C2
50μF, 50V
Q4†
2N5148
Q3†
2N6254
**
R6
33
Q5
2N3904
R11
330
R13
3.9k
R10
100
R12
0.25
2.0W
D1†
1N3938
C1
0.002μF
D3
1N914
L1*
10μH
OUTPUT
2
7
6
3
4
R2
100k
LM143
D4
1N914
R16
0.25
2.0W
R18
22
2.0W
R19
22
2.0W
VIN
D2†
1N3938
R14
3.9k
C7
0.05μF
R3
100k
Q6
2N3906
R15
330
Q1†
2N4033
R17
2.2
R7
2.7k
C3
50μF
50V
Q2†
2N6254
R8
2.7k
R9
100
C4
0.01μF
C6
0.1μF
CERAMIC
V− = −38V

†Put on common heat sink

*34 turns of no. 20 wire on a 3/8″ form

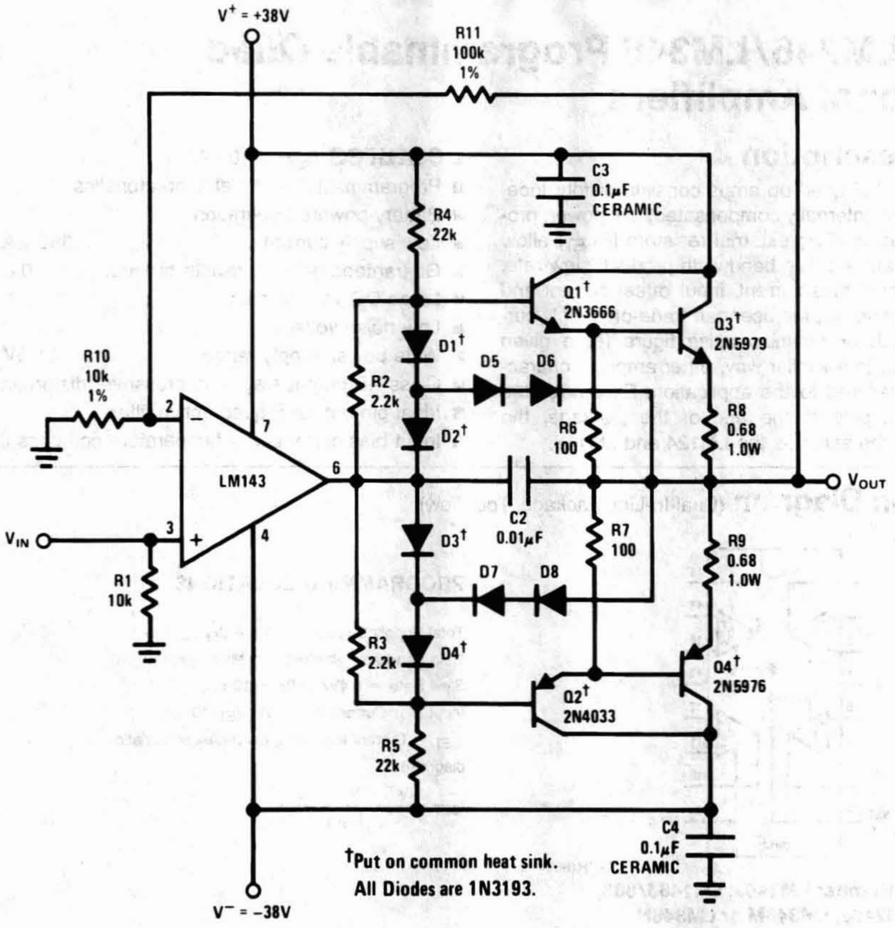
**Adjust R6 to set I_Q = 100 mA

TL/H/7783-12

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

Typical Applications ‡ (Continued) (For more detail see AN-127)

1 Amp Power Amplifier with Short Circuit Protection


V+ = +38V
R11
100k
1%
C3
0.1µF
CERAMIC
R4
22k
Q1†
2N3666
Q3†
2N5979
D1†
R10
10k
1%
D5
D6
R2
2.2k
2
−
7
D2†
R6
100
R8
0.68
1.0W
LM143
6
VOUT
VIN
3
+
4
C2
0.01µF
D3†
R7
100
R9
0.68
1.0W
R1
10k
D7
D8
R3
2.2k
D4†
Q4†
2N5976
Q2†
2N4033
R5
22k
C4
0.1µF
CERAMIC
V− = −38V

†Put on common heat sink.
All Diodes are 1N3193.

TL/H/7783-13

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

National Semiconductor

LM146/LM246/LM346 Programmable Quad Operational Amplifiers

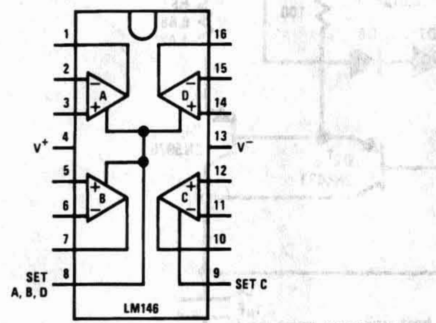
General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

Features (I_{SET} = 10 μA)

■ Programmable electrical characteristics	
■ Battery-powered operation	
■ Low supply current	350 μA/amplifier
■ Guaranteed gain bandwidth product	0.8 MHz min
■ Large DC voltage gain	120 dB
■ Low noise voltage	28 nV/$\sqrt{\text{Hz}}$
■ Wide power supply range	±1.5V to ±22V
■ Class AB output stage–no crossover distortion	
■ Ideal pin out for Biquad active filters	
■ Input bias currents are temperature compensated	

Connection Diagram (Dual-In-Line Package, Top View)



1
2
3
V+ 4
5
6
7
SET A, B, D 8
16
15
14
13 V−
12
11
10
9 SET C
A
B
C
D
LM146

TL/H/5654-1

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)

Gain Bandwidth Product = 1 MHz (I_{SET}/10 μA)

Slew Rate = 0.4V/μs (I_{SET}/10 μA)

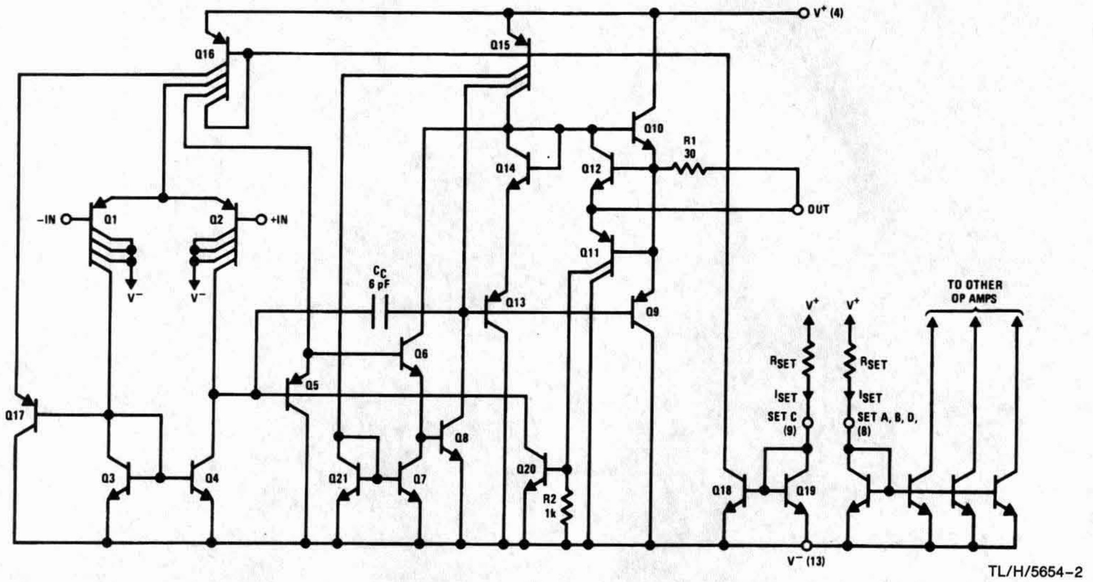
Input Bias Current ≅ 50 nA (I_{SET}/10 μA)

I_{SET} = Current into pin 8, pin 9 (see schematic-diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Order Number LM146J, LM146J/883, LM246J, LM346M or LM346N
See NS Package Number J16A, M16A or N16A

Schematic Diagram



V+ (4)
Q16
Q15
Q10
R1 30
Q14
Q12
OUT
−IN
Q1
Q2
+IN
V−
V−
Q11
CC 6 pF
Q13
Q9
Q6
Q5
V+
V+
RSET
RSET
ISET
ISET
SET C (9)
SET A, B, D, (8)
TO OTHER OP AMPS
Q17
Q8
Q3
Q4
Q21
Q7
Q20
R2 1k
Q18
Q19
V− (13)

TL/H/5654-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 5)

	LM146	**LM246**	**LM346**
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage (Note 1)	±30V	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW	500 mW
Output Short-Circuit Duration (Note 3)	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Maximum Junction Temperature	150°C	110°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C	260°C
Thermal Resistance (θ_{jA}), (Note 2)			
Cavity DIP (J) Pd	900 mW	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W	100°C/W
Small Outline (M) θ_{jA}			115°C/W
Molded DIP (N) Pd			500 mW
θ_{jA}			90°C/W
Soldering Information			
Dual-In-Line Package			
Soldering (10 seconds)	+260°C	+260°C	+260°C
Small Outline Package			
Vapor Phase (60 seconds)	+215°C	+215°C	+215°C
Infrared (15 seconds)	+220°C	+220°C	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

DC Electrical Characteristics ($V_S = \pm 15V$, $I_{SET} = 10\ \mu A$, Note 4)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM}=0V$, $R_S \le 50\Omega$, $T_A=25°C$		0.5	5		0.5	6	mV
Input Offset Current	$V_{CM}=0V$, $T_A=25°C$		2	20		2	100	nA
Input Bias Current	$V_{CM}=0V$, $T_A=25°C$		50	100		50	250	nA
Supply Current (4 Op Amps)	$T_A=25°C$		1.4	2.0		1.4	2.5	mA
Large Signal Voltage Gain	$R_L=10\ k\Omega$, $\Delta V_{OUT}=\pm 10V$, $T_A=25°C$	100	1000		50	1000		V/mV
Input CM Range	$T_A=25°C$	±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \le 10\ k\Omega$, $T_A=25°C$	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \le 10\ k\Omega$, $T_A=25°C$, $V_S = \pm 5$ to $\pm 15V$	80	100		74	100		dB
Output Voltage Swing	$R_L \ge 10\ k\Omega$, $T_A=25°C$	±12	±14		±12	±14		V
Short-Circuit	$T_A=25°C$	5	20	35	5	20	35	mA
Gain Bandwidth Product	$T_A=25°C$	0.8	1.2		0.5	1.2		MHz
Phase Margin	$T_A=25°C$		60			60		Deg
Slew Rate	$T_A=25°C$		0.4			0.4		V/μs
Input Noise Voltage	f=1 kHz, $T_A=25°C$		28			28		nV/√Hz
Channel Separation	$R_L=10\ k\Omega$, $\Delta V_{OUT}=0V$ to $\pm 12V$, $T_A=25°C$		120			120		dB
Input Resistance	$T_A=25°C$		1.0			1.0		MΩ
Input Capacitance	$T_A=25°C$		2.0			2.0		pF
Input Offset Voltage	$V_{CM}=0V$, $R_S \le 50\Omega$		0.5	6		0.5	7.5	mV
Input Offset Current	$V_{CM}=0V$		2	25		2	100	nA
Input Bias Current	$V_{CM}=0V$		50	100		50	250	nA
Supply Current (4 Op Amps)			1.7	2.2		1.7	2.5	mA

DC Electrical Characteristics (Continued) ($V_S = \pm 15V$, $I_{SET} = 10\ \mu A$, Note 4)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$R_L = 10\ k\Omega$, $\Delta V_{OUT} = \pm 10V$	50	1000		25	1000		V/mV
Input CM Range		±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 50\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 50\Omega$, $V_S = \pm 5V$ to $\pm 15V$	76	100		74	100		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V

DC Electrical Characteristic ($V_S = \pm 15V$, $I_{SET} = 1\ \mu A$)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input Bias Current	$V_{CM} = 0V$, $T_A = 25°C$		7.5	20		7.5	100	nA
Supply Current (4 Op Amps)	$T_A = 25°C$		140	250		140	300	μA
Gain Bandwidth Product	$T_A = 25°C$	80	100		50	100		kHz

DC Electrical Characteristics ($V_S = \pm 1.5V$, $I_{SET} = 10\ \mu A$)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input CM Range	$T_A = 25°C$	±0.7			±0.7			V
CM Rejection Ratio	$R_S \leq 50\Omega$, $T_A = 25°C$		80			80		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$, $T_A = 25°C$	±0.6			±0.6			V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

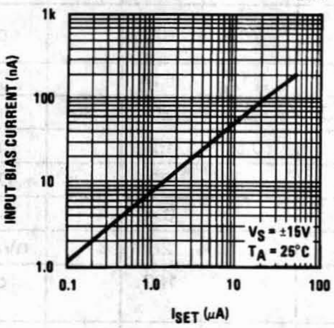
Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

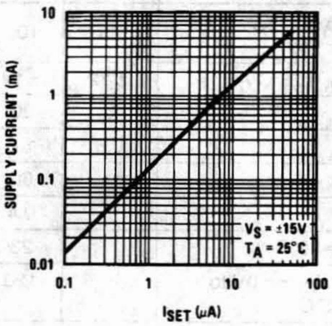
Note 5: Refer to RETS146X for LM146J military specifications.

Typical Performance Characteristics

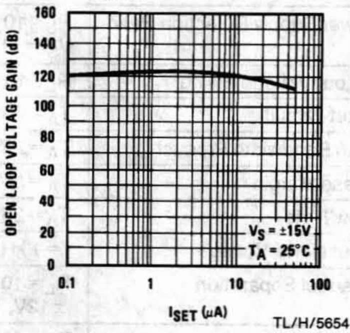
Input Bias Current vs I_{SET}



Supply Current vs I_{SET}



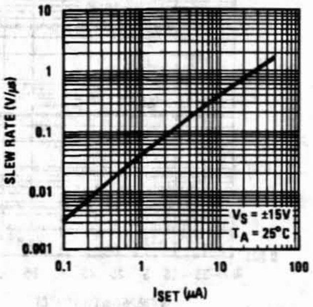
Open Loop Voltage Gain vs I_{SET}



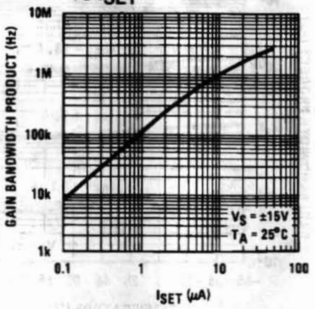
TL/H/5654-3

Typical Performance Characteristics

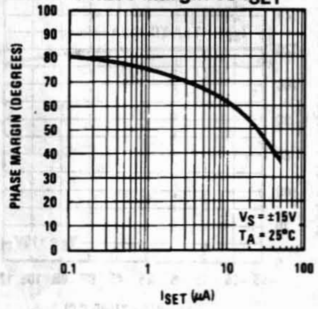
Slew Rate vs I_{SET}



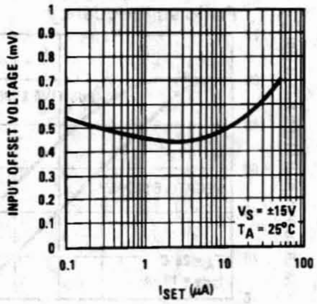
Gain Bandwidth Product vs I_{SET}



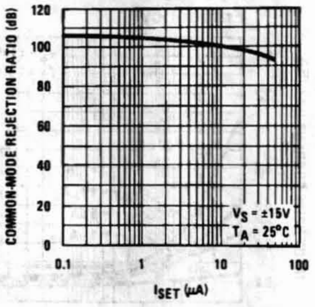
Phase Margin vs I_{SET}



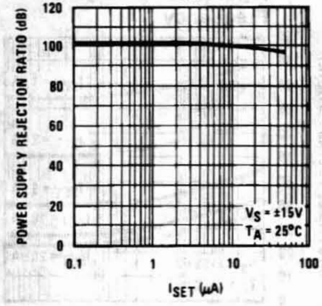
Input Offset Voltage vs I_{SET}



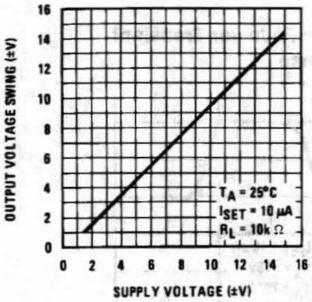
Common-Mode Rejection Ratio vs I_{SET}



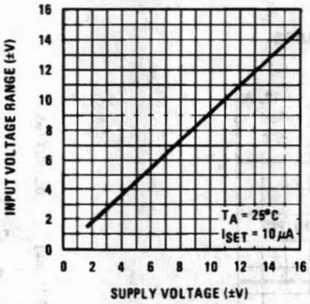
Power Supply Rejection Ratio vs I_{SET}



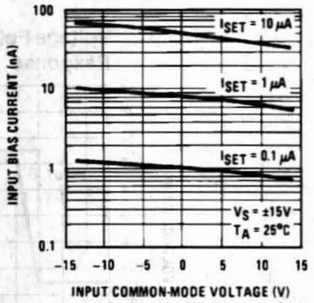
Output Voltage Swing vs Supply Voltage



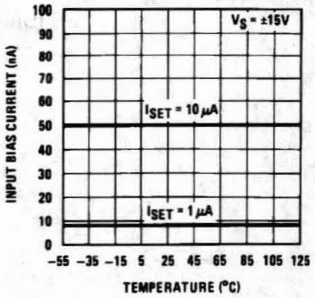
Input Voltage Range vs Supply Voltage



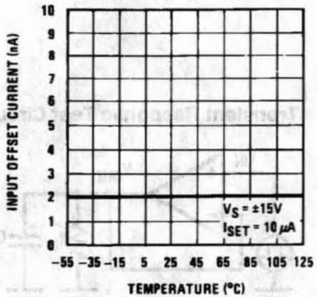
Input Bias Current vs Input Common-Mode Voltage



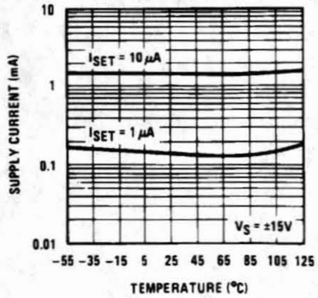
Input Bias Current vs Temperature



Input Offset Current vs Temperature



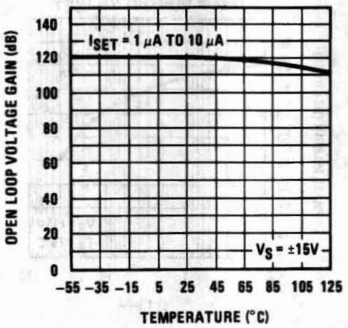
Supply Current vs Temperature



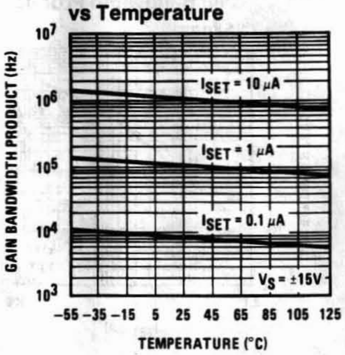
TL/H/5654–4

Typical Performance Characteristics (Continued)

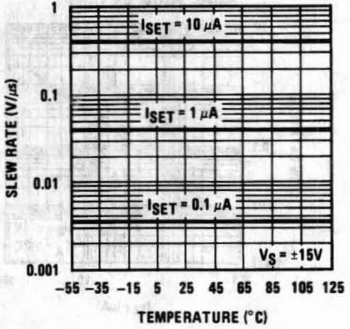
Open Loop Voltage Gain vs Temperature



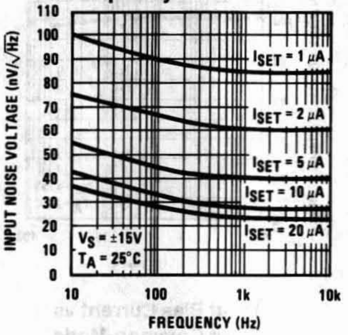
Gain Bandwidth Product vs Temperature



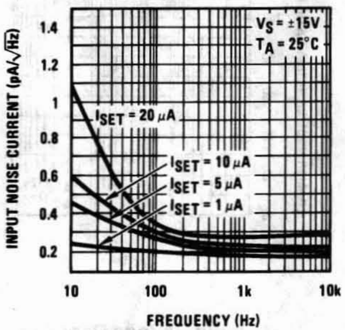
Slew Rate vs Temperature



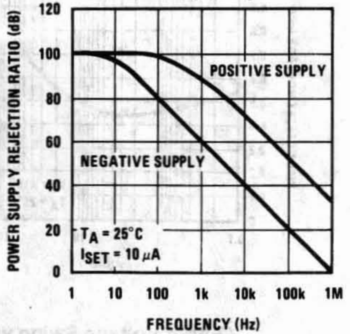
Input Noise Voltage vs Frequency



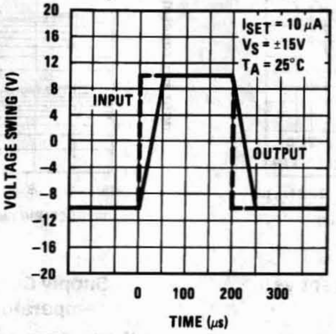
Input Noise Current vs Frequency



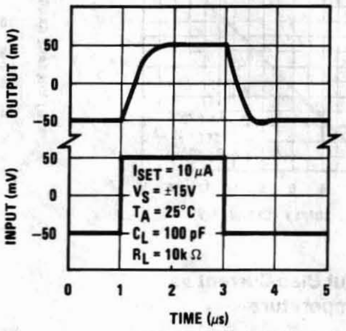
Power Supply Rejection Ratio vs Frequency



Voltage Follower Pulse Response

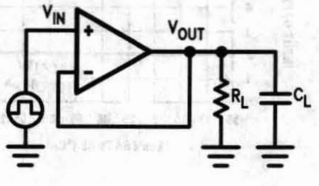


Voltage Follower Transient Response



TL/H/5654–5

Transient Response Test Circuit



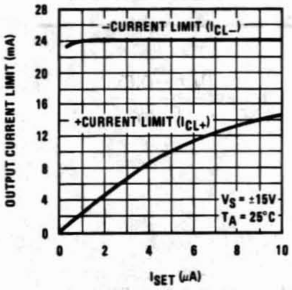
TL/H/5654–6

Application Hints

Avoid reversing the power supply polarity; the device will fail.

Common-Mode Input Voltage: The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

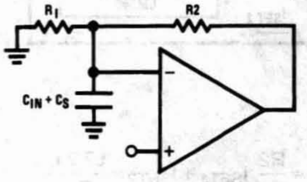
Output Voltage Swing vs I_{SET}: For a desired output voltage swing the value of the minimum load depends on the positive and negative output current capability of the op amp. The maximum available positive output current, ($I_{CL}+$), of the device increases with I_{SET} whereas the negative output current ($I_{CL}-$) is independent of I_{SET}. *Figure 1* illustrates the above.



TL/H/5654-7

FIGURE 1. Output Current Limit vs I_{SET}

Input Capacitance: The input capacitance, C_{IN}, of the LM146 is approximately 2 pF; any stray capacitance, C_S, (due to external circuit circuit layout) will add to C_{IN}. When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback (*Figure 2*), this pole occurs at $\frac{1}{2}\pi$ (R1||R2) ($C_{IN} + C_S$). Make sure that this pole occurs at least 2 octaves beyond the expected −3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_I(C_S + C_{IN})$, where R_I is the input resistance of the circuit.



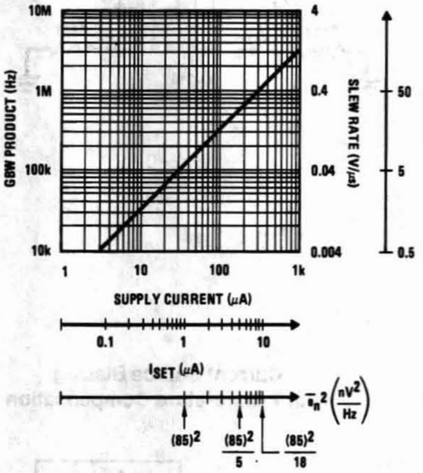
TL/H/5654-9

FIGURE 2

Temperature Effect on the GBW: The GBW (gain bandwidth product), of the LM146 is directly proportional to I_{SET} and inversely proportional to the absolute temperature. When using resistors to set the bias current, I_{SET}, of the device, the GBW product will decrease with increasing temperature. Compensation can be provided by creating an I_{SET} current directly proportional to temperature (see typical applications).

Isolation Between Amplifiers: The LM146 die is isothermally layed out such that crosstalk between *all 4* amplifiers is in excess of −105 dB (DC). Optimum isolation (better than −110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

LM146 Typical Performance Summary: The LM146 typical behaviour is shown in *Figure 3*. The device is fully predictable. As the set current, I_{SET}, increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the V_{OS} remains constant. The usable GBW range of the op amp is 10 kHz to 3.5−4 MHz.

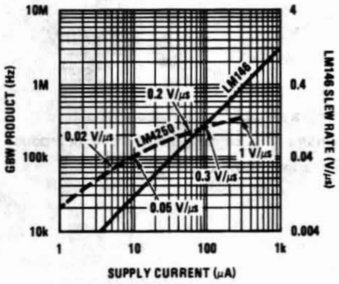


TL/H/5654-8

FIGURE 3. LM146 Typical Characteristics

Low Power Supply Operation: The quad op amp operates down to ±1.3V supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

Speed vs Power Consumption: LM146 vs LM4250 (single programmable). Through *Figure 4*, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz. For GBW products below 200 kHz, the LM4250 will consume less power.

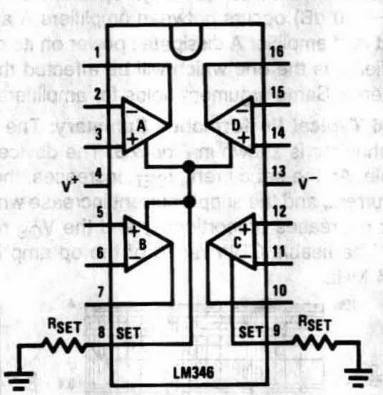


TL/H/5654-10

FIGURE 4. LM146 vs LM4250

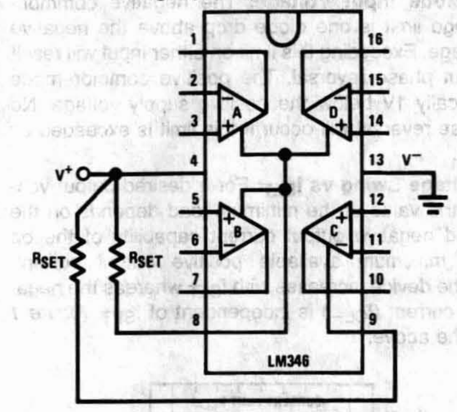
Typical Applications

Dual Supply or Negative Supply Biasing


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
A
B
C
D
V⁺
V⁻
RSET
SET
LM346

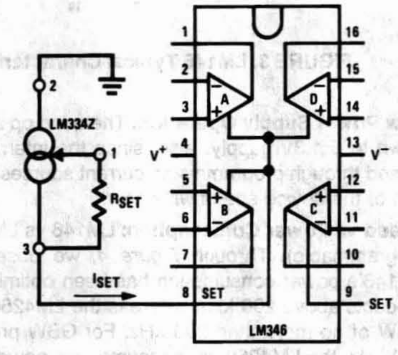
$$I_{SET} \cong \frac{|V^-| - 0.6V}{R_{SET}}$$

Single (Positive) Supply Biasing


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
A
B
C
D
V⁺
V⁻
RSET
RSET
LM346

$$I_{SET} \cong \frac{V^+ - 0.6V}{R_{SET}}$$

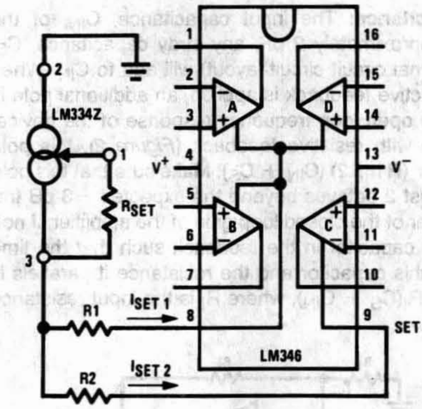
Current Source Biasing with Temperature Compensation


LM334Z
1
2
3
RSET
ISET
V⁺
V⁻
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
A
B
C
D
SET
SET
LM346

$$I_{SET} = \frac{67.7\ mV}{R_{SET}}$$

- The LM334 provides an I_{SET} directly proportional to absolute temperature. This cancels the slight GBW product Temperature coefficient of the LM346.

Biasing all 4 Amplifiers with Single Current Source


LM334Z
1
2
3
RSET
R1
R2
ISET 1
ISET 2
V⁺
V⁻
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
A
B
C
D
SET
LM346

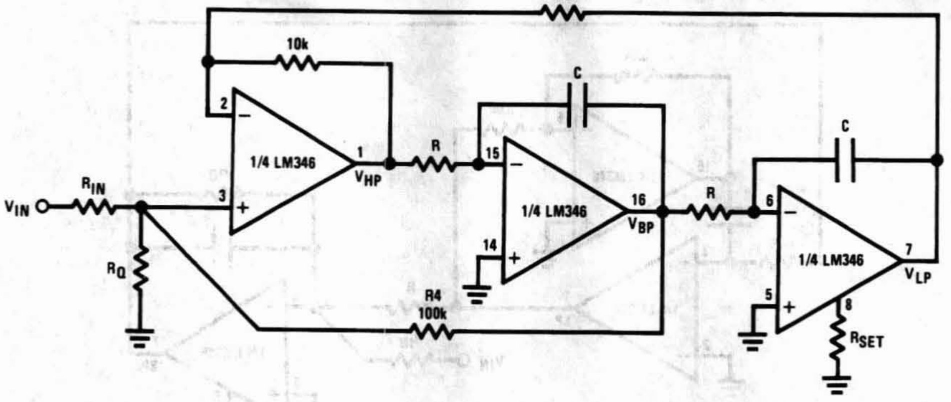
TL/H/5654-11

$$\frac{I_{SET1}}{I_{SET2}} = \frac{R2}{R1},\ I_{SET1} + I_{SET2} = \frac{67.7\ mV}{R_{SET}}$$

- For $I_{SET1} \cong I_{SET2}$ resistors R1 and R2 are not required if a slight error between the 2 set currents can be tolerated. If not, then use R1 = R2 to create a 100 mV drop across these resistors.

Active Filters Applications

Basic (Non-Inverting "State Variable") Active Filter Building Block



TL/H/5654-12

- The LM146 quad programmable op amp is especially suited for active filters because of their adequate GBW product and low power consumption.

Circuit synthesis equations (for circuit analysis equations, consult with the LM148 data sheet).

Need to know desired: f_o = center frequency measured at the BP output

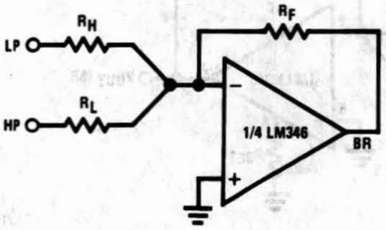
Q_o = quality factor measured at the BP output

H_o = gain at the output of interest (BP or HP or LP or all of them)

- Relation between different gains: $H_{o(BP)} = 0.316 \times Q_o \times H_{o(LP)}$; $H_{o(LP)} = 10 \times H_{o(HP)}$
- $R \times C = \dfrac{5.033 \times 10^{-2}}{f_o}$ (sec)
- For BP output: $R_Q = \left(\dfrac{3.478\,Q_o - H_{o(BP)}}{10^5} - \dfrac{H_{o(BP)}}{10^5 \times 3.748 \times Q_o} \right)^{-1}$; $R_{IN} = \dfrac{\left(\dfrac{3.478\,Q_o}{H_{o(BP)}} - 1 \right)}{\dfrac{1}{RQ} + 10^{-5}}$
- For HP ouput: $R_Q = \dfrac{1.1 \times 10^5}{3.478\,Q_o\,(1.1 - H_{o(HP)}) - H_{o(HP)}}$; $R_{IN} = \dfrac{\dfrac{1.1}{H_{o(HP)}} - 1}{\dfrac{1}{RQ} + 10^{-5}}$

Note. All resistor values are given in ohms.

- For LP output: $R_Q = \dfrac{11 \times 10^5}{3.478\,Q_o\,(11 - H_{o(LP)}) - H_{o(LP)}}$; $R_{IN} = \dfrac{\dfrac{11}{H_{o(LP)}} - 1}{\dfrac{1}{RQ} + 10^{-5}}$
- For BR (notch) output: Use the 4th amplifier of the LM146 to sum the LP and HP outputs of the basic filter.



$$\sqrt{\frac{R_H}{R_L}} = 0.316\,\frac{f_{notch}}{f_o}$$

TL/H/5654-13

Determine R_F according to the desired gains: $H_{o(BR)}\Big|_{f << f_{notch}} = \dfrac{R_F}{R_L} H_{o(LP)}$, $H_{o(BR)}\Big|_{f >> f_{notch}} = \dfrac{R_F}{R_H} H_{o(HP)}$

- **Where to use amplifier C:** Examine the above gain relations and determine the dynamics of the filter. Do not allow slew rate limiting in any output (V_{HP}, V_{BP}, V_{LP}), **that is:**

$$V_{IN(peak)} < 63.66 \times 10^3 \times \frac{I_{SET}}{10\ \mu A} \times \frac{1}{f_o \times H_o}\ \text{(Volts)}$$

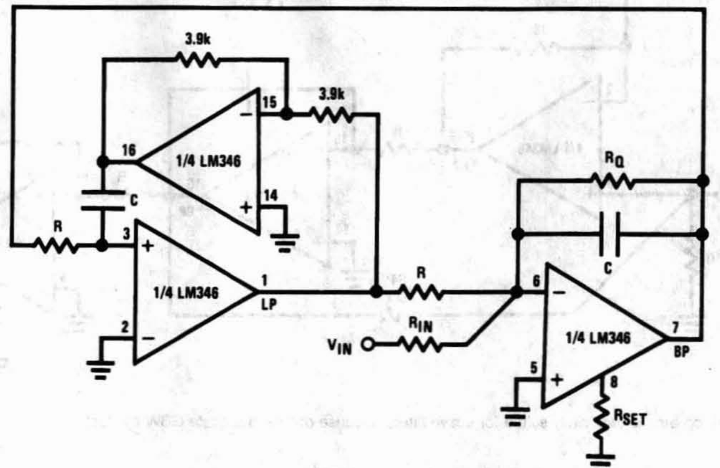
If necessary, use amplifier C, biased at higher I_{SET}, where you get the largest output swing.

Deviation from Theoretical Predictions: Due to the finite GBW products of the op amps the f_o, Q_o will be slightly different from the theoretical predictions.

$$f_{real} \cong \frac{f_o}{1 + \dfrac{2\,f_o}{GBW}},\quad Q_{real} \cong \frac{Q_o}{1 - \dfrac{3.2\,f_o \times Q_o}{GBW}}$$

Active Filters Applications (Continued)

A Simple-to-Design BP, LP Filter Building Block


3.9k
3.9k
15
16
14
1/4 LM346
C
R
3
2
1
LP
1/4 LM346
R
R_IN
V_IN
R_Q
C
6
5
7
BP
8
1/4 LM346
R_SET

TL/H/5654–14

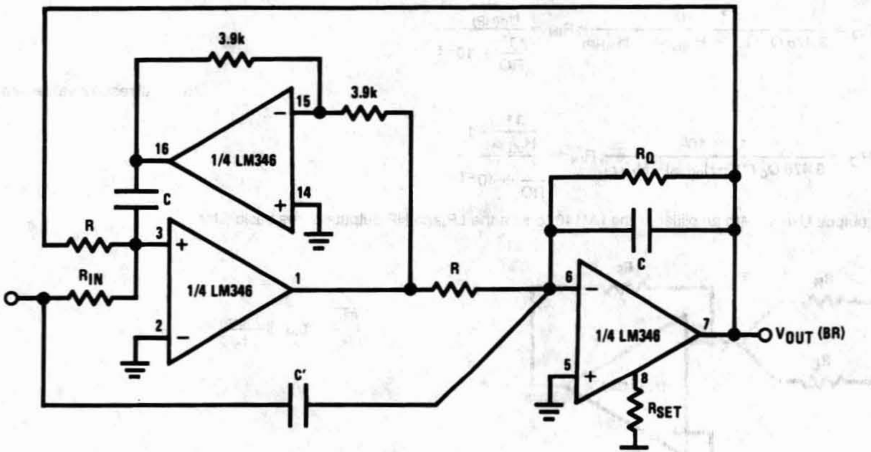
- If resistive biasing is used to set the LM346 performance, the Q_o of this filter building block is nearly insensitive to the op amp's GBW product temperature drift; it has also better noise performance than the state variable filter.

Circuit Synthesis Equations

$$H_{o(BP)} = Q_o H_{o(LP)};\ R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{R_Q}{H_{o(BP)}} = \frac{R}{H_{o(LP)}}$$

- For the eventual use of amplifier C, see comments on the previous page.

A 3-Amplifier Notch Filter (or Elliptic Filter Building Block)


3.9k
3.9k
15
16
14
1/4 LM346
C
R
3
R_IN
V_IN
2
1
1/4 LM346
C'
R
6
5
7
8
C
R_Q
1/4 LM346
R_SET
V_OUT (BR)

TL/H/5654–15

Circuit Synthesis Equations

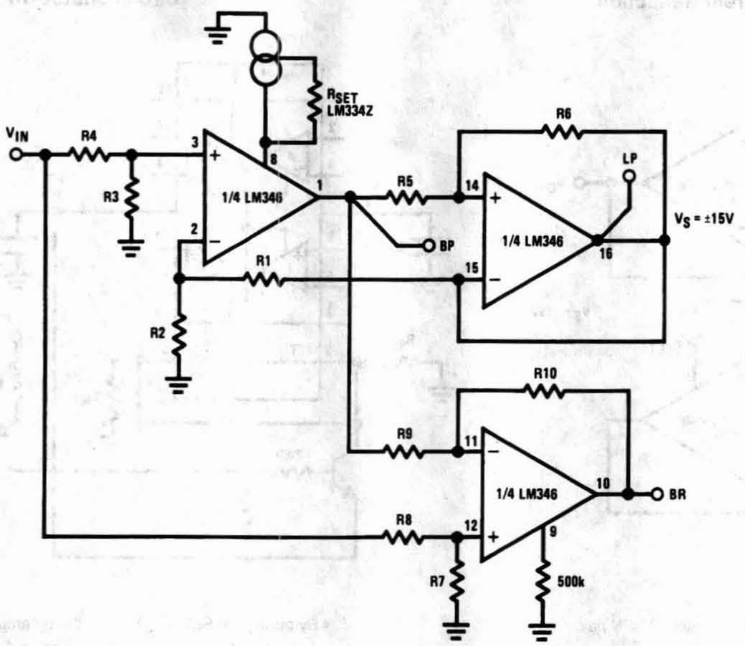
$$R \times C = \frac{0.159}{f_o};\ R_o = Q_o \times R;\ R_{IN} = \frac{0.159 \times f_o}{C' \times f^2_{notch}}$$

$$H_{o(BR)}\Big|_{f<<f_{notch}} = \frac{R}{R_{IN}}\quad H_{o(BR)}\Big|_{f>>f_{notch}} = \frac{C'}{C}$$

- For nothing but a notch output: $R_{IN} = R$, $C' = C$.

Active Filters Applications (Continued)

Capacitorless Active Filters (Basic Circuit)


RSET
LM334Z
VIN
R4
R3
3
8
2
1/4 LM346
1
R1
R2
R5
BP
14
15
1/4 LM346
16
LP
R6
VS = ±15V
R10
R9
11
1/4 LM346
10
BR
R8
12
9
R7
500k

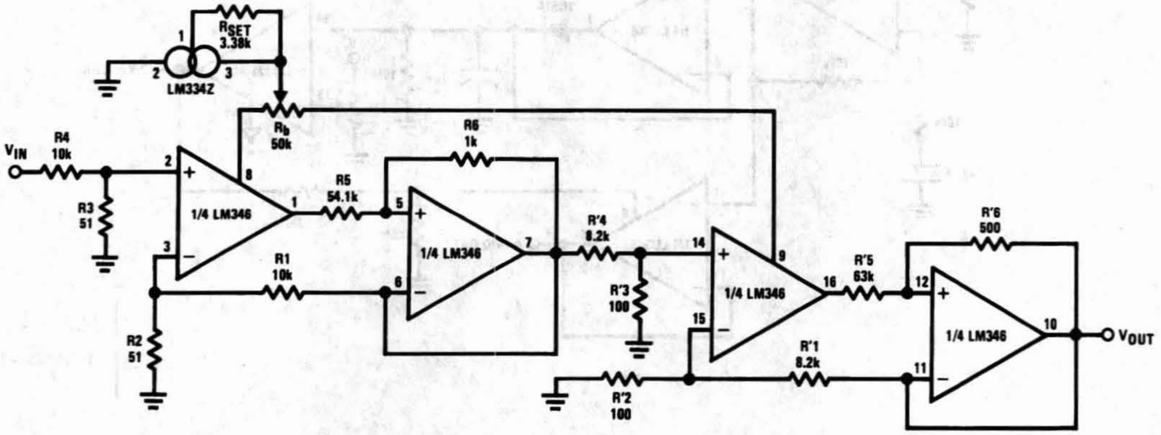
TL/H/5654–16

- This is a BP, LP, BR filter. The filter characteristics are created by using the tunable frequency response of the LM346.
- **Limitations:** $Q_o < 10$, $f_o \times Q_o < 1.5$ MHz, output voltage should not exceed $\text{Vpeak(out)} \le \frac{63.66 \times 10^3}{f_o} \times \frac{I_{SET}(\mu A)}{10\ \mu A}$ (V)
- Design equations: $a = \frac{R6 + R5}{R6}$, $b = \frac{R2}{R1 + R2}$, $c = \frac{R3}{R3 + R4}$, $d = \frac{R7}{R8 + R7}$, $e = \frac{R10}{R(+ R10}$, $f_{o(BP)} = f_u\sqrt{\frac{b}{a}}$, $H_{o(BP)} = a \times c$, $H_{o(LP)} = \frac{c}{b}$, $Q_o = \sqrt{a \times b}$

$f_{o(BR)} = f_{o(BP)}, \left(1 - \frac{c}{b}\right) \cong f_{o(BP)}$ ($C << 1$) provided that $d = H_{o(BP)} \times e$, $H_{o(BR)} = \frac{R10}{R9}$.

- Advantage: f_oQ_o, H_o can be independently adjusted; that is, the filter is extremely easy to tune.
- Tuning procedure (ex. BP tuning)
  1. Pick up a convenient value for b; ($b < 1$)
  2. Adjust Q_o through R5
  3. Adjust $H_{o(BP)}$ through R4
  4. Adjust f_o through R_{SET}. This adjusts the unity gain frequency (f_u) of the op amp.

A 4th Order Butterworth Low Pass Capacitorless Filter


RSET
3.38k
1
2
3
LM334Z
Rb
50k
R4
10k
VIN
R3
51
2
8
1/4 LM346
1
3
R1
10k
R2
51
R6
1k
R5
54.1k
5
6
1/4 LM346
7
R'4
8.2k
R'3
100
14
15
9
1/4 LM346
16
R'5
63k
R'6
500
12
11
1/4 LM346
10
VOUT
R'1
8.2k
R'2
100

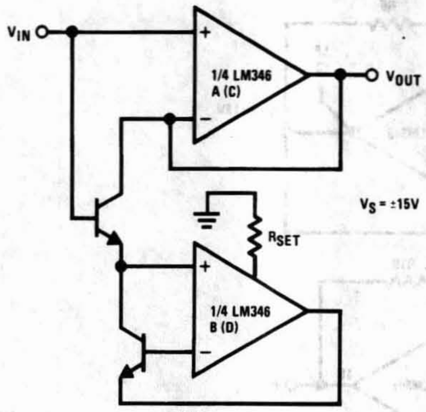
TL/H/5654–17

Ex: $f_c = 20$ kHz, H_o (gain of the filter) $= 1$, $Q_{01} = 0.541$, $Q_{02} = 1.306$.

- Since for this filter the GBW product of all 4 amplifiers has been designed to be the same (~1 MHz) only one current source can be used to bias the circuit. Fine tuning can be further accomplished through R_b.

Miscellaneous Applications

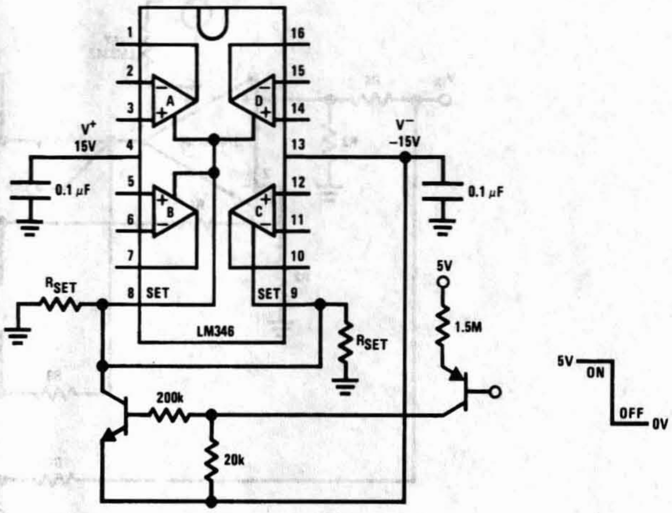
A Unity Gain Follower with Bias Current Reduction



V_IN
1/4 LM346
A (C)
V_OUT
V_S = ±15V
R_SET
1/4 LM346
B (D)

- For better performance, use a matched NPN pair.

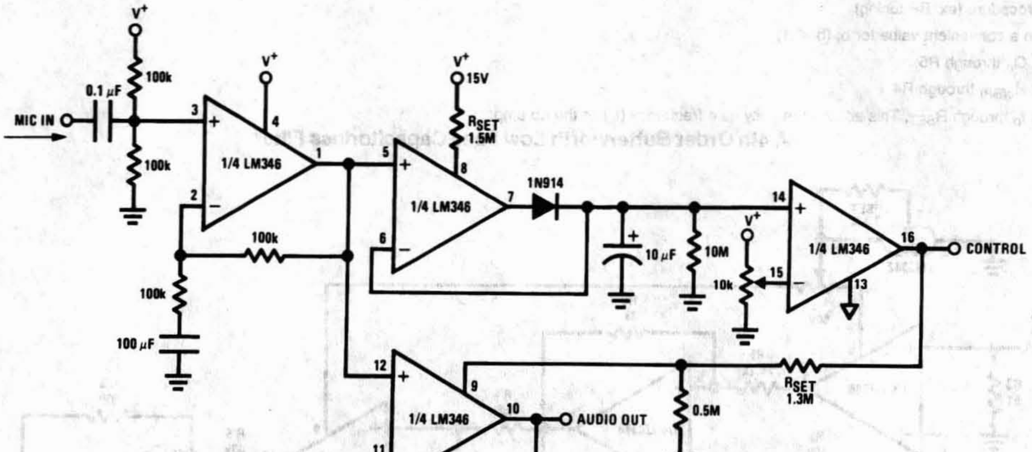
Circuit Shutdown



V⁺
15V
0.1 µF
R_SET
SET
LM346
SET
R_SET
200k
20k
V⁻
−15V
0.1 µF
5V
1.5M
5V
ON
OFF
0V
A
B
C
D

- By pulling the SET pin(s) to V⁻ the op amp(s) shuts down and its output goes to a high impedance state. According to this property, the LM346 can be used as a very low speed analog switch.

Voice Activated Switch and Amplifier

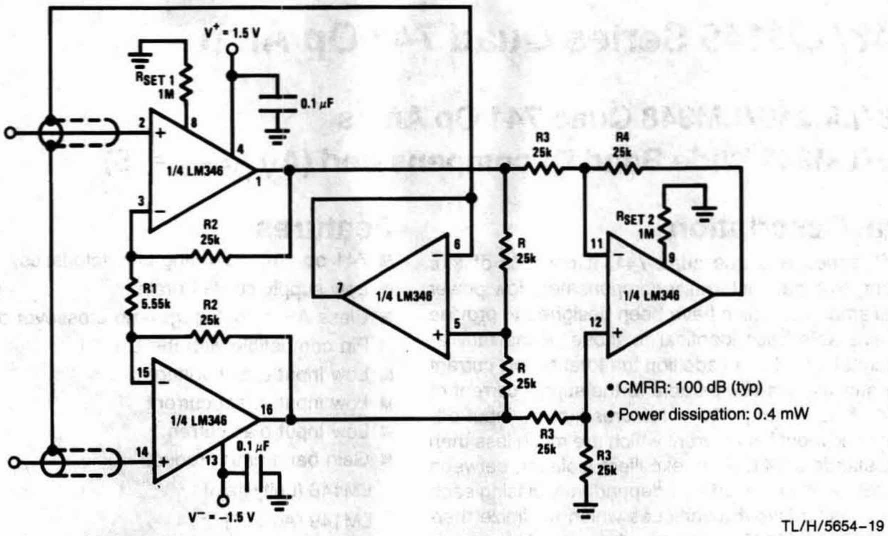


V⁺
100k
0.1 µF
MIC IN
100k
1/4 LM346
100k
100k
100 µF
V⁺
V⁺
15V
R_SET
1.5M
1/4 LM346
1N914
10 µF
10M
V⁺
10k
1/4 LM346
CONTROL
R_SET
1.3M
0.5M
1/4 LM346
AUDIO OUT

TL/H/5654-18

Miscellaneous Applications (Continued)

X10 Micropower Instrumentation Amplifier with Buffered Input Guarding


V⁺ = 1.5 V
RSET 1
1M
0.1 µF
8
2
4
3
1
1/4 LM346
R2
25k
R1
5.55k
R2
25k
15
16
14
13
0.1 µF
V⁻ = −1.5 V
6
7
5
R
25k
R
25k
R3
25k
R4
25k
RSET 2
1M
11
9
12
R3
25k
R3
25k

- CMRR: 100 dB (typ)
- Power dissipation: 0.4 mW

TL/H/5654–19

National Semiconductor

LM148/LM149 Series Quad 741 Op Amp

LM148/LM248/LM348 Quad 741 Op Amps
LM149/LM349 Wide Band Decompensated ($A_{V\,(MIN)} = 5$)

General Description

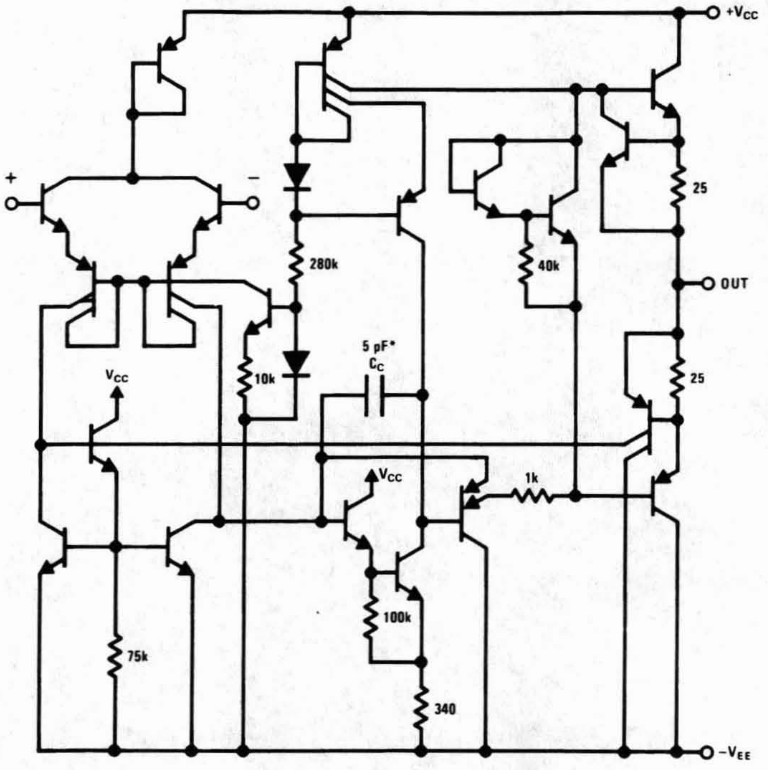
The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The LM149 series has the same features as the LM148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Features

■ 741 op amp operating characteristics	
■ Low supply current drain	0.6 mA/Amplifier
■ Class AB output stage—no crossover distortion	
■ Pin compatible with the LM124	
■ Low input offset voltage	1 mV
■ Low input offset current	4 nA
■ Low input bias current	30 nA
■ Gain bandwidth product	
LM148 (unity gain)	1.0 MHz
LM149 ($A_V \geq 5$)	4 MHz
■ High degree of isolation between amplifiers	120 dB
■ Overload protection for inputs and outputs	

Schematic Diagram



TL/H/7786-1

*1 pF in the LM149

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM148/LM149	LM248	LM348/LM349
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Output Short Circuit Duration (Note 1)	Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and			
Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) P_d	—	—	750 mW
θ_{jA}	—	—	100°C/W
Cavity DIP (J) P_d	1100 mW	800 mW	700 mW
θ_{JA}	110°C/W	110°C/W	110°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	110°C	100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$-25°C \leq T_A \leq +85°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.) Ceramic	300°C	300°C	300°C
Lead Temperature (Soldering, 10 sec.) Plastic			260°C
Soldering Information			
Dual-In-Line Package			
Soldering (10 seconds)	260°C	260°C	260°C
Small Outline Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	220°C	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

	LM148/LM149	LM248	LM348/LM349
ESD tolerance (Note 5)	500V	500V	500V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM148/LM149			LM248			LM348/LM349			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		4	25		4	50		4	50	nA
Input Bias Current	$T_A = 25°C$		30	100		30	200		30	200	nA
Input Resistance	$T_A = 25°C$	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	$T_A = 25°C$, $V_S = \pm 15V$		2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		25	160		25	160		V/mV
Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz to 20 kHz (Input Referred) See Crosstalk Test Circuit		−120			−120			−120		dB
Small Signal Bandwidth	LM148 Series $T_A = 25°C$		1.0			1.0			1.0		MHz
	LM149 Series		4.0			4.0			4.0		MHz
Phase Margin	LM148 Series ($A_V = 1$) $T_A = 25°C$		60			60			60		degrees
	LM149 Series ($A_V = 5$)		60			60			60		degrees
Slew Rate	LM148 Series ($A_V = 1$) $T_A = 25°C$		0.5			0.5			0.5		V/µs
	LM149 Series ($A_V = 5$)		2.0			2.0			2.0		V/µs
Output Short Circuit Current	$T_A = 25°C$		25			25			25		mA
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0			7.5			7.5	mV
Input Offset Current				75			125			100	nA
Input Bias Current				325			500			400	nA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM148/LM149			LM248			LM348/LM349			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L > 2\ k\Omega$	25			15			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			±12			V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		70	90		dB
Supply Voltage Rejection	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	77	96		77	96		77	96		dB

Note 1: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

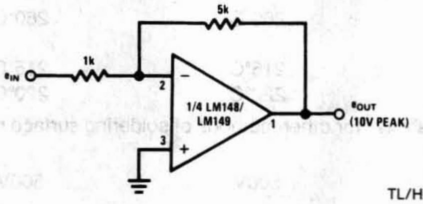
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dicated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

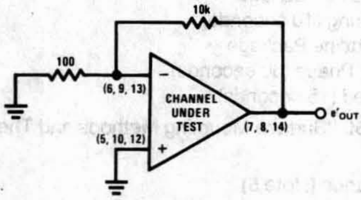
Note 4: Refer to RETS 148X for LM148 military specifications and refer to RETS 149X for LM149 military specifications.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

Cross Talk Test Circuit



TL/H/7786-6



TL/H/7786-7

$$\text{Crosstalk} = -20 \log \frac{e'_{OUT}}{101 \times e_{OUT}} \text{ (dB)}$$

$V_S = \pm 15V$

Application Hints

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The LM149 series has the same characteristics as the LM148 except it has been decompensated to provide a wider bandwidth. As a result the part requires a minimum gain of 5.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

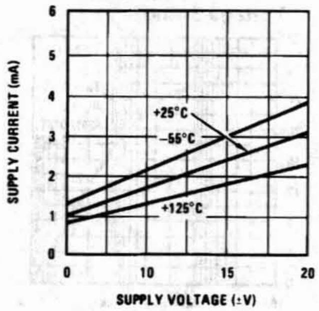
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

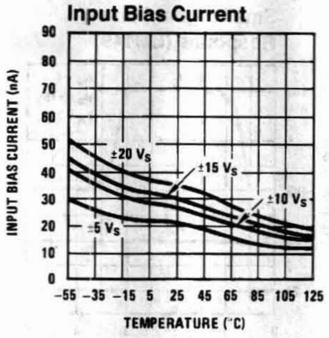
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Performance Characteristics

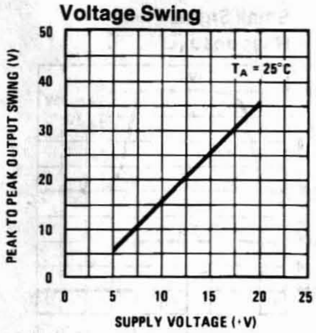
Supply Current



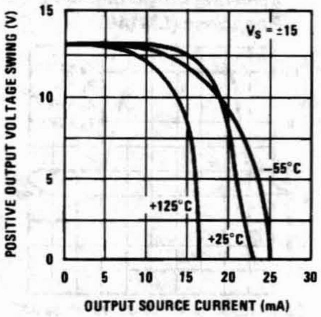
Input Bias Current



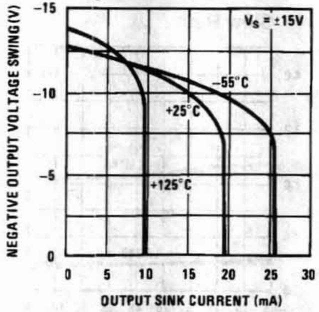
Voltage Swing



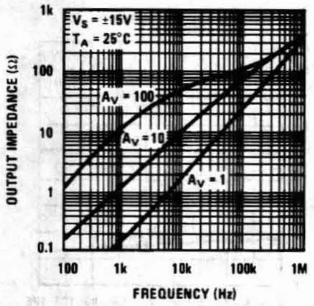
Positive Current Limit



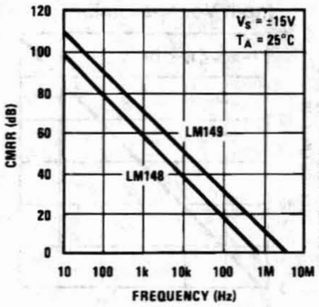
Negative Current Limit



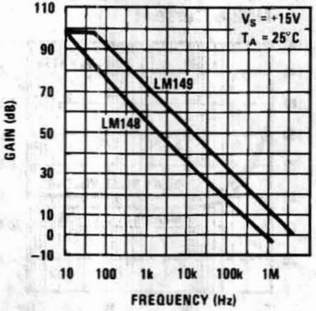
Output Impedance



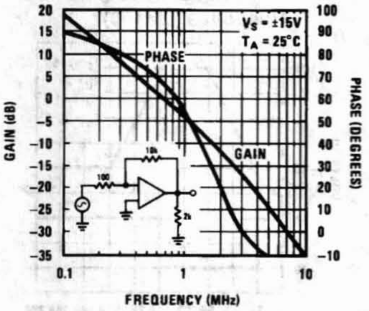
Common-Mode Rejection Ratio



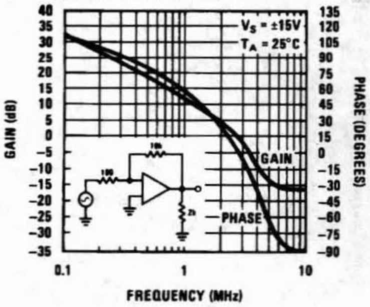
Open Loop Frequency Response



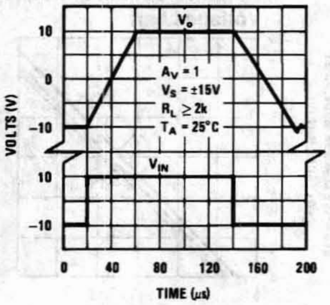
Bode Plot LM148



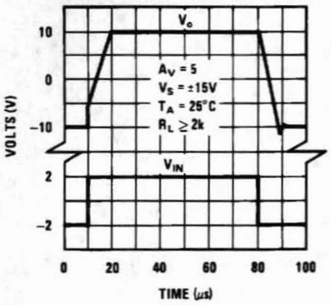
Bode Plot LM149



Large Signal Pulse Response (LM148)



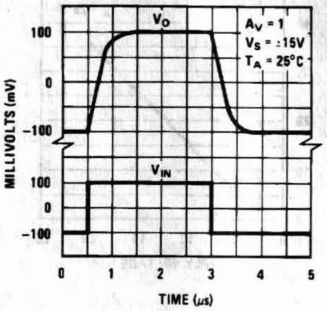
Large Signal Pulse Response (LM149)



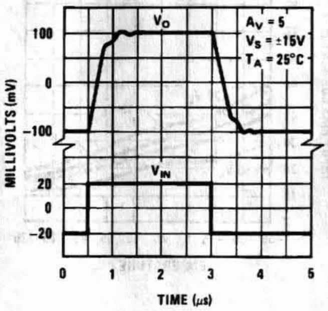
TL/H/7786–3

1

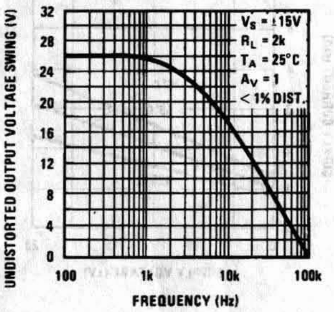
Typical Performance Characteristics (Continued)



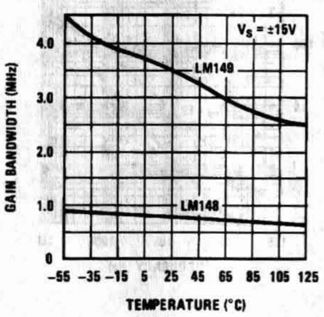
Small Signal Pulse Response (LM148)



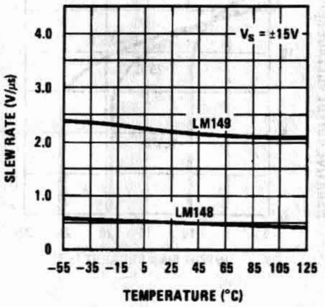
Small Signal Pulse Response (LM149)



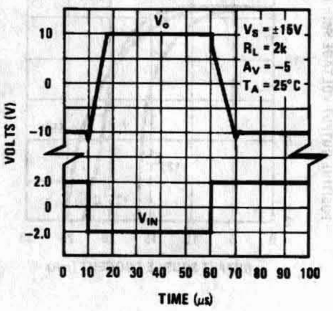
Undistorted Output Voltage Swing



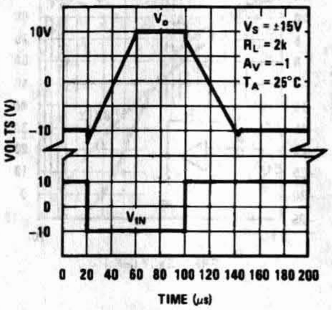
Gain Bandwidth



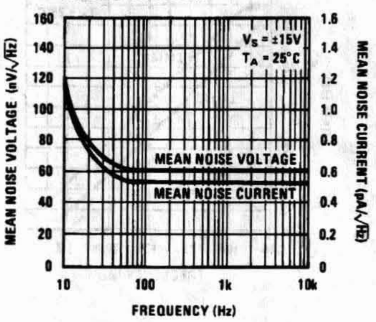
Slew Rate



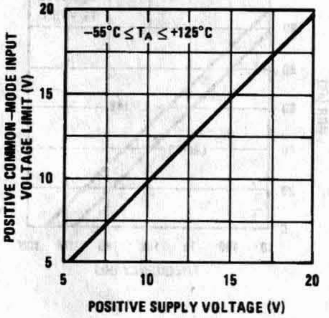
Inverting Large Signal Pulse Response (LM149)



Inverting Large Signal Pulse Response (LM148)

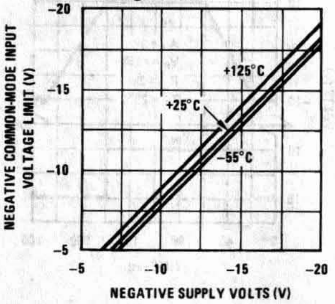


Input Noise Voltage and Noise Current



Positive Common-Mode Input Voltage Limit

TL/H/7786–4

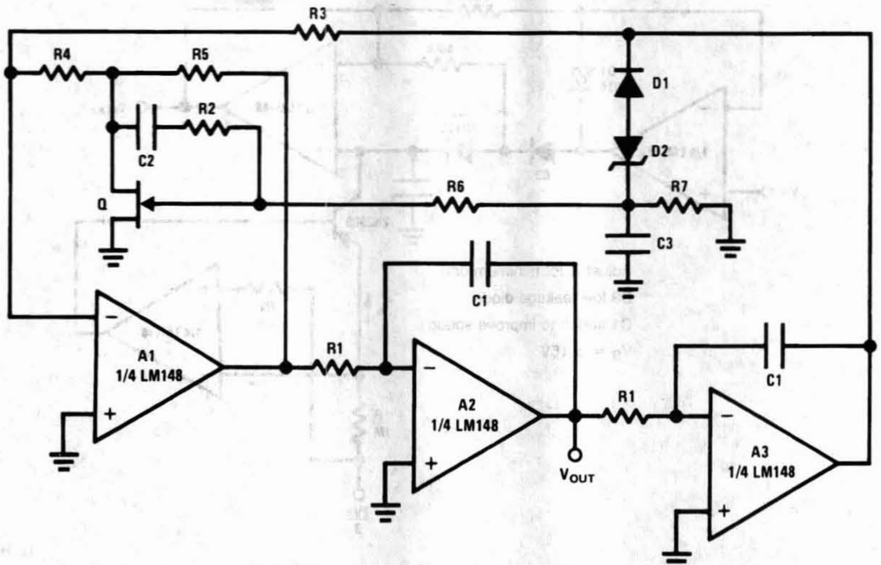


Negative Common-Mode Input Voltage Limit

TL/H/7786–5

Typical Applications—LM148

One Decade Low Distortion Sinewave Generator


R3
R4
R5
R2
C2
Q
R6
R7
D1
D2
C3
C1
A1
1/4 LM148
R1
A2
1/4 LM148
V_{OUT}
R1
C1
A3
1/4 LM148

$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\quad r_{DS} \approx \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

TL/H/7786-8

f_{MAX} = 5 kHz, THD ≤ 0.03%

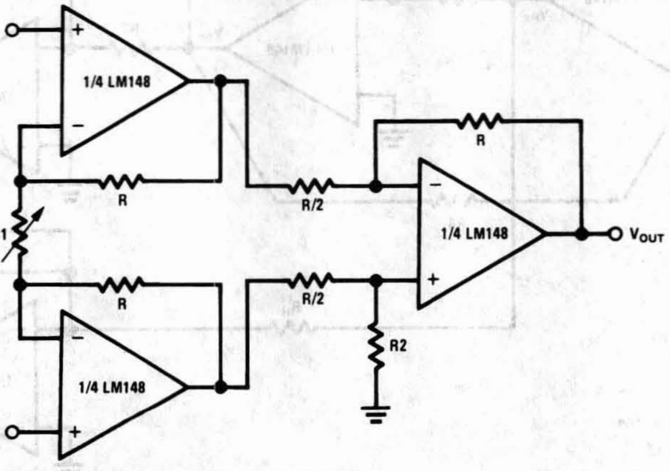
R1 = 100k pot. C1 = 0.0047 μF, C2 = 0.01 μF, C3 = 0.1 μF, R2 = R6 = R7 = 1M,

R3 = 5.1k, R4 = 12Ω, R5 = 240Ω, Q = NS5102, D1 = 1N914, D2 = 3.6V avalanche

diode (ex. LM103), V_S = ±15V

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

Low Cost Instrumentation Amplifier


1/4 LM148
R
R/2
R
R1
R/2
R
1/4 LM148
V_{OUT}
R2
1/4 LM148

TL/H/7786-9

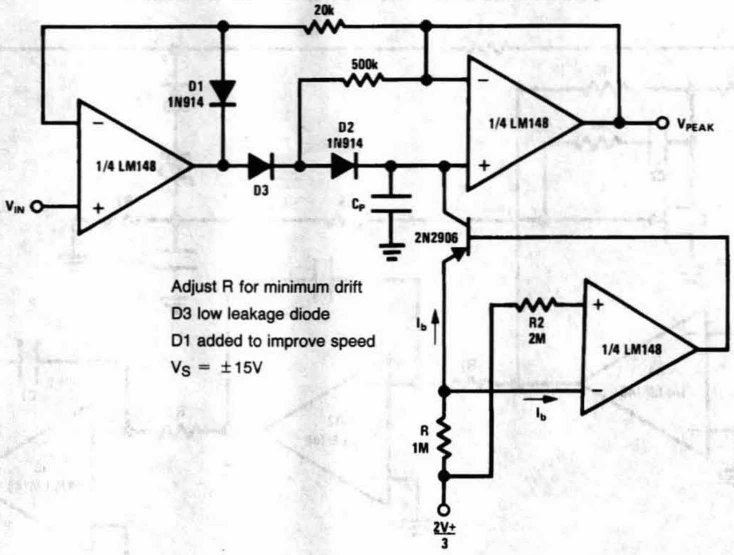
$$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right),\ V_S^- - 3V \le V_{IN\,CM} \le V_S^+ - 3V,$$

V_S = ±15V

R = R2, trim R2 to boost CMRR

Typical Applications—LM148 (Continued)

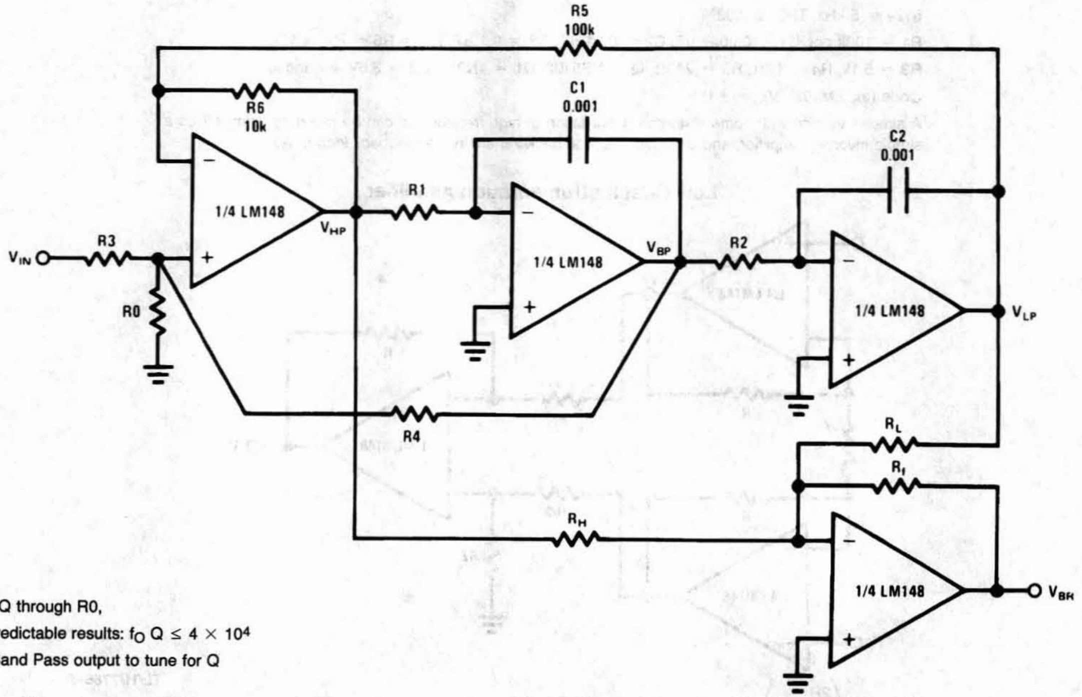
Low Drift Peak Detector with Bias Current Compensation


20k
D1
1N914
500k
1/4 LM148
V_PEAK
D2
1N914
1/4 LM148
D3
V_IN
C_P
2N2906
I_b
R2
2M
1/4 LM148
I_b
R
1M
2V+/3

Adjust R for minimum drift
D3 low leakage diode
D1 added to improve speed
$V_S = \pm 15V$

TL/H/7786-10

Universal State-Variable Filter


R5
100k
R6
10k
C1
0.001
C2
0.001
1/4 LM148
V_HP
R1
V_IN
R3
R0
1/4 LM148
V_BP
R2
1/4 LM148
V_LP
R4
R_L
R_f
R_H
1/4 LM148
V_BR

Tune Q through R0,
For predictable results: $f_O\,Q \le 4 \times 10^4$
Use Band Pass output to tune for Q

$$\frac{V_{(s)}}{V_{IN(s)}} = \frac{N_{(s)}}{D_{(s)}},\ D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o{}^2$$

$$N_{HP(s)} = S^2\,H_{OHP},\ N_{BP(s)} = \frac{-s\omega_O\,H_{OBP}}{Q}\quad N_{LP} = \omega_o{}^2\,H_{OLP}.$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1t2}},\ t_i = R_iC_i,\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right)\left(\frac{R6}{R5}\frac{t_1}{t_2}\right)^{1/2}$$

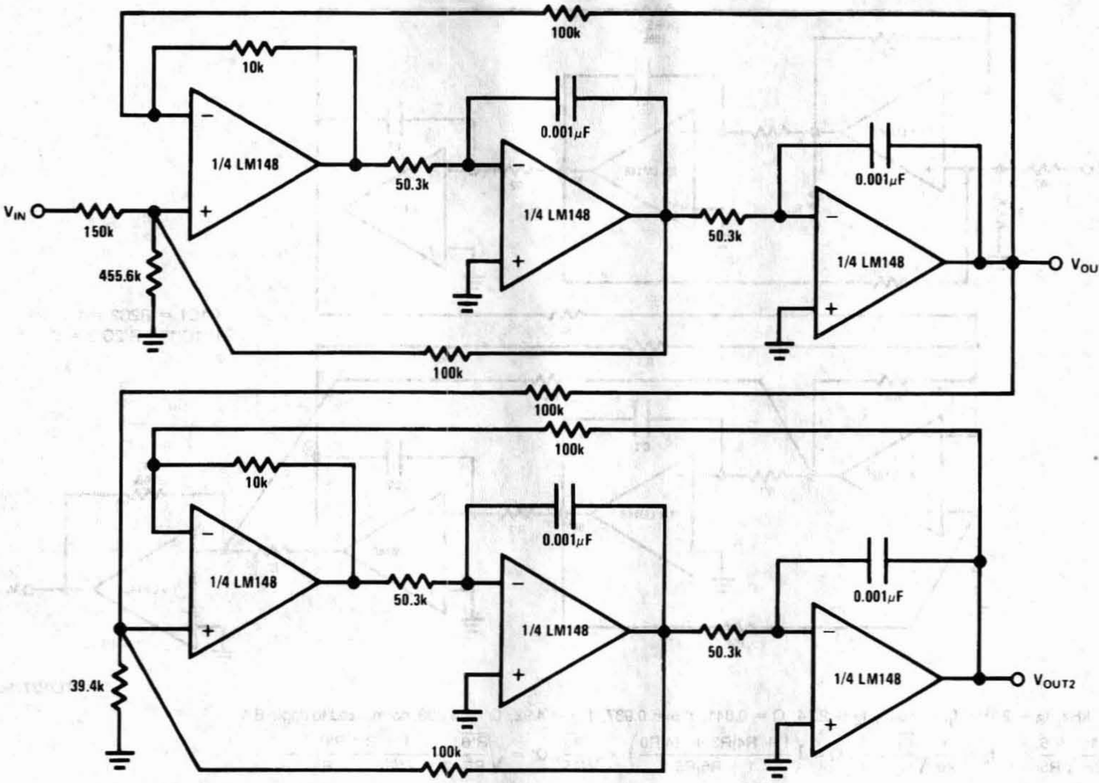
$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L\,t_1\,t_2}\right)^{1/2},\ H_{OHP} = \frac{1 + R6|R5}{1 + R3|R0 + R3|R4},\ H_{OBP} = \frac{1 + R4|R3 + R4|R0}{1 + R3|R0 + R3|R4}$$

$$H_{OLP} = \frac{1 + R5|R6}{1 + R3|R0 + R3|R4}$$

TL/H/7786-11

Typical Applications—LM148 (Continued)

A 1 kHz 4 Pole Butterworth


100k
10k
0.001 μF
1/4 LM148
50.3k
0.001 μF
V_IN
150k
1/4 LM148
50.3k
455.6k
1/4 LM148
V_OUT1
100k
100k
100k
10k
0.001 μF
1/4 LM148
50.3k
0.001 μF
1/4 LM148
50.3k
39.4k
1/4 LM148
V_OUT2
100k

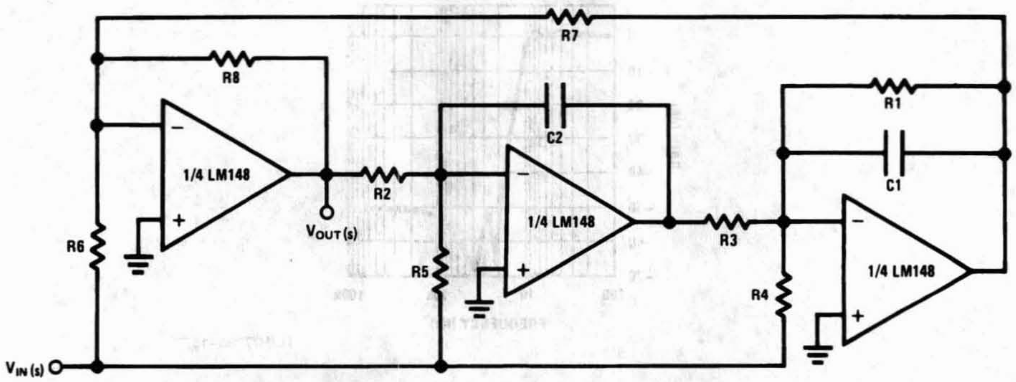
TL/H/7786–12

Use general equations, and tune each section separately

$Q_{1stSECTION} = 0.541$, $Q_{2ndSECTION} = 1.306$

The response should have 0 dB peaking

A 3 Amplifier Bi-Quad Notch Filter


R7
R8
R1
C2
C1
1/4 LM148
R2
V_OUT (s)
1/4 LM148
R3
R6
R5
1/4 LM148
R4
V_IN (s)

TL/H/7786–13

$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}},\ f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}},\ f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

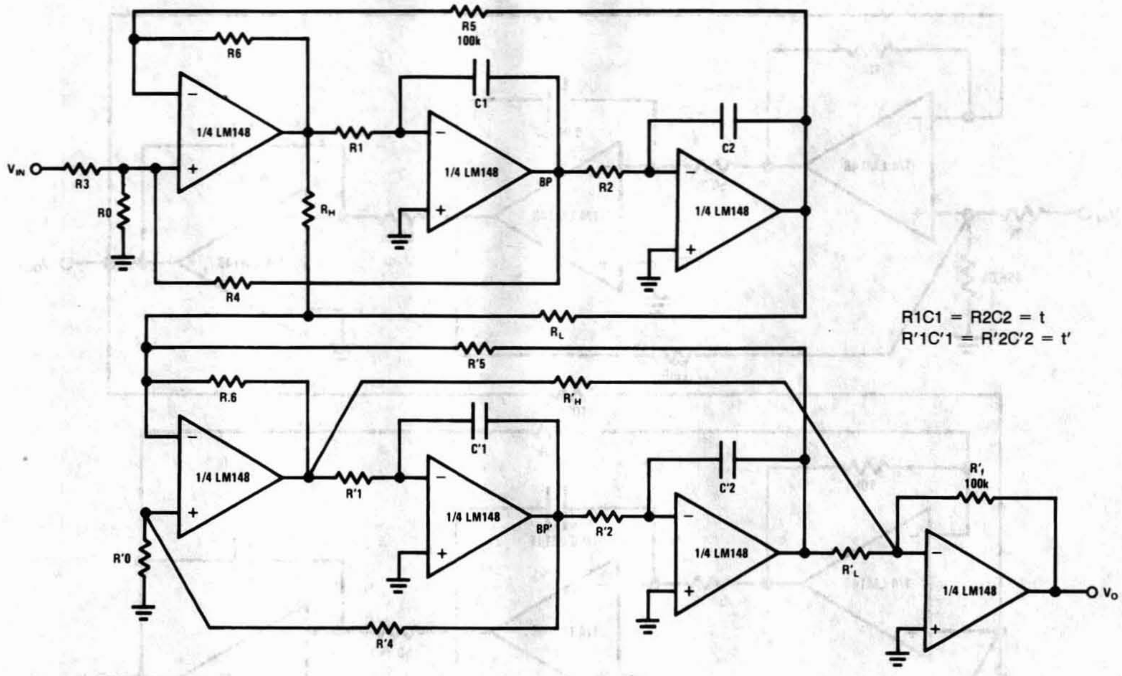
Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: $f_{NOTCH} = 3$ kHz, Q = 5, R1 = 270k, R2 = R3 = 20k, R4 = 27k, R5 = 20k, R6 = R8 = 10k, R7 = 100k, C1 = C2 = 0.001 μF

Better noise performance than the state-space approach.

Typical Applications—LM148 (Continued)

A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)


R5
100k
R6
1/4 LM148
C1
R1
1/4 LM148
BP
R2
C2
1/4 LM148
V_IN
R3
R0
R_H
R4
R_L
R'5
R.6
R'_H
1/4 LM148
C'1
R'1
1/4 LM148
BP'
C'2
R'2
1/4 LM148
R'_f
100k
R'_L
1/4 LM148
V_O
R'0
R'4

R1C1 = R2C2 = t
R'1C'1 = R'2C'2 = t'

TL/H/7786-14

$f_C = 1\text{ kHz},\ f_S = 2\text{ kHz},\ f_p = 0.543,\ f_Z = 2.14,\ Q = 0.841,\ f'_P = 0.987,\ f'_Z = 4.92,\ Q' = 4.403$, normalized to ripple BW

$$f_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}} \times \frac{1}{t'},\ f_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}} \times \frac{1}{t},\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right) \times \sqrt{\frac{R6}{R5}},\ Q' = \sqrt{\frac{R'6}{R5}}\ \frac{1 + R'4|R'0}{1 + R'6|R'5 + R'6|R_P}$$

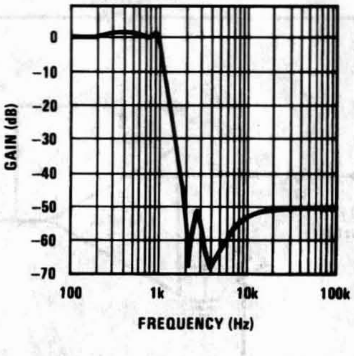
$$R_P = \frac{R_H R_L}{R_H + R_L}$$

Use the BP outputs to tune Q, Q', tune the 2 sections separately

$R1 = R2 = 92.6k,\ R3 = R4 = R5 = 100k,\ R6 = 10k,\ R0 = 107.8k,\ R_L = 100k,\ R_H = 155.1k,$

$R'1 = R'2 = 50.9k,\ R'4 = R'5 = 100k,\ R'6 = 10k,\ R'0 = 5.78k,\ R'_L = 100k,\ R'_H = 248.12k,\ R'f = 100k$. All capacitors are 0.001 µF.

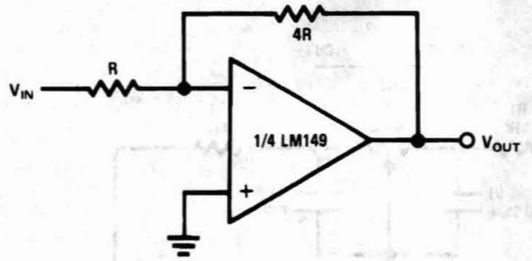
Lowpass Response



TL/H/7786-15

Typical Applications—LM149

Minimum Gain to Insure LM149 Stability


4R
R
V_{IN}
1/4 LM149
V_{OUT}
−
+

TL/H/7786-16

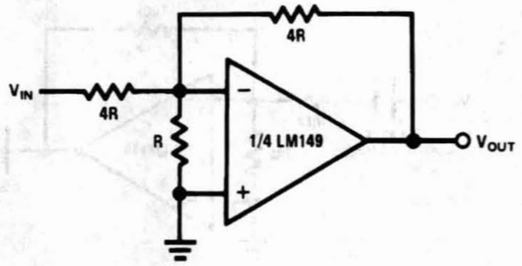
$$A_{CL(S)} = \frac{V_{OUT}}{V_{IN}} = \frac{-4}{\left(1+\frac{5}{A_{OL(s)}}\right)} \cong -4$$

$$V_O\Big|_{V_{IN}=0} \cong \pm 5\,V_{OS}$$

Power BW = 40 kHz

Small Signal BW = G BW/5

The LM149 as a Unity Gain Inverter


4R
V_{IN}
4R
R
1/4 LM149
V_{OUT}
−
+

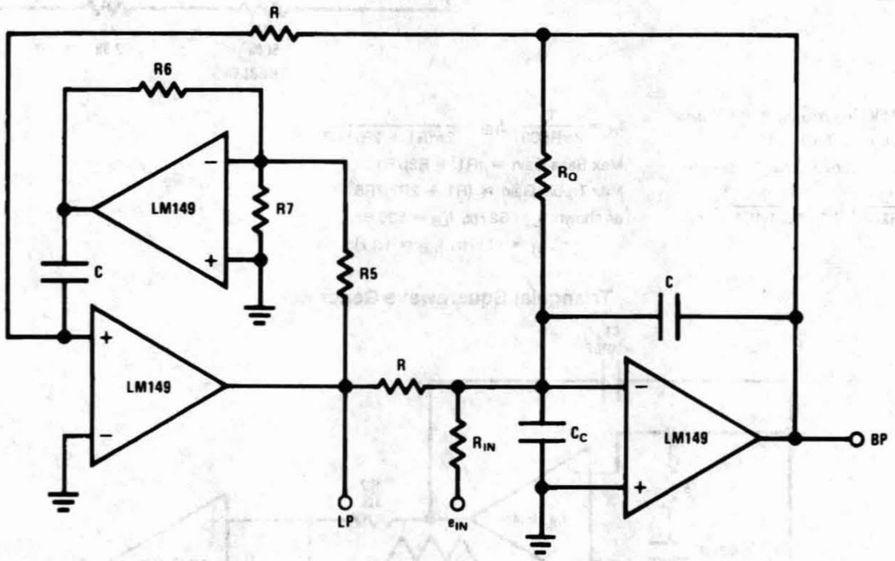
TL/H/7786-17

$$A_{CL(s)} = \frac{V_{OUT}}{V_{IN}} = \left(\frac{-1}{1+\frac{6}{A_{OL(s)}}}\right) \cong -1$$

$$V_O\Big|_{V_{IN}=0} \cong \pm 5\,V_{OS}$$

Small Signal BW = G BW/5

Non-inverting-Integrator Bandpass Filter


R
R6
LM149
R7
R5
C
LM149
R
R_Q
C
R_{IN}
C_C
LM149
BP
LP
e_{IN}
−
+

TL/H/7786-18

For stability purposes: R7 = R6/4, 10R6 = R5, C_C = 10C

$$f_O = \frac{1}{2\pi}\sqrt{\frac{R5}{R6}} \times \frac{1}{RC},\ Q = \frac{R_Q}{R}\sqrt{\frac{R5}{R6}},\ H_{O_{BP}} = \frac{R_Q}{R_{IN}}$$

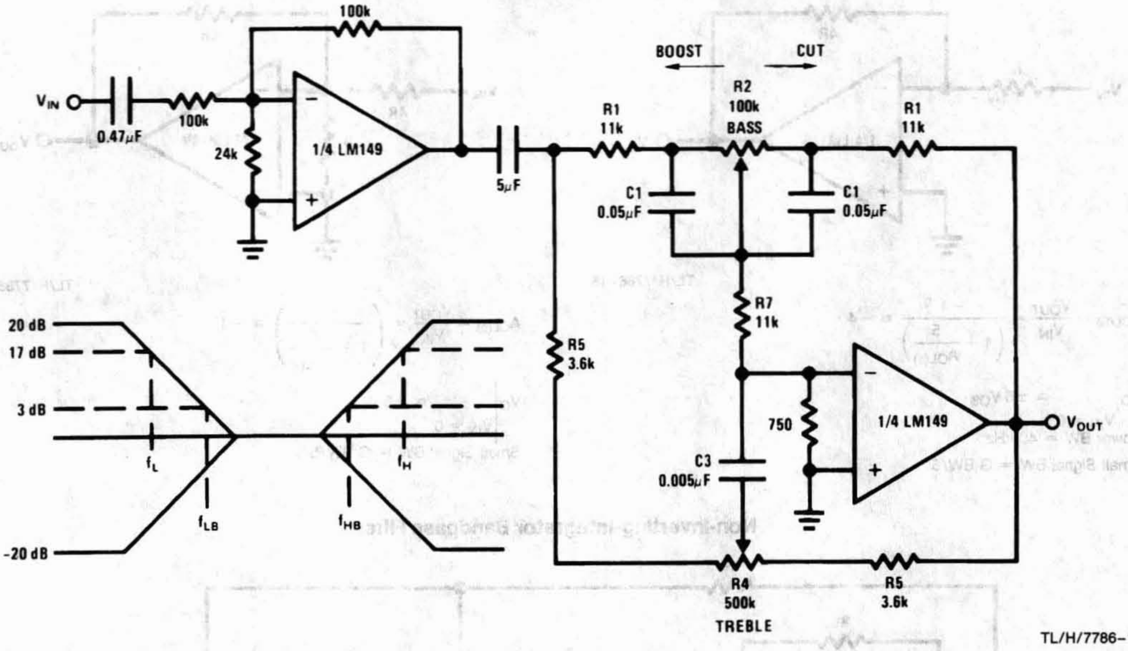
$f_{O(MAX)}$, Q_{MAX} = 20 kHz, 10

Better Q sensitivity with respect to open loop gain variations than the state variable filter.

R7, C_C added for compensation

Typical Applications—LM149 (Continued)

Active Tone Control with Full Output Swing (No Slew Limiting at 20 kHz)

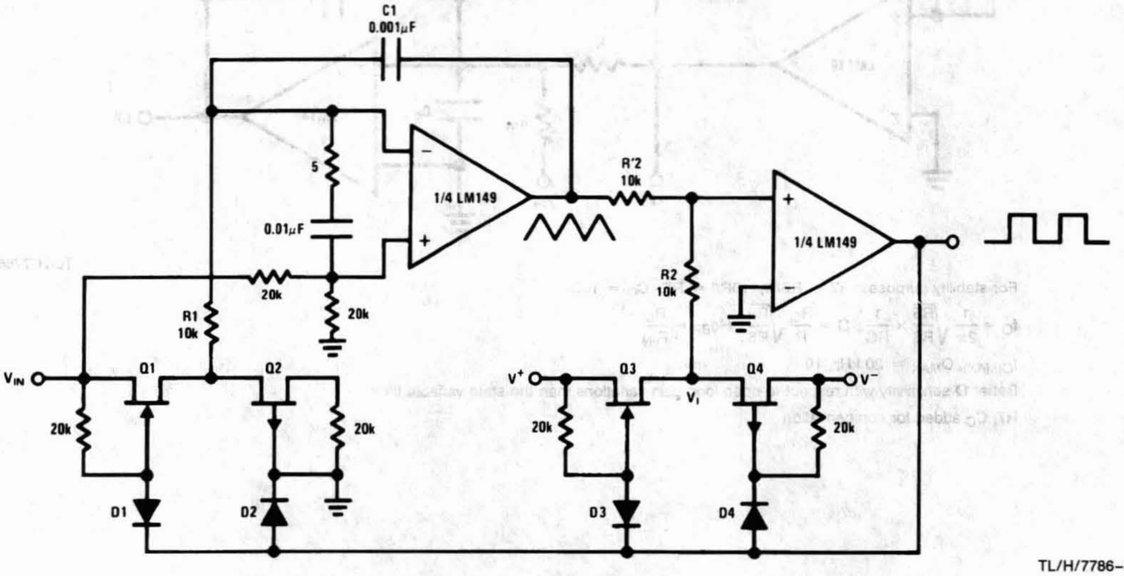

V_IN
0.47µF
100k
100k
24k
1/4 LM149
5µF
BOOST
CUT
R1 11k
R2 100k BASS
R1 11k
C1 0.05µF
C1 0.05µF
R7 11k
R5 3.6k
750
C3 0.005µF
1/4 LM149
V_OUT
R4 500k TREBLE
R5 3.6k
20 dB
17 dB
3 dB
-20 dB
f_L
f_LB
f_H
f_HB

TL/H/7786-19

$V_S = \pm 15V$, $V_{OUT(MAX)} = 9.1\ V_{RMS}$,
$f_{MAX} = 20$ kHz, THD $\le$ 1%
Duplicate the above circuit for stereo
$f_L = \frac{1}{2\pi R2C1}$, $f_{LB} = \frac{1}{2\pi R1C1}$

$f_H = \frac{1}{2\pi R5C3}$, $f_{HB} = \frac{1}{2\pi(R1 + 2R7)\,C3}$
Max Bass Gain $\cong$ (R1 + R2)/R1
Max Treble Gain $\cong$ (R1 + 2R7)/R5
as shown: $f_L \cong 32$ Hz, $f_{LB} \cong 320$ Hz
$f_H \cong 11$ kHz, $f_{HB} \cong 1.1$ Hz

Triangular Squarewave Generator


C1 0.001µF
5
0.01µF
1/4 LM149
20k
20k
R1 10k
V_IN
Q1
Q2
20k
20k
D1
D2
R'2 10k
1/4 LM149
R2 10k
V+
Q3
Q4
V−
V_I
20k
20k
D3
D4

TL/H/7786-20

$f = \frac{K \times V_{IN}}{8V^+C1R1}$, $K = R2/R'2$, $\frac{2V_I}{K} \le 25V$, $V^+ = V^-$, $V_S = \pm 15V$

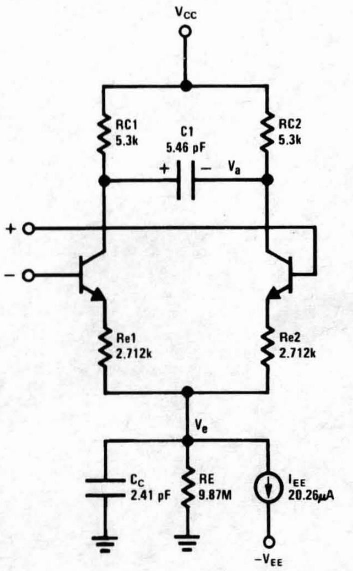
Use LM125 for ±15V supply

The circuit can be used as a low frequency V/F for process control.

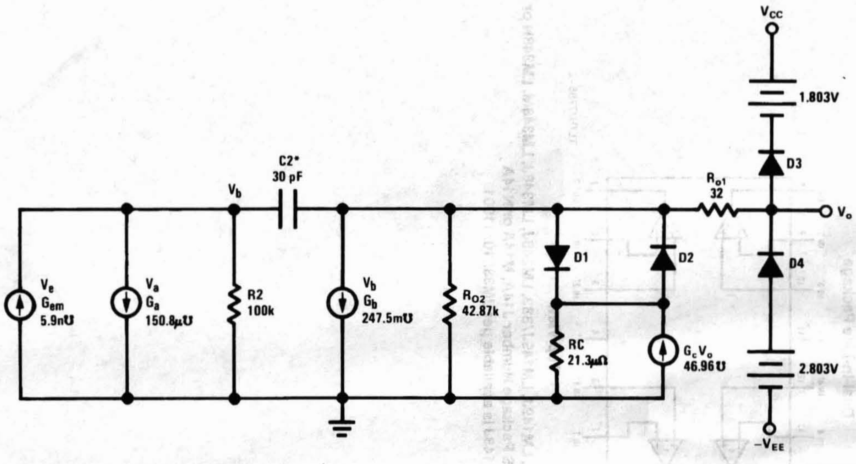
Q1, Q3: KE4393, Q2, Q4: P1087E, D1–D4 = 1N914

Typical Simulation

LM148, LM149, LM741 Macromodel for Computer Simulation


V_{CC}
RC1 5.3k
C1 5.46 pF
RC2 5.3k
+
−
V_a
+
−
Re1 2.712k
Re2 2.712k
V_e
C_C 2.41 pF
RE 9.87M
I_{EE} 20.26μA
−V_{EE}

TL/H/7786–21


V_b
C2* 30 pF
V_e G_{em} 5.9n℧
V_a G_a 150.8μ℧
R2 100k
V_b G_b 247.5m℧
R_{O2} 42.87k
D1
D2
RC 21.3μΩ
G_cV_o 46.96℧
R_{o1} 32
V_{CC}
1.803V
D3
V_o
D4
2.803V
−V_{EE}

TL/H/7786–22

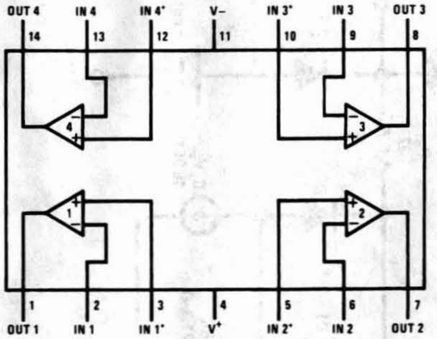
$\beta_{o1} = 112$ $\quad I_S = 8 \times 10^{-16}$

$\beta_{o2} = 144$ $\quad$ *C2 = 6 pF for LM149

For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974

Connection Diagram

Dual-In-Line Package


OUT 4
IN 4⁻
IN 4⁺
V−
IN 3⁺
IN 3⁻
OUT 3
14
13
12
11
10
9
8
4
3
1
2
1
2
3
4
5
6
7
OUT 1
IN 1⁻
IN 1⁺
V⁺
IN 2⁺
IN 2⁻
OUT 2

TL/H/7786–2

Top View

Order Number LM148J, LM148J/883, LM149J, LM149J/883, LM248J, LM348J, LM348M, LM348N or LM349N
See NS Package Number J14A, M14A or N14A
LM148J is available per JM38510/11001

National Semiconductor

LM158/LM258/LM358/LM2904
Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

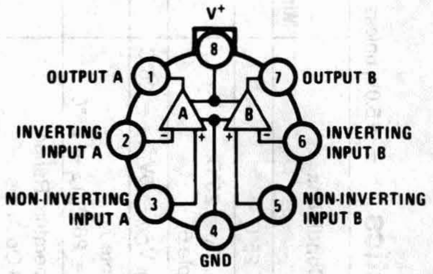
- Two internally compensated op amps in a single package
- Eliminates need for dual supplies
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3V to 32V
  - or dual supplies ±1.5V to ±16V
- Very low supply current drain (500 μA)—essentially independent of supply voltage
- Low input offset voltage 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to $V^+ - 1.5V$

Connection Diagrams (Top Views)

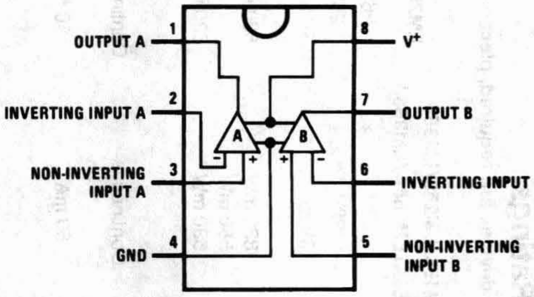
Metal Can Package



TL/H/7787–1

Order Number LM158AH, LM158AH/883*, LM158H, LM158H/883*, LM258H or LM358H
See NS Package Number H08C

DIP/SO Package



TL/H/7787–2

Order Number LM158J, LM158J/883*, LM158AJ or LM158AJ/883*
See NS Package Number J08A
Order Number LM358M, LM358AM or LM2904M
See NS Package Number M08A
Order Number LM358AN, LM358N or LM2904N
See NS Package Number N08E

*LM158 is available per SMD #5962-8771001
LM158A is available per SMD #5962-8771002

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP	830 mW	830 mW
Metal Can	550 mW	
Small Outline Package (M)	530 mW	530 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA	50 mA

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature, DIP (Soldering, 10 seconds)	260°C	260°C
Lead Temperature, Metal Can (Soldering, 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5), $T_A = 25°C$		1	2		2	3		2	5		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, $V_{CM} = 0V$, (Note 6)		20	50		45	100		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		5	30		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 7) (LM2904, $V^+ = 26V$), $T_A = 25°C$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps $V^+ = 30V$ (LM2904 $V^+ = 26V$) $V^+ = 5V$		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2	mA mA

Electrical Characteristics (Continued) V+ = +5.0V, Note 4, unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Large Signal Voltage Gain		$V^+ = 15V$, $T_A = 25°C$, $R_L \geq 2\ k\Omega$, (For $V_O = 1V$ to 11V)	50	100		25	100		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio		$T_A = 25°C$, $V_{CM} = 0V$ to $V^+ - 1.5V$	70	85		65	85		70	85		65	85		50	70		dB
Power Supply Rejection Ratio		$V^+ = 5V$ to 30V (LM2904, $V^+ = 5V$ to 26V), $T_A = 25°C$	65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8)		−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}{}^+ = 1V$, $V_{IN}{}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		mA
	Sink	$V_{IN}{}^- = 1V$, $V_{IN}{}^+ = 0V$ $V^+ = 15V$, $T_A = 25°C$, $V_O = 2V$	10	20		10	20		10	20		10	20		10	20		mA
		$V_{IN}{}^- = 1V$, $V_{IN}{}^+ = 0V$ $T_A = 25°C$, $V_O = 200\ mV$, $V^+ = 15V$	12	50		12	50		12	50		12	50		12	50		μA
Short Circuit to Ground		$T_A = 25°C$, (Note 2), $V^+ = 15V$		40	60		40	60		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 5)			4			5			7			9			10	mV
Input Offset Voltage Drift		$R_S = 0\Omega$		7	15		7	20		7			7			7		μV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100			150		45	200	nA
Input Offset Current Drift		$R_S = 0\Omega$		10	200		10	300		10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300		40	500		40	500	nA

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Common-Mode Voltage Range		$V^+ = 30$ V, (Note 7) (LM2904, $V^+ = 26V$)		0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V
Large Signal Voltage Gain		$V^+ = +15V$ ($V_O = 1V$ to 11V) $R_L \geq 2\ k\Omega$		25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30V$ (LM2904, $V^+ = 26V$)	$R_L = 2\ k\Omega$	26			26			26			26			22			V
			$R_L = 10\ k\Omega$	27	28		27	28		27	28		27	28		23	24		V
	V_{OL}	$V^+ = 5V$, $R_L = 10\ k\Omega$			5	20		5	20		5	20		5	20		5	100	mV
Output Current	Source	$V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$		10	20		10	20		10	20		10	20		10	20		mA
	Sink	$V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$		10	15		5	8		5	8		5	8		5	8		mA

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 120°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short cirucits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM358/LM358A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2904 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$) at 25°C. For LM2904, V^+ from 5V to 26V.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2904), independent of the magnitude of V^+.

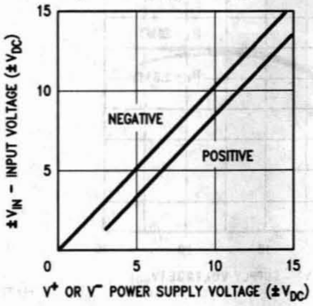
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

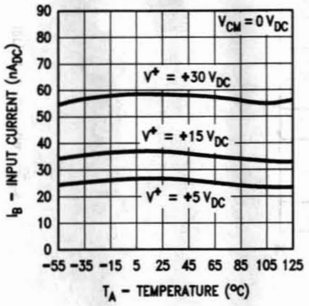
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

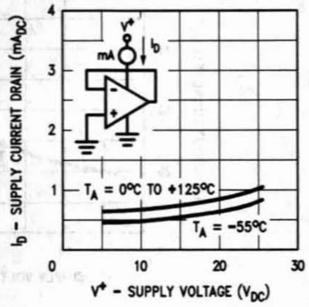
Input Voltage Range



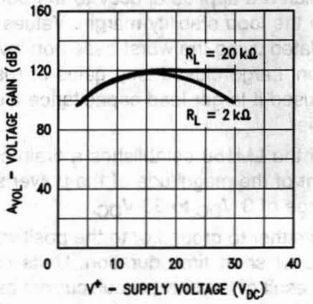
Input Current



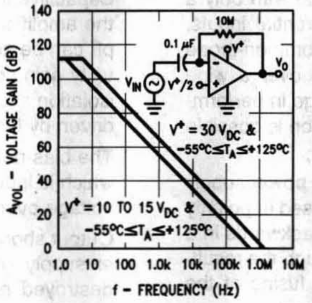
Supply Current



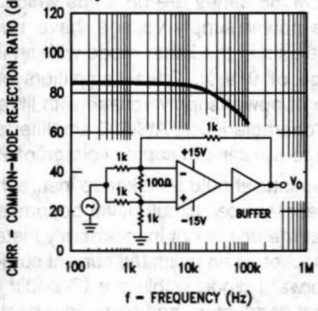
Voltage Gain



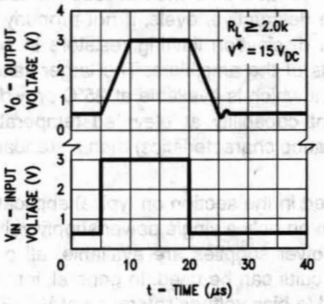
Open Loop Frequency Response



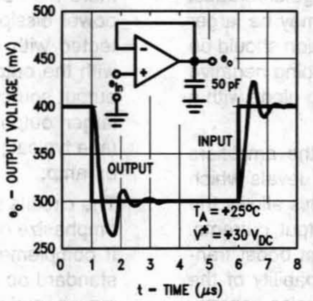
Common-Mode Rejection Ratio



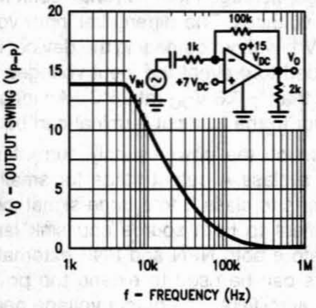
Voltage Follower Pulse Response



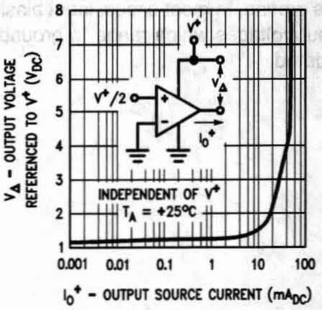
Voltage Follower Pulse Response (Small Signal)



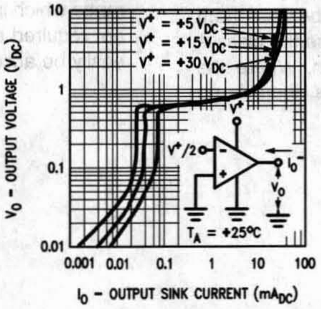
Large Signal Frequency Response



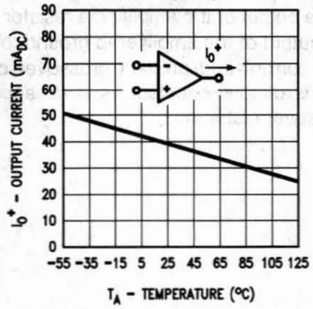
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

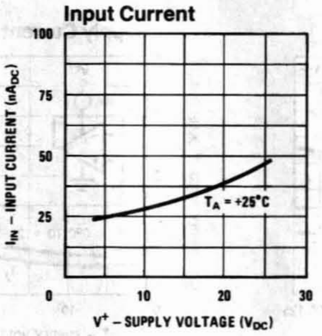


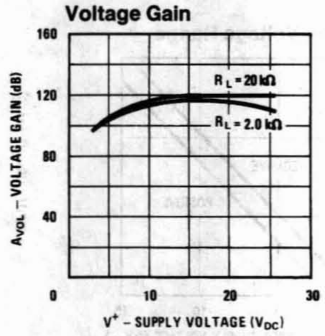
Current Limiting



TL/H/7787–4

Typical Performance Characteristics (Continued) (LM2902 only)


Input Current


Voltage Gain

TL/H/7787–5

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

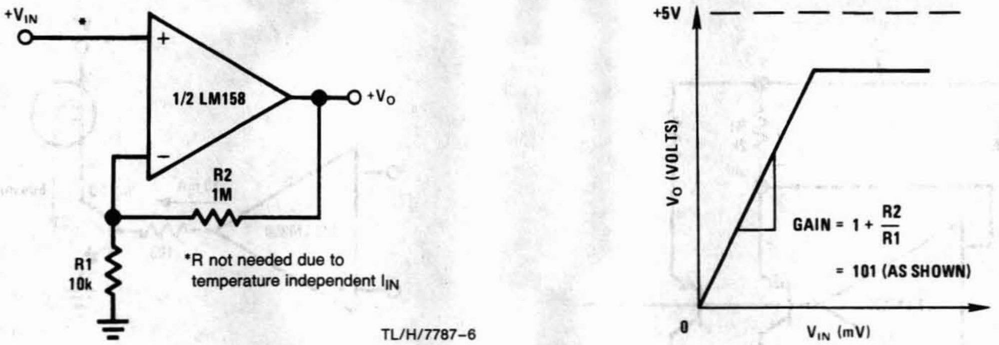
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

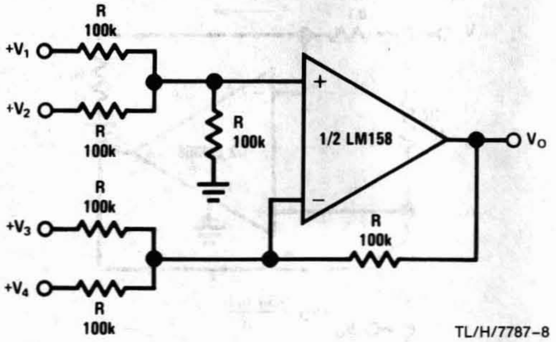
Non-Inverting DC Gain (0V Input = 0V Output)


$+V_{IN}$
*
1/2 LM158
$+V_O$
R2
1M
R1
10k
*R not needed due to temperature independent I_{IN}
+5V
V_O (VOLTS)
GAIN = $1 + \frac{R2}{R1}$
= 101 (AS SHOWN)
0
V_{IN} (mV)

TL/H/7787-6

TL/H/7787-7

DC Summing Amplifier (V_{IN}'S $\geq$ 0 V_{DC} and $V_O \geq 0\ V_{DC}$)

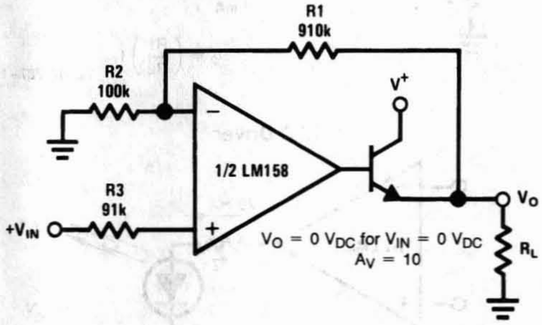

R
100k
$+V_1$
$+V_2$
R
100k
R
100k
1/2 LM158
V_O
R
100k
$+V_3$
$+V_4$
R
100k
R
100k
R
100k

TL/H/7787-8

Where: $V_O = V_1 + V_2 + V_3 + V_4$

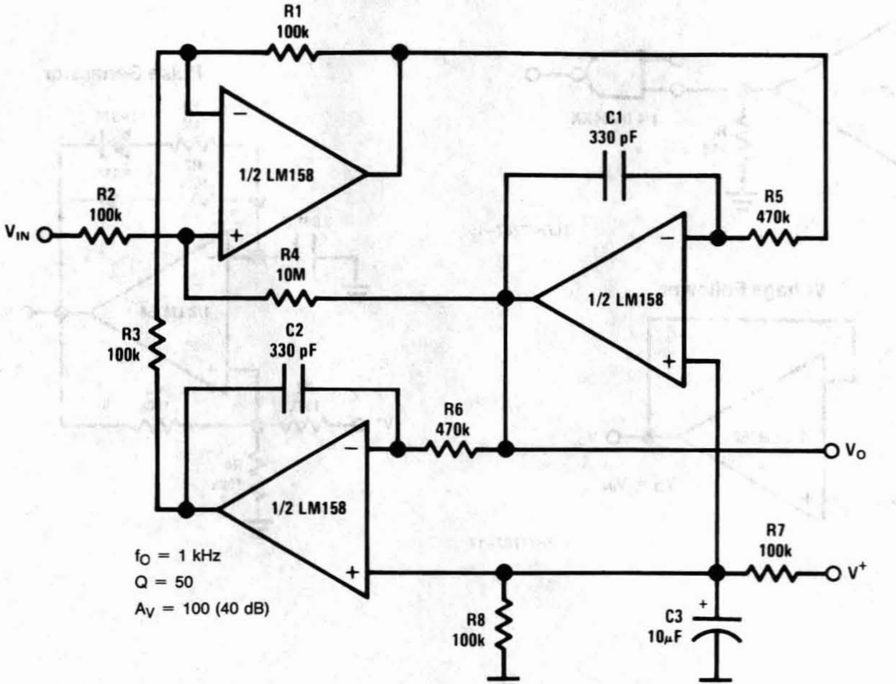
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier


R1
910k
R2
100k
V^+
1/2 LM158
R3
91k
$+V_{IN}$
V_O
$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$
$A_V = 10$
R_L

TL/H/7787-9

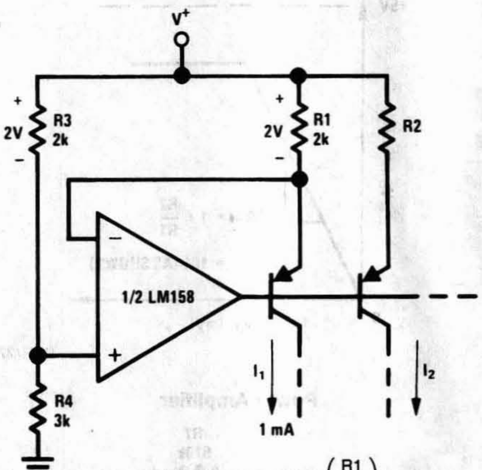
"BI-QUAD" RC Active Bandpass Filter


R1
100k
1/2 LM158
C1
330 pF
R2
100k
V_{IN}
R5
470k
R4
10M
1/2 LM158
R3
100k
C2
330 pF
R6
470k
V_O
1/2 LM158
$f_O = 1$ kHz
Q = 50
$A_V = 100$ (40 dB)
R7
100k
V^+
R8
100k
C3
10µF

TL/H/7787-10

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

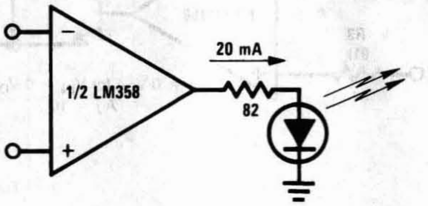
Fixed Current Sources


V+
+
2V
R3
2k
−
+
2V
R1
2k
−
R2
−
+
1/2 LM158
I1
1 mA
I2
R4
3k

$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

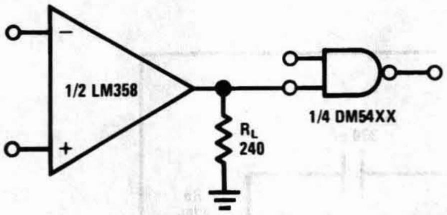
TL/H/7787-11

LED Driver


−
+
1/2 LM358
20 mA
82

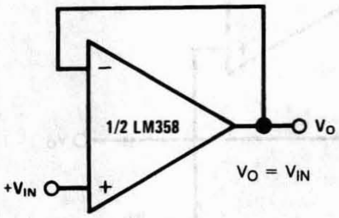
TL/H/7787-13

Driving TTL


−
+
1/2 LM358
RL
240
1/4 DM54XX

TL/H/7787-15

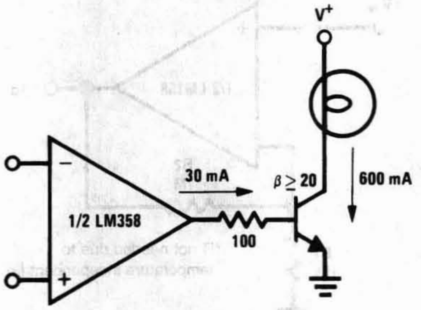
Voltage Follower


−
+
1/2 LM358
VO
+VIN

$V_O = V_{IN}$

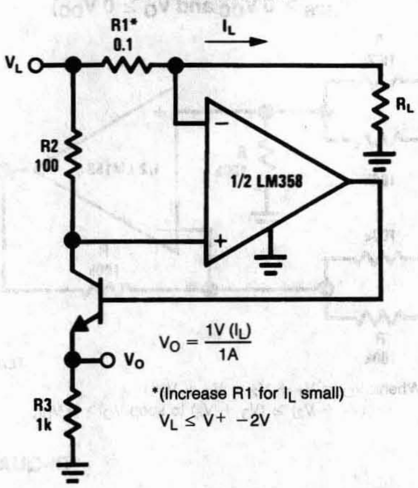
TL/H/7787-17

Lamp Driver


V+
−
+
1/2 LM358
30 mA
100
β ≥ 20
600 mA

TL/H/7787-12

Current Monitor


R1*
0.1
IL
VL
RL
R2
100
−
+
1/2 LM358
VO
R3
1k

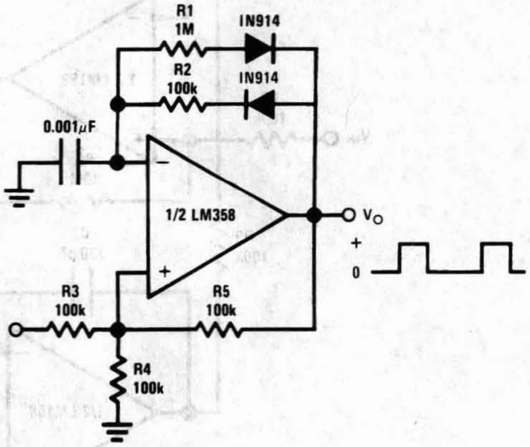
$$V_O = \frac{1V\,(I_L)}{1A}$$

*(Increase R1 for I_L small)

$V_L \le V^+ - 2V$

TL/H/7787-14

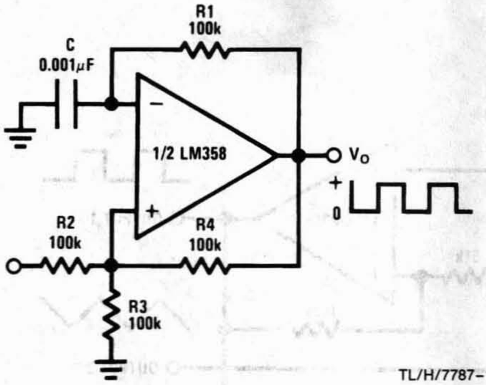
Pulse Generator


R1
1M
IN914
R2
100k
IN914
0.001μF
−
+
1/2 LM358
VO
+
0
R3
100k
V+
R5
100k
R4
100k

TL/H/7787-16

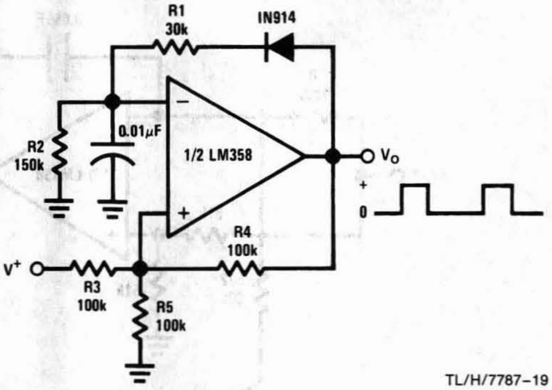
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Squarewave Oscillator


R1
100k
C
0.001μF
1/2 LM358
V_O
+
0
R2
100k
R4
100k
V^+
R3
100k

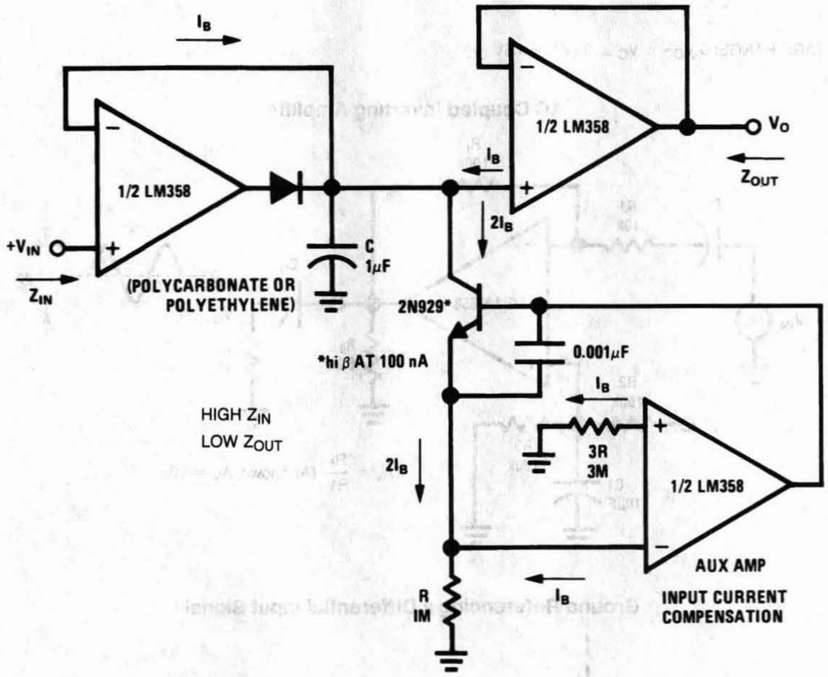
TL/H/7787–18

Pulse Generator


R1
30k
IN914
0.01μF
R2
150k
1/2 LM358
V_O
+
0
R4
100k
V^+
R3
100k
R5
100k

TL/H/7787–19

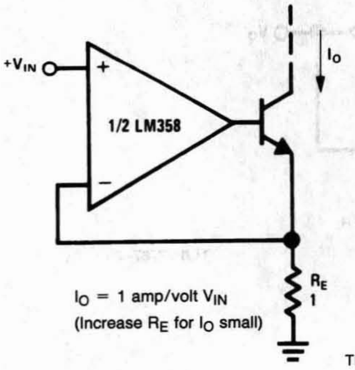
Low Drift Peak Detector


I_B
1/2 LM358
1/2 LM358
V_O
I_B
Z_{OUT}
$2I_B$
$+V_{IN}$
Z_{IN}
C
1μF
(POLYCARBONATE OR POLYETHYLENE)
2N929*
0.001μF
*hi β AT 100 nA
I_B
3R
3M
1/2 LM358
$2I_B$
AUX AMP
R
IM
I_B
INPUT CURRENT COMPENSATION

HIGH Z_{IN}
LOW Z_{OUT}

TL/H/7787–20

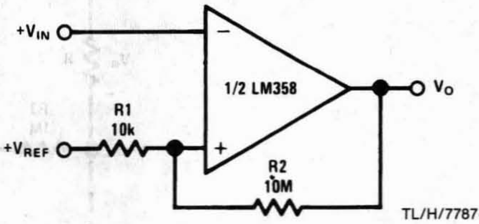
High Compliance Current Sink


$+V_{IN}$
1/2 LM358
I_O
R_E
1

I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

TL/H/7787–21

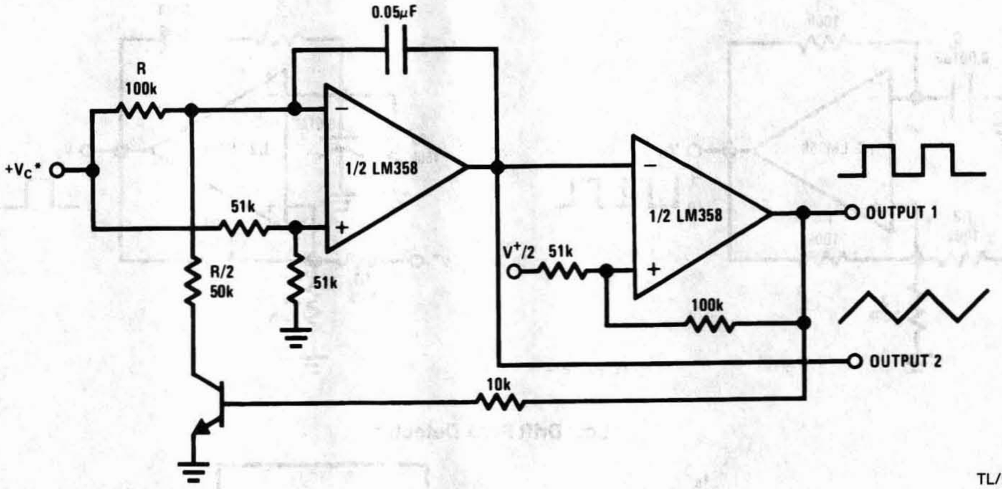
Comparator with Hysteresis


$+V_{IN}$
1/2 LM358
V_O
R1
10k
$+V_{REF}$
R2
10M

TL/H/7787–22

Typical Single-Supply Applications $(V^+ = 5.0\ V_{DC})$ (Continued)

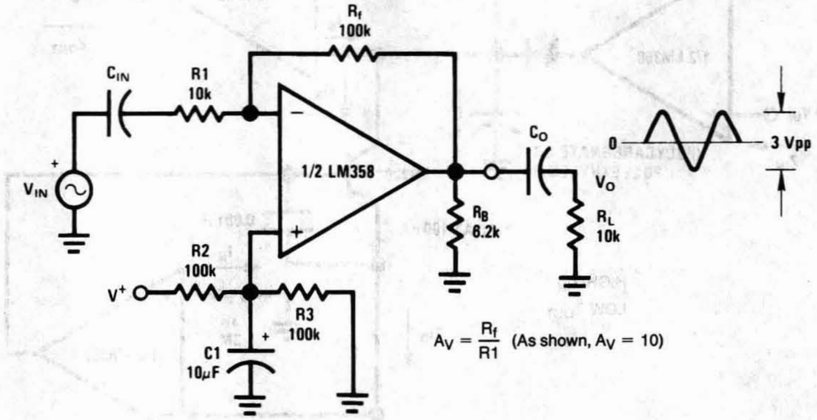
Voltage Controlled Oscillator (VCO)


0.05μF
R
100k
+VC*
1/2 LM358
51k
R/2
50k
51k
1/2 LM358
V+/2
51k
100k
OUTPUT 1
OUTPUT 2
10k

TL/H/7787-23

*WIDE CONTROL VOLTAGE RANGE: $0\ V_{DC} \le V_C \le 2\ (V^+ - 1.5V_{DC})$

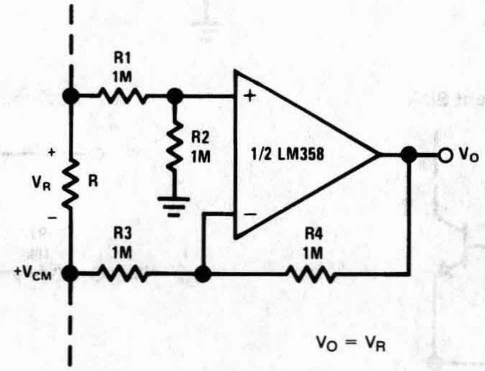
AC Coupled Inverting Amplifier


Rf
100k
CIN
R1
10k
VIN
1/2 LM358
CO
0
3 Vpp
VO
RB
6.2k
RL
10k
R2
100k
V+
R3
100k
C1
10μF

$A_V = \frac{R_f}{R1}$ (As shown, $A_V = 10$)

TL/H/7787-24

Ground Referencing a Differential Input Signal

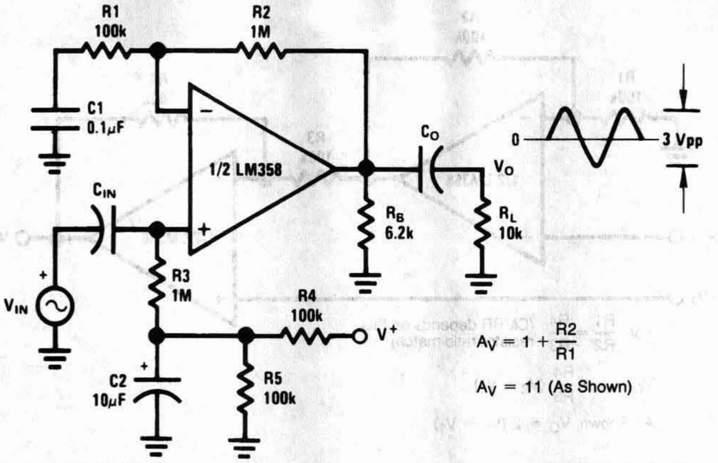

R1
1M
R2
1M
1/2 LM358
VO
VR
R
+VCM
R3
1M
R4
1M

$V_O = V_R$

TL/H/7787-25

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

AC Coupled Non-Inverting Amplifier

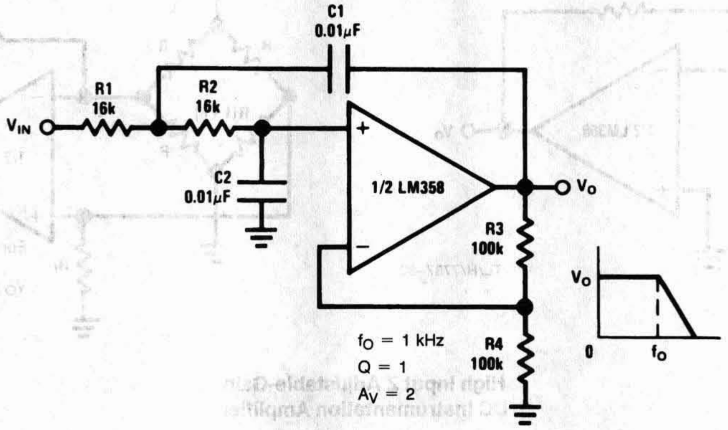

R1
100k
R2
1M
C1
0.1μF
1/2 LM358
C_{IN}
C_O
V_O
0
3 Vpp
R_B
6.2k
R_L
10k
V_{IN}
R3
1M
R4
100k
V^+
C2
10μF
R5
100k

$A_V = 1 + \frac{R2}{R1}$

$A_V = 11$ (As Shown)

TL/H/7787–26

DC Coupled Low-Pass RC Active Filter


C1
0.01μF
R1
16k
R2
16k
V_{IN}
C2
0.01μF
1/2 LM358
V_O
R3
100k
R4
100k
V_O
0
f_O

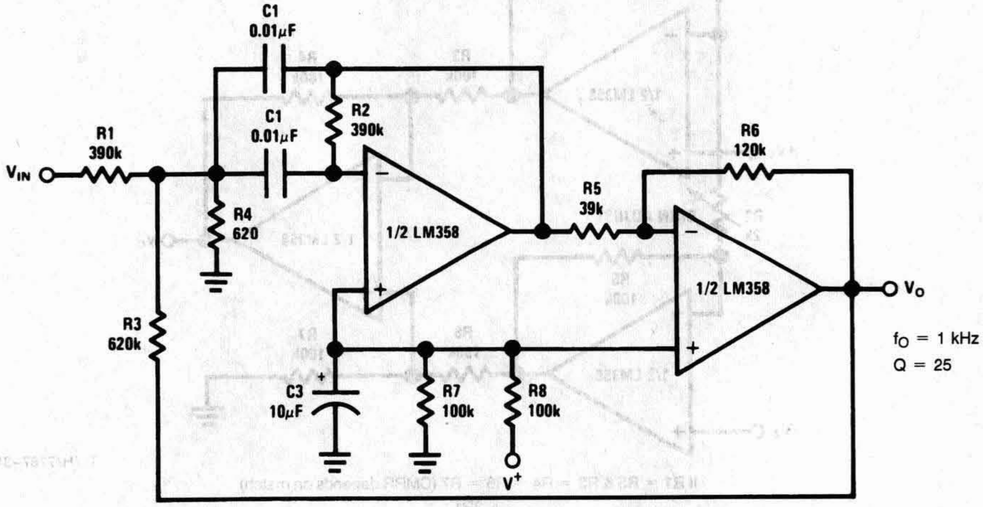
$f_O = 1$ kHz

$Q = 1$

$A_V = 2$

TL/H/7787–27

Bandpass Active Filter


C1
0.01μF
C1
0.01μF
R2
390k
R1
390k
V_{IN}
R4
620
1/2 LM358
R5
39k
R6
120k
1/2 LM358
V_O
R3
620k
C3
10μF
R7
100k
R8
100k
V^+

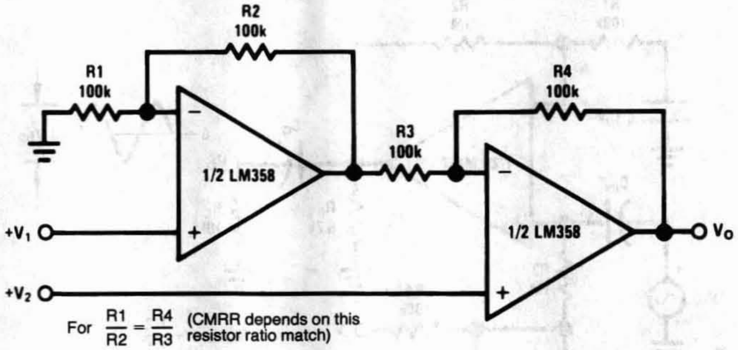
$f_O = 1$ kHz

$Q = 25$

TL/H/7787–28

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

High Input Z, DC Differential Amplifier


R2
100k
R1
100k
R4
100k
R3
100k
1/2 LM358
1/2 LM358
+V1
+V2
Vo

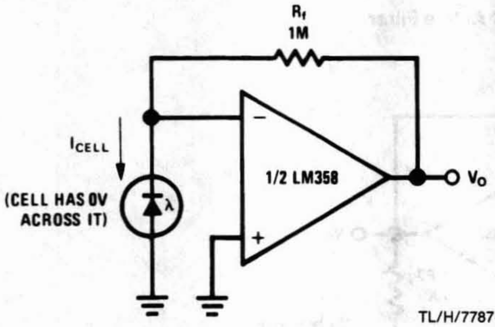
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3} (V_2 - V_1)$

As Shown: $V_O = 2 (V_2 - V_1)$

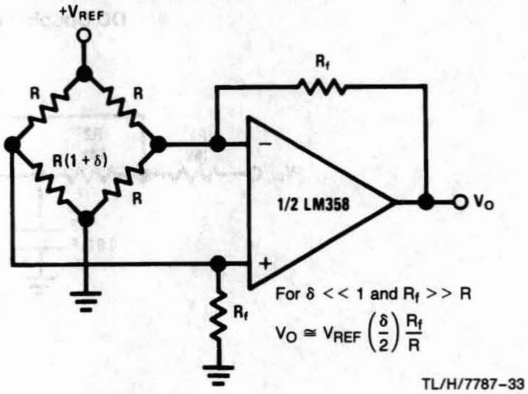
TL/H/7787-29

Photo Voltaic-Cell Amplifier


Rf
1M
ICELL
(CELL HAS 0V ACROSS IT)
λ
1/2 LM358
Vo

TL/H/7787-30

Bridge Current Amplifier

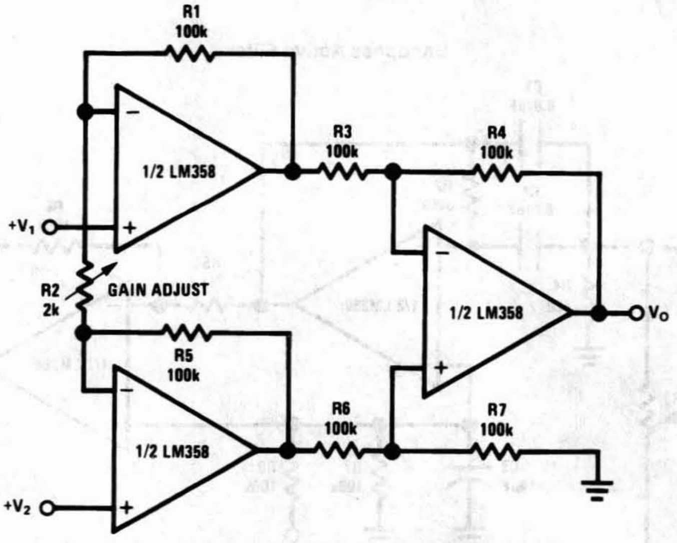

+VREF
R
R
R(1 + δ)
R
Rf
1/2 LM358
Vo
Rf

For $\delta << 1$ and $R_f >> R$

$V_O \cong V_{REF} \left(\frac{\delta}{2}\right) \frac{R_f}{R}$

TL/H/7787-33

High Input Z Adjustable-Gain DC Instrumentation Amplifier


R1
100k
1/2 LM358
R3
100k
R4
100k
+V1
R2
2k
GAIN ADJUST
R5
100k
1/2 LM358
Vo
R6
100k
R7
100k
1/2 LM358
+V2

TL/H/7787-31

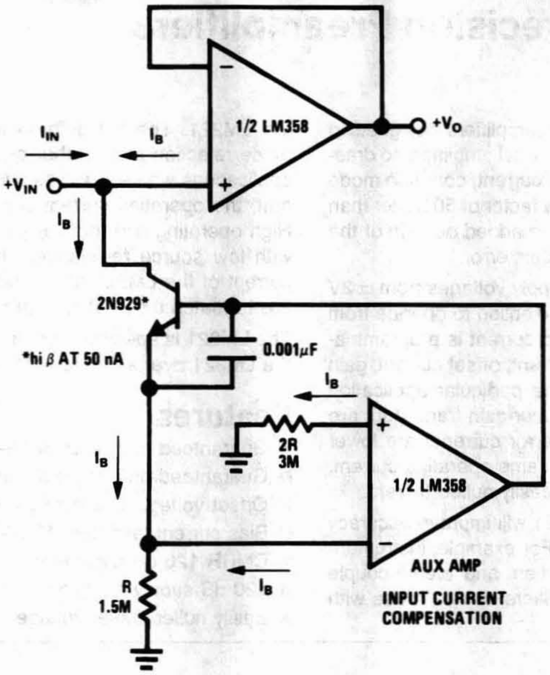
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$V_O = 1 + \frac{2R1}{R2} (V_2 - V_1)$

As shown $V_O = 101 (V_2 - V_1)$

Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)

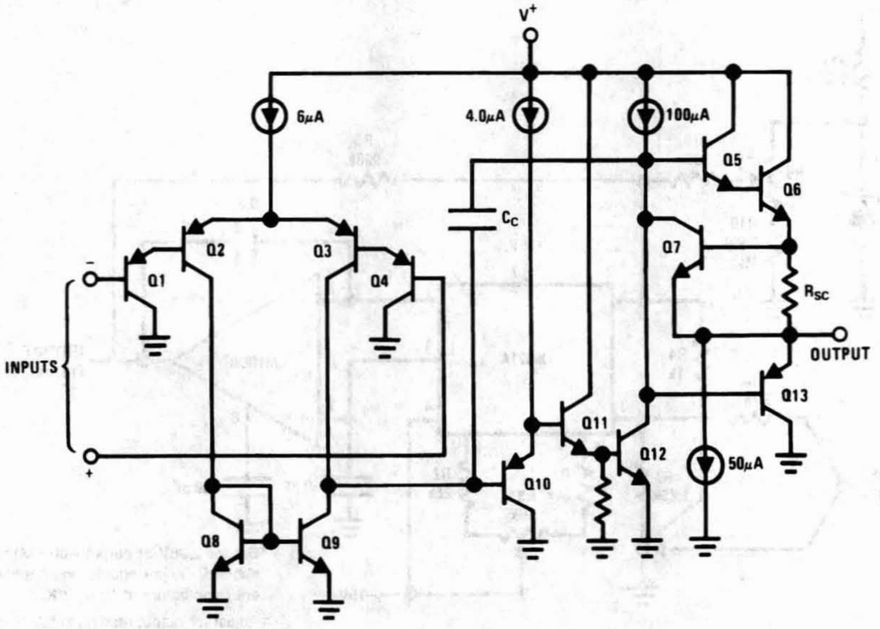
Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



−
+
1/2 LM358
$+V_O$
I_{IN}
I_B
$+V_{IN}$
I_B
2N929*
0.001μF
*hi β AT 50 nA
I_B
+
2R
3M
1/2 LM358
−
I_B
AUX AMP
INPUT CURRENT
COMPENSATION
R
1.5M
I_B

TL/H/7787-32

Schematic Diagram (Each Amplifier)



V^+
6μA
4.0μA
100μA
Q5
Q6
C_C
Q2
Q3
Q1
Q4
Q7
R_{SC}
OUTPUT
INPUTS
−
+
Q13
Q11
Q12
50μA
Q10
Q8
Q9

TL/H/7787-3

National Semiconductor

LM221/LM321 Precision Preamplifiers

General Description

The LM221 series are precision preamplifiers designed to operate with general purpose operational amplifiers to drastically decrease dc errors. Drift, bias current, common mode and supply rejection are more than a factor of 50 better than standard op amps alone. Further, the added dc gain of the LM221 decreases the closed loop gain error.

The LM221 series operates with supply voltages from ±3V to ±20V and has sufficient supply rejection to operate from unregulated supplies. The operating current is programmable from 5 μA to 200 μA so bias current, offset current, gain and noise can be optimized for the particular application while still realizing very low drift. Super-gain transistors are used for the input stage so input error currents are lower than conventional amplifiers at the same operating current. Further, the initial offset voltage is easily nulled to zero.

The extremely low drift of the LM221 will improve accuracy on almost any precision dc circuit. For example, instrumentation amplifier, strain gauge amplifiers and thermocouple amplifiers now using chopper amplifiers can be made with the LM221. The full differential input and high common-mode rejection are another advantage over choppers. For applications where low bias current is more important than drift, the operating current can be reduced to low values. High operating currents can be used for low voltage noise with low source resistance. The programmable operating current of the LM221 allows tailoring the input characteristics to match those of specialized op amps.

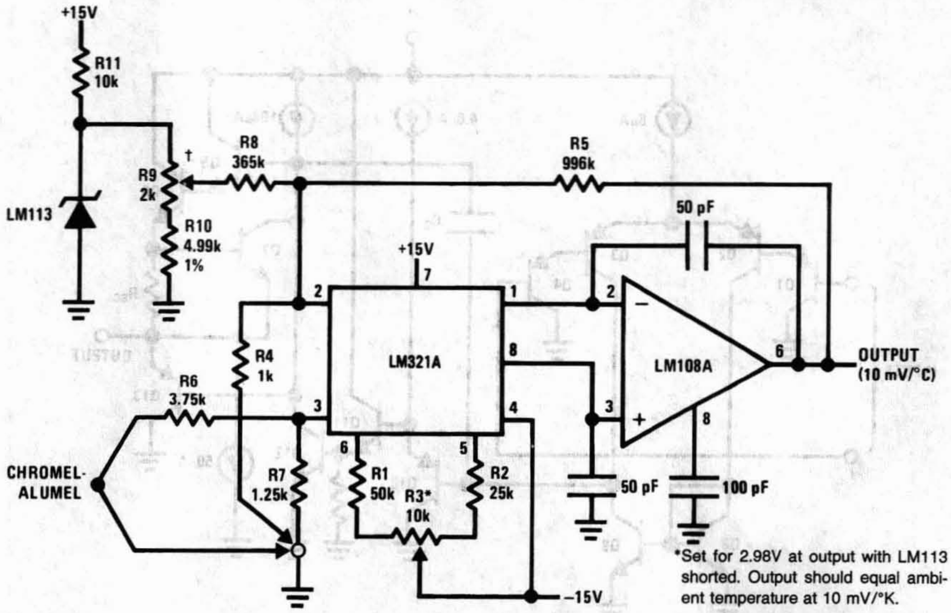
The LM221 is specified over a −25°C to +85°C range and the LM321 over a 0°C to +70°C temperature range.

Features

- Guaranteed drift of LM321A—0.2 μV/°C
- Guaranteed drift of LM221 series—1 μV/°C
- Offset voltage less than 0.4 mV
- Bias current less than 10 nA at 10 μA operating current
- CMRR 126 dB minimum
- 120 dB supply rejection
- Easily nulled offset voltage

Typical Applications

Thermocouple Amplifier with Cold Junction Compensation



*Set for 2.98V at output with LM113 shorted. Output should equal ambient temperature at 10 mV/°K.

†Adjust for output reading in °C.

TL/H/7769–1

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Notes 2 and 3)	±15V
Input Voltage (Note 3)	±15V

Operating Temperature Range	
LM321A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD rating to be determined.	

Electrical Characteristics (Note 4) LM321A

Parameter	Conditions	LM321A			Units
		Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, 6.4k ≤ R_{SET} ≤ 70k		0.2	0.4	mV
Input Offset Current	T_A = 25°C, R_{SET} = 70k R_{SET} = 6.4k		0.3	0.5 5	nA nA
Input Bias Current	T_A = 25°C, R_{SET} = 70k R_{SET} = 6.4k		5 50	15 150	nA nA
Input Resistance	T_A = 25°C, R_{SET} = 70k R_{SET} = 6.4k	2 0.2	8		MΩ MΩ
Supply Current	T_A = 25°C, R_{SET} = 70k		0.8	2.2	mA
Input Offset Voltage	6.4k ≤ R_{SET} ≤ 70k		0.5	0.65	mV
Input Bias Current	R_{SET} = 70k R_{SET} = 6.4k		15 150	25 250	nA nA
Input Offset Current	R_{SET} = 70k R_{SET} = 6.4k		0.5 5	1 10	nA nA
Input Offset Current Drift	R_{SET} = 70k		3		pA/°C
Average Temperature Coefficient of Input Offset Voltage	R_S ≤ 200Ω, 6.4k ≤ R_{SET} ≤ 70k Offset Voltage Nulled		0.07	0.2	µV/°C
Long Term Stability			3		µV/yr
Supply Current			1	3.5	mA
Input Voltage Range	V_S = ±15V, (Note 5) R_{SET} = 70k R_{SET} = 6.4k	±13 +7, −13			V V
Common-Mode Rejection Ratio	R_{SET} = 70k R_{SET} = 6.4k	126 120	140 130		dB dB
Supply Voltage Rejection Ratio	R_{SET} = 70k R_{SET} = 6.4k	118 114	126 120		dB dB
Voltage Gain	T_A = 25°C, R_{SET} = 70k, R_L > 3 MΩ	12	20		V/V
Noise	R_{SET} = 70k, R_{SOURCE} = 0		8		nV/√Hz

Note 1: The maximum junction temperature of the LM321A is 85°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 18°C/W, junction to case.

Note 2: The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for ±5 ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C, unless otherwise specified. With the LM221A, however all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, and for the LM321A the specifications apply over a 0°C to +70°C temperature range.

Note 5: External precision resistor —0.1%— can be placed from pins 1 and 8 to 7 increase positive common-mode range.

Note 6: See RETS121X for LM121H/883 military specs and RET121AX for LM121AH/883 military specs.

1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Notes 2 and 3)	±15V
Input Voltage (Note 3)	±15V

Operating Temperature Range	
LM221, LM121A (-883), LM121 (-883)	−25°C to +85°C
LM321, LM321A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

Electrical Characteristics (Note 4) LM221, LM321

Parameter	Conditions	LM221			LM321			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C, 6.4k \le R_{SET} \le 70k$			0.7			1.5	mV
Input Offset Current	$T_A = 25°C$, $R_{SET} = 70k$ $R_{SET} = 6.4k$			 1 10			 2 20	 nA nA
Input Bias Current	$T_A = 25°C$, $R_{SET} = 70k$ $R_{SET} = 6.4k$			 10 100			 18 180	 nA nA
Input Resistance	$T_A = 25°C$, $R_{SET} = 70k$ $R_{SET} = 6.4k$	 4 0.4			 2 0.2			 MΩ MΩ
Supply Current	$T_A = 25°C, R_{SET} = 70k$			1.5			2.2	mA
Input Offset Voltage	$6.4k \le R_{SET} \le 70k$			1.0			2.5	mV
Input Bias Current	$R_{SET} = 70k$ $R_{SET} = 6.4k$			30 300			28 280	nA nA
Input Offset Current	$R_{SET} = 70k$ $R_{SET} = 6.4k$			3 30			4 40	nA nA
Input Offset Current Drift	$R_{SET} = 70k$		3			3		pA/°C
Average Temperature Coefficient of Input Offset Voltage	$R_S \le 200\Omega, 6.4k \le R_{SET} \le 70k$ Offset Voltage Nulled			1			1	μV/°C
Long Term Stability			5			5		μV/yr
Supply Current				2.5			3.5	mA
Input Voltage Range	$V_S = \pm15V$, (Note 5) $R_{SET} = 70k$ $R_{SET} = 6.4k$	 ±13 +7, −13			 ±13 +7, −13			 V V
Common-Mode Rejection Ratio	$R_{SET} = 70k$ $R_{SET} = 6.4k$	120 114			114 114			dB dB
Supply Voltage Rejection Ratio	$R_{SET} = 70k$ $R_{SET} = 6.4k$	120 114			114 114			dB dB
Voltage Gain	$T_A = 25°C, R_{SET} = 70k$, $R_L > 3\ M\Omega$	 16			 12			 V/V
Noise	$R_{SET} = 70k, R_{SOURCE} = 0$		8			8		$nV/\sqrt{Hz}$

Note 1: The maximum junction temperature of the LM221 is 100°C. The maximum junction temperature of the LM321 is 85°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 18°C/W, junction to case.

Note 2: The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

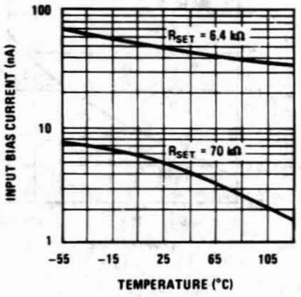
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm5 \le V_S \le \pm20V$ and $-55°C \le T_A \le +125°C$, unless otherwise specified. With the LM221, however all temperature specifications are limited to $-25°C \le T_A \le +85°C$, and for the LM321 the specifications apply over a 0°C to +70°C temperature range.

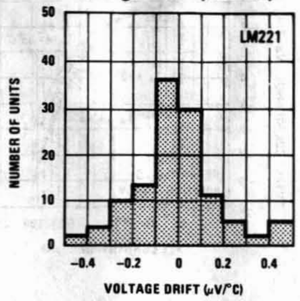
Note 5: External precision resistor —0.1%— can be placed from pins 1 and 8 to 7 increase positive common-mode range.

Typical Performance Characteristics

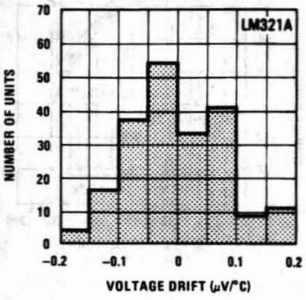
Input Bias Current



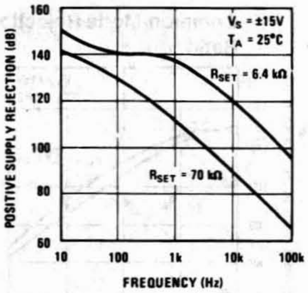
Distribution of Offset Voltage Drift (Nulled)



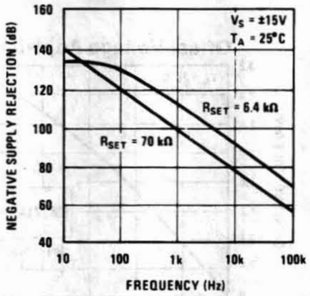
Distribution of Offset Voltage Drift (Nulled)



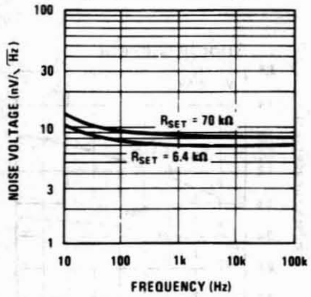
Positive Power Supply Rejection



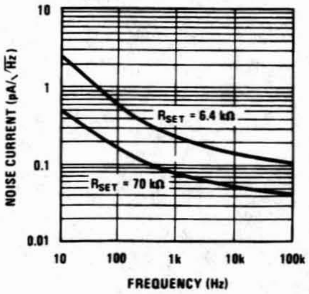
Negative Power Supply Rejection



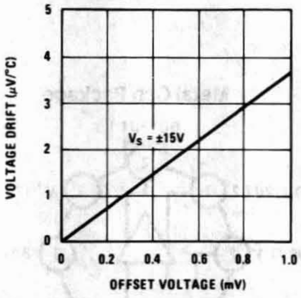
Input Noise Voltage



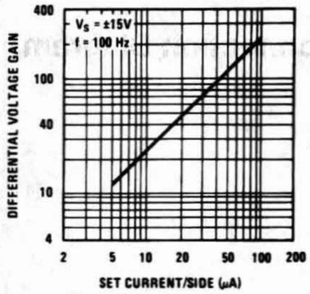
Input Noise Current



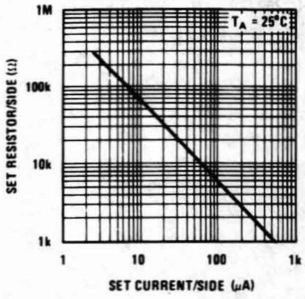
Voltage Drift



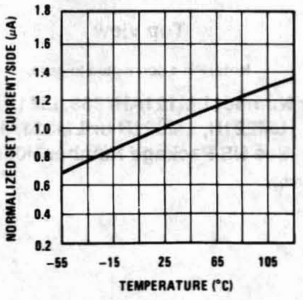
Differential Voltage Gain



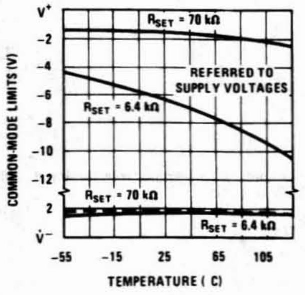
Set Resistor and Set Current



Set Current



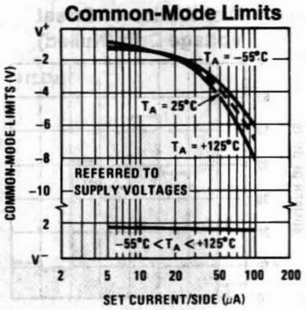
Common-Mode Limits



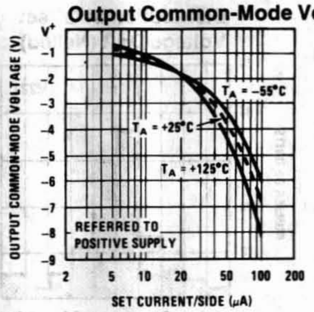
TL/H/7769–9

Typical Performance Characteristics (Continued)

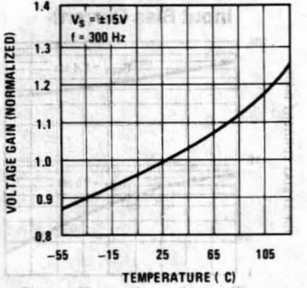
Common-Mode Limits



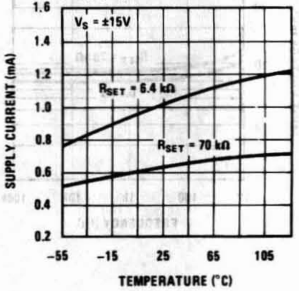
Output Common-Mode Voltage



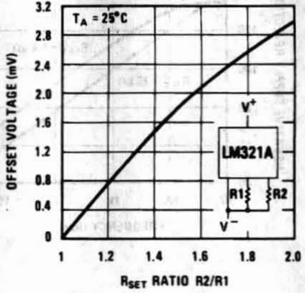
Differential Voltage Gain



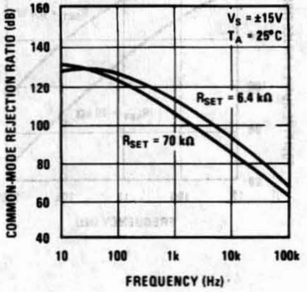
Supply Current



Offset Voltage Adjustment



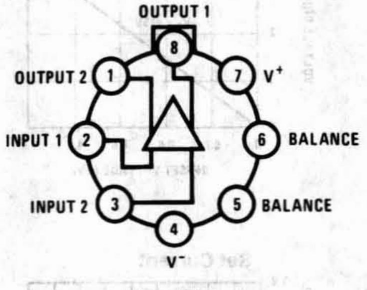
Common-Mode Rejection Ratio



TL/H/7769-10

Connection Diagram

Metal Can Package


OUTPUT 1
8
OUTPUT 2
1
7
V⁺
INPUT 1
2
6
BALANCE
INPUT 2
3
5
BALANCE
4
V⁻

TL/H/7769-7

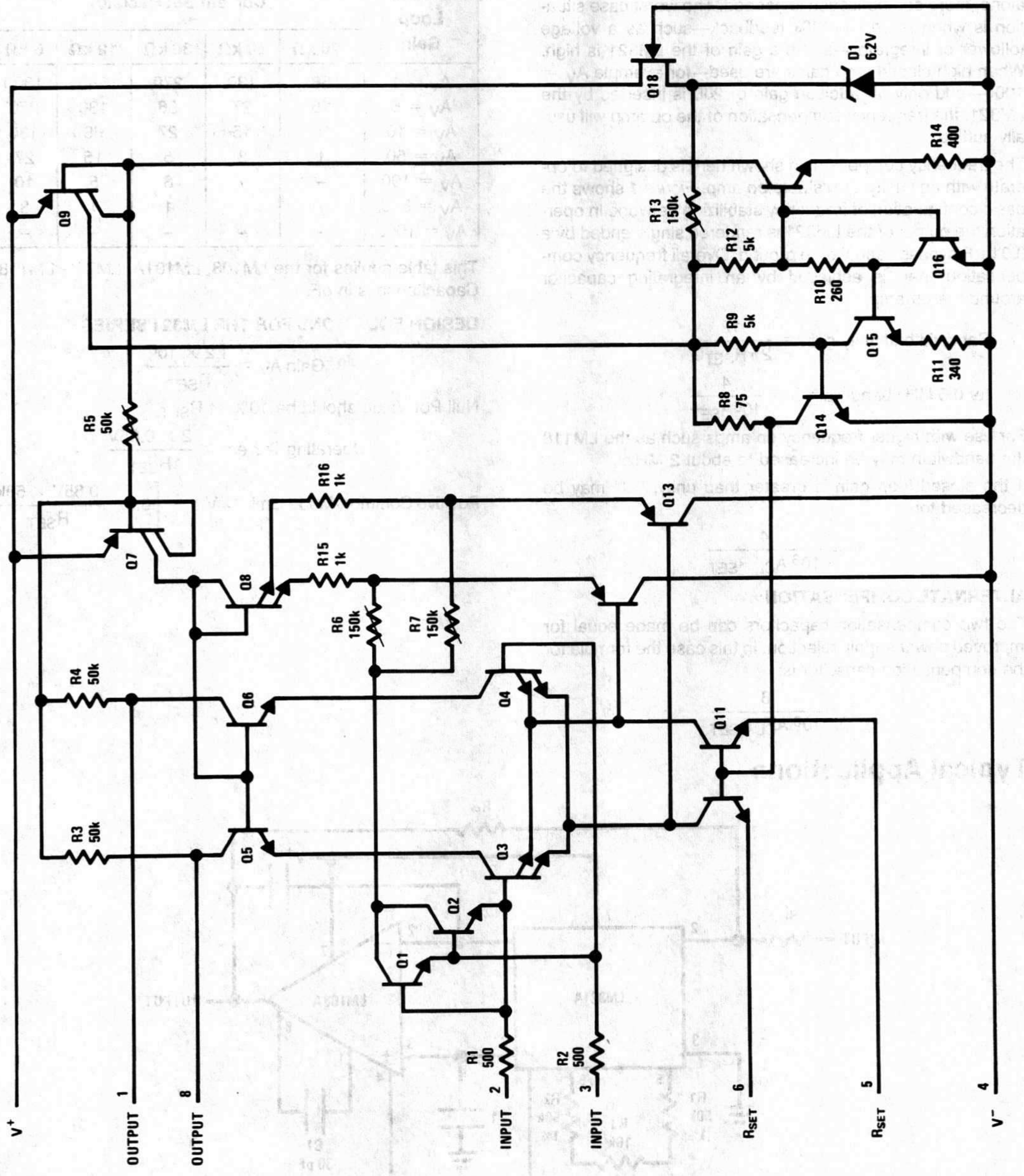
Top View

Note: Pin 4 connected to case.

Order Number LM121AH/883, LM121H/883, LM221H, LM321H or LM321AH
See NS Package Number H08C

Note: Outputs are inverting from the input of the same number.

Schematic Diagram


TL/H/7769-8
Q18
D1 6.2V
R14 400
Q9
R13 150k
R12 5k
Q16
R10 260
R9 5k
Q15
R11 340
R8 75
Q14
R5 50k
R16 1k
Q13
Q7
Q8
R15 1k
R6 150k
R7 150k
R4 50k
Q6
Q4
Q11
R3 50k
Q5
Q3
Q2
Q1
R1 500
R2 500
V+
OUTPUT 1
OUTPUT 8
INPUT 2
INPUT 3
RSET 6
RSET 5
V− 4

Frequency Compensation

UNIVERSAL COMPENSATION

The additional gain of the LM321 preamplifier when used with an operational amplifier usually necessitates additional frequency compensation. When the closed loop gain of the op amp with the LM321 is less than the gain of the LM321 alone, more compensation is needed. The worst case situation is when there is 100% feedback—such as a voltage follower or integrator—and the gain of the LM321 is high. When high closed loop gains are used—for example $A_V = 1000$—and only an addition gain of 200 is inserted by the LM321, the frequency compensation of the op amp will usually suffice.

The frequency compensation shown here is designed to operate with any unity-gain stable op amp. *Figure 1* shows the basic configuration of frequency stabilizing network. In operation the output of the LM321 is rendered single ended by a 0.01 µF bypass capacitor to ground. Overall frequency compensation then is achieved by an integrating capacitor around the op amp.

$$\text{Bandwidth at unity-gain} \cong \frac{12}{2\pi R_{SET} C}$$

$$\text{for 0.5 MHz bandwidth } C = \frac{4}{10^6 R_{SET}}$$

For use with higher frequency op amps such as the LM118 the bandwidth may be increased to about 2 MHz.

If the closed loop gain is greater than unity, "C" may be decreased to:

$$C = \frac{4}{10^6\, A_{CL}\, R_{SET}}$$

ALTERNATE COMPENSATION

The two compensation capacitors can be made equal for improved power supply rejection. In this case the formula for the compensation capscitor is:

$$C = \frac{8}{10^6\, A_{CL}\, R_{SET}}$$

Table I shows typical values for the two compensating capacitors for various gains and operating currents.

TABLE I

Closed Loop Gain	Current Set Resistor				
	120 kΩ	**60 kΩ**	**30 kΩ**	**12 kΩ**	**6 kΩ**
$A_V = 1$	68	130	270	680	1300
$A_V = 5$	15	27	56	130	270
$A_V = 10$	10	15	27	68	130
$A_V = 50$	1	3	5	15	27
$A_V = 100$	–	1	3	5	10
$A_V = 500$	–	–	1	1	3
$A_V = 1000$	–	–	–	–	–

This table applies for the LM108, LM101A, LM741, LM118. Capacitance is in pF.

DESIGN EQUATIONS FOR THE LM321 SERIES

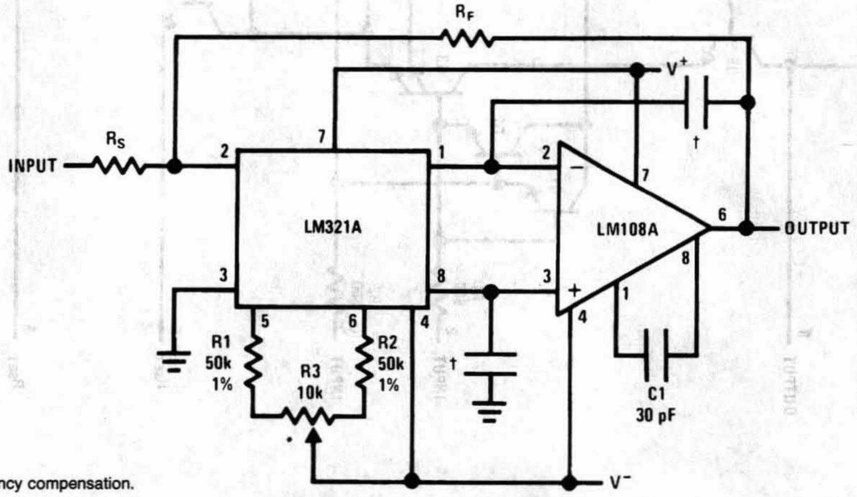
$$\text{Gain } A_V \approx \frac{1.2 \times 10^6}{R_{SET}}$$

Null Pot Value should be 10% of R_{SET}

$$\text{Operating Current} \approx \frac{2 \times 0.65\text{V}}{R_{SET}}$$

$$\text{Positive Common-Mode Limit} \approx V^+ - \left[0.6 - \frac{0.65\text{V} \times 50\text{k}}{R_{SET}}\right]$$

Typical Applications



*Offset adjust.

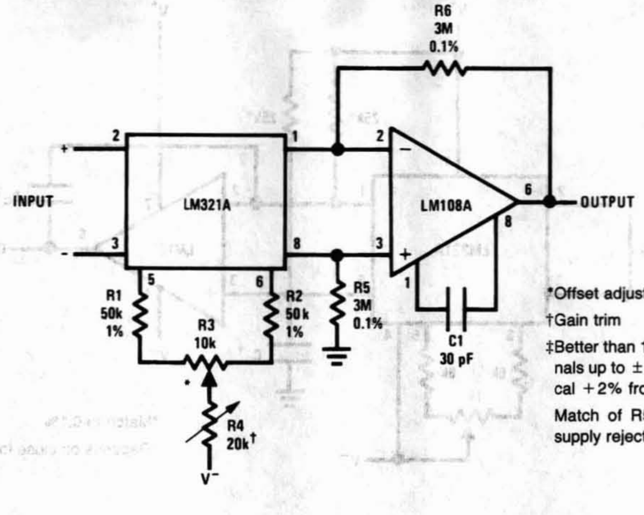
†See table for frequency compensation.

TL/H/7769-2

FIGURE 1. Low Drift Op Amp Using the LM321A as a Preamp

Typical Applications (Continued)

Gain of 1000 Instrumentation Amplifier‡


R6
3M
0.1%
2
1
2
+
INPUT
−
3
LM321A
8
3
5
6
LM108A
6
8
OUTPUT
R1
50k
1%
R2
50k
1%
R5
3M
0.1%
1
R3
10k
*
C1
30 pF
R4
20k†
V−

*Offset adjust

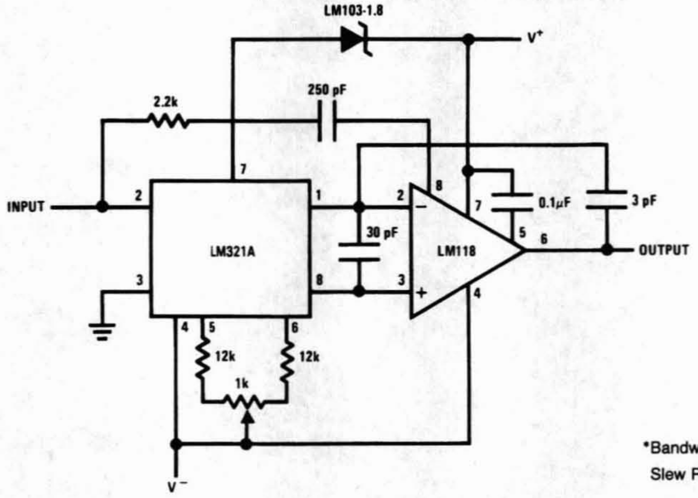
†Gain trim

‡Better than 1% linearity for input signals up to ±10 mV gain stability typical +2% from −55 to +125°C.

Match of R5 and R6 effect power supply rejection

TL/H/7769–3

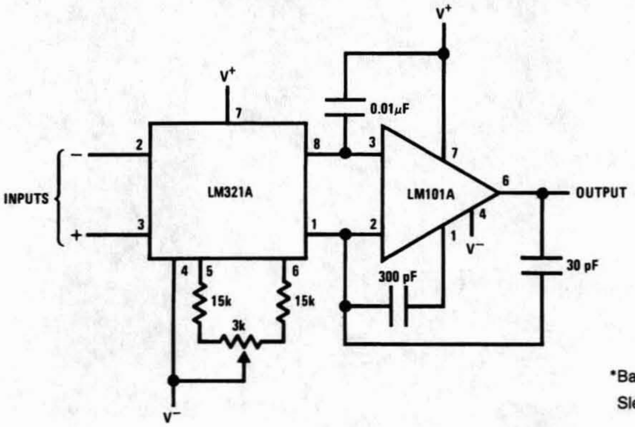
High Speed* Inverting Amplifier with Low Drift


LM103-1.8
V+
2.2k
250 pF
7
8
INPUT
2
1
2
7
0.1μF
3 pF
LM321A
30 pF
5
6
LM118
OUTPUT
3
8
3
4
4
5
6
12k
12k
1k
V−

*Bandwidth = 10 MHz
Slew Rate = 40 V/μs

TL/H/7769–4

Medium Speed* General Purpose Amplifier

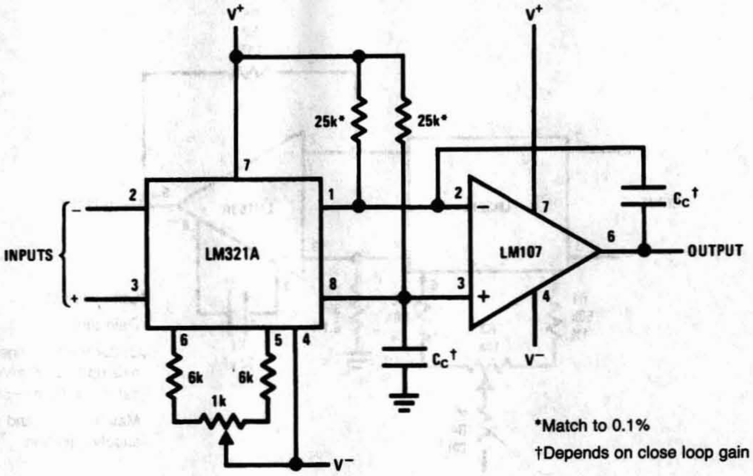

V+
V+
0.01μF
7
2
8
3
7
−
INPUTS
LM321A
LM101A
6
OUTPUT
+
3
1
2
4
1
V−
4
5
6
30 pF
300 pF
15k
15k
3k
V−

*Bandwidth = 3.5 MHz
Slew Rate = 1.1 V/μs

TL/H/7769–5

Typical Applications (Continued)

Increased Common-Mode Range at High Operating Currents


V+
V+
25k*
25k*
7
2
1
2
7
Cc†
INPUTS
−
+
3
LM321A
8
3
LM107
6
OUTPUT
4
6
5
4
Cc†
V−
6k
6k
1k
V−

*Match to 0.1%

†Depends on close loop gain

TL/H/7769-6

National Semiconductor

LM359 Dual, High Speed, Programmable, Current Mode (Norton) Amplifiers

General Description

The LM359 consists of two current differencing (Norton) input amplifiers. Design emphasis has been placed on obtaining high frequency performance and providing user programmable amplifier operating characteristics. Each amplifier is broadbanded to provide a high gain bandwidth product, fast slew rate and stable operation for an inverting closed loop gain of 10 or greater. Pins for additional external frequency compensation are provided. The amplifiers are designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

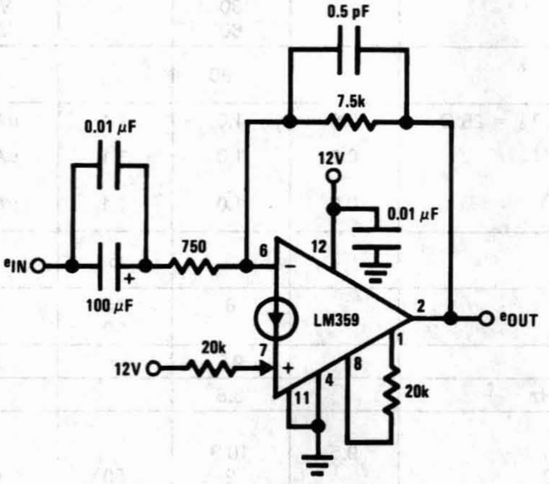
Applications

- General purpose video amplifiers
- High frequency, high Q active filters
- Photo-diode amplifiers
- Wide frequency range waveform generation circuits
- All LM3900 AC applications work to much higher frequencies

Features

- User programmable gain bandwidth product, slew rate, input bias current, output stage biasing current and total device power dissipation
- High gain bandwidth product (I_{SET} = 0.5 mA)
  400 MHz for A_V = 10 to 100
  30 MHz for A_V = 1
- High slew rate (I_{SET} = 0.5 mA)
  60 V/μs for A_V = 10 to 100
  30 V/μs for A_V = 1
- Current differencing inputs allow high common-mode input voltages
- Operates from a single 5V to 22V supply
- Large inverting amplifier output swing, 2 mV to V_{CC} − 2V
- Low spot noise, 6 nV/$\sqrt{Hz}$, for f > 1 kHz

Typical Application

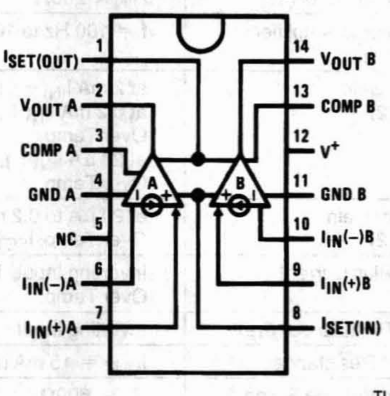


TL/H/7788–1

- A_V = 20 dB
- −3 dB bandwidth = 2.5 Hz to 25 MHz
- Differential phase error < 1° at 3.58 MHz
- Differential gain error < 0.5% at 3.58 MHz

Connection Diagram

Dual-In-Line Package



TL/H/7788–2

Top View

Order Number LM359J, LM359M or LM359N
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	22 V_{DC} or ±11 V_{DC}
Power Dissipation (Note 1)	
J Package	1W
N Package	750 mW
Maximum T_J	
J Package	+150°C
N Package	+125°C

Thermal Resistance

J Package

θ_{jA} 147°C/W still air
110°C/W with 400 linear feet/min air flow

N Package

θ_{jA} 100°C/W still air
75°C/W with 400 linear feet/min air flow

Input Currents, $I_{IN}(+)$ or $I_{IN}(-)$	10 mA_{DC}
Set Currents, $I_{SET(IN)}$ or $I_{SET(OUT)}$	2 mA_{DC}
Operating Temperature Range	
LM359	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics $I_{SET(IN)} = I_{SET(OUT)} = 0.5$ mA, $V_{supply} = 12V$, $T_A = 25°C$ unless otherwise noted

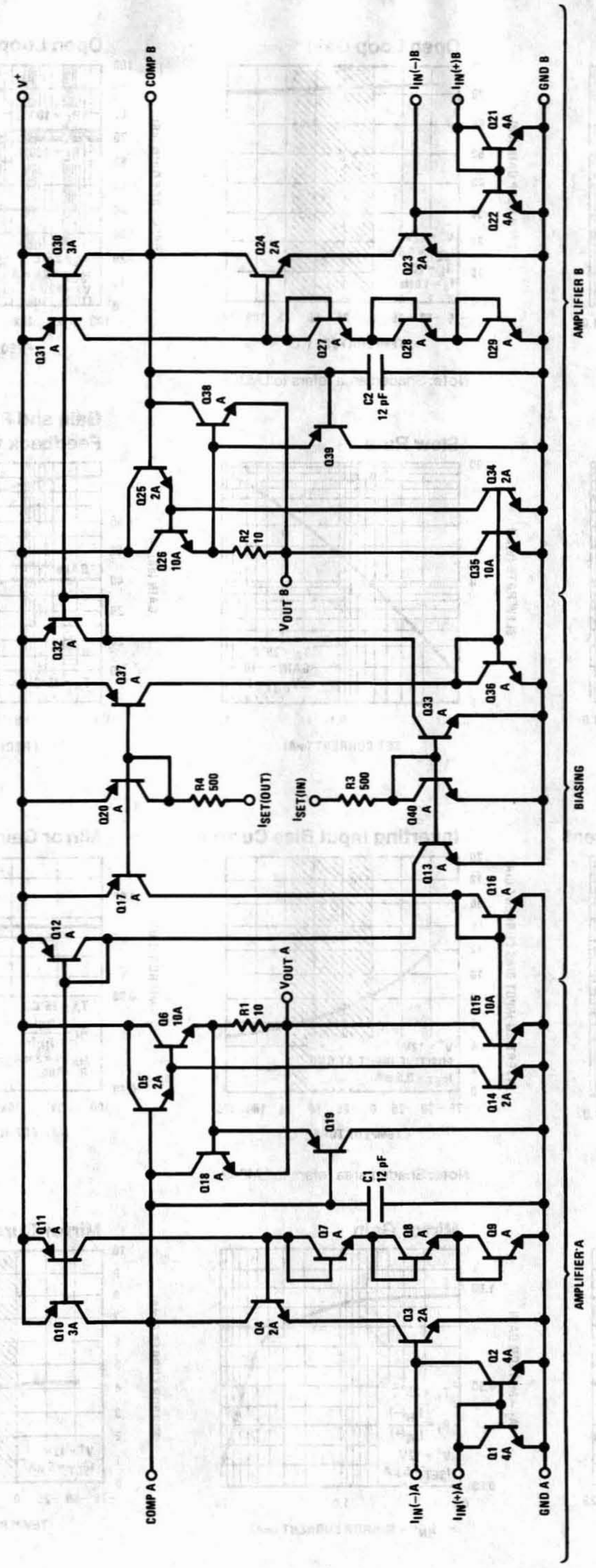
Parameter	Conditions	LM359			Units
		Min	Typ	Max	
Open Loop Voltage Gain	$V_{supply} = 12V$, $R_L = 1k$, f = 100 Hz $T_A = 125°C$	62	72 68		dB dB
Bandwidth Unity Gain	$R_{IN} = 1\ k\Omega$, $C_{comp} = 10$ pF	15	30		MHz
Gain Bandwidth Product Gain of 10 to 100	$R_{IN} = 50\Omega$ to 200Ω	200	400		MHz
Slew Rate Unity Gain Gain of 10 to 100	$R_{IN} = 1\ k\Omega$, $C_{comp} = 10$ pF $R_{IN} < 200\Omega$		30 60		V/μs V/μs
Amplifier to Amplifier Coupling	f = 100 Hz to 100 kHz, $R_L = 1k$		−80		dB
Mirror Gain (Note 2)	at 2 mA $I_{IN}(+)$, $I_{SET} = 5\ \mu A$, $T_A = 25°C$ at 0.2 mA $I_{IN}(+)$, $I_{SET} = 5\ \mu A$ Over Temp. at 20 μA $I_{IN}(+)$, $I_{SET} = 5\ \mu A$ Over Temp.	0.9 0.9 0.9	1.0 1.0 1.0	1.1 1.1 1.1	μA/μA μA/μA μA/μA
ΔMirror Gain (Note 2)	at 20 μA to 0.2 mA $I_{IN}(+)$ Over Temp, $I_{SET} = 5\ \mu A$		3	5	%
Input Bias Current	Inverting Input, $T_A = 25°C$ Over Temp.		8	15 30	μA μA
Input Resistance (βre)	Inverting Input		2.5		kΩ
Output Resistance	$I_{OUT} = 15$ mA rms, f = 1 MHz		3.5		Ω
Output Voltage Swing V_{OUT} High V_{OUT} Low	$R_L = 600\Omega$ $I_{IN}(-)$ and $I_{IN}(+)$ Grounded $I_{IN}(-) = 100\ \mu A$, $I_{IN}(+) = 0$	9.5	10.3 2	50	V mV
Output Currents Source Sink (Linear Region) Sink (Overdriven)	$I_{IN}(-)$ and $I_{IN}(+)$ Grounded, $R_L = 100\Omega$ $V_{comp} - 0.5V = V_{OUT} = 1V$, $I_{IN}(+) = 0$ $I_{IN}(-) = 100\ \mu A$, $I_{IN}(+) = 0$, V_{OUT} Force = 1V	16 1.5	40 4.7 3		mA mA mA
Supply Current	Non-Inverting Input Grounded, $R_L = \infty$		18.5	22	mA
Power Supply Rejection (Note 3)	f = 120 Hz, $I_{IN}(+)$ Grounded	40	50		dB

Note 1: See Maximum Power Dissipation graph.

Note 2: Mirror gain is the current gain of the current mirror which is used as the non-inverting input. $\left(A_I = \frac{I_{IN}(-)}{I_{IN}(+)}\right)$ ΔMirror Gain is the % change in A_I for two different mirror currents at any given temperature.

Note 3: See Supply Rejection graphs.

Schematic Diagram


V+
COMP B
IIN(−)B
IIN(+)B
GND B
Q30 3A
Q31 A
Q24 2A
Q23 2A
Q22 4A
Q21 4A
Q27 A
Q28 A
Q29 A
C2 12 pF
Q38 A
Q39
Q25 2A
Q26 10A
R2 10
VOUT B
Q34 2A
Q35 10A
Q32 A
Q37 A
Q33 A
Q36 A
Q20 A
R4 500
ISET(OUT)
ISET(IN)
R3 500
Q40 A
Q13 A
Q17 A
Q16 A
Q12 A
VOUT A
R1 10
Q6 10A
Q5 2A
Q15 10A
Q14 2A
Q19
Q18 A
C1 12 pF
Q11 A
Q7 A
Q8 A
Q9 A
Q10 3A
Q4 2A
Q3 2A
Q2 4A
Q1 4A
COMP A
IIN(−)A
IIN(+)A
GND A
AMPLIFIER B
BIASING
AMPLIFIER A

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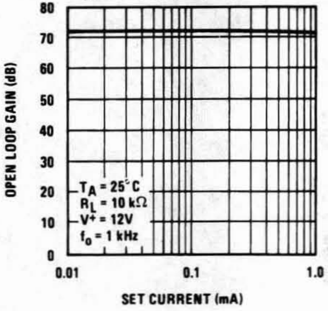
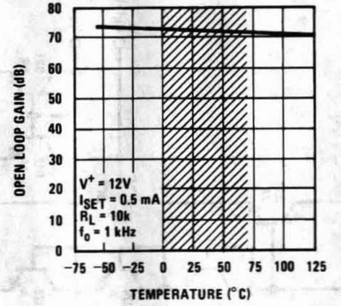
Typical Performance Characteristics

Open Loop Gain

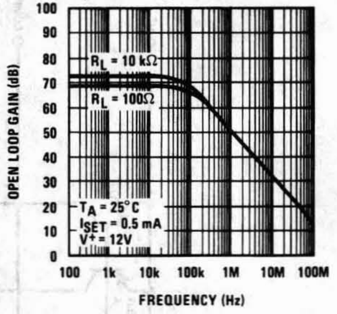


Open Loop Gain

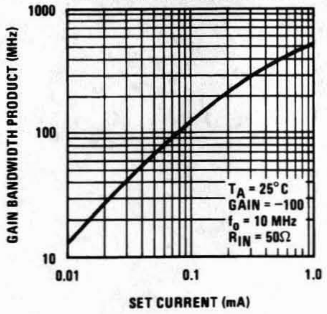


Note: Shaded area refers to LM359

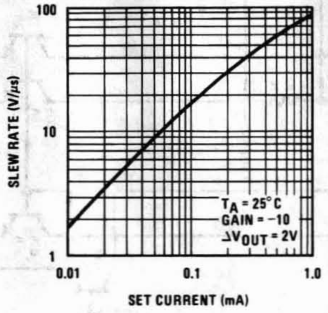
Open Loop Gain



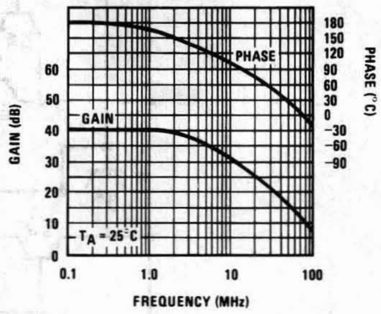
Gain Bandwidth Product



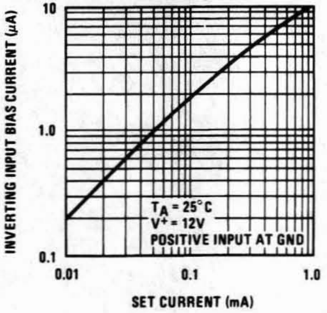
Slew Rate



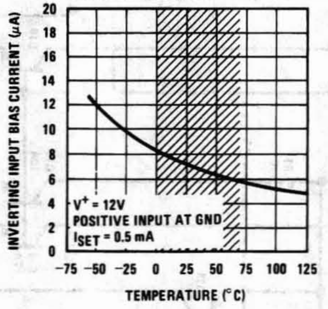
Gain and Phase
Feedback Gain = −100



Inverting Input Bias Current

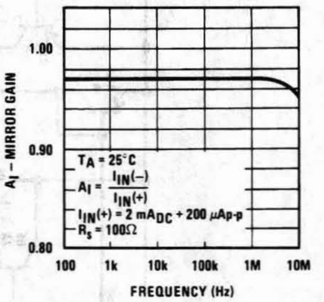


Inverting Input Bias Current

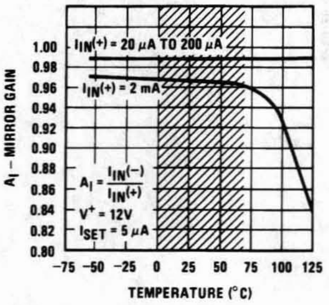


Note: Shaded area refers to LM359

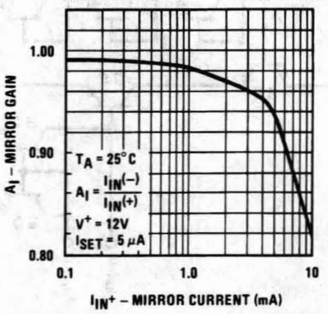
Mirror Gain



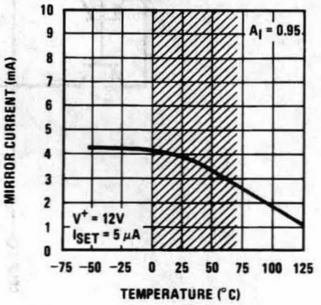
Mirror Gain



Mirror Gain



Mirror Current



Note: Shaded area refers to LM359

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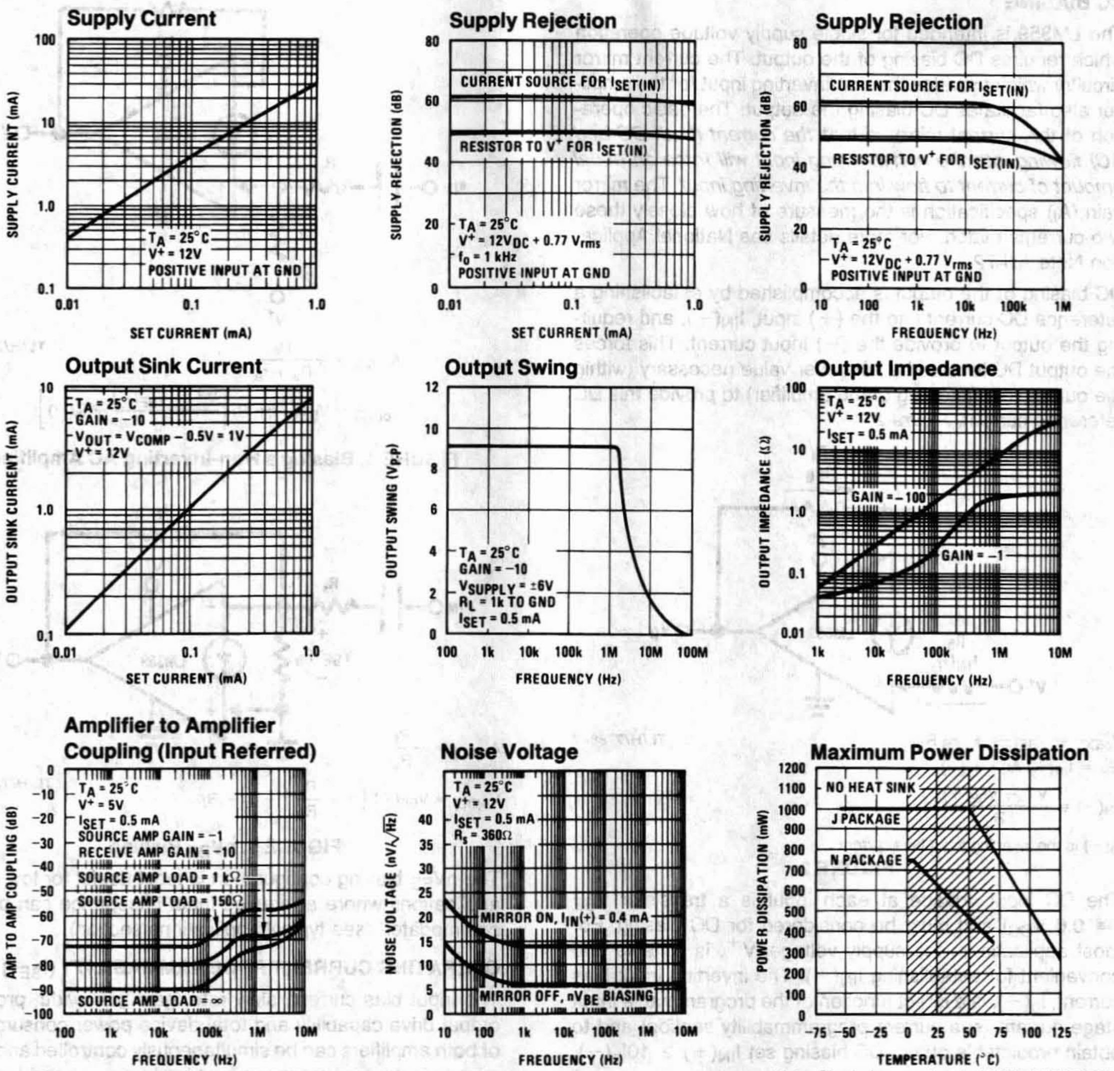
Note: Shaded area refers to LM359

Typical Performance Characteristics (Continued)



Note: Shaded area refers to LM359J/LM359N

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Application Hints

The LM359 consists of two wide bandwidth, decompensated current differencing (Norton) amplifiers. Although similar in operation to the original LM3900, design emphasis for these amplifiers has been placed on obtaining much higher frequency performance as illustrated in *Figure 1*.

This significant improvement in frequency response is the result of using a common-emitter/common-base (cascode) gain stage which is typical in many discrete and integrated video and RF circuit designs. Another versatile aspect of these amplifiers is the ability to externally program many internal amplifier parameters to suit the requirements of a wide variety of applications in which this type of amplifier can be used.

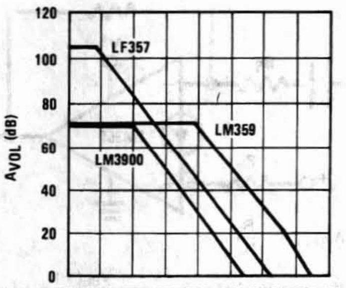

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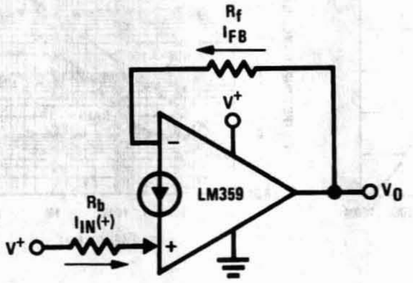
FIGURE 1

Application Hints (Continued)

DC BIASING

The LM359 is intended for single supply voltage operation which requires DC biasing of the output. The current mirror circuitry which provides the non-inverting input for the amplifier also facilitates DC biasing the output. The basic operation of this current mirror is that *the current (both DC and AC) flowing into the non-inverting input will force an equal amount of current to flow into the inverting input.* The mirror gain (A_I) specification is the measure of how closely these two currents match. For more details see National Application Note AN-72.

DC biasing of the output is accomplished by establishing a reference DC current into the (+) input, $I_{IN}(+)$, and requiring the output to provide the (−) input current. This forces the output DC level to be whatever value necessary (within the output voltage swing of the amplifier) to provide this DC reference current, *Figure 2.*



$V_{o(DC)} = V_{BE}(-) + I_{FB}\,R_f$

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$I_{FB} = I_{IN}(+)\,A_I + I_b(-)$

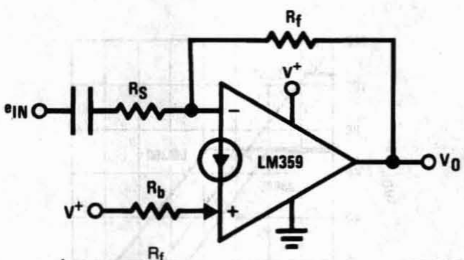
$I_{IN}(+) = \frac{V^+ - V_{BE}(+)}{R_b}$

$I_b(-)$ is the inverting input bias current

FIGURE 2

The DC input voltage at each input is a transistor V_{BE} ($\cong$ 0.6 V_{DC}) and must be considered for DC biasing. For most applications, the supply voltage, V^+, is suitable and convenient for establishing $I_{IN}(+)$. The inverting input bias current, $I_b(-)$, is a direct function of the programmable input stage current (see current programmability section) and to obtain predictable output DC biasing set $I_{IN}(+) \geq 10 I_b(-)$.

The following figures illustrate typical biasing schemes for AC amplifiers using the LM359:



$A_{V(AC)} = -\frac{R_f}{R_s}$

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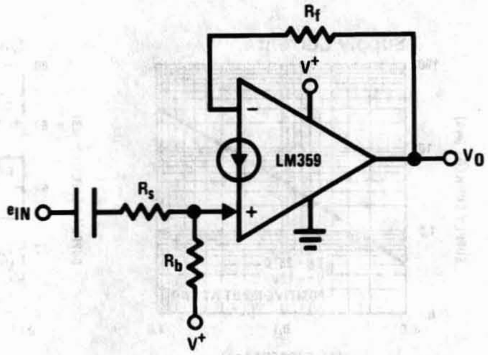
$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$

FIGURE 3. Biasing an Inverting AC Amplifier



$A_{V(AC)} = +\frac{R_f}{R_s + r_e}$

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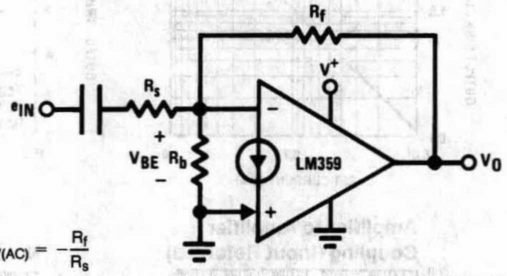
$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$

FIGURE 4. Biasing a Non-Inverting AC Amplifier



$A_{V(AC)} = -\frac{R_f}{R_s}$

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$V_{o(DC)} = V_{BE}(-)\left(1 + \frac{R_f}{R_B}\right) + I_b(-)R_f$

FIGURE 5. nV$_{BE}$ Biasing

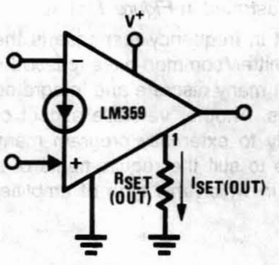
The nV$_{BE}$ biasing configuration is most useful for low noise applications where a reduced input impedance can be accommodated (see typical applications section).

OPERATING CURRENT PROGRAMMABILITY (I_{SET})

The input bias current, slew rate, gain bandwidth product, output drive capability and total device power consumption of both amplifiers can be simultaneously controlled and optimized via the two programming pins $I_{SET(OUT)}$ and $I_{SET(IN)}$.

$I_{SET(OUT)}$

The output set current ($I_{SET(OUT)}$) is equal to the amount of current sourced from pin 1 and establishes the class A biasing current for the Darlington emitter follower output stage. Using a single resistor from pin 1 to ground, as shown in *Figure 6*, this current is equal to:



$I_{SET(OUT)} = \frac{V^+ - V_{BE}}{R_{SET(OUT)} + 500\Omega}$

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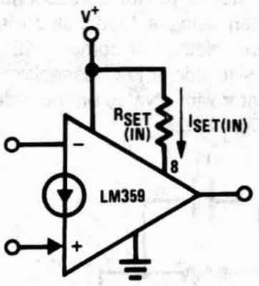
FIGURE 6. Establishing the Output Set Current

Application Hints (Continued)

The output set current can be adjusted to optimize the amount of current the output of the amplifier can sink to drive load capacitance and for loads connected to V^+. *The maximum output sinking current is approximately 10 times* $I_{SET(OUT)}$. This set current is best used to reduce the total device supply current if the amplifiers are not required to drive small load impedances.

$I_{SET(IN)}$

The input set current $I_{SET(IN)}$ is equal to the current flowing into pin 8. A resistor from pin 8 to V^+ sets this current to be:



$$I_{SET(IN)} = \frac{V^+ - V_{BE}}{R_{SET(IN)} + 500\Omega}$$

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FIGURE 7. Establishing the Input Set Current

$I_{SET(IN)}$ is most significant in controlling the AC characteristics of the LM359 as it directly sets the total input stage current of the amplifiers which determines the maximum slew rate, the frequency of the open loop dominant pole, the input resistance of the (−) input and the biasing current $I_b(-)$. All of these parameters are significant in wide band amplifier design. The input stage current is approximately 3 times $I_{SET(IN)}$ and by using this relationship the following first order approximations for these AC parameters are:

$$S_{r(MAX)} = \text{max slew rate} \cong \frac{3\, I_{SET(IN)}\,(10^{-6})}{C_{comp}}\ (\text{V}/\mu\text{s})$$

$$\text{frequency of dominant pole} \cong \frac{3\, I_{SET(IN)}}{2\pi\, C_{comp}\, A_{VOL}\,(0.026\text{V})}\ (\text{Hz})$$

$$\text{input resistance} = \beta r_e \cong \frac{150\,(0.026\text{V})}{3 I_{SET(IN)}}\ (\Omega)$$

where C_{comp} is the total capacitance from the compensation pin (pin 3 or pin 13) to ground, A_{VOL} is the low frequency open loop voltage gain in V/V and an ambient temperature of 25°C is assumed ($KT/q = 26$ mV and $\beta_{typ} = 150$). $I_{SET(IN)}$ also controls the DC input bias current by the expression:

$$I_b(-) = \frac{3 I_{SET}}{\beta} \cong \frac{I_{SET}}{50} \text{ for NPN } \beta = 150$$

which is important for DC biasing considerations.

The total device supply current (for both amplifiers) is also a direct function of the set currents and can be approximated by:

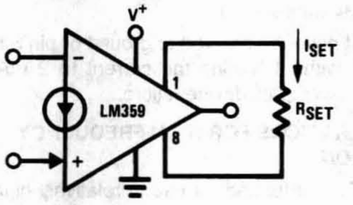
$$I_{supply} \cong 27 \times I_{SET(OUT)} + 11 \times I_{SET(IN)}$$

with each set current programmed by individual resistors.

PROGRAMMING WITH A SINGLE RESISTOR

Operating current programming may also be accomplished using only one resistor by letting $I_{SET(IN)}$ equal $I_{SET(OUT)}$. The programming current is now referred to as I_{SET} and it is created by connecting a resistor from pin 1 to pin 8 *(Figure 8)*.

$$I_{SET} = \frac{V^+ - 2\,V_{BE}}{R_{SET} + 1\text{ k}\Omega} \text{ where } V_{BE} \cong 0.6\text{V}$$



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$I_{SET(IN)} = I_{SET(OUT)} = I_{SET}$

FIGURE 8. Single Resistor Programming of I_{SET}

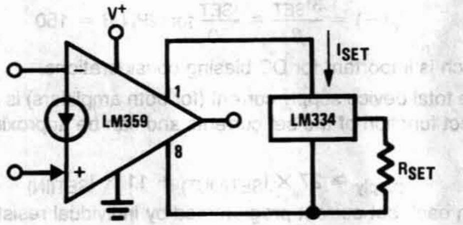
This configuration does not affect any of the internal set current dependent parameters differently than previously discussed except the total supply current which is now equal to:

$$I_{supply} \cong 37 \times I_{SET}$$

Care must be taken when using resistors to program the set current to prevent significantly increasing the supply voltage above the value used to determine the set current. This would cause an increase in total supply current due to the resulting increase in set current and the maximum device power dissipation could be exceeded. The set resistor value(s) should be adjusted for the new supply voltage.

Application Hints (Continued)

One method to avoid this is to use an adjustable current source which has voltage compliance to generate the set current as shown in *Figure 9.*



$$I_{SET} = \frac{67.7\ mV}{R_{SET}}\ @25°C$$

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FIGURE 9. Current Source Programming of I_{SET}

This circuit allows I_{SET} to remain constant over the entire supply voltage range of the LM359 which also improves power supply ripple rejection as illustrated in the Typical Performance Characteristics. It should be noted, however, that the current through the LM334 as shown will change linearly with temperature but this can be compensated for (see LM334 data sheet).

Pin 1 must never be shorted to ground or pin 8 never shorted to V^+ without limiting the current to 2 mA or less to prevent catastrophic device failure.

CONSIDERATIONS FOR HIGH FREQUENCY OPERATION

The LM359 is intended for use in relatively high frequency applications and many factors external to the amplifier itself must be considered. Minimization of stray capacitances and their effect on circuit operation are the primary requirements. The following list contains some general guidelines to help accomplish this end:

1. Keep the leads of all external components as short as possible.
2. Place components conducting signal current from the output of an amplifier away from that amplifier's non-inverting input.
3. Use reasonably low value resistances for gain setting and biasing.
4. Use of a ground plane is helpful in providing a shielding effect between the inputs and from input to output. Avoid using vector boards.
5. Use a single-point ground and single-point supply distribution to minimize crosstalk. Always connect the two grounds (one from each amplifier) together.
6. Avoid use of long wires (> 2 ") but if necessary, use shielded wire.
7. Bypass the supply close to the device with a low inductance, low value capacitor (typically a 0.01 μF ceramic) to create a good high frequency ground. If long supply leads are unavoidable, a small resistor (~10Ω) in series with the bypass capacitor may be needed and using shielded wire for the supply leads is also recommended.

COMPENSATION

The LM359 is internally compensated for stability with closed loop inverting gains of 10 or more. For an inverting gain of less than 10 and all non-inverting amplifiers (the amplifier always has 100% negative current feedback regardless of the gain in the non-inverting configuration) some external frequency compensation is required because the stray capacitance to ground from the (−) input and the feedback resistor add additional lagging phase within the feedback loop. The value of the input capacitance will typically be in the range of 6 pF to 10 pF for a reasonably constructed circuit board. When using a feedback resistance of 30 kΩ or less, the best method of compensation, without sacrificing slew rate, is to add a lead capacitor in parallel with the feedback resistor with a value on the order of 1 pF to 5 pF as shown in *Figure 10.*

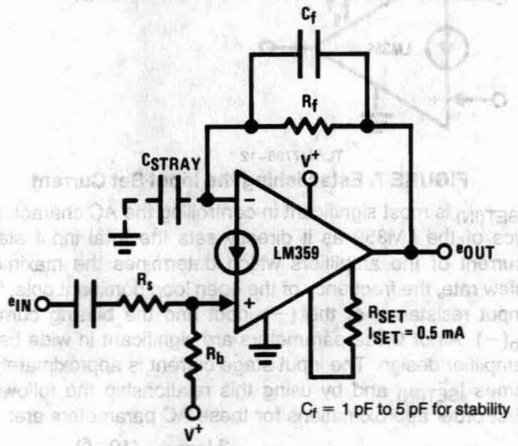

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FIGURE 10. Best Method of Compensation

Another method of compensation is to increase the effective value of the internal compensation capacitor by adding capacitance from the COMP pin of an amplifier to ground. An external 20 pF capacitor will generally compensate for all gain settings but will also reduce the gain bandwidth product and the slew rate. These same results can also be obtained by reducing $I_{SET(IN)}$ if the full capabilities of the amplifier are not required. This method is termed over-compensation.

Another area of concern from a stability standpoint is that of capacitive loading. The amplifier will generally drive capacitive loads up to 100 pF without oscillation problems. Any larger C loads can be isolated from the output as shown in *Figure 11.* Over-compensation of the amplifier can also be used if the corresponding reduction of the GBW product can be afforded.

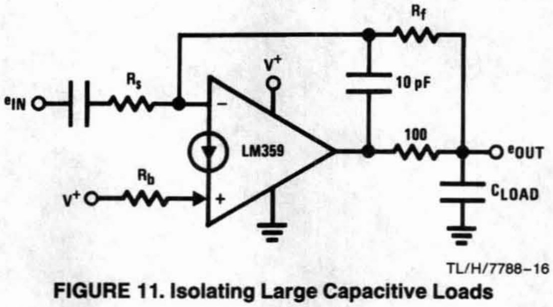

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FIGURE 11. Isolating Large Capacitive Loads

Application Hints (Continued)

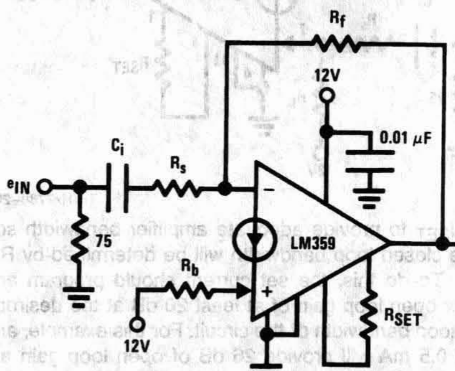
In most applications using the LM359, the input signal will be AC coupled so as not to affect the DC biasing of the amplifier. This gives rise to another subtlety of high frequency circuits which is the effective series inductance (ESL) of the coupling capacitor which creates an increase in the impedance of the capacitor at high frequencies and can cause an unexpected gain reduction. Low ESL capacitors like solid tantalum for large values of C and ceramic for smaller values are recommended. A parallel combination of the two types is even better for gain accuracy over a wide frequency range.

AMPLIFIER DESIGN EXAMPLES

The ability of the LM359 to provide gain at frequencies higher than most monolithic amplifiers can provide makes it most useful as a basic broadband amplification stage. The design of standard inverting and non-inverting amplifiers, though different than standard op amp design due to the current differencing inputs, also entail subtle design differences between the two types of amplifiers. These differences will be best illustrated by design examples. For these examples a practical video amplifier with a passband of 8 Hz to 10 MHz and a gain of 20 dB will be used. It will be assumed that the input will come from a 75Ω source and proper signal termination will be considered. The supply voltage is 12 V_{DC} and single resistor programming of the operating current, I_{SET}, will be used for simplicity.

AN INVERTING VIDEO AMPLIFIER

1. Basic circuit configuration:



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2. Determine the required I_{SET} from the characteristic curves for gain bandwidth product.

$$GBW_{MIN} = 10 \times 10\text{ MHz} = 100\text{ MHz}$$

For a flat response to 10 MHz a closed loop response to two octaves above 10 MHz (40 MHz) will be sufficient.

Actual GBW = 10 × 40 MHz = 400 MHz

I_{SET} required = 0.5 mA

$$R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\text{ k}\Omega = \frac{10.8\text{V}}{0.5\text{ mA}} - 1\text{ k}\Omega = 20.6\text{ k}\Omega$$

3. Determine maximum value for R_f to provide stable DC biasing

$$I_{f(MIN)} \geq 10 \times \frac{3\,I_{SET}}{\beta} = 100\,\mu\text{A minimum DC feedback current}$$

Optimum output DC level for maximum symmetrical swing without clipping is:

$$V_{ODC(opt)} = \frac{V_{O(MAX)} - V_{O(MIN)}}{2} + V_{O(MIN)}$$

$$\approx \frac{(V^+ - 3\,V_{BE}) - 2\text{ mV}}{2}$$

$$V_{ODC(opt)} \cong \frac{12 - 1.8\text{V}}{2} = \frac{10.2\text{V}}{2} = 5.1\,V_{DC}$$

$R_{f(MAX)}$ can now be found:

$$R_{f(MAX)} = \frac{V_{ODC(opt)} - V_{BE}(-)}{I_{f(MIN)}} = \frac{5.1\text{V} - 0.6\text{V}}{100\,\mu\text{A}} = 45\text{ k}\Omega$$

This value should not be exceeded for predictable DC biasing.

4. Select R_s to be large enough so as not to appreciably load the input termination resistance:

$$R_s \geq 750\Omega \text{ Let } R_s = 750\Omega$$

5. Select R_f for appropriate gain:

$$A_V = -\frac{R_f}{R_s} \text{ so; } R_f = 10\,R_s = 7.5\text{ k}\Omega$$

7.5 kΩ is less than the calculated $R_{f(MAX)}$ so DC predictability is insured.

6. Since R_f = 7.5k, for the output to be biased to 5.1 V_{DC}, the reference current $I_{IN}(+)$ must be:

$$I_{IN}(+) = \frac{5.1\text{V} - V_{BE}(-)}{R_f} = \frac{5.1\text{V} - 0.6\text{V}}{7.5\text{ k}\Omega} = 600\,\mu\text{A}$$

Now R_b can be found by:

$$R_b = \frac{V^+ - V_{BE}(+)}{I_{IN}(+)} = \frac{12 - 0.6}{600\,\mu\text{A}} = 19\text{ k}\Omega$$

7. Select C_i to provide the proper gain for the 8 Hz minimum input frequency:

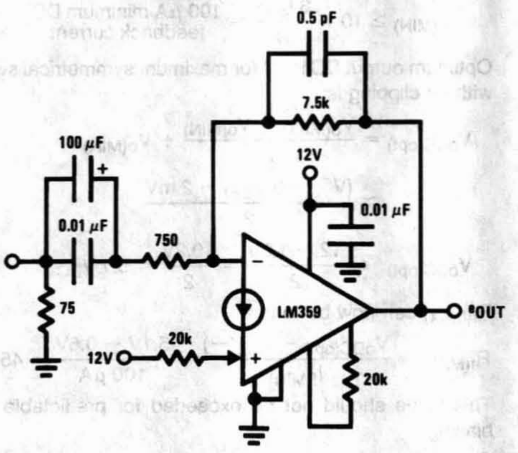
$$C_i \geq \frac{1}{2\pi\,R_s\,(f_{low})} = \frac{1}{2\pi\,(750\Omega)\,(8\text{ Hz})} = 26\,\mu\text{F}$$

A larger value of C_i will allow a flat frequency response down to 8 Hz and a 0.01 μF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

8. Test for peaking of the frequency response and add a feedback "lead" capacitor to compensate if necessary.

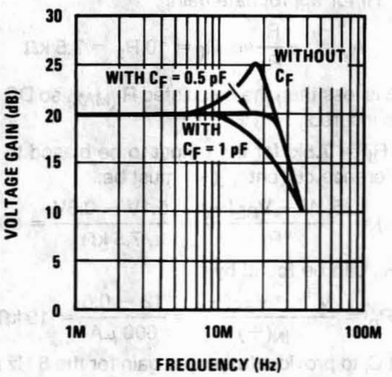
Application Hints (Continued)

Final Circuit Using Standard 5% Tolerance Resistor Values:



TL/H/7788-18

Circuit Performance:



TL/H/7788-19

$V_{o(DC)} = 5.1V$

Differential phase error < 1° for 3.58 MHz f_{IN}

Differential gain error < 0.5% for 3.58 MHz f_{IN}

$f_{-3\,dB}$ low = 2.5 Hz

A NON-INVERTING VIDEO AMPLIFIER

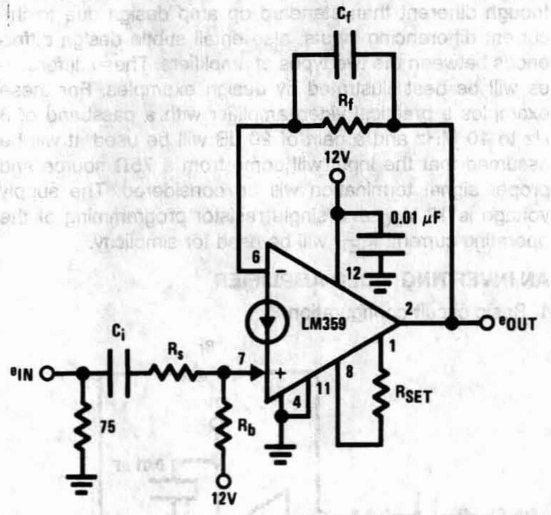
For this case several design considerations must be dealt with.

- The output voltage (AC and DC) is strictly a function of the size of the feedback resistor and the sum of AC and DC "mirror current" flowing into the (+) input.
- The amplifier always has 100% current feedback so external compensation is required. Add a small (1 pF–5 pF) feedback capacitance to leave the amplifier's open loop response and slew rate unaffected.
- To prevent saturating the mirror stage the total AC and DC current flowing into the amplifier's (+) input should be less than 2 mA.
- The output's maximum negative swing is one diode above ground due to the V_{BE} diode clamp at the (−) input.

DESIGN EXAMPLE:

e_{IN} = 50 mV (MAX), f_{IN} = 10 MHz (MAX), desired circuit BW = 20 MHz, A_V = 20 dB, driving source impedance = 75Ω, V^+ = 12V.

1. Basic circuit configuration:



TL/H/7788-20

2. Select I_{SET} to provide adequate amplifier bandwidth so that the closed loop bandwidth will be determined by R_f and C_f. To do this, the set current should program an amplifier open loop gain of at least 20 dB at the desired closed loop bandwidth of the circuit. For this example, an I_{SET} of 0.5 mA will provide 26 dB of open loop gain at 20 MHz which will be sufficient. Using single resistor programming for I_{SET}:

$$R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\,k\Omega = 20.6\,k\Omega$$

3. Since the closed loop bandwidth will be determined by R_f and C_f $\left(f_{-3\,dB} = \frac{1}{2\pi\,R_f\,C_f}\right)$

Application Hints (Continued)

to obtain a 20 MHz bandwidth, both R_f and C_f should be kept small. It can be assumed that C_f can be in the range of 1 pF to 5 pF for carefully constructed circuit boards to insure stability and allow a flat frequency response. This will limit the value of R_f to be within the range of:

$$\frac{1}{2\pi\ 5\ \text{pF}\ 20\ \text{MHz}} \leq R_f \leq \frac{1}{2\pi\ 1\ \text{pF}\ 20\ \text{MHz}}$$

$$\text{or } 1.6\ \text{k}\Omega \leq R_f \leq 7.96\ \text{k}\Omega$$

Also, for a closed loop gain of +10, R_f must be 10 times $R_s + r_e$ where r_e is the mirror diode resistance.

4. So as not to appreciably load the 75Ω input termination resistance the value of $(R_s + r_e)$ is set to 750Ω.
5. For $A_v = 10$; R_f is set to 7.5 kΩ.
6. The optimum output DC level for symmetrical AC swing is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$= \frac{(12 - 1.8)\text{V} - 0.6\text{V}}{2} + 0.6\text{V} = 5.4\ V_{DC}$$

7. The DC feedback current must be:

$$I_{FB} = \frac{V_{oDC(opt)} - V_{BE}(-)}{R_f} = \frac{5.4\text{V} - 0.6\text{V}}{7.5\text{k}}$$

$$= 640\ \mu\text{A} = I_{IN}(+)$$

DC biasing predictability will be insured because 640 µA is greater than the minimum of $I_{SET}/5$ or 100 µA.

For gain accuracy the total AC and DC mirror current should be less than 2 mA. For this example the maximum AC mirror current will be;

$$\frac{\pm e_{\text{in peak}}}{R_s + r_e} = \frac{\pm 50\ \text{mV}}{750\Omega} = \pm 66\ \mu\text{A}$$

therefore the total mirror current range will be 574 µA to 706 µA which will insure gain accuracy.

8. R_b can now be found:

$$R_b = \frac{V^+ - V_{BE}(+)}{I_{IN}(+)} = \frac{12 - 0.6}{640\ \mu\text{A}} = 17.8\ \text{k}\Omega$$

9. Since $R_s + r_e$ will be 750Ω and r_e is fixed by the DC mirror current to be:

$$r_e = \frac{KT}{q\ I_{IN(+)}} = \frac{26\ \text{mV}}{640\ \mu\text{A}} \cong 40\Omega \text{ at } 25°\text{C}$$

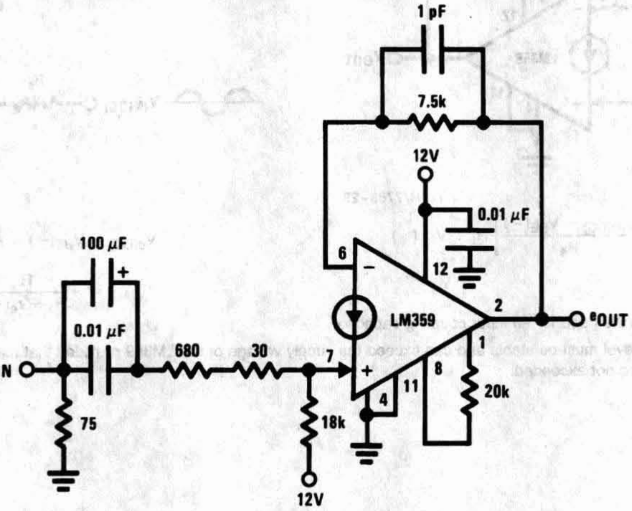
R_s must be 750Ω−40Ω or 710Ω which can be a 680Ω resistor in series with a 30Ω resistor which are standard 5% tolerance resistor values.

10. As a final design step, C_i must be selected to pass the lower passband frequency corner of 8 Hz for this example.

$$C_i = \frac{1}{2\pi\ (R_s + r_e)\ f_{low}} = \frac{1}{2\pi\ (750\Omega)\ (8\ \text{Hz})} = 26.5\ \mu\text{F}$$

A larger value may be used and a 0.01 µF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

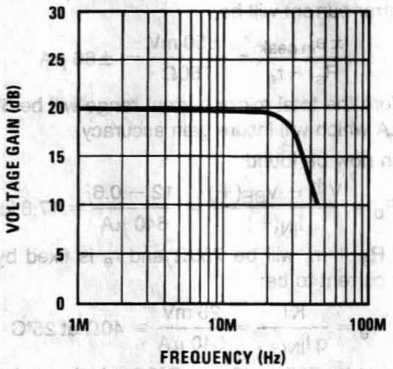
Final Circuit Using Standard 5% Tolerance Resistor Values



TL/H/7788–21

Application Hints (Continued)

Circuit Performance



TL/H/7788-22

$V_{o(DC)} = 5.4V$

Differential phase error < 0.5°

Differential gain error < 2%

$f_{-3\ dB}$ low = 2.5 Hz

GENERAL PRECAUTIONS

The LM359 is designed primarily for single supply operation but split supplies may be used if the negative supply voltage is well regulated as the amplifiers have no negative supply rejection.

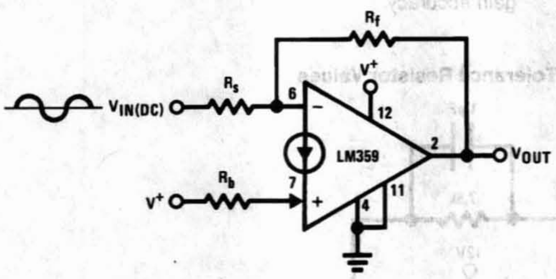
The total device power dissipation must always be kept in mind when selecting an operating supply voltage, the programming current, I_{SET}, and the load resistance, particularly when DC coupling the output to a succeeding stage. To prevent damaging the current mirror input diode, the mirror current should always be limited to 10 mA, or less, which is important if the input is susceptible to high voltage transients. The voltage at any of the inputs must not be forced more negative than −0.7V without limiting the current to 10 mA.

The supply voltage must never be reversed to the device; however, plugging the device into a socket backwards would then connect the positive supply voltage to the pin that has no internal connection (pin 5) which may prevent inadvertent device failure.

Typical Applications

DC Coupled Inputs

Inverting

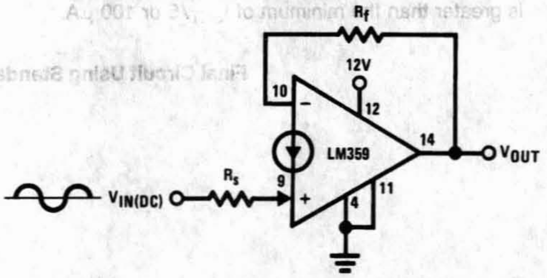


TL/H/7788-23

$$V_{o(DC)} = \left[\frac{V^{+} - V_{BE}(+)}{R_b} - \frac{V_{IN(DC)} - V_{BE}(-)}{R_s}\right] R_f + V_{BE}(-)$$

$$A_{V(AC)} = \frac{R_f}{R_s}$$

Non-Inverting



TL/H/7788-24

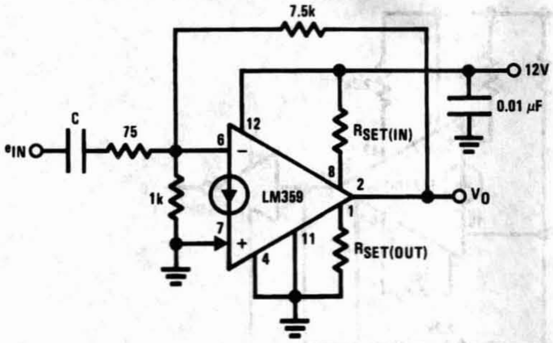
$$V_{o(DC)} = V_{BE}(-) + \frac{(V_{IN(DC)} - V_{BE}(+))\,R_f}{R_s}$$

$$A_{V(AC)} = +\frac{R_f}{R_s + r_e(+)}$$

- Eliminates the need for an input coupling capacitor
- Input DC level must be stable and can exceed the supply voltage of the LM359 provided that maximum input currents are not exceeded.

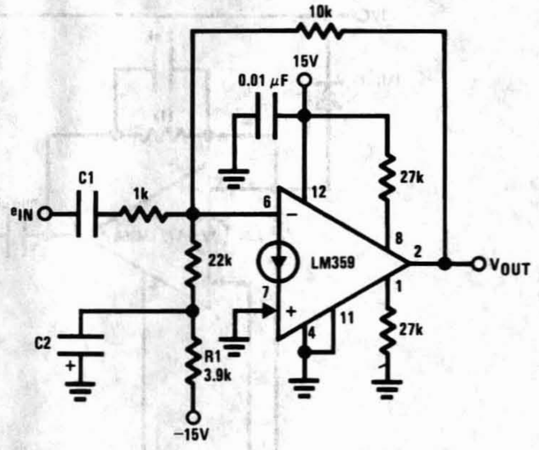
Application Hints (Continued)

Noise Reduction using nV_{BE} Biasing


7.5k
12V
0.01 μF
C
75
e_{IN}
6
12
$R_{SET(IN)}$
8
1k
LM359
2
V_O
−
+
7
1
11
4
$R_{SET(OUT)}$

TL/H/7788-25

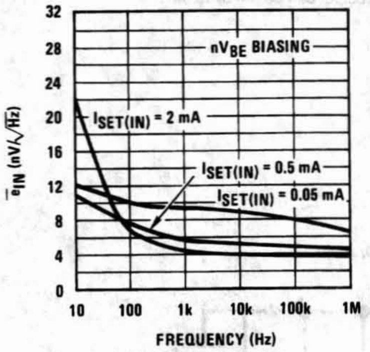
nV_{BE} Biasing with a Negative Supply


10k
15V
0.01 μF
C1
1k
e_{IN}
6
12
27k
8
2
V_{OUT}
−
+
22k
LM359
7
1
11
4
27k
C2
R1
3.9k
−15V

TL/H/7788-26

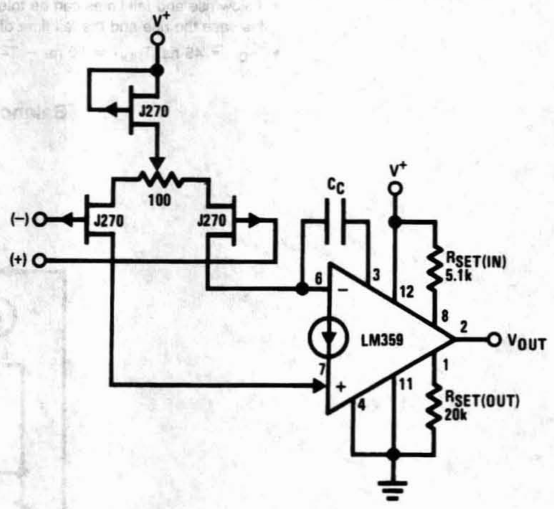
- R1 and C2 provide additional filtering of the negative biasing supply

Typical Input Referred Noise Performance



TL/H/7788-27

Adding a JFET Input Stage

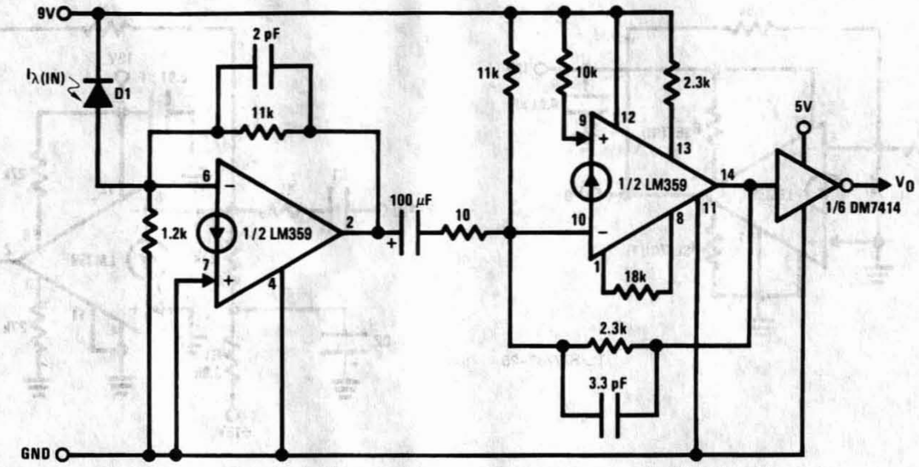

V+
J270
100
J270
J270
(−)
(+)
C_C
V+
$R_{SET(IN)}$ 5.1k
6
3
12
8
2
V_{OUT}
−
+
LM359
7
1
11
4
$R_{SET(OUT)}$ 20k

TL/H/7788-28

- FET input voltage mode op amp
- For $A_V = +1$; BW = 40 MHz, $S_r = 60\ V/\mu s$; $C_C = 51$ pF
- For $A_V = +11$; BW = 24 MHz, $S_r = 130\ V/\mu s$; $C_C = 5$ pF
- For $A_V = +100$; BW = 4.5 MHz, $S_r = 150\ V/\mu s$; $C_C = 2$ pF
- V_{OS} is typically <25 mV; 100Ω potentiometer allows a V_{OS} adjust range of $\approx \pm 200$ mV
- Inputs must be DC biased for single supply operation

Typical Applications (Continued)

Photo Diode Amplifier

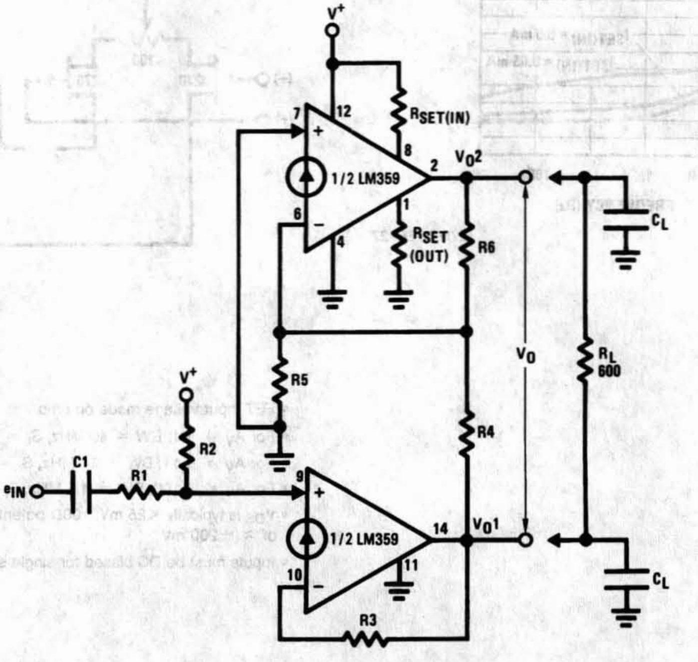

9V
I_{λ}(IN)
D1
2 pF
11k
6
1.2k
1/2 LM359
7
4
2
100 µF
10
11k
10k
2.3k
9
12
13
1/2 LM359
14
10
8
11
1
18k
2.3k
3.3 pF
5V
1/6 DM7414
V_O
GND

TL/H/7788–29

D1 ~ RCA N-Type Silicon P-I-N Photodiode

- Frequency response of greater than 10 MHz
- If slow rise and fall times can be tolerated the gate on the output can be removed. In this case the rise and the fall time of the LM359 is 40 ns.
- T_{PDL} = 45 ns, T_{PDH} = 50 ns − T^2L output

Balanced Line Driver


V+
7
12
$R_{SET(IN)}$
8
1/2 LM359
2
V_O2
6
4
1
R_{SET} (OUT)
R6
C_L
V_O
R_L 600
R5
V+
R2
R4
C1
R1
e_{IN}
9
1/2 LM359
14
V_O1
11
10
R3
C_L

TL/H/7788–30

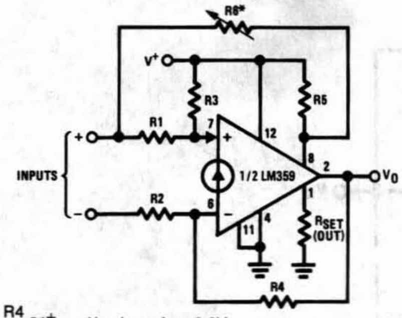
For $V_O1 = V_O2 = \dfrac{V^+}{2}$, $\dfrac{R3}{R2} = \dfrac{V^+ - 2\phi}{2(V^+ - \phi)}$, $\dfrac{R6}{R5} = \dfrac{V^+ - 2\phi}{\phi}$ where $\phi \approx 0.6V$

$$A_V = \frac{R3}{R1}\left(\frac{R6}{R4} + 1\right)$$

- 1 MHz—3 dB bandwidth with gain of 10 and 0 dbm into 600Ω
- 0.3% distortion at full bandwidth; reduced to 0.05% with bandwidth of 10 kHz
- Will drive C_L = 1500 pF with no additional compensation, ±0.01 µF with C_{comp} = 180 pF
- 70 dB signal to noise ratio at 0 dbm into 600Ω, 10 kHz bandwidth

Typical Applications (Continued)

Difference Amplifier


R6*
V+
R3
R5
R1
7
12
INPUTS
+
−
8
2
V0
1/2 LM359
R2
6
1
4
11
RSET (OUT)
R4

TL/H/7788-31

$V_{O(DC)} = \frac{R4}{R3}(V^+ - \phi)$ where $\phi = 0.6V$

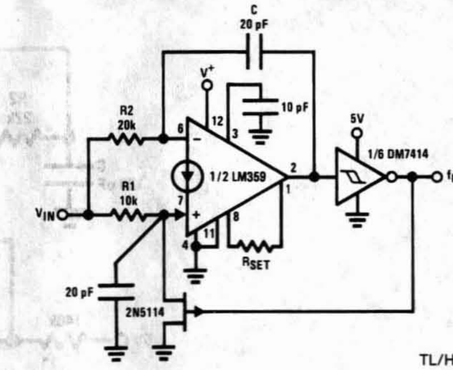
$A_V = \frac{R4}{R1}$ for R1 = R2

*CMRR is adjusted for max at expected CM input signal

$R6 \approx \frac{R5}{5}$, for R5 = 100 kΩ

- Wide bandwidth
- 70 dB CMRR typ
- Wide CM input voltage range

Voltage Controlled Oscillator


C
20 pF
V+
10 pF
12
3
R2
20k
6
5V
1/6 DM7414
f0
R1
10k
1/2 LM359
2
VIN
7
1
8
11
4
RSET
20 pF
2N5114

TL/H/7788-32

$f_o = \frac{V_{IN} - \phi}{4\,C\,\Delta V\,R1}$

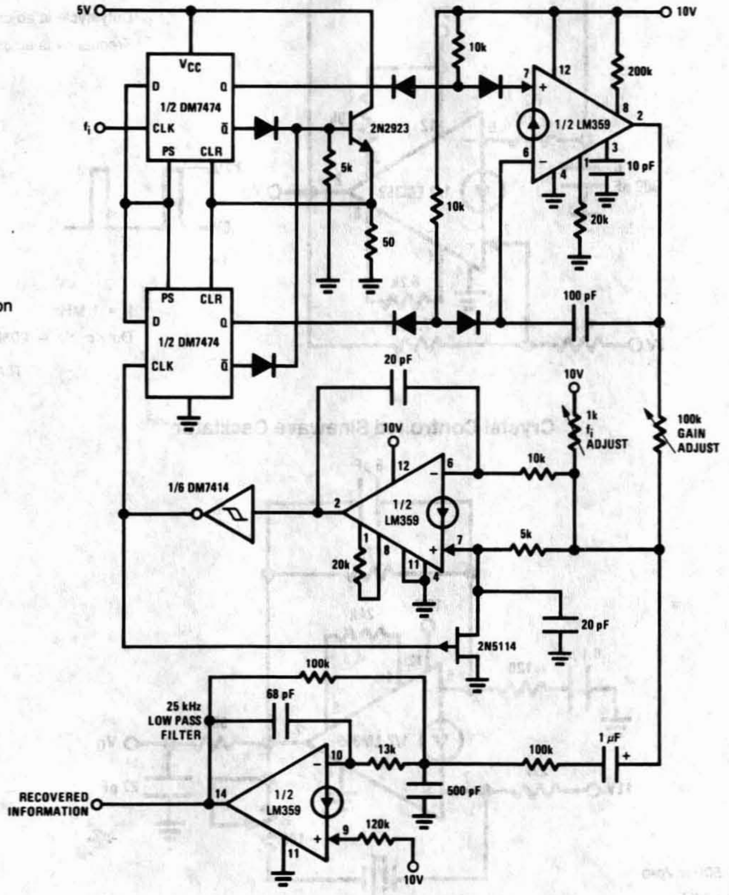
where: R2 = 2R1

ϕ = amplifier input voltage = 0.6V

ΔV = DM7414 hysteresis, typ 1V

- 5 MHz operation
- T²L output

Phase Locked Loop


5V
10V
VCC
D
Q
1/2 DM7474
fi
CLK
Q̄
PS
CLR
2N2923
5k
50
10k
7
12
200k
8
2
1/2 LM359
6
3
10 pF
4
1
20k
10k
PS
CLR
D
Q
1/2 DM7474
CLK
Q̄
100 pF
20 pF
10V
1k
fi ADJUST
100k GAIN ADJUST
10V
12
6
10k
1/6 DM7414
2
1/2 LM359
7
5k
20k
8
11
4
20 pF
2N5114
100k
68 pF
25 kHz LOW PASS FILTER
10
13k
100k
1 µF
+
RECOVERED INFORMATION
14
1/2 LM359
500 pF
9
120k
11
10V

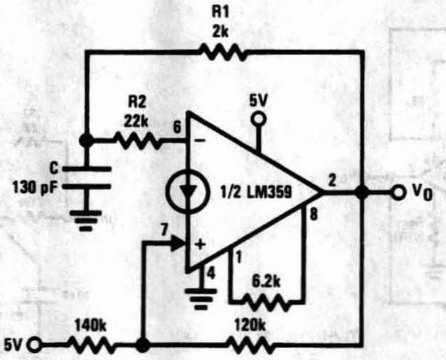
- Up to 5 MHz operation
- T²L compatible input

All diodes = 1N914

TL/H/7788-33

Typical Applications (Continued)

Squarewave Generator


R1
2k
R2
22k
5V
6
C
130 pF
1/2 LM359
2
V_O
8
7
+
1
4
6.2k
5V
140k
120k

TL/H/7788–34

f = 1 MHz

Output is TTL compatible

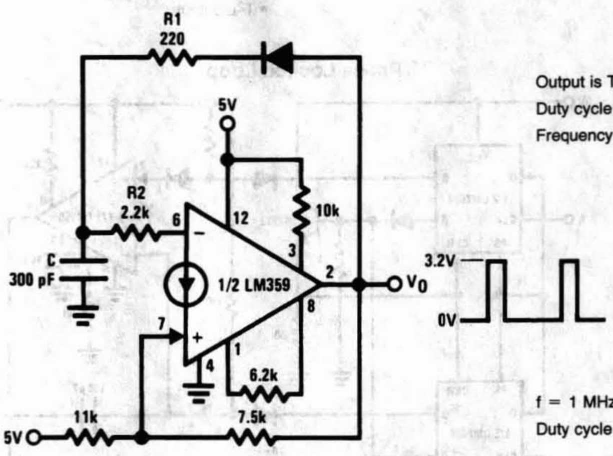
Frequency is adjusted by R1 & C (R1 ≪ R2)

Pulse Generator

Output is TTL compatible

Duty cycle is adjusted by R1

Frequency is adjusted by C

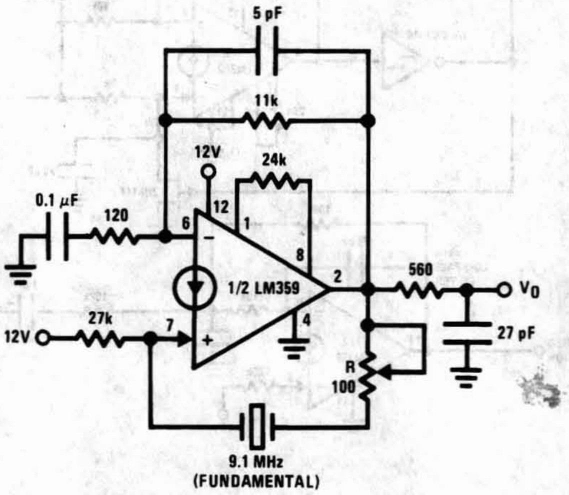

R1
220
5V
R2
2.2k
6
12
10k
3
C
300 pF
1/2 LM359
2
V_O
8
7
+
1
4
6.2k
5V
11k
7.5k
3.2V
0V

f = 1 MHz

Duty cycle = 20%

TL/H/7788–36

Crystal Controlled Sinewave Oscillator


5 pF
11k
12V
24k
0.1 μF
120
6
12
1
8
1/2 LM359
2
560
V_O
12V
27k
7
+
4
27 pF
R
100
9.1 MHz
(FUNDAMENTAL)

V_O = 500 mVp-p

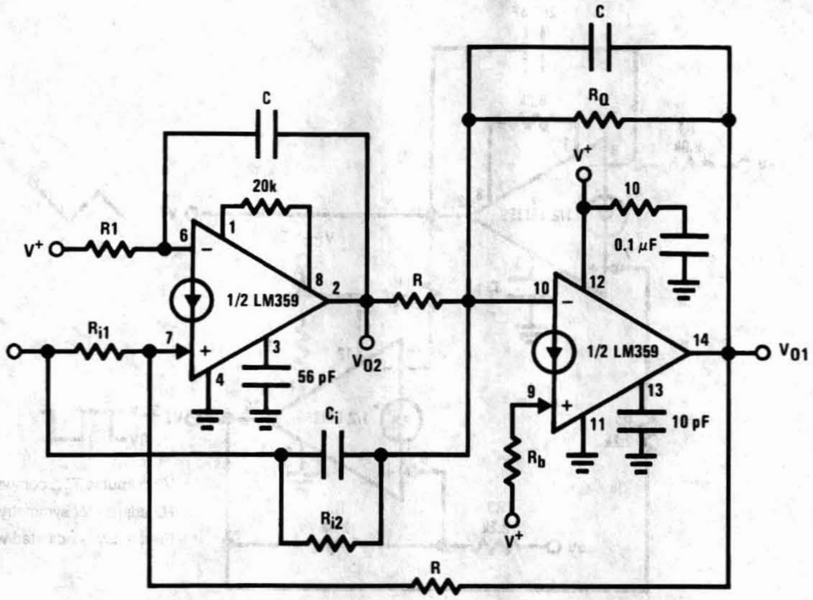
f = 9.1 MHz

THD < 2.5%

TL/H/7788–37

Typical Applications (Continued)

High Performance 2 Amplifier Biquad Filter(s)



TL/H/7788–35

- The high speed of the LM359 allows the center frequency Q_o product of the filter to be: $f_o \times Q_o \leq 5$ MHz
- The above filter(s) maintains performance over wide temperature range
- One half of LM359 acts as a true non-inverting integrator so only 2 amplifiers (instead of 3 or 4) are needed for the biquad filter structure

DC Biasing Equations for $V_{O1(DC)} \cong V_{O2(DC)} \cong V^+/2$

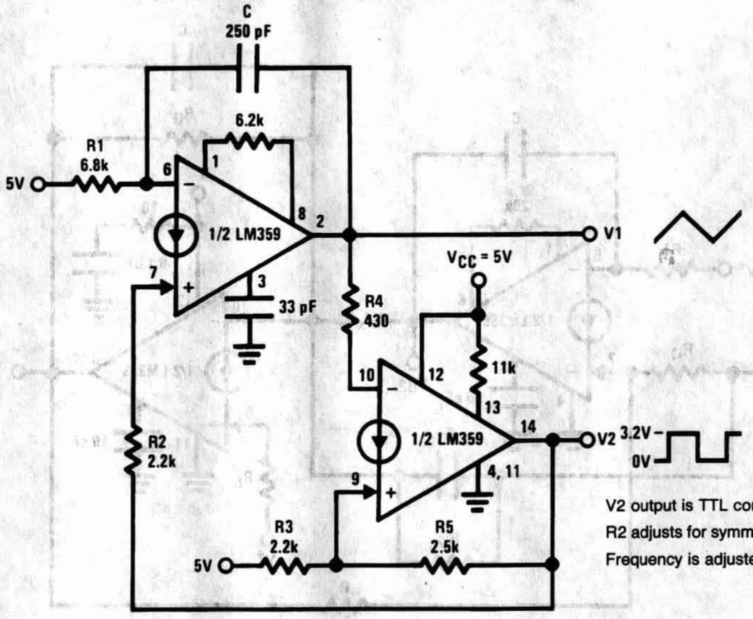
Type I	$\frac{2\,V_{IN(DC)}}{V^+\,(R_{i2})} + \frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type II	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type III	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}; \frac{1}{R1} = \frac{V_{IN(DC)}}{V^+\,(R_{i1})} + \frac{1}{2R}$

Analysis and Design Equations

Type	V_{O1}	V_{O2}	C_i	R_{i2}	R_{i1}	f_o	Q_o	f_Z(notch)	$H_{o(LP)}$	$H_{o(BP)}$	$H_{o(HP)}$	$H_{o(BR)}$
I	BP	LP	O	R_{i2}	∞	$½\,\pi RC$	R_Q/R	—	R/R_{i2}	R_Q/R_{i2}	—	—
II	HP	BP	C_i	∞	∞	$½\,\pi RC$	R_Q/R	—	—	R_QC_i/RC	C_i/C	—
III	Notch/ BR	—	C_i	∞	R_{i1}	$½\,\pi RC$	R_Q/R	$½\pi\,\sqrt{RR_iCC_i}$	—	—	—	$H_o\Big\vert_{f \to \infty} = C_i/C$ $H_o\Big\vert_{f \to O} = C/R_i$

Typical Applications (Continued)

Triangle Waveform Generator


C
250 pF
6.2k
R1
6.8k
5V
6
1
8
2
1/2 LM359
V1
7
3
33 pF
R4
430
VCC = 5V
10
12
11k
13
14
1/2 LM359
V2
3.2V
0V
4, 11
9
R2
2.2k
R3
2.2k
R5
2.5k
5V

V2 output is TTL compatible

R2 adjusts for symmetry of the triangle waveform

Frequency is adjusted with R5 and C

TL/H/7788–38

National Semiconductor

LM392/LM2924
Low Power Operational Amplifier/Voltage Comparator

General Description

The LM392 series consists of 2 independent building block circuits. One is a high gain, internally frequency compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages which will common-mode input down to ground when operating from a single power supply. Operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Application areas include transducer amplifier with pulse shaper, DC gain block with level detector, VCO, as well as all conventional operational amplifier or voltage comparator circuits. Both circuits can be operated directly from the standard 5 V_{DC} power supply voltage used in digital systems, and the output of the comparator will interface directly with either TTL or CMOS logic. In addition, the low power drain makes the LM392 extremely useful in the design of portable equipment.

Advantages

- Eliminates need for dual power supplies
- An internally compensated op amp and a precision comparator in the same package
- Allows sensing at or near ground
- Power drain suitable for battery operation
- Pin-out is the same as both the LM358 dual op amp and the LM393 dual comparator

Features

- Wide power supply voltage range
  - Single supply 3V to 32V
  - Dual supply ±1.5V to ±16V
- Low supply current drain—essentially independent of supply voltage 600 μA
- Low input biasing current 50 nA
- Low input offset voltage 2 mV
- Low input offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage

ADDITIONAL OP AMP FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
- Large output voltage swing 0V to V+ − 1.5V

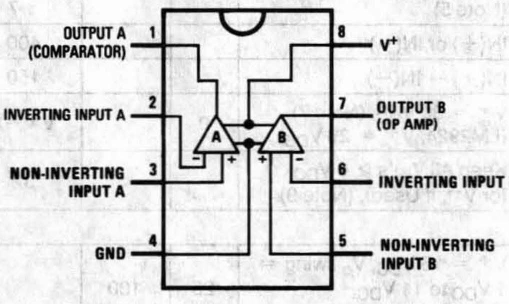
ADDITIONAL COMPARATOR FEATURES

- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with all types of logic systems

Connection Diagram (Top View)

(Amplifier A = Comparator)
(Amplifier B = Operational Amplifier)

Dual-In-Line Package



TL/H/7793-1

Order Number LM392M or LM2924M
See NS Package Number M08A
Order Number LM392N or LM2924N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LM392	LM2924
Supply Voltage, V^+	32V or ±16V	26V or ±13V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP (LM392N, LM2924N)	820 mW	820 mW
Small Outline Package (LM392M, LM2924M)	530 mW	530 mW
Output Short-Circuit to Ground (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA	50 mA
Operating Temperature Range	0°C to +70°C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
ESD rating to be determined.		
Soldering Information		
Dual-in-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 4)

Parameter	Conditions	LM392			LM2924			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		±2	±5		±2	±7	mV
Input Bias Current	IN(+) or IN(−), $T_A = 25°C$, (Note 6), $V_{CM} = 0V$		50	250		50	250	nA
Input Offset Current	IN(+) − IN(−), $T_A = 25°C$		±5	±50		±5	±50	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, $T_A = 25°C$, (Note 7) (LM2924, $V^+ = 26\ V_{DC}$)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	$R_L = \infty$, $V^+ = 30V$, (LM2924, $V^+ = 26V$)		1	2		1	2	mA
Supply Current	$R_L = \infty$, $V^+ = 5V$		0.5	1		0.5	1	mA
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, $T_A = 25°C$, Input Referred, (Note 8)		−100			−100		dB
Input Offset Voltage	(Note 5)			±7			±10	mV
Input Bias Current	IN(+) or IN(−)			400			500	nA
Input Offset Current	IN(+) − IN(−)			150			200	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 7) (LM2924, $V^+ = 26\ V_{DC}$)	0		$V^+ - 2$	0		$V^+ - 2$	V
Differential Input Voltage	Keep All V_{IN}'s ≥ 0 V_{DC} (or V^-, if Used), (Note 9)			32			26	V
OP AMP ONLY								
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$, V_o swing = 1 V_{DC} to 11 V_{DC}, $R_L = 2\ k\Omega$, $T_A = 25°C$	25	100		25	100		V/mV

Electrical Characteristics ($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 4) (Continued)

Parameter	Conditions	LM392			LM2924			Units
		Min	Typ	Max	Min	Typ	Max	
OP AMP ONLY								
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$, (LM2924, $R_L \geq 10\ k\Omega$)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Common-Mode Rejection Ratio	DC, $T_A = 25°C$, $V_{CM} =$ $0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$	65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		50	100		dB
Output Current Source	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o =$ $2\ V_{DC}$, $T_A = 25°C$	20	40		20	40		mA
Output Current Sink	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o =$ $2\ V_{DC}$, $T_A = 25°C$	10	20		10	20		mA
	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o =$ 200 mV, $T_A = 25°C$	12	50		12	50		μA
Input Offset Voltage Drift	$R_S = 0\Omega$		7			7		μV/°C
Input Offset Current Drift	$R_S = 0\Omega$		10			10		pA_{DC}/°C
COMPARATOR ONLY								
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$	50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$ $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 10)		1.3			1.5		μs
Output Sink Current	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V_o \geq 1.5\ V_{DC}$, $T_A = 25°C$	6	16		6	16		mA
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA, $T_A = 25°C$		250	400			400	mV
	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA			700			700	mV
Output Leakage Current	$V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\ V_{DC}$, $V_o = 5\ V_{DC}$, $T_A = 25°C$		0.1			0.1		nA
	$V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\ V_{DC}$, $V_o = 30\ V_{DC}$			1.0			1.0	μA

Note 1: For operating at temperatures above 25°C, the LM392 and the LM2924 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 122°C/W which applies for the device soldered in a printed circuit board, operating in still air ambient. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA for the op amp and 30 mA for the comparator independent of the magnitude of V^+. At values of supply voltage in excess of 15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications apply for $V^+ = 5V$, unless otherwise stated. For the LM392, temperature specifications are limited to $0°C \le T_A \le +70°C$ and the LM2924 temperature specifications are limited to $-40°C \le T_A \le +85°C$.

Note 5: At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$).

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

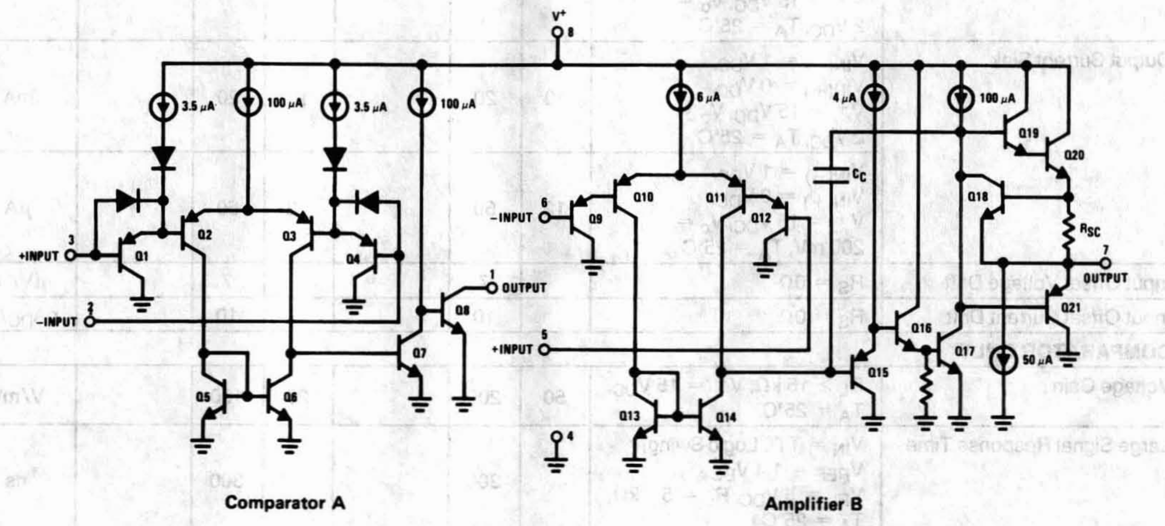
Note 7: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to 32V without damage (26V for LM2924).

Note 8: Due to proximity of external components, insure that coupling is not originating via the stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Note 9: Positive excursions of input voltage may exceed the power supply level. As long as the other input voltage remains within the common-mode range, the comparator will provide a proper output state. The input voltage to the op amp should not exceed the power supply level. The input voltage state must not be less than $-0.3V$ (or 0.3V below the magnitude of the negative power supply, if used) on either amplifier.

Note 10: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

Schematic Diagram



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Application Hints

Please refer to the application hints section of the LM193 and the LM158 datasheets.

National Semiconductor

LM611
Operational Amplifier and Adjustable Reference

General Description

The LM611 consists of a single-supply op-amp and a programmable voltage reference in one space saving 8-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with a wide output swing op-amp makes the LM611 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM611 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

- Low operating current 300 µA (op amp)
- Wide supply voltage range 4V to 36V
- Wide common-mode range V⁻ to (V⁺ −1.8V)
- Wide differential input voltage ±36V
- Available in low cost 8-pin DIP
- Available in plastic package rated for Military Temperature Range Operation

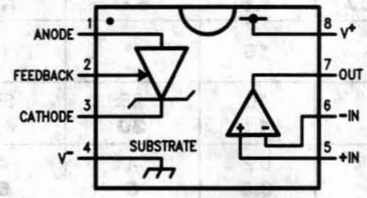
REFERENCE

- Adjustable output voltage 1.2V to 6.3V
- Tight initial tolerance available ±0.6%
- Wide operating current range 17 µA to 20 mA
- Reference floats above ground
- Tolerant of load capacitance

Applications

- Transducer bridge driver
- Process and Mass Flow Control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagrams



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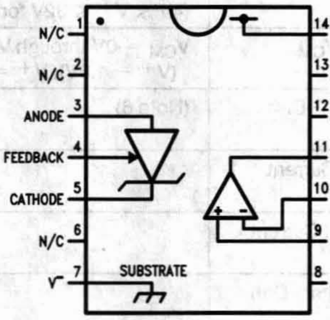

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Ordering Information

Reference Tolerance & V_{OS}	Temperature Range			Package	NSC Drawing
	Military $-55°C \leq T_A \leq +125°C$	Industrial $-40°C \leq T_A \leq +85°C$	Commercial $0°C \leq T_A \leq +70°C$		
±0.6% @ 80 ppm/°C max V_{OS} = 3.5 mV max	LM611AMN	LM611AIN	—	8-pin molded DIP	N08E
	LM611AMJ/883 (Note 12)	—	—	8-pin ceramic DIP	J08A
±2.0% @ 150 ppm/°C max V_{OS} = 5 mV max	LM611MN	LM611BIN	LM611CN	8-pin molded DIP	N08E
	—	LM611IM	LM611CM	14-pin Narrow Surface Mount	M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pins Except V_R	
(referred to V^- pin)	36V (Max)
(Note 2)	−0.3V (Min)
Current through Any Input Pin and V_R Pin	±20 mA
Differential Input Voltage	
Military and Industrial	±36V
Commercial	±32V
Storage Temperature Range	$-65°C \leq T_J \leq +150°C$
Maximum Junction Temperature	150°C
Thermal Resistance, Junction-to-Ambient (Note 3)	
N Package	100°C/W
M Package	150°C/W
Soldering Information Soldering (10 seconds)	
N Package	260°C
M Package	220°C
ESD Tolerance (Note 4)	±1 kV

Operating Temperature Range

LM611AI, LM611I, LM611BI	$-40°C \leq T_J \leq +85°C$
LM611AM, LM611M	$-55°C \leq T_J \leq +125°C$
LM611C	$0°C \leq T_J \leq 70°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 5)	LM611AM LM611AI Limits (Note 6)	LM611M LM611BI LM611I LM611C Limits (Note 6)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \leq V^+ \leq 36V$ (32V for LM611C)	210 **221**	300 **320**	350 **370**	μA max μA max
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	2.8 **3**	V min V min
			46 **43**	36 **36**	32 **32**	V max V max
OPERATIONAL AMPLIFIER						
V_{OS1}	V_{OS} Over Supply	$4V \leq V^+ \leq 36V$ ($4V \leq V^+ \leq 32V$ for LM611C)	1.5 **2.0**	3.5 **6.0**	5.0 **7.0**	mV max mV max
V_{OS2}	V_{OS} Over V_{CM}	$V_{CM} = 0V$ through $V_{CM} =$ $(V^+ - 1.8V)$, $V^+ = 30V$, $V^- = 0V$	1.0 **1.5**	3.5 **6.0**	5.0 **7.0**	mV max mV max
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 6)	**15**			μV/°C max
I_B	Input Bias Current		10 **11**	25 **30**	35 **40**	nA max nA max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA max nA max
$\frac{I_{OS1}}{\Delta T}$	Average Offset Drift Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1800			MΩ
		Common-Mode	3800			MΩ
C_{IN}	Input Capacitance	Common-Mode	5.7			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection-Ratio	$V^+ = 30V$, $0V \leq V_{CM} \leq (V^+ - 1.8V)$ $CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	95 **90**	80 **75**	75 **70**	dB min dB min
PSRR	Power Supply Rejection-Ratio	$4V \leq V^+ \leq 30V$, $V_{CM} = V^+/2$, $PSRR = 20 \log (\Delta V^+/\Delta V_{OS})$	110 **100**	80 **75**	75 **70**	dB min dB min
A_V	Open Loop Voltage Gain	$R_L = 10\ k\Omega$ to GND, $V^+ = 30V$, $5V \leq V_{OUT} \leq 25V$	500 **50**	100 **40**	94 **40**	V/mV min
SR	Slew Rate	$V^+ = 30V$ (Note 7)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/μs

Electrical Characteristics (Continued)

These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{CM} = V_{OUT} = 2.5\text{V}$, $I_R = 100\ \mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 5)	LM611AM LM611AI Limits (Note 6)	LM611M LM611BI LM611I LM611C Limits (Note 6)	Units
OPERATIONAL AMPLIFIER (Continued)						
GBW	Gain Bandwidth	$C_L = 50$ pF	0.80 **0.50**			MHz
V_{O1}	Output Voltage Swing High	$R_L = 10\ \text{k}\Omega$ to GND $V^+ = 36\text{V}$ (32V for LM611C)	$V^+ - 1.4$ **$V^+ - 1.6$**	$V^+ - 1.7$ **$V^+ - 1.9$**	$V^+ - 1.8$ **$V^+ - 1.9$**	V min V min
V_{O2}	Output Voltage Swing Low	$R_L = 10\ \text{k}\Omega$ to V^+ $V^+ = 36\text{V}$ (32V for LM611C)	$V^- + 0.8$ **$V^- + 0.9$**	$V^- + 0.9$ **$V^- + 1.0$**	$V^- + 0.95$ **$V^- + 1.0$**	V max V max
I_{OUT}	Output Source Current	$V_{OUT} = 2.5\text{V}$, $V_{+IN} = 0\text{V}$, $V_{-IN} = -0.3\text{V}$	25 **15**	20 **13**	16 **13**	mA min mA min
I_{SINK}	Output Sink Current	$V_{OUT} = 1.6\text{V}$, $V_{+IN} = 0\text{V}$, $V_{-IN} = 0.3\text{V}$	17 **9**	14 **8**	13 **8**	mA min mA min
I_{SHORT}	Short Circuit Current	$V_{OUT} = 0\text{V}$, $V_{+IN} = 3\text{V}$, $V_{-IN} = 2\text{V}$, Source	30 **40**	50 **60**	50 **60**	mA max mA max
		$V_{OUT} = 5\text{V}$, $V_{+IN} = 2\text{V}$, $V_{-IN} = 3\text{V}$, Sink	30 **32**	60 **80**	70 **90**	mA max mA max
VOLTAGE REFERENCE						
V_R	Reference Voltage	(Note 8)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2.0%)	V min V max
$\frac{\Delta V_R}{\Delta T}$	Average Temperature Drift	(Note 9)	**10**	**80**	**150**	PPM/°C max
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	Hyst $= (\text{Vro}' - \text{Vro})/\Delta T_J$ (Note 10)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV max mV max
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 11)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV max mV max
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}/9.9$ mA $\Delta V_{R(100 \rightarrow 17\ \mu A)}/83\ \mu$A	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω max Ω max
$\frac{\Delta V_R}{V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro = Vr)} - V_{R(Vro = 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV max mV max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R(V^+ = 5V)} - V_{R(V^+ = 36V)}$ ($V^+ = 32\text{V}$ for LM611C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV max mV max
		$V_{R(V^+ = 5V)} - V_{R(V^+ = 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV max mV max
$\frac{\Delta V_R}{\Delta V_{ANODE}}$	V_R Change with V_{ANODE} Change	$V^+ = V^+$ max, $\Delta V_R = V_R$ (@ $V_{ANODE} = V^- = \text{GND}) - V_R$ (@ $V_{ANODE} = V^+ - 1.0\text{V}$)	0.7 **3.3**	1.5 **3.0**	1.6 **3.0**	mV max mV max
I_{FB}	FEEDBACK Bias Current	I_{FB}; $V_{ANODE} \le V_{FB} \le 5.06\text{V}$	22 **29**	35 **40**	50 **55**	nA max nA max
e_n	V_R Noise	10 Hz to 10,000 Hz, $V_{RO} = V_R$	30			μV_{RMS}

Electrical Characteristics (Continued)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 3: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one op amp or reference output transistor, nominal θ_{JA} is 90°C/W for the N package amd 135°C/W for the M package

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold face type).**

Note 7: Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and output voltage transition is sampled at 20V and 10V.

Note 8: V_R is the cathode-feedback voltage, nominally 1.244V.

Note 9: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R / (V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

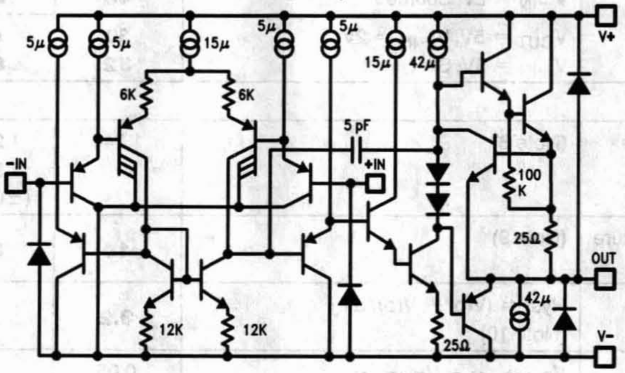
Note 10: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 11: Low contact resistance is required for accurate measurement.

Note 12: Military RETS 611AMX electrical test specification is available on request. The LM611AMJ/883 can also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams

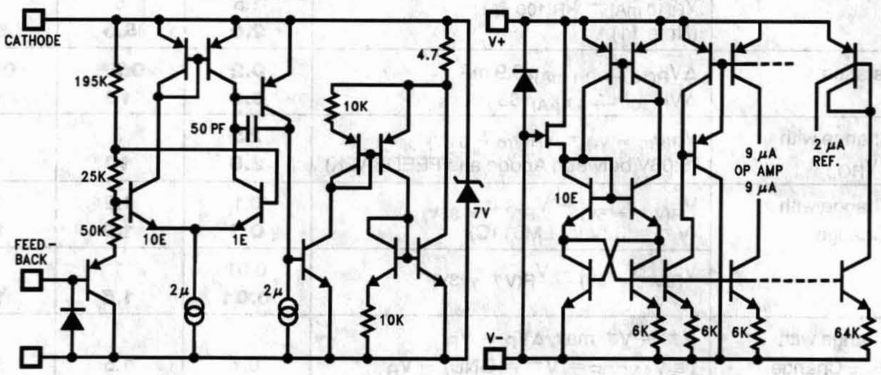
Op Amp



TL/H/9221-3

Reference

Bias

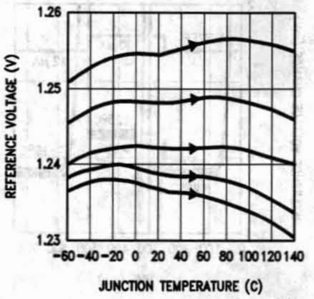


TL/H/9221-4

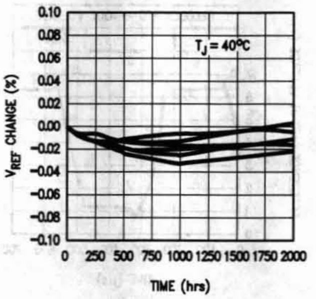
Typical Performance Characteristics (Reference)

$T_J = 25°C$, FEEDBACK pin shorted to $V^- = 0V$, unless otherwise noted

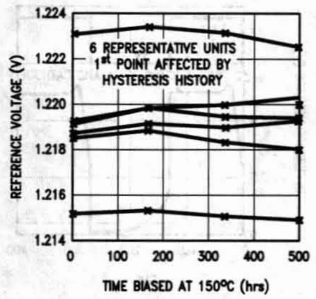
Reference Voltage vs Temp on 5 Representative Units



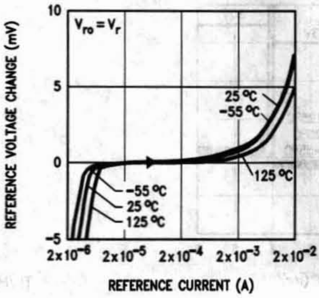
Reference Voltage Drift



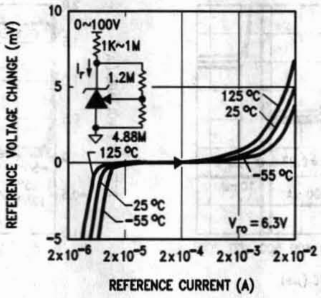
Accelerated Reference Voltage Drift vs Time



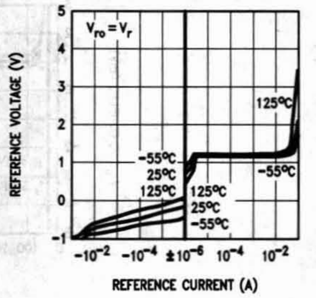
Reference Voltage vs Current and Temperature



Reference Voltage vs Current and Temperature

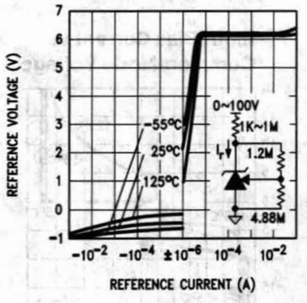


Reference Voltage vs Reference Current

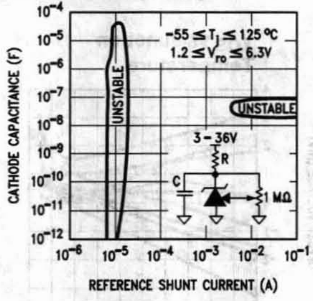


TL/H/9221–5

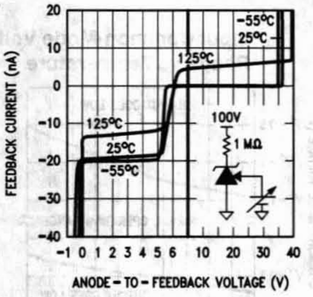
Reference Voltage vs Reference Current



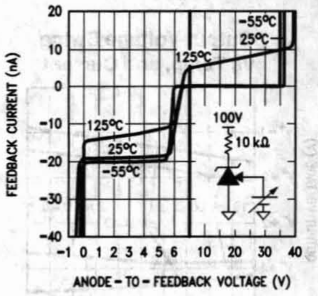
Reference AC Stability Range



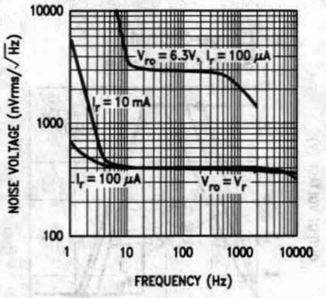
Feedback Current vs Feedback-to-Anode Voltage



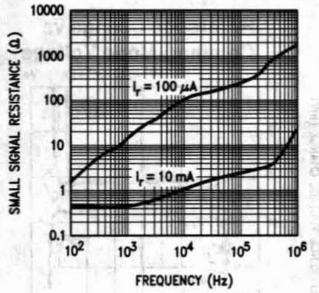
Feedback Current vs Feedback-to-Anode Voltage



Reference Noise Voltage vs Frequency



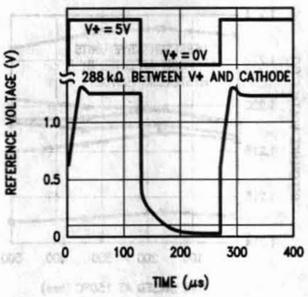
Reference Small-Signal Resistance vs Frequency



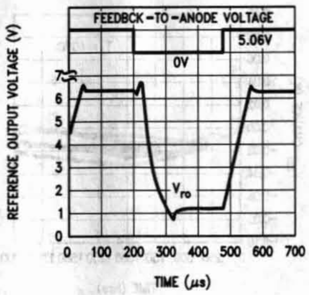
TL/H/9221–6

Typical Performance Characteristics (Reference) (Continued)

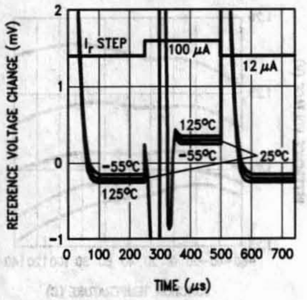
$T_J = 25°C$, FEEDBACK pin shorted to $V^- = 0V$, unless otherwise noted



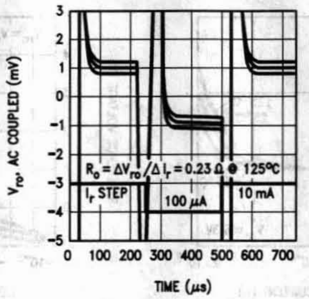
Reference Power-Up Time



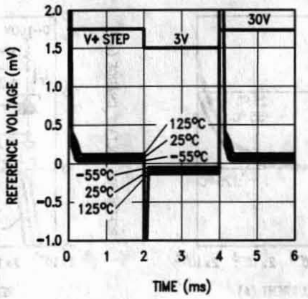
Reference Voltage with Feedback Voltage Step



Reference Voltage with 100 ~ 12 µA Current Step



Reference Step Response for 100 µA ~ 10 mA Current Step

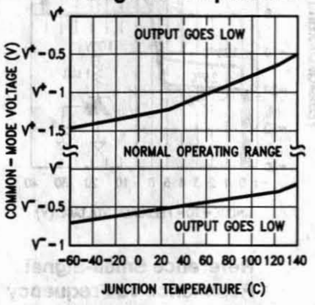


Reference Voltage Change with Supply Voltage Step

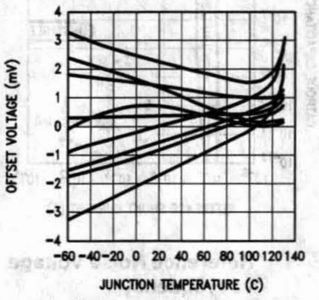
TL/H/9221–7

Typical Performance Characteristics (Op Amps)

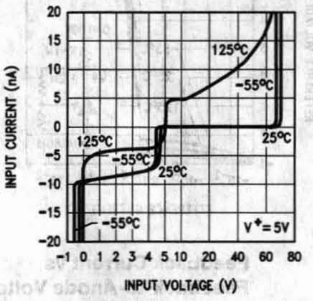
$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted



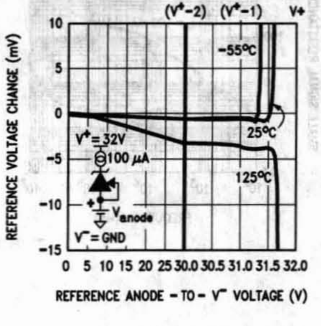
Input Common-Mode Voltage Range vs Temperature



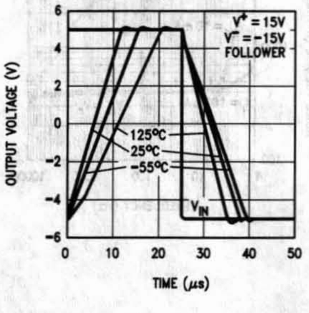
V_{OS} vs Junction Temperature



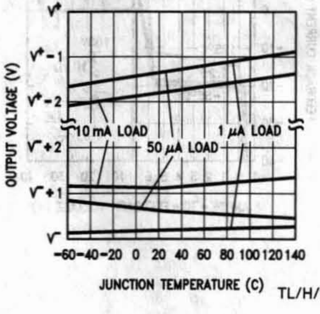
Input Bias Current vs Common-Mode Voltage



Reference Change vs Common-Mode Voltage



Large-Signal Step Response



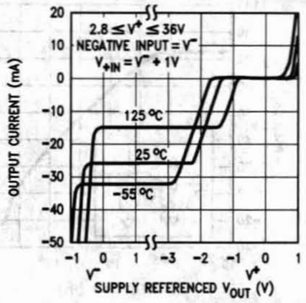
Output Voltage Swing vs Temp. and Current

TL/H/9221–8

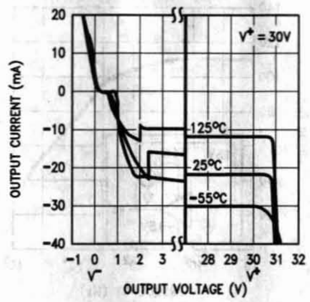
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

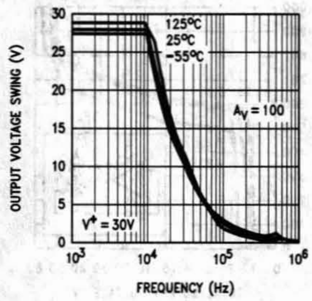
Output Source Current vs Output Voltage and Temp.



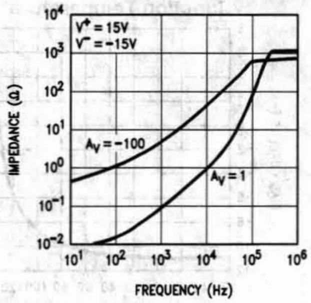
Output Sink Current vs Output Voltage



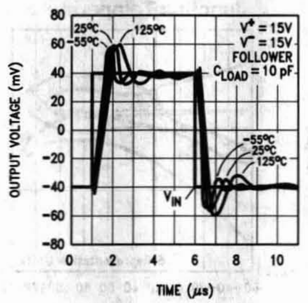
Output Swing, Large Signal



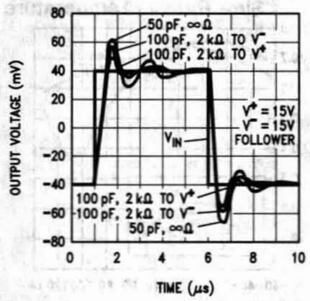
Output Impedance vs Frequency and Gain



Small Signal Pulse Response vs Temp.

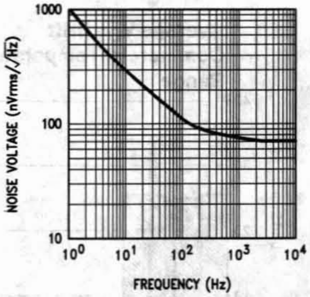


Small-Signal Pulse Response vs Load

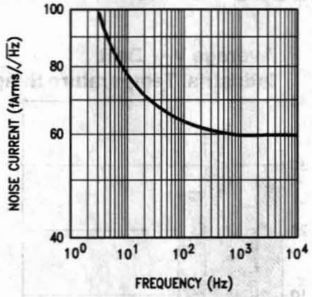


TL/H/9221–9

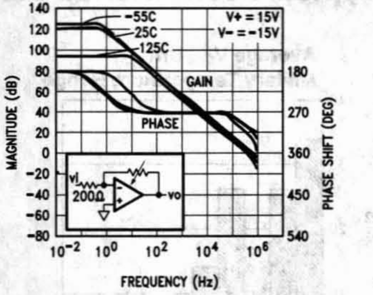
Op Amp Voltage Noise vs Frequency



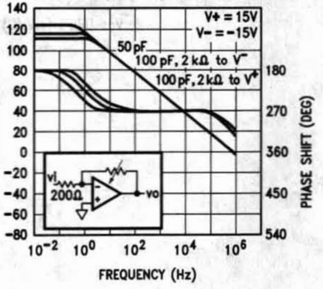
Op Amp Current Noise vs Frequency



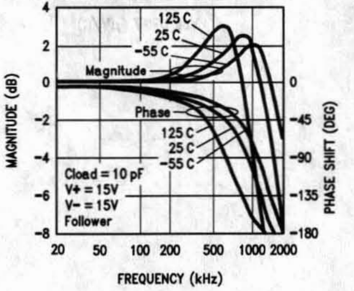
Small-Signal Voltage Gain vs Frequency and Temperature



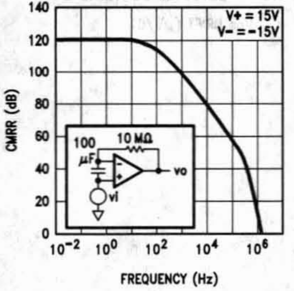
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

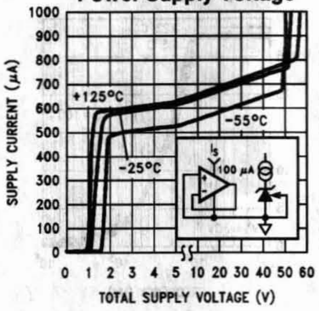


TL/H/9221–10

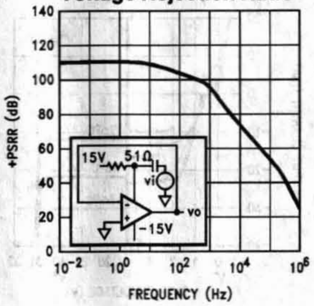
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- \text{ Q GND} = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

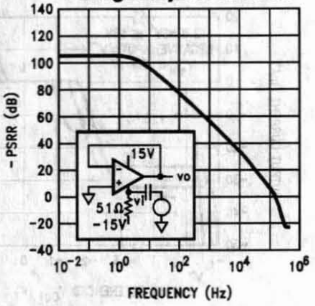
Power Supply Current vs Power Supply Voltage



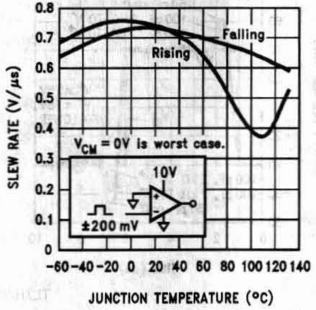
Positive Power Supply Voltage Rejection Ratio



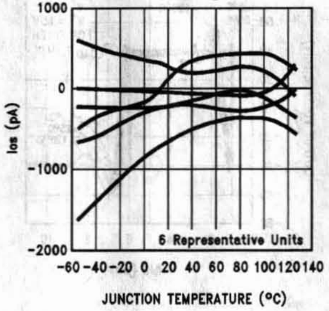
Negative Power Supply Voltage Rejection Ratio



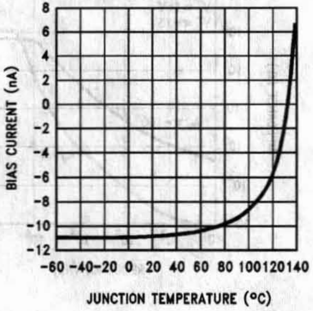
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature



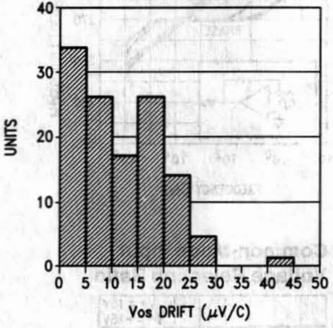
Input Bias Current vs Junction Temperature



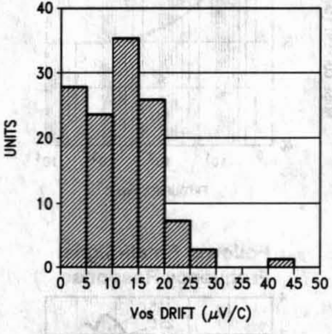
TL/H/9221–11

Typical Performance Distributions

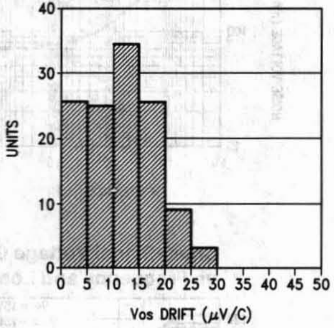
Average V_{OS} Drift Military Temperature Range



Average V_{OS} Drift Industrial Temperature Range

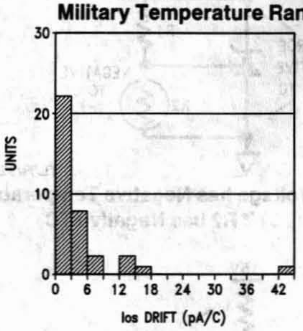


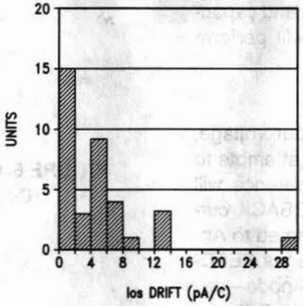
Average V_{OS} Drift Commercial Temperature Range

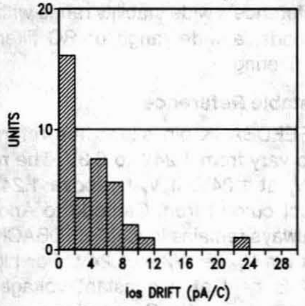


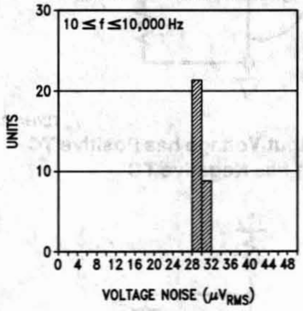
TL/H/9221–12

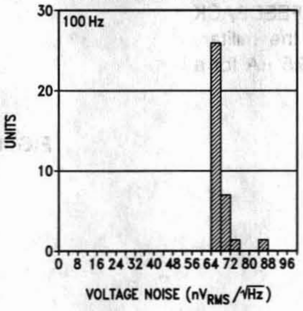
Typical Performance Distributions (Continued)

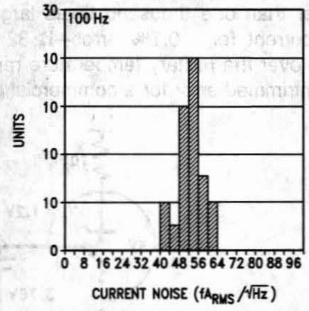

Average I_{OS} Drift
Military Temperature Range


Average I_{OS} Drift
Industrial Temperature Range


Average I_{OS} Drift
Commercial Temperature Range


Voltage Reference Broad-Band
Noise Distribution


Op Amp Voltage
Noise Distribution


Op Amp Current
Noise Distribution

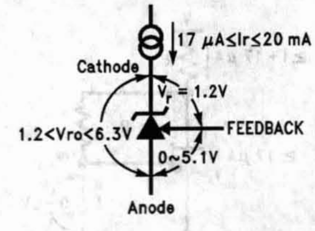
TL/H/9221–13

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The applied voltage to the cathode may range from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.

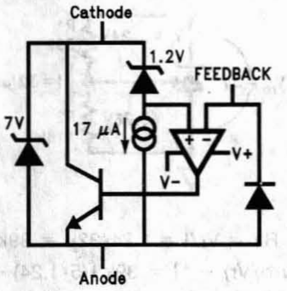


TL/H/9221–14

FIGURE 1. Voltages Associated with Reference (Current Source I_r is External)

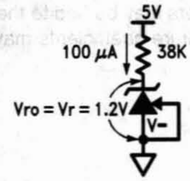
The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.



TL/H/9221–15

FIGURE 2. Reference Equivalent Circuit



TL/H/9221–16

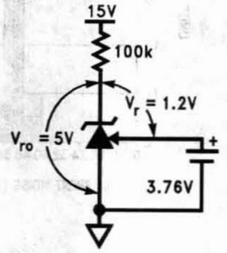
FIGURE 3. 1.2V Reference

Application Information (Continued)

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

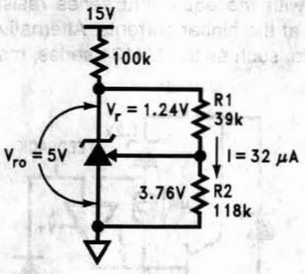
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constant V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—$I \geq 32$ μA for the military grade over the military temperature range ($I \geq 5.5$ μA for a 1% untrimmed error for a commercial part.)


15V
100k
V_r = 1.2V
V_{ro} = 5V
+
3.76V

TL/H/9221–17

FIGURE 4. Thevenin Equivalent of Reference with 5V Output


15V
100k
R1
39k
V_r = 1.24V
V_{ro} = 5V
I = 32 µA
3.76V
R2
118k

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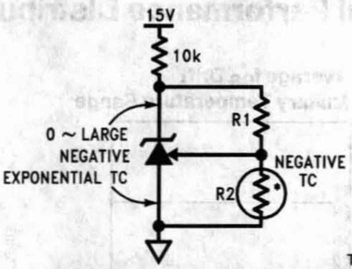
$R1 = Vr/I = 1.24/32\mu = 39k$

$R2 = R1 \{(Vro/Vr) - 1\} = 39k \{(5/1.24) - 1)\} = 118k$

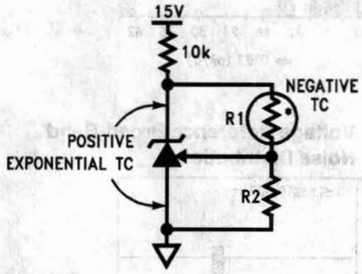
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.


15V
10k
R1
0 ~ LARGE
NEGATIVE
EXPONENTIAL TC
NEGATIVE
TC
R2

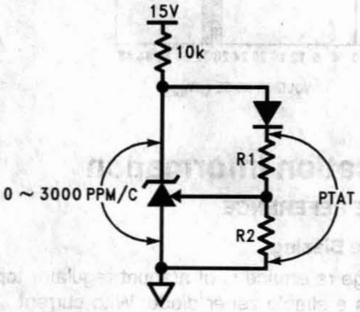
TL/H/9221–19

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC


15V
10k
NEGATIVE
TC
R1
POSITIVE
EXPONENTIAL TC
R2

TL/H/9221–20

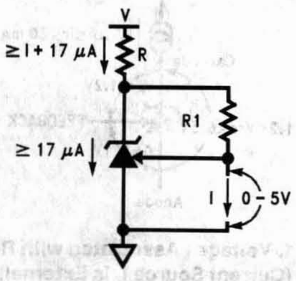
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC


15V
10k
R1
0 ~ 3000 PPM/C
PTAT
R2

TL/H/9221–21

FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.

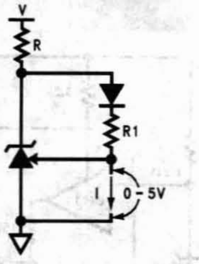

V
≥ I + 17 µA
R
R1
≥ 17 µA
I
0 – 5V

TL/H/9221–22

$I = Vr/R1 = 1.24/R1$

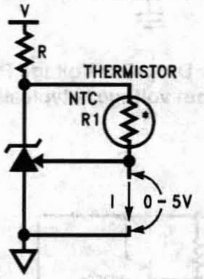
FIGURE 9. Current Source is Programmed by R1

Application Information (Continued)



TL/H/9221-23

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9221-24

FIGURE 11. Negative −TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIER

The amp or the reference may be biased in any way with no effect on the other, except when a substrate diode conducts (see Guaranteed Electrical Characteristics Note 1). The amp may have inputs outside the common-mode range, may be operated as a comparator, or have all terminals floating with no effect on the reference (tying inverting input to output and non-inverting input to V^- on unused amp is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

The op amp, like the LM124 series, has a flexible and relatively wide-swing output stage. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.

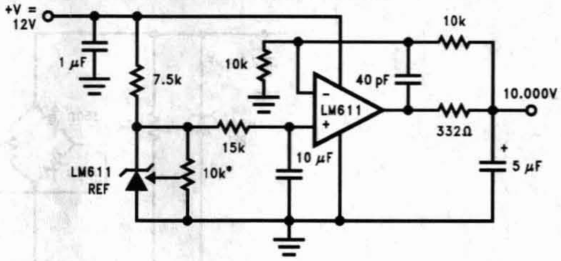
2) Cross-over Distortion: The LM611 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.

3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Op Amp Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

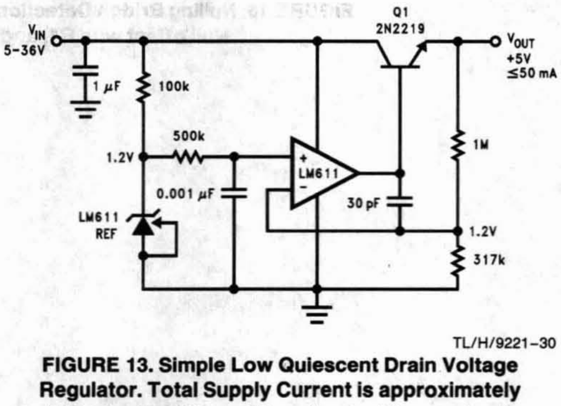
Typical Applications



*10k must be low t.c. trim pot.

TL/H/9221-28

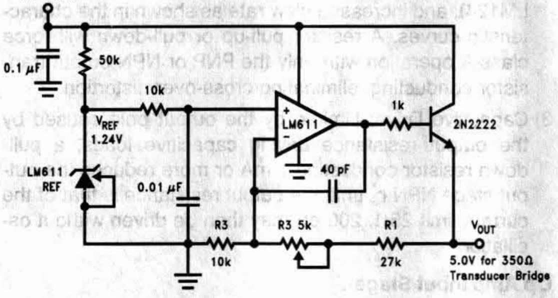
FIGURE 12. Ultra Low Noise 10.00V Reference. Total Output Noise is Typically 14 μV_{RMS}. Adjust the 10k pot for 10.000V.



TL/H/9221-30

FIGURE 13. Simple Low Quiescent Drain Voltage Regulator. Total Supply Current is approximately 320 μA when V_{IN} = 5V, and output has no load.

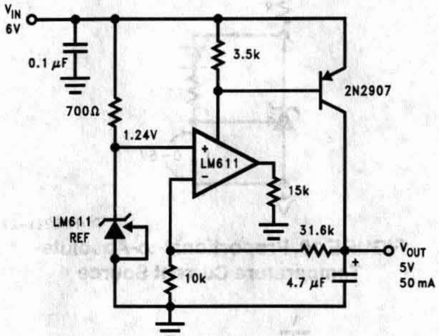
Typical Applications (Continued)


+V = 15V
0.1 µF
50k
10k
V_{REF}
1.24V
LM611
1k
2N2222
LM611
REF
0.01 µF
40 pF
R3
R3 5k
R1
V_{OUT}
10k
27k
5.0V for 350Ω
Transducer Bridge

TL/H/9221-29

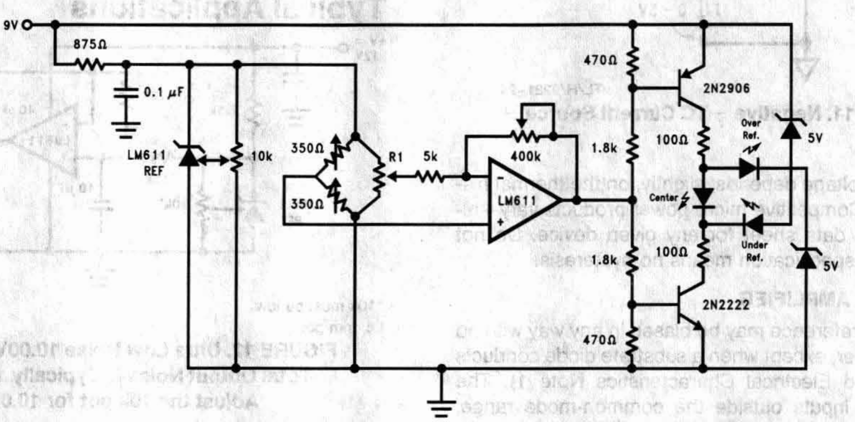
$V_{OUT} = (R1/R2 + 1) V_{REF}$.
R1, R2 should be 1% metal film.
R3 should be low t.c. trim pot.

FIGURE 14. Slow Rise-Time Upon Power-Up, Adjustable Transducer Bridge Driver. Rise-time is approximately 0.5 ms.


V_{IN}
6V
0.1 µF
3.5k
2N2907
700Ω
1.24V
LM611
15k
LM611
REF
31.6k
V_{OUT}
5V
50 mA
10k
4.7 µF

TL/H/9221-31

FIGURE 15. Low Drop-Out Voltage Regulator Circuit. Drop out voltage is typically 0.2V.


9V
875Ω
0.1 µF
LM611
REF
10k
350Ω
350Ω
R1
5k
400k
LM611
470Ω
2N2906
1.8k
100Ω
Over
Ref.
5V
Center
100Ω
Under
Ref.
1.8k
5V
2N2222
470Ω

TL/H/9221-32

FIGURE 16. Nulling Bridge Detection System. Adjust sensitivity via 400 kΩ pot. Null offset with R1, and bridge drive with the 10k pot.

National Semiconductor

LM613 Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

General Description

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

- Low operating current (Op Amp) 300 μA
- Wide supply voltage range 4V to 36V
- Wide common-mode range V^- to $(V^+ - 1.8V)$
- Wide differential input voltage ±36V
- Available in plastic package rated for Military Temp. Range Operation

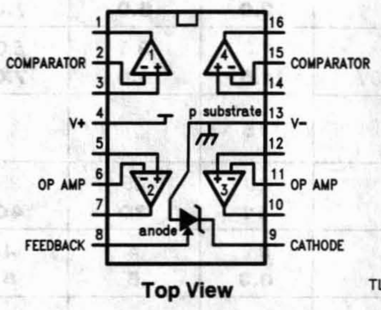
REFERENCE

- Adjustable output voltage 1.2V to 6.3V
- Tight initial tolerance available ±0.6%
- Wide operating current range 17 μA to 20 mA
- Tolerant of load capacitance

Applications

- Transducer bridge driver
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

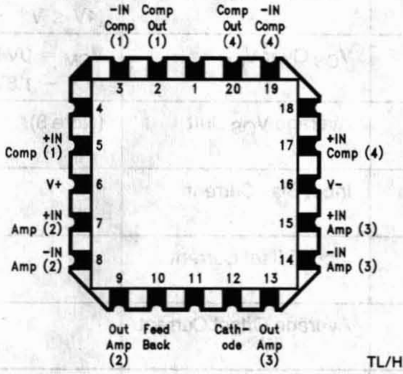
Connection Diagrams


1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
COMPARATOR
COMPARATOR
V+
p substrate
V−
OP AMP
OP AMP
FEEDBACK
anode
CATHODE

Top View

TL/H/9226-1

E Package Pinout


−IN Comp (1)
Comp Out (1)
Comp Out (4)
−IN Comp (4)
3
2
1
20
19
4
18
+IN Comp (1)
5
17
+IN Comp (4)
V+
6
16
V−
+IN Amp (2)
7
15
+IN Amp (3)
−IN Amp (2)
8
14
−IN Amp (3)
9
10
11
12
13
Out Amp (2)
Feed Back
Cath- ode
Out Amp (3)

TL/H/9226-48

Ordering Information

Reference Tolerance & V_{OS}	Temperature Range			Package	NSC Drawing
	Military $-55°C \leq T_A \leq +125°C$	Industrial $-40°C \leq T_A \leq +85°C$	Commercial $0°C \leq T_A \leq +70°C$		
±0.6% 80 ppm/°C Max. $V_{OS} \leq 3.5$ mV	LM613AMN	LM613AIN	—	16-Pin Molded DIP	N16E
	LM613AMJ/883 (Note 14)	—	—	16-Pin Ceramic DIP	J16A
	LM613AME/883 (Note 14)	—	—	20-Pin LCC	E20A
±2.0% 150 ppm/°C Max. $V_{OS} \leq 5.0$ mV Max.	LM613MN	LM613IN	LM613CN	16-Pin Molded DIP	N16E
	—	LM613IWM		16-Pin Wide Surface Mount	M16B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except V_R (referred to V^- pin)	
(Note 2)	36V (Max)
(Note 3)	−0.3V (Min)
Current through Any Input Pin & V_R Pin	±20 mA
Differential Input Voltage	
Military and Industrial	±36V
Commercial	±32V
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Maximum Junction Temperature (Note 4)	150°C
Thermal Resistance, Junction-to-Ambient (Note 5)	
N Package	100°C/W
WM Package	150°C/W
Soldering Information (10 Seconds)	
N Package	260°C
WM Package	220°C
ESD Tolerance (Note 6)	±1 kV

Operating Temperature Range

LM613AI, LM613BI	−40°C to +85°C
LM613AM, LM613M	−55°C to +125°C
LM613C	$0°C \le T_J \le +70°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ (32V for LM613C)	450 **550**	940 **1000**	1000 **1070**	μA (Max) μA (Max)
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	2.8 **3**	V (Min) V (Min)
			46 **43**	36 **36**	32 **32**	V (Max) V (Max)
OPERATIONAL AMPLIFIERS						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$ ($4V \le V^+ \le 32V$ for LM613C)	1.5 **2.0**	3.5 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
V_{OS2}	V_{OS} Over V_{CM}	$V_{CM} = 0V$ through $V_{CM} = (V^+ - 1.8V)$, $V^+ = 30V$, $V^- = 0V$	1.0 **1.5**	3.5 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 8)	**15**			μV/°C (Max)
I_B	Input Bias Current		10 **11**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
$\frac{I_{OS1}}{\Delta T}$	Average Offset Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1000			MΩ
C_{IN}	Input Capacitance	Common-Mode	6			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			nV/$\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			fA/$\sqrt{Hz}$
CMRR	Common-Mode Rejection Ratio	$V^+ = 30V$, $0V \le V_{CM} \le (V^+ - 1.8V)$ CMRR = 20 log ($\Delta V_{CM}/\Delta V_{OS}$)	95 **90**	80 **75**	75 **70**	dB (Min) dB (Min)
PSRR	Power Supply Rejection Ratio	$4V \le V^+ \le 30V$, $V_{CM} = V^+/2$, PSRR = 20 log ($\Delta V^+/V_{OS}$)	110 **100**	80 **75**	75 **70**	dB (Min) dB (Min)
A_V	Open Loop Voltage Gain	$R_L = 10\ k\Omega$ to GND, $V^+ = 30V$, $5V \le V_{OUT} \le 25V$	500 **50**	100 **40**	94 **40**	V/mV (Min)

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over **Operating Temperature Range**. (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
OPERATIONAL AMPLIFIERS (Continued)						
SR	Slew Rate	$V^+ = 30V$ (Note 9)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/µs
GBW	Gain Bandwidth	$C_L = 50$ pF	0.8 **0.5**			MHz MHz
V_{O1}	Output Voltage Swing High	$R_L = 10$ kΩ to GND, $V^+ = 36V$ (32V for LM613C)	$V^+ - 1.4$ **$V^+ - 1.6$**	$V^+ - 1.7$ **$V^+ - 1.9$**	$V^+ - 1.8$ **$V^+ - 1.9$**	V (Min) V (Min)
V_{O2}	Output Voltage Swing Low	$R_L = 10$ kΩ to V^+, $V^+ = 36V$ (32V for LM613C)	$V^- + 0.8$ **$V^- + 0.9$**	$V^- + 0.9$ **$V^- + 1.0$**	$V^- + 0.95$ **$V^- + 1.0$**	V (Max) V (Max)
I_{OUT}	Output Source Current	$V_{OUT} = 2.5V$, $V^+_{IN} = 0V$, $V^-_{IN} = -0.3V$	25 **15**	20 **13**	16 **13**	mA (Min) mA (Min)
I_{SINK}	Output Sink Current	$V_{OUT} = 1.6V$, $V^+_{IN} = 0V$, $V^-_{IN} = 0.3V$	17 **9**	14 **8**	13 **8**	mA (Min) mA (Min)
I_{SHORT}	Short Circuit Current	$V_{OUT} = 0V$, $V^+_{IN} = 3V$, $V^-_{IN} = 2V$	30 **40**	50 **60**	50 **60**	mA (Max) mA (Max)
		$V_{OUT} = 5V$, $V^+_{IN} = 2V$, $V^-_{IN} = 3V$	30 **32**	60 **80**	70 **90**	mA (Max) mA (Max)
COMPARATORS						
V_{OS}	Offset Voltage	$4V \le V^+ \le 36V$ (32V for LM613C), $R_L = 15$ kΩ	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{V_{CM}}$	Offset Voltage over V_{CM}	$0V \le V_{CM} \le 36V$ $V^+ = 36V$, (32V for LM613C)	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			µV/°C (Max)
I_B	Input Bias Current		5 **8**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
A_V	Voltage Gain	$R_L = 10$ kΩ to 36V (32V for LM613C) $2V \le V_{OUT} \le 27V$	500 **100**			V/mV V/mV
t_r	Large Signal Response Time	$V^+_{IN} = 1.4V$, V^-_{IN} = TTL Swing, $R_L = 5.1$ kΩ	1.5 **2.0**			µs µs
I_{SINK}	Output Sink Current	$V^+_{IN} = 0V$, $V^-_{IN} = 1V$, $V_{OUT} = 1.5V$	20 **13**	10 **8**	10 **8**	mA (Min) mA (Min)
		$V_{OUT} = 0.4V$	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA (Min) mA (Min)
I_{LEAK}	Output Leakage Current	$V^+_{IN} = 1V$, $V^-_{IN} = 0V$, $V_{OUT} = 36V$ (32V for LM613C)	0.1 **0.2**	10	10	µA (Max) µA (Max)

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over **Operating Temperature Range**. (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
VOLTAGE REFERENCE						
V_R	Voltage Reference	(Note 10)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V (Min) V (Max)
$\frac{\Delta V_R}{\Delta T}$	Average Temp. Drift	(Note 11)	**10**	**80**	**150**	ppm/°C (Max)
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 12)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV (Max) mV (Max)
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 13)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV (Max) mV (Max)
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}/9.9\ mA$ $\Delta V_{R(100 \rightarrow 17\ \mu A)}/83\ \mu A$	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω (Max) Ω (Max)
$\frac{V_R}{\Delta V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro = Vr)} - V_{R(Vro = 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV (Max) mV (Max)
$\frac{V_R}{\Delta V^+}$	V_R Change with V_{ANODE} Change	$V_{R(V^+ = 5V)} - V_{R(V^+ = 36V)}$ ($V^+ = 32V$ for LM613C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV (Max) mV (Max)
		$V_{R(V^+ = 5V)} - V_{R(V^+ = 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV (Max) mV (Max)
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \le V_{FB} \le 5.06V$	22 **29**	35 **40**	50 **55**	nA (Max) nA (Max)
e_n	V_R Noise	10 Hz to 10 kHz, $V_{RO} = V_R$	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Simultaneous short-circuit of multiple comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D\ \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 90°C/W for the N package, and 135°C/W for the WM package.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for $T_J = 25°C$; values in **bold face type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold type face)**.

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @ 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 10: V_R is the Cathode-to-feedback voltage, nominally 1.244V.

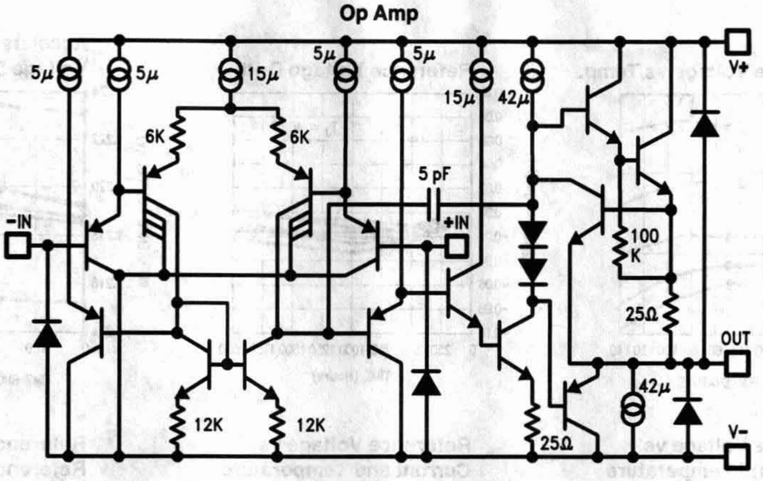
Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R/(V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 12: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

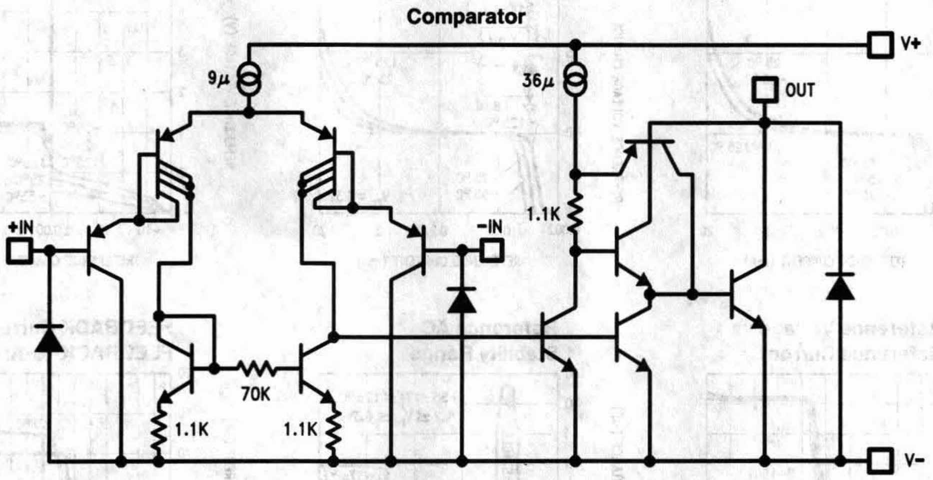
Note 13: Low contact resistance is required for accurate measurement.

Note 14: A military RETS 613AMX electrical test specification is available on request. The Military screened parts can also be procured as a Standard Military Drawing.

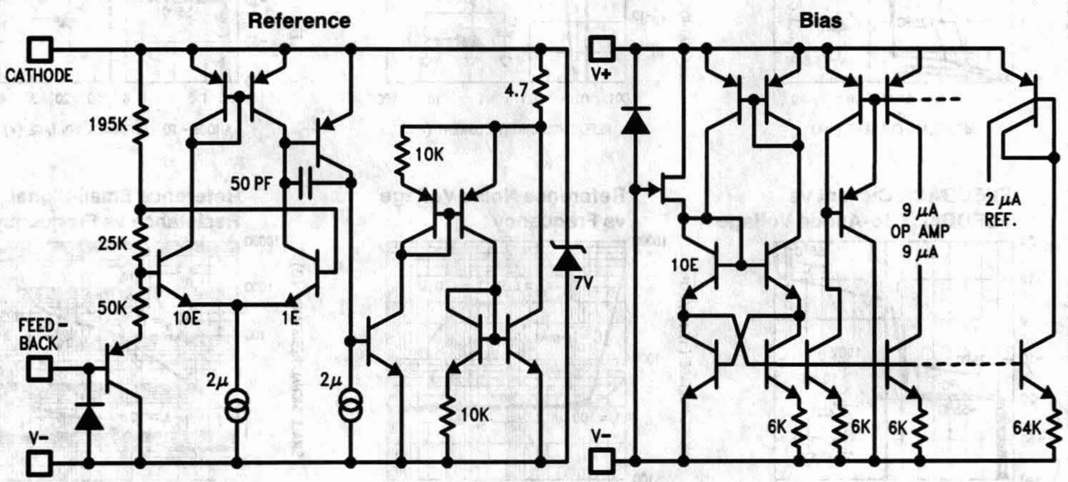
Simplified Schematic Diagrams


Op Amp
5μ
5μ
15μ
5μ
5μ
15μ
42μ
V+
6K
6K
5 pF
-IN
+IN
100
K
25Ω
OUT
42μ
12K
12K
25Ω
V-

TL/H/9226-2


Comparator
V+
9μ
36μ
OUT
1.1K
+IN
-IN
70K
1.1K
1.1K
V-

TL/H/9226-3

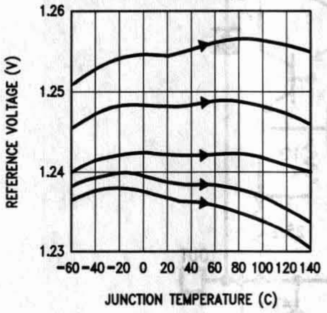

Reference
Bias
CATHODE
195K
4.7
50 PF
10K
25K
7V
50K
10E
1E
FEED-
BACK
2μ
2μ
10K
V-
V+
10E
9 μA
OP AMP
9 μA
2 μA
REF.
6K
6K
6K
64K
V-

TL/H/9226-4

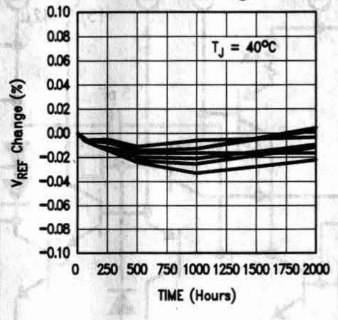
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

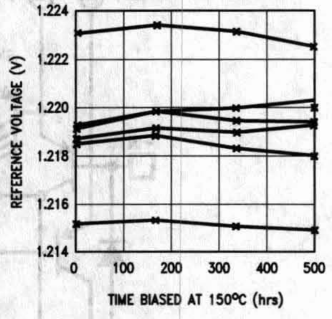
Reference Voltage vs Temp.



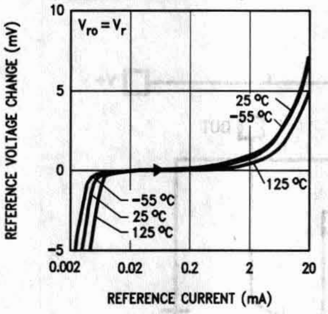
Reference Voltage Drift



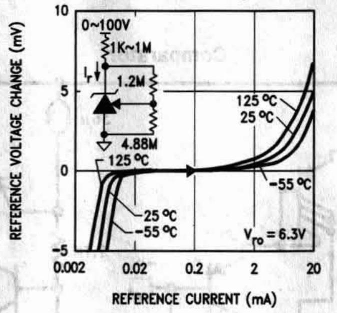
Accelerated Reference Voltage Drift vs Time



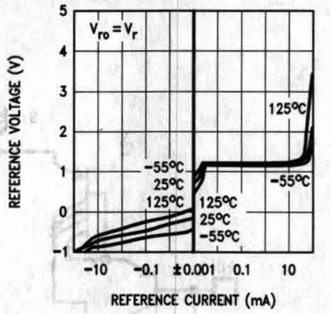
Reference Voltage vs Current and Temperature



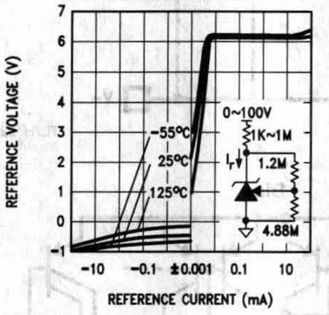
Reference Voltage vs Current and Temperature



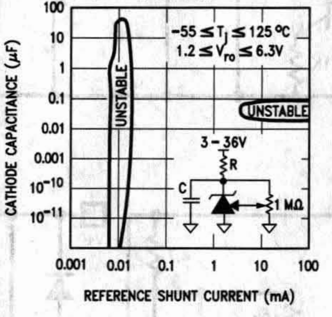
Reference Voltage vs Reference Current



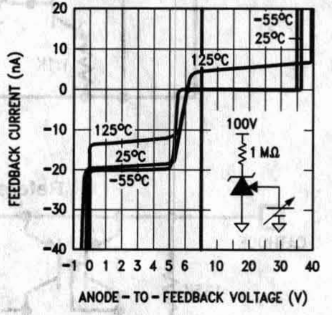
Reference Voltage vs Reference Current



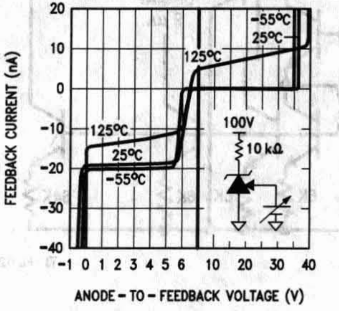
Reference AC Stability Range



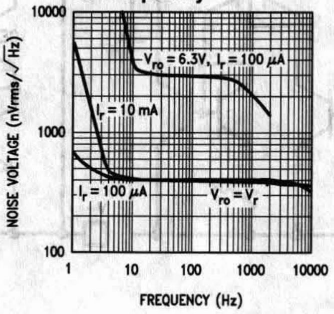
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



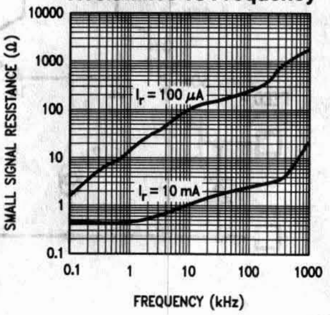
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency

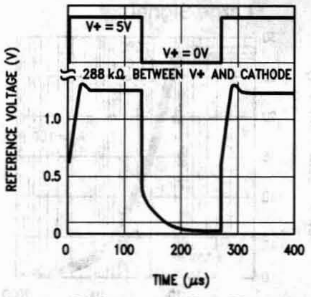


TL/H/9226–5

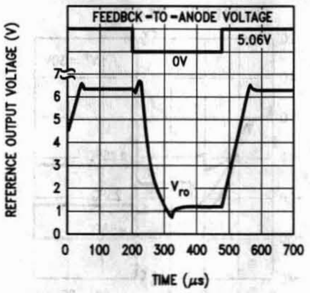
Typical Performance Characteristics (Reference) (Continued)

$T_J = 25°C$, FEEDBACK pin shorted to $V^- = 0V$, unless otherwise noted

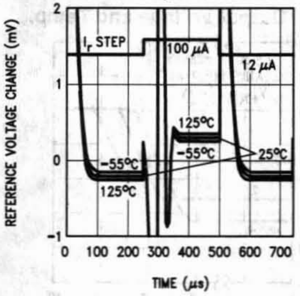
Reference Power-Up Time



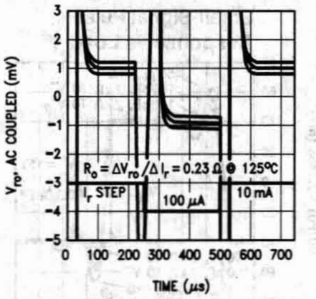
Reference Voltage with FEEDBACK Voltage Step



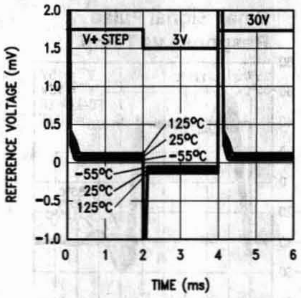
Reference Voltage with 100 ~ 12 µA Current Step



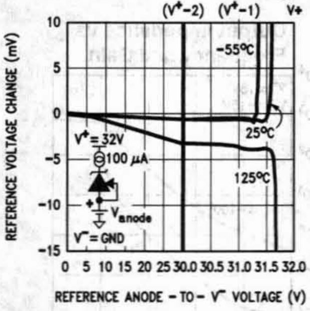
Reference Step Response for 100 µA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step



Reference Change vs Common-Mode Voltage

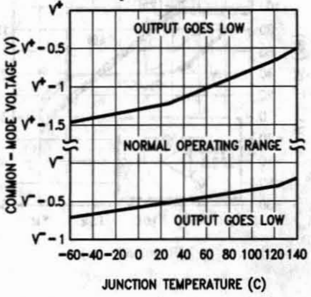


TL/H/9226-6

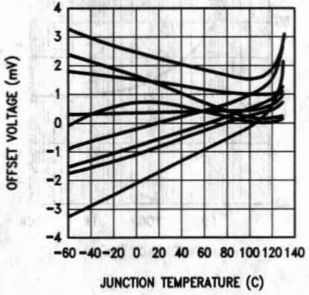
Typical Performance Characteristics (Op Amps)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

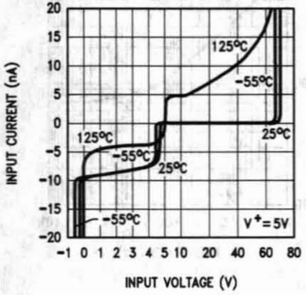
Input Common-Mode Voltage Range vs Temperature



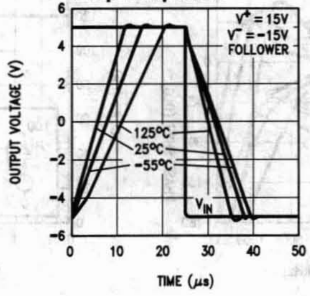
V_{OS} vs Junction Temperature



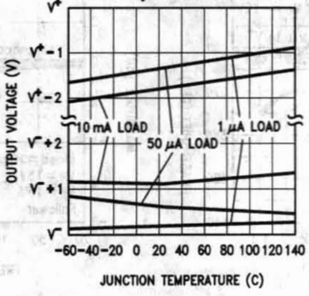
Input Bias Current vs Common-Mode Voltage



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

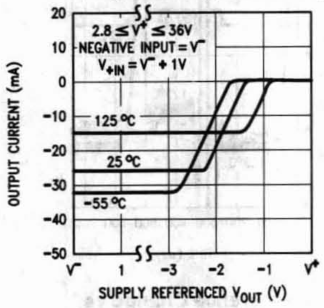


TL/H/9226-7

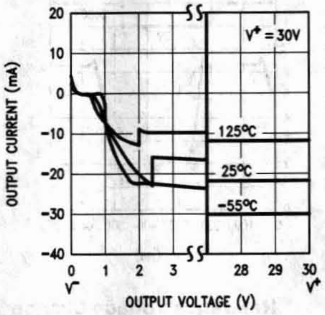
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

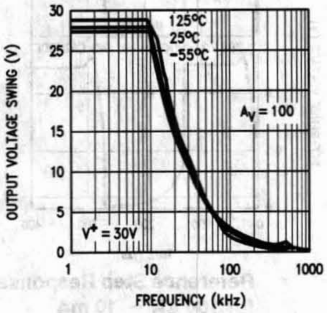
Output Source Current vs Output Voltage and Temp.



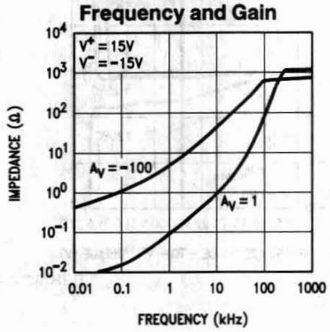
Output Sink Current vs Output Voltage



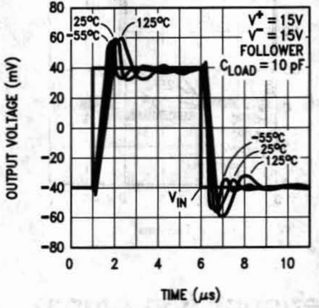
Output Swing, Large Signal



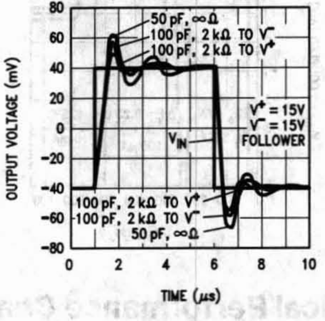
Output Impedance vs Frequency and Gain



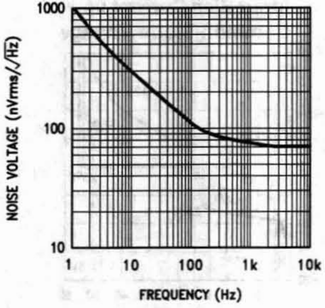
Small Signal Pulse Response vs Temp.



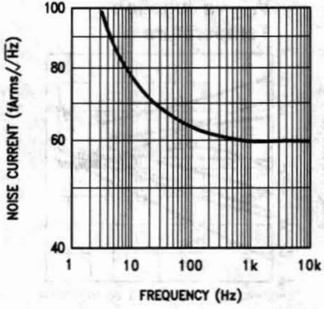
Small-Signal Pulse Response vs Load



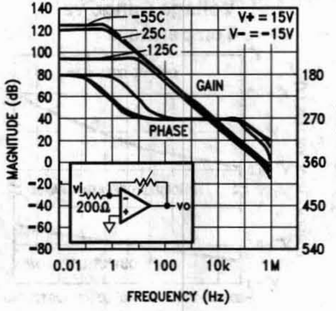
Op Amp Voltage Noise vs Frequency



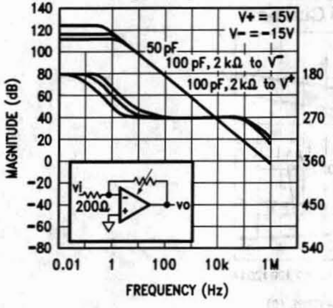
Op Amp Current Noise vs Frequency



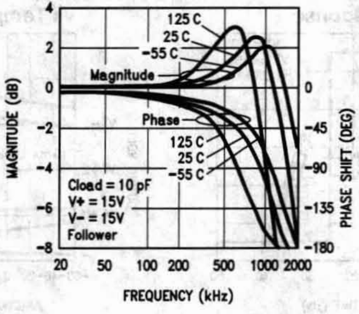
Small-Signal Voltage Gain vs Frequency and Temperature



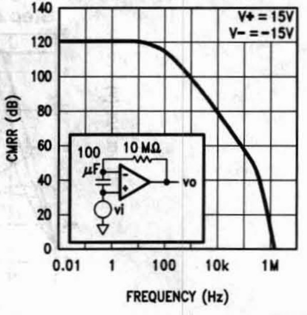
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

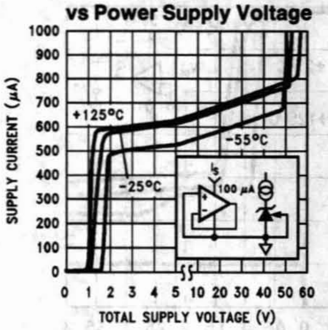


TL/H/9226–8

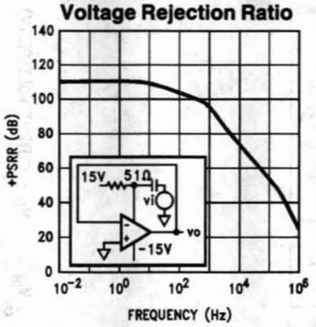
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

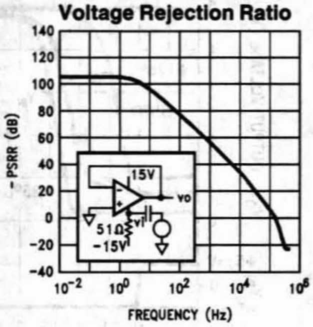
Power Supply Current vs Power Supply Voltage



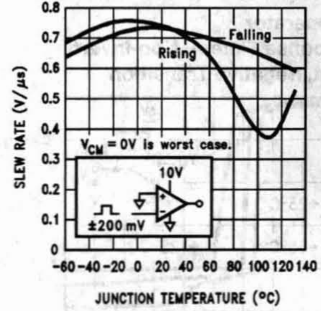
Positive Power Supply Voltage Rejection Ratio



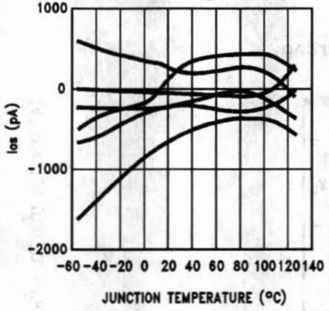
Negative Power Supply Voltage Rejection Ratio



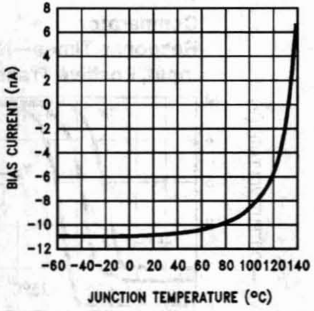
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature



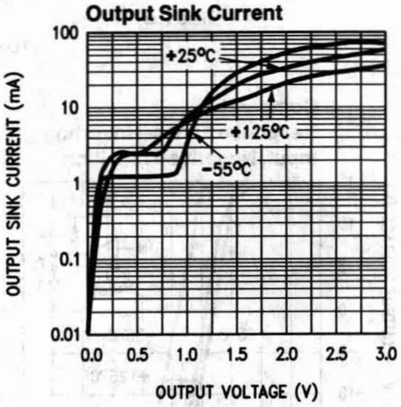
Input Bias Current vs Junction Temperature



TL/H/9226–9

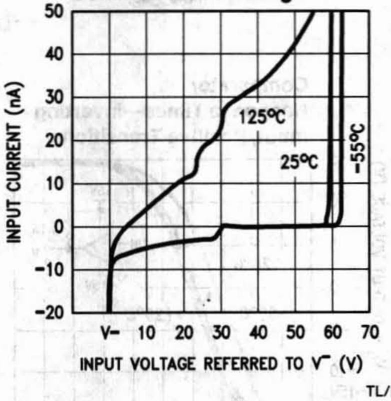
Typical Performance Characteristics (Comparators)

Output Sink Current



TL/H/9226–10

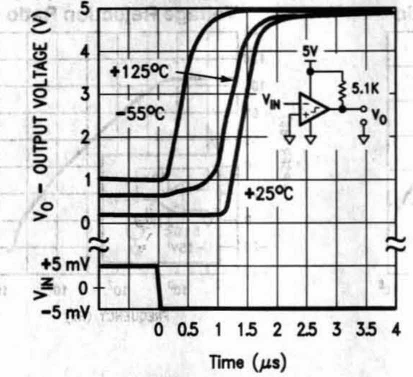
Input Bias Current vs Common-Mode Voltage



TL/H/9226–11

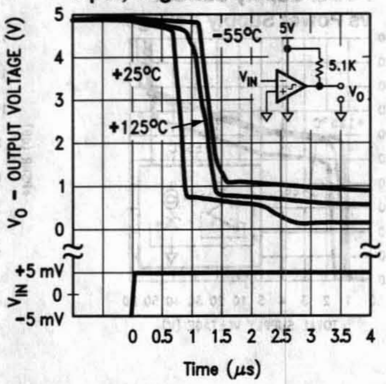
Typical Performance Characteristics (Comparators) (Continued)

Comparator Response Times—Inverting Input, Positive Transition



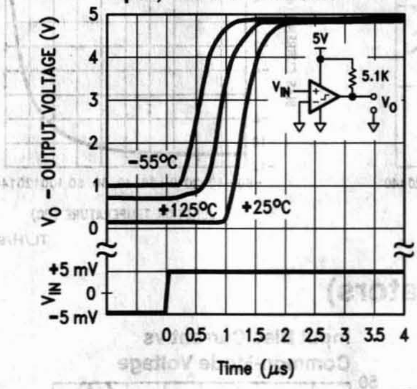
TL/H/9226–12

Comparator Response Times—Inverting Input, Negative Transition



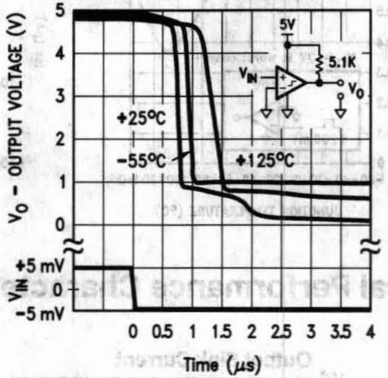
TL/H/9226–13

Comparator Response Times—Non-Inverting Input, Positive Transition



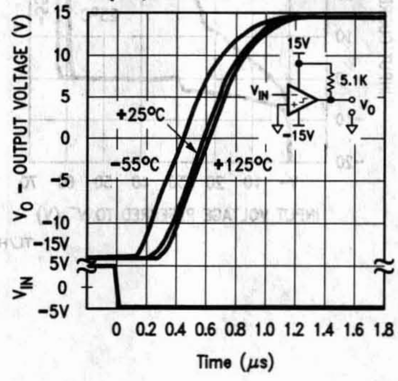
TL/H/9226–14

Comparator Response Times—Non-Inverting Input, Negative Transition



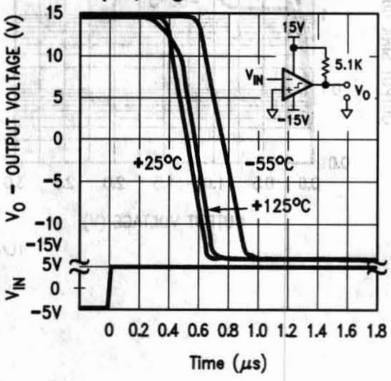
TL/H/9226–15

Comparator Response Times—Inverting Input, Positive Transition



TL/H/9226–16

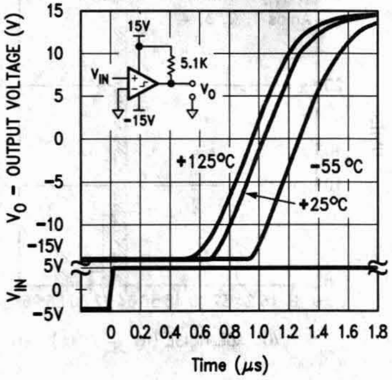
Comparator Response Times—Inverting Input, Negative Transition



TL/H/9226–17

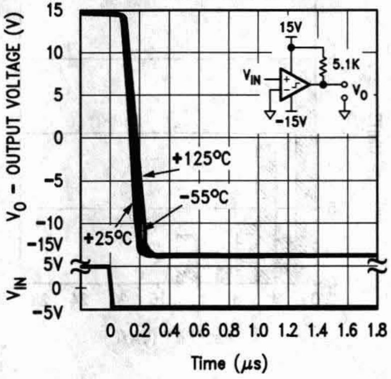
Typical Performance Characteristics (Comparators) (Continued)

Comparator Response Times—Non-Inverting Input, Positive Transition



TL/H/9226-18

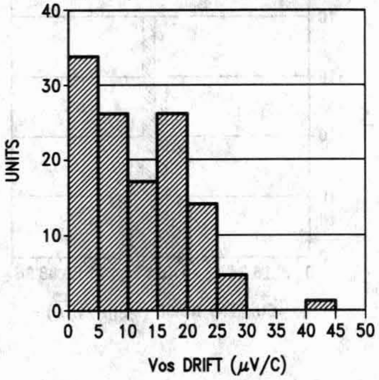
Comparator Response Times—Non-Inverting Input, Negative Transition



TL/H/9226-19

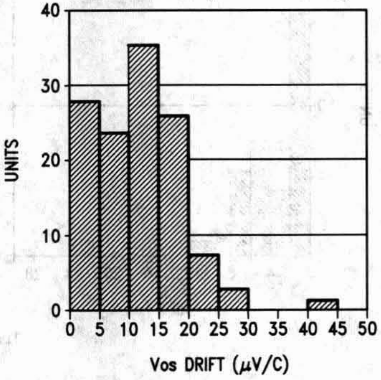
Typical Performance Distributions

Average V_{OS} Drift Military Temperature Range



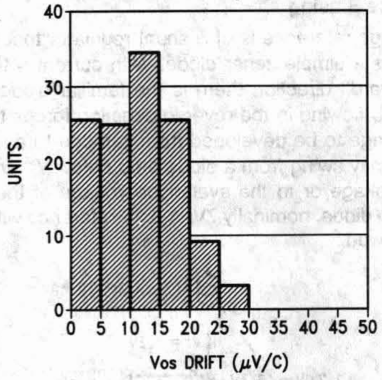
TL/H/9226-20

Average V_{OS} Drift Industrial Temperature Range



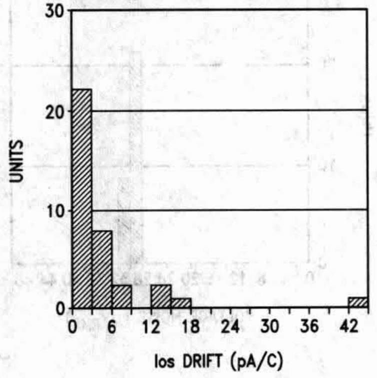
TL/H/9226-21

Average V_{OS} Drift Commercial Temperature Range



TL/H/9226-22

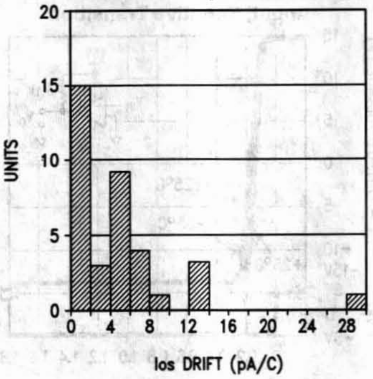
Average I_{OS} Drift Military Temperature Range



TL/H/9226-23

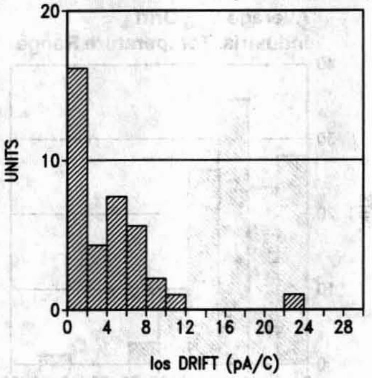
Typical Performance Distributions (Continued)

Average I_{OS} Drift Industrial Temperature Range



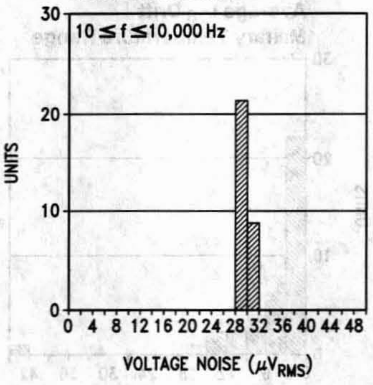
TL/H/9226-24

Average I_{OS} Drift Commercial Temperature Range



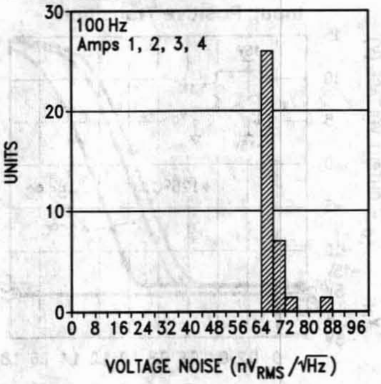
TL/H/9226-25

Voltage Reference Broad-Band Noise Distribution



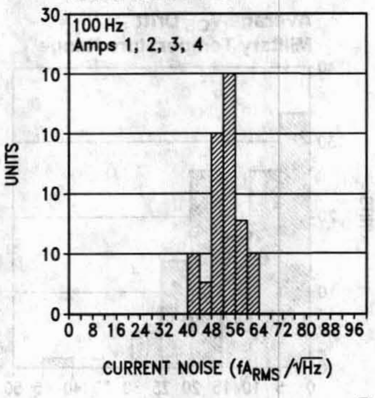
TL/H/9226-26

Op Amp Voltage Noise Distribution



TL/H/9226-27

Op Amp Current Noise Distribution



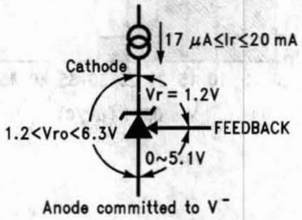
TL/H/9226-28

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.



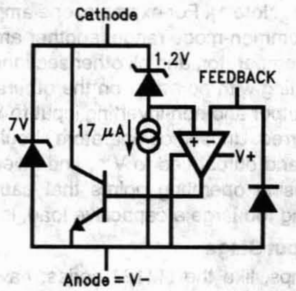
TL/H/9226-29

FIGURE 1. Voltage Associated with Reference (current source I_r is external)

Application Information (Continued)

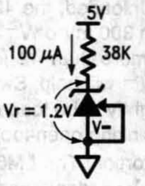
The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.



TL/H/9226-30

FIGURE 2. Reference Equivalent Circuit



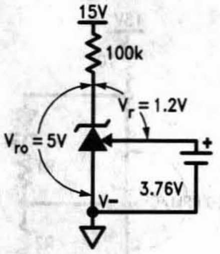
TL/H/9226-31

FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

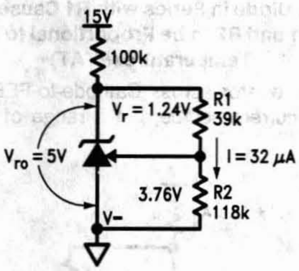
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constaint V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—$I \geq 32$ μA for the military grade over the military temperature range ($I \geq 5.5$ μA for a 1% untrimmed error for a commercial part).



TL/H/9226-32

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



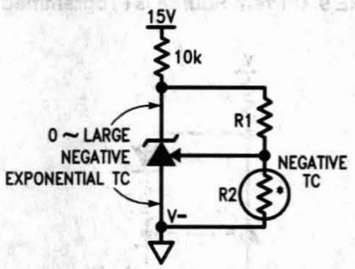
TL/H/9226-33

$R1 = Vr/I = 1.24/32\mu = 39k$

$R2 = R1\ \{(Vro/Vr) - 1\} = 39k\ \{(5/1.24) - 1)\} = 118k$

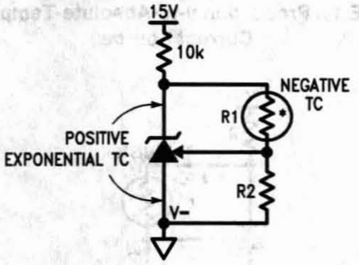
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



TL/H/9226-34

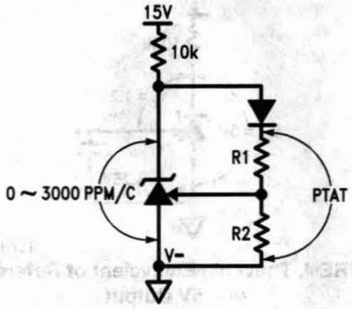
FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC



TL/H/9226-35

FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC

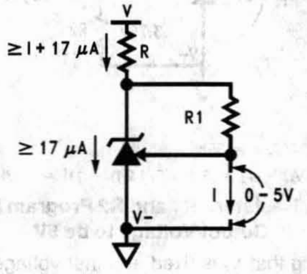
Application Information (Continued)



TL/H/9226–36

FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

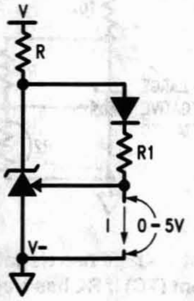
Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



TL/H/9226–37

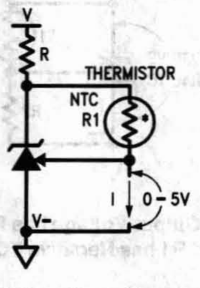
I = Vr/R1 = 1.24/R1

FIGURE 9. Current Source is Programmed by R1



TL/H/9226–38

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9226–39

FIGURE 11. Negative-TC Current Source

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS AND COMPARATORS

Any amp, comparator, or the reference may be biased in any way with no effect on the other sections of the LM613, except when a substrate diode conducts (see Electrical Characteristics Note 1). For example, one amp input may be outside the common-mode range, another amp may be operating as a comparator, and all other sections may have all terminals floating with no effect on the others. Tying inverting input to output and non-inverting input to V^- on unused amps is preferred. Unused comparators should have non-inverting input and output tied to V^+, and inverting input tied to V^-. Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like the LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.

2) Cross-Over Distortion: The LM613 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.

3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Comparator Output Stage

The comparators, like the LM139 series, have open-collector output stages. A pull-up resistor must be added from each output pin to a positive voltage for the output transistor to switch properly. When the output transistor is OFF, the output voltage will be this external positive voltage.

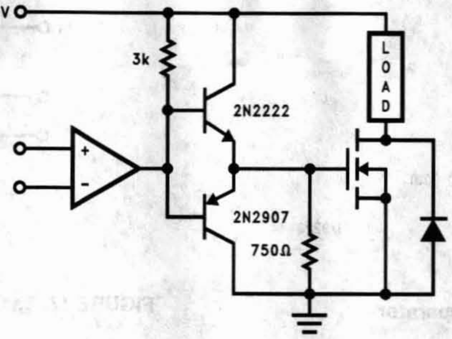
For the output voltage to be under the TTL-low voltage threshold when the output transistor is ON, the output current must be less than 8 mA (over temperature). This impacts the minimum value of pull-up resistor.

The offset voltage may increase when the output voltage is low and the output current is less than 30 μA. Thus, for best accuracy, the pull-up resistor value should be low enough to allow the output transistor to sink more than 30 μA.

Op Amp and Comparator Input Stage

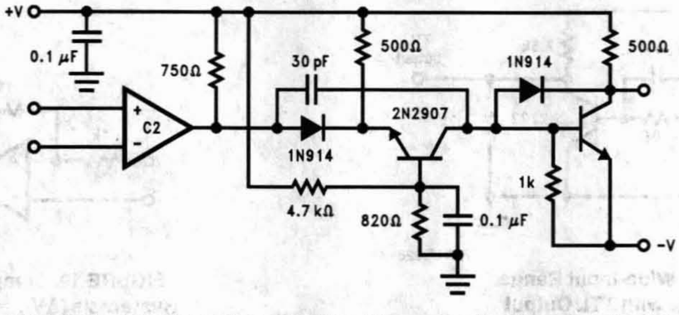
The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications


+V
3k
2N2222
2N2907
750Ω
LOAD
+
-

TL/H/9226-40

FIGURE 12. High Current, High Voltage Switch


+V
0.1 µF
750Ω
30 pF
500Ω
1N914
500Ω
C2
+
-
2N2907
1N914
4.7 kΩ
820Ω
0.1 µF
1k
-V

TL/H/9226-41

FIGURE 13. High Speed Level Shifter. Response time is approximately 1.5 µs, where output is either approximately +V or −V.

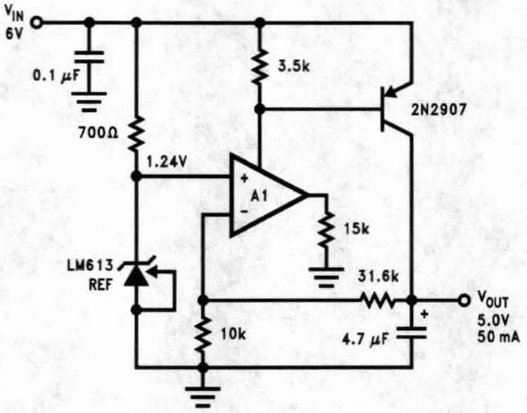

V_IN
6V
0.1 µF
3.5k
2N2907
700Ω
1.24V
A1
+
-
15k
LM613
REF
31.6k
V_OUT
5.0V
50 mA
10k
4.7 µF
+

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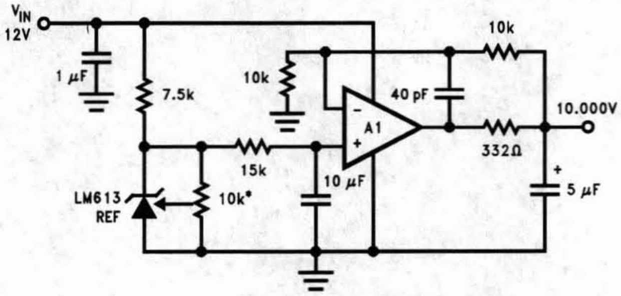
FIGURE 14. Low Voltage Regulator. Dropout voltage is approximately 0.2V.


V_IN
12V
1 µF
7.5k
10k
10k
40 pF
A1
-
+
10.000V
332Ω
15k
10 µF
+
5 µF
LM613
REF
10k*

*10k must be low
t.c. trimpot

TL/H/9226-43

FIGURE 15. Ultra Low Noise, 10.00V Reference. Total output noise is typically 14 μV_{RMS}.

Typical Applications (Continued)

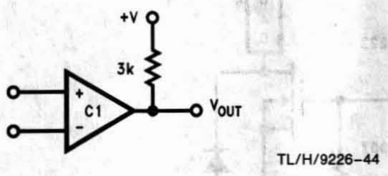

+V
3k
C1
VOUT
TL/H/9226-44

FIGURE 16. Basic Comparator

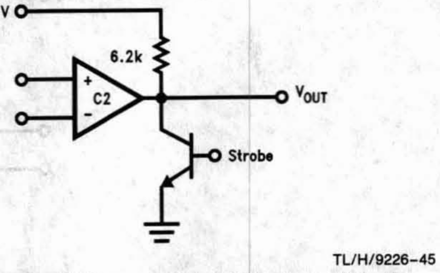

+V
6.2k
C2
VOUT
Strobe
TL/H/9226-45

FIGURE 17. Basic Comparator with External Strobe

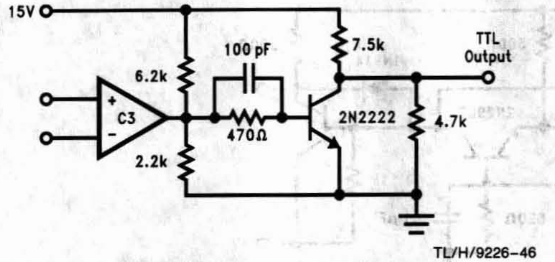

15V
6.2k
100 pF
7.5k
TTL Output
C3
470Ω
2N2222
4.7k
2.2k
TL/H/9226-46

FIGURE 18. Wide-Input Range Comparator with TTL Output

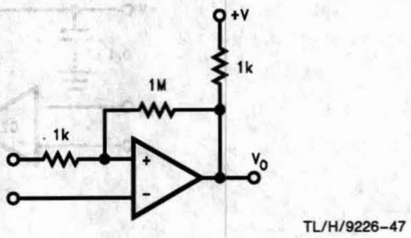

+V
1k
1M
1k
VO
TL/H/9226-47

FIGURE 19. Comparator with Hysteresis ($\Delta V_H = +V(1k/1M)$)

National Semiconductor

LM614 Quad Operational Amplifier and Adjustable Reference

General Description

The LM614 consists of four op-amps and a programmable voltage reference in a 16-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with four wide output swing op-amps makes the LM614 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's new Super-Block™ family, the LM614 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

Op Amp

- Low operating current 300 μA
- Wide supply voltage range 4V to 36V
- Wide common-mode range V^- to $(V^+ - 1.8V)$
- Wide differential input voltage ±36V
- Available in plastic package rated for Military Temperature Range Operation

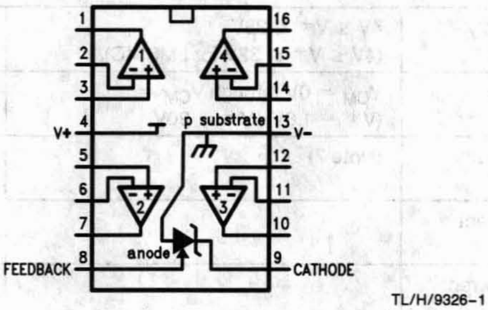
Reference

- Adjustable output voltage 1.2V to 6.3V
- Tight initial tolerance available ±0.6%
- Wide operating current range 17 μA to 20 mA
- Tolerant of load capacitance

Applications

- Transducer bridge driver and signal processing
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagram



TL/H/9326–1

Ordering Information

Reference Tolerance & V_{OS}	Temperature Range: Military $-55°C \le T_A \le +125°C$	Industrial $-40°C \le T_A \le +85°C$	Commercial $0°C \le T_A \le +70°C$	Package	NSC Drawing
±0.6%@ 80 ppm/°C max $V_{OS} \le 3.5$ mV max	LM614AMN	LM614AIN	—	16-pin Molded DIP	N16E
	LM614AMJ/883 (Note 13)	—	—	16-pin Ceramic DIP	J16A
±2.0%@ 150 ppm/°C max $V_{OS} \le 5.0$ mV	LM614MN	LM614BIN	LM614CN	16-pin Molded DIP	N16E
	—	LM614WM	LM614CWM	16-pin Wide Surface Mount	M16B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pins except V_R (referred to V^- pin)	
(Note 2)	36V (Max)
(Note 3)	−0.3V (Min)
Current through Any Input Pin & V_R Pin	±20 mA
Differential Input Voltage	
Military and Industrial	±36V
Commercial	±32V
Storage Temperature Range	$-65°C \leq T_J \leq +150°C$
Maximum Junction Temperature	150°C
Thermal Resistance, Junction-to-Ambient (Note 4)	
N Package	100°C
WM Package	150°C
Soldering Information (Soldering, 10 seconds)	
N Package	260°C
WM Package	220°C
ESD Tolerance (Note 5)	±1kV

Operating Temperature Range

LM614AI, LM614I, LM614BI	$-40°C \leq T_J \leq +85°C$
LM614AM, LM614M	$-55°C \leq T_J \leq +125°C$
LM614C	$0°C \leq T_J \leq +70°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 6)	LM614AM LM614AI Limits (Note 7)	LM614M LM614BI LM614I LM614C Limits (Note 7)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \leq V^+ \leq 36V$ (32V for LM614C)	450 **550**	940 **1000**	1000 **1070**	μA max μA max
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	2.8 **3**	V min V min
			46 **43**	36 **36**	32 **32**	V max V max
OPERATIONAL AMPLIFIER						
V_{OS1}	V_{OS} Over Supply	$4V \leq V^+ \leq 36V$ ($4V \leq V^+ \leq 32V$ for LM614C)	1.5 **2.0**	3.5 **6.0**	5.0 **7.0**	mV max mV max
V_{OS2}	V_{OS} Over V_{CM}	$V_{CM} = 0V$ through $V_{CM} =$ $(V^+ - 1.8V)$, $V^+ = 30V$	1.0 **1.5**	3.5 **6.0**	5.0 **7.0**	mV max mV max
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 7)	**15**			μV/°C max
I_B	Input Bias Current		10 **11**	25 **30**	35 **40**	nA max nA max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA max nA max
$\frac{I_{OS1}}{\Delta T}$	Average Offset Drift Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1800			MΩ
		Common-Mode	3800			MΩ
C_{IN}	Input Capacitance	Common-Mode Input	5.7			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection Ratio	$V^+ = 30V$, $0V \leq V_{CM} \leq (V^+ - 1.8V)$, $CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	95 **90**	80 **75**	75 **70**	dB min dB min
PSRR	Power Supply Rejection Ratio	$4V \leq V^+ \leq 30V$, $V_{CM} = V^+/2$, $PSRR = 20 \log (\Delta V^+/\Delta V_{OS})$	110 **100**	80 **75**	75 **70**	dB min dB min
A_V	Open Loop Voltage Gain	$R_L = 10\ k\Omega$ to GND, $V^+ = 30V$, $5V \leq V_{OUT} \leq 25V$	500 **50**	100 **40**	94 **40**	V/mV min

Electrical Characteristics (Continued)

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 6)	LM614AM LM614AI Limits (Note 8)	LM614M LM614BI LM614I LM614C Limits (Note 8)	Units
SR	Slew Rate	$V^+ = 30V$ (Note 8)	±0.70 **±0.65**	±0.55 **±0.45**	±0.50 **±0.45**	V/µs
GBW	Gain Bandwidth	$C_L = 50$ pF	0.8 **0.52**			MHz MHz
V_{O1}	Output Voltage Swing High	$R_L = 10\ k\Omega$ to GND $V^+ = 36V$ (32V for LM614C)	$V^+ - 1.4$ **$V^+ - 1.6$**	$V^+ - 1.7$ **$V^+ - 1.9$**	$V^+ - 1.8$ **$V^+ - 1.9$**	V min V min
V_{O2}	Output Voltage Swing Low	$R_L = 10\ k\Omega$ to V^+ $V^+ = 36V$ (32V for LM614C)	$V^- + 0.8$ **$V^- + 0.9$**	$V^- + 0.9$ **$V^- + 1.0$**	$V^- + 0.95$ **$V^- + 1.0$**	V max V max
I_{OUT}	Output Source	$V_{OUT} = 2.5V$, $V_{+IN} = 0V$, $V_{-IN} = -0.3V$	25 **15**	20 **13**	16 **13**	mA min mA min
I_{SINK}	Output Sink Current	$V_{OUT} = 1.6V$, $V_{+IN} = 0V$, $V_{-IN} = 0.3V$	17 **9**	14 **8**	13 **8**	mA min mA min
I_{SHORT}	Short Circuit Current	$V_{OUT} = 0V$, $V_{+IN} = 3V$, $V_{-IN} = 2V$, Source	30 **40**	50 **60**	50 **60**	mA max mA max
		$V_{OUT} = 5V$, $V_{+IN} = 2V$, $V_{-IN} = 3V$, Sink	30 **32**	60 **80**	70 **90**	mA max mA max
VOLTAGE REFERENCE						
V_R	Voltage Reference	(Note 9)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2.0%)	V min V max
$\frac{\Delta V_R}{\Delta T}$	Average Temperature Drift	(Note 10)	**10**	**80**	**150**	PPM/°C max
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 11)	**3.2**			µV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV max mV max
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 12)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV max mV max
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}/9.9$ mA $\Delta V_{R(100 \rightarrow 17\ \mu A)}/83\ \mu A$	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω max Ω max
$\frac{\Delta V_R}{\Delta V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro = Vr)} - V_{R(Vro = 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV max mV max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R(V^+ = 5V)} - V_{R(V^+ = 36V)}$ ($V^+ = 32V$ for LM614C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV max mV max
		$V_{R(V^+ = 5V)} - V_{R(V^+ = 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV max mV max
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \le V_{FB} \le 5.06V$	22 **29**	35 **40**	50 **55**	nA max nA max
e_n	Voltage Noise	BW = 10 Hz to 10 kHz, $V_{RO} = V_R$	30			μV_{RMS}

Electrical Characteristics (Continued)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V+ is allowed.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V−, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Junction temperature may be calculated using $T_J = T_A + P_D\theta_{jA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{jA} are 90°C/W for the N package, WM package.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 7: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 8: Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 9: V_R is the Cathode-feedback voltage, nominally 1.244V.

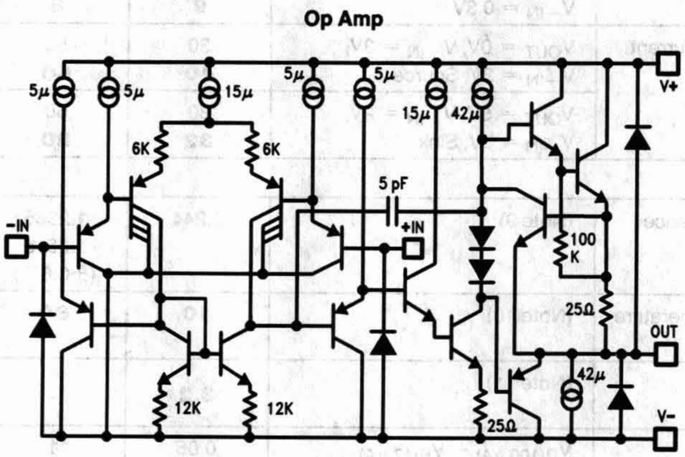
Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R/(V_{R[25^\circ C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25^\circ C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 11: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, cycle its junction temperature in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

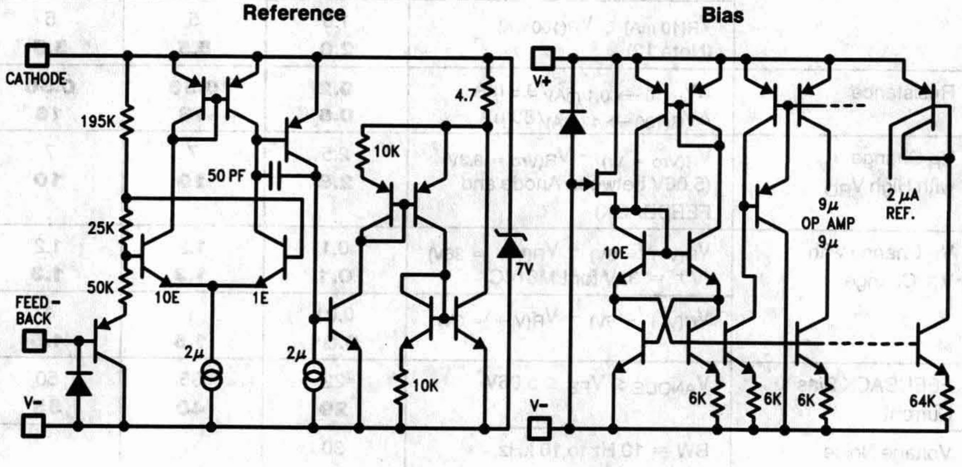
Note 12: Low contact resistance is required for accurate measurement.

Note 13: A military RETSLM614AMX electrical test specification is available on request. The LM614AMJ/883 can also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams



TL/H/9326-2

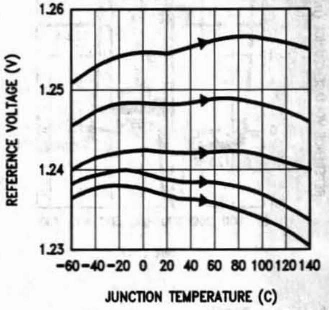


TL/H/9326-3

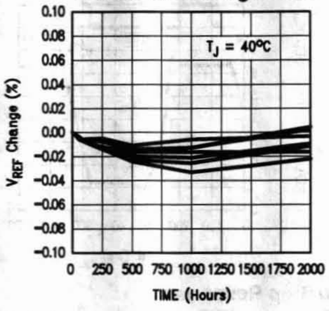
Typical Performance Characteristics (Reference)

$T_J = 25°C$, FEEDBACK pin shorted to $V^- = 0V$, unless otherwise noted

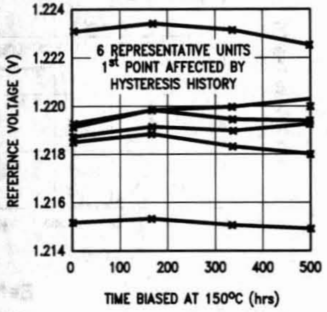
Reference Voltage vs Temperature on 5 Representative Units



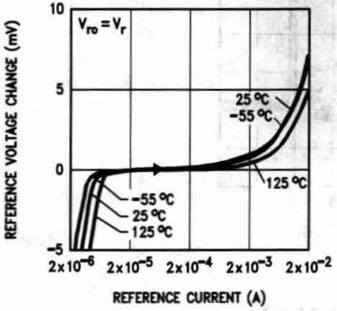
Reference Voltage Drift



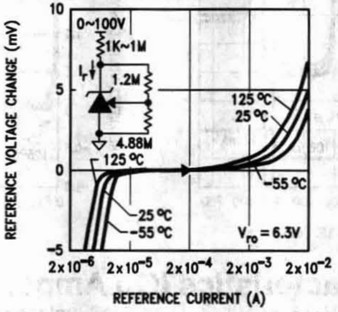
Accelerated Reference Voltage Drift vs Time



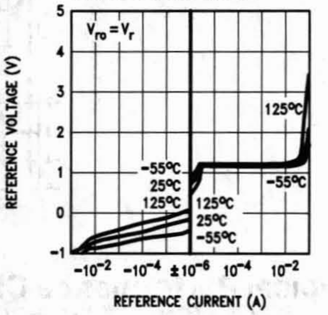
Reference Voltage vs Current and Temperature



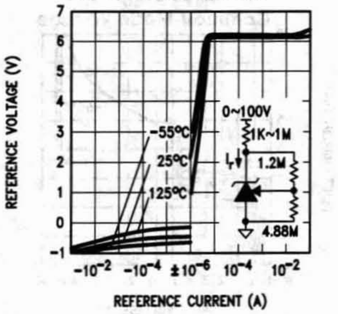
Reference Voltage vs Current and Temperature



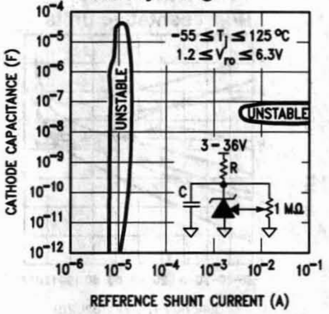
Reference Voltage vs Reference Current



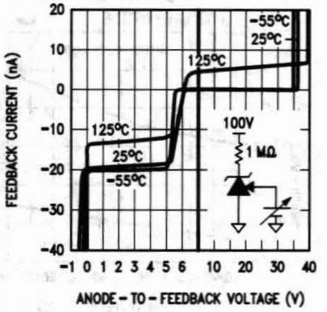
Reference Voltage vs Reference Current



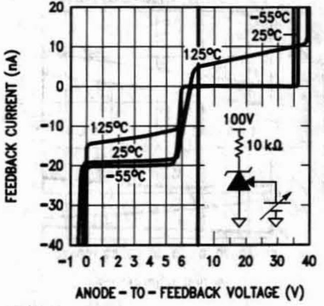
Reference AC Stability Range



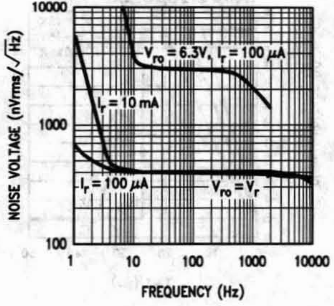
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



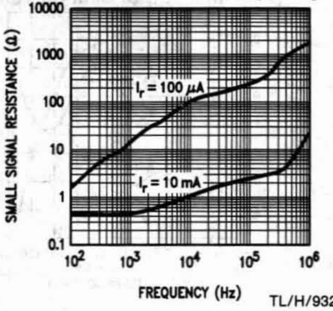
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency

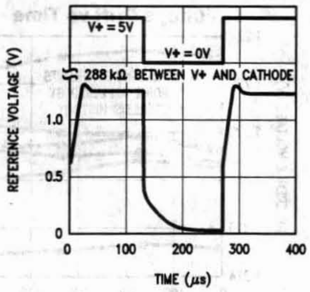


TL/H/9326–4

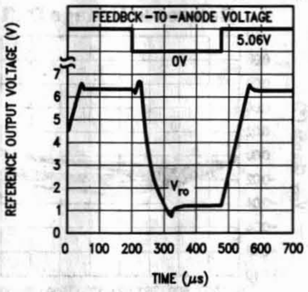
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

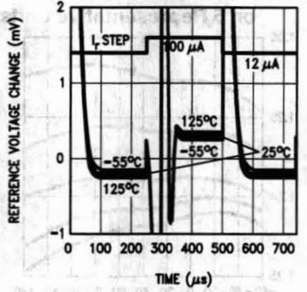
Reference Power-Up Time



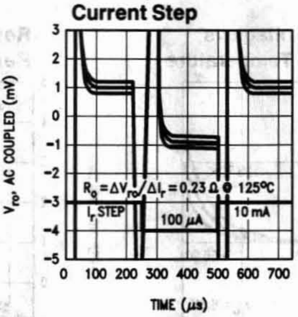
Reference Voltage with FEEDBACK Voltage Step



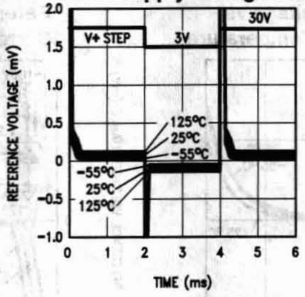
Reference Voltage with 100 ~ 12 µA Current Step



Reference Step Response for 100 µA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step

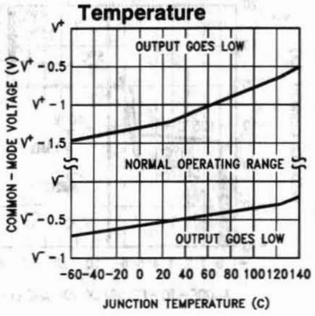


TL/H/9326–8

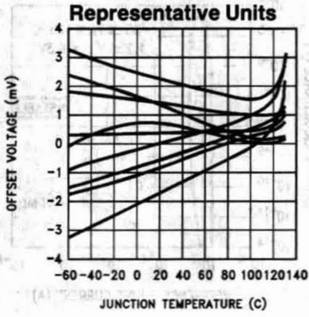
Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = 0V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, T_J = 25°C, unless otherwise noted

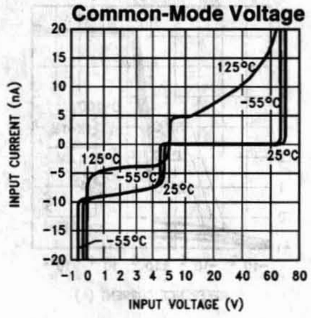
Input Common-Mode Voltage Range vs Temperature



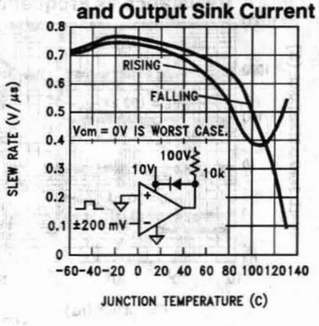
V_{OS} vs Junction Temperature on 9 Representative Units



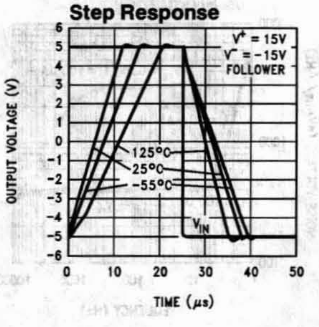
Input Bias Current vs Common-Mode Voltage



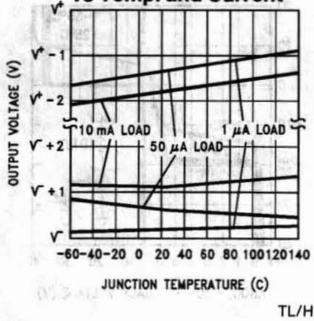
Slew Rate vs Temperature and Output Sink Current



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

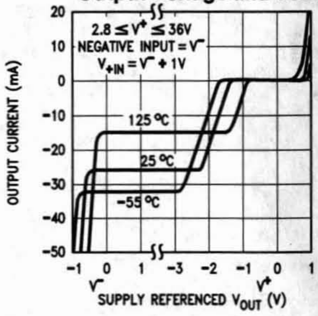


TL/H/9326–5

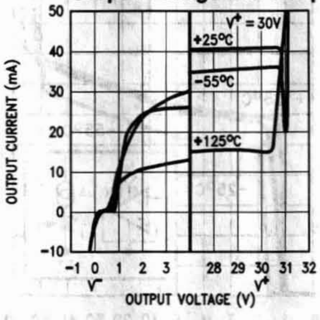
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

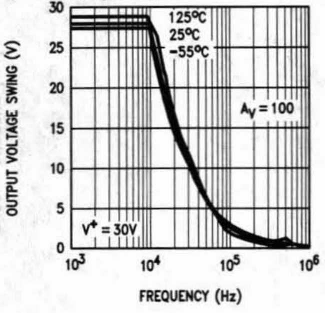
Output Source Current vs Output Voltage and Temp.



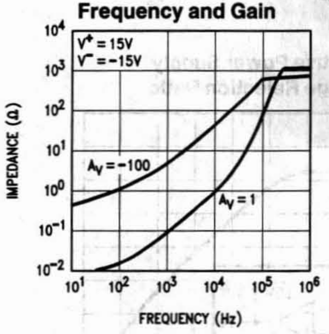
Output Sink Current vs Output Voltage and Temp.



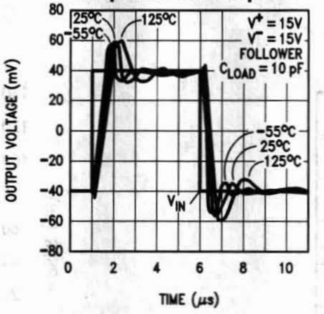
Output Swing, Large Signal



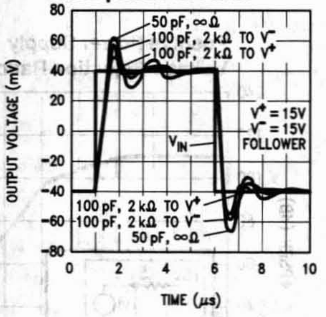
Output Impedance vs Frequency and Gain



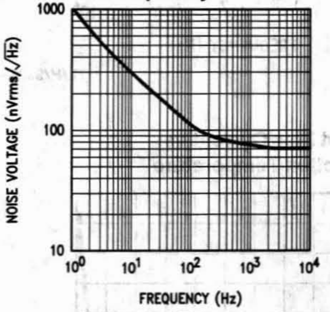
Small-Signal Pulse Response vs Temp.



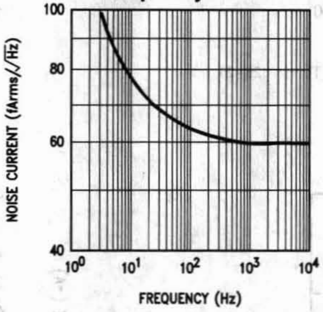
Small-Signal Pulse Response vs Load



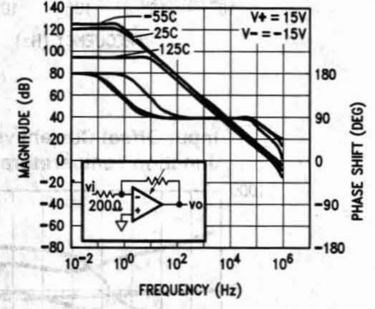
Op Amp Voltage Noise vs Frequency



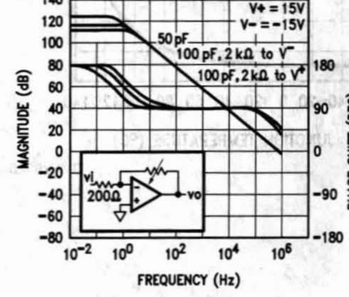
Op Amp Current Noise vs Frequency



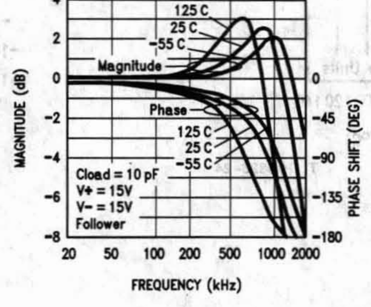
Small-Signal Voltage Gain vs Frequency and Temperature



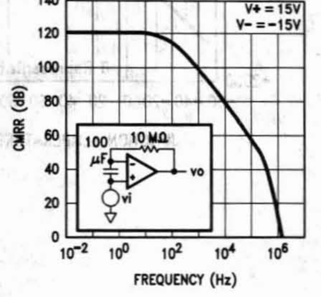
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

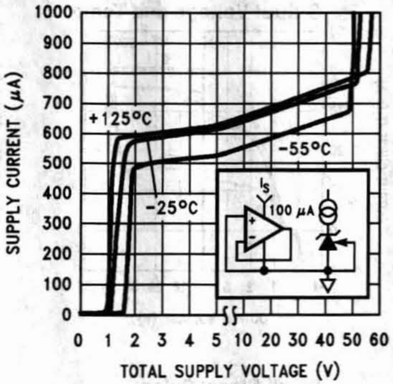


TL/H/9326-6

Typical Performance Characteristics (Op Amps) (Continued)

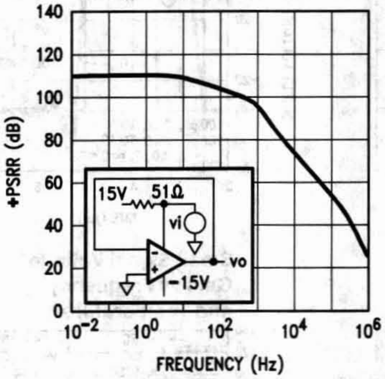
$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

Power Supply Current vs Power Supply Voltage



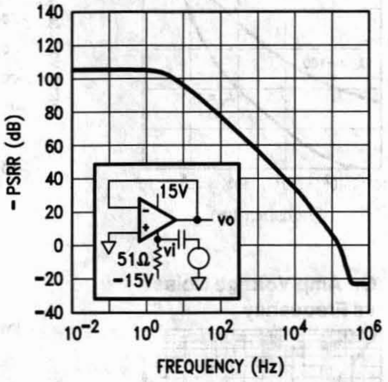
TL/H/9326–7

Positive Power Supply Voltage Rejection Ratio



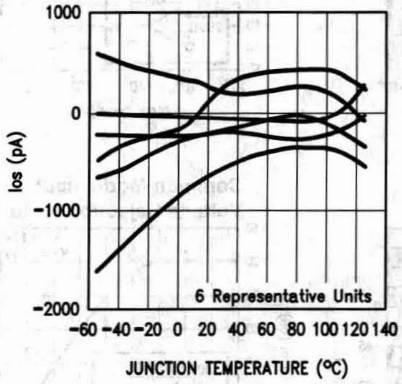
TL/H/9326–21

Negative Power Supply Voltage Rejection Ratio



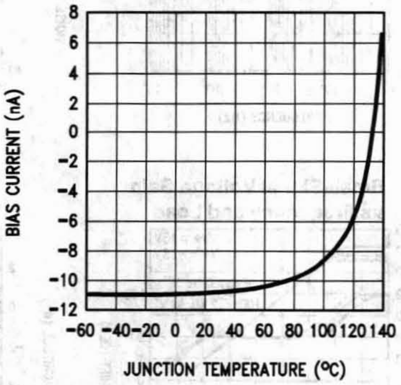
TL/H/9326–22

Input Offset Current vs Junction Temperature



TL/H/9326–24

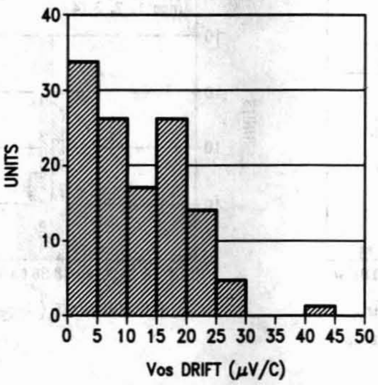
Input Bias Current vs Junction Temperature



TL/H/9326–38

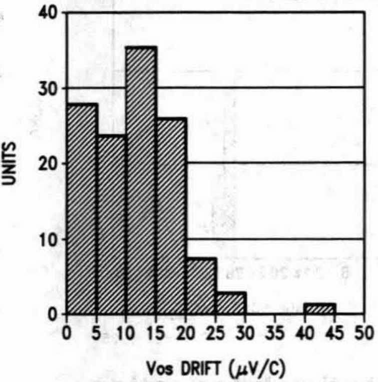
Typical Performance Distributions

Average V_{OS} Drift Military Temperature Range



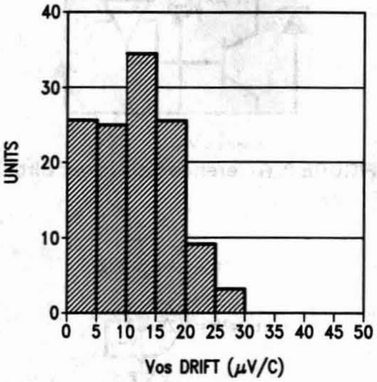
TL/H/9326–29

Average V_{OS} Drift Industrial Temperature Range



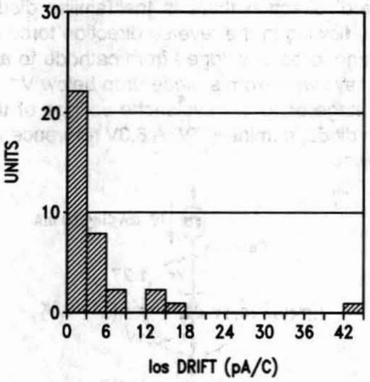
TL/H/9326–30

Average V_{OS} Drift Commercial Temperature Range



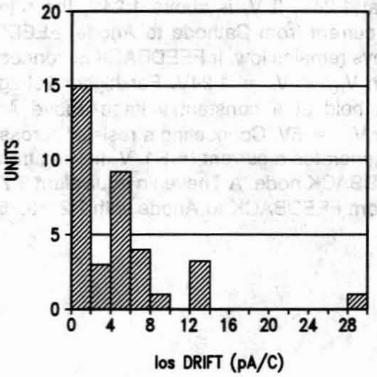
TL/H/9326–31

Average I_{OS} Drift Military Temperature Range



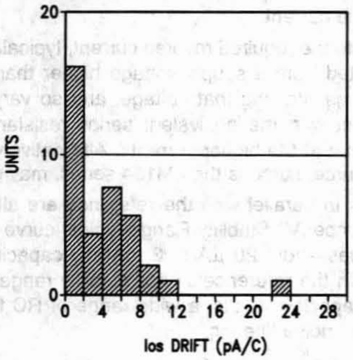
TL/H/9326–32

Average I_{OS} Drift Industrial Temperature Range



TL/H/9326–33

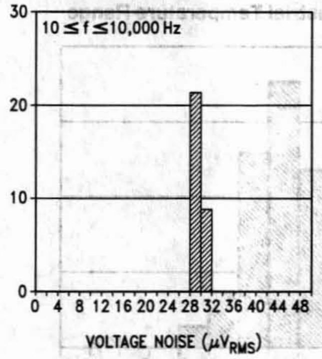
Average I_{OS} Drift Commercial Temperature Range



TL/H/9326–34

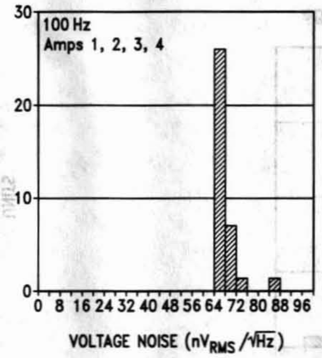
Typical Performance Distributions (Continued)

Voltage Reference Broad-Band Noise Distribution



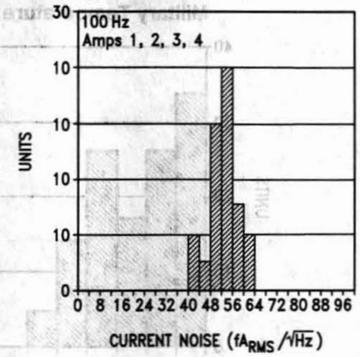
TL/H/9326-35

Op Amp Voltage Noise Distribution



TL/H/9326-36

Op Amp Current Noise Distribution



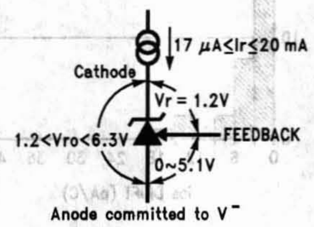
TL/H/9326-37

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.



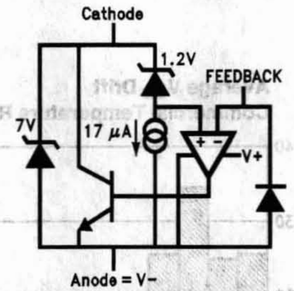
TL/H/9326-9

FIGURE 1. Voltages Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

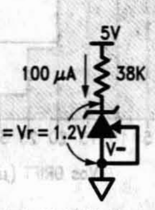
To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 µA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.



TL/H/9326-10

FIGURE 2. Reference Equivalent Circuit



TL/H/9326-11

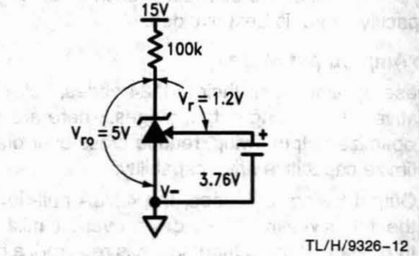
FIGURE 3. 1.2V Reference

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constaint V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I

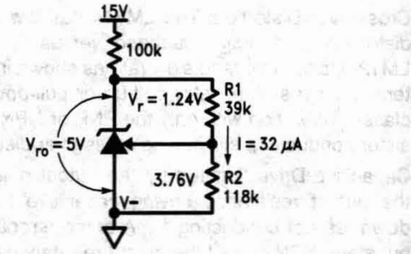
Application Information (Continued)

greater than one thousand times larger than FEEDBACK bias current for $<0.1\%$ error—$I \geq 32\ \mu A$ for the military grade over the military temperature range ($I \geq 5.5\ \mu A$ for a 1% untrimmed error for a commercial part.)


15V
100k
$V_r = 1.2V$
$V_{ro} = 5V$
+
3.76V
V−

TL/H/9326-12

FIGURE 4. Thevenin Equivalent of Reference with 5V Output


15V
100k
$V_r = 1.24V$
R1
39k
$V_{ro} = 5V$
$I = 32\ \mu A$
3.76V
R2
118k
V−

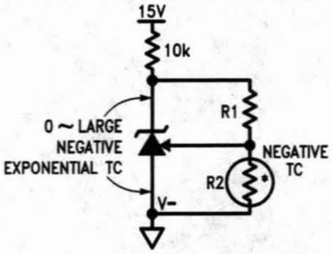
TL/H/9326-13

$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1\ \{(Vro/Vr) - 1\} = 39k\ \{(5/1.24) - 1)\} = 118k$$

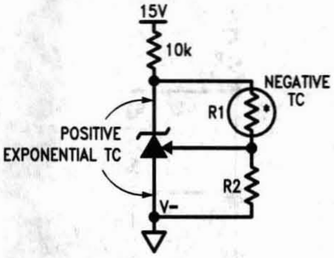
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.


15V
10k
R1
0 ~ LARGE
NEGATIVE
EXPONENTIAL TC
NEGATIVE
TC
R2
V−

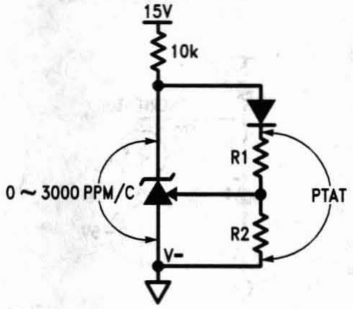
TL/H/9326-14

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC


15V
10k
NEGATIVE
TC
R1
POSITIVE
EXPONENTIAL TC
R2
V−

TL/H/9326-15

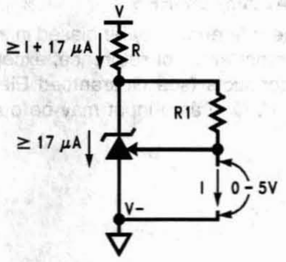
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC


15V
10k
R1
0 ~ 3000 PPM/C
PTAT
R2
V−

TL/H/9326-16

FIGURE 8. Diode in Series with R1 Causes Voltage across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.

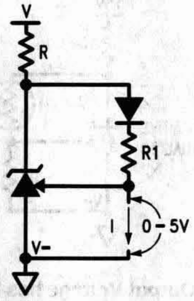

V
$\geq I + 17\ \mu A$
R
R1
$\geq 17\ \mu A$
I
0 − 5V
V−

TL/H/9326-17

$$I = Vr/R1 = 1.24/R1$$

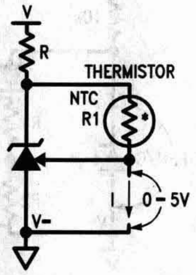
FIGURE 9. Current Source is Programmed by R1

Application Information (Continued)



TL/H/9326–18

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9326–19

FIGURE 11. Negative-TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS

Any amp or the reference may be biased in any way with no effect on the other amps or reference, except when a substrate diode conducts (see Guaranteed Electrical Characteristics Note 1). One amp input may be outside the common-mode range, another amp may be operated as a comparator, another with all terminals floating with no effect on the others (tying inverting input to output and non-inverting input to V^- on unused amps is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like their LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain

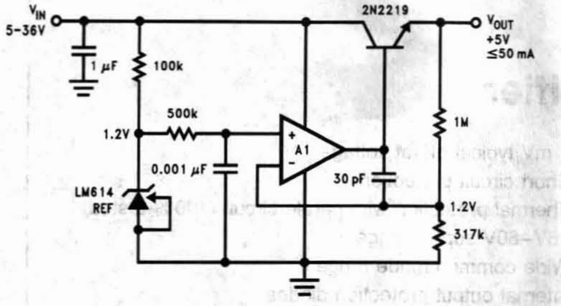
2) Cross-over Distortion: The LM614 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion

3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Op Amp Input Stage

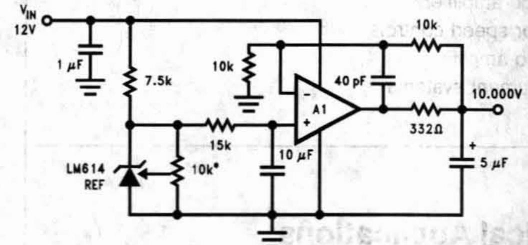
The lateral PNP input transistors, unlike most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications


V_IN
5–36V
1 µF
100k
Q1
2N2219
V_OUT
+5V
≤50 mA
500k
1.2V
0.001 µF
A1
30 pF
1M
1.2V
317k
LM614
REF

TL/H/9326–42

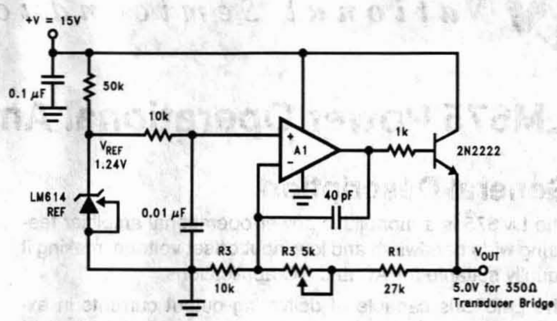
FIGURE 12. Simple Low Quiescent Drain Voltage Regulator. Total supply current approximately 320 μA, when $V_{IN} = +5V$.


V_IN
12V
1 µF
7.5k
10k
10k
40 pF
A1
10.000V
332Ω
15k
10 µF
5 µF
LM614
REF
10k*

TL/H/9326–43

*10k must be low t.c. trimpot.

FIGURE 13. Ultra Low Noise 10.00V Reference. Total output noise is typically 14 μV_{RMS}.


+V = 15V
0.1 µF
50k
10k
V_REF
1.24V
A1
1k
2N2222
40 pF
LM614
REF
0.01 µF
R3
10k
R3 5k
R1
27k
V_OUT
5.0V for 350Ω
Transducer Bridge

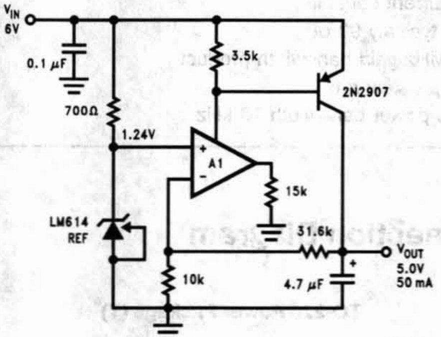
$V_{OUT} = (R_1/P_\beta + 1)\ V_{REF}$

R_1, R_2 should be 1% metal film

P_β should be low T.C. trim pot

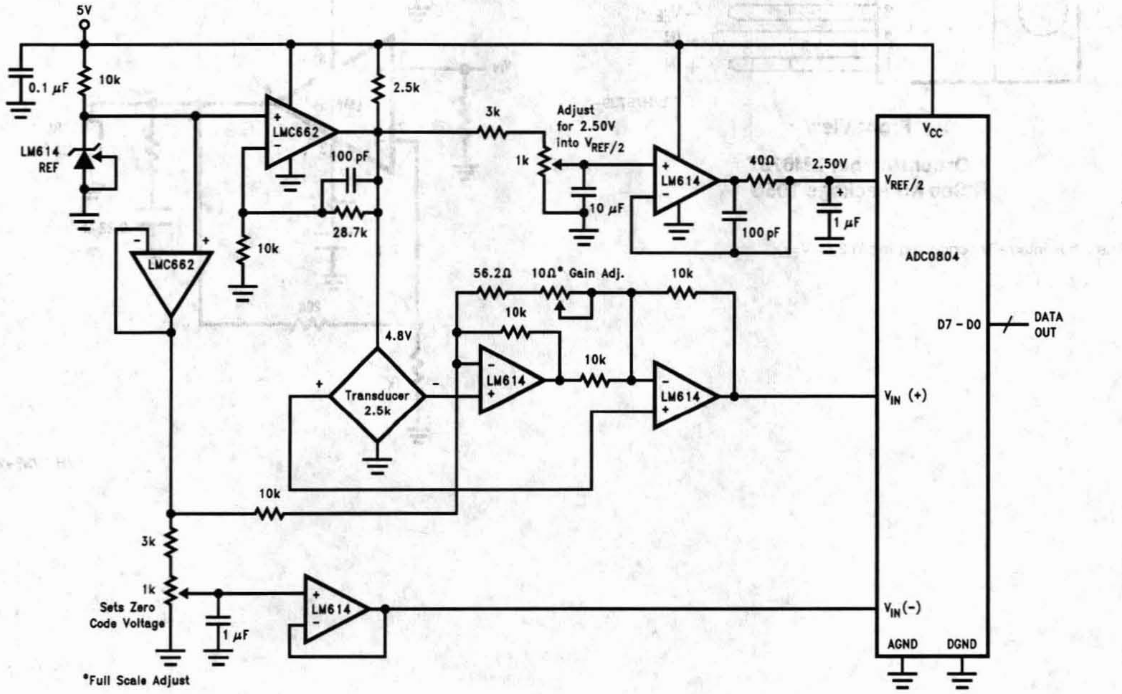
TL/H/9326–44

FIGURE 14. Slow Rise Time Upon Power-Up, Adjustable Transducer Bridge Driver. Rise time is approximately 1 ms.


V_IN
6V
0.1 µF
3.5k
2N2907
700Ω
1.24V
A1
15k
LM614
REF
31.6k
V_OUT
5.0V
50 mA
10k
4.7 µF

TL/H/9326–46

FIGURE 16. Low Drop-Out Voltage Regulator Circuit, drop-out voltage is typically 0.2V.


5V
0.1 µF
10k
LM614
REF
LMC662
2.5k
3k
Adjust
for 2.50V
into V_REF/2
1k
100 pF
28.7k
10k
10 µF
LM614
40Ω
2.50V
100 pF
1 µF
V_CC
V_REF/2
ADC0804
LMC662
56.2Ω
10Ω* Gain Adj.
10k
10k
4.8V
10k
Transducer
2.5k
LM614
LM614
D7 – D0
DATA
OUT
V_IN (+)
10k
3k
1k
Sets Zero
Code Voltage
1 µF
LM614
V_IN (−)
AGND
DGND
*Full Scale Adjust

TL/H/9326–45

FIGURE 15. Transducer Data Acquisition System. Set zero code voltage, then adjust 10Ω gain adjust pot for full scale.

National Semiconductor

LM675 Power Operational Amplifier

General Description

The LM675 is a monolithic power operational amplifier featuring wide bandwidth and low input offset voltage, making it equally suitable for AC and DC applications.

The LM675 is capable of delivering output currents in excess of 3 amps, operating at supply voltages of up to 60V. The device overload protection consists of both internal current limiting and thermal shutdown. The amplifier is also internally compensated for gains of 10 or greater.

Features

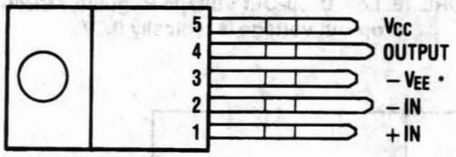
- 3A current capability
- A_{VO} typicaly 90 dB
- 5.5 MHz gain bandwidth product
- 8 V/µs slew rate
- Wide power bandwidth 70 kHz
- 1 mV typical offset voltage
- Short circuit protection
- Thermal protection with parole circuit (100% tested)
- 16V–60V supply range
- Wide common mode range
- Internal output protection diodes
- 90 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance power op amp
- Bridge amplifiers
- Motor speed controls
- Servo amplifiers
- Instrument systems

Connection Diagram

TO-220 Power Package (T)



TL/H/6739–1

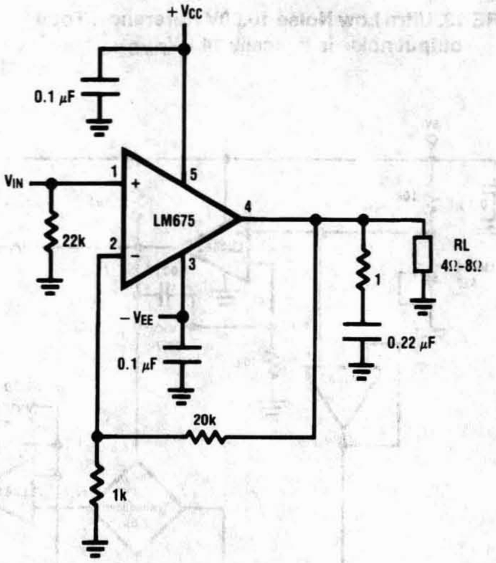
Front View

Order Number LM675T
See NS Package T05B

*The tab is internally connected to pin 3 ($-V_{EE}$)

Typical Applications

Non-Inverting Amplifier



TL/H/6739–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±30V
Input Voltage	$-V_{EE}$ to V_{CC}
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Note 1)	30W
Lead Temperature (Soldering, 10 seconds)	260°C

ESD rating to be determined.

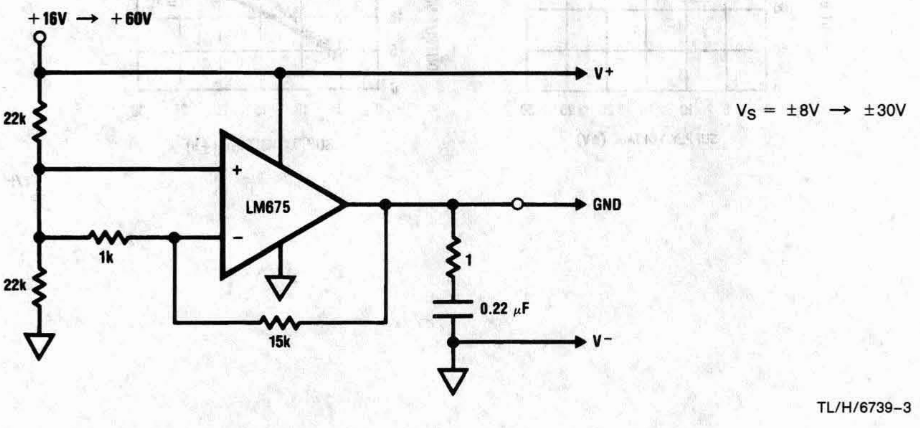
Electrical Characteristics $V_S = \pm 25V$, $T_A = 25°C$ unless otherwise specified.

Parameter	Conditions	Typical	Tested Limit	Units
Supply Current	$P_{OUT} = 0W$	18	50 (max)	mA
Input Offset Voltage	$V_{CM} = 0V$	1	10 (max)	mV
Input Bias Current	$V_{CM} = 0V$	0.2	2 (max)	μA
Input Offset Current	$V_{CM} = 0V$	50	500 (max)	nA
Open Loop Gain	$R_L = \infty\Omega$	90	70 (min)	dB
PSRR	$\Delta V_S = \pm 5V$	90	70 (min)	dB
CMRR	$V_{IN} = \pm 20V$	90	70 (min)	dB
Output Voltage Swing	$R_L = 8\Omega$	±21	±18 (min)	V
Offset Voltage Drift Versus Temperature	$R_S < 100 k\Omega$	25		μV/°C
Offset Voltage Drift Versus Output Power		25		μV/W
Output Power	THD = 1%, $f_O = 1$ kHz, $R_L = 8\Omega$	25	20	W
Gain Bandwidth Product	$f_O = 20$ kHz, $A_{VCL} = 1000$	5.5		MHz
Max Slew Rate		8		V/μs
Input Common Mode Range		±22	±20 (min)	V

Note 1: Assumes T_A equal to 70°C. For operation at higher tab temperatures, the LM675 must be derated based on a maximum junction temperature of 150°C.

Typical Applications (Continued)

Generating a Split Supply From a Single Supply



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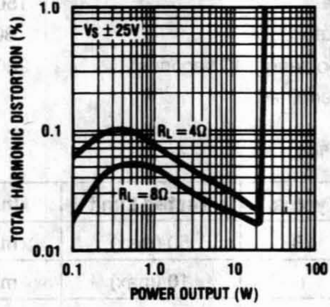
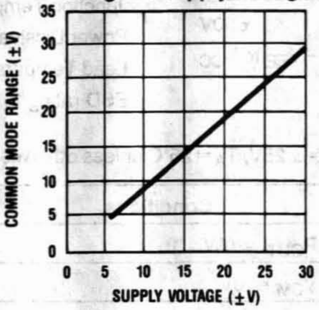
Typical Performance Characteristics

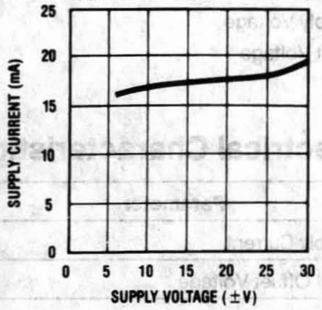
THD vs Power Output



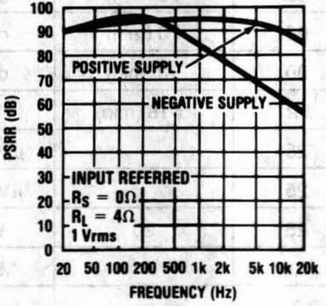
Input Common Mode Range vs Supply Voltage



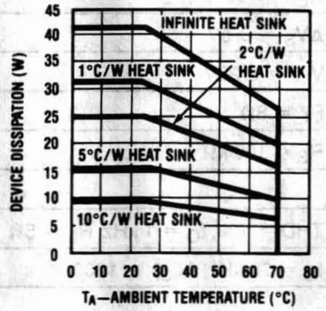
Supply Current vs Supply Voltage



PSRR vs Frequency

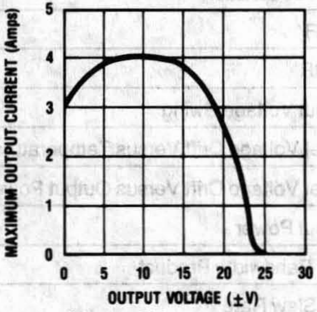


Device Dissipation vs Ambient Temperature†



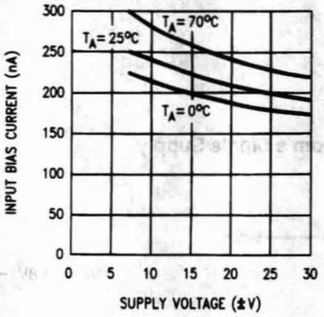
†θ INTERFACE = 1° C/W.
See Application Hints.

Current Limit vs Output Voltage*

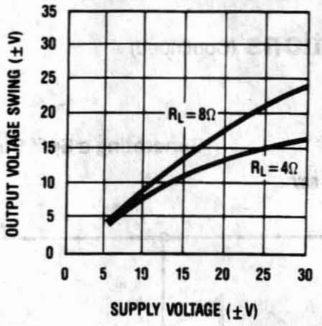


$^*V_S$ = ±25V

I_B vs Supply Voltage

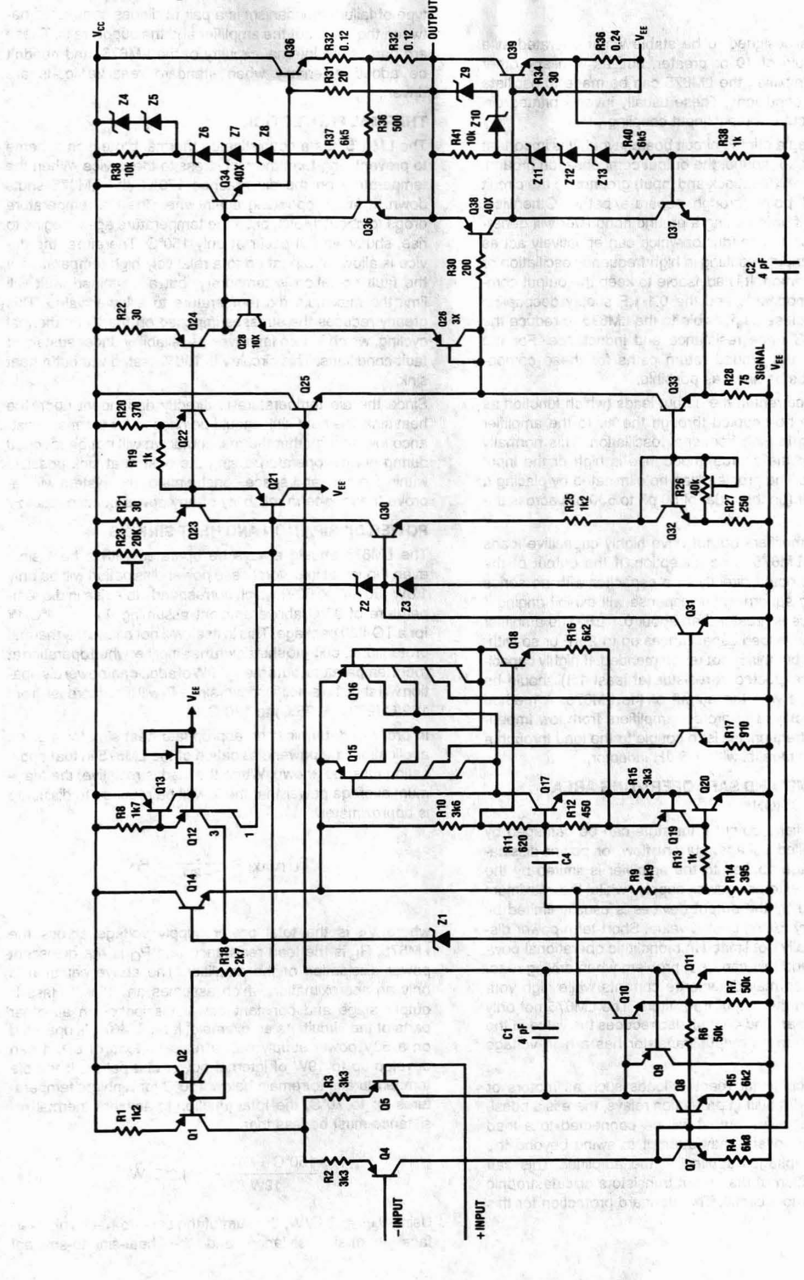


Output Voltage Swing vs Supply Voltage



TL/H/6739–4

Schematic Diagram


V_CC
V_EE
-INPUT
+INPUT
OUTPUT
SIGNAL
R1 1k2
R2 3k3
R3 3k3
R4 6k8
R5 6k2
R6 50k
R7 50k
R8 1k7
R9 4k9
R10 3k6
R11 620
R12 450
R13 1k
R14 395
R15 3k3
R16 6k2
R17 910
R18 2k7
R19 1k
R20 370
R21 30
R22 30
R23 20K
R25 1k2
R26 40k
R27 250
R28 75
R30 200
R31 20
R32 0.12
R32 0.12
R34 30
R36 500
R36 0.24
R37 6k5
R38 10k
R38 1k
R40 6k5
R41 10k
C1 4 pF
C2 4 pF
C4
Q1
Q2
Q4
Q5
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26 3X
Q28 10X
Q30
Q31
Q32
Q33
Q34 40X
Q36
Q36
Q37
Q38 40X
Q39
Z1
Z2
Z3
Z4
Z5
Z6
Z7
Z8
Z9
Z10
Z11
Z12
Z13
1
3

TL/H/6739–5

Application Hints

STABILITY

The LM675 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM675 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a printed circuit board layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM675 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM675 is no exception. If the output of the LM675 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF. The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1Ω) should be placed in series with the output of the LM675. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 5 μH inductor.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic operational power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM675 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM675, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM675 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM675 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions. This circuitry is 100% tested without a heat sink.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operaton. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor.

POWER DISSIPATION AND HEAT SINKING

The LM675 should always be operated with a heat sink, even though at idle worst case power dissipation will be only 1.8W (30 mA × 60V) which corresponds to a rise in die temperature of 97°C above ambient assuming $\theta_{jA} = 54°C/W$ for a TO-220 package. This in itself will not cause the thermal protection circuitry to shut down the amplifier when operating at room temperature, but a mere 0.9W of additional power dissipation will shut the amplifier down since T_J will then increase from 122°C (97°C + 25°C) to 170°C.

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM675 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D\,(MAX)} \approx \frac{V_S{}^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM675, R_L is the load resistance and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. As an example, if the LM675 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150°C - 70°C}{19W} = 4.2°C/W.$$

Using $\theta_{JC} = 2°C/W$, the sum of the case-to-heat sink interface thermal resistance and the heat-sink-to-ambient

Application Hints (Continued)

thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry. If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM675 and the heat sink. The heat sink thermal resistance must then be less than

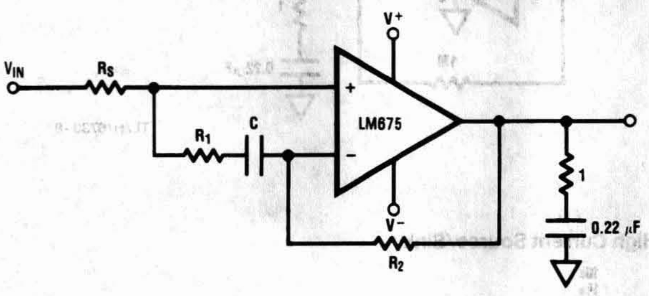
$$4.2^\circ\mathrm{C/W} - 2^\circ\mathrm{C/W} - 1.6^\circ\mathrm{C/W} = 0.6^\circ\mathrm{C/W}.$$

This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be restricted to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load will be roughly that of the same amplifier driving the resistive part of that load. For example, some reactive loads may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 8Ω × cos 60° or 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Typical Applications (Continued)

Non-Inverting Unity Gain Operation



$$R_1C \geq \frac{1}{2\pi 500\ \mathrm{kHz}}$$

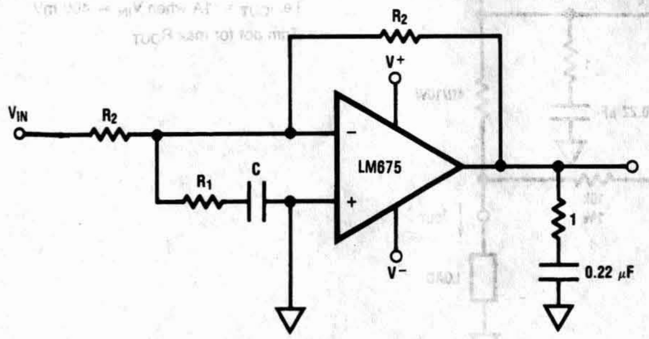
$$R_1 \leq \frac{R_S + R_2}{10}$$

$$A_{V(DC)} = 1$$

UNITY GAIN BANDWIDTH ≅ 50 kHz

TL/H/6739-6

Inverting Unity Gain Operation



$$R_1C \geq \frac{1}{2\pi 500\ \mathrm{kHz}}$$

$$R_1 \leq \frac{R_2}{10}$$

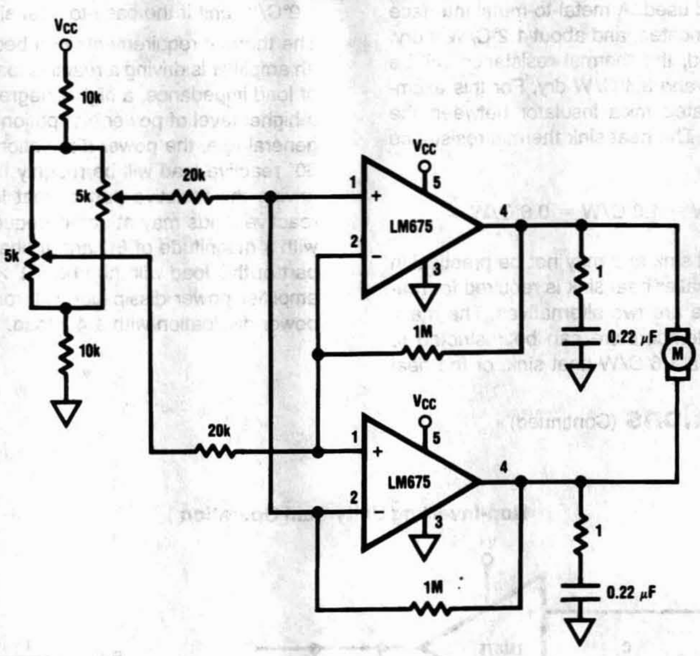
$$A_{V(DC)} = -1$$

UNITY GAIN BANDWIDTH ≅ 50 kHz

TL/H/6739-7

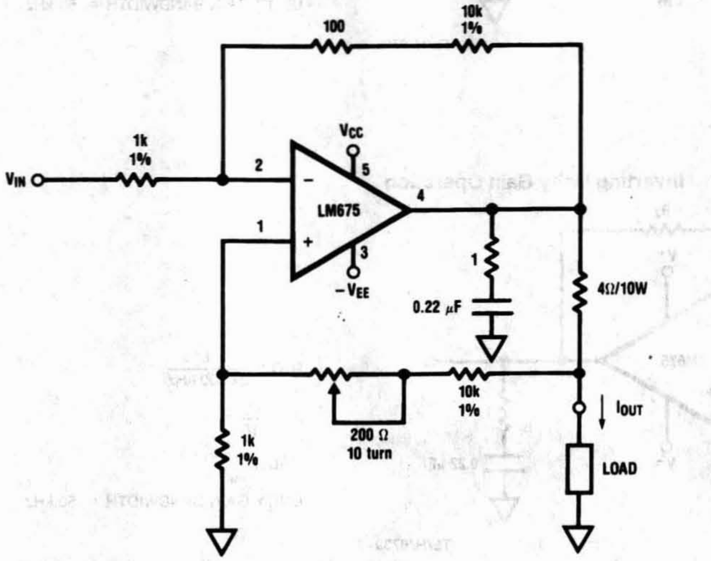
Typical Applications (Continued)

Servo Motor Control


VCC
10k
5k
20k
5k
10k
20k
VCC
1
+
5
2
−
LM675
4
3
1
0.22 μF
M
1M
VCC
1
+
5
LM675
4
2
−
3
1
1M
0.22 μF

TL/H/6739-8

High Current Source/Sink


100
10k
1%
1k
1%
VIN
2
−
VCC
5
LM675
4
1
+
3
−VEE
1
0.22 μF
4Ω/10W
10k
1%
200 Ω
10 turn
I_{OUT}
LOAD
1k
1%

$I_{OUT} = V_{IN} \times 2.5$ amps/volt

i.e. $I_{OUT} = 1A$ when $V_{IN} = 400$ mV

Trim pot for max R_{OUT}

TL/H/6739-9

National Semiconductor

LM709
Operational Amplifier

General Description

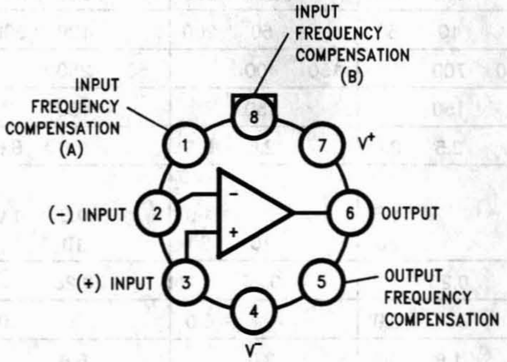
The LM709 series is a monolithic operational amplifier intended for general-purpose applications. Operation is completely specified over the range of voltages commonly used for these devices. The design, in addition to providing high gain, minimizes both offset voltage and bias currents. Further, the class-B output stage gives a large output capability with minimum power drain.

External components are used to frequency compensate the amplifier. Although the unity-gain compensation network specified will make the amplifier unconditionally stable in all feedback configurations, compensation can be tailored to optimize high-frequency performance for any gain setting.

The LM709C is the commercial-industrial version of the LM709. It is identical to the LM709 except that it is specified for operation from 0°C to +70°C.

Connection Diagrams

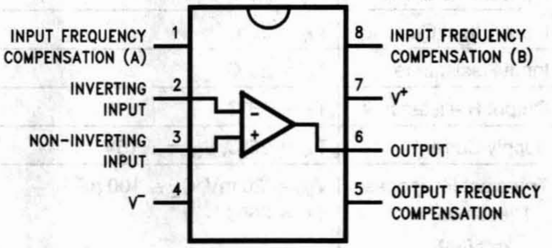
Metal Can Package


INPUT FREQUENCY COMPENSATION (B)
INPUT FREQUENCY COMPENSATION (A)
V⁺
(−) INPUT
OUTPUT
(+) INPUT
OUTPUT FREQUENCY COMPENSATION
V⁻
1
2
3
4
5
6
7
8
−
+

TL/H/11477–4

Order Number LM709AH, LM709H or LM709CH
See NS Package Number H08C

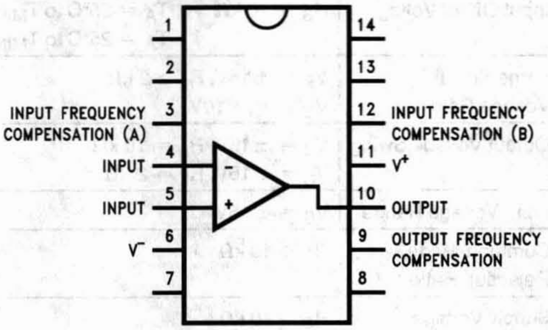
Dual-In-Line Package


INPUT FREQUENCY COMPENSATION (A)
INVERTING INPUT
NON-INVERTING INPUT
V⁻
INPUT FREQUENCY COMPENSATION (B)
V⁺
OUTPUT
OUTPUT FREQUENCY COMPENSATION
1
2
3
4
5
6
7
8
−
+

TL/H/11477–6

Order Number LM709CN-8
See NS Package Number N08E

Dual-In-Line Package


INPUT FREQUENCY COMPENSATION (A)
INPUT
INPUT
V⁻
INPUT FREQUENCY COMPENSATION (B)
V⁺
OUTPUT
OUTPUT FREQUENCY COMPENSATION
1
2
3
4
5
6
7
8
9
10
11
12
13
14
−
+

TL/H/11477–5

Order Number LM709CN
See NS Package Number N14A

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
LM709/LM709A/LM709C	±18V
Power Dissipation (Note 1)	
LM709/LM709A	300 mW
LM709C	250 mW
Differential Input Voltage	
LM709/LM709A/LM709C	±5V
Input Voltage	
LM709/LM709A/LM709C	±10V
Output Short-Circuit Duration ($T_A = +25°C$)	
LM709/LM709A/LM709C	5 seconds
Storage Temperature Range	
LM709/LM709A/LM709C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
LM709/LM709A/LM709C	300°C

Operating Ratings (Note 3)

Junction Temperature Range (Note 1)	
LM709/LM709A	−55°C to +150°C
LM709C	0°C to +100°C
Thermal Resistance (θ_{JA})	
H Package	150°C/W, (θ_{JC}) 45°C/W
8-Pin N Package	134°C/W
14-Pin N Package	109°C/W

Electrical Characteristics (Note 2)

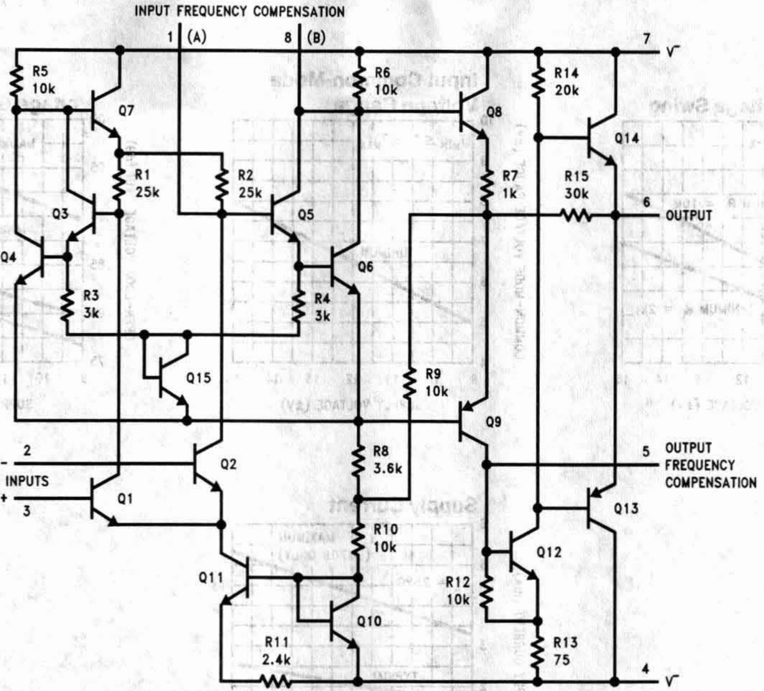
Parameter	Conditions	LM709A			LM709			LM709C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		0.6	2.0		1.0	5.0		2.0	7.5	mV
Input Bias Current	$T_A = 25°C$		100	200		200	500		300	1500	nA
Input Offset Current	$T_A = 25°C$		10	50		50	200		100	500	nA
Input Resistance	$T_A = 25°C$	350	700		150	400		50	250		kΩ
Output Resistance	$T_A = 25°C$		150			150			150		Ω
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		2.5	3.6		2.6	5.5		2.6	6.6	mA
Transient Response	$V_{IN} = 20\ mV$, $C_L \leq 100\ pF$										
Risetime	$T_A = 25°C$			1.5		0.3	1.0		0.3	1.0	μs
Overshoot				30		10	30		10	30	%
Slew Rate	$T_A = 25°C$		0.25			0.25			0.25		V/μs
Input Offset Voltage	$R_S \leq 10\ k\Omega$			3.0			6.0			10	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ to T_{MAX}		1.8	10		3.0			6.0		μV/°C
	$T_A = 25°C$ to T_{MIN}		1.8	10		6.0			12		
	$R_S = 10\ k\Omega$, $T_A = 25°C$ to T_{MAX}		2.0	15							
	$T_A = 25°C$ to T_{MIN}		4.8	25							
Large Signal Voltage Gain	$V_S = \pm 15V$, $R_L \geq 2\ k\Omega$ $V_{OUT} = \pm 10V$	25		70	25	45	70	15	45		V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		±12	±14		V
	$V_S = \pm 15V$, $R_L = 2\ k\Omega$	±10	±13		±10	±13		±10	±13		
Input Voltage Range	$V_S = \pm 15V$	±8			±8	±10		±8	±10		V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	80	110		70	90		65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		40	100		25	150		25	200	μV/V
Input Offset Current	$T_A = T_{MAX}$		3.5	50		20	200		75	400	nA
	$T_A = T_{MIN}$		40	250		100	500		125	750	
Input Bias Current	$T_A = T_{MIN}$		0.3	0.6		0.5	1.5		0.36	2.0	μA
Input Resistance	$T_A = T_{MIN}$	85	170		40	100		50	250		kΩ

Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature for LM709/LM709A and 100°C maximum for L709C. For operating at elevated temperatures, the device must be derated based on thermal resistance θ_{JA}, $T_{J(MAX)}$ and T_A.

Note 2: These specifications apply for $-55°C \leq T_A \leq +125°C$ for the LM709/LM709A and $0°C \leq T_A \leq +70°C$ for the LM709C with the following conditions: $\pm 9V \leq V_S \leq \pm 15V$, C1 = 5000 pF, R1 = 1.5 kΩ, C2 = 200 pF and R2 = 51Ω.

Note 3: Absolute Maximum Ratings indicate limits which if exceeded may result in damage. Operating Ratings are conditions where the device is expected to be functional but not necessarily within the guaranteed performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

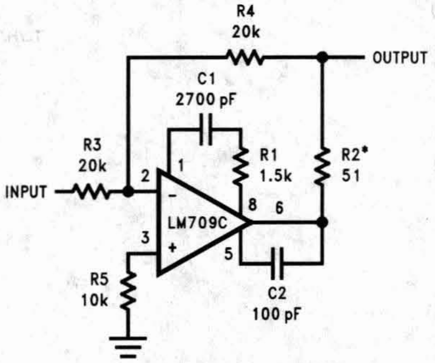
Schematic Diagram**


INPUT FREQUENCY COMPENSATION
1 (A)
8 (B)
7
V⁺
R5 10k
Q7
R1 25k
R2 25k
Q5
R6 10k
Q8
R14 20k
Q14
Q3
Q4
R3 3k
Q6
R4 3k
R7 1k
R15 30k
6
OUTPUT
Q15
R9 10k
Q9
2
INPUTS
3
Q1
Q2
R8 3.6k
5
OUTPUT FREQUENCY COMPENSATION
Q13
R10 10k
Q12
Q11
R12 10k
Q10
R11 2.4k
R13 75
4
V⁻

TL/H/11477–1

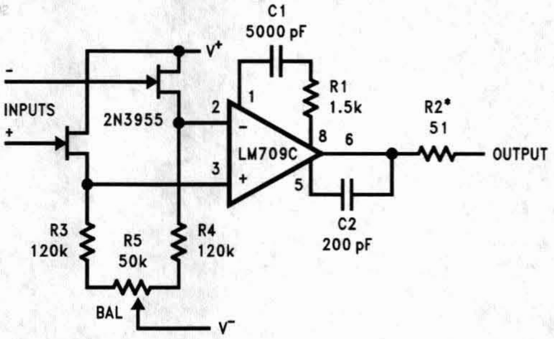
Typical Applications**

Unity Gain Inverting Amplifier


R4 20k
OUTPUT
C1 2700 pF
R3 20k
INPUT
R1 1.5k
R2* 51
1
2
8
6
LM709C
3
5
R5 10k
C2 100 pF

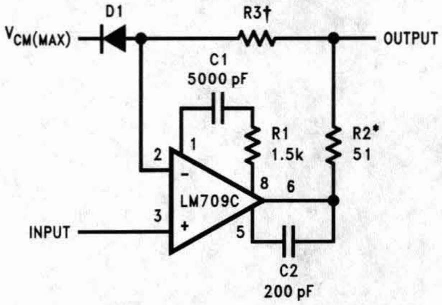
TL/H/11477–2

FET Operational Amplifier


C1 5000 pF
V⁺
R1 1.5k
INPUTS
2N3955
R2* 51
2
1
8
6
LM709C
OUTPUT
3
5
C2 200 pF
R3 120k
R5 50k
R4 120k
BAL
V⁻

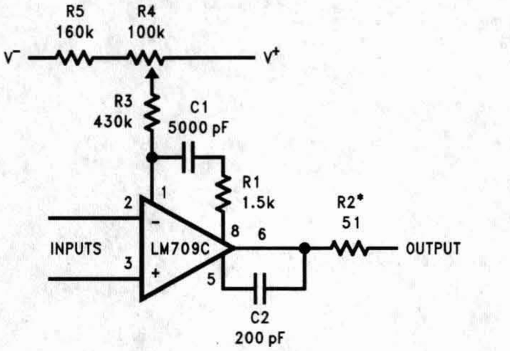
TL/H/11477–3

Voltage Follower


D1
R3†
$V_{CM(MAX)}$
OUTPUT
C1 5000 pF
R1 1.5k
R2* 51
1
2
8
6
LM709C
INPUT
3
5
C2 200 pF

TL/H/11477–7

Offset Balancing Circuit


R5 160k
R4 100k
V⁻
V⁺
R3 430k
C1 5000 pF
R1 1.5k
1
2
8
6
R2* 51
INPUTS
LM709C
OUTPUT
3
5
C2 200 pF

TL/H/11477–8

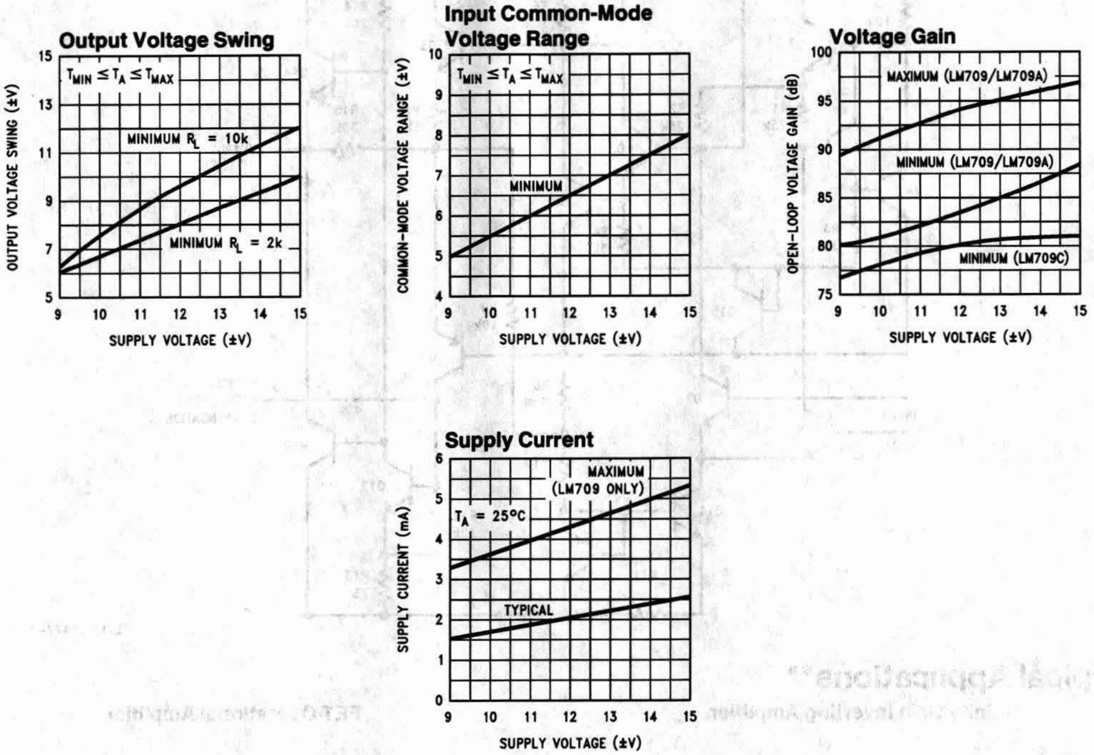
*To be used with any capacitive loading on output.

**Pin connections shown are for metal can package.

†Should be equal to DC source resistance on input.

1

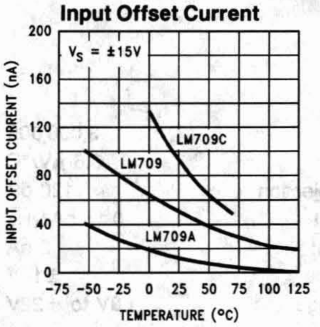
Guaranteed Performance Characteristics



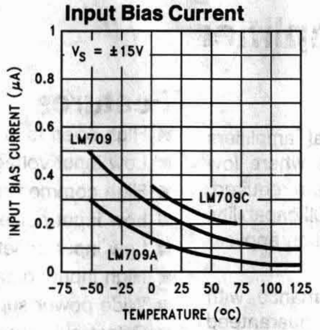
TL/H/11477–9

Typical Performance Characteristics

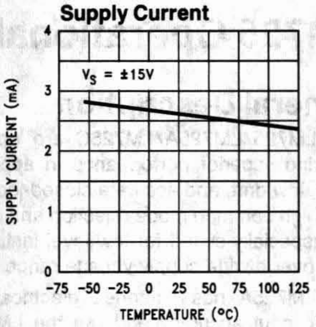
Input Offset Current



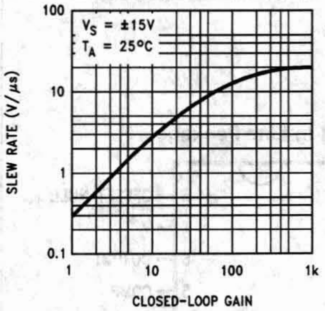
Input Bias Current



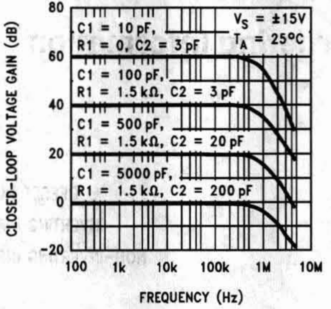
Supply Current



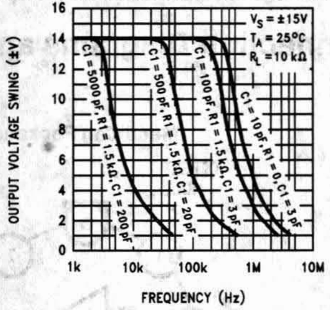
Slew Rate as a Function of Closed-Loop Gain Using Recommended Compensation Networks



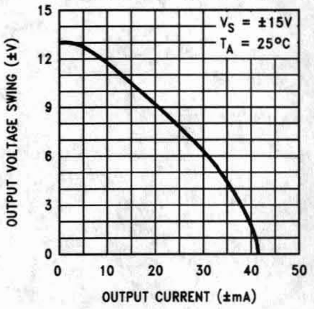
Frequency Response for Various Closed-Loop Gains



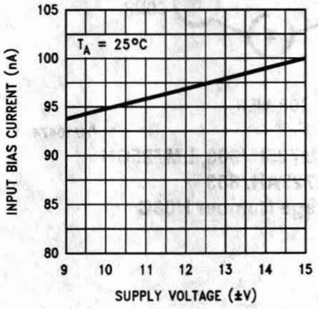
Output Voltage Swing as a Function of Frequency



Output Voltage Swing



Input Bias Current as a Function of Supply Voltage



TL/H/11477-10

National Semiconductor

LM725 Operational Amplifier

General Description

The LM725/LM725A/LM725C are operational amplifiers featuring superior performance in applications where low noise, low drift, and accurate closed-loop gain are required. With high common mode rejection and offset null capability, it is especially suited for low level instrumentation applications over a wide supply voltage range.

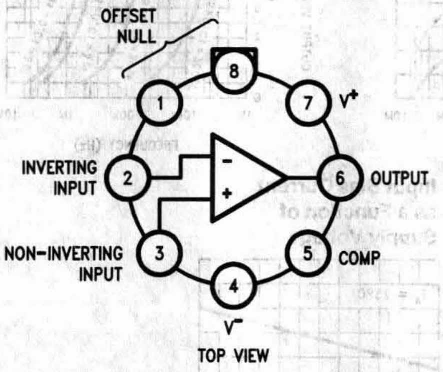
The LM725A has tightened electrical performance with higher input accuracy and like the LM725, is guaranteed over a −55°C to +125°C temperature range. The LM725C has slightly relaxed specifications and has its performance guaranteed over a 0°C to 70°C temperature range.

Features

■ High open loop gain	3,000,000
■ Low input voltage drift	0.6 μV/°C
■ High common mode rejection	120 dB
■ Low input noise current	0.15 pA/$\sqrt{\text{Hz}}$
■ Low input offset current	2 nA
■ High input voltage range	±14V
■ Wide power supply range	±3V to ±22V
■ Offset null capability	
■ Output short circuit protection	

Connection Diagrams and Ordering Information

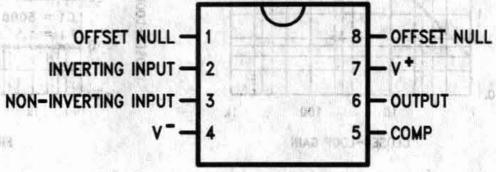
Metal Can Package


OFFSET
NULL
8
1
7
V+
INVERTING
INPUT
2
−
+
6
OUTPUT
NON-INVERTING
INPUT
3
5
COMP
4
V−
TOP VIEW

TL/H/10474-1

Order Number LM725H/883, LM725CH
or LM725AH/883
See NS Package Number H08C

Dual-In-Line Package


OFFSET NULL
1
INVERTING INPUT
2
NON-INVERTING INPUT
3
V−
4
8
OFFSET NULL
7
V+
6
OUTPUT
5
COMP

TL/H/10474-2

Order Number LM725CN
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	260°C
Maximum Junction Temperature	150°C

Operating Temperature Range	$T_{A(MIN)}$		$T_{A(MAX)}$
LM725	−55°C	to	+125°C
LM725A	−55°C	to	+125°C
LM725C	0°C	to	+70°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM725A			LM725			LM725C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Without External Trim)	T_A = 25°C, R_S ≤ 10 kΩ			0.5		0.5	1.0		0.5	2.5	mV
Input Offset Current	T_A = 25°C		2.0	5.0		2.0	20		2.0	35	nA
Input Bias Current	T_A = 25°C		42	80		42	100		42	125	nA
Input Noise Voltage	T_A = 25°C										
	f_o = 10 Hz		15			15			15		nV/√Hz
	f_o = 100 Hz		9.0			9.0			9.0		nV/√Hz
	f_o = 1 kHz		8.0			8.0			8.0		nV/√Hz
Input Noise Current	T_A = 25°C										
	f_o = 10 Hz		1.0			1.0			1.0		pA/√Hz
	f_o = 100 Hz		0.3			0.3			0.3		pA/√Hz
	f_o = 1 kHz		0.15			0.15			0.15		pA/√Hz
Input Resistance	T_A = 25°C		1.5			1.5			1.5		MΩ
Input Voltage Range	T_A = 25°C	±13.5	±14		±13.5	±14		±13.5	±14		V
Large Signal Voltage Gain	T_A = 25°C, R_L ≥ 2 kΩ, V_{OUT} = ±10V	1000	3000		1000	3000		250	3000		V/mV
Common-Mode Rejection Ratio	T_A = 25°C, R_S ≤ 10 kΩ	120			110	120		94	120		dB
Power Supply Rejection Ratio	T_A = 25°C, R_S ≤ 10 kΩ		2.0	5.0		2.0	10		2.0	35	μV/V
Output Voltage Swing	T_A = 25°C,										
	R_L ≥ 10 kΩ	±12.5	±13.5		±12	±13.5		±12	±13.5		V
	R_L ≥ 2 kΩ	±12.0	±13.5		±10	±13.5		±10	±13.5		V
Power Consumption	T_A = 25°C		80	105		80	105		80	150	mW
Input Offset Voltage (Without External Trim)	R_S ≤ 10 kΩ			0.7			1.5			3.5	mV
Average Input Offset Voltage Drift (Without External Trim)	R_S = 50Ω			2.0		2.0	5.0		2.0		μV/°C
Average Input Offset Voltage Drift (With External Trim)	R_S = 50Ω		0.6	1.0		0.6			0.6		μV/°C
Input Offset Current	T_A = T_{MAX}		1.2	4.0		1.2	20		1.2	35	nA
	T_A = T_{MIN}		7.5	18.0		7.5	40		4.0	50	nA
Average Input Offset Current Drift			35	90		35	150		10		pA/°C
Input Bias Current	T_A = T_{MAX}		20	70		20	100			125	nA
	T_A = T_{MIN}		80	180		80	200			250	nA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM725A Min	LM725A Typ	LM725A Max	LM725 Min	LM725 Typ	LM725 Max	LM725C Min	LM725C Typ	LM725C Max	Units
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$ $T_A = T_{MAX}$	1,000,000			1,000,000			125,000			V/V
	$R_L \geq 2\ k\Omega$ $T_A = T_{MIN}$	500,000			250,000			125,000			V/V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	110			100				115		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$			8.0			20		20		μV/V
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±12			±10			±10			V

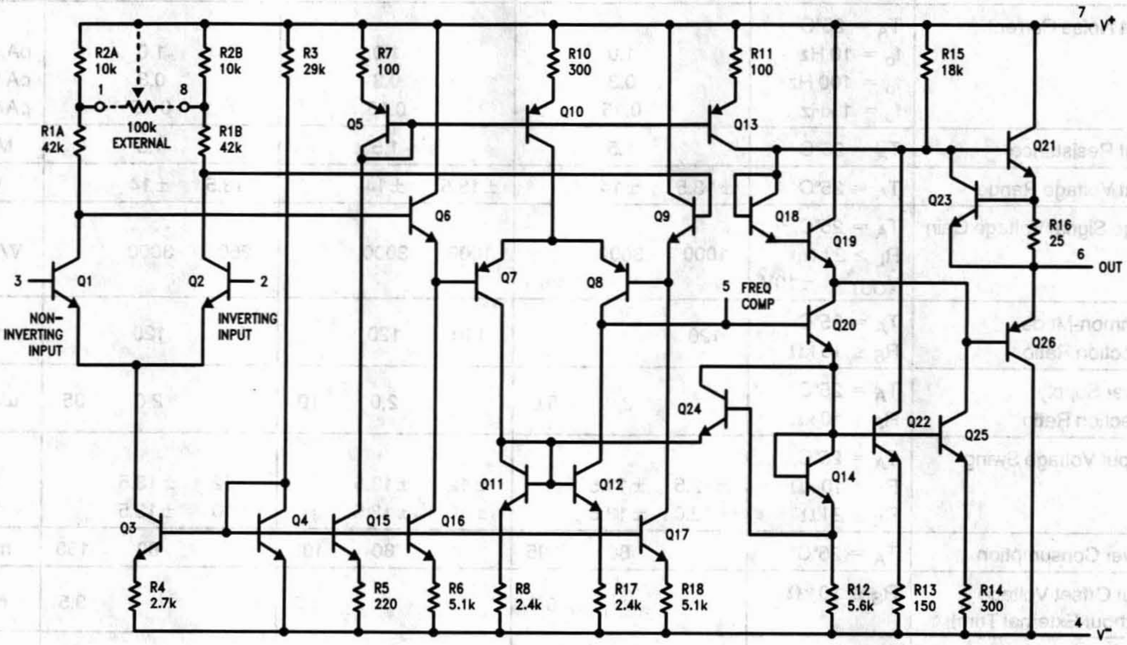
Note 1: Derate at 150°C/W for operation at ambient temperatures above 75°C.

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ unless otherwise specified.

Note 4: For Military electrical specifications RETS725AX are available for LM725AH and RETS725X are available for LM725H.

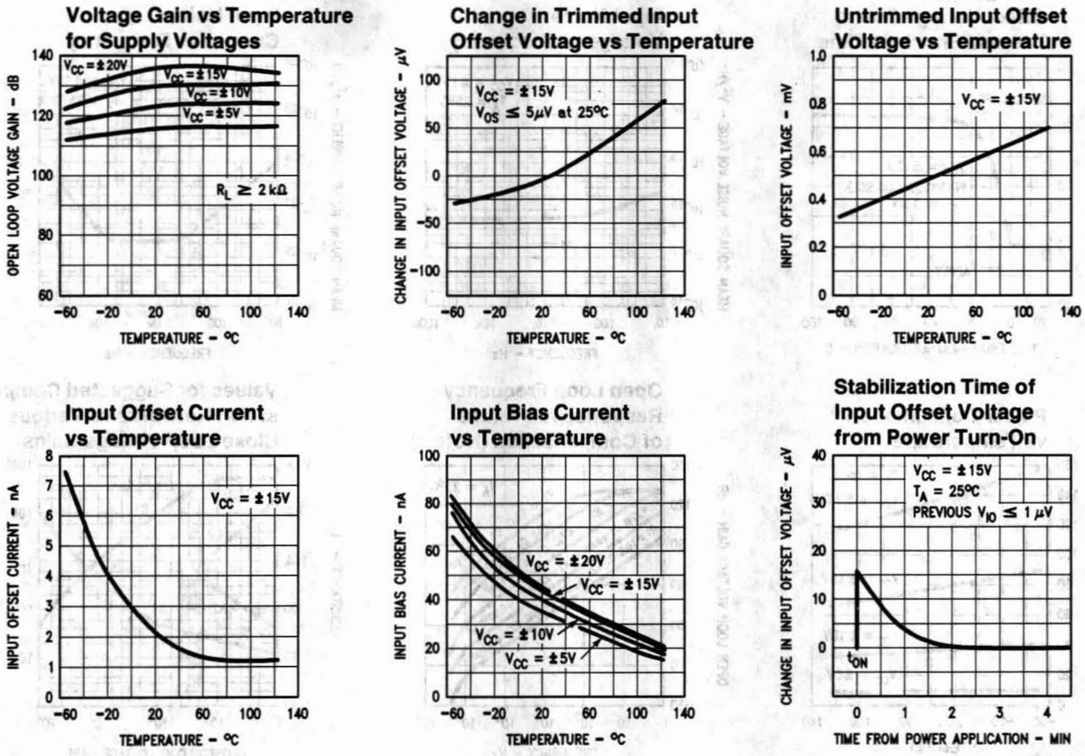
Schematic Diagram



R2A 10k
R2B 10k
1
8
100k EXTERNAL
R1A 42k
R1B 42k
R3 29k
R7 100
R10 300
R11 100
R15 18k
7
V+
Q5
Q10
Q13
Q21
Q6
Q9
Q18
Q19
Q23
R16 25
6
OUT
3
Q1
Q2
2
NON-INVERTING INPUT
INVERTING INPUT
Q7
Q8
5
FREQ COMP
Q20
Q26
Q24
Q22
Q25
Q14
Q11
Q12
Q3
Q4
Q15
Q16
Q17
R4 2.7k
R5 220
R6 5.1k
R8 2.4k
R17 2.4k
R18 5.1k
R12 5.6k
R13 150
R14 300
4
V−

TL/H/10474–5

Typical Performance Characteristics



Voltage Gain vs Temperature for Supply Voltages

Change in Trimmed Input Offset Voltage vs Temperature

Untrimmed Input Offset Voltage vs Temperature

Input Offset Current vs Temperature

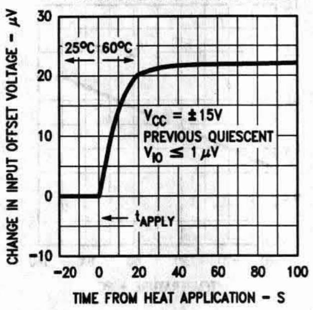
Input Bias Current vs Temperature

Stabilization Time of Input Offset Voltage from Power Turn-On

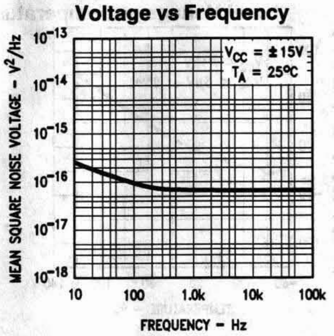
TL/H/10474–6

Typical Performance Characteristics (Continued)

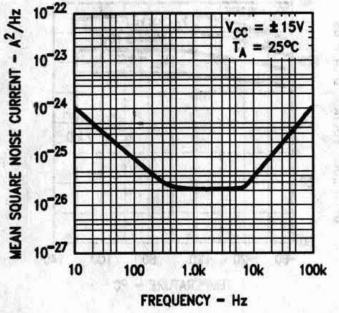
Change in Input Offset Voltage Due to Thermal Shock vs Time



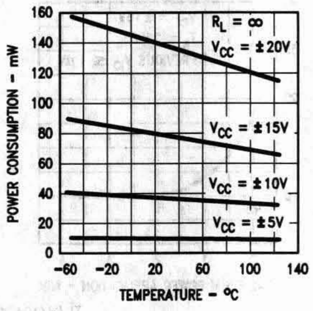
Input Noise Voltage vs Frequency



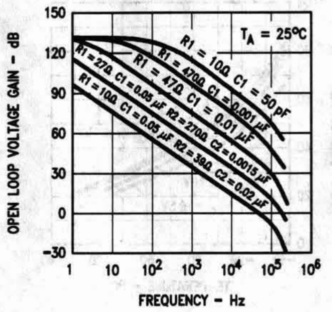
Input Noise Current vs Frequency



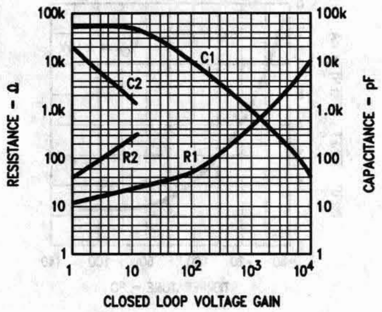
Power Consumption vs Temperature



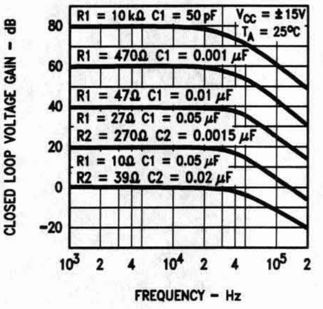
Open Loop Frequency Response for Values of Compensation (Note 1)



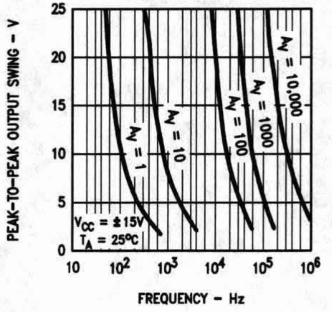
Values for Suggested Compensation Networks vs Various Close Loop Voltage Gains



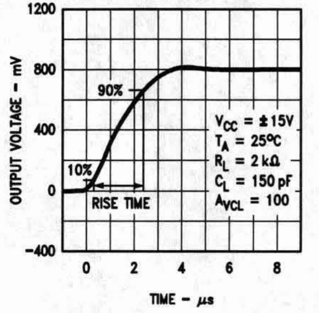
Frequency Response for Various Close Loop Gain (Note 1)



Output Voltage Swing vs Frequency (Note 1)



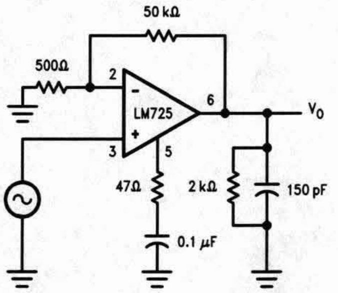
Transient Response



TL/H/10474–7

Note 1: Performance is shown using recommended compensation networks.

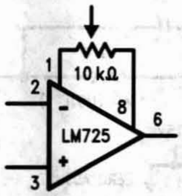
Transient Response Test Circuit



TL/H/10474–8

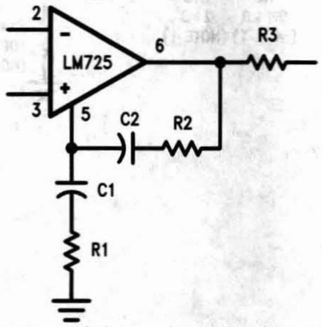
Auxiliary Circuits

Voltage Offset Null Circuit


V+
10 kΩ
1
2
8
6
LM725
−
+
3

TL/H/10474-3

Frequency Compensation Circuit


2
−
LM725
+
3
6
R3
5
C2
R2
C1
R1

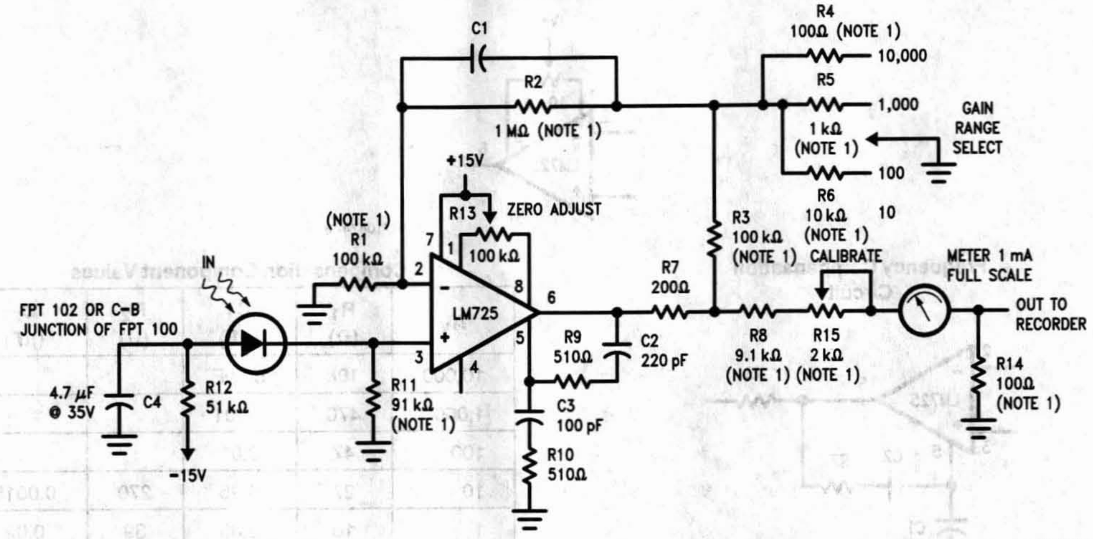
TL/H/10474-4

Compensation Component Values

A_V	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10k	50 pF		
1,000	470	0.001		
100	47	0.01		
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

Typical Applications

Photodiode Amplifier

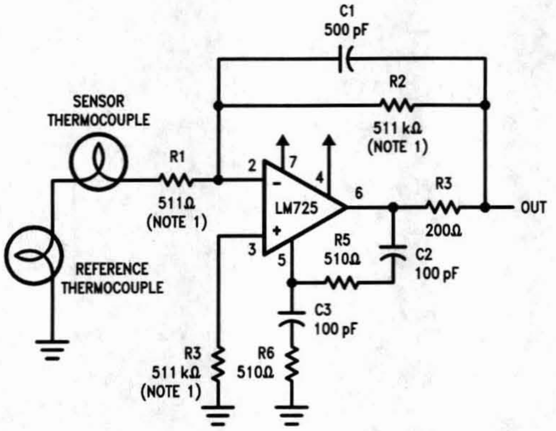

C1
R2
1 MΩ (NOTE 1)
R4
100Ω (NOTE 1)
10,000
R5
1,000
1 kΩ
(NOTE 1)
100
R6
10 kΩ
(NOTE 1)
10
GAIN
RANGE
SELECT
+15V
R13
ZERO ADJUST
100 kΩ
(NOTE 1)
R1
100 kΩ
IN
FPT 102 OR C-B
JUNCTION OF FPT 100
LM725
7
1
2
8
6
3
5
4
R3
100 kΩ
(NOTE 1)
CALIBRATE
METER 1 mA
FULL SCALE
OUT TO
RECORDER
R7
200Ω
R8
9.1 kΩ
(NOTE 1)
R15
2 kΩ
(NOTE 1)
R14
100Ω
(NOTE 1)
R9
510Ω
C2
220 pF
C3
100 pF
R10
510Ω
R11
91 kΩ
(NOTE 1)
R12
51 kΩ
4.7 µF
@ 35V
C4
-15V

TL/H/10474–9

DC Gains = 10,000; 1,000; 100; and 10

Bandwidth = Determined by value of C1

Thermocouple Amplifier


C1
500 pF
R2
511 kΩ
(NOTE 1)
SENSOR
THERMOCOUPLE
R1
511Ω
(NOTE 1)
REFERENCE
THERMOCOUPLE
LM725
2
7
4
6
3
5
R3
200Ω
OUT
R5
510Ω
C2
100 pF
C3
100 pF
R3
511 kΩ
(NOTE 1)
R6
510Ω

TL/H/10474–10

$$\frac{R2}{R5} = \frac{R6}{R7} \text{ for best CMR}$$

$R1 = R4$

$R2 = R5$

$$\text{Gain} = \frac{R6}{R2} + \left(\frac{2R1}{R3}\right)$$

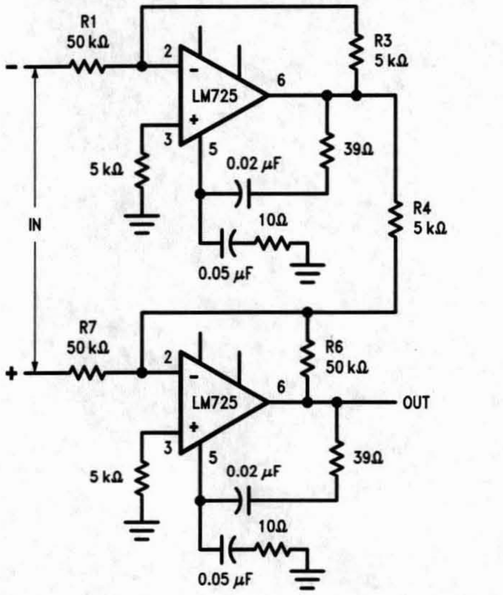
DC Gain = 1000

Bandwidth = DC to 540 Hz

Equivalent Input Noise = 0.24 μV_{rms}

Note 1: Indicates ±1% metal film resistors recommended for temperature stability.

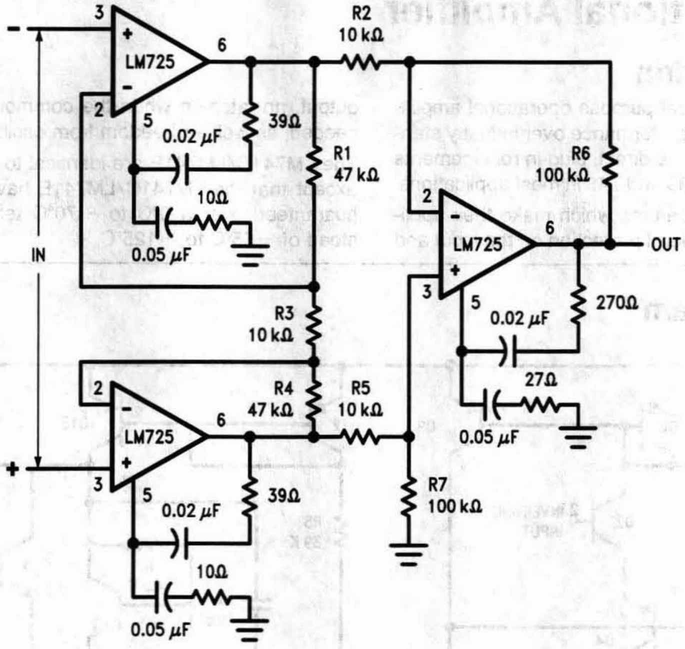
±100V Common Mode Range Differential Amplifier


R1
50 kΩ
-
2
LM725
6
3
5
R3
5 kΩ
5 kΩ
39Ω
0.02 µF
10Ω
0.05 µF
IN
R4
5 kΩ
R7
50 kΩ
+
R6
50 kΩ
2
LM725
6
OUT
3
5
5 kΩ
39Ω
0.02 µF
10Ω
0.05 µF

TL/H/10474–11

Typical Applications (Continued)

Instrumentation Amplifier with High Common Mode Rejection


−
+
IN
3
2
5
6
LM725
39Ω
0.02 μF
10Ω
0.05 μF
R1
47 kΩ
R2
10 kΩ
R3
10 kΩ
R4
47 kΩ
R5
10 kΩ
R6
100 kΩ
R7
100 kΩ
270Ω
27Ω
OUT

TL/H/10474-12

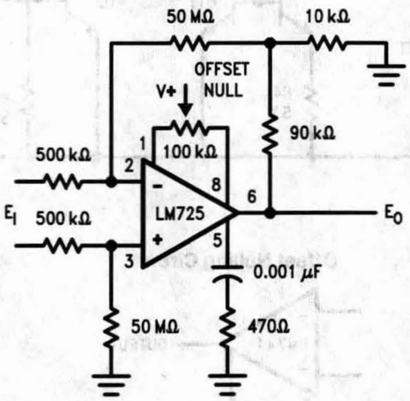
$\frac{R1}{R6} = \frac{R3}{R4}$ for best CMRR

$R3 = R4$

$R1 = R6 = 10\ R3$

$\text{Gain} = \frac{R6}{R7}$

Precision Amplifier $A_{VCL} = 1000$


50 MΩ
10 kΩ
OFFSET NULL
V+
100 kΩ
90 kΩ
500 kΩ
500 kΩ
E_I
1
2
3
5
6
8
LM725
E_O
0.001 μF
50 MΩ
470Ω

TL/H/10474-13

National Semiconductor

LM741 Operational Amplifier

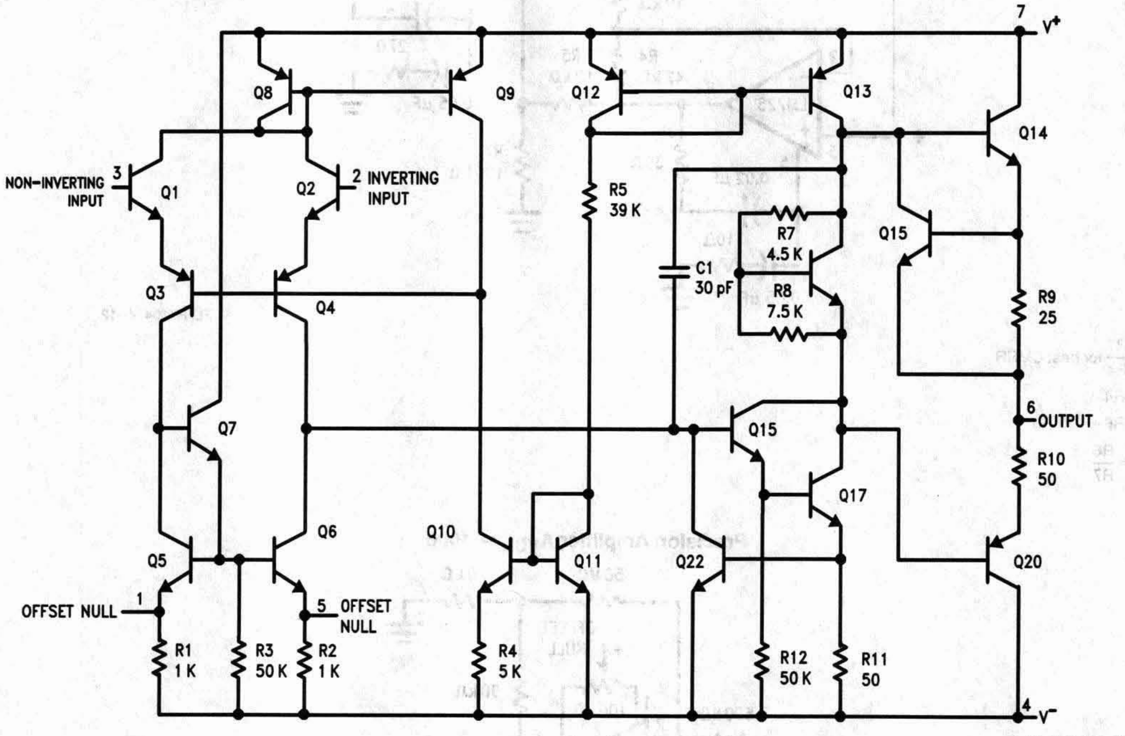
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

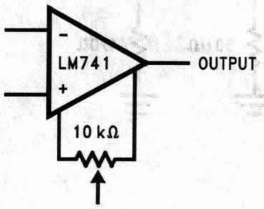
The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Schematic Diagram


7
V+
Q8
Q9
Q12
Q13
Q14
3
NON-INVERTING INPUT
Q1
Q2
2 INVERTING INPUT
R5
39 K
R7
4.5 K
Q15
C1
30 pF
R8
7.5 K
R9
25
Q3
Q4
6
OUTPUT
Q7
Q15
R10
50
Q17
Q6
Q10
Q5
Q11
Q22
Q20
1
OFFSET NULL
5 OFFSET NULL
R1
1 K
R3
50 K
R2
1 K
R4
5 K
R12
50 K
R11
50
4
V−

TL/H/9341-1

Offset Nulling Circuit


−
LM741
+
OUTPUT
10 kΩ
V−

TL/H/9341-7

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 5)

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	100°C	150°C	100°C
Soldering Information				
N-Package (10 seconds)	260°C	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C	300°C
M-Package				
Vapor Phase (60 seconds)	215°C	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C	215°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

	LM741A	LM741E	LM741	LM741C
ESD Tolerance (Note 6)	400V	400V	400V	400V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C, V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25°C, V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	$T_A = 25°C, R_L \ge 2\ k\Omega$										
	$V_S = \pm 20V, V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V, V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2\ k\Omega$,										
	$V_S = \pm 20V, V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V, V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V, V_O = \pm 2V$	10									V/mV

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM741A/LM741E Min	LM741A/LM741E Typ	LM741A/LM741E Max	LM741 Min	LM741 Typ	LM741 Max	LM741C Min	LM741C Typ	LM741C Max	Units
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
	$V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		μs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/μs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 1: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

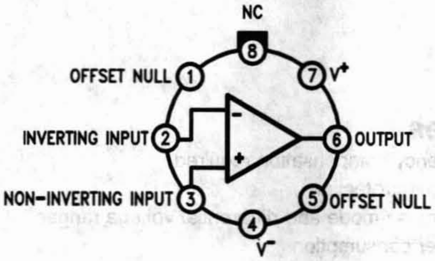
Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 5: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

Connection Diagrams

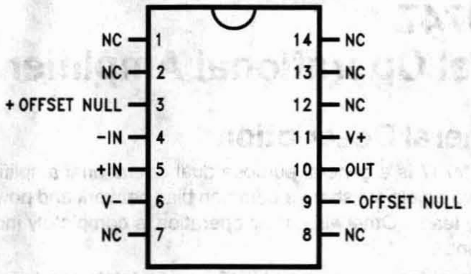
Metal Can Package


NC
8
OFFSET NULL
1
7
V+
INVERTING INPUT
2
6
OUTPUT
NON-INVERTING INPUT
3
5
OFFSET NULL
4
V−
−
+

TL/H/9341–2

Order Number LM741H, LM741H/883*, LM741AH/883 or LM741CH
See NS Package Number H08C

Ceramic Dual-In-Line Package


NC 1
NC 2
+OFFSET NULL 3
−IN 4
+IN 5
V− 6
NC 7
14 NC
13 NC
12 NC
11 V+
10 OUT
9 −OFFSET NULL
8 NC

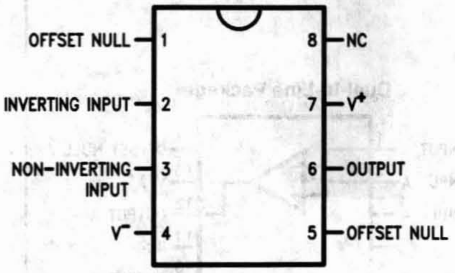
TL/H/9341–5

Order Number LM741J-14/883*, LM741AJ-14/883**
See NS Package Number J14A

*also available per JM38510/10101

**also available per JM38510/10102

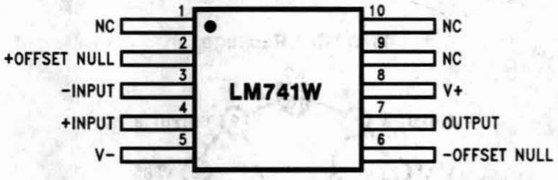
Dual-In-Line or S.O. Package


OFFSET NULL 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
V− 4
8 NC
7 V+
6 OUTPUT
5 OFFSET NULL

TL/H/9341–3

Order Number LM741J, LM741J/883, LM741CM, LM741CN or LM741EN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak


LM741W
NC 1
+OFFSET NULL 2
−INPUT 3
+INPUT 4
V− 5
10 NC
9 NC
8 V+
7 OUTPUT
6 −OFFSET NULL

TL/H/9341–6

Order Number LM741W/883
See NS Package Number W10A

*LM741H is available per JM38510/10101

National Semiconductor

LM747
Dual Operational Amplifier

General Description

The LM747 is a general purpose dual operational amplifier. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

Additional features of the LM747 are: no latch-up when input common mode range is exceeded, freedom from oscillations, and package flexibility.

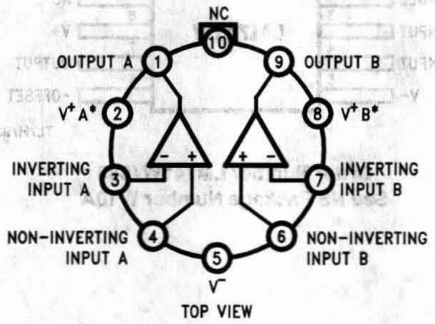
The LM747C/LM747E is identical to the LM747/LM747A except that the LM747C/LM747E has its specifications guaranteed over the temperature range from 0°C to +70°C instead of −55°C to +125°C.

Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low power consumption
- No latch-up
- Balanced offset null

Connection Diagrams

Metal Can Package

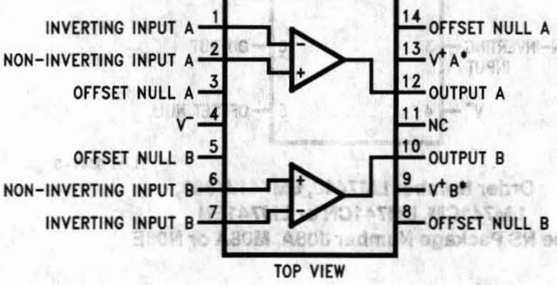

NC
10
OUTPUT A 1
V+A* 2
INVERTING INPUT A 3
NON-INVERTING INPUT A 4
5
V−
OUTPUT B 9
V+B* 8
INVERTING INPUT B 7
NON-INVERTING INPUT B 6
TOP VIEW

TL/H/11479-4

Order Number LM747H
See NS Package Number H10C

*V+A and V+B are internally connected.

Dual-In-Line Package


INVERTING INPUT A 1
NON-INVERTING INPUT A 2
OFFSET NULL A 3
V− 4
OFFSET NULL B 5
NON-INVERTING INPUT B 6
INVERTING INPUT B 7
14 OFFSET NULL A
13 V+A*
12 OUTPUT A
11 NC
10 OUTPUT B
9 V+B*
8 OFFSET NULL B
TOP VIEW

TL/H/11479-5

Order Number LM747CN or LM747EN
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
LM747/LM747A	±22V
LM747C/LM747E	±18V
Power Dissipation (Note 1)	800 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LM747/LM747A	−55°C to +125°C
LM747C/LM747E	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM747A/LM747E			LM747			LM747C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$										mV
	$R_S \leq 10\ k\Omega$					1.0	5.0		2.0	6.0	
	$R_S \leq 50\Omega$		0.8	3.0							
	$R_S \leq 50\Omega$			4.0							mV
	$R_S \leq 10\ k\Omega$						6.0			7.5	
Average Input Offset Voltage Drift				15							μV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C, V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
				70		85	500			300	
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25°C, V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$V_S = \pm 20V$	0.5									
Input Voltage Range	$T_A = 25°C$							±12	±13		V
		±12	±13		±12	±13					
Large Signal Voltage Gain	$T_A = 25°C, R_L \geq 2\ k\Omega$ $V_S = \pm 20V, V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V, V_O = \pm 10V$ $R_L \geq 2\ k\Omega$				50	200		20	200		V/mV
	$V_S = \pm 20V, V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V, V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V, V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$										V
	$R_L \geq 10\ k\Omega$	±16									
	$R_L \geq 2\ k\Omega$	±15									
	$V_S = \pm 15V$										V
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
		10		40							
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega, V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\ k\Omega, V_{CM} = \pm 12V$	80	95								

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM747A/LM747E			LM747			LM747C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage Rejection Ratio	$V_S = \pm20V$ to $V_S = \pm5V$										
	$R_S \le 50\Omega$	86	96								dB
	$R_S \le 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current/Amp	$T_A = 25°C$			2.5		1.7	2.8		1.7	2.8	mA
Power Consumption/Amp	$T_A = 25°C$										mW
	$V_S = \pm20V$		80	150							mW
	$V_S = \pm15V$					50	85		50	85	mW
LM747A	$V_S = \pm20V$										mW
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM747E	$V_S = \pm20V$			150							mW
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM747	$V_S = \pm15V$										mW
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

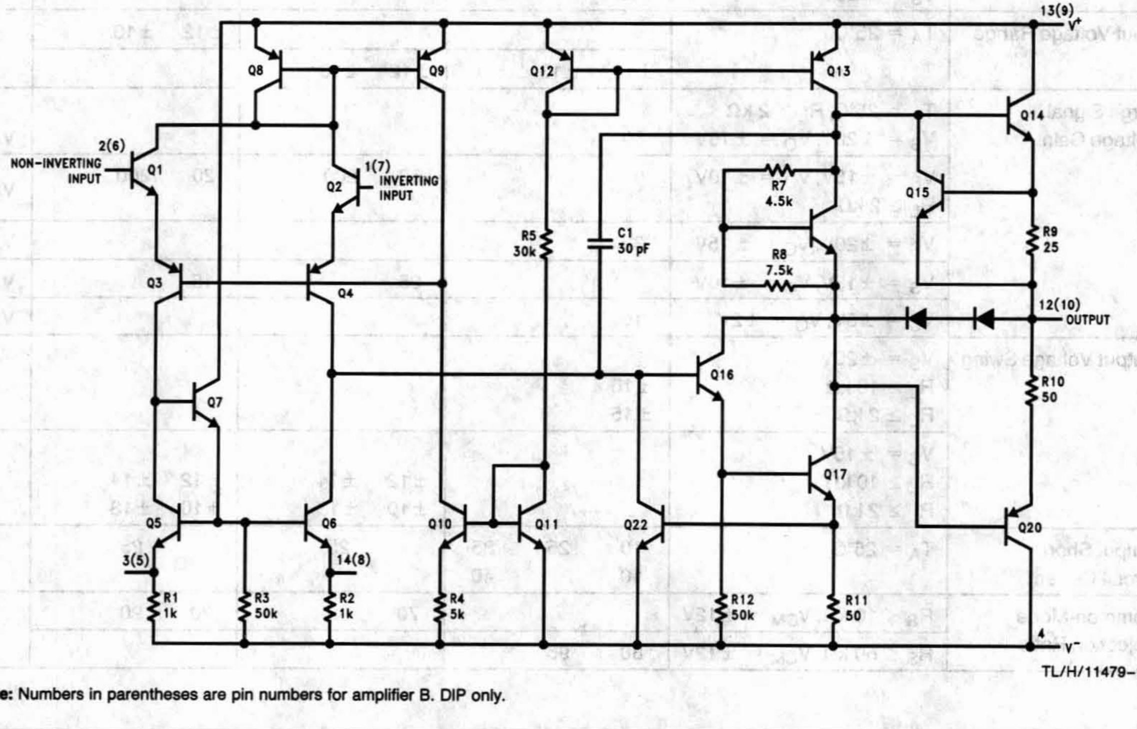
Note 1: The maximum junction temperature of the LM747C/LM747E is 100°C. For operating at elevated temperatures, devies in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm5V \le V_S \le \pm20V$ and $-55°C \le T_A \le 125°C$ for the LM747A and $0°C \le T_A \le 70°C$ for the LM747E unless otherwise specified. The LM747 and LM747C are specified for $V_S = \pm15V$ and $-55°C \le T_A \le 125°C$ and $0°C \le T_A \le 70°C$, respectively, unless otherwise specified.

Note 4: Calculated value from: 0.35/Rise Time (µs).

Schematic Diagram (Each Amplifier)

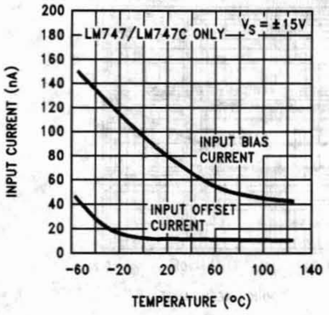

13(9)
V+
Q8
Q9
Q12
Q13
Q14
2(6)
NON-INVERTING
INPUT
Q1
Q2
1(7)
INVERTING
INPUT
Q15
R7
4.5k
R5
30k
C1
30 pF
R8
7.5k
R9
25
Q3
Q4
12(10)
OUTPUT
Q16
Q7
R10
50
Q17
Q5
Q6
Q10
Q11
Q22
Q20
3(5)
14(8)
R1
1k
R3
50k
R2
1k
R4
5k
R12
50k
R11
50
4
V-

TL/H/11479-1

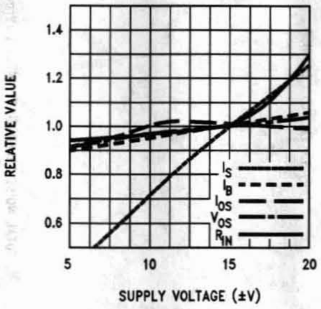
Note: Numbers in parentheses are pin numbers for amplifier B. DIP only.

Typical Performance Characteristics

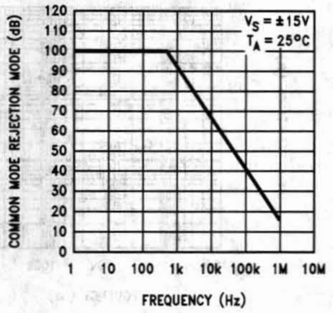
Input Bias and Offset Currents vs Ambient Temperature



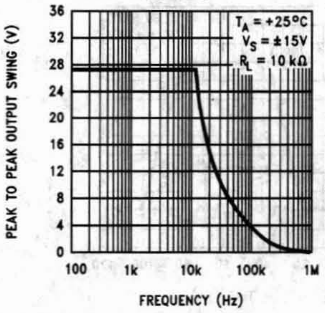
DC Parameters vs Supply Voltage



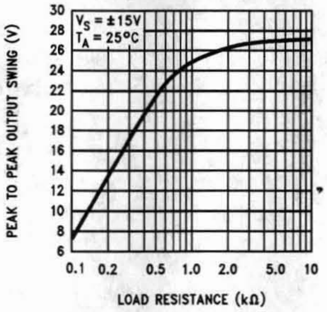
Common Mode Rejection Ratio vs Frequency



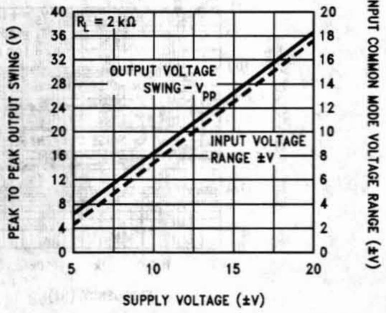
Output Voltage Swing vs Frequency



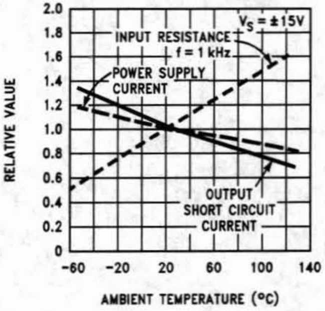
Output Voltage Swing vs Load Resistance



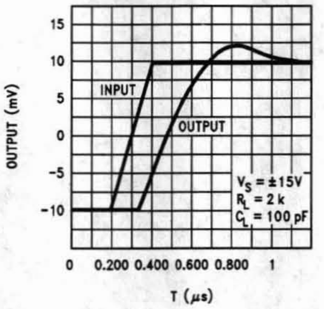
Output Swing and Input Range vs Supply Voltage



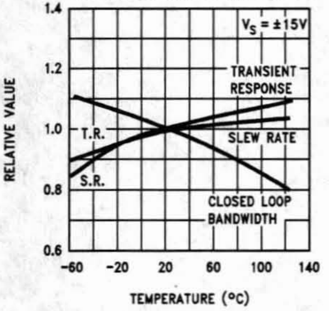
Normalized DC Parameters vs Ambient Temperature



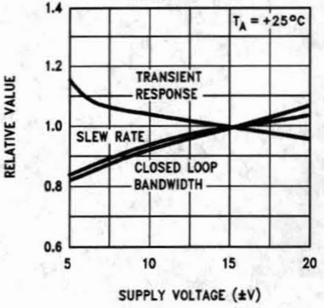
Transient Response



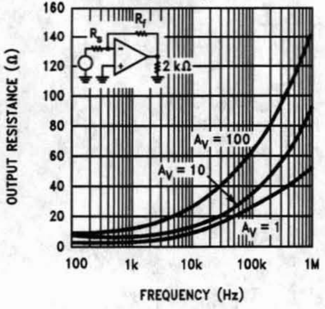
Frequency Characteristics vs Ambient Temperature



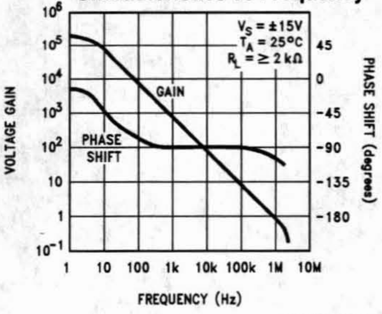
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency

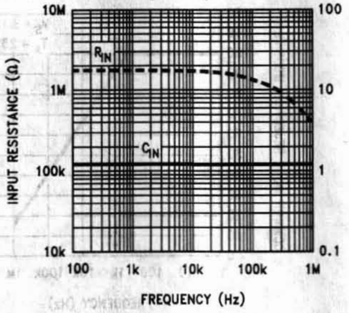


Open Loop Transfer Characteristics vs Frequency

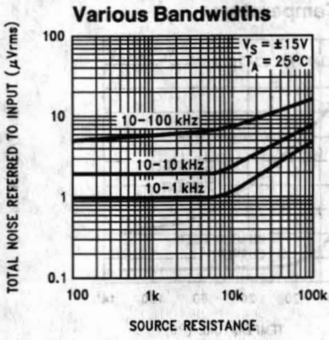


TL/H/11479–2

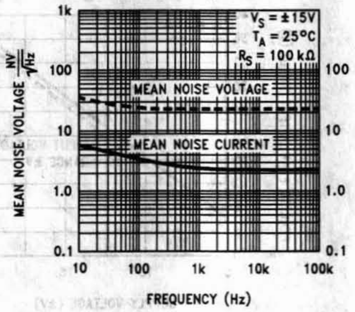
Typical Performance Characteristics (Continued)



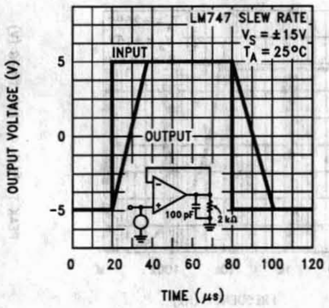
Input Resistance and Input Capacitance vs Frequency



Broadband Noise for Various Bandwidths



Input Noise Voltage and Current vs Frequency



Voltage Follower Large Signal Pulse Response

TL/H/11479–3

National Semiconductor

LM748 Operational Amplifier

General Description

The LM748 is a general purpose operational amplifier with external frequency compensation.

The unity-gain compensation specified makes the circuit stable for all feedback configurations, even with capacitive loads. It is possible to optimize compensation for best high frequency performance at any gain. As a comparator, the output can be clamped at any desired level to make it compatible with logic circuits.

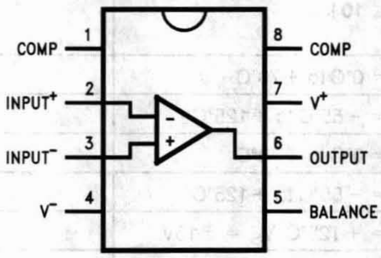
The LM748C is specified for operation over the 0°C to +70°C temperature range.

Features

- Frequency compensation with a single 30 pF capacitor
- Operation from ±5V to ±20V
- Continuous short-circuit protection
- Operation as a comparator with differential inputs as high as ±30V
- No latch-up when common mode range is exceeded
- Same pin configuration as the LM101

Connection Diagram

Dual-In-Line Package



TL/H/11478-2

Top View

Order Number LM748CN
See NS Package Number N08B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	
Operating Temperature Range:	
LM748C	0°C to +70C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Electrical Characteristics (Note 4)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25°C$, $R_S \le 10\ k\Omega$		1.0	5.0	mV
Input Offset Current	$T_A = 25°C$		40	200	nA
Input Bias Current	$T_A = 25°C$		120	500	nA
Input Resistance	$T_A = 25°C$	300	800		kΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		1.8	2.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \ge 2\ k\Omega$	50	160		V/mV
Input Offset Voltage	$R_S \le 10\ k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \le 50\Omega$		3.0		μV/°C
	$R_S \le 10\ k\Omega$		6.0		μV/°C
Input Offset Current	$T_A = 0°C$ to $+70°C$			300	nA
	$T_A = -55°C$ to $+125°C$			500	nA
Input Bias Current	$T_A = 0°C$ to $+70°C$			0.8	μA
	$T_A = -55°C$ to $+125°C$			1.5	μA
Supply Current	$T_A = +125°C$, $V_S = \pm 15V$		1.2	2.25	mA
	$T_A = -55°C$ to $+125°C$		1.9	3.3	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \ge 2\ k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±14		V
	$V_S = \pm 15V$, $R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	77	90		dB

Note 1: For operating at elevated temperatures, the device must be derated based on a maximum junction to case thermal resistance of 45°C per watt, or 150°C per watt junction to ambient. (See Curves).

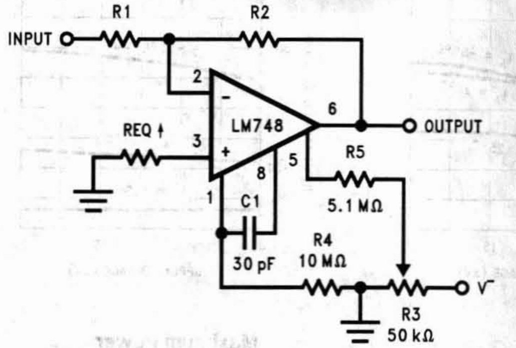
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to +125°C and ambient temperatures to +70°C.

Note 4: These specifications apply for $\pm 5V \le V_S \le +15V$ and $0°C \le T_A \le +70°C$, unless otherwise specified.

Typical Applications

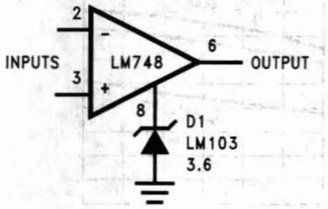
Inverting Amplifier with Balancing Circuit


R1
R2
INPUT
2
REQ †
3
LM748
6
OUTPUT
8
5
R5
5.1 MΩ
1
C1
30 pF
R4
10 MΩ
R3
50 kΩ
V⁻

†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

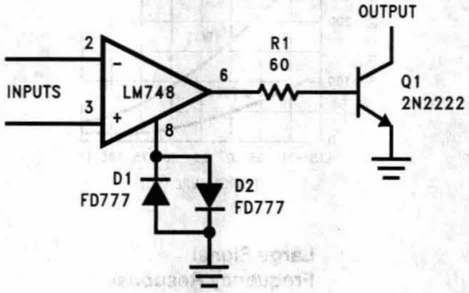
TL/H/11478–3

Voltage Comparator for Driving DTL or TTL Integrated Circuits


2
INPUTS
3
LM748
6
OUTPUT
8
D1
LM103
3.6

TL/H/11478–4

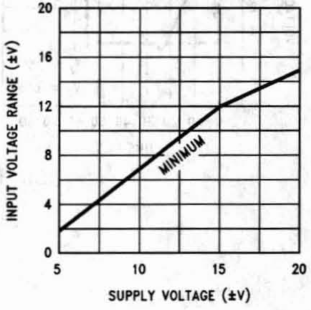
Voltage Comparator for Driving RTL Logic or High Current Driver


OUTPUT
2
INPUTS
3
LM748
6
8
R1
60
Q1
2N2222
D1
FD777
D2
FD777

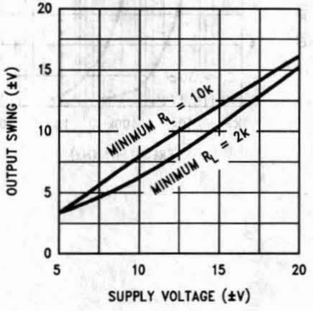
TL/H/11478–5

Guaranteed Performance Characteristics (Note 4)

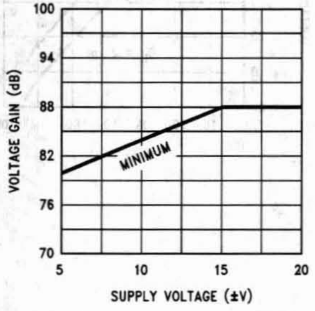
Input Voltage Range



Output Swing



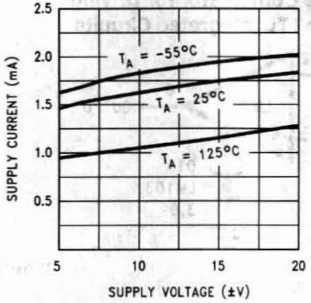
Voltage Gain



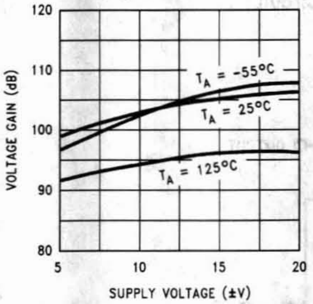
TL/H/11478–6

Typical Performance Characteristics

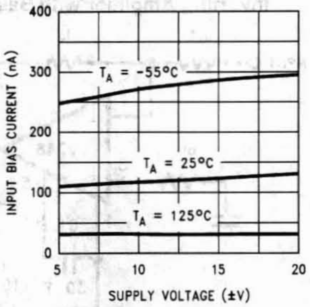
Supply Current



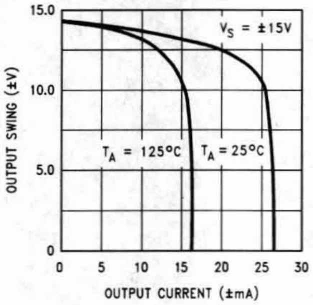
Voltage Gain



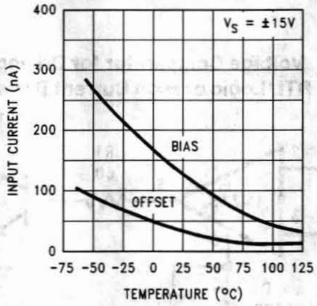
Input Bias Current



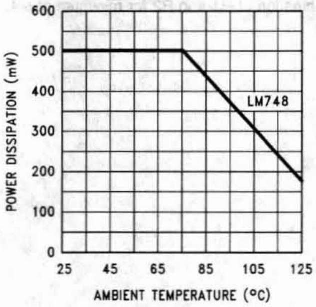
Current Limiting



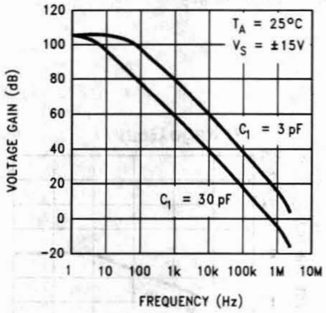
Input Current



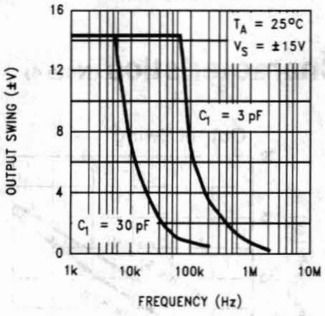
Maximum Power Dissipation



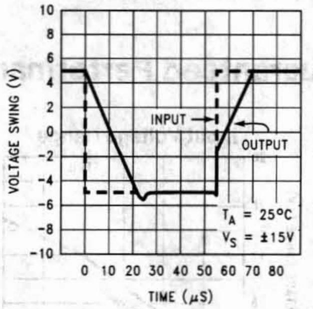
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



TL/H/11478-7

National Semiconductor

LM759/LM77000 Power Operational Amplifiers

General Description

The LM759 and LM77000 are high performance operational amplifiers that feature high output current capability. The LM759 is capable of providing 325 mA and the LM77000 providing 250 mA. Both amplifiers feature small signal characteristics that are better than the LM741. The amplifiers are designed to operate from a single or dual power supply with an input common mode range that includes the negative supply. The high gain and high output power provide superior performance. Internal current limiting, thermal shutdown, and safe area compensation are employed making the LM759 and LM77000 essentially indestructible.

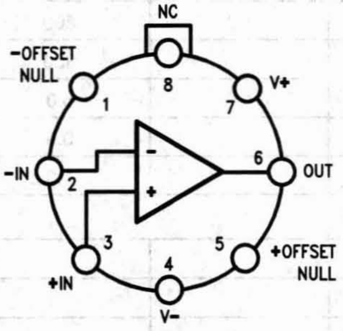
Features

- Output current
  - LM759—325 mA minimum
  - LM77000—250 mA minimum
- Internal short circuit current limiting
- Internal thermal overload protection
- Internal output transistors safe-area protection
- Input common mode voltage range includes ground or negative supply

Applications

- Voltage regulators
- Audio amplifiers
- Servo amplifiers
- Power drivers

Connection Diagrams and Ordering Information

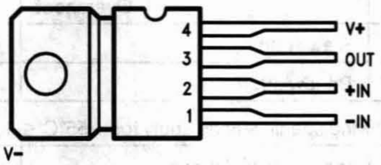


TL/H/10075–1

Lead 4 connected to case.

Top View

Order Number LM759MH, LM759CH or LM759H/883
See NS Package Number H08C



TL/H/10075–2

Top View

Order Number LM759CP or LM77000CP
See NS Package Number P04A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Metal Can	−65°C to +175°C
Plastic Package	−65°C to +150°C
Operating Junction Temperature Range	
Military (LM759M)	−55°C to +150°C
Commercial (LM759C, LM77000C)	0°C to +125°C
Lead Temperature	
Metal Can (soldering, 60 sec)	300°C
Plastic Package (soldering, 10 sec)	265°C
Internal Power Dissipation (Note 1)	Internally Limited
Supply Voltage	±18V
Differential Input Voltage	30V
Input Voltage (note 2)	±15V

LM759
Electrical Characteristics $T_J = 25°C, V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	3.0	mV
I_{IO}	Input Offset Current			5.0	30	nA
I_{IB}	Input Bias Current			50	150	nA
Z_I	Input Impedance		0.25	1.5		MΩ
I_{CC}	Supply Current			12	18	mA
V_{IR}	Input Voltage Range		$V^+ - 2V$ to V^-	$V^+ - 2V$ to V^-		V
I_{OS}	Output Short Circuit Current	$\lvert V_{CC} - V_O \rvert = 30V$		±200		mA
$I_{O\ PEAK}$	Peak Output Current	$3.0V \leq \lvert V_{CC} - V_O \rvert \leq 10V$	±325	±500		mA
A_{VS}	Large Signal Voltage Gain	$R_L \geq 50\Omega, V_O = \pm 10V$	50	200		V/mV
TR	Transient Response — Rise Time	$R_L = 50\Omega, A_V = 1.0$		300		ns
	Transient Response — Overshoot			5.0		%
SR	Slew Rate	$R_L = 50\Omega, A_V = 1.0$		0.6		V/μs
BW	Bandwidth	$A_V = 1.0$		1.0		MHz
The following specifications apply for $-55°C \leq T_J \leq +150°C$						
V_{IO}	Input Offset Voltage	$R_S \leq 10\ k\Omega$			4.5	mV
I_{IO}	Input Offset Current				60	nA
I_{IB}	Input Bias Current				300	nA
CMRR	Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	80	100		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$	80	100		dB
A_{VS}	Large Signal Voltage Gain	$R_L \geq 50\Omega, V_O = \pm 10V$	25	200		V/mV
V_{OP}	Output Voltage Swing	$R_L = 50\Omega$	±10	±12.5		V

LM759C

Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current				5.0	50	nA
I_{IB}	Input Bias Current				50	250	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			$V^+ - 2V$ to V^-	$V^+ - 2V$ to V^-		V
I_{OS}	Output Short Circuit Current		$\lvert V_{CC} - V_O \rvert = 30V$		±200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0V \leq \lvert V_{CC} - V_O \rvert \leq 10V$	±325	±500		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
TR	Transient Response	Rise Time	$R_L = 50\Omega$, $A_V = 1.0$		300		ns
		Overshoot			10		%
SR	Slew Rate		$R_L = 50\Omega$, $A_V = 1.0$		0.5		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz
The following specifications apply for $0° \leq T_J \leq +125°C$							
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			7.5	mV
I_{IO}	Input Offset Current					100	nA
I_{IB}	Input Bias Current					400	nA
CMRR	Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	70	100		dB
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 50\Omega$	±10	±12.5		V

LM77000

Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage		$R_S \le 10\ k\Omega$		1.0	8.0	mV
I_{IO}	Input Offset Current				5.0	50	nA
I_{IB}	Input Bias Current				50	250	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			$+13$ to V^-	$+13$ to V^-		V
I_{OS}	Output Short Circuit Current		$\lvert V_{CC}-V_O \rvert = 30V$		±200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0V \le \lvert V_{CC}-V_O \rvert \le 10V$	±250	±400		mA
A_{VS}	Large Signal Voltage Gain		$R_L \ge 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
TR	Transient Response	Rise Time	$R_L = 50\Omega$, $A_V = 1.0$		300		ns
		Overshoot			10		%
SR	Slew Rate		$R_L = 50\Omega$, $A_V = 1.0$		0.5		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz

The following specifications apply for $0° \le T_J \le +125°C$

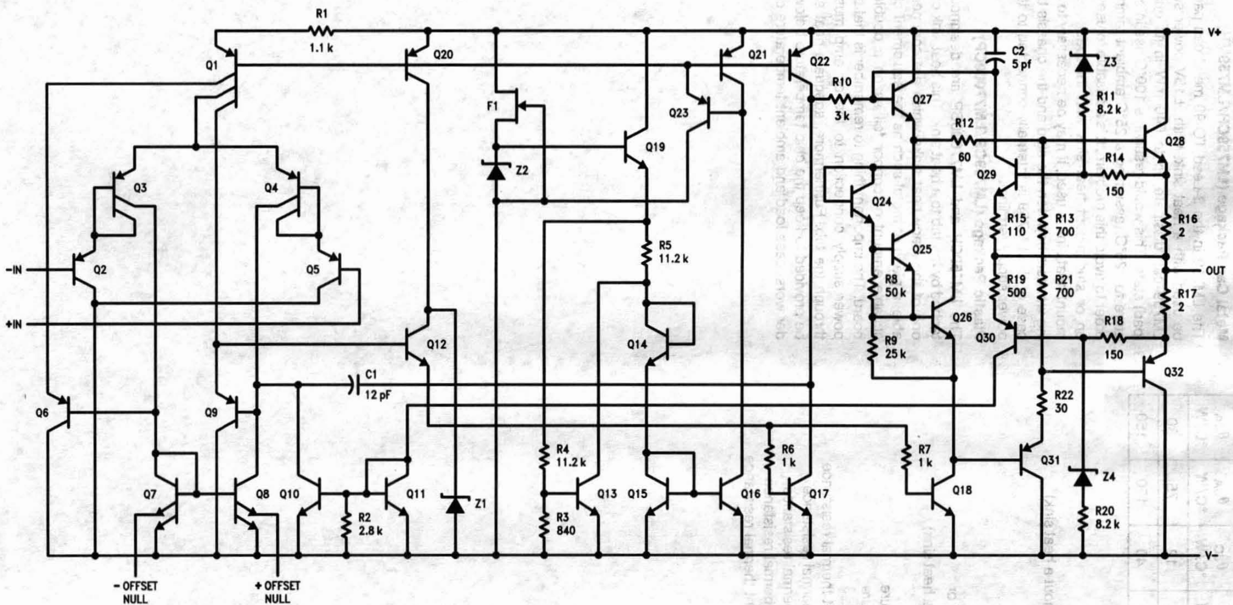
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage	$R_S \le 10\ k\Omega$			10	mV
I_{IO}	Input Offset Current				100	nA
I_{IB}	Input Bias Current				400	nA
CMR	Common Mode Rejection	$R_S \le 10\ k\Omega$	70	100		dB
PSRR	Power Supply Rejection Ratio	$R_S \le 10\ k\Omega$	80	100		dB
A_{VS}	Large Signal Voltage Gain	$R_L \ge 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
V_{OP}	Output Voltage Swing	$R_L = 50\Omega$	±10	±12.5		V

Note 1: Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, use the thermal resistance values which follow the Equivalent Circuit Schematic.

Note 2: For a supply voltage less than 30V between V^+ and V^-, the absolute maximum input voltage is equal to the supply voltage.

Note 3: For military electrical specifications RETS759X are available for LM759H.

Equivalent Circuit


V+
V−
OUT
−IN
+IN
− OFFSET NULL
+ OFFSET NULL
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
F1
Z1
Z2
Z3
Z4
C1 12 pF
C2 5 pf
R1 1.1 k
R2 2.8 k
R3 840
R4 11.2 k
R5 11.2 k
R6 1 k
R7 1 k
R8 50 k
R9 25 k
R10 3 k
R11 8.2 k
R12 60
R13 700
R14 150
R15 110
R16 2
R17 2
R18 150
R19 500
R20 8.2 k
R21 700
R22 30

TL/H/10075–3

Note: All resistor values in ohms.

Package	Typ θ_{JC} °C/W	Max θ_{JC} °C/W	Typ θ_{JA} °C/W	Max θ_{JA} °C/W
Plastic Package (P)	8.0	12	75	80
Metal Can (H)	30	40	120	150

$$P_{D\,Max} = \frac{T_{J\,Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$= \frac{T_{J\,Max} - T_A}{\theta_{JA}} \text{ (without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving T_J:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CA}) \text{ or}$$

$$= T_A + P_D\theta_{JA} \text{ (without a heat sink)}$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction to ambient thermal resistance
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink thermal resistance
θ_{SA} = Heat sink to ambient thermal resistance

Mounting Hints

Metal Can Package (LM759CH/LM759MH)

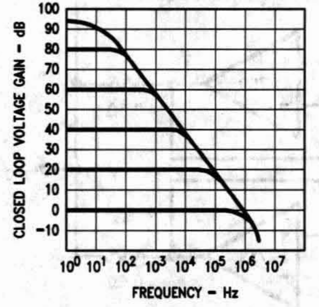
The LM759 in the 8-Lead TO-99 metal can package must be used with a heat sink. With ±15V power supplies, the LM759 can dissipate up to 540 mW in its quiescent (no load) state. This would result in a 100°C rise in chip temperature to 125°C (assuming a 25°C ambient temperature). In order to avoid this problem, it is advisable to use either a slip on or stud mount heat sink with this package. If a stud mount heat sink is used, it may be necessary to use insulating washers between the stud and the chassis because the case of the LM759 is internally connected to the negative power supply terminal.

Plastic Package (LM759CP/LM77000CP)

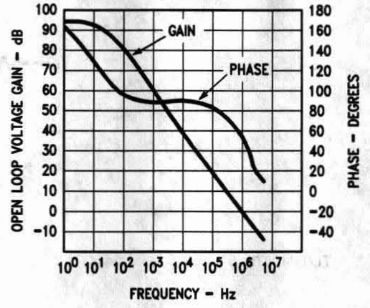
The LM759CP and LM77000CP are designed to be attached by the tab to a heat sink. This heat sink can be either one of the many heat sinks which are commercially available, a piece of metal such as the equipment chassis, or a suitable amount of copper foil as on a double sided PC board. The important thing to remember is that the negative power supply connection to the op amp must be made through the tab. Furthermore, adequate heat sinking must be provided to keep the chip temperature below 125°C under worst case load and ambient temperature conditions.

Typical Performance Characteristics

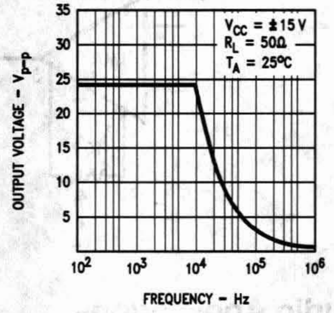
Frequency Response for Various Closed Loop Gains



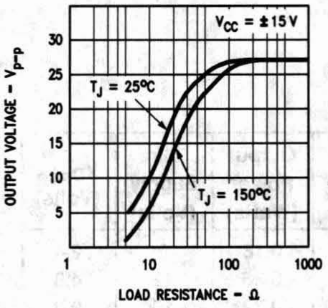
Open Loop vs Frequency Response



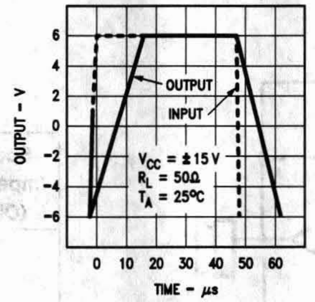
Output Voltage vs Frequency



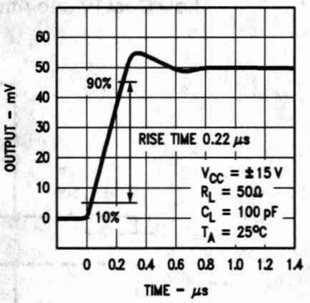
Output Voltage vs Load Resistance



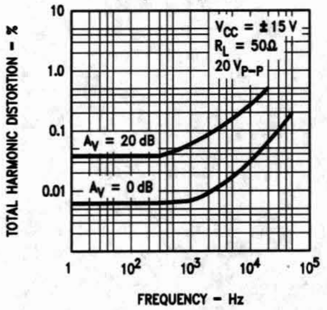
Voltage Follower Large Signal Pulse Response



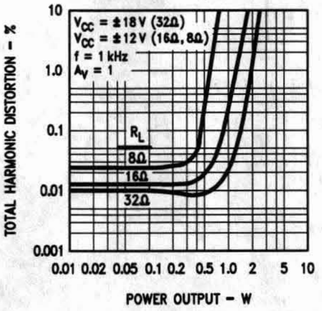
Voltage Follower Transient Response



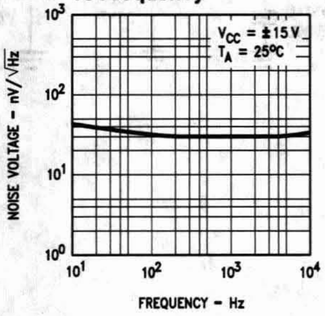
Total Harmonic Distortion vs Frequency



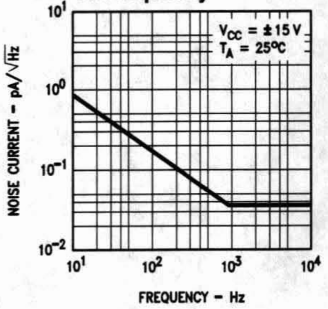
Total Harmonic Distortion vs Power Output



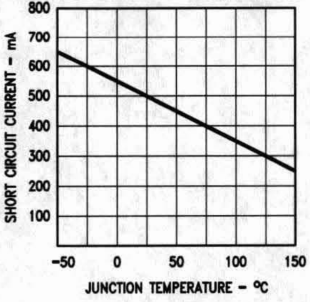
Input Noise Voltage vs Frequency



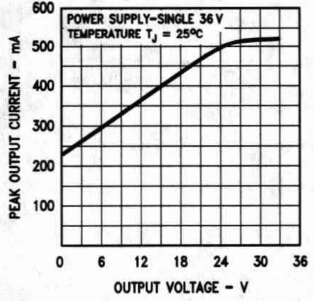
Noise Current vs Frequency



Short Circuit Current vs Junction Temperature



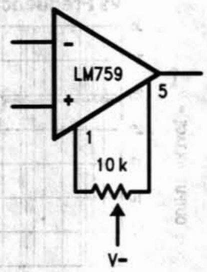
Peak Output Current vs Output Voltage



TL/H/10075–4

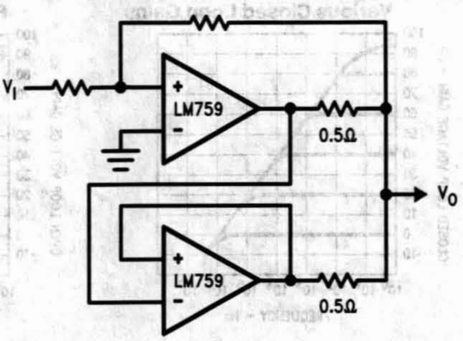
Applications

Offset Null Circuit


-
+
LM759
5
1
10 k
V-

TL/H/10075-5

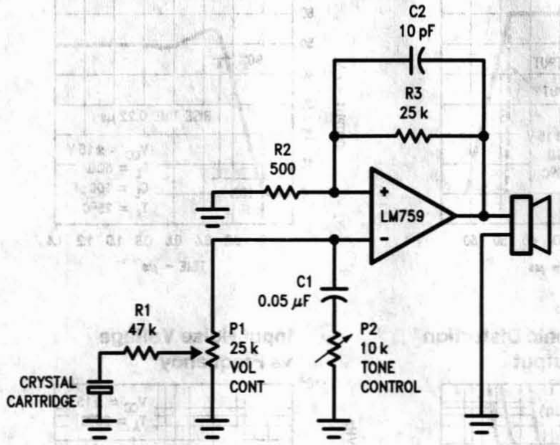
Paralleling LM759 Power Op Amps


V$_I$
+
LM759
-
0.5Ω
V$_O$
+
LM759
-
0.5Ω

TL/H/10075-6

Audio Applications

Low Cost Phono Amplifier

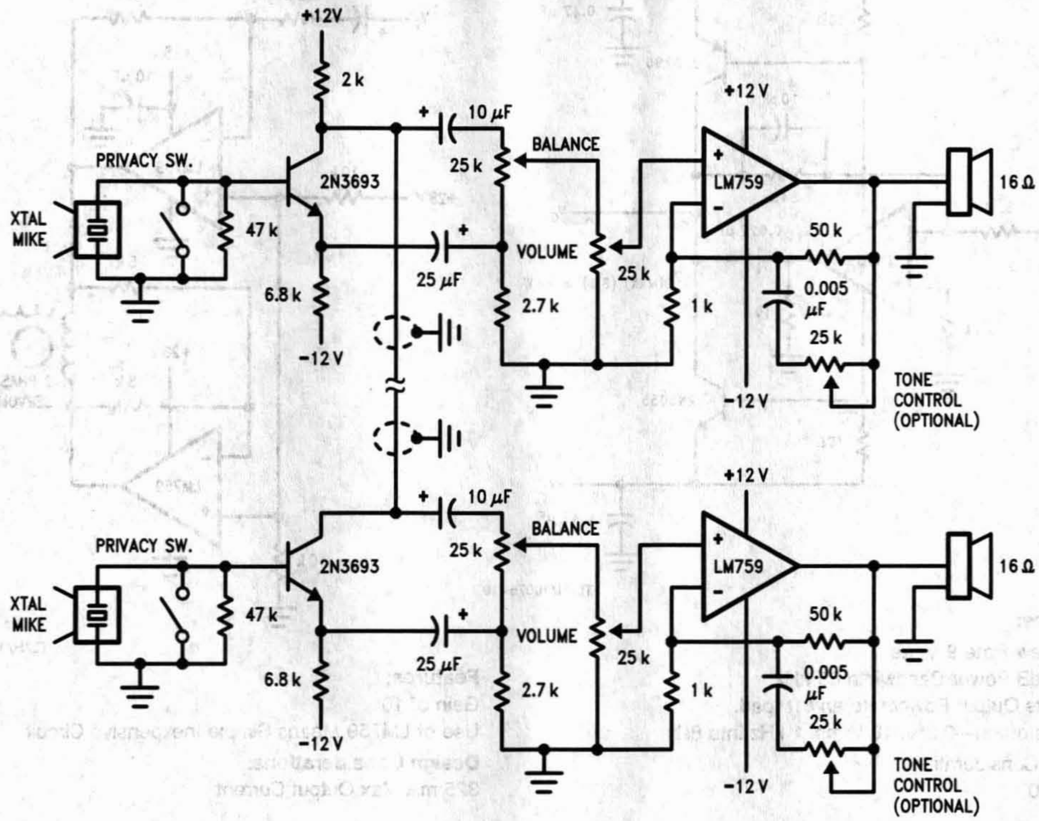

C2
10 pF
R3
25 k
R2
500
+
LM759
-
C1
0.05 μF
R1
47 k
P1
25 k
VOL
CONT
P2
10 k
TONE
CONTROL
CRYSTAL
CARTRIDGE

TL/H/10075-7

Speaker Impedance (Ohms)	Output Power (Watts)	Min Supply (Volts)	V_{Op-p} (Volts)
4	0.18	9	2.4
8	0.36	12	4.8
16	0.72	15	9.6
32	1.44	25	19.2

Applications (Continued)

Bi-Directional Intercom System Using the LM759 Power Op Amp


+12V
2 k
10 µF
BALANCE
25 k
PRIVACY SW.
2N3693
XTAL
MIKE
47 k
25 µF
VOLUME
25 k
6.8 k
2.7 k
-12 V
+12 V
LM759
16 Ω
50 k
0.005 µF
1 k
25 k
TONE
CONTROL
(OPTIONAL)
-12 V
+12 V
10 µF
BALANCE
25 k
PRIVACY SW.
2N3693
LM759
16 Ω
XTAL
MIKE
47 k
50 k
25 µF
VOLUME
25 k
6.8 k
0.005 µF
2.7 k
1 k
25 k
-12 V
-12 V
TONE
CONTROL
(OPTIONAL)

TL/H/10075-9

Features:

Circuit Simplicity

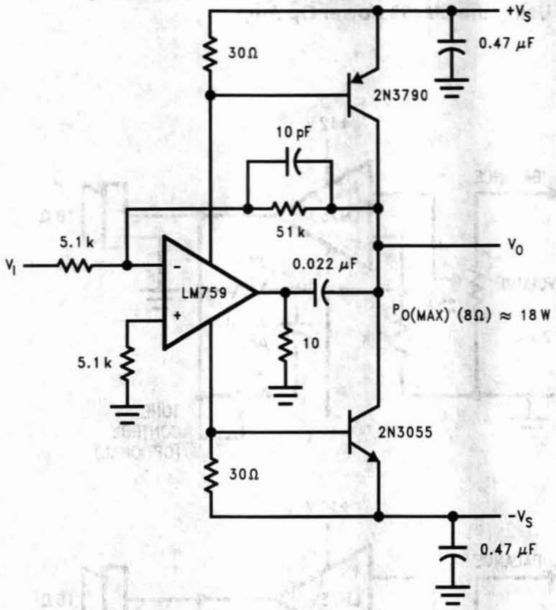
1 Watt of Audio Output

Duplex operation with only one two-wire cable as interconnect.

Note 1: All resistor values in ohms.

Applications (Continued)

High Slew Rate Power Op Amp/Audio Amp


+V_S
0.47 μF
30Ω
2N3790
10 pF
51 k
5.1 k
V_I
LM759
V_O
0.022 μF
10
P_O(MAX) (8Ω) ≈ 18 W
5.1 k
2N3055
30Ω
-V_S
0.47 μF

TL/H/10075-10

Features:

High Slew Rate 9 V/μs

High 3 dB Power Bandwidth 85 kHz

18 Watts Output Power into an 8Ω load.

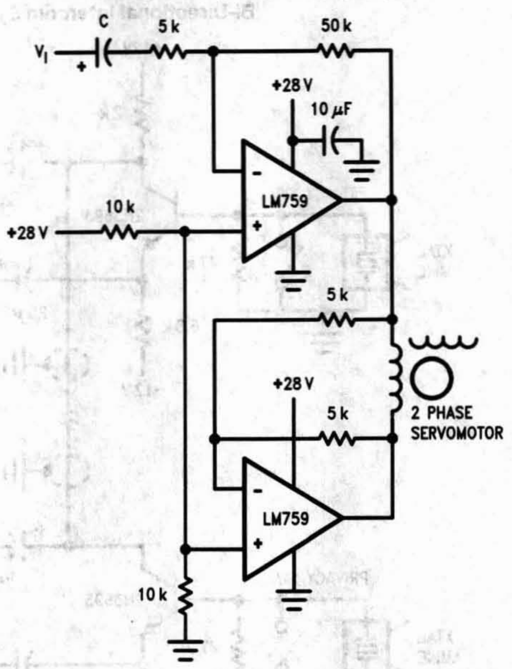
Low Distortion—0.2%, 10 Vrms, 1 kHz into 8Ω

Design Consideration

$A_V \geq 10$

Servo Applications

AG Servo Amplifier—Bridge Type


V_I
C
5 k
50 k
+28 V
10 μF
LM759
10 k
+28 V
5 k
+28 V
5 k
2 PHASE SERVOMOTOR
LM759
10 k

TL/H/10075-11

Features:

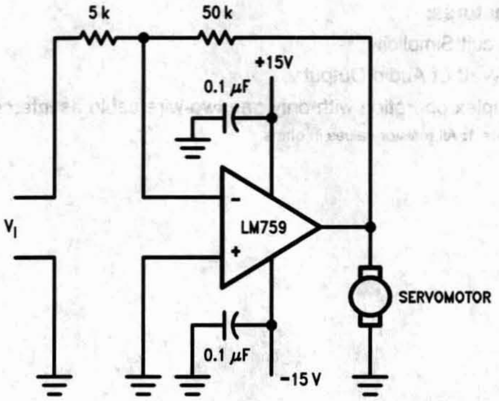
Gain of 10

Use of LM759 Means Simple Inexpensive Circuit

Design Considerations:

325 mA Max Output Current

DC Servo Amplifier


5 k
50 k
+15V
0.1 μF
V_I
LM759
SERVOMOTOR
0.1 μF
-15 V

TL/H/10075-12

Features:

Circuit Simplicity

One Chip Means Excellent Reliability

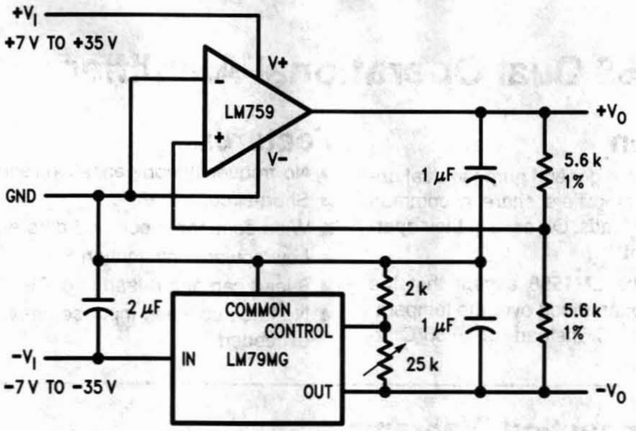
Design Considerations

$I_O \leq 325$ mA

Note 1: All resistor values in ohms.

Regulator Applications

Adjustable Dual Tracking Regulator


+V_I
+7 V TO +35 V
LM759
V+
V−
−
+
GND
+V_O
1 µF
5.6 k
1%
2 µF
COMMON
CONTROL
IN
LM79MG
OUT
2 k
1 µF
25 k
5.6 k
1%
−V_I
−7 V TO −35 V
−V_O

TL/H/10075–13

Features:

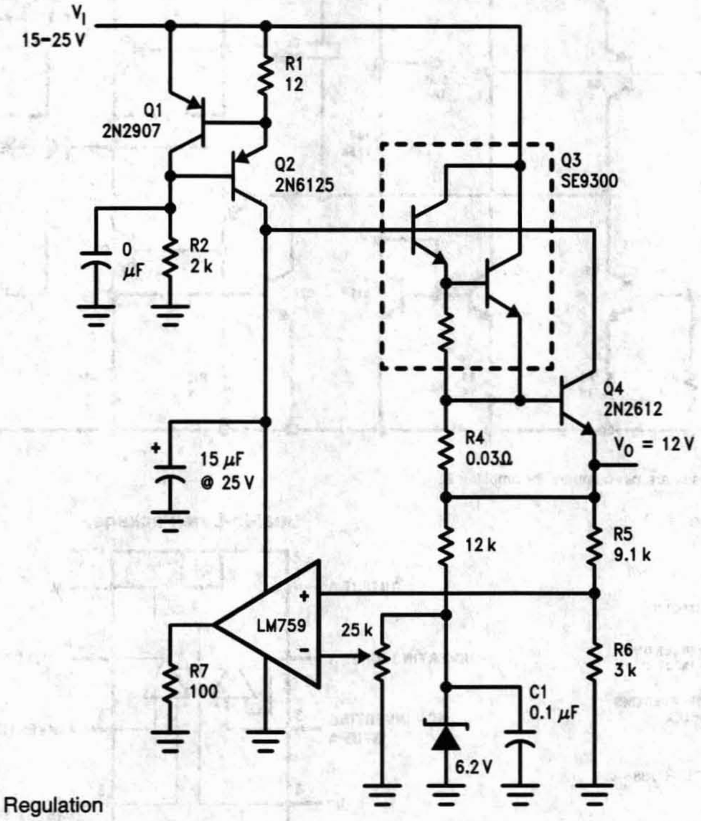
Wide Output Voltage Range (±2.2V to ±30V)

Excellent Load Regulation $\Delta V_O < \pm 5$ mV for $\Delta I_O = \pm 0.2$ A

Excellent Line Regulation $\Delta V_O < \pm 2$ mV for $\Delta V_I = 10V$

Note 1: All resistor values in ohms.

10 Amp — 12 Volt Regulator


V_I
15–25 V
R1
12
Q1
2N2907
Q2
2N6125
0 µF
R2
2 k
Q3
SE9300
Q4
2N2612
V_O = 12 V
R4
0.03Ω
15 µF
@ 25 V
12 k
R5
9.1 k
LM759
+
−
25 k
R7
100
R6
3 k
C1
0.1 µF
6.2 V

TL/H/10075–14

Features:

Excellent Load and Line Regulation

Excellent Temperature Coefficient-Depends Largely on Tempco of the Reference Zener

Note 1: All resistor values in ohms.

National Semiconductor

LM1558/LM1458 Dual Operational Amplifier

General Description

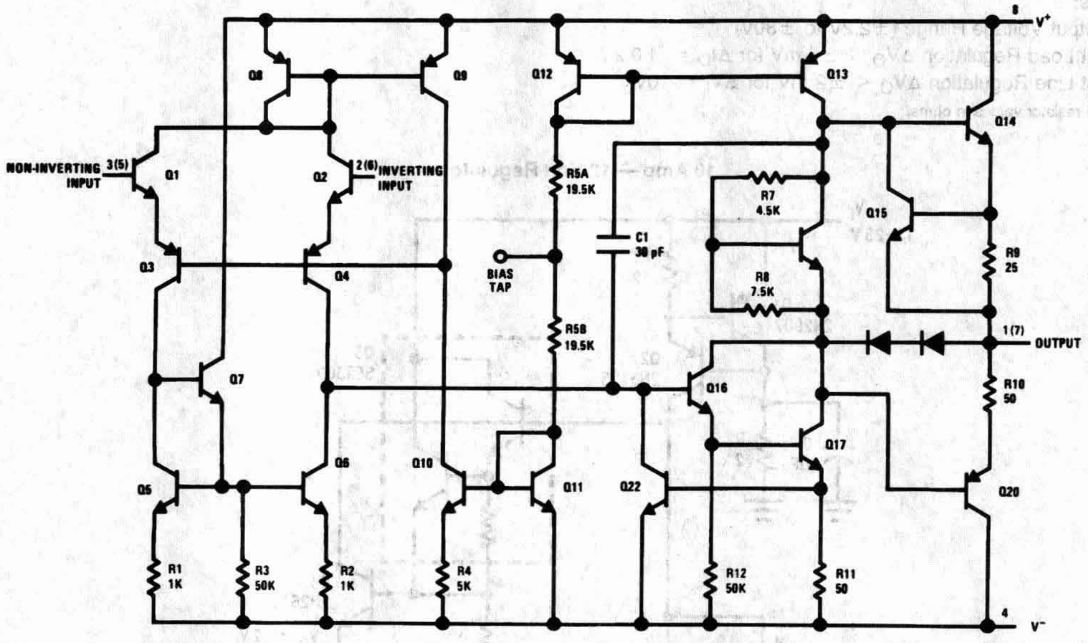
The LM1558 and the LM1458 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

The LM1458 is identical to the LM1558 except that the LM1458 has its specifications guaranteed over the temperature range from 0°C to +70°C instead of −55°C to +125°C.

Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead can and 8-lead mini DIP
- No latch up when input common mode range is exceeded

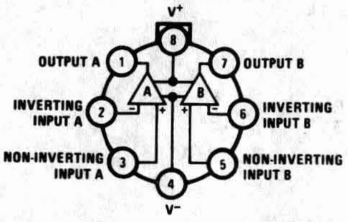
Schematic and Connection Diagrams


8
V+
Q8
Q9
Q12
Q13
Q14
NON-INVERTING INPUT
3(5)
Q1
Q2
2(6)
INVERTING INPUT
R5A 19.5K
R7 4.5K
Q15
C1 30 pF
Q3
Q4
BIAS TAP
R8 7.5K
R9 25
R5B 19.5K
1(7)
OUTPUT
Q7
Q16
R10 50
Q17
Q6
Q10
Q11
Q22
Q5
Q20
R1 1K
R3 50K
R2 1K
R4 5K
R12 50K
R11 50
4
V−

TL/H/7886–1

Note: Numbers in parentheses are pin numbers for amplifier B.

Metal Can Package

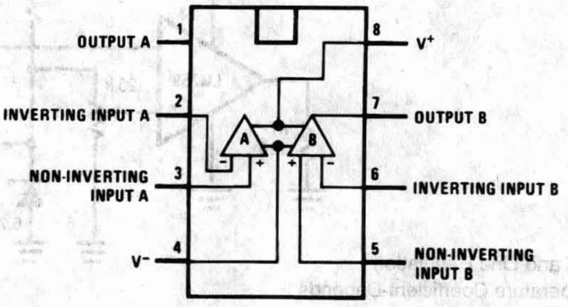

V+
8
OUTPUT A
1
7
OUTPUT B
A
B
INVERTING INPUT A
2
6
INVERTING INPUT B
NON-INVERTING INPUT A
3
5
NON-INVERTING INPUT B
4
V−

TL/H/7886–2

Top View

Order Number LM1558H, LM1558H/883 or LM1458H
See NS Package Number H08C

Dual-In-Line Package


OUTPUT A
1
8
V+
INVERTING INPUT A
2
7
OUTPUT B
A
B
NON-INVERTING INPUT A
3
6
INVERTING INPUT B
V−
4
5
NON-INVERTING INPUT B

TL/H/7886–3

Top View

Order Number LM1558J, LM1558J/883, LM1458J, LM1458M or LM1458N
See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Supply Voltage	
LM1558	±22V
LM1458	±18V
Power Dissipation (Note 1)	
LM1558H/LM1458H	500 mW
LM1458N	400 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LM1558	−55°C to +125°C
LM1458	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 5)	300V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM1558			LM1458			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C, R_S \le 10\ k\Omega$		1.0	5.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		80	200		80	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current Both Amplifiers	$T_A = 25°C, V_S = \pm 15V$		3.0	5.0		3.0	5.6	mA
Large Signal Voltage Gain	$T_A = 25°C, V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \ge 2\ k\Omega$	50	160		20	160		V/mV
Input Offset Voltage	$R_S \le 10\ k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \ge k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V, R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	77	96		77	96		dB

Note 1: The maximum junction temperature of the LM1558 is 150°C, while that of the LM1458 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 20°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 187°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \le T_A \le 125°C$, unless otherwise specified. With the LM1458, however, all specifications are limited to $0°C \le T_A \le 70°C$ and $V_S = \pm 15V$.

Note 4: Refer to RETS 1558V for LM1558J and LM1558H military specifications.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM1875 20W Audio Power Amplifier

General Description

The LM1875 is a monolithic power amplifier offering very low distortion and high quality performance for consumer audio applications.

The LM1875 delivers 20 watts into a 4Ω or 8Ω load on ±25V supplies. Using an 8Ω load and ±30V supplies, over 30 watts of power may be delivered. The amplifier is designed to operate with a minimum of external components. Device overload protection consists of both internal current limit and thermal shutdown.

The LM1875 design takes advantage of advanced circuit techniques and processing to achieve extremely low distortion levels even at high output power levels. Other outstanding features include high gain, fast slew rate and a wide power bandwidth, large output voltage swing, high current capability, and a very wide supply range. The amplifier is internally compensated and stable for gains of 10 or greater.

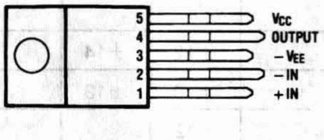
Features

- Up to 30 watts output power
- A_{VO} typically 90 dB
- Low distortion: 0.015%, 1 kHz, 20 W
- Wide power bandwidth: 70 kHz
- Protection for AC and DC short circuits to ground
- Thermal protection with parole circuit
- High current capability: 4A
- Wide supply range 16V-60V
- Internal output protection diodes
- 94 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance audio systems
- Bridge amplifiers
- Stereo phonographs
- Servo amplifiers
- Instrument systems

Connection Diagram

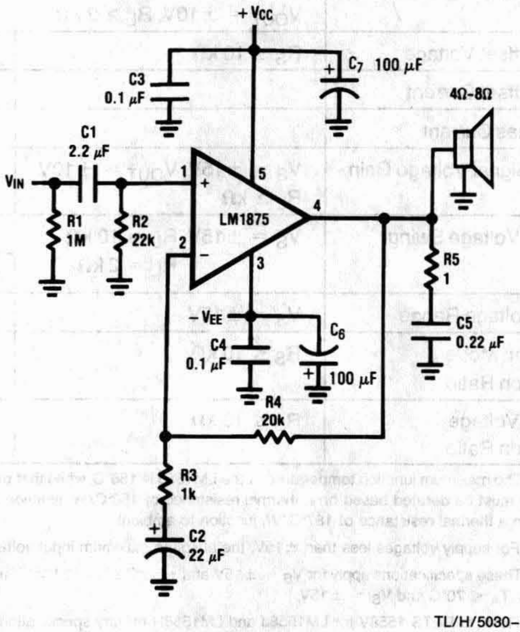


TL/H/5030–1

Front View

Order Number LM1875T
See NS Package Number T05B

Typical Applications



TL/H/5030–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	60V
Input Voltage	$-V_{EE}$ to V_{CC}
Storage Temperature	$-65°C$ to $+150°C$
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	260°C
θ_{JC}	3°C
θ_{JA}	73°C

Electrical Characteristics

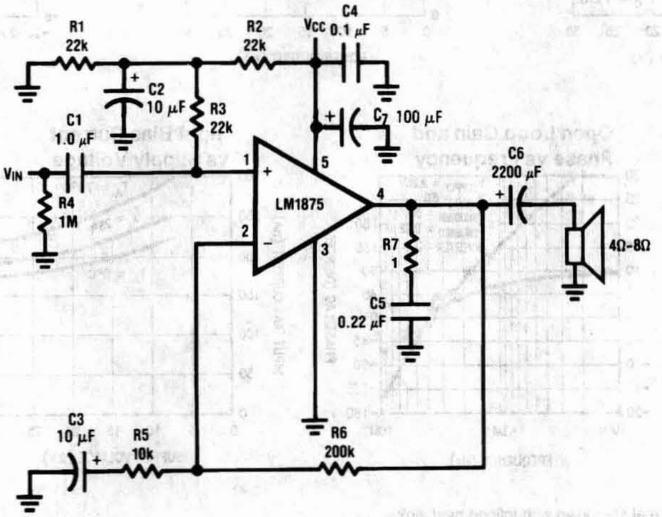
$V_{CC} = +25V$, $-V_{EE} = -25V$, $T_{AMBIENT} = 25°C$, $R_L = 8\Omega$, $A_V = 20$ (26 dB), $f_o = 1$ kHz, unless otherwise specified.

Parameter	Conditions	Typical	Tested Limits	Units
Supply Current	$P_{OUT} = 0W$	70	100	mA
Output Power (Note 1)	THD = 1%	25		W
THD (Note 1)	$P_{OUT} = 20W$, $f_o = 1$ kHz	0.015		%
	$P_{OUT} = 20W$, $f_o = 20$ kHz	0.05	0.4	%
	$P_{OUT} = 20W$, $R_L = 4\Omega$, $f_o = 1$ kHz	0.022		%
	$P_{OUT} = 20W$, $R_L = 4\Omega$, $f_o = 20$ kHz	0.07	0.6	%
Offset Voltage		±1	±15	mV
Input Bias Current		±0.2	±2	μA
Input Offset Current		0	±0.5	μA
Gain-Bandwidth Product	$f_o = 20$ kHz	5.5		MHz
Open Loop Gain	DC	90		dB
PSRR	V_{CC}, 1 kHz, 1 Vrms	95	52	dB
	V_{EE}, 1 kHz, 1 Vrms	83	52	dB
Max Slew Rate	20W, 8Ω, 70 kHz BW	8		V/μs
Current Limit	$V_{OUT} = V_{SUPPLY} - 10V$	4	3	A
Equivalent Input Noise Voltage	$R_S = 600\Omega$, CCIR	3		μVrms

Note 1: Assumes the use of a heat sink having a thermal resistance of 1°C/W and no insulator with an ambient temperature of 25°C. Because the output limiting circuitry has a negative temperature coefficient, the maximum output power delivered to a 4Ω load may be slightly reduced when the tab temperature exceeds 55°C.

Typical Applications (Continued)

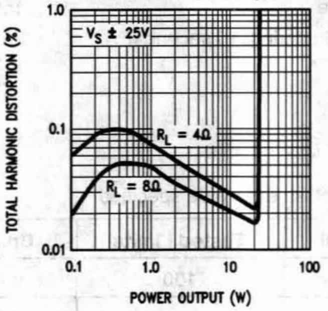
Typical Single Supply Operation



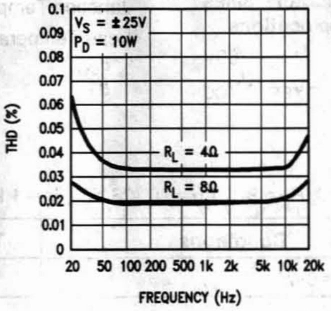
TL/H/5030-3

Typical Performance Characteristics

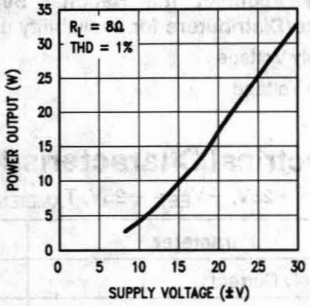
THD vs Power Output



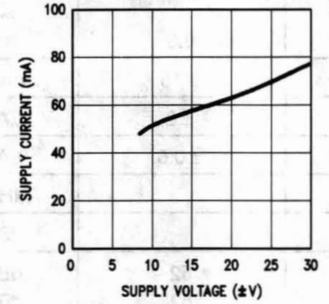
THD vs Frequency



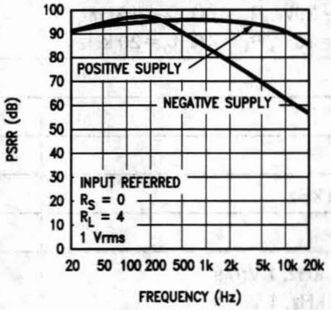
Power Output vs Supply Voltage



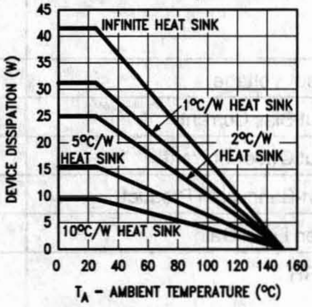
Supply Current vs Supply Voltage



PSRR vs Frequency

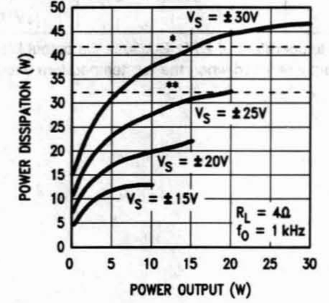


Device Dissipation vs Ambient Temperature†

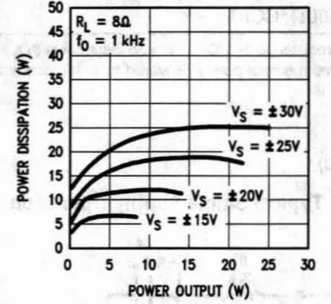


†ϕINTERFACE = 1°C/W.
See Application Hints.

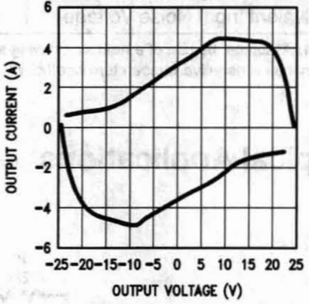
Power Dissipation vs Power Output



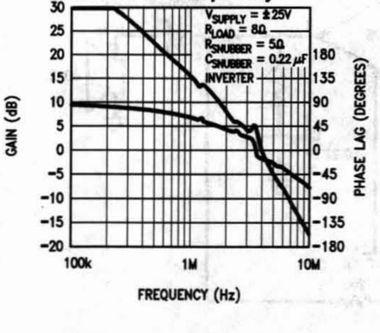
Power Dissipation vs Power Output



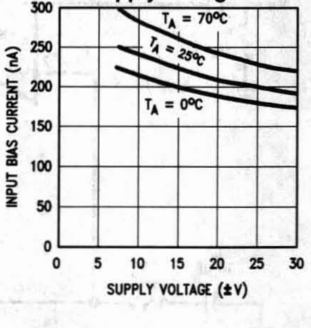
I_{OUT} vs V_{OUT}-Current Limit/ Safe Operating Area Boundary



Open Loop Gain and Phase vs Frequency



Input Bias Current vs Supply Voltage

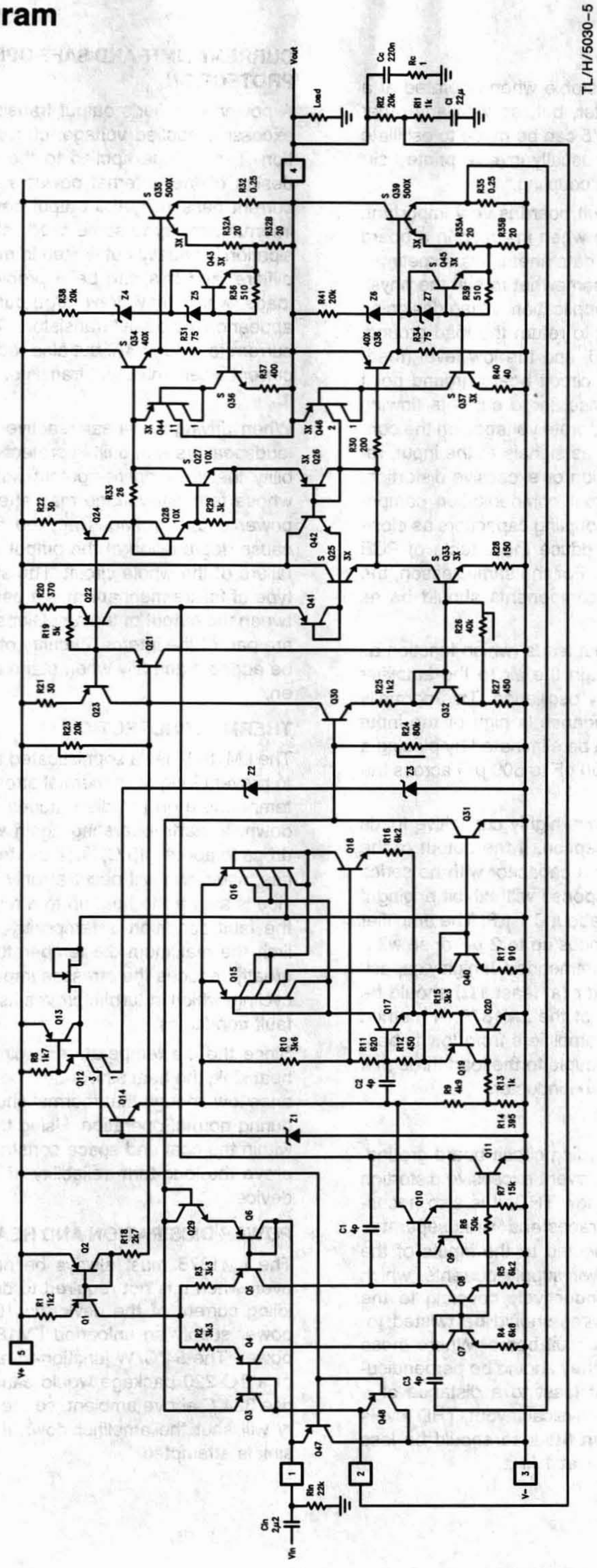


TL/H/5030–4

*Thermal shutdown with infinite heat sink

**Thermal shutdown with 1°C/W heat sink

Schematic Diagram


Vout
Load
Cc 220n
Rc 1
R2 20k
R1 1k
Ci 22μ
TL/H/5030-5
4
5
V+
V−
3
1
2
Vin
Cin 2μ2
Rin 22k
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
Q37
Q38
Q39
Q40
Q41
Q42
Q43
Q44
Q45
Q46
Q47
Q48
R1 1k2
R2 3k3
R3 3k3
R4 4k8
R5 6k2
R6 50k
R7 15k
R8 1k7
R9 4k9
R10 3k6
R11 620
R12 450
R13 1k
R14 395
R15 3k3
R16 6k2
R17 910
R18 2k7
R19 5k
R20 370
R21 30
R22 30
R23 20k
R24 80k
R25 1k2
R26 40k
R27 450
R28 150
R29 3k
R30 200
R31 75
R32 0.25
R32A 20
R32B 20
R33 2k
R34 75
R35 0.25
R35A 20
R35B 20
R36 510
R37 400
R38 20k
R39 510
R40 40
R41 20k
C1 4p
C2 4p
C3 4p
Z1
Z2
Z3
Z4
Z5
Z6
Z7
500X
40X
10X
3X
2
1
3
S

Application Hints

STABILITY

The LM1875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM1875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

Proper layout of the printed circuit board is very important. While the LM1875 will be stable when installed in a board similar to the ones shown in this data sheet, it is sometimes necessary to modify the layout somewhat to suit the physical requirements of a particular application. When designing a different layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM1875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM1875 is no exception. If the output of the LM1875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF. The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1Ω) should be placed in series with the output of the LM1875. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 5 μH inductor.

DISTORTION

The preceding suggestions regarding circuit board grounding techniques will also help to prevent excessive distortion levels in audio applications. For low THD, it is also necessary to keep the power supply traces and wires separated from the traces and wires connected to the inputs of the LM1875. This prevents the power supply currents, which are large and nonlinear, from inductively coupling to the LM1875 inputs. Power supply wires should be twisted together and separated from the circuit board. Where these wires are soldered to the board, they should be perpendicular to the plane of the board at least to a distance of a couple of inches. With a proper physical layout, THD levels at 20 kHz with 10W output to an 8Ω load should be less than 0.05%, and less than 0.02% at 1 kHz.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic audio power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM1875 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM1875, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM1875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM1875 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

POWER DISSIPATION AND HEAT SINKING

The LM1875 must always be operated with a heat sink, even when it is not required to drive a load. The maximum idling current of the device is 100 mA, so that on a 60V power supply an unloaded LM1875 must dissipate 6W of power. The 54°C/W junction-to-ambient thermal resistance of a TO-220 package would cause the die temperature to rise 324°C above ambient, so the thermal protection circuitry will shut the amplifier down if operation without a heat sink is attempted.

Application Hints (Continued)

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM1875 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D(MAX)} \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM1875, R_L is the load resistance, and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. The curves of "Power Dissipation vs Power Output" give a better representation of the behavior of the LM1875 with various power supply voltages and resistive loads. As an example, if the LM1875 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150°\text{C} - 70°\text{C}}{19\text{W}} = 4.2°\text{C/W}.$$

Using $\theta_{JC} = 2°\text{C/W}$, the sum of the case-to-heat-sink interface thermal resistance and the heat-sink-to-ambient thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry. If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM1875 and the heat sink. The heat sink thermal resistance must then be less than

$$4.2°\text{C/W} - 2°\text{C/W} - 1.6°\text{C/W} = 0.6°\text{C/W}.$$

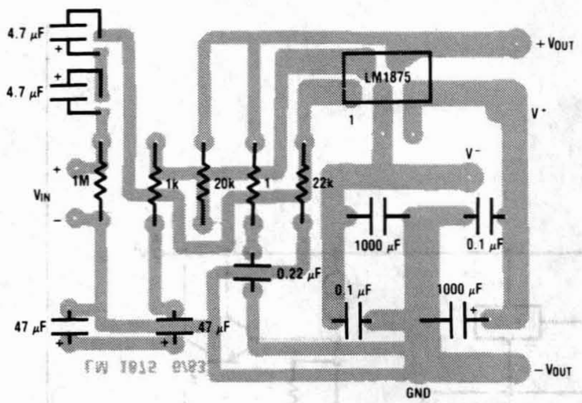
This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be reduced to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

Note: When using a single supply, maximum transfer of heat away from the LM1875 can be achieved by mounting the device directly to the heat sink (tab is at ground potential); this avoids the use of a mica or other type insulator.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load (usually considered to be a worst-case loudspeaker load) will be roughly that of the same amplifier driving the resistive part of that load. For example, a loudspeaker may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Component Layouts

Split Supply



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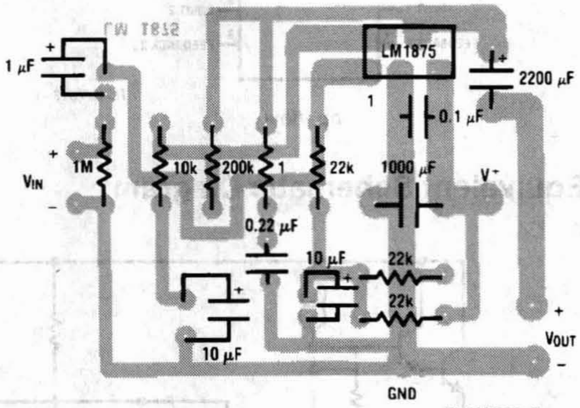
Single Supply



TL/H/5030-7

National Semiconductor

LM1877 Dual Audio Power Amplifier

General Description

The LM1877 is a monolithic dual power amplifier designed to deliver 2W/channel continuous into 8Ω loads. The LM1877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection, and output Q point centering. The LM1877 is internally compensated for all gains greater than 10.

Features

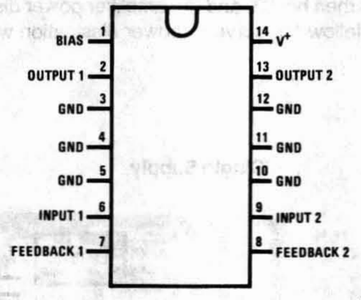
- 2W/channel
- −65 dB ripple rejection, output referred
- −65 dB channel separation, output referred
- Wide supply range, 6V–24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

Dual-In-Line Package or Surface Mount Package



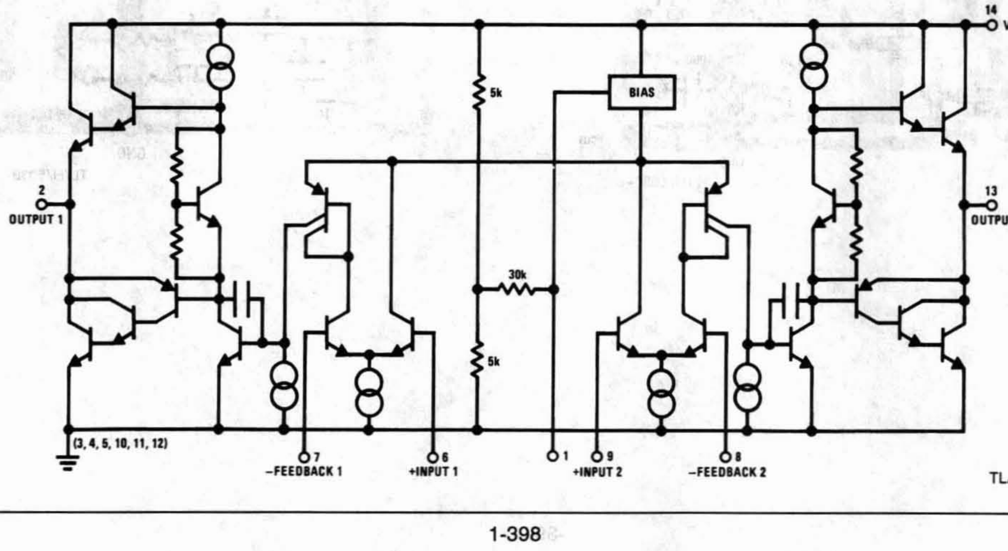
BIAS 1
OUTPUT 1 2
GND 3
GND 4
GND 5
INPUT 1 6
FEEDBACK 1 7
14 V+
13 OUTPUT 2
12 GND
11 GND
10 GND
9 INPUT 2
8 FEEDBACK 2

TL/H/7913–1

Top View

Order Number LM1877M-9 or LM1877N-9
See NS Package Number M14B or N14A

Equivalent Schematic Diagram



14 V+
BIAS
5k
30k
5k
2 OUTPUT 1
13 OUTPUT 2
(3, 4, 5, 10, 11, 12)
7 −FEEDBACK 1
6 +INPUT 1
1
9 +INPUT 2
8 −FEEDBACK 2

TL/H/7913–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C

Lead Temperature	
N-Package Soldering (10 sec.)	260°C
M-Package Infared (15 sec.)	220°C
M-Package Vapor Phase (60 sec.)	215°C
Thermal Resistance	
θ_{JC} (N-Package)	30°C/W
θ_{JA} (N-Package)	79°C/W
θ_{JC} (M-Package)	27°C/W
θ_{JA} (M-Package)	114°C/W

Electrical Characteristics

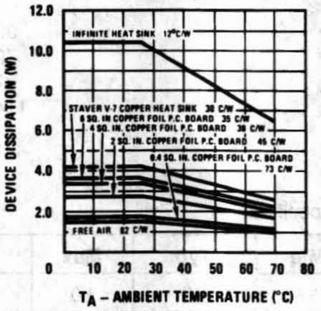
$V_S = 20V$, $T_A = 25°C$, (See Note 1) $R_L = 8\Omega$, $A_V = 50$ (34 dB) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	$P_O = 0W$		25	50	mA
Output Power	THD = 10%				
LM1877	$V_S = 20V, R_L = 8\Omega$	2.0			W/Ch
	$V_S = 12V, R_L = 8\Omega$		1.3		W/Ch
Total Harmonic Distortion LM1877	$f = 1$ kHz, $V_S = 14V$				
	$P_O = 50$ mW/Channel		0.075		%
	$P_O = 500$ mW/Channel		0.045		%
	$P_O = 1$ W/Channel		0.055		%
Output Swing	$R_L = 8\Omega$		$V_S - 6$		Vp-p
Channel Separation	$C_F = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$, $f = 1$ kHz, Output Referred				
	$V_S = 20V$, $V_O = 4$ Vrms	−50	−70		dB
	$V_S = 7V$, $V_O = 0.5$ Vrms		−60		dB
PSRR Power Supply Rejection Ratio	$C_F = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$, $f = 120$ Hz, Output Referred				
	$V_S = 20V$, $V_{RIPPLE} = 1$ Vrms	−50	−65		dB
	$V_S = 7V$, $V_{RIPPLE} = 0.5$ Vrms		−40		dB
Noise	Equivalent Input Noise				
	$R_S = 0$, $C_{IN} = 0.1\ \mu F$, BW = 20 Hz–20 kHz, Output Noise Wideband		2.5		μV
	$R_S = 0$, $C_N = 0.1\ \mu F$, A_V 200		0.80		mV
Open Loop Gain	$R_S = 0$, $f = 100$ kHz, $R_L = 8\Omega$		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	$V_S = 20V$	9	10	11	V
Slew Rate			2.0		V/μs
Power Bandwidth			65		kHz
Current Limit			1.0		A

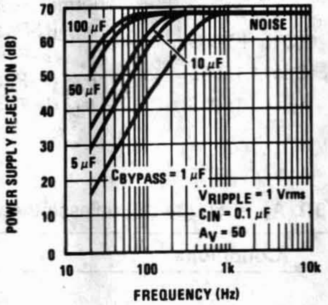
Note 1: For operation at ambient temperature greater than 25°C, the LM1877 must be derated based on a maximum 150°C junction temperature.

Typical Performance Characteristics

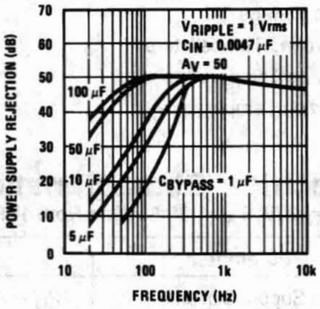
Device Dissipation vs Ambient Temperature



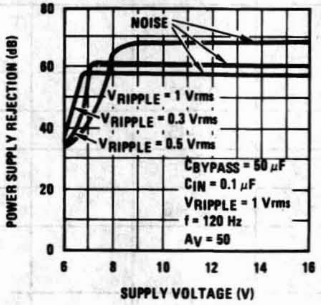
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



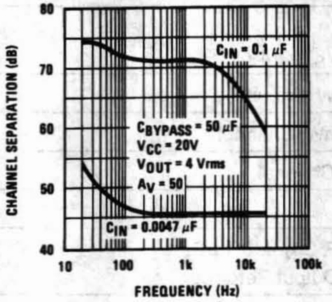
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



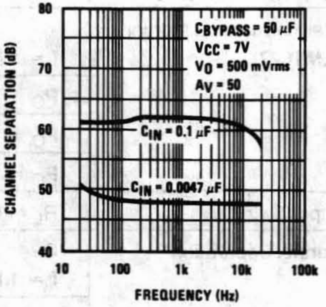
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



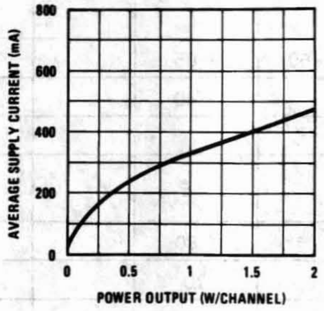
Channel Separation (Referred to the Output) vs Frequency



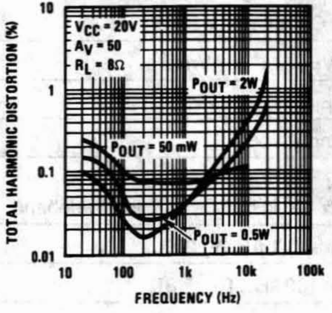
Channel Separation (Referred to the Output) vs Frequency



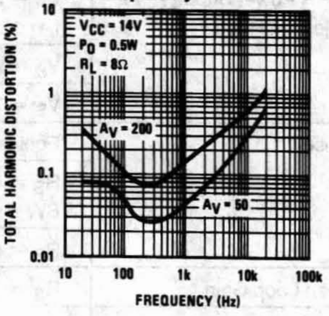
Average Supply Current vs P_{OUT}



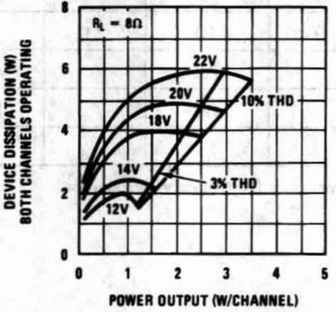
Total Harmonic Distortion vs Frequency



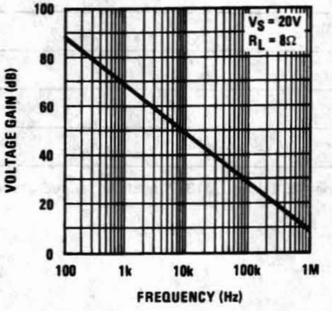
Total Harmonic Distortion vs Frequency



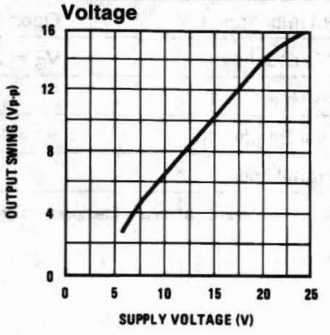
Power Dissipation (W) Both Channels Operating



Open Loop Gain vs Frequency



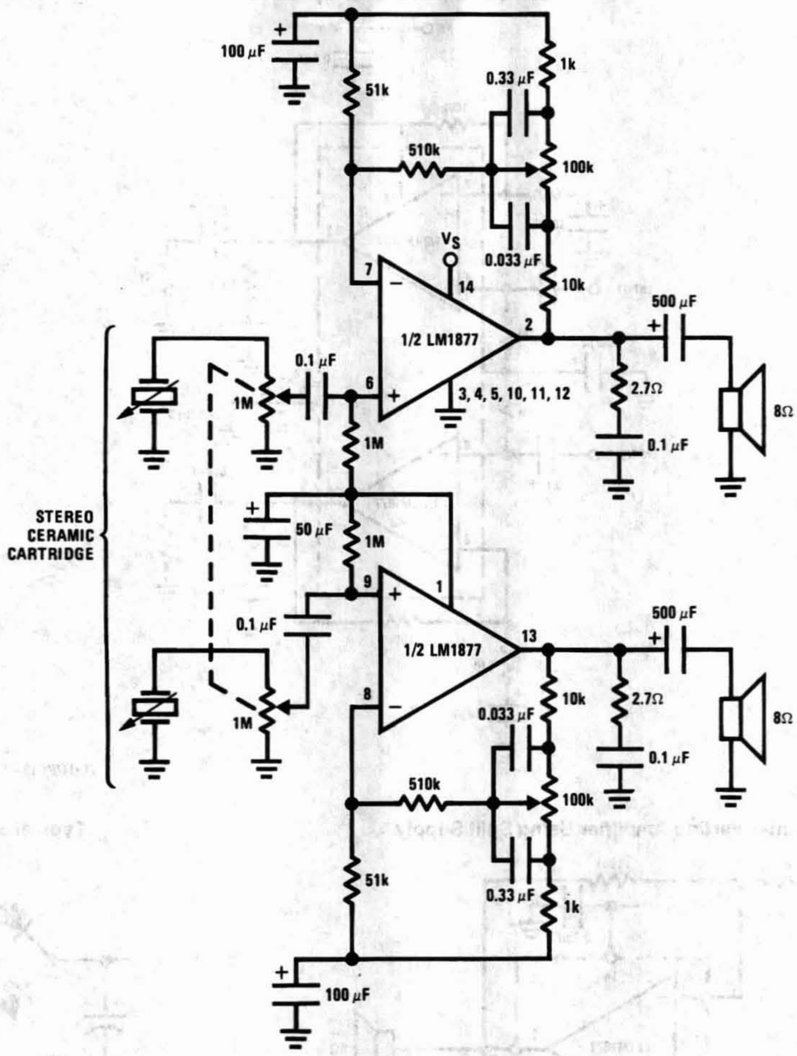
Output Swing vs Supply Voltage



TL/H/7913–3

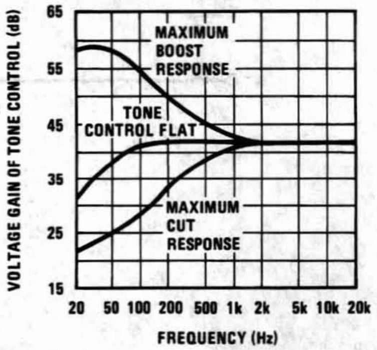
Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control


100 μF
51k
1k
0.33 μF
510k
100k
0.033 μF
V_S
14
7
10k
500 μF
2
1/2 LM1877
0.1 μF
6
1M
3, 4, 5, 10, 11, 12
2.7Ω
8Ω
0.1 μF
1M
STEREO
CERAMIC
CARTRIDGE
50 μF
1M
9
1
0.1 μF
1/2 LM1877
13
500 μF
8
10k
2.7Ω
1M
0.033 μF
0.1 μF
8Ω
510k
100k
51k
0.33 μF
1k
100 μF

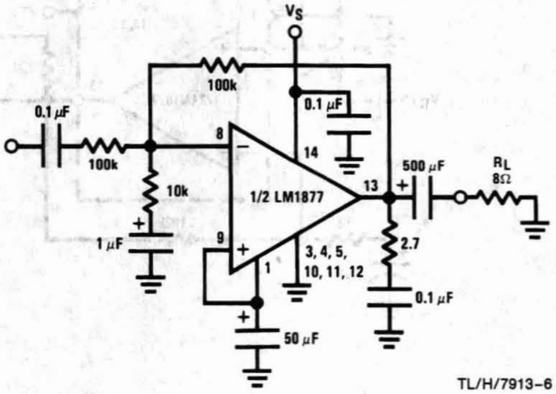
TL/H/7913-4

Frequency Response of Bass Tone Control



TL/H/7913-5

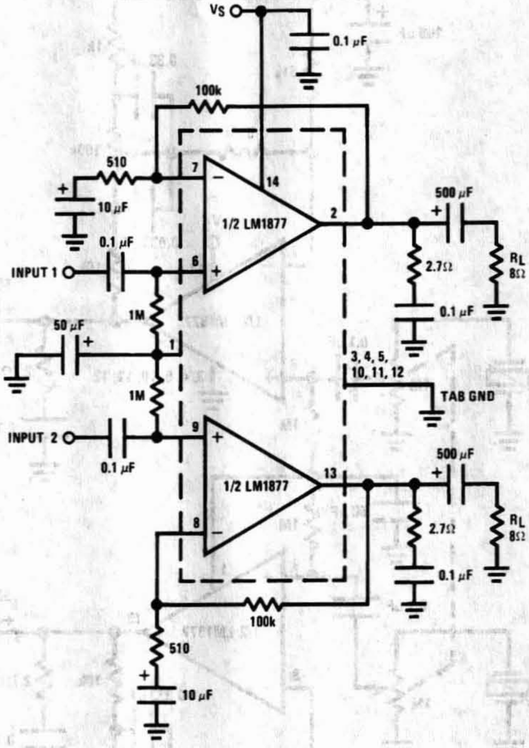
Inverting Unity Gain Amplifier


V_S
100k
0.1 μF
0.1 μF
100k
8
14
10k
1/2 LM1877
13
500 μF
R_L
8Ω
1 μF
9
1
3, 4, 5,
10, 11, 12
2.7
0.1 μF
50 μF

TL/H/7913-6

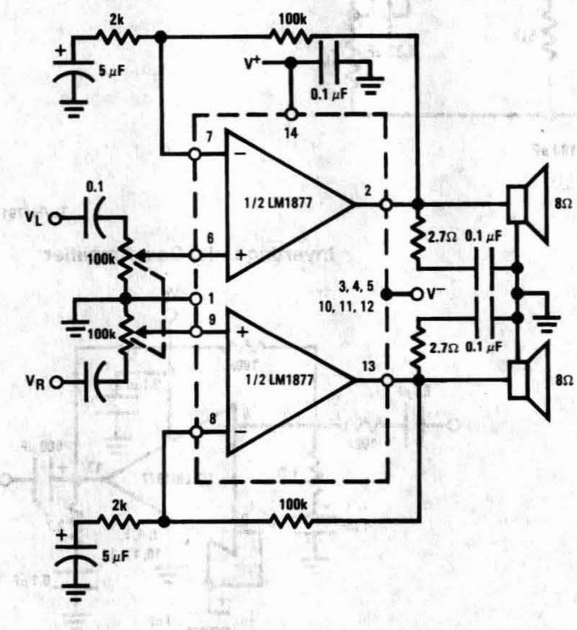
Typical Applications (Continued)

Stereo Amplifier with $A_V = 200$


VS
0.1 μF
100k
510
10 μF
7
14
1/2 LM1877
2
500 μF
0.1 μF
INPUT 1
6
2.7Ω
RL
8Ω
1M
50 μF
1
3, 4, 5,
10, 11, 12
TAB GND
1M
INPUT 2
9
0.1 μF
13
1/2 LM1877
8
100k
510
10 μF

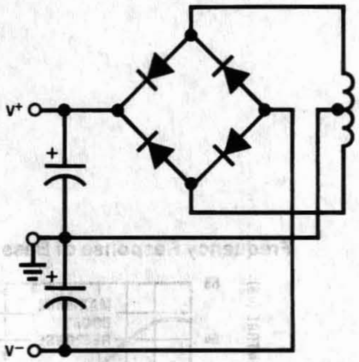
TL/H/7913–7

Non-Inverting Amplifier Using Split Supply


2k
100k
5 μF
V+
0.1 μF
14
7
1/2 LM1877
2
8Ω
0.1
VL
100k
6
2.7Ω
0.1 μF
3, 4, 5
10, 11, 12
V−
1
100k
9
2.7Ω
0.1 μF
VR
1/2 LM1877
13
8Ω
8
2k
100k
5 μF

TL/H/7913–8

Typical Split Supply



TL/H/7913–9

National Semiconductor

LM1896/LM2896 Dual Audio Power Amplifier

General Description

The LM1896 is a high performance 6V stereo power amplifier designed to deliver 1 watt/channel into 4Ω or 2 watts bridged monaural into 8Ω. Utilizing a unique patented compensation scheme, the LM1896 is ideal for sensitive AM radio applications. This new circuit technique exhibits lower wideband noise, lower distortion, and less AM radiation than conventional designs. The amplifier's wide supply range (3V–9V) is ideal for battery operation. For higher supplies (V_S > 9V) the LM2896 is available in an 11-lead single-in-line package. The LM2896 package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

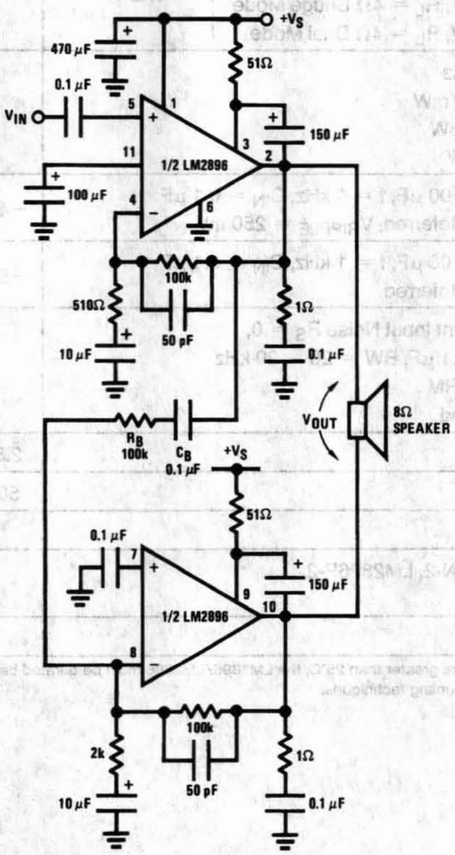
Features

- Low AM radiation
- Low noise
- 3V, 4Ω, stereo P_o = 250 mW
- Wide supply operation 3V–15V (LM2896)
- Low distortion
- No turn on "pop"
- Adjustable voltage gain and bandwidth
- Smooth waveform clipping
- P_o = 9W bridged, LM2896

Applications

- Compact AM-FM radios
- Stereo tape recorders and players
- High power portable stereos

Typical Applications


+V_S
470 µF
0.1 µF
51Ω
V_IN
5
1
3
150 µF
2
11
1/2 LM2896
100 µF
4
6
100k
510Ω
1Ω
50 pF
10 µF
0.1 µF
8Ω SPEAKER
V_OUT
R_B 100k
C_B 0.1 µF
+V_S
51Ω
0.1 µF
7
150 µF
9
10
1/2 LM2896
8
100k
2k
1Ω
50 pF
10 µF
0.1 µF

TL/H/7920–1

FIGURE 1. LM2896 in Bridge Configuration (A_V = 400, BW = 20 kHz)

Order Number LM1896N
See NS Package Number N14A

Order Number LM2896P
See NS Package Number P11A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
LM1896	V_S = 12V
LM2896	V_S = 18V
Operating Temperature (Note 1)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Thermal Resistance	
θ_{JC} (DIP)	30°C/W
θ_{JA} (DIP)	137°C/W
θ_{JC} (SIP)	10°C/W
θ_{JA} (SIP)	55°C/W

Electrical Characteristics

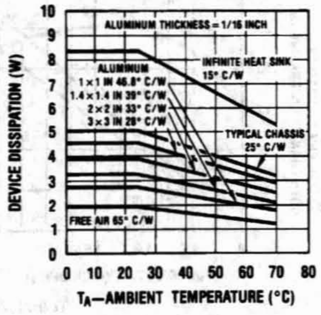
Unless otherwise specified, T_A = 25°C, A_V = 200 (46 dB). For the LM1896; V_S = 6V and R_L = 4Ω. For LM2896, T_{TAB} = 25°C, V_S = 12V and R_L = 8Ω. Test circuit shown in *Figure 2*.

Parameter	Conditions	LM1896			LM2896			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Current	P_o = 0W, Dual Mode		15	25		25	40	mA
Operating Supply Voltage		3		10	3		15	V
Output Power	THD = 10%, f = 1 kHz							
LM1896N-1	V_S = 6V, R_L = 4Ω Dual Mode T_A = 25°C	0.9	1.1					W/ch
LM1896N-2	V_S = 6V, R_L = 8Ω Bridge Mode		1.8	2.1				W
	V_S = 9V, R_L = 8Ω Dual Mode		1.3					W/ch
LM2896P-1	V_S = 12V, R_L = 8Ω Dual Mode T_{TAB} = 25°C				2.0	2.5		W/ch
LM2896P-2	V_S = 12V, R_L = 8Ω Bridge Mode				7.2	9.0		W
	V_S = 9V, R_L = 4Ω Bridge Mode					7.8		W
	V_S = 9V, R_L = 4Ω Dual Mode					2.5		W/ch
Distortion	f = 1 kHz							
	P_o = 50 mW		0.09			0.09		%
	P_o = 0.5W		0.11			0.11		%
	P_o = 1W					0.14		%
Power Supply Rejection Ratio (PSRR)	C_{BY} = 100 μF, f = 1 kHz, C_{IN} = 0.1 μF Output Referred, V_{RIPPLE} = 250 mV	−40	−54		−40	−54		dB
Channel Separation	C_{BY} = 100 μF, f = 1 kHz, C_{IN} = 0.1 μF Output Referred	−50	−64		−50	−64		dB
Noise	Equivalent Input Noise R_S = 0,							
	C_{IN} = 0.1 μF, BW = 20 − 20 kHz		1.4			1.4		μV
	CCIR/ARM		1.4			1.4		μV
	Wideband		2.0			2.0		μV
DC Output Level		2.8	3	3.2	5.6	6	6.4	V
Input Impedance		50	100	350	50	100	350	kΩ
Input Offset Voltage			5			5		mV
Voltage Difference between Outputs	LM1896N-2, LM2896P-2		10	20		10	20	mV
Input Bias Current			120			120		nA

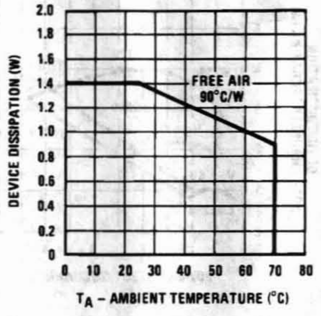
Note 1: For operation at ambient temperature greater than 25°C, the LM1896/LM2896 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon mounting techniques.

Typical Performance Curves

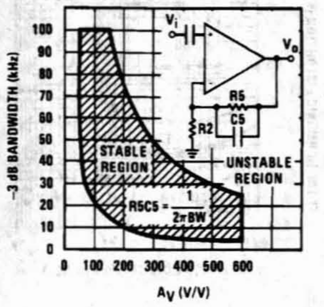
LM2896 Device Dissipation vs Ambient Temperature



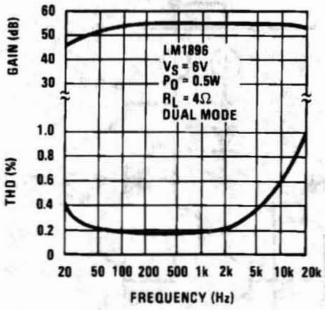
LM1896 Maximum Device Dissipation vs Ambient Temperature



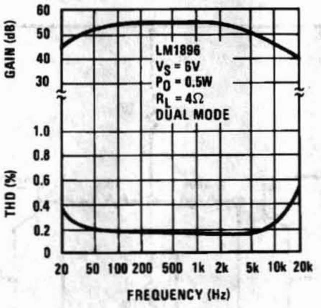
−3 dB Bandwidth vs Voltage Gain for Stable Operation



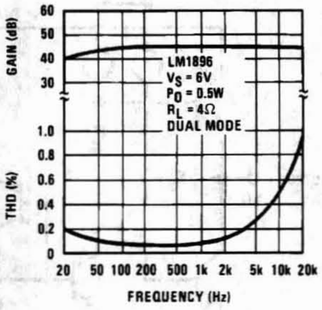
THD and Gain vs Frequency $A_V = 54$ dB, BW = 30 kHz



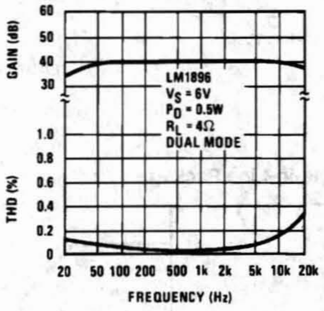
THD and Gain vs Frequency $A_V = 54$ dB, BW = 5 kHz



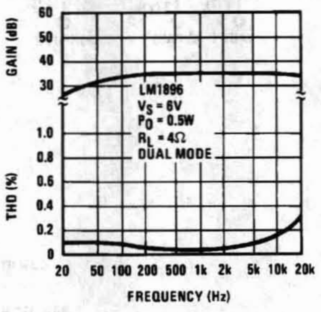
THD and Gain vs Frequency $A_V = 46$ dB, BW = 50 kHz



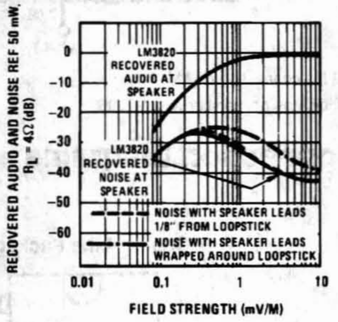
THD and Gain vs Frequency $A_V = 40$ dB, BW = 20 kHz



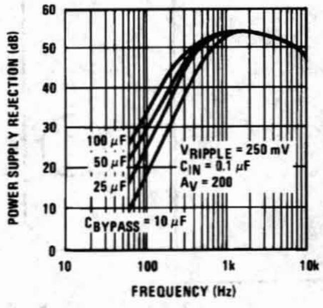
THD and Gain vs Frequency $A_V = 34$ dB, BW = 50 kHz



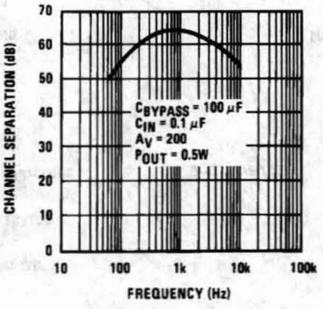
AM Recovered Audio and Noise vs Field Strength for Different Speaker Lead Placement



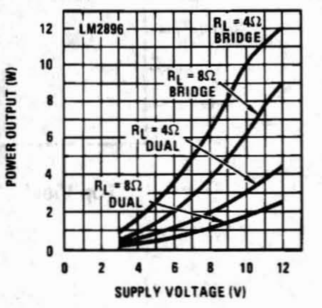
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



Channel Separation (Referred to the Output) vs Frequency



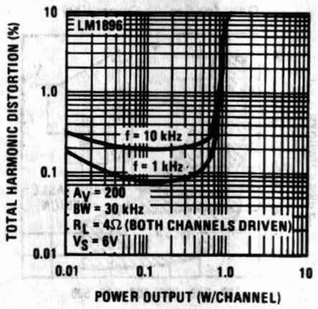
Power Output vs Supply Voltage



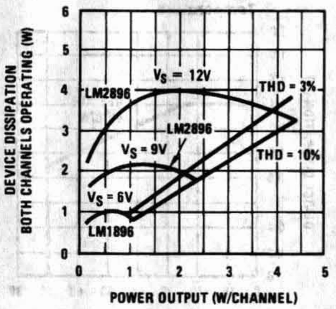
TL/H/7920–2

Typical Performance Curves (Continued)

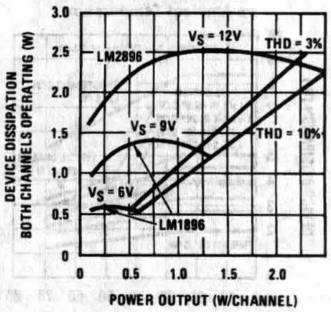
Total Harmonic Distortion vs Power Output



Power Dissipation vs Power Output R_L = 4Ω

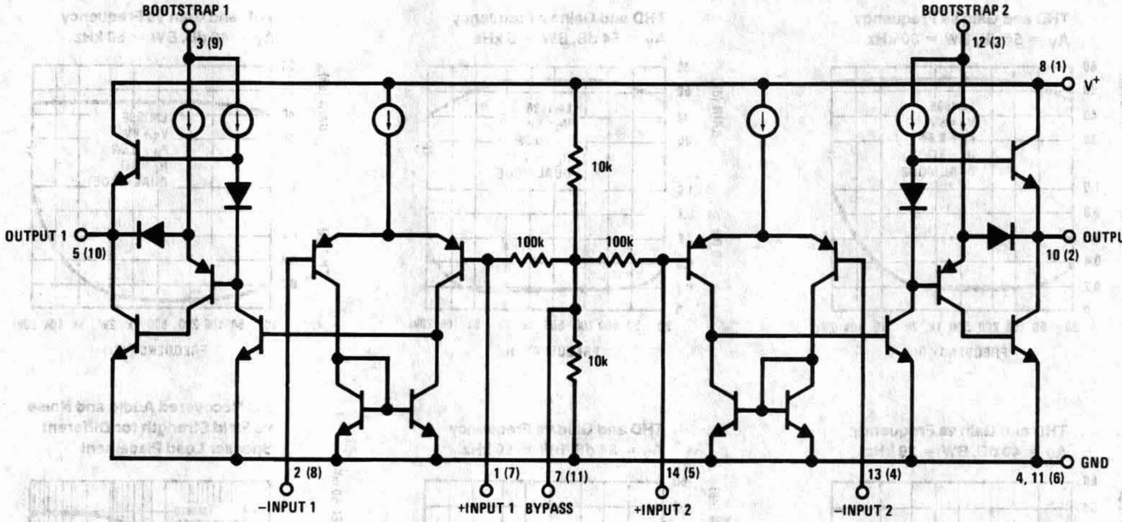


Power Dissipation vs Power Output R_L = 8Ω



TL/H/7920–3

Equivalent Schematic


BOOTSTRAP 1
3 (9)
OUTPUT 1
5 (10)
10k
100k
100k
10k
2 (8)
–INPUT 1
1 (7)
+INPUT 1
7 (11)
BYPASS
14 (5)
+INPUT 2
13 (4)
–INPUT 2
4, 11 (6)
GND
BOOTSTRAP 2
12 (3)
8 (1)
V+
OUTPUT 2
10 (2)

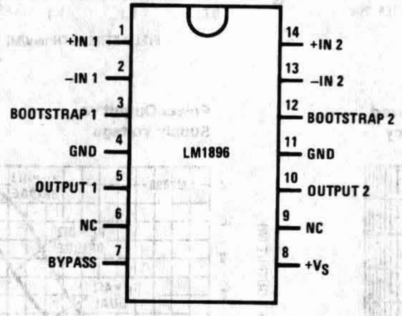
6, 9 No connection on LM1896

( ) indicates pin number for LM2896

TL/H/7920–4

Connection Diagrams

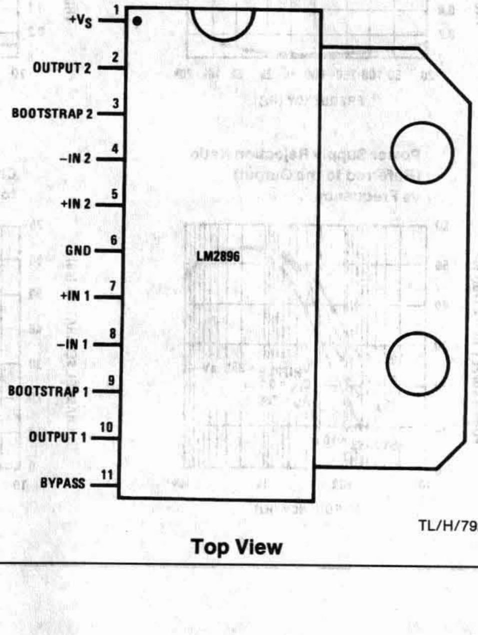
Dual-In-Line Package


+IN 1
1
–IN 1
2
BOOTSTRAP 1
3
GND
4
OUTPUT 1
5
NC
6
BYPASS
7
LM1896
14
+IN 2
13
–IN 2
12
BOOTSTRAP 2
11
GND
10
OUTPUT 2
9
NC
8
$+V_S$

Top View

TL/H/7920–5

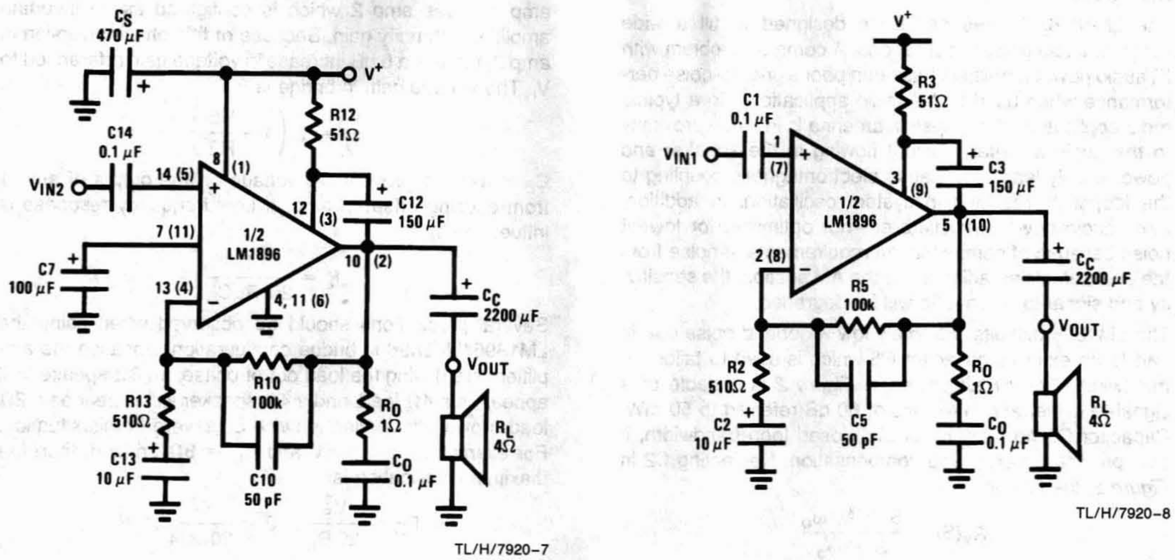
Single-In-Line Package


$+V_S$
1
OUTPUT 2
2
BOOTSTRAP 2
3
–IN 2
4
+IN 2
5
GND
6
+IN 1
7
–IN 1
8
BOOTSTRAP 1
9
OUTPUT 1
10
BYPASS
11
LM2896

TL/H/7920–6

Top View

Typical Applications (Continued)


CS
470 µF
+
V+
R12
51Ω
C14
0.1 µF
8
(1)
14 (5)
VIN2
+
12
(3)
C12
150 µF
7 (11)
1/2
LM1896
10
(2)
C7
100 µF
13 (4)
−
4, 11 (6)
CC
2200 µF
VOUT
R10
100k
R13
510Ω
RO
1Ω
RL
4Ω
C13
10 µF
C10
50 pF
CO
0.1 µF
TL/H/7920-7
V+
R3
51Ω
C1
0.1 µF
1
(7)
VIN1
+
3
(9)
C3
150 µF
1/2
LM1896
5 (10)
2 (8)
−
CC
2200 µF
R5
100k
VOUT
R2
510Ω
RO
1Ω
RL
4Ω
C2
10 µF
C5
50 pF
CO
0.1 µF
TL/H/7920-8

6, 9 No connection on LM1896

( ) Indicates pin number for LM2896

FIGURE 2. Stereo Amplifier with $A_V = 200$, BW = 30 kHz

External Components *(Figure 2)*

Components	Comments
1. R2, R5, R10, R13	Sets voltage gain, $A_V = 1 + R5/R2$ for one channel and $A_V = 1 + R10/R13$ for the other channel.
2. R3, R12	Bootstrap resistor sets drive current for output stage and allows pins 3 and 12 to go above V_S.
3. R_O	Works with C_O to stabilize output stage.
4. C1, C14	Input coupling capacitor. Pins 1 and 14 are at a DC potential of $V_S/2$. Low frequency pole set by: $f_L = \frac{1}{2\pi R_{IN} C1}$
5. C2, C13	Feedback capacitors. Ensure unity gain at DC. Also a low frequency pole at: $f_L = \frac{1}{2\pi R2C2}$
6. C3, C12	Bootstrap capacitors, used to increase drive to output stage. A low frequency pole is set by: $f_L = \frac{1}{2\pi R3C3}$
7. C5, C10	Compensation capacitor. These stabilize the amplifiers and adjust their bandwidth. See curve of bandwidth vs allowable gain.
8. C7	Improves power supply rejection (See Typical Performance Curves). Increasing C7 increases turn-on delay.
9. C_C	Output coupling capacitor. Isolates pins 5 and 10 from the load. Low frequency pole set by: $f_L = \frac{1}{2\pi C_C R_L}$
10. C_O	Works with R_O to stabilize output stage.
11. C_S	Provides power supply filtering.

Application Hints

AM Radios

The LM1896/LM2896 has been designed fo fill a wide range of audio power applications. A common problem with IC audio power amplifiers has been poor signal-to-noise performance when used in AM radio applications. In a typical radio application, the loopstick antenna is in close proximity to the audio amplifer. Current flowing in the speaker and power supply leads can cause electromagnetic coupling to the loopstick, resulting in system oscillation. In addition, most audio power amplifiers are not optimized for lowest noise because of compensation requirements. If noise from the audio amplifier radiates into the AM section, the sensitivity and signal-to-noise ratio will be degraded.

The LM1896 exhibits extremely low wideband noise due in part to an external capacitor C5 which is used to tailor the bandwidth. The circuit shown in *Figure 2* is capable of a signal-to-noise ratio in excess of 60 dB referred to 50 mW. Capacitor C5 not only limits the closed loop bandwidth, it also provides overall loop compensation. Neglecting C2 in *Figure 2*, the gain is:

$$A_V(S) = \frac{S + A_V\,\omega_o}{S + \omega_o}$$

$$\text{where } A_V = \frac{R2 + R5}{R2}, \quad \omega_o = \frac{1}{R5C5}$$

A curve of −3 dB BW (ω_o) vs A_V is shown in the Typical Performance Curves.

Figure 3 shows a plot of recovered audio as a function of field strength in μV/M. The receiver section in this example is an LM3820. The power amplifier is located about two inches from the loopstick antenna. Speaker leads run parallel to the loopstick and are 1/8 inch from it. Referenced to a 20 dB S/N ratio, the improvement in noise performance over conventional designs is about 10 dB. This corresponds to an increase in usable sensitivity of about 8.5 dB.

Bridge Amplifiers

The LM1896/LM2896 can be used in the bridge mode as a monaural power amplifier. In addition to much higher power output, the bridge configuration does not require output coupling capacitors. The load is connected directly between the amplifier outputs as shown in *Figure 4*.

Amp 1 has a voltage gain set by 1 + R5/R2. The output of amp 1 drives amp 2 which is configured as an inverting amplifier with unity gain. Because of this phase inversion in amp 2, there is a 6 dB increase in voltage gain referenced to V_i. The voltage gain in bridge is:

$$\frac{V_o}{V_i} = 2\left(1 + \frac{R5}{R2}\right)$$

C_B is used to prevent DC voltage on the output of amp 1 from causing offset in amp 2. Low frequency response is influenced by:

$$f_L = \frac{1}{2\pi\, R_B C_B}$$

Several precautions should be observed when using the LM1896/LM2896 in bridge configuration. Because the amplifiers are driving the load out of phase, an 8Ω speaker will appear as a 4Ω load, and a 4Ω speaker will appear as a 2Ω load. Power dissipation is twice as severe in this situation. For example, if V_S = 6V and R_L = 8Ω bridged, then the maximum dissipation is:

$$P_D = \frac{V_S^2}{20\,R_L} \times 2 = \frac{6^2}{20 \times 4} \times 2$$

$$P_D = 0.9 \text{ Watts}$$

This amount of dissipation is equivalent to driving two 4Ω loads in the stereo configuration.

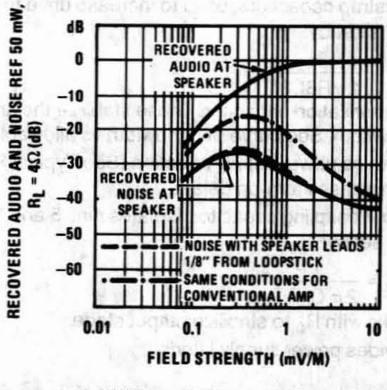
When adjusting the frequency response in the bridge configuration, R5C5 and R10C10 form a 2 pole cascade and the −3 dB bandwidth is actually shifted to a lower frequency:

$$BW = \frac{0.707}{2\pi RC}$$

where R = feedback resistor

C = feedback capacitor

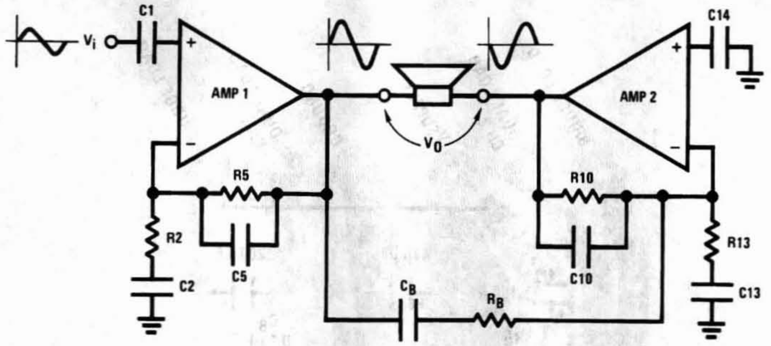
To measure the output voltage, a floating or differential meter should be used because a prolonged output short will over dissipate the package. *Figure 1* shows the complete bridge amplifier.



TL/H/7920–9

FIGURE 3. Improved AM Sensitivity over Conventional Design

Application Hints (Continued)


C1
V_i
AMP 1
R5
R2
C2
C5
C_B
R_B
V_O
R10
C10
R13
C13
C14
AMP 2

TL/H/7920-10

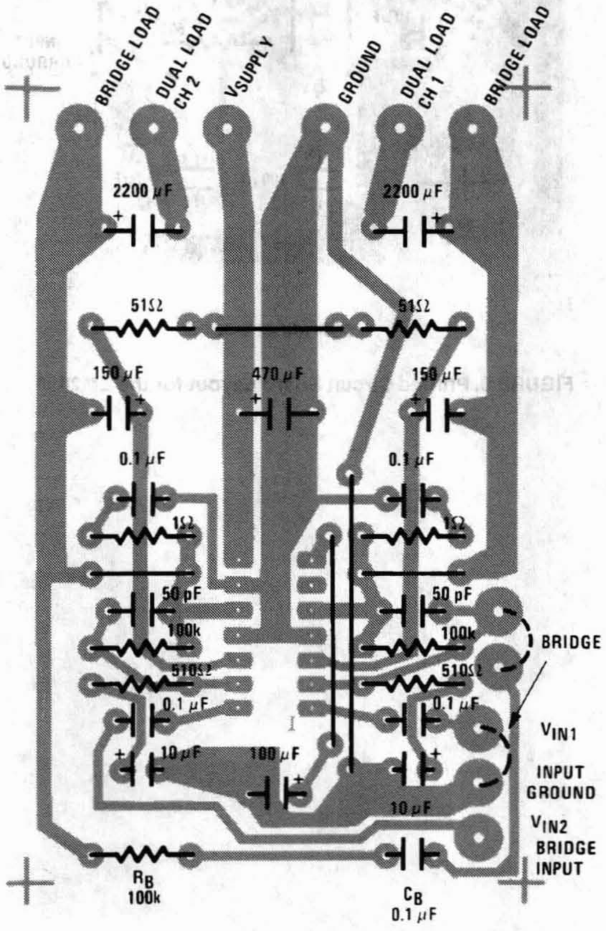
Figure 4. Bridge Amplifier Connection

Printed Circuit Layout

Printed Circuit Board Layout

Figure 5 and *Figure 6* show printed circuit board layouts for the LM1896 and LM2896. The circuits are wired as stereo amplifiers. The signal source ground should return to the input ground shown on the boards. Returning the loads to power supply ground through a separate wire will keep the THD at its lowest value. The inputs should be terminated in less than 50 kΩ to prevent an input-output oscillation. This oscillation is dependent on the gain and the proximity of the bridge elements R_B and C_B to the (+) input. If the bridge mode is not used, do not insert R_B, C_B into the PCB.

To wire the amplifer into the bridge configuration, short the capacitor on pin 7 (pin 1 of the LM1896) to ground. Connect together the nodes labeled BRIDGE and drive the capacitor connected to pin 5 (pin 14 of the LM1896).

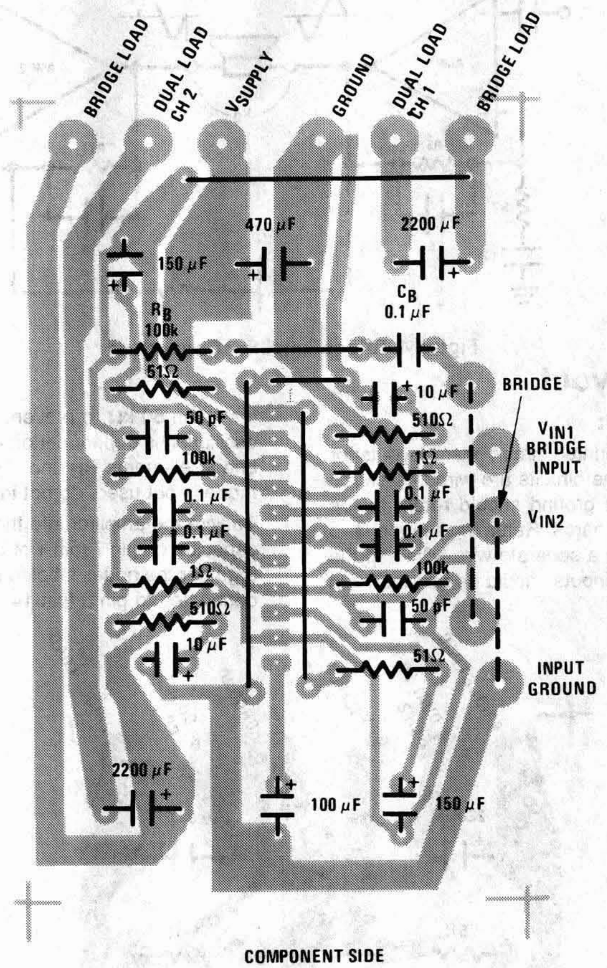

BRIDGE LOAD
DUAL LOAD CH 2
VSUPPLY
GROUND
DUAL LOAD CH 1
BRIDGE LOAD
2200 μF
2200 μF
51Ω
51Ω
150 μF
470 μF
150 μF
0.1 μF
0.1 μF
1Ω
1Ω
50 pF
50 pF
100k
100k
510Ω
510Ω
0.1 μF
0.1 μF
10 μF
100 μF
10 μF
BRIDGE
V_{IN1}
INPUT GROUND
V_{IN2}
BRIDGE INPUT
R_B
100k
C_B
0.1 μF

COMPONENT SIDE

TL/H/7920-11

FIGURE 5. Printed Circuit Board Layout for the LM1896

Printed Circuit Layout (Continued)


BRIDGE LOAD
DUAL LOAD CH 2
V_{SUPPLY}
GROUND
DUAL LOAD CH 1
BRIDGE LOAD
470 μF
2200 μF
150 μF
C_B 0.1 μF
R_B 100k
51Ω
10 μF
BRIDGE
510Ω
50 pF
V_{IN1}
BRIDGE INPUT
100k
1Ω
0.1 μF
0.1 μF
V_{IN2}
0.1 μF
0.1 μF
1Ω
100k
510Ω
50 pF
10 μF
51Ω
INPUT GROUND
2200 μF
100 μF
150 μF
COMPONENT SIDE

TL/H/7920-12

FIGURE 6. Printed Circuit Board Layout for the LM2896

National Semiconductor

LM2877 Dual 4W Audio Power Amplifier

General Description

The LM2877 is a monolithic dual power amplifier designed to deliver 4W/channel continuous into 8Ω loads. The LM2877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection and output Q point centering. The LM2877 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package.

Features

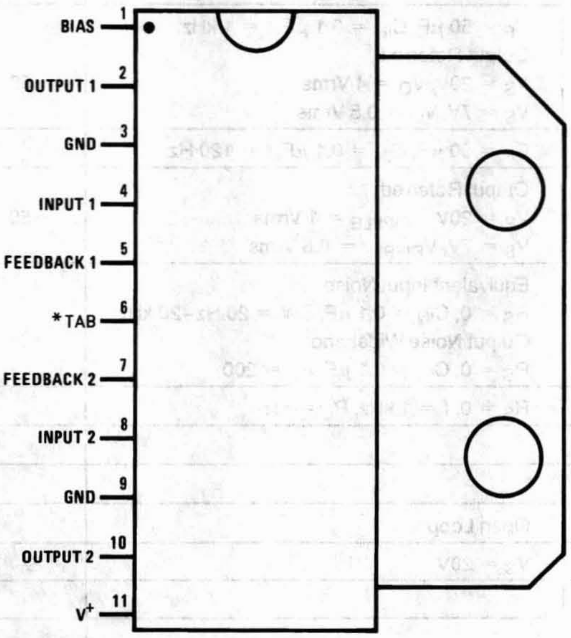
- 4W/channel
- −68 dB ripple rejection, output referred
- −70 dB channel separation, output referred
- Wide supply range, 6-24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

(Single-In-Line Package)



TL/H/7933–1

Top View

Order Number LM2877P
See NS Package Number P11A

*Pin 6 must be connected to GND.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

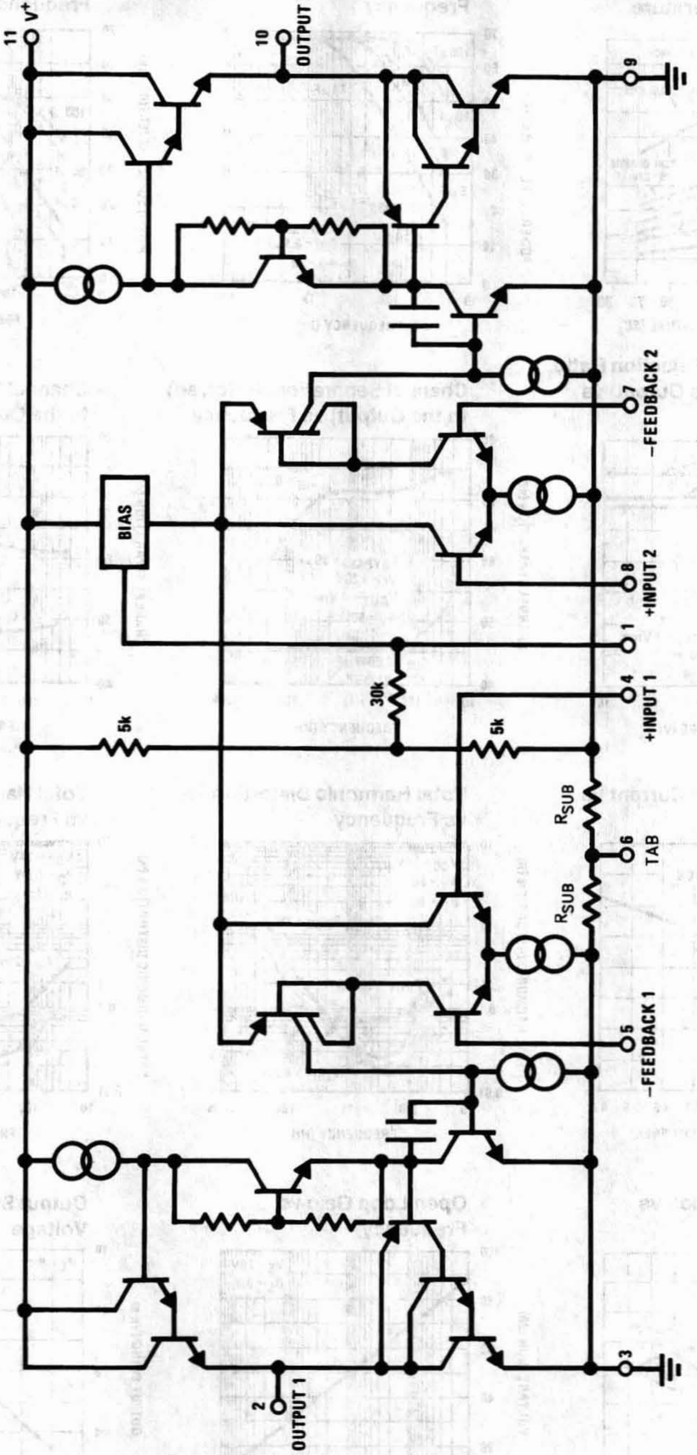
Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Thermal Resistance	
θ_{JC}	10°C/W
θ_{JA}	55°C/W

Electrical Characteristics $V_S = 20V$, $T_{TAB} = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB) unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	$P_O = 0W$		25	50	mA
Operating Supply Voltage		6		24	V
Output Power/Channel	f = 1 kHz, THD = 10%, $T_{TAB} = 25°C$				
	$V_S = 20V$	4.0	4.5		W
	$V_S = 18V$		3.6		W
	$V_S = 12V$, $R_L = 4\Omega$	1.5	1.9		W
	$V_S = 12V$, $R_L = 8\Omega$		1.0		W
Distortion, THD	f = 1 kHz, $V_S = 20V$				
	$P_O = 50$ mW/Channel		0.1		%
	$P_O = 1W$/Channel		0.07	1	%
	$P_O = 2W$/Channel		0.07		%
	f = 1 kHz, $V_S = 12V$, $R_L = 4\Omega$				
	$P_O = 50$ mW/Channel		0.25		%
	$P_O = 500$ mW/Channel		0.20		%
	$P_O = 1W$/Channel		0.15	1	%
Output Swing	$R_L = 8\Omega$		$V_S - 4$		V_{p-p}
Channel Separation	$C_F = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$, f = 1 kHz, Output Referred				
	$V_S = 20V$, $V_O = 4$ Vrms	−50	−70		dB
	$V_S = 7V$, $V_O = 0.5$ Vrms		−60		dB
PSRR Power Supply	$C_F = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$, f = 120 Hz				
Rejection Ratio	Output Referred				
	$V_S = 20V$, $V_{RIPPLE} = 1$ Vrms	−50	−68		dB
	$V_S = 7V$, $V_{RIPPLE} = 0.5$ Vrms		−40		dB
Noise	Equivalent Input Noise				
	$R_S = 0$, $C_{IN} = 0.1\ \mu F$, BW = 20 Hz–20 kHz		2.5		μV
	Output Noise Wideband				
	$R_S = 0$, $C_{IN} = 0.1\ \mu F$, $A_V = 200$		0.80		mV
Open Loop Gain	$R_S = 0$, f = 1 kHz, $R_L = 8\Omega$		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	$V_S = 20V$	9	10	11	V
Slew Rate			2.0		V/μs
Power Bandwidth			65		kHz
Current Limit			1.0		A

Note 1: For operation at ambient temperature greater than 25°C, the LM2877 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

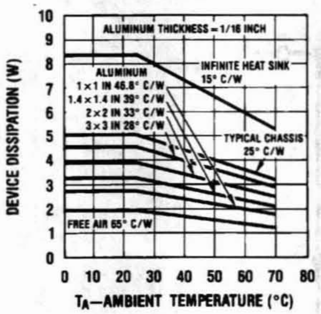
Equivalent Schematic Diagram


11 V+
10 OUTPUT 2
9
BIAS
7 −FEEDBACK 2
8 +INPUT 2
1
30k
4 +INPUT 1
5k
5k
RSUB
6 TAB
RSUB
5 −FEEDBACK 1
3
2 OUTPUT 1

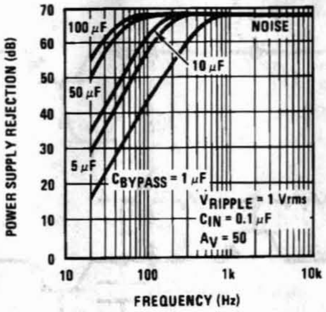
TL/H/7933–2

Typical Performance Characteristics

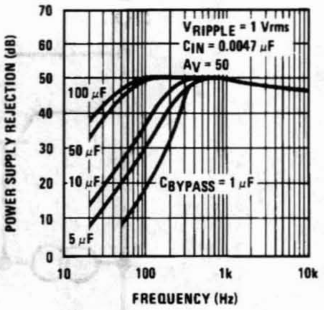
Device Dissipation vs Ambient Temperature



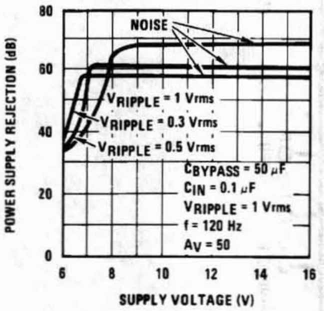
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



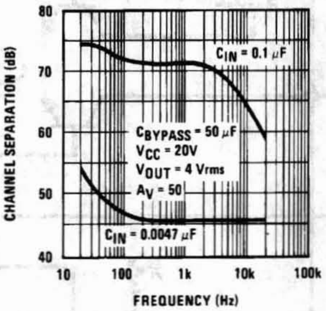
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



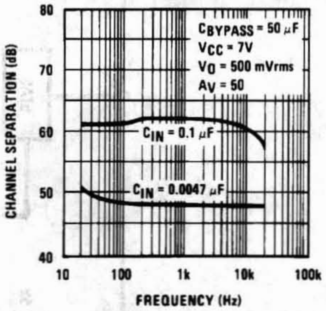
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



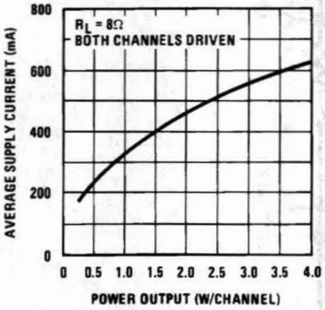
Channel Separation (Referred) to the Output) vs Frequency



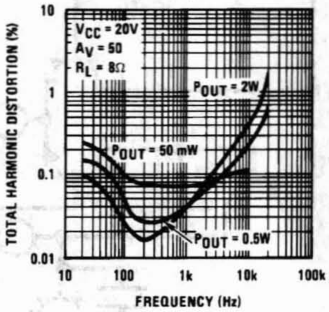
Channel Separation (Referred) to the Output) vs Frequency



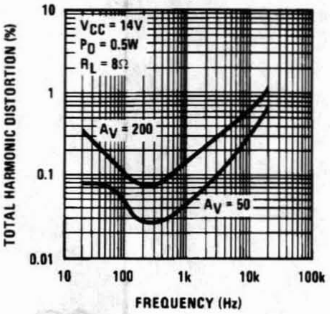
Average Supply Current vs Power Output



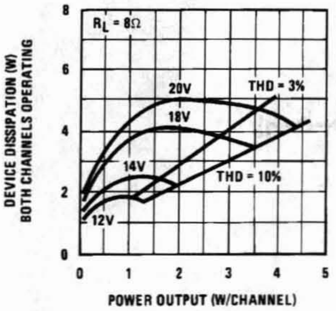
Total Harmonic Distortion vs Frequency



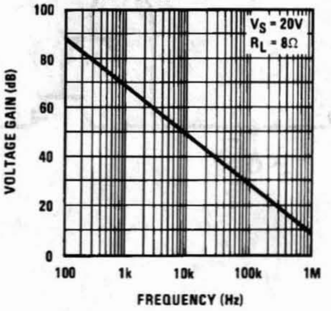
Total Harmonic Distortion vs Frequency



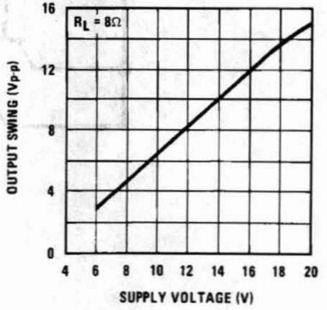
Power Dissipation vs Power Output



Open Loop Gain vs Frequency



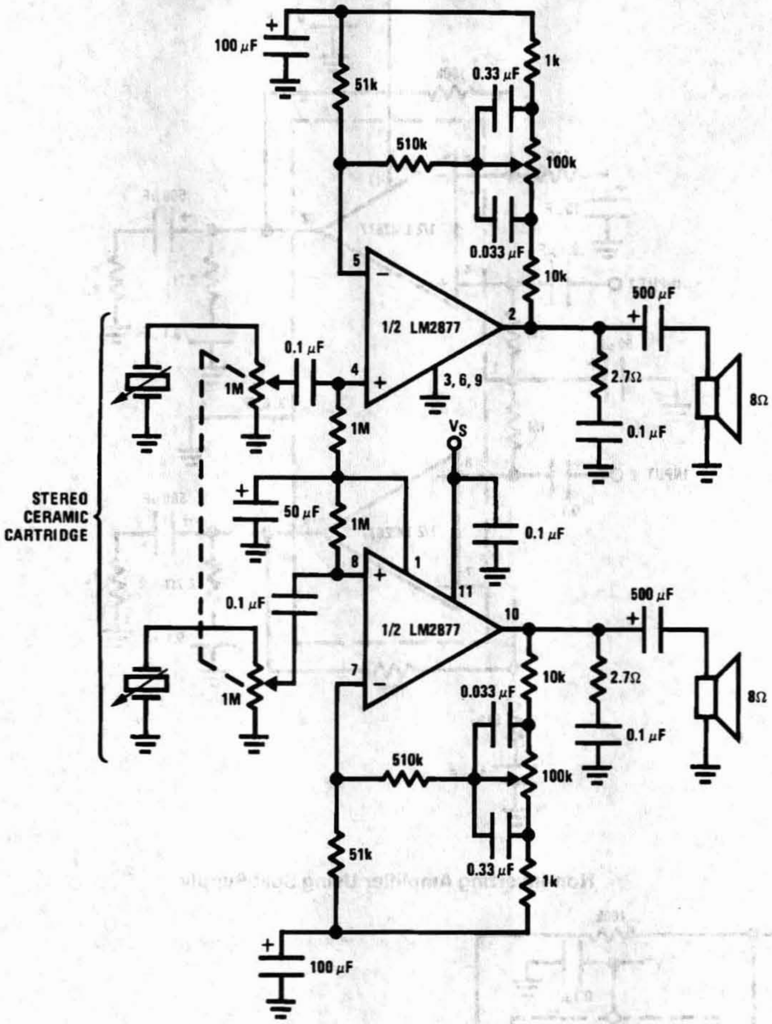
Output Swing vs Supply Voltage



TL/H/7933–3

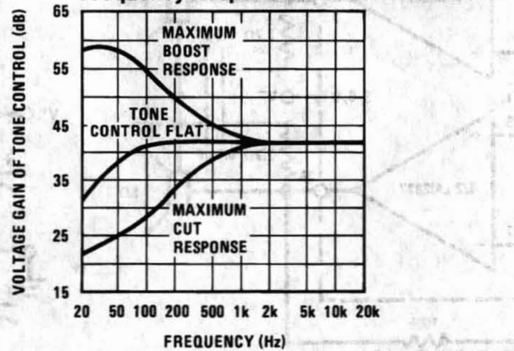
Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control


100 μF
51k
1k
0.33 μF
510k
100k
0.033 μF
10k
5
1/2 LM2877
2
500 μF
8Ω
0.1 μF
4
1M
3, 6, 9
2.7Ω
0.1 μF
V_S
STEREO
CERAMIC
CARTRIDGE
50 μF
1M
8
1
0.1 μF
11
0.1 μF
10
500 μF
1/2 LM2877
7
1M
10k
0.033 μF
2.7Ω
8Ω
0.1 μF
510k
100k
51k
0.33 μF
1k
100 μF

TL/H/7933-4

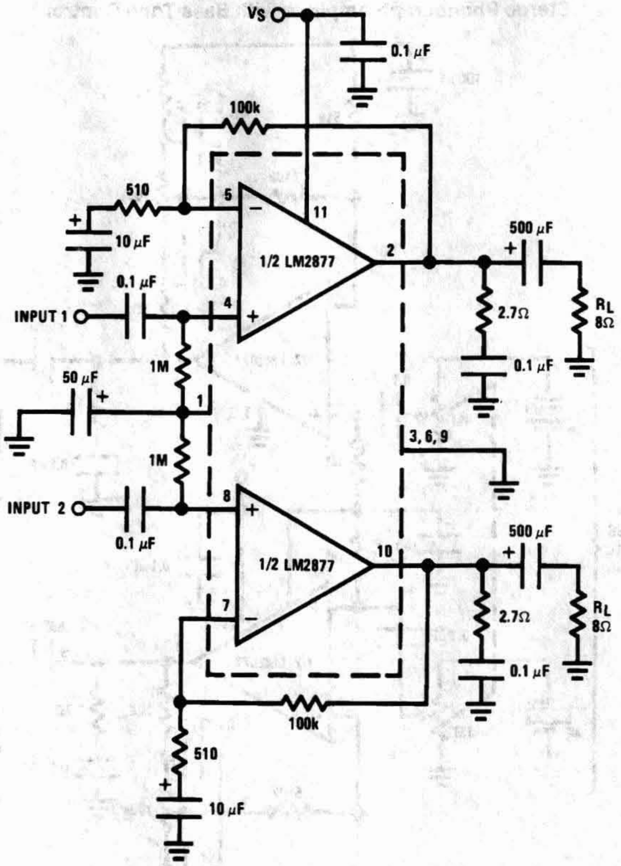
Frequency Response of Bass Tone Control



TL/H/7933-5

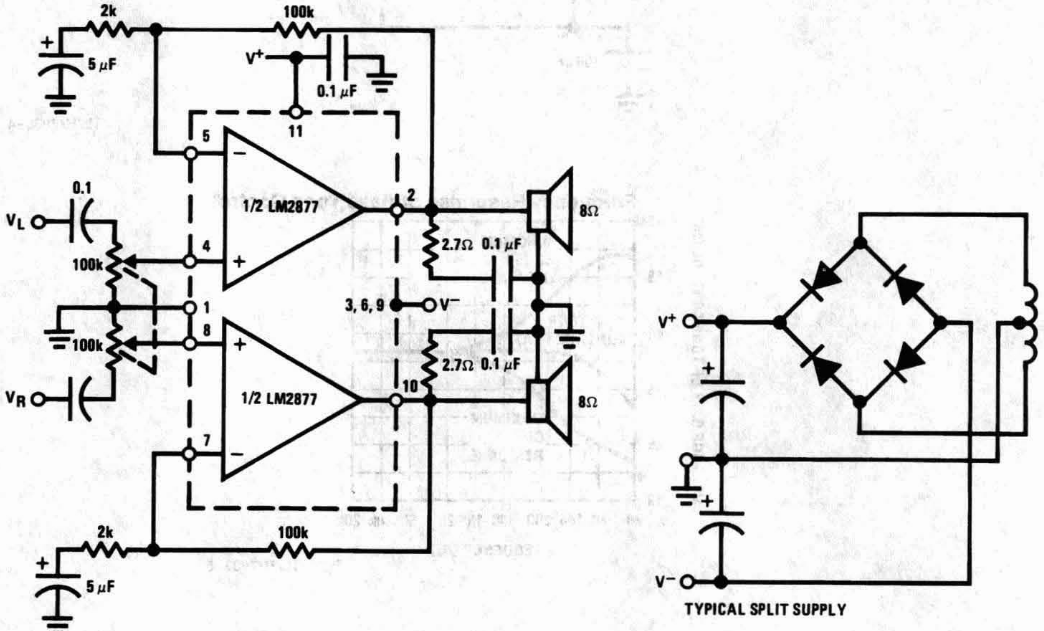
Typical Applications (Continued)

Stereo Amplifier with $A_V = 200$


VS
0.1 μF
100k
510
5
11
+
10 μF
1/2 LM2877
2
500 μF
0.1 μF
INPUT 1
4
2.7Ω
RL
8Ω
0.1 μF
1M
50 μF
1
3, 6, 9
1M
INPUT 2
8
0.1 μF
500 μF
1/2 LM2877
10
7
2.7Ω
RL
8Ω
0.1 μF
100k
510
10 μF

TL/H/7933-6

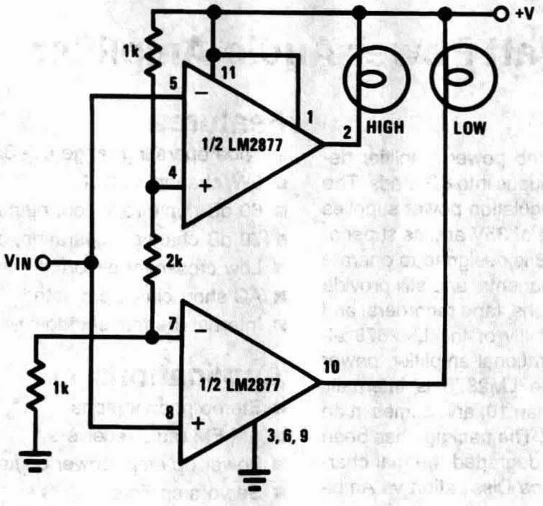
Non-Inverting Amplifier Using Split Supply


2k
100k
5 μF
V+
0.1 μF
11
5
0.1
VL
100k
4
1/2 LM2877
2
8Ω
2.7Ω
0.1 μF
1
3, 6, 9
V−
8
100k
2.7Ω
0.1 μF
VR
1/2 LM2877
10
8Ω
7
2k
100k
5 μF
V+
V−
TYPICAL SPLIT SUPPLY

TL/H/7933-7

Typical Applications (Continued)

Window Comparator Driving High, Low Lamps



TL/H/7933-8

Truth Table

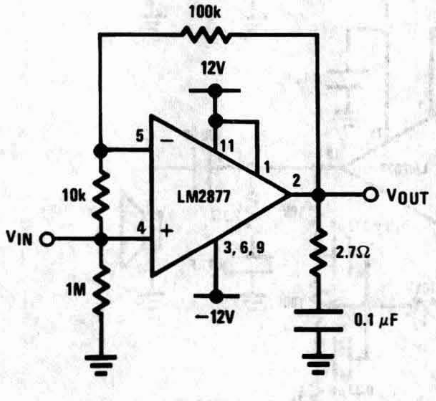
V_{IN}	High	Low
$< \frac{1}{4} V^+$	Off	On
$\frac{1}{4} V^+$ to $\frac{3}{4} V^+$	Off	Off
$> \frac{3}{4} V^+$	On	Off

Application Hints

The LM2877 is an improved LM377 in typical audio applications. In the LM2877, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within ±0.7V of this pin 1 voltage. Nevertheless, the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2877 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may change.

Figure 1 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.



TL/H/7933-9

FIGURE 1

National Semiconductor

LM2878 Dual 5 Watt Power Audio Amplifier

General Description

The LM2878 is a high voltage stereo power amplifier designed to deliver 5W/channel continuous into 8Ω loads. The amplifier is ideal for use with low regulation power supplies due to the absolute maximum rating of 35V and its superior power supply rejection. The LM2878 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders, and AM-FM stereo receivers. The flexibility of the LM2878 allows it to be used as a power operational amplifier, power comparator or servo amplifier. The LM2878 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package (SIP). The package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

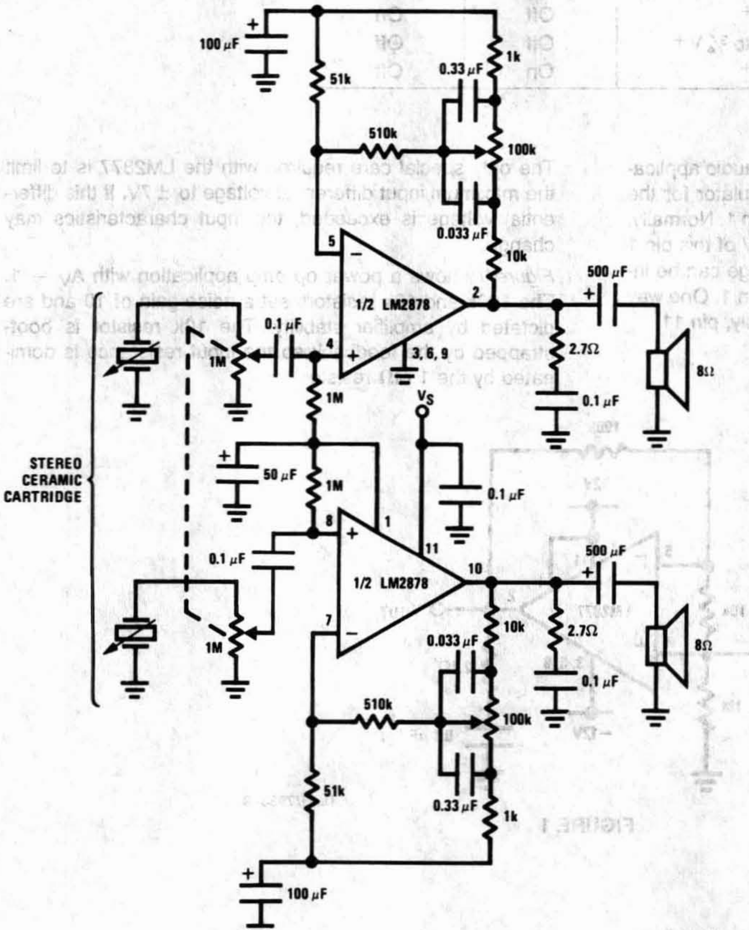
Features

- Wide operating range 6V–32V
- 5W/channel output
- 60 dB ripple rejection, output referred
- 70 dB channel separation, output referred
- Low crossover distortion
- AC short circuit protected
- Internal thermal shutdown

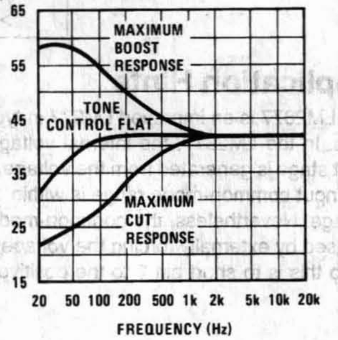
Applications

- Stereo phonographs
- AM-FM radio receivers
- Power op amp, power comparator
- Servo amplifiers

Typical Applications


100 μF
51k
0.33 μF
1k
510k
100k
0.033 μF
10k
5
1/2 LM2878
2
500 μF
0.1 μF
4
3, 6, 9
2.7Ω
8Ω
0.1 μF
1M
1M
V_S
50 μF
1M
0.1 μF
STEREO CERAMIC CARTRIDGE
8
1
11
0.1 μF
1/2 LM2878
10
500 μF
7
1M
0.033 μF
10k
2.7Ω
8Ω
0.1 μF
510k
100k
51k
0.33 μF
1k
100 μF

Frequency Response of Bass Tone Control



TL/H/7934-2

TL/H/7934-1

FIGURE 1. Stereo Phonograph Amplifier with Bass Tone Control

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	35V
Input Voltage (Note 1)	±0.7V
Operating Temperature (Note 2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	+260°C
Thermal Resistance	
θ_{JC}	10°C/W
θ_{JA}	55°C/W

Electrical Characteristics $V_S = 22V$, $T_{TAB} = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB) unless otherwise specified.

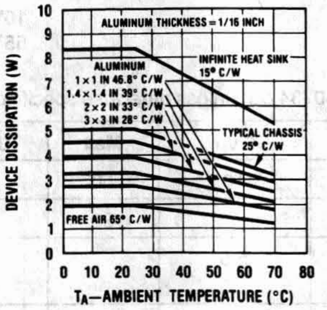
Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	$P_O = 0W$		10	50	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, $T_{TAB} = 25°C$	5	5.5		W
	f = 1 kHz, THD = 10%, $V_S = 12V$		1.3		W
Distortion	f = 1 kHz, $R_L = 8\Omega$ $P_O = 50$ mW		0.20		%
	$P_O = 0.5W$		0.15		%
	$P_O = 2W$		0.14		%
Output Swing	$R_L = 8\Omega$		$V_S - 6V$		Vp-p
Channel Separation	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 1 kHz, Output Referred $V_O = 4$ Vrms	−50	−70		dB
PSRR Power Supply Rejection Ratio	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 120 Hz, Output Referred $V_{ripple} = 1$ Vrms	−50	−60		dB
PSRR Negative Supply	Measured at DC, Input Referred		−60		dB
Common-Mode Range	Split Supplies ±15V, Pin 1 Tied to Pin 11		±13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\ \mu F$ BW = 20 − 20 kHz		2.5		μV
	CCIR•ARM		3.0		μV
	Output Noise Wideband $R_S = 0$, $C_{IN} = 0.1\ \mu F$, $A_V = 200$		0.8		mV
Open Loop Gain	$R_S = 51\Omega$, f = 1 kHz, $R_L = 8\Omega$		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	$V_S = 22V$	10	11	12	V
Slew Rate			2		V/μS
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

Note 1: ±0.7V applies to audio applications; for extended range, see Application Hints.

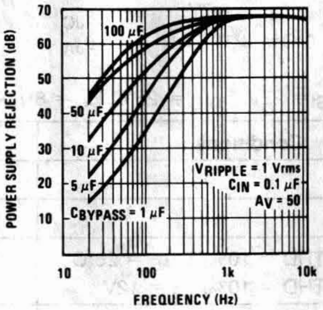
Note 2: For operation at ambient temperature greater than 25°C, the LM2878 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Typical Performance Characteristics

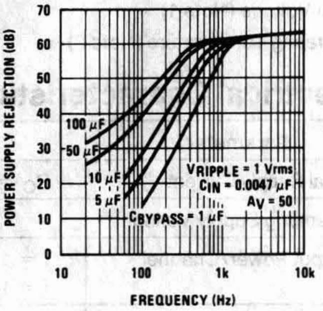
Device Dissipation vs Ambient Temperature



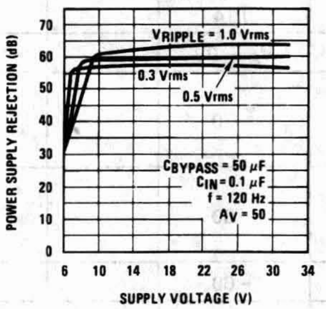
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



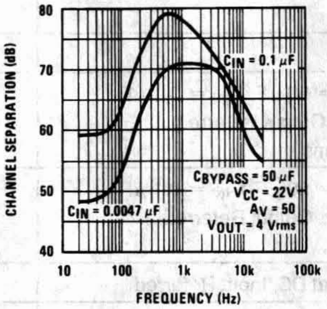
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



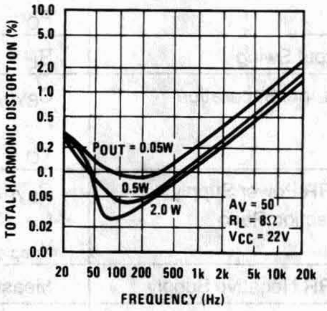
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



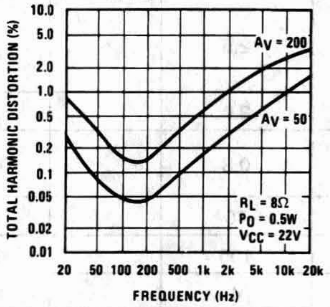
Channel Separation (Referred to the Output) vs Frequency



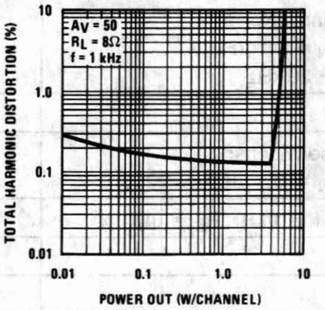
Total Harmonic Distortion vs Frequency



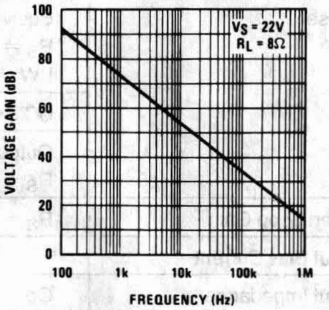
Total Harmonic Distortion vs Frequency



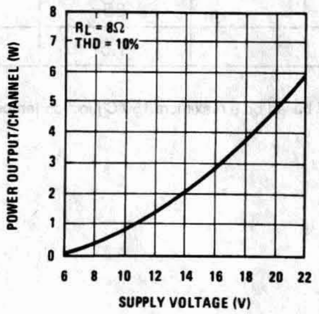
Total Harmonic Distortion vs Power Out



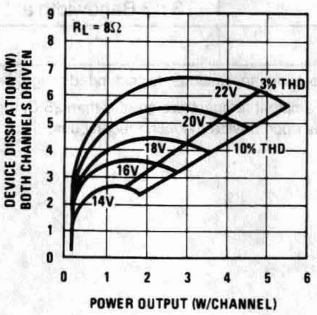
Open Loop Gain vs Frequency



Power Output/Channel vs Supply Voltage

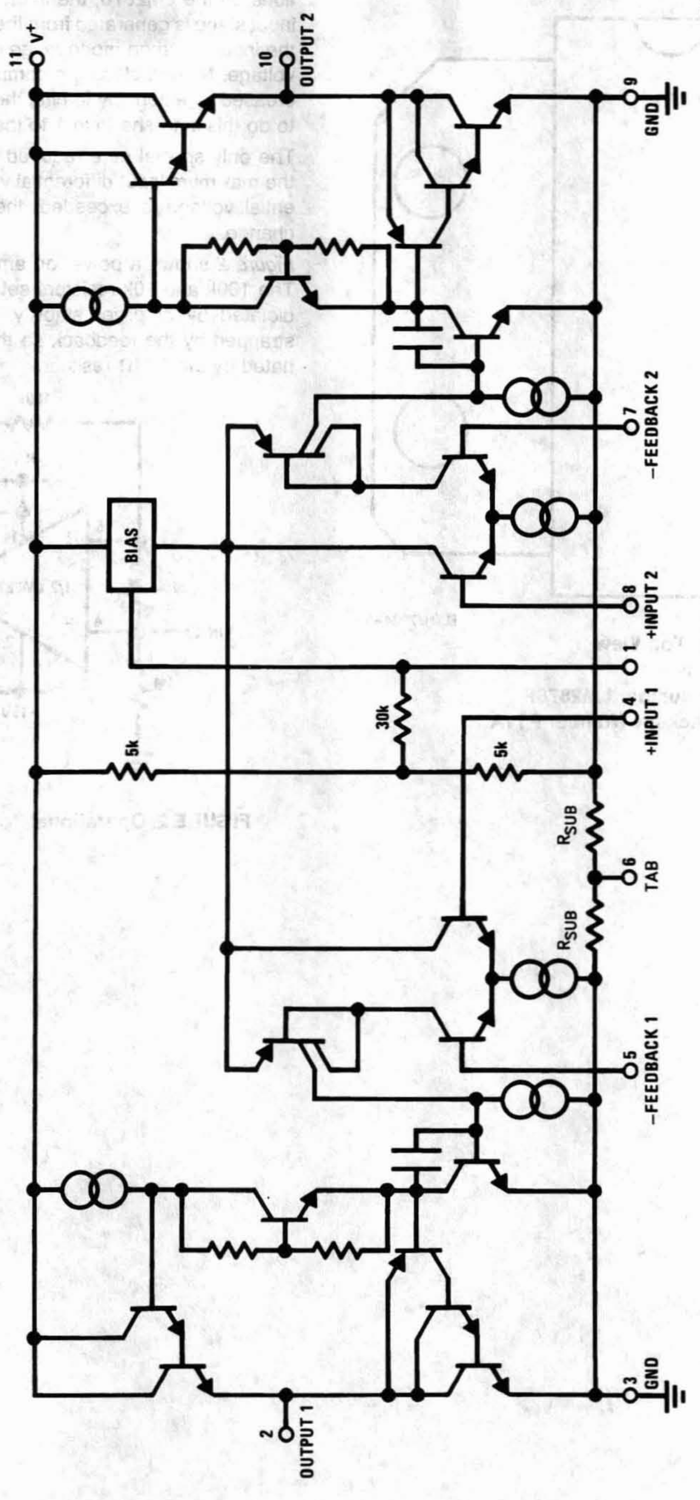


Power Dissipation vs Power Out



TL/H/7934–3

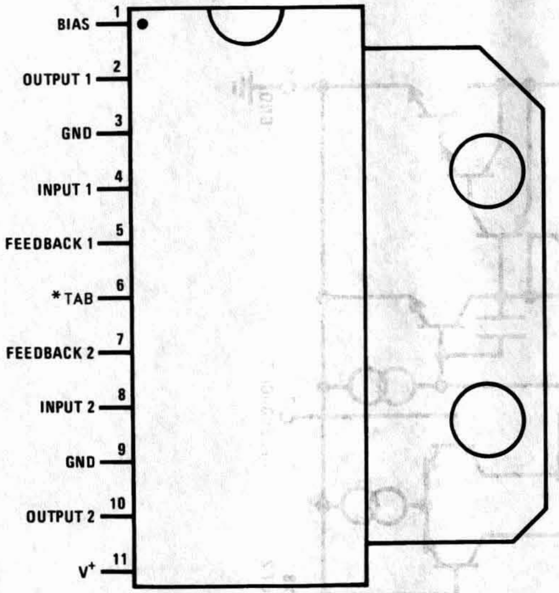
Equivalent Schematic Diagram


11 V+
10 OUTPUT 2
9 GND
7 −FEEDBACK 2
BIAS
8 +INPUT 2
1
30k
4 +INPUT 1
5k
5k
RSUB
6 TAB
RSUB
5 −FEEDBACK 1
3 GND
2 OUTPUT 1

TL/H/7934–4

Connection Diagram

Single-In-Line Package


BIAS
1
OUTPUT 1
2
GND
3
INPUT 1
4
FEEDBACK 1
5
*TAB
6
FEEDBACK 2
7
INPUT 2
8
GND
9
OUTPUT 2
10
V+
11

TL/H/7934-5

Top View

*Pin 6 must be connected to GND.

Order Number LM2878P
See NS Package Number P11A

Application Hints

The LM2878 is an improved LM378 in typical audio applications. In the LM2878, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within ±0.7V of this pin 1 voltage. Nevertheless the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2878 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may change.

Figure 2 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.

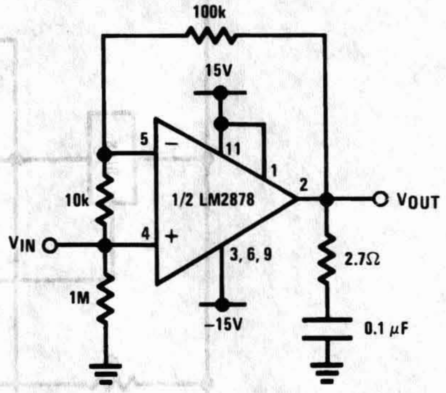

100k
15V
5
−
11
1
2
1/2 LM2878
VOUT
10k
VIN
4
+
3, 6, 9
2.7Ω
1M
−15V
0.1 μF

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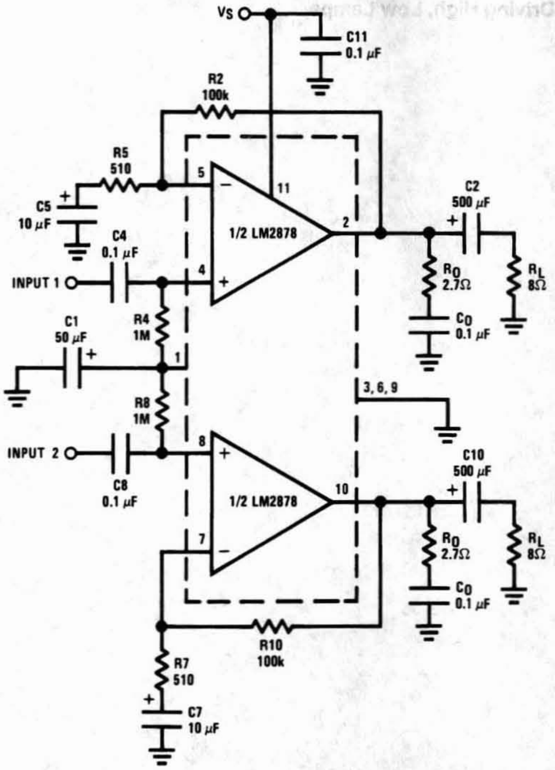
FIGURE 2. Operational Power Amplifier, $A_V = 1$

External Components *(Figure 3)*

1.	R2, R5, R7, R10	Sets voltage gain $A_V = 1 + R2/R5$ for one channel and $A_V = 1 + R10/R7$ for the other channel.
2.	R4, R8	Resistors set input impedance and supply bias current for the positive input.
3.	R_O	Works with C_O to stabilize output stage.
4.	C1	Improves power supply rejection (see Typical Performance Characteristics).
5.	C11	Stabilizes amplifier, may need to be larger depending on power supply filtering.
6.	C4, C8	Input coupling capacitor. Pins 4 and 8 are at a DC potential of $V_S/2$. Low frequency pole set by: $f_L = \frac{1}{2\pi R4C4}$
7.	C5, C7	Feedback capacitors. Ensure unity gain at DC. Also low frequency pole at: $f_L = \frac{1}{2\pi R5C5}$
8.	C_O	Works with R_O to stabilize output stage.
9.	C2, C10	Output coupling capacitor. Low frequency pole given by: $f_L = \frac{1}{R\pi RLC2}$

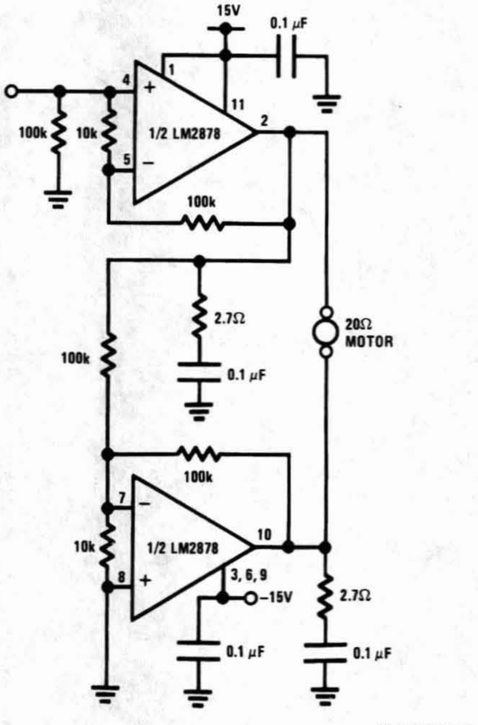
Typical Applications (Continued)



VS
C11
0.1 µF
R2
100k
R5
510
5
11
C5
10 µF
C4
0.1 µF
INPUT 1
4
1/2 LM2878
2
C2
500 µF
R0
2.7Ω
RL
8Ω
C0
0.1 µF
C1
50 µF
R4
1M
1
R8
1M
3, 6, 9
INPUT 2
8
C8
0.1 µF
1/2 LM2878
10
C10
500 µF
R0
2.7Ω
RL
8Ω
C0
0.1 µF
7
R10
100k
R7
510
C7
10 µF

TL/H/7934-7

FIGURE 3. Stereo Amplifier with $A_V = 200$

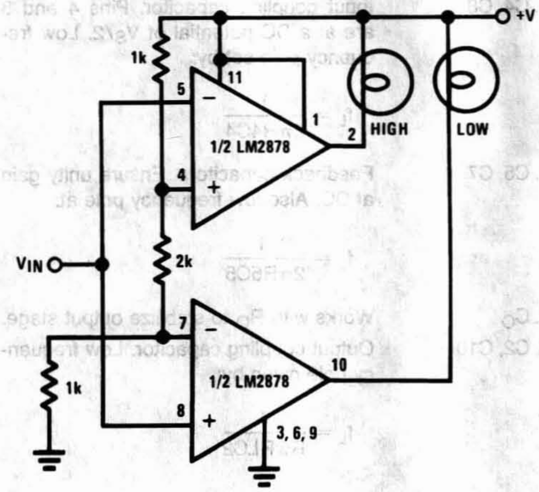


15V
0.1 µF
4
1
11
100k
10k
1/2 LM2878
2
5
100k
2.7Ω
20Ω
MOTOR
100k
0.1 µF
100k
7
1/2 LM2878
10
10k
8
3, 6, 9
−15V
2.7Ω
0.1 µF
0.1 µF

TL/H/7934-8

FIGURE 4. LM2878 Servo Amplifier in Bridge Configuration

Typical Applications (Continued)


+V
1k
11
5
−
1/2 LM2878
1
2
HIGH
LOW
4
+
2k
V_IN
7
−
1/2 LM2878
10
1k
8
+
3, 6, 9

Truth Table

V_{IN}	High	Low
$<\frac{1}{4}V^+$	Off	On
$\frac{1}{4}V^+$ to $\frac{3}{4}V^+$	Off	Off
$>\frac{3}{4}V^+$	On	Off

TL/H/7934–9

FIGURE 5. Window Comparator Driving High, Low Lamps

National Semiconductor

LM2879 Dual 8W Audio Amplifier

General Description

The LM2879 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, AM-FM stereo receivers, etc.

The LM2879 will deliver 8W/channel to an 8Ω load. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown.

Features

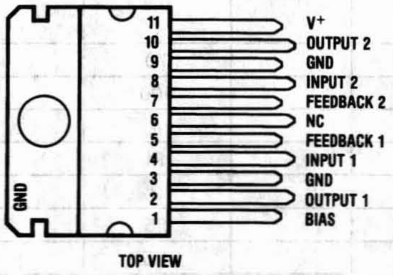
- A_{VO} typical 90 dB
- 9W per channel (typical)
- 60 dB ripple rejection
- 70 dB channel separation
- Self-centering biasing
- 4 MΩ input impedance
- Internal current limiting
- Internal thermal protection

Applications

- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Connection Diagram and Typical Application

Plastic Package

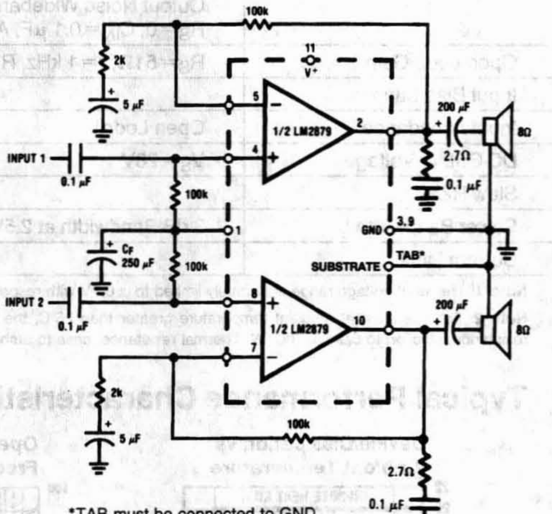

11
10
9
8
7
6
5
4
3
2
1
GND
V+
OUTPUT 2
GND
INPUT 2
FEEDBACK 2
NC
FEEDBACK 1
INPUT 1
GND
OUTPUT 1
BIAS

TOP VIEW

TL/H/5291-1

Order Number LM2879T
See NS Package Number TA11B

Stereo Amplifier


100k
11
V+
2k
5 µF
5
1/2 LM2879
2
200 µF
8Ω
INPUT 1
0.1 µF
4
2.7Ω
0.1 µF
100k
1
GND
3, 9
Cf
250 µF
100k
TAB*
SUBSTRATE
INPUT 2
0.1 µF
8
1/2 LM2879
10
200 µF
8Ω
7
2k
5 µF
100k
2.7Ω
0.1 µF

*TAB must be connected to GND.

TL/H/5291-2

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	35V
Input Voltage (Note 1)	±0.7V
Operating Temperature (Note 2)	0°C to + 70°C
Storage Temperature	−65°C to + 150°C
Junction Temperature	150°C
Lead Temp. (Soldering, 10 seconds)	260°C
ESD rating to be determined.	
Thermal Resistance	
θ_{JC}	1°C/W
θ_{JA}	43°C/W

Electrical Characteristics $V_S = 28V$, $T_{TAB} = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB), unless otherwise specified.

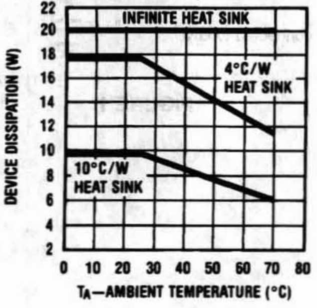
Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	$P_O = 0W$		12	65	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, $T_{TAB} = 25°C$	6	8		W
Distortion	f = 1 kHz, $R_L = 8\Omega$ $P_O = 1$ W/Channel		0.05	1	%
Output Swing	$R_L = 8\Omega$		$V_S - 6V$		Vp-p
Channel Separation	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 1 kHz, Output Referred $V_O = 4$ Vrms	−50	−70		dB
PSRR Positive Supply	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 120 Hz, Output Referred $V_{ripple} = 1$ Vrms	−50	−60		dB
PSRR Negative Supply	Measured at DC, Input Referred		−60		dB
Common-Mode Range	Split Supplies ±15V, Pin 1 Tied to Pin 11		±13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\ \mu F$ BW = 20 − 20 kHz CCIR•ARM Output Noise Wideband $R_S = 0$, $C_{IN} = 0.1\ \mu F$, $A_V = 200$		 2.5 3.0 0.8		 μV μV mV
Open Loop Gain	$R_S = 51\Omega$, f = 1 kHz, $R_L = 8\Omega$		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	$V_S = 28V$		14		V
Slew Rate			2		V/μs
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

Note 1: The input voltage range is normally limited to ±0.7V with respect to pin 1. This range may be extended by shorting pin 1 to the positive supply.

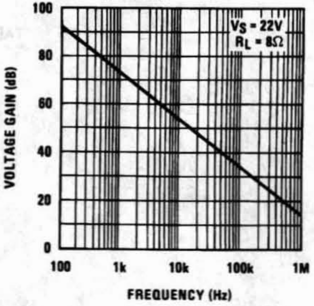
Note 2: For operation at ambient temperature greater than 25°C, the LM2879 must be derated based on a maximum 150°C junction temperature. Thermal resistance, junction to case, is 3°C/W. Thermal resistance, case to ambient, is 40°C/W.

Typical Performance Characteristics

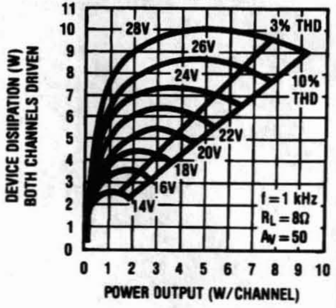
Device Dissipation vs Ambient Temperature



Open Loop Gain vs Frequency



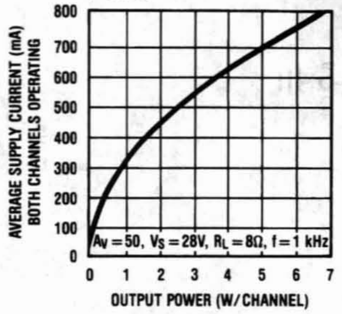
Power Dissipation vs Power Output



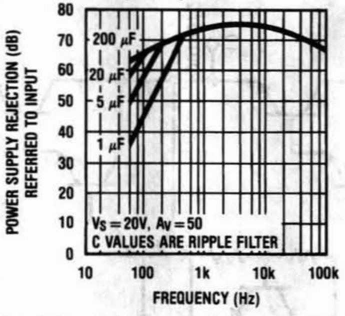
TL/H/5291–3

Typical Performance Characteristics (Continued)

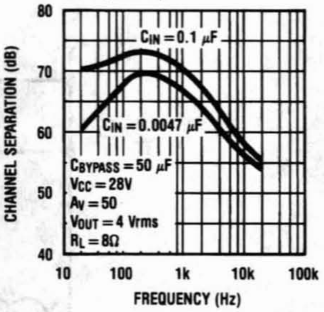
Supply Current vs Output Power



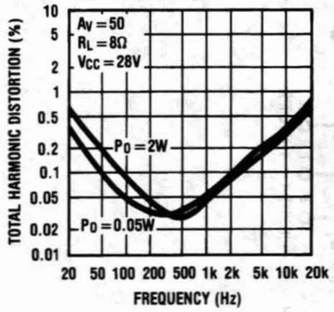
Supply Rejection vs Frequency



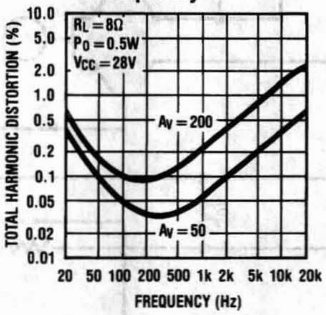
Channel Separation (Referred to the Output) Frequency



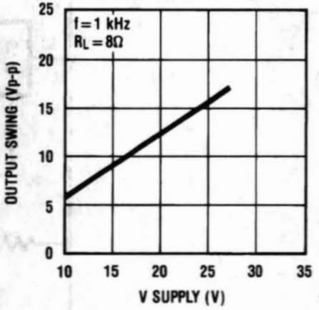
Total Harmonic Distortion vs Frequency



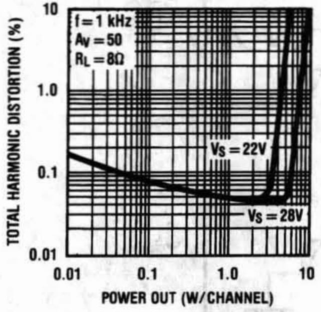
Total Harmonic Distortion vs Frequency



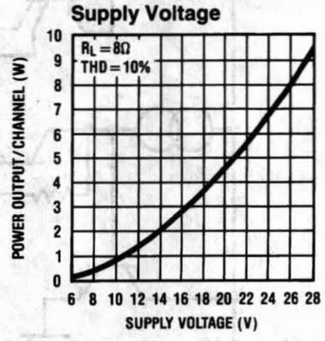
Output Swing vs V_S



Total Harmonic Distortion vs Power Output

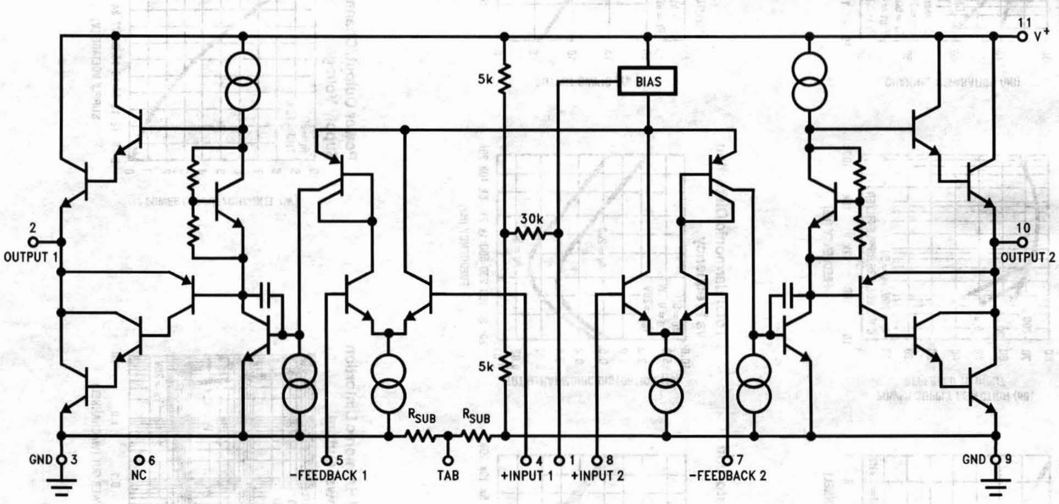


Power Output/Channel vs Supply Voltage



TL/H/5291–4

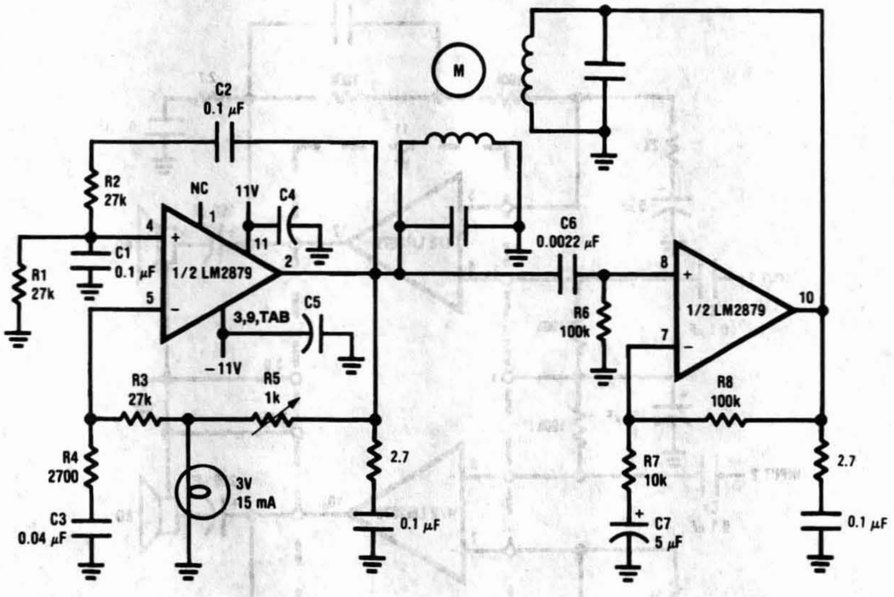
Equivalent Schematic Diagram


11
V+
BIAS
5k
30k
5k
2
OUTPUT 1
10
OUTPUT 2
R_SUB
R_SUB
GND 3
6
NC
5
-FEEDBACK 1
TAB
4
+INPUT 1
1
8
+INPUT 2
7
-FEEDBACK 2
GND 9

TL/H/5291-5

Typical Applications

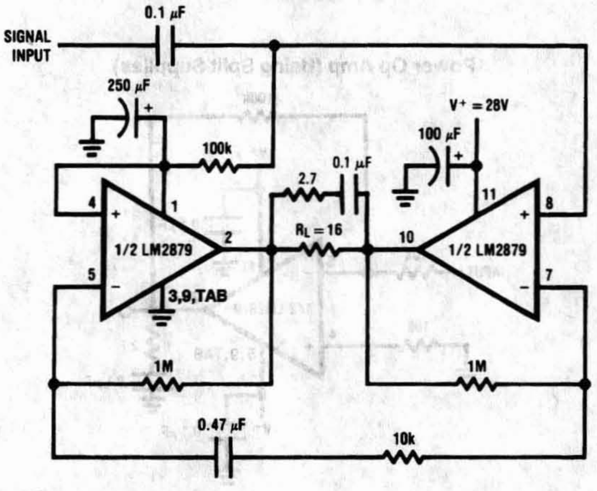
Two-Phase Motor Drive



M
C2
0.1 µF
R2
27k
NC
11V
C4
4
1
11
+
C1
0.1 µF
R1
27k
1/2 LM2879
2
5
−
C5
3,9,TAB
−11V
R3
27k
R5
1k
R4
2700
3V
15 mA
2.7
0.1 µF
C3
0.04 µF
C6
0.0022 µF
R6
100k
8
+
1/2 LM2879
10
7
−
R8
100k
R7
10k
C7
5 µF
2.7
0.1 µF

TL/H/5291-6

12W Bridge Amplifier

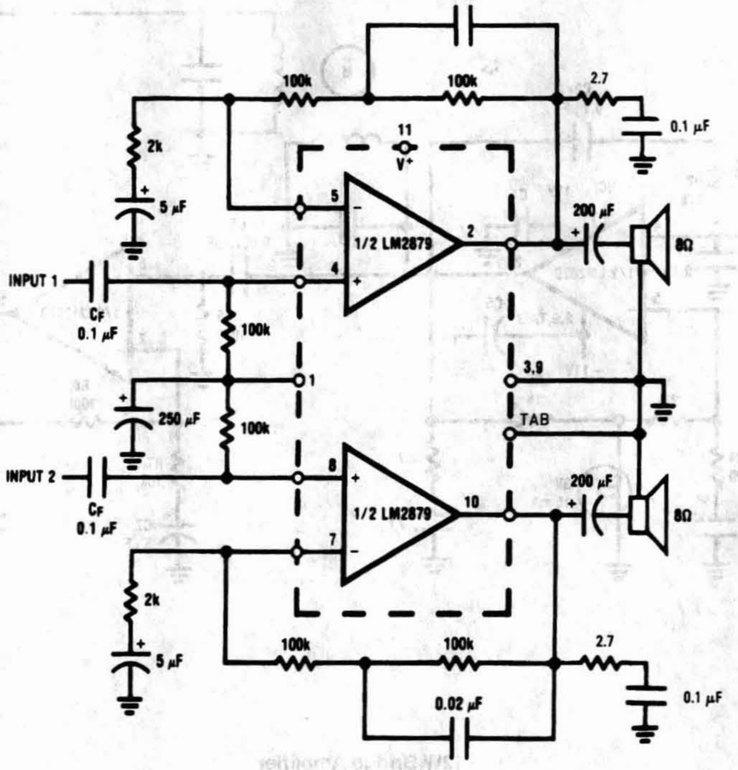


SIGNAL
INPUT
0.1 µF
250 µF
100k
4
1
+
1/2 LM2879
2
5
−
3,9,TAB
2.7
0.1 µF
$R_L = 16$
10
V+ = 28V
100 µF
11
8
1/2 LM2879
7
1M
1M
0.47 µF
10k

TL/H/5291-7

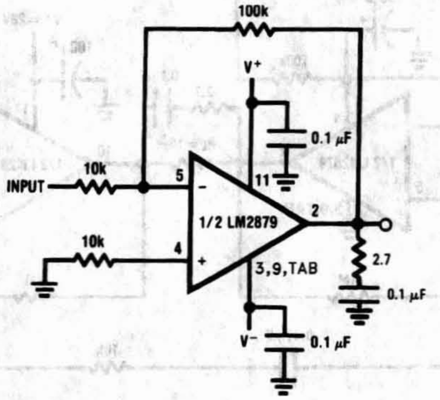
Typical Applications (Continued)

Simple Stereo Amplifier with Bass Boost


0.02 μF
100k
100k
2.7
0.1 μF
2k
11
V+
5 μF
5
–
1/2 LM2879
2
200 μF
+
8Ω
INPUT 1
4
+
CF
0.1 μF
100k
1
3,9
250 μF
100k
TAB
INPUT 2
8
+
200 μF
CF
0.1 μF
1/2 LM2879
10
+
8Ω
7
–
2k
5 μF
100k
100k
2.7
0.02 μF
0.1 μF

TL/H/5291–8

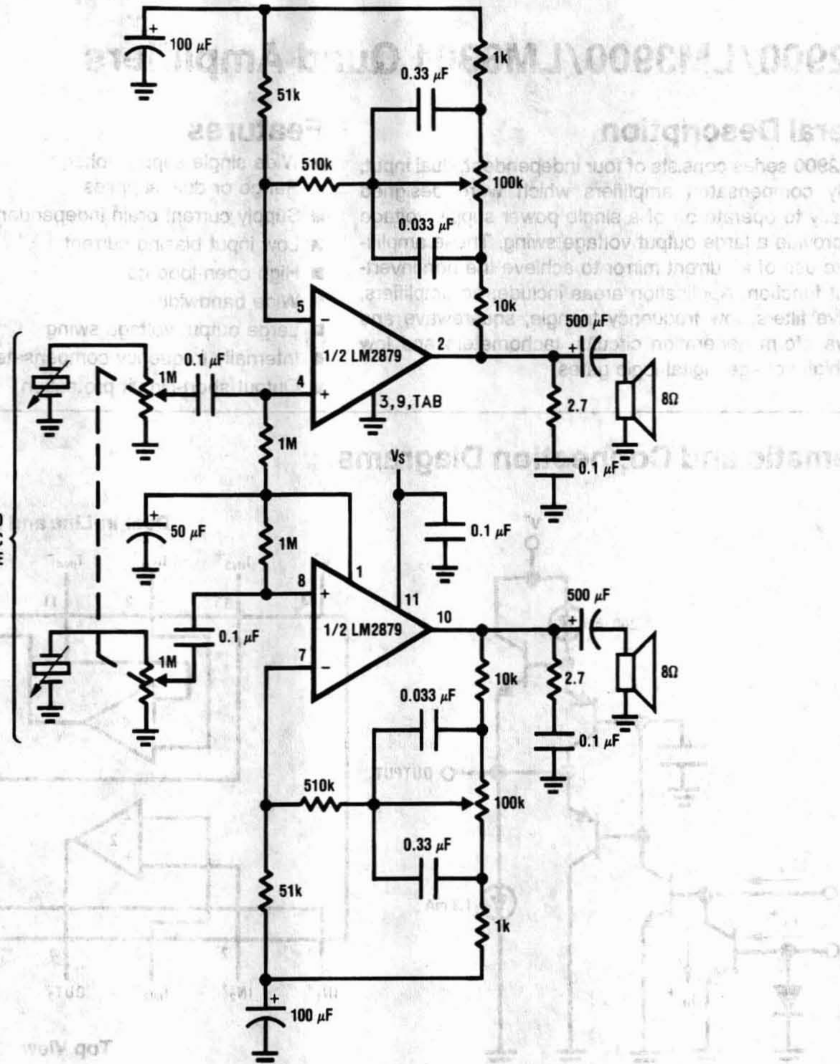
Power Op Amp (Using Split Supplies)


100k
V+
0.1 μF
10k
INPUT
5
–
11
1/2 LM2879
2
10k
4
+
3,9,TAB
2.7
0.1 μF
V–
0.1 μF

TL/H/5291–9

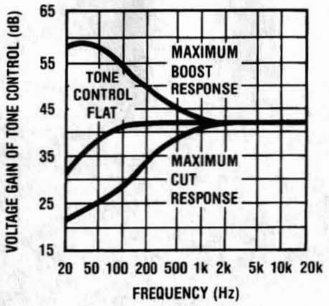
Typical Applications (Continued)

Stereo Phonograph Amplifier with Bass Tone Control


100 µF
51k
1k
0.33 µF
510k
100k
0.033 µF
10k
5
2
500 µF
1/2 LM2879
0.1 µF
1M
4
3,9,TAB
2.7
8Ω
1M
Vs
0.1 µF
STEREO
CERAMIC
CARTRIDGE
50 µF
1M
1
8
11
10
500 µF
1/2 LM2879
0.1 µF
1M
7
10k
2.7
8Ω
0.033 µF
0.1 µF
510k
100k
0.33 µF
51k
1k
100 µF

TL/H/5291-10

Frequency Response of Bass Tone Control



TL/H/5291-11

National Semiconductor

LM2900/LM3900/LM3301 Quad Amplifiers

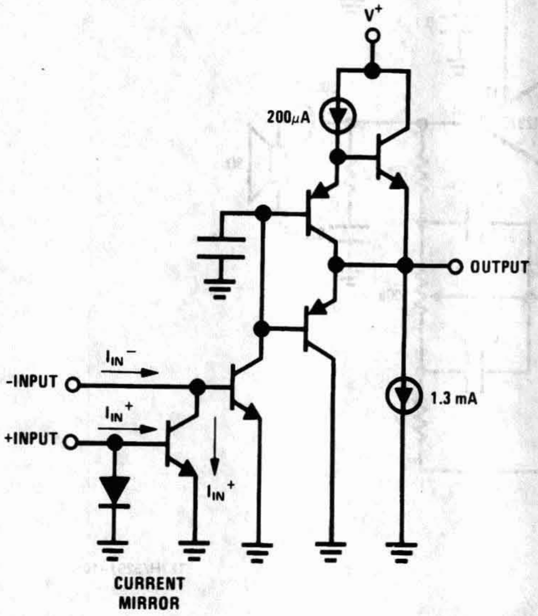
General Description

The LM2900 series consists of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off of a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: ac amplifiers, RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

Features

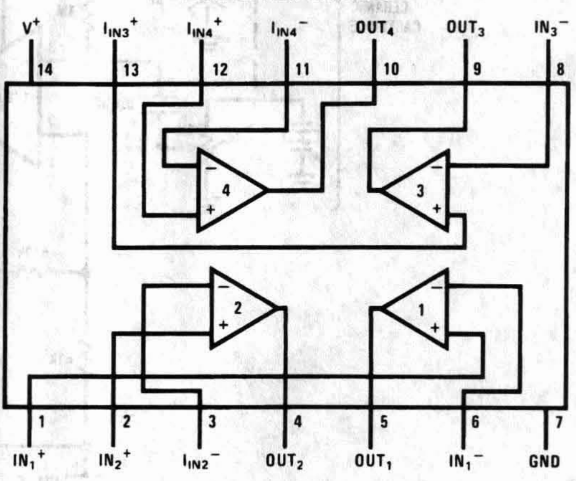
■ Wide single supply voltage	4 V_{DC} to 32 V_{DC}
Range or dual supplies	±2 V_{DC} to ±16 V_{DC}
■ Supply current drain independent of supply voltage	
■ Low input biasing current	30 nA
■ High open-loop gain	70 dB
■ Wide bandwidth	2.5 MHz (unity gain)
■ Large output voltage swing	$(V^+ - 1)$ Vp-p
■ Internally frequency compensated for unity gain	
■ Output short-circuit protection	

Schematic and Connection Diagrams


V+
200μA
OUTPUT
1.3 mA
I_{IN}^-
-INPUT
I_{IN}^+
+INPUT
I_{IN}^+
CURRENT MIRROR

TL/H/7936-1

Dual-In-Line and S.O.


V+
I_{IN3}^+
I_{IN4}^+
I_{IN4}^-
OUT_4
OUT_3
IN_3^-
14
13
12
11
10
9
8
4
3
2
1
1
2
3
4
5
6
7
IN_1^+
IN_2^+
I_{IN2}^-
OUT_2
OUT_1
IN_1^-
GND

TL/H/7936-2

Top View

Order Number LM2900N, LM3900M, LM3900N or LM3301N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM2900/LM3900	LM3301
Supply Voltage	32 V_{DC} ±16 V_{DC}	28 V_{DC} ±14 V_{DC}
Power Dissipation ($T_A = 25°C$) (Note 1)		
Molded DIP	1080 mW	1080 mW
S.O. Package	765 mW	
Input Currents, I_{IN}^+ or I_{IN}^-	20 mA_{DC}	20 mA_{DC}
Output Short-Circuit Duration—One Amplifier $T_A = 25°C$ (See Application Hints)	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM2900	−40°C to +85°C	
LM3900	0°C to +70°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 sec.)	260°C	260°C
Small Outline Package		
Vapor Phase (60 sec.)	215°C	215°C
Infrared (15 sec.)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 7)	2000V	2000V

Electrical Characteristics $T_A = 25°C, V^+ = 15\ V_{DC}$, unless otherwise stated

Parameter		Conditions		LM2900			LM3900			LM3301			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Open Loop	Voltage Gain	Over Temp.											V/mV
	Voltage Gain	$\Delta V_O = 10\ V_{DC}$ Inverting Input		1.2	2.8		1.2	2.8		1.2	2.8		
	Input Resistance				1			1			1		MΩ
	Output Resistance				8			8			9		kΩ
Unity Gain Bandwidth		Inverting Input			2.5			2.5			2.5		MHz
Input Bias Current		Inverting Input, $V^+ = 5\ V_{DC}$ Inverting Input			30	200		30	200		30	300	nA
Slew Rate		Positive Output Swing Negative Output Swing			0.5 20			0.5 20			0.5 20		V/μs
Supply Current		$R_L = \infty$ On All Amplifiers			6.2	10		6.2	10		6.2	10	mA_{DC}
Output Voltage Swing	V_{OUT} High	$R_L = 2k$, $V^+ = 15.0\ V_{DC}$	$I_{IN}^- = 0$, $I_{IN}^+ = 0$	13.5			13.5			13.5			V_{DC}
	V_{OUT} Low		$I_{IN}^- = 10\ \mu A$, $I_{IN}^+ = 0$		0.09	0.2		0.09	0.2		0.09	0.2	
	V_{OUT} High	V^+ = Absolute Maximum Ratings	$I_{IN}^- = 0$, $I_{IN}^+ = 0$ $R_L = \infty$,	29.5			29.5			26.0			
Output Current Capability	Source			6	18		6	10		5	18		mA_{DC}
	Sink	(Note 2)		0.5	1.3		0.5	1.3		0.5	1.3		
	I_{SINK}	$V_{OL} = 1V, I_{IN}^- = 5\ \mu A$			5			5			5		

Electrical Characteristics (Note 6), $V^{+} = 15\ V_{DC}$, unless otherwise stated (Continued)

Parameter	Conditions	LM2900			LM3900			LM3301			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Rejection	$T_A = 25°C$, f = 100 Hz		70			70			70		dB
Mirror Gain	@ 20 µA (Note 3)	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1	1.10	µA/µA
	@ 200 µA (Note 3)	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1	1.10	
ΔMirror Gain	@ 20 µA to 200 µA (Note 3)		2	5		2	5		2	5	%
Mirror Current	(Note 4)		10	500		10	500		10	500	$µA_{DC}$
Negative Input Current	$T_A = 25°C$ (Note 5)		1.0			1.0			1.0		mA_{DC}
Input Bias Current	Inverting Input		300			300					nA

Note 1: For operating at high temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 92°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. Thermal resistance for the S.O. package is 131°C/W.

Note 2: The output current sink capability can be increased for large signal conditions by overdriving the inverting input. This is shown in the section on Typical Characteristics.

Note 3: This spec indicates the current gain of the current mirror which is used as the non-inverting input.

Note 4: Input V_{BE} match between the non-inverting and the inverting inputs occurs for a mirror current (non-inverting input current) of approximately 10 µA. This is therefore a typical design center for many of the application circuits.

Note 5: Clamp transistors are included on the IC to prevent the input voltages from swinging below ground more than approximately $-0.3\ V_{DC}$. The negative input currents which may result from large signal overdrive with capacitance input coupling need to be externally limited to values of approximately 1 mA. Negative input currents in excess of 4 mA will cause the output voltage to drop to a low voltage. This maximum current applies to any one of the input terminals. If more than one of the input terminals are simultaneously driven negative smaller maximum currents are allowed. Common-mode current biasing can be used to prevent negative input voltages; see for example, the "Differentiator Circuit" in the applications section.

Note 6: These specs apply for $-40°C \leq T_A \leq +85°C$, unless otherwise stated.

Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Application Hints

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak input current. Currents as large as 20 mA will not damage the device, but the current mirror on the non-inverting input will saturate and cause a loss of mirror gain at mA current levels—especially at high operating temperatures.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example, when operating from a well-regulated $+5\ V_{DC}$ power supply at $T_A = 25°C$ with a 100 kΩ shunt-feedback resistor (from the output to the inverting input) a short directly to the power supply will not cause catastrophic failure but the current magnitude will be approximately 50 mA and the junction temperature will be above T_J max. Larger feedback resistors will reduce the current, 11 MΩ provides approximately 30 mA, an open circuit provides 1.3 mA, and a direct connection from the output to the non-inverting input will result in catastrophic failure when the output is shorted to V^{+} as this then places the base-emitter junction of the input transistor directly across the power supply. Short-circuits to ground will have magnitudes of approximately 30 mA and will not cause catastrophic failure at $T_A = 25°C$.

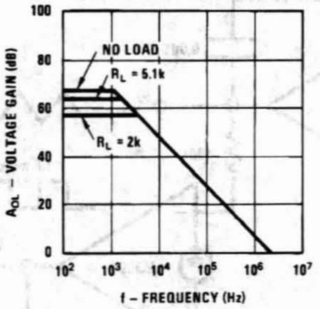
Unintentional signal coupling from the output to the non-inverting input can cause oscillations. This is likely only in breadboard hook-ups with long component leads and can be prevented by a more careful lead dress or by locating the non-inverting input biasing resistor close to the IC. A quick check of this condition is to bypass the non-inverting input to ground with a capacitor. High impedance biasing resistors used in the non-inverting input circuit make this input lead highly susceptible to unintentional AC signal pickup.

Operation of this amplifier can be best understood by noticing that input currents are differenced at the inverting-input terminal and this difference current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near ground or even negative as this maintains the inputs biased at $+V_{BE}$. Internal clamp transistors (see note 5) catch-negative input voltages at approximately $-0.3\ V_{DC}$ but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately 100 µA.

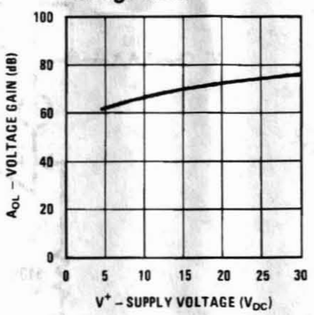
This new "Norton" current-differencing amplifier can be used in most of the applications of a standard IC op amp. Performance as a DC amplifier using only a single supply is not as precise as a standard IC op amp operating with split supplies but is adequate in many less critical applications. New functions are made possible with this amplifier which are useful in single power supply systems. For example, biasing can be designed separately from the AC gain as was shown in the "inverting amplifier," the "difference integrator" allows controlling the charging and the discharging of the integrating capacitor with positive voltages, and the "frequency doubling tachometer" provides a simple circuit which reduces the ripple voltage on a tachometer output DC voltage.

Typical Performance Characteristics

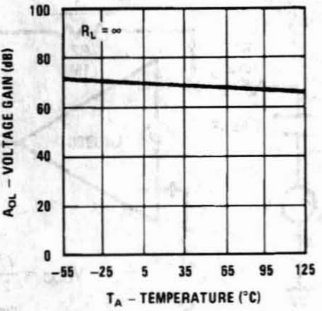
Open Loop Gain



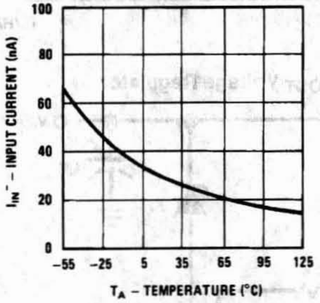
Voltage Gain



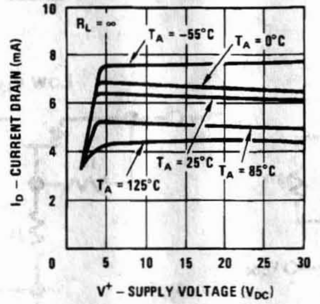
Voltage Gain



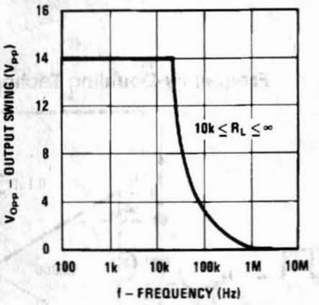
Input Current



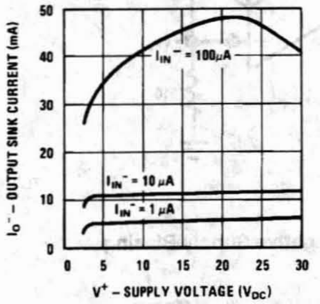
Supply Current



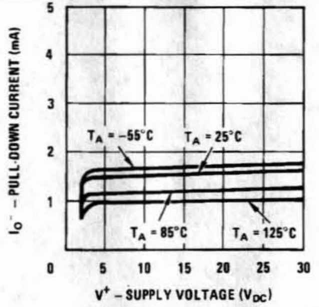
Large Signal Frequency Response



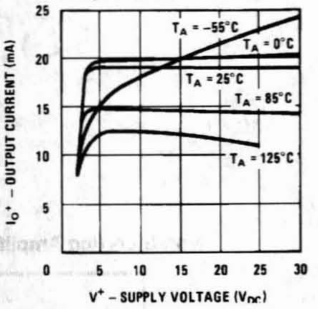
Output Sink Current



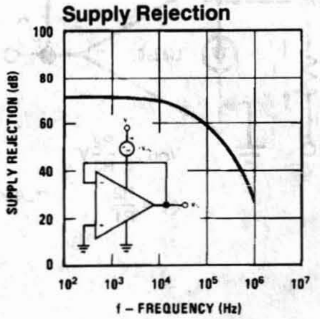
Output Class-A Bias Current



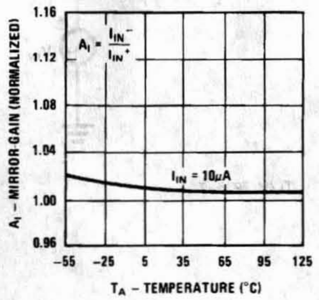
Output Source Current



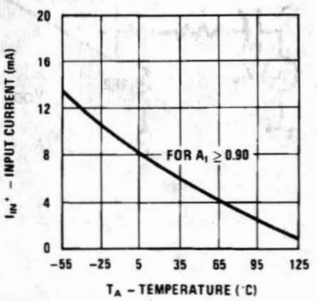
Supply Rejection



Mirror Gain



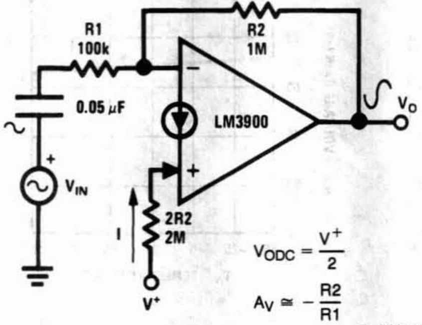
Maximum Mirror Current



TL/H/7936–9

Typical Applications ($V^+ = 15\ V_{DC}$)

Inverting Amplifier

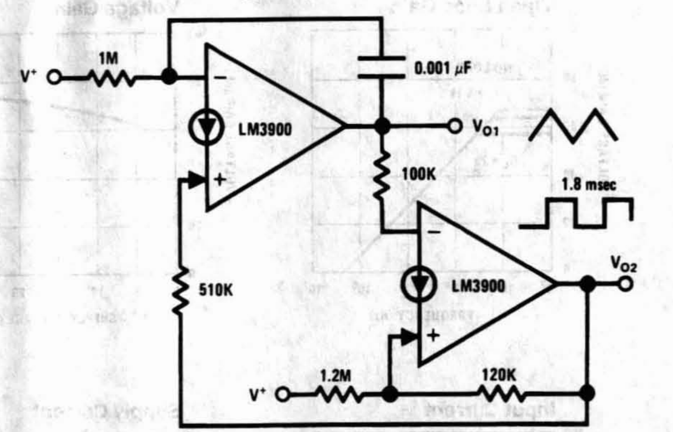

I
R2
1M
R1
100k
0.05 µF
LM3900
V_O
V_IN
2R2
2M
I
V+

$$V_{ODC} = \frac{V^+}{2}$$

$$A_V \cong -\frac{R2}{R1}$$

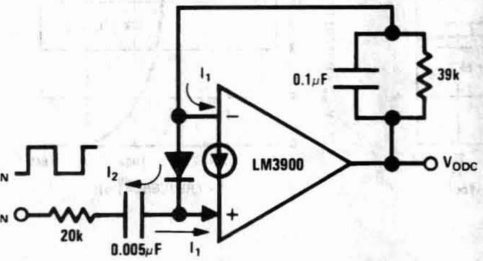
TL/H/7936-3

Triangle/Square Generator


V+
1M
0.001 µF
LM3900
V_O1
100K
1.8 msec
510K
LM3900
V_O2
V+
1.2M
120K

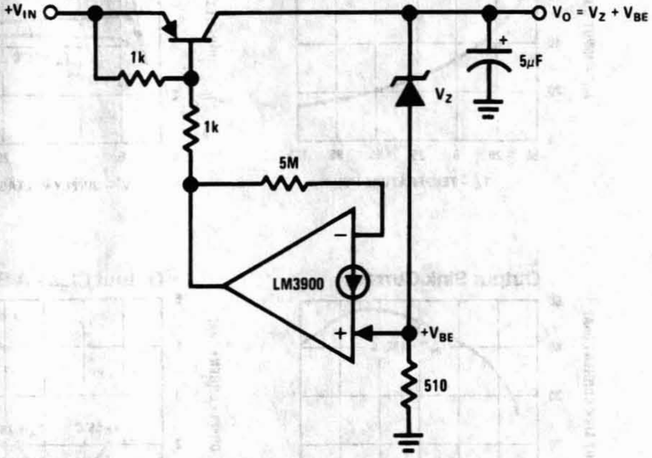
TL/H/7936-4

Frequency-Doubling Tachometer


I1
0.1µF
39k
V_IN
I2
LM3900
V_ODC
f_IN
20k
0.005µF
I1

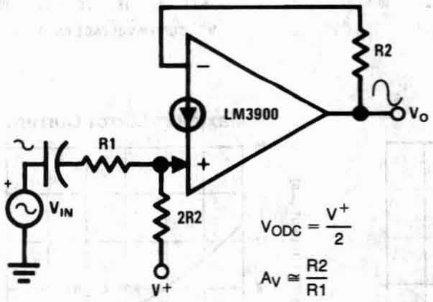
TL/H/7936-5

Low $V_{IN} - V_{OUT}$ Voltage Regulator


+V_IN
V_O = V_Z + V_BE
1k
5µF
V_Z
1k
5M
LM3900
+V_BE
510

TL/H/7936-6

Non-Inverting Amplifier

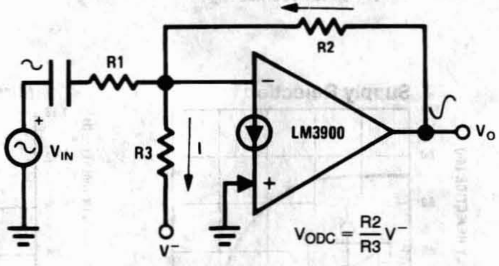

R2
LM3900
V_O
R1
V_IN
2R2
V+

$$V_{ODC} = \frac{V^+}{2}$$

$$A_V \cong \frac{R2}{R1}$$

TL/H/7936-7

Negative Supply Biasing


I
R2
R1
LM3900
V_O
V_IN
R3
I
V−

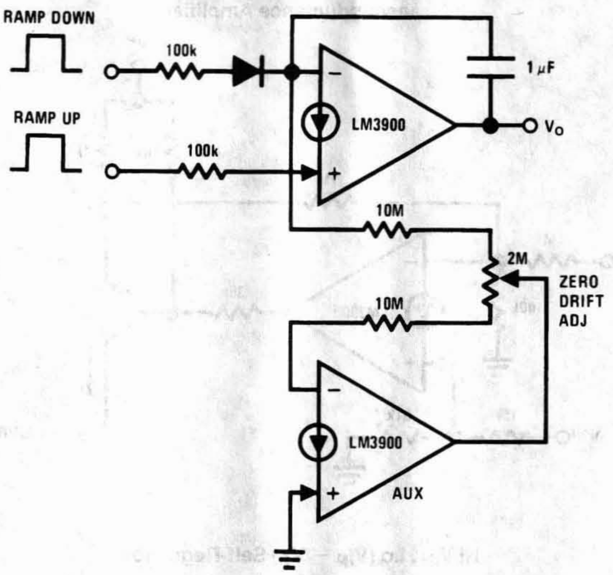
$$V_{ODC} = \frac{R2}{R3} V^-$$

$$A_V \cong \frac{R2}{R1}$$

TL/H/7936-8

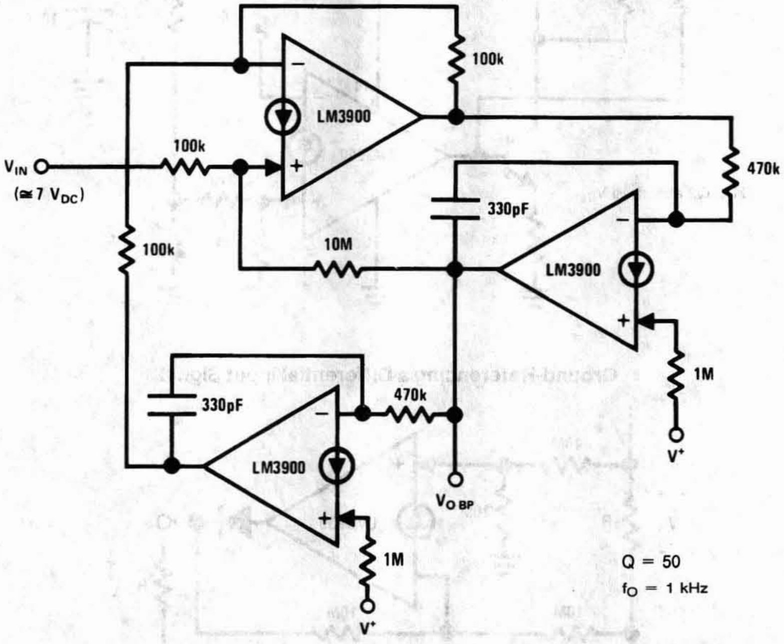
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Low-Drift Ramp and Hold Circuit


RAMP DOWN
RAMP UP
100k
100k
1 μF
LM3900
V_O
10M
2M
ZERO DRIFT ADJ
10M
LM3900
AUX

TL/H/7936–10

Bi-Quad Active Filter (2nd Degree State-Variable Network)

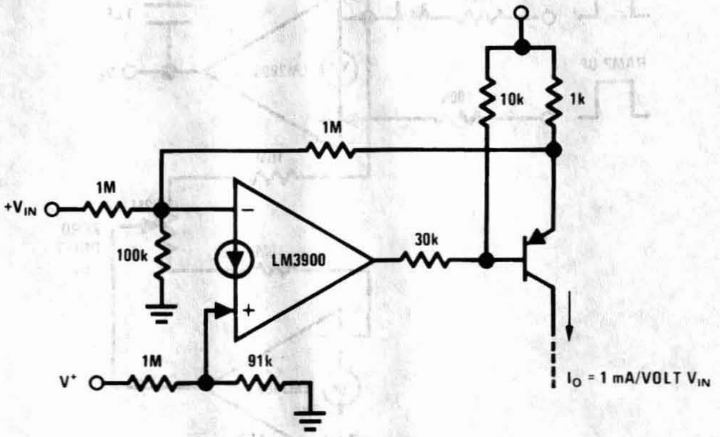

100k
LM3900
V_IN
(≅7 V_DC)
100k
470k
330pF
100k
10M
LM3900
1M
V+
330pF
470k
LM3900
V_O BP
1M
V+

Q = 50
$f_O = 1\ kHz$

TL/H/7936–11

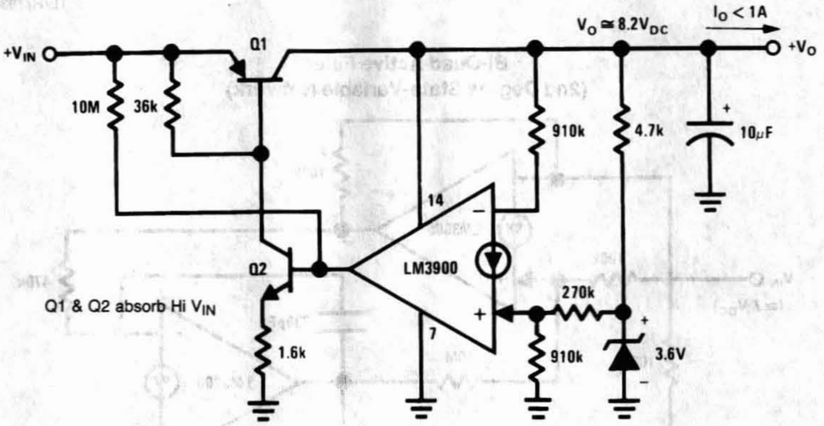
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Voltage-Controlled Current Source (Transconductance Amplifier)


V+
10k
1k
1M
1M
+VIN
100k
LM3900
30k
V+
1M
91k
IO = 1 mA/VOLT VIN

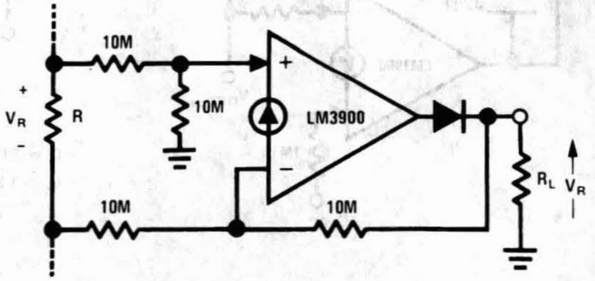
TL/H/7936–12

Hi V_{IN}, Lo ($V_{IN} - V_O$) Self-Regulator


VO ≅ 8.2VDC
IO < 1A
+VIN
+VO
Q1
10M
36k
910k
4.7k
10μF
14
Q2
LM3900
270k
Q1 & Q2 absorb Hi VIN
7
1.6k
910k
3.6V

TL/H/7936–13

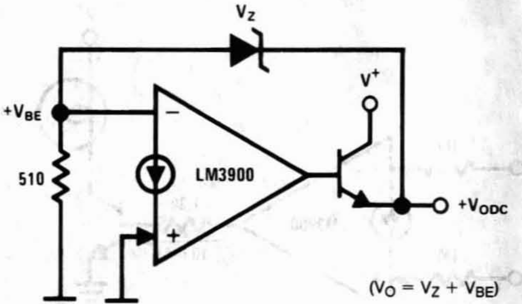
Ground-Referencing a Differential Input Signal


10M
10M
VR
R
LM3900
RL
VR
10M
10M

TL/H/7936–14

Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

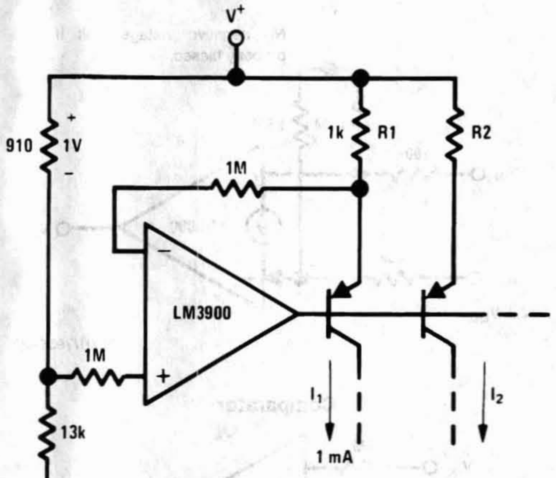
Voltage Regulator


V_Z
$+V_{BE}$
510
LM3900
V^+
$+V_{ODC}$

($V_O = V_Z + V_{BE}$)

TL/H/7936-15

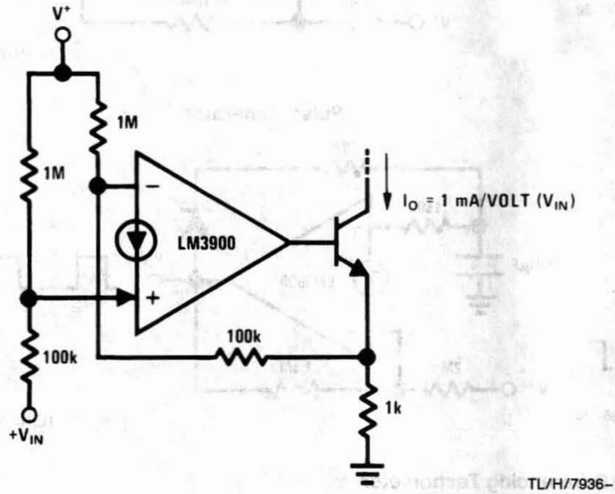
Fixed Current Sources


V^+
910
+
1V
−
1k
R1
R2
1M
LM3900
1M
13k
I_1
1 mA
I_2

$I_2 = \frac{R1}{R2} I_1$

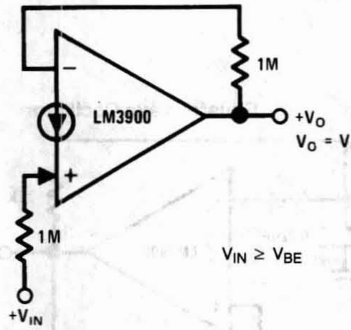
TL/H/7936-16

Voltage-Controlled Current Sink (Transconductance Amplifier)


V^+
1M
1M
LM3900
$I_O = 1\ mA/VOLT\ (V_{IN})$
100k
100k
1k
$+V_{IN}$

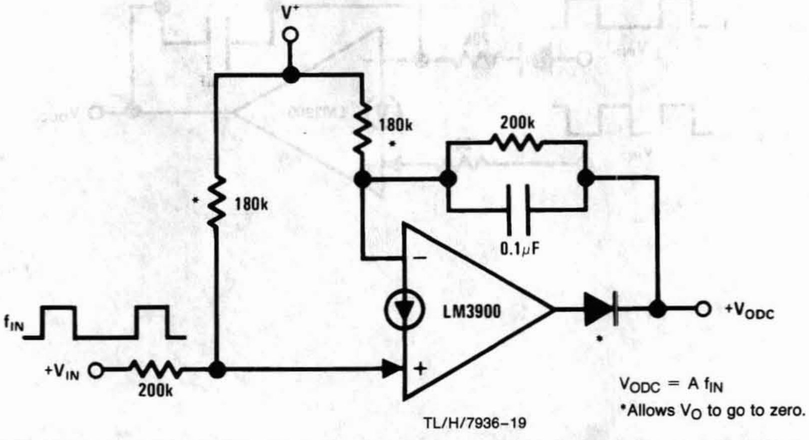
TL/H/7936-17

Buffer Amplifier


1M
LM3900
$+V_O$
$V_O = V_{IN}$
1M
$V_{IN} \geq V_{BE}$
$+V_{IN}$

TL/H/7936-18

Tachometer


V^+
180k
*
200k
*
180k
0.1 μF
LM3900
*
$+V_{ODC}$
f_{IN}
$+V_{IN}$
200k

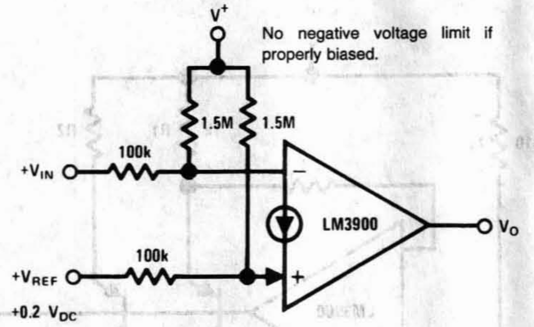
$V_{ODC} = A\ f_{IN}$

*Allows V_O to go to zero.

TL/H/7936-19

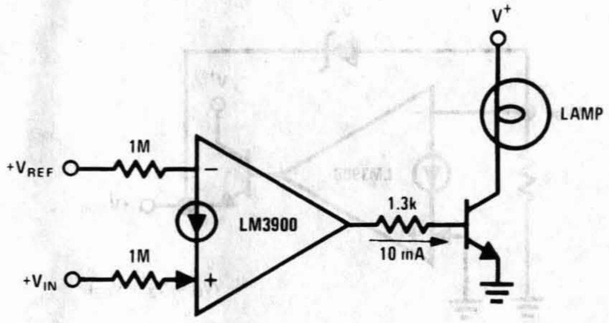
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Low-Voltage Comparator


V+
No negative voltage limit if properly biased.
1.5M
1.5M
100k
+VIN
LM3900
VO
100k
+VREF
+0.2 VDC

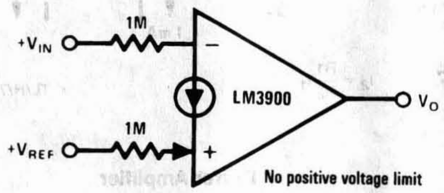
TL/H/7936-20

Power Comparator


V+
LAMP
1M
+VREF
LM3900
1.3k
10 mA
1M
+VIN

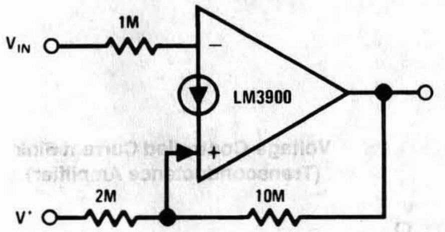
TL/H/7936-21

Comparator


1M
+VIN
LM3900
VO
1M
+VREF
No positive voltage limit

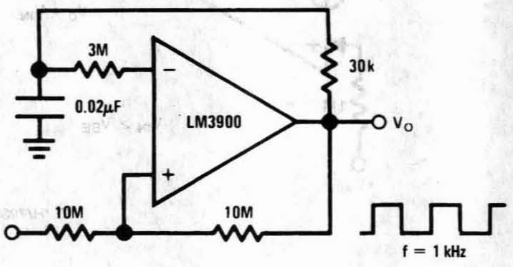
TL/H/7936-22

Schmitt-Trigger


1M
VIN
LM3900
VO
2M
V+
10M

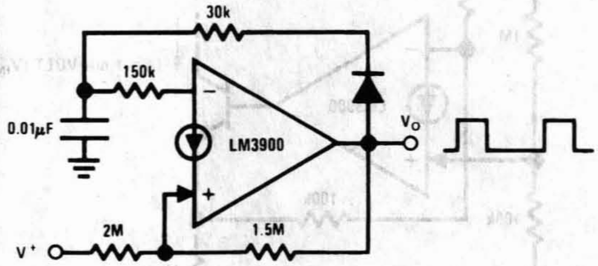
TL/H/7936-23

Square-Wave Oscillator


3M
30k
0.02μF
LM3900
VO
10M
V+
10M
f = 1 kHz

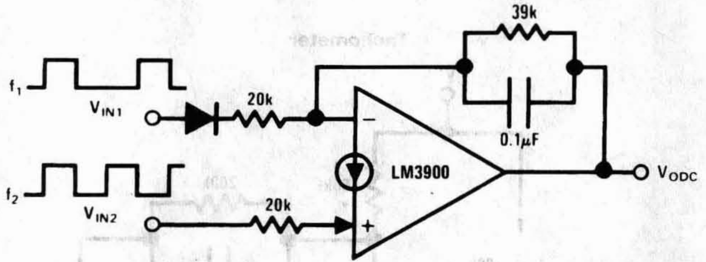
TL/H/7936-24

Pulse Generator


30k
150k
0.01μF
LM3900
VO
2M
V+
1.5M

TL/H/7936-25

Frequency Differencing Tachometer

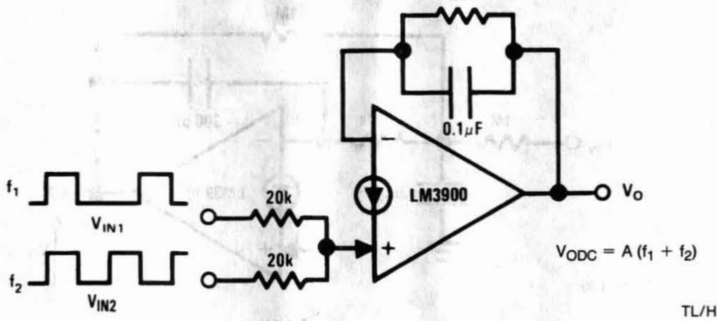

39k
f1
VIN1
20k
0.1μF
f2
LM3900
VODC
VIN2
20k

$V_{ODC} = A\,(f_1 - f_2)$

TL/H/7936-26

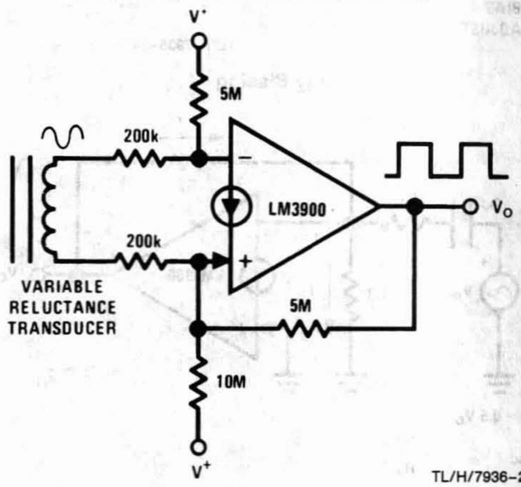
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Frequency Averaging Tachometer


39k
0.1µF
f1
VIN1
f2
VIN2
20k
20k
LM3900
VO
VODC = A (f1 + f2)

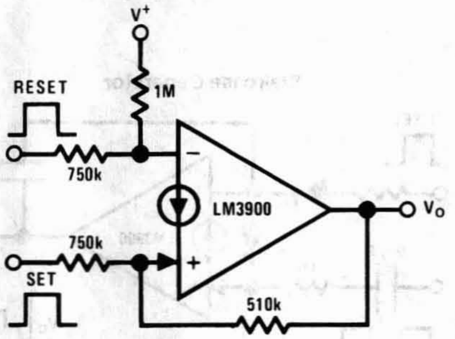
TL/H/7936-27

Squaring Amplifier (W/Hysteresis)


V+
5M
200k
200k
LM3900
VO
VARIABLE RELUCTANCE TRANSDUCER
5M
10M
V+

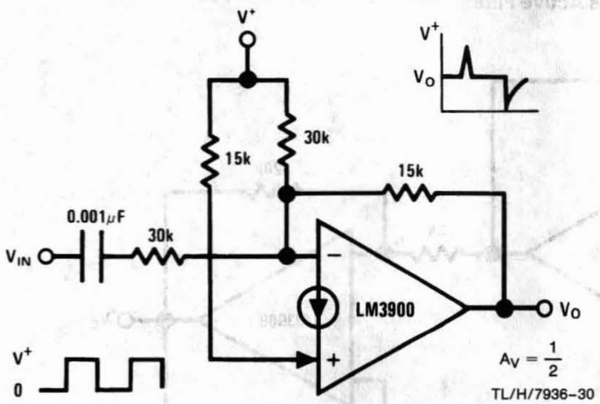
TL/H/7936-28

Bi-Stable Multivibrator


V+
RESET
1M
750k
750k
SET
LM3900
VO
510k

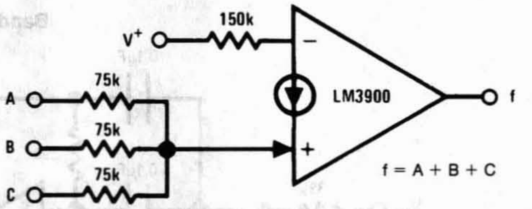
TL/H/7936-29

Differentiator (Common-Mode Biasing Keeps Input at $+V_{BE}$)


V+
V+
VO
15k
30k
15k
0.001µF
30k
VIN
LM3900
VO
V+
0
AV = 1/2

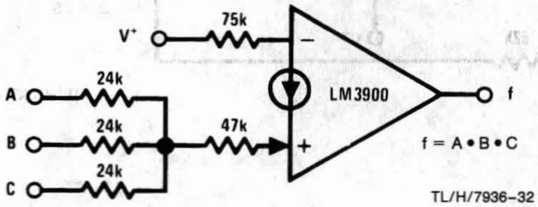
TL/H/7936-30

"OR" Gate


V+
150k
75k
75k
75k
A
B
C
LM3900
f
f = A + B + C

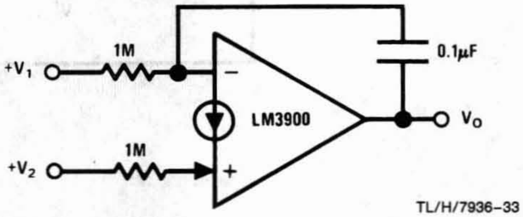
TL/H/7936-31

"AND" Gate


V+
75k
24k
24k
24k
47k
A
B
C
LM3900
f
f = A • B • C

TL/H/7936-32

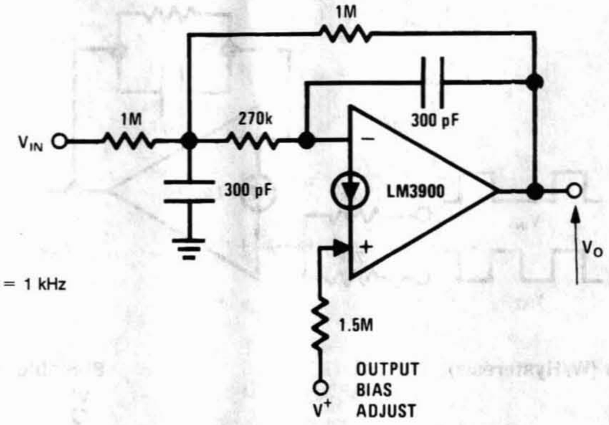
Difference Integrator


+V1
1M
0.1µF
LM3900
VO
+V2
1M

TL/H/7936-33

Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

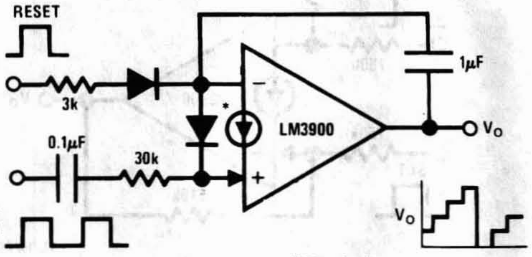
Low Pass Active Filter


1M
300 pF
1M
270k
V_{IN}
300 pF
LM3900
V_O
1.5M
V^+
OUTPUT
BIAS
ADJUST

$f_O = 1\ kHz$

TL/H/7936-34

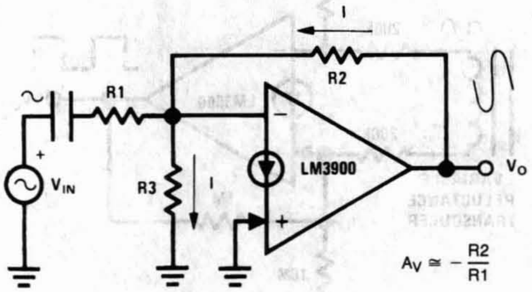
Staircase Generator


RESET
3k
0.1μF
30k
V^+_{IN}
1μF
LM3900
V_O
V_O

*2 Step/cycle

TL/H/7936-35

V_{BE} Biasing


I
R2
R1
V_{IN}
R3
I
LM3900
V_O

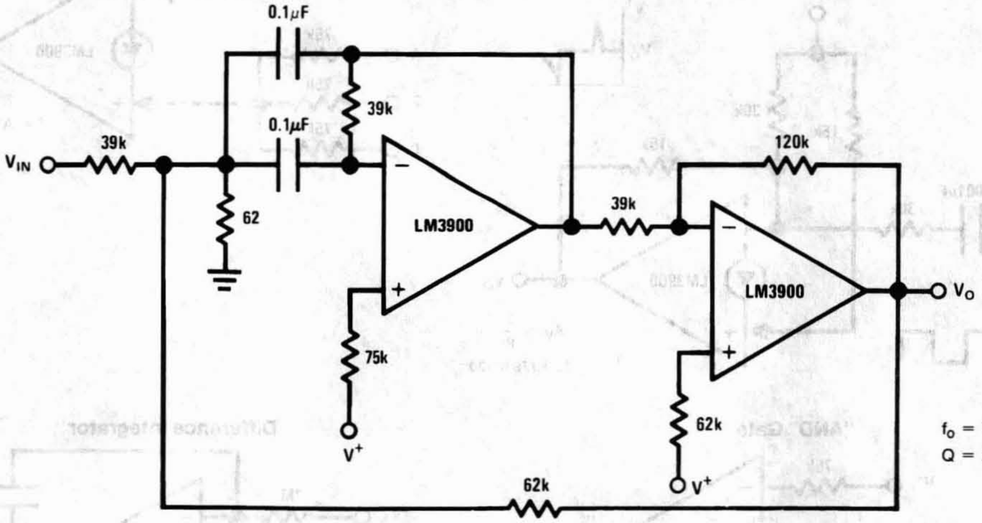
$A_V \cong -\frac{R2}{R1}$

$V_{BE} = 0.5\ V_{DC}$

$V_{ODC} = V_{BE}\left(1 + \frac{R2}{R3}\right)$

TL/H/7936-36

Bandpass Active Filter

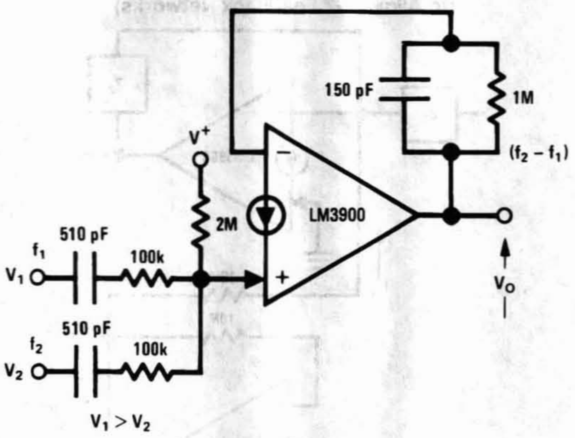

0.1μF
39k
0.1μF
V_{IN}
39k
62
LM3900
75k
V^+
39k
120k
LM3900
V_O
62k
V^+
62k

$f_o = 1\ kHz$
$Q = 25$

TL/H/7936-37

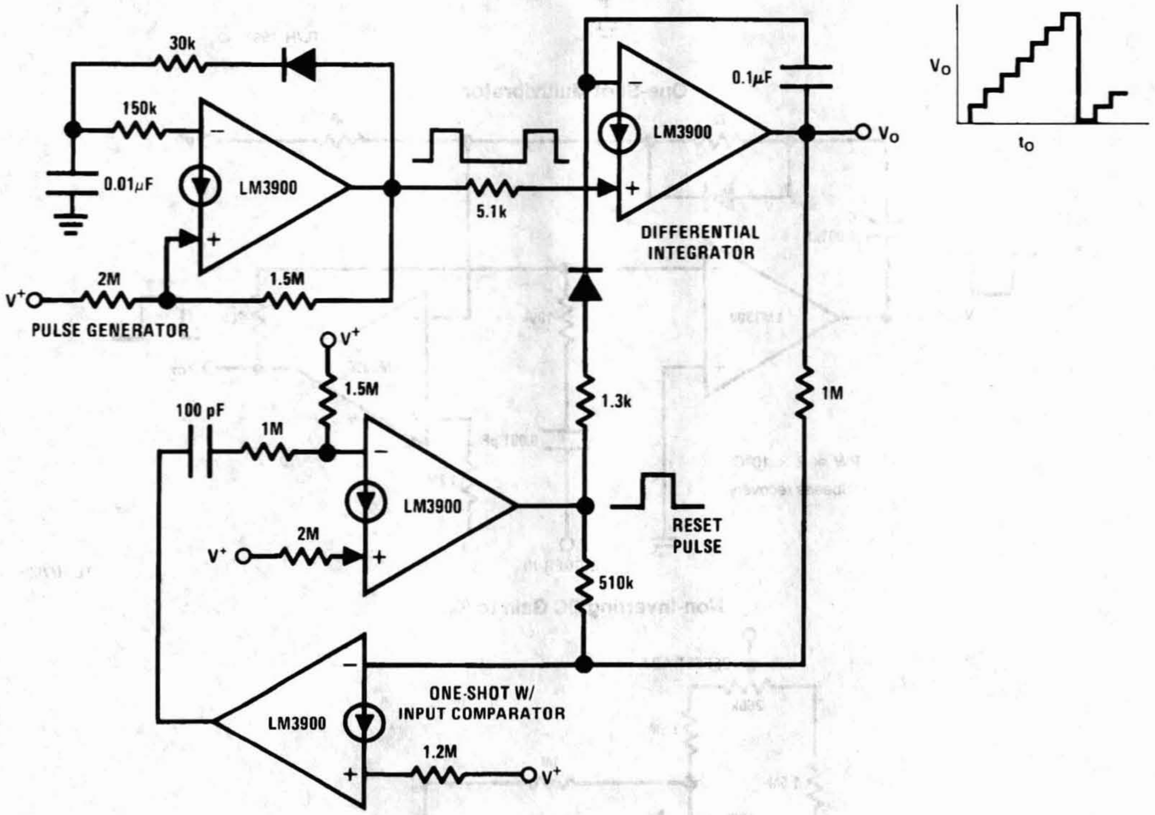
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Low-Frequency Mixer


150 pF
1M
$(f_2 - f_1)$
V^+
2M
LM3900
−
+
510 pF
f_1
V_1
100k
510 pF
f_2
V_2
100k
V_O
$V_1 > V_2$

TL/H/7936–38

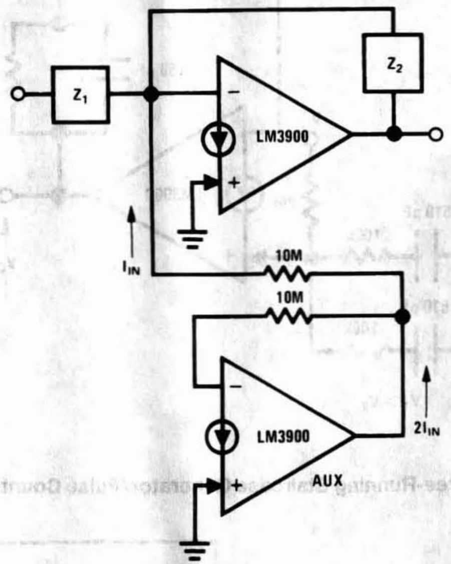
Free-Running Staircase Generator/Pulse Counter


30k
150k
0.01µF
LM3900
2M
1.5M
V^+
PULSE GENERATOR
5.1k
0.1µF
LM3900
V_O
DIFFERENTIAL INTEGRATOR
t_O
V^+
1.5M
100 pF
1M
LM3900
2M
V^+
1.3k
1M
RESET PULSE
510k
ONE-SHOT W/ INPUT COMPARATOR
LM3900
1.2M
V^+

TL/H/7936–39

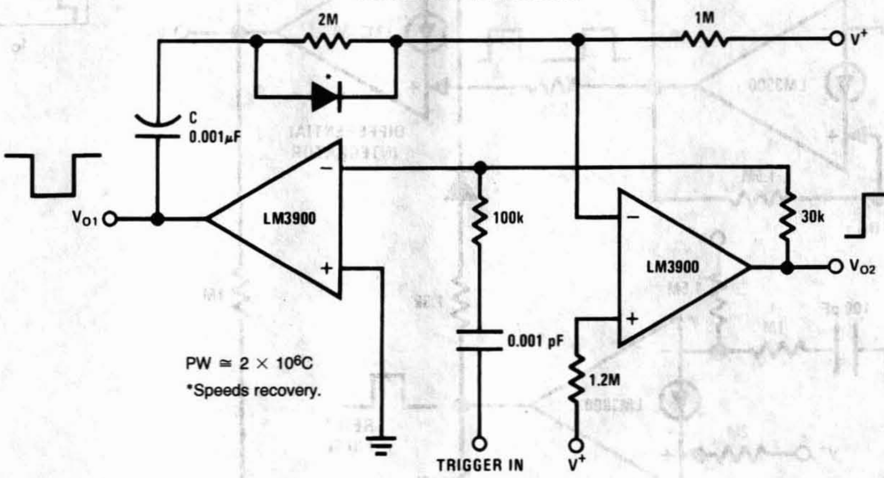
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Supplying I_{IN} with Aux. Amp (to Allow Hi-Z Feedback Networks)


Z1
Z2
LM3900
I_IN
10M
10M
LM3900
AUX
2I_IN

TL/H/7936-40

One-Shot Multivibrator

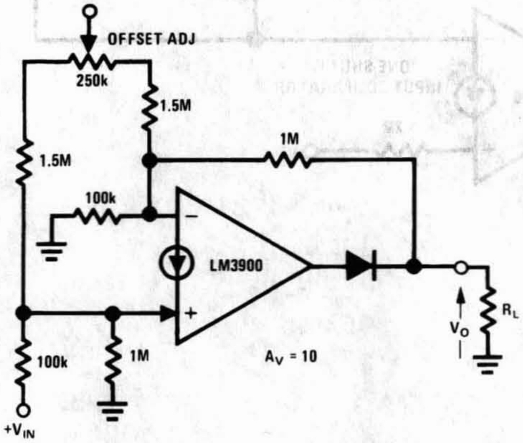

2M
1M
V+
C
0.001µF
V_O1
LM3900
100k
30k
LM3900
V_O2
0.001 pF
1.2M
TRIGGER IN
V+

PW ≅ 2 × 10^6C

*Speeds recovery.

TL/H/7936-41

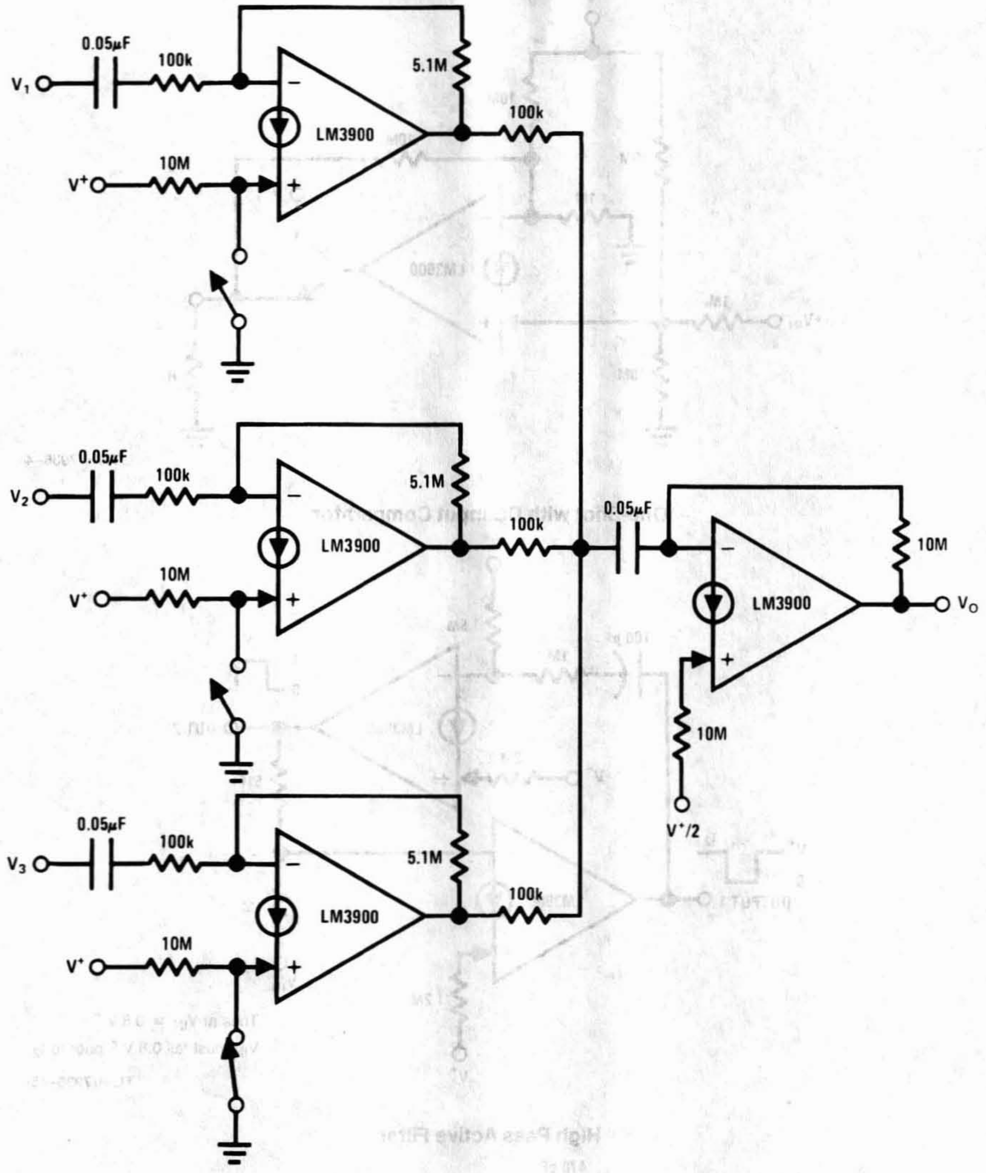
Non-Inverting DC Gain to (0,0)


OFFSET ADJ
250k
1.5M
1.5M
1M
100k
LM3900
100k
1M
A_V = 10
V_O
R_L
+V_IN

TL/H/7936-42

Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Channel Selection by DC Control (or Audio Mixer)

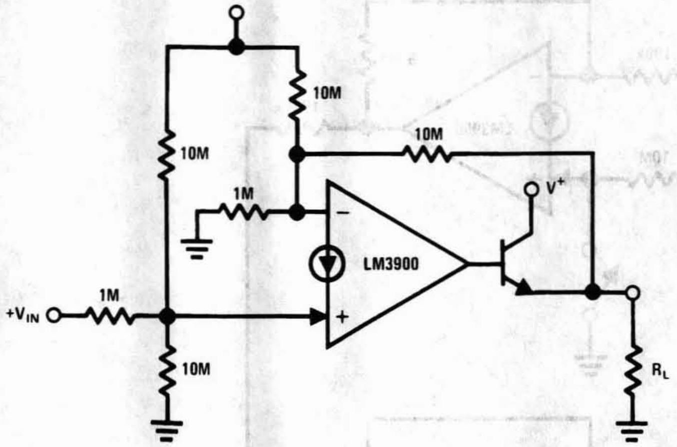


V₁
0.05µF
100k
5.1M
LM3900
100k
10M
V⁺
V₂
0.05µF
100k
5.1M
LM3900
100k
10M
V⁺
V₃
0.05µF
100k
5.1M
LM3900
100k
10M
V⁺
0.05µF
10M
LM3900
V_O
10M
V⁺/2

TL/H/7936–43

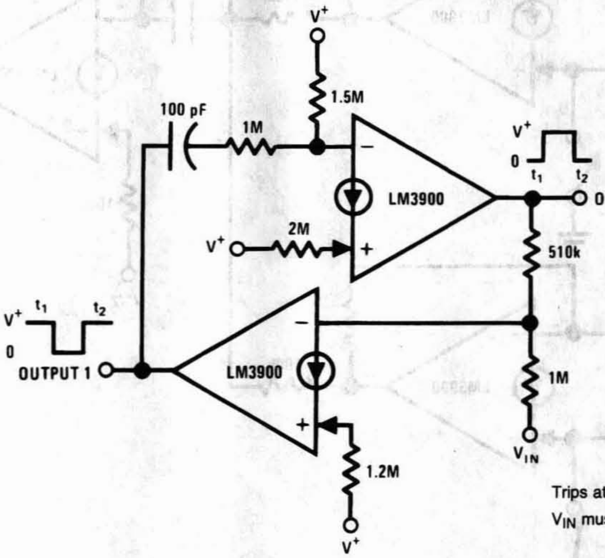
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Power Amplifier


V+
10M
10M
10M
1M
V+
LM3900
+VIN
1M
10M
RL
−
+

TL/H/7936–44

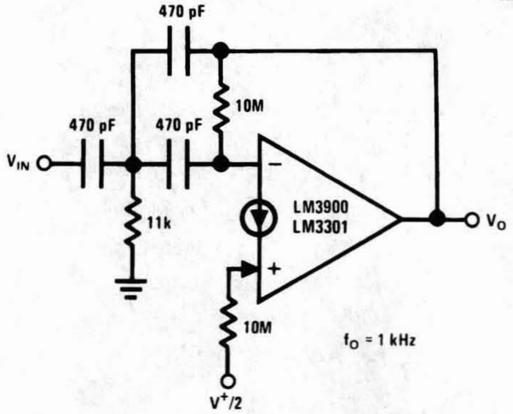
One-Shot with DC Input Comparator


V+
1.5M
100 pF
1M
V+
0
t1
t2
OUT 2
LM3900
V+
2M
510k
V+
t1
t2
0
OUTPUT 1
LM3900
1M
VIN
1.2M
V+

Trips at $V_{IN} \cong 0.8\ V^+$
V_{IN} must fall $0.8\ V^+$ prior to t_2

TL/H/7936–45

High Pass Active Filter

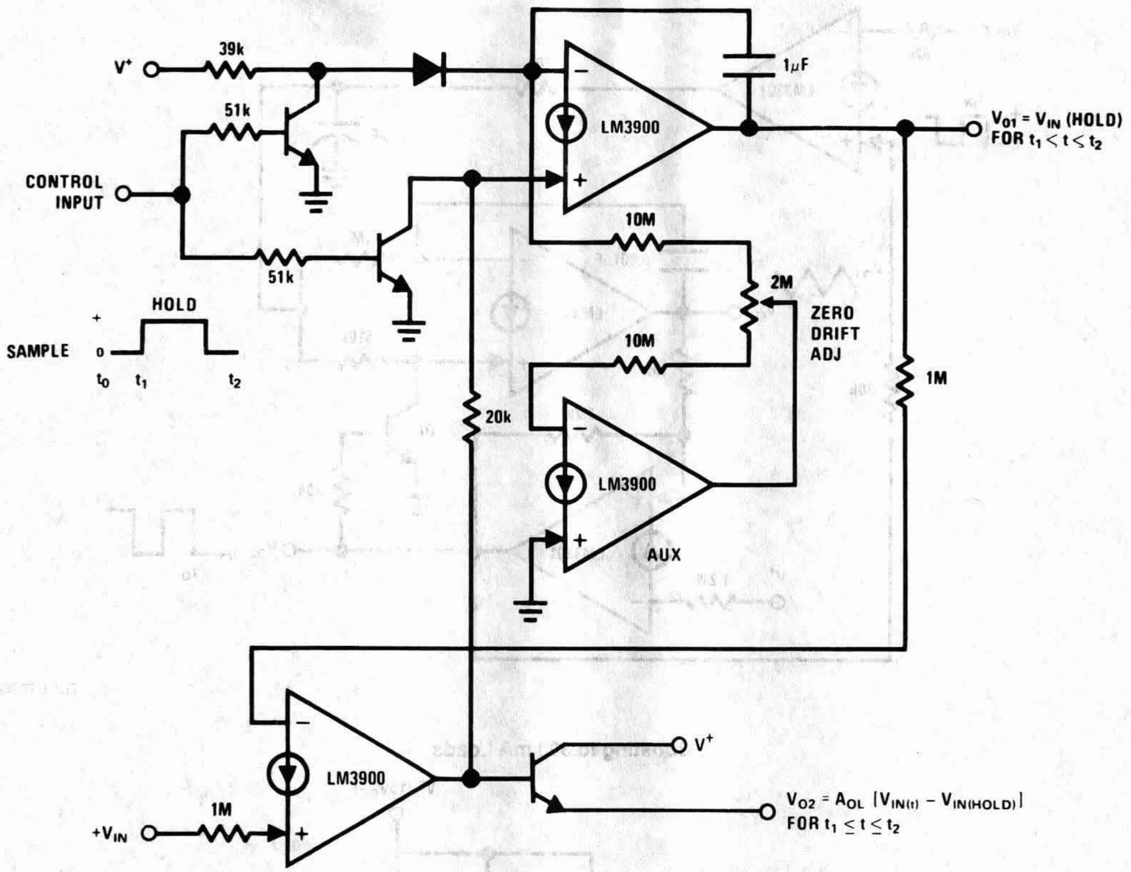

470 pF
10M
470 pF
470 pF
VIN
LM3900
LM3301
VO
11k
10M
V+/2

$f_O = 1\ kHz$

TL/H/7936–46

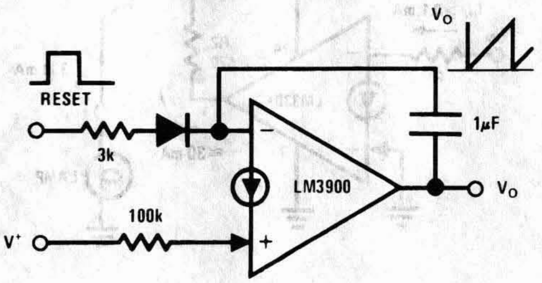
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Sample-Hold and Compare with New $+V_{IN}$


V+
39k
51k
CONTROL INPUT
51k
HOLD
+
SAMPLE
0
t0
t1
t2
LM3900
1µF
V01 = VIN (HOLD) FOR t1 < t < t2
10M
2M
ZERO DRIFT ADJ
10M
20k
1M
LM3900
AUX
LM3900
1M
+VIN
V+
V02 = AOL [VIN(t) − VIN(HOLD)] FOR t1 ≤ t ≤ t2

TL/H/7936–47

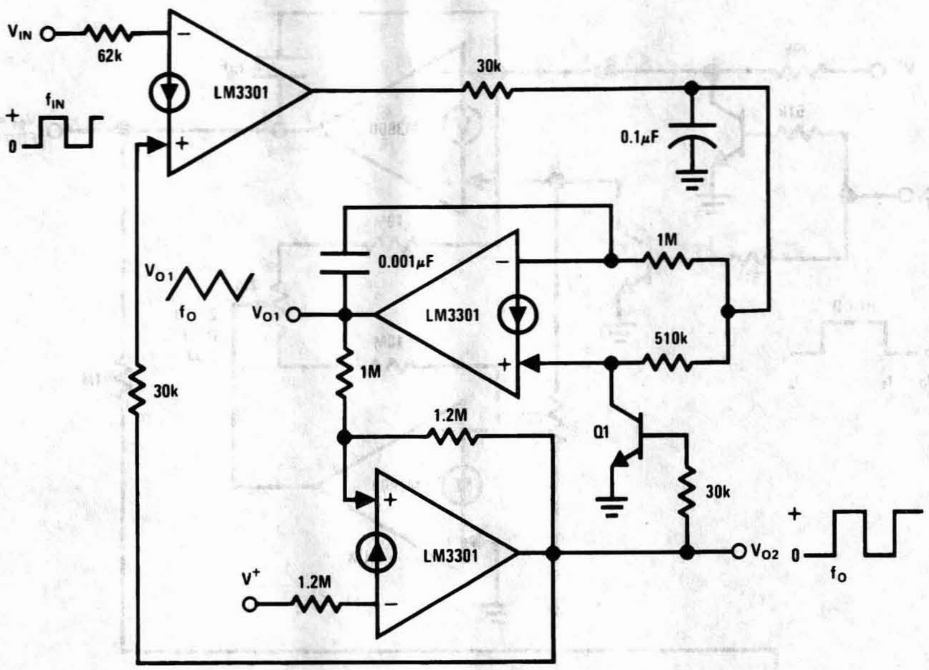
Sawtooth Generator


RESET
3k
V+
100k
LM3900
1µF
VO
VO

TL/H/7936–48

Typical Applications (V$^+$ = 15 V$_{DC}$) (Continued)

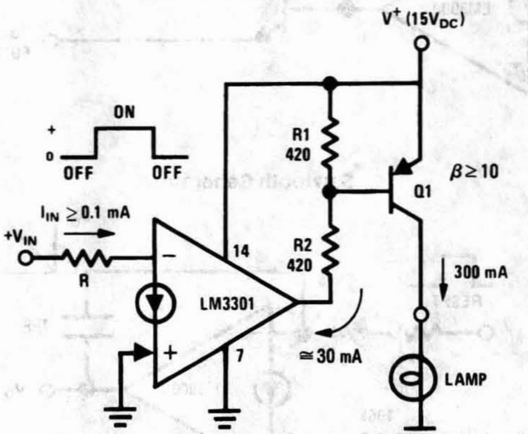
Phase-Locked Loop



V$_{IN}$
62k
LM3301
f$_{IN}$
+
0
30k
0.1μF
0.001μF
1M
V$_{O1}$
f$_O$
V$_{O1}$
LM3301
510k
30k
1M
1.2M
Q1
30k
+
LM3301
V$_{O2}$
0
f$_O$
V$^+$
1.2M

TL/H/7936-49

Boosting to 300 mA Loads

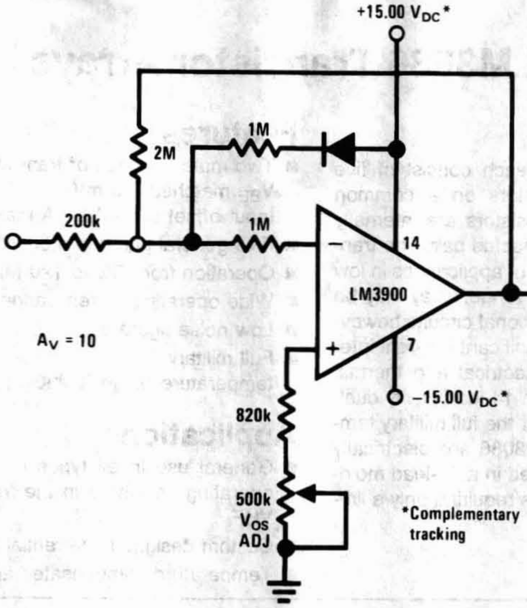


V$^+$ (15V$_{DC}$)
ON
+
0
OFF
OFF
R1
420
β≥10
Q1
I$_{IN}$ ≥ 0.1 mA
+V$_{IN}$
R
14
R2
420
LM3301
300 mA
7
≅30 mA
LAMP

TL/H/7936-50

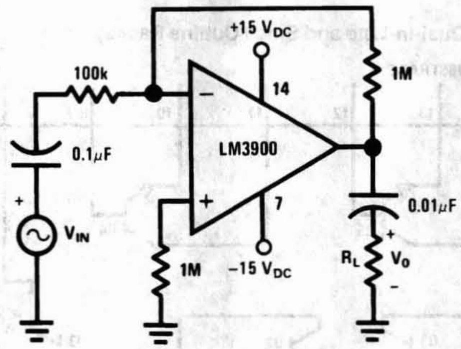
Split-Supply Applications ($V^+ = +15\ V_{DC}$ & $V^- = -15\ V_{DC}$)

Non-Inverting DC Gain


+15.00 V_DC*
2M
1M
200k
±V_IN
1M
14
LM3900
±V_O
A_V = 10
7
−15.00 V_DC*
820k
500k
V_OS
ADJ
*Complementary tracking

TL/H/7936-51

AC Amplifier


+15 V_DC
100k
14
1M
LM3900
0.1μF
+
V_IN
7
0.01μF
+
R_L
V_O
−
1M
−15 V_DC

TL/H/7936-52

National Semiconductor

LM3045/LM3046/LM3086 Transistor Arrays

General Description

The LM3045, LM3046 and LM3086 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3045 is supplied in a 14-lead cavity dual-in-line package rated for operation over the full military temperature range. The LM3046 and LM3086 are electrically identical to the LM3045 but are supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

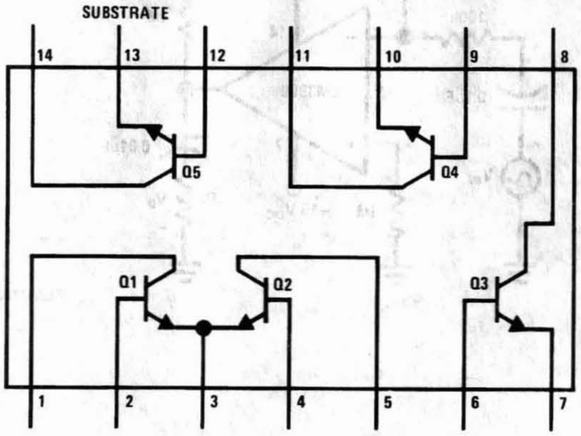
- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 μA max at $I_C = 1$ mA
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz
- Full military temperature range (LM3045) −55°C to +125°C

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Schematic and Connection Diagram

Dual-In-Line and Small Outline Packages



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Top View

Order Number LM3045J, LM3046M, LM3046N or LM3086N
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings (T_A = 25°C)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM3045		LM3046/LM3086		
	Each Transistor	**Total Package**	**Each Transistor**	**Total Package**	**Units**
Power Dissipation:					
T_A = 25°C	300	750	300	750	mW
T_A = 25°C to 55°C			300	750	mW
T_A > 55°C			Derate at 6.67		mW/°C
T_A = 25°C to 75°C	300	750			mW
T_A > 75°C	Derate at 8				mW/°C
Collector to Emitter Voltage, V_{CEO}	15		15		V
Collector to Base Voltage, V_{CBO}	20		20		V
Collector to Substrate Voltage, V_{CIO} (Note 1)	20		20		V
Emitter to Base Voltage, V_{EBO}	5		5		V
Collector Current, I_C	50		50		mA
Operating Temperature Range	−55°C to +125°C		−40°C to +85°C		
Storage Temperature Range	−65°C to +150°C		−65°C to +85°C		
Soldering Information					
Dual-In-Line Package Soldering (10 Sec.)	260°C		260°C		
Small Outline Package					
Vapor Phase (60 Seconds)			215°C		
Infrared (15 Seconds)			220°C		

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Parameter	Conditions		Limits LM3045, LM3046			Limits LM3086		Units
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	

Parameter	Conditions	LM3045, LM3046 Min	LM3045, LM3046 Typ	LM3045, LM3046 Max	LM3086 Min	LM3086 Typ	LM3086 Max	Units
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	$I_C = 10\ \mu A, I_E = 0$	20	60		20	60		V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	$I_C = 1\ mA, I_B = 0$	15	24		15	24		V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	$I_C = 10\ \mu A, I_{CI} = 0$	20	60		20	60		V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$)	$I_E\ 10\ \mu A, I_C = 0$	5	7		5	7		V
Collector Cutoff Current (I_{CBO})	$V_{CB} = 10V, I_E = 0$		0.002	40		0.002	100	nA
Collector Cutoff Current (I_{CEO})	$V_{CE} = 10V, I_B = 0$			0.5			5	μA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	$V_{CE} = 3V$, $I_C = 10\ mA$		100			100		
	$I_C = 1\ mA$	40	100		40	100		
	$I_C = 10\ \mu A$		54			54		
Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{O1} - I_{O2}\rvert$	$V_{CE} = 3V, I_C = 1\ mA$		0.3	2				μA
Base to Emitter Voltage (V_{BE})	$V_{CE} = 3V$, $I_E = 1\ mA$		0.715			0.715		V
	$I_E = 10\ mA$		0.800			0.800		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2}\rvert$	$V_{CE} = 3V, I_C = 1\ mA$		0.45	5				mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE3} - V_{BE4}\rvert, \lvert V_{BE4} - V_{BE5}\rvert, \lvert V_{BE5} - V_{BE3}\rvert$	$V_{CE} = 3V, I_C = 1\ mA$		0.45	5				mV
Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$	$V_{CE} = 3V, I_C = 1\ mA$		−1.9			−1.9		mV/°C
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	$I_B = 1\ mA, I_C = 10\ mA$		0.23			0.23		V
Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{10}}{\Delta T}\right)$	$V_{CE} = 3V, I_C = 1\ mA$		1.1					μV/°C

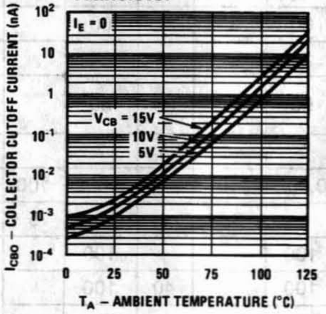
Note 1: The collector of each transistor of the LM3045, LM3046, and LM3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Electrical Characteristics (Continued)

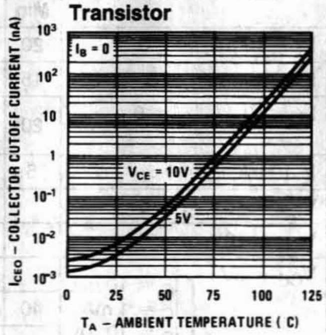
Parameter	Conditions	Min	Typ	Max	Units
Low Frequency Noise Figure (NF)	f = 1 kHz, V_{CE} = 3V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRCUIT CHARACTERISTICS					
Forward Current Transfer Ratio (h_{fe})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		110 (LM3045, LM3046) (LM3086)		
Short Circuit Input Impednace (h_{ie})			3.5		kΩ
Open Circuit Output Impedance (h_{oe})			15.6		μmho
Open Circuit Reverse Voltage Transfer Ratio (h_{re})			1.8×10^{-4}		
ADMITTANCE CHARACTERISTICS					
Forward Transfer Admittance (Y_{fe})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		
Input Admittance (Y_{ie})			0.3+J 0.04		
Output Admittance (Y_{oe})			0.001+j 0.03		
Reverse Transfer Admittance (Y_{re})			See Curve		
Gain Bandwidth Product (f_T)	V_{CE} = 3V, I_C = 3 mA	300	550		
Emitter to Base Capacitance (C_{EB})	V_{EB} = 3V, I_E = 0		0.6		pF
Collector to Base Capacitance (C_{CB})	V_{CB} = 3V, I_C = 0		0.58		pF
Collector to Substrate Capacitance (C_{CI})	V_{CS} = 3V, I_C = 0		2.8		pF

Typical Performance Characteristics

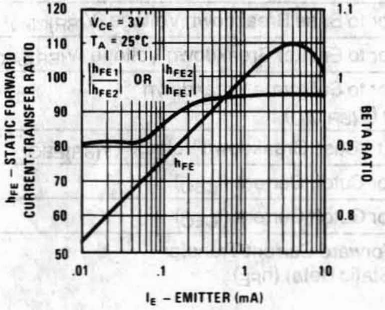
Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor



Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor



Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current



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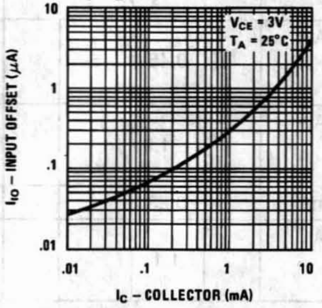
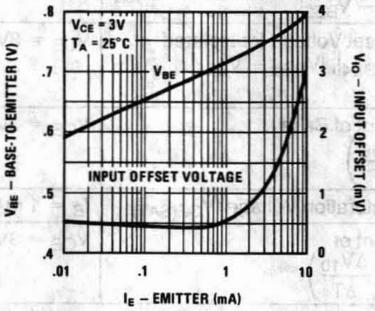
Typical Input Offset Current for Matched Transistor Pair Q_1 Q_2 vs Collector Current



Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current



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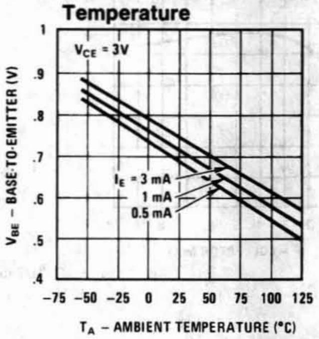
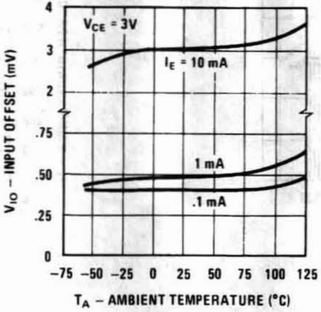
Typical Performance Characteristics (Continued)

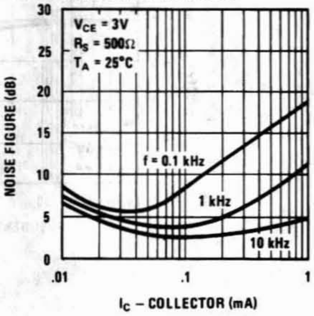
Typical Base To Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature



Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature

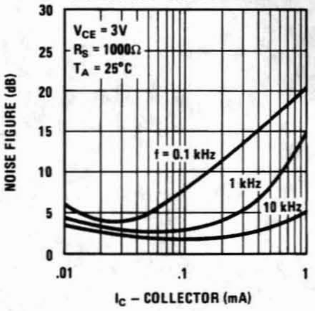


Typical Noise Figure vs Collector Current

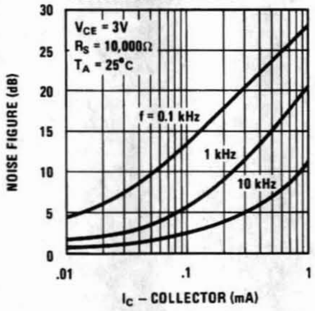


TL/H/7950–4

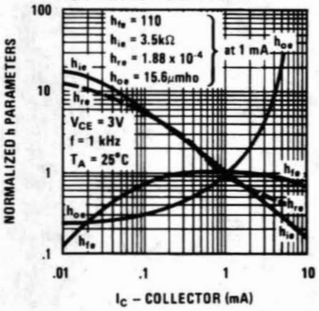
Typical Noise Figure vs Collector Current



Typical Noise Figure vs Collector Current



Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current



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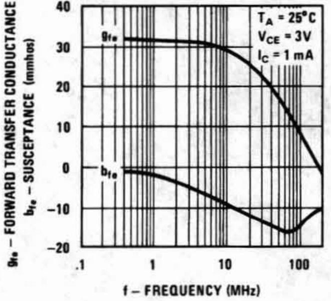
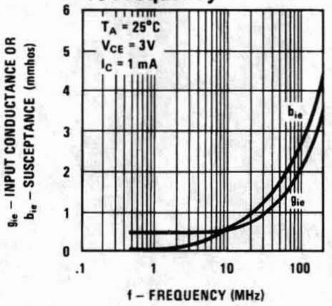
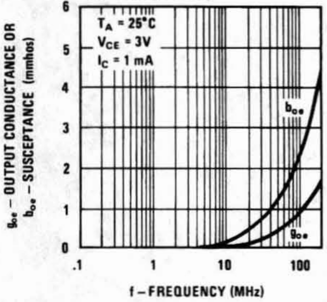
Typical Forward Transfer Admittance vs Frequency



Typical Input Admittance vs Frequency



Typical Output Admittance vs Frequency



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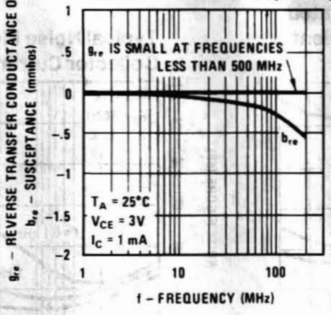
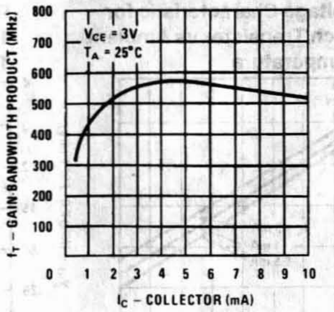
Typical Performance Characteristics (Continued)

Typical Reverse Transfer Admittance vs Frequency



Typical Gain-Bandwidth Product vs Collector Current



TL/H/7950–7

National Semiconductor

LM3080
Operational Transconductance Amplifier

General Description

The LM3080 is a programmable transconductance block intended to fulfill a wide variety of variable gain applications. The LM3080 has differential inputs and high impedance push-pull outputs. The device has high input impedance and its transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

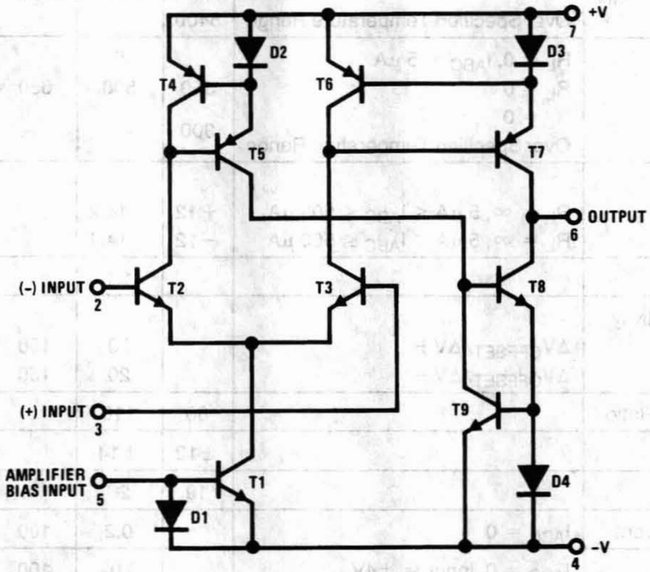
High slew rate together with programmable gain make the LM3080 an ideal choice for variable gain applications such as sample and hold, multiplexing, filtering, and multiplying.

The LM3080N and LM3080AN are guaranteed from 0°C to +70°C.

Features

- Slew rate (unity gain compensated): 50 V/µs
- Fully adjustable gain: 0 to $g_m \bullet R_L$ limit
- Extended g_m linearity: 3 decades
- Flexible supply voltage range: ±2V to ±18V
- Adjustable power consumption

Schematic and Connection Diagrams


+V
7
D2
D3
T4
T6
T5
T7
OUTPUT
6
(-) INPUT
2
T2
T3
T8
(+) INPUT
3
T9
AMPLIFIER
BIAS INPUT
5
T1
D4
D1
-V
4

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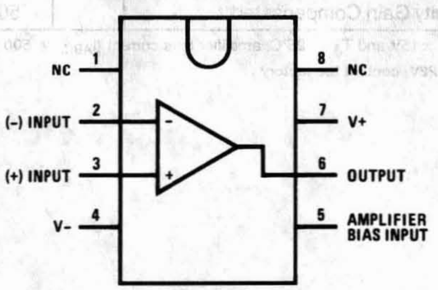
Dual-In-Line Package


NC
1
(-) INPUT
2
(+) INPUT
3
V-
4
8
NC
7
V+
6
OUTPUT
5
AMPLIFIER
BIAS INPUT
-
+

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Top View

Order Number LM3080AN, LM3080M or LM3080N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	
LM3080	±18V
LM3080A	±22V
Power Dissipation	250 mW
Differential Input Voltage	±5V
Amplifier Bias Current (I_{ABC})	2 mA
DC Input Voltage	$+V_S$ to $-V_S$
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LM3080N or LM3080AN	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Note 1)

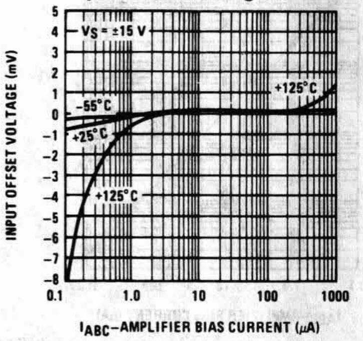
Parameter	Conditions	LM3080			LM3080A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			0.4	5		0.4	2	mV
	Over Specified Temperature Range			6			5	mV
	I_{ABC} = 5 μA		0.3			0.3	2	mV
Input Offset Voltage Change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1			0.1	3	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current			0.4	5		0.4	5	μA
	Over Specified Temperature Range		1	7		1	8	μA
Forward Transconductance (g_m)		6700	9600	13000	7700	9600	12000	μmho
	Over Specified Temperature Range	5400			4000			μmho
Peak Output Current	R_L = 0, I_{ABC} = 5 μA		5		3	5	7	μA
	R_L = 0	350	500	650	350	500	650	μA
	R_L = 0 Over Specified Temperature Range	300			300			μA
Peak Output Voltage								
Positive	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+12	+14.2		+12	+14.2		V
Negative	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	−12	−14.4		−12	−14.4		V
Amplifier Supply Current			1.1			1.1		mA
Input Offset Voltage Sensitivity								
Positive	$\Delta V_{OFFSET}/\Delta V+$		20	150		20	150	μV/V
Negative	$\Delta V_{OFFSET}/\Delta V-$		20	150		20	150	μV/V
Common Mode Rejection Ratio		80	110		80	110		dB
Common Mode Range		±12	±14		±12	±14		V
Input Resistance		10	26		10	26		kΩ
Magnitude of Leakage Current	I_{ABC} = 0		0.2	100		0.2	5	nA
Differential Input Current	I_{ABC} = 0, Input = ±4V		0.02	100		0.02	5	nA
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μs

Note 1: These specifications apply for V_S = ±15V and T_A = 25°C, amplifier bias current (I_{ABC}) = 500 μA, unless otherwise specified.

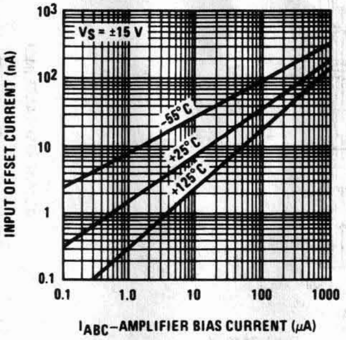
Note 2: Selection to supply voltage above ±22V, contact the factory.

Typical Performance Characteristics

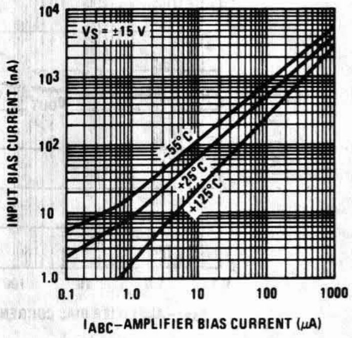
Input Offset Voltage



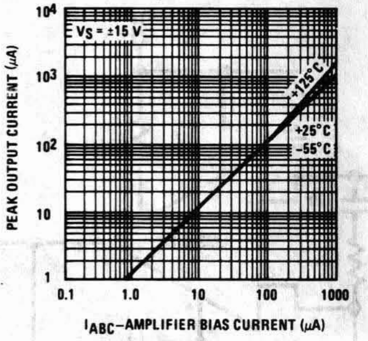
Input Offset Current



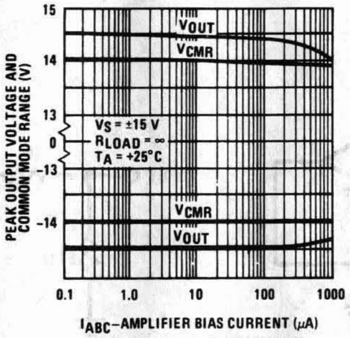
Input Bias Current



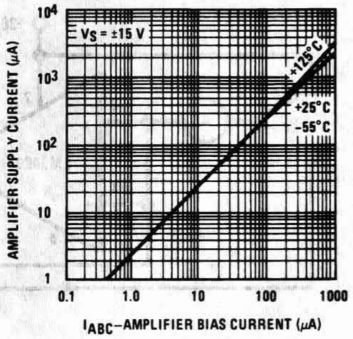
Peak Output Current



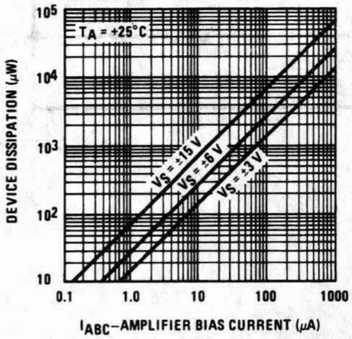
Peak Output Voltage and Common Mode Range



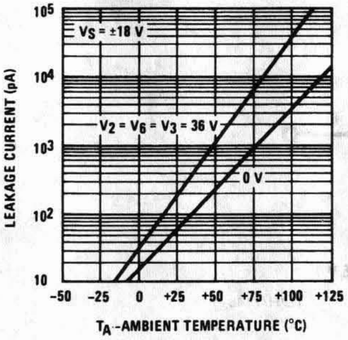
Amplifier Supply Current



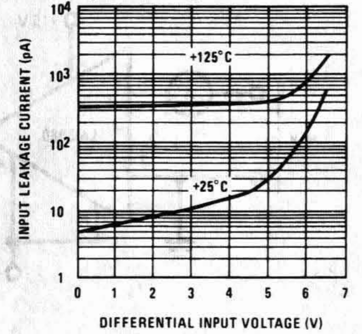
Total Power Dissipation



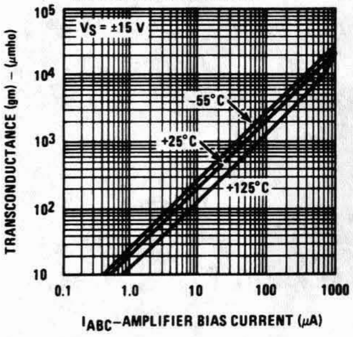
Leakage Current



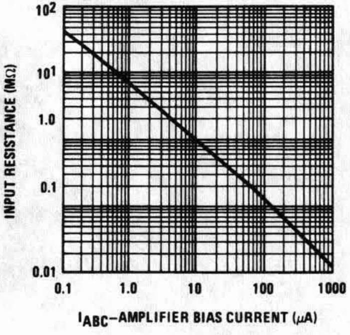
Input Leakage



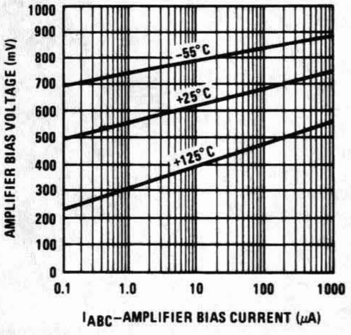
Transconductance



Input Resistance



Amplifier Bias Voltage vs Amplifier Bias Current



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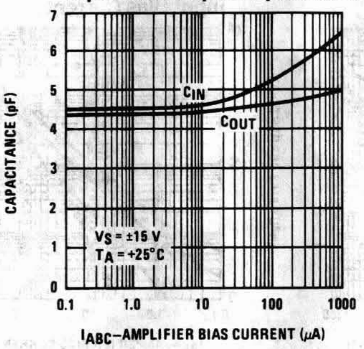
Typical Performance Characteristics (Continued)

Input and Output Capacitance



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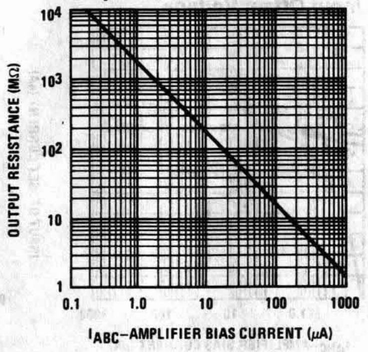
Output Resistance



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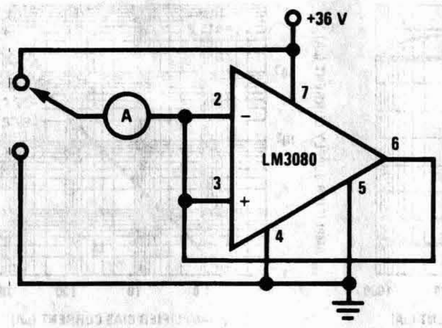
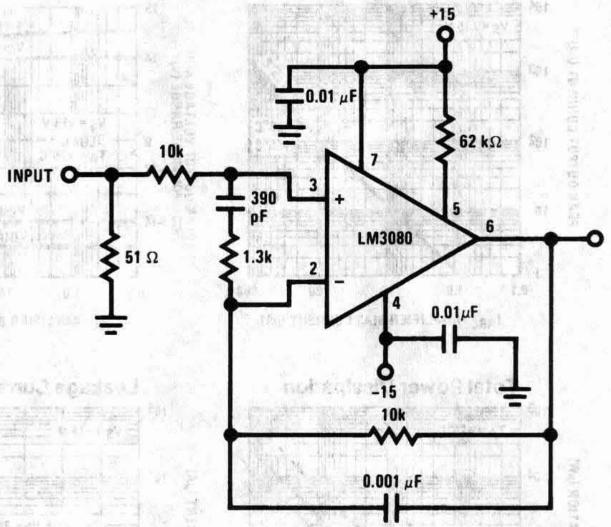
Leakage Current Test Circuit


+36 V
A
2
3
7
6
5
4
−
+
LM3080

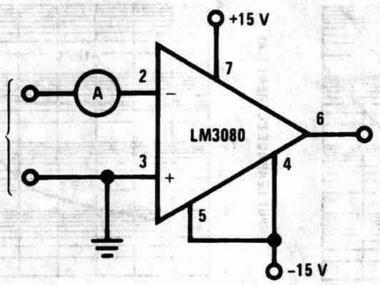
TL/H/7148–6

Unity Gain Follower


+15
0.01 μF
62 kΩ
INPUT
10k
390 pF
51 Ω
1.3k
3
2
7
5
6
4
+
−
LM3080
0.01μF
−15
10k
0.001 μF

TL/H/7148–8

Differential Input Current Test Circuit


+15 V
A
±4 V
2
3
7
6
4
5
−
+
LM3080
−15 V

TL/H/7148–7

National Semiconductor

LM3303/LM3403
Quad Operational Amplifiers

General Description

The LM3303 and LM3403 are monolithic quad operational amplifiers consisting of four independent high gain, internally frequency compensated, operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications.

Features

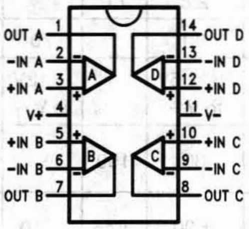
- Input common mode voltage range includes ground or negative supply
- Output voltage can swing to ground or negative supply
- Four internally compensated operational amplifiers in a single package
- Wide power supply range single supply of 3.0V to 36V dual supply of ±1.5V to ±18V
- Class AB output stage for minimal crossover distortion
- Short circuit protected outputs
- High open loop gain 200k
- LM741 operational amplifier type performance

Applications

- Filters
- Voltage controlled oscillators

Connection Diagram

14-Lead DIP and SO-14 Package


OUT A 1
−IN A 2
+IN A 3
V+ 4
+IN B 5
−IN B 6
OUT B 7
A
B
C
D
14 OUT D
13 −IN D
12 +IN D
11 V−
10 +IN C
9 −IN C
8 OUT C

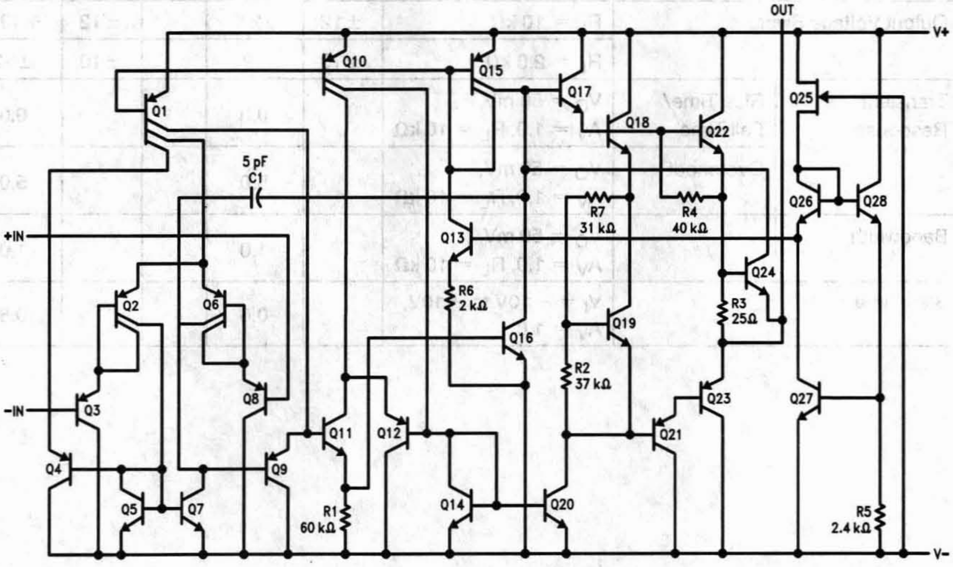
TL/H/10064–1

Top View

Order Information

Device Code	Package Code	Package Description
LM3303J	J14A	Ceramic DIP
LM3303N	N14A	Molded DIP
LM3303M	M14A	Molded Surface Mount
LM3403J	J14A	Ceramic DIP
LM3403N	N14A	Molded DIP
LM3403M	M14A	Molded Surface Mount

Equivalent Circuit (¼ of Circuit)


OUT
V+
V−
+IN
−IN
5 pF
C1
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
R1 60 kΩ
R2 37 kΩ
R3 25Ω
R4 40 kΩ
R5 2.4 kΩ
R6 2 kΩ
R7 31 kΩ

TL/H/10064–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Operating Temperature Range	
Industrial (LM3303)	−40°C to +85°C
Commercial (LM3403)	0°C to +70°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP and SO-14 (Soldering, 10 sec.)	265°C
Internal Power Dissipation (Notes 1, 2)	
14L-Ceramic DIP	1.36W
14L-Molded DIP	1.04W
SO-14	0.93W
Supply Voltage between V+ and V−	36V
Differential Input Voltage (Note 3)	±30V
Input Voltage	(V−) − 0.3V to V+
ESD Tolerance	(To Be Determined)

LM3303 and LM3403 Electrical Characteristics

T_A = 25°C, V_{CC} = ±15V, unless otherwise specified

Symbol	Parameter	Conditions	LM3303			LM3403			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage			2.0	8.0		2.0	8.0	mV
I_{IO}	Input Offset Current			30	75		30	50	nA
I_{IB}	Input Bias Current			200	500		200	500	nA
Z_I	Input Impedance		0.3	1.0		0.3	1.0		MΩ
I_{CC}	Supply Current	V_O = 0V, R_L = ∞		2.8	7.0		2.8	7.0	mA
CMR	Common Mode Rejection	R_S ≤ 10 kΩ	70	90		70	90		dB
V_{IR}	Input Voltage Range		+12V to V−	+12.5V to V−		+13V to V−	+13.5V to V−		V
PSRR	Power Supply Rejection Ratio			30	150		30	150	μV/V
I_{OS}	Output Short Circuit Current (Per Amplifier) (Note 4)		±10	±30	±45	±10	±30	±45	mA
A_{VS}	Large Signal Voltage Gain	V_O = ±10V, R_L ≥ 2.0 kΩ	20	200		20	200		V/mV
V_{OP}	Output Voltage Swing	R_L = 10 kΩ	±12	12.5		±12	+13.5		V
		R_L = 2.0 kΩ	±10	12		±10	±13		
TR	Transient Response Rise Time/Fall Time	V_O = 50 mV, A_V = 1.0, R_L = 10 kΩ		0.3			0.3		μs
	Overshoot	V_O = 50 mV, A_V = 1.0, R_L = 10 kΩ		5.0			5.0		%
BW	Bandwidth	V_O = 50 mV, A_V = 1.0, R_L = 10 kΩ		1.0			1.0		MHz
SR	Slew Rate	V_I = −10V to +10V, A_V = 1.0		0.6			0.6		V/μs

LM3303 and LM3403 (Continued)

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

The following specifications apply for $-40°C \leq T_A \leq +85°C$ for the LM3303, and $0°C \leq T_A \leq +70°C$ for the LM3403

Symbol	Parameter	Conditions	LM3303			LM3403			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage				10			10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			10			10		µV/°C
I_{IO}	Input Offset Current				250			200	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			50			50		pA/°C
I_{IB}	Input Bias Current				1000			800	nA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L \geq 2.0 k\Omega$	15			15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0 k\Omega$	±10			±10			V

LM3303 and LM3403
Electrical Characteristics $T_A = 25°C$, $V+ = 5.0V$, $V- = GND$, unless otherwise specified

Symbol	Parameter	Conditions	LM3303			LM3403			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage				8.0		2.0	8.0	mV
I_{IO}	Input Offset Current				75		30	50	nA
I_{IB}	Input Bias Current				500		200	500	nA
I_{CC}	Supply Current			2.5	7.0		2.5	7.0	mA
PSRR	Power Supply Rejection Ratio				150			150	µV/V
A_{VS}	Large Signal Voltage Gain	$R_L \geq 2.0 k\Omega$	20	200		20	200		V/mV
V_{OP}	Output Voltage Swing (Note 5)	$R_L = 10 k\Omega$	3.3			3.3			V
		$5.0V \leq V+ \leq 30V$, $R_L = 10 k\Omega$	(V+) −2.0			(V+) −2.0			
CS	Channel Separation	$1.0 Hz \leq f \leq 20 kHz$ (Input Referenced)		−120			−120		dB

Note 1: $T_{J\,Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

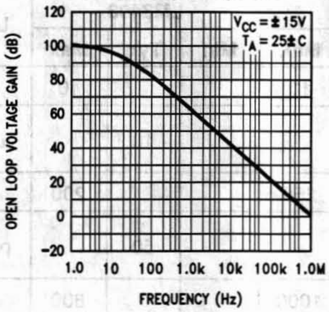
Note 3: For supply voltage less than 30V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.

Note 4: Not to exceed maximum package power dissipation.

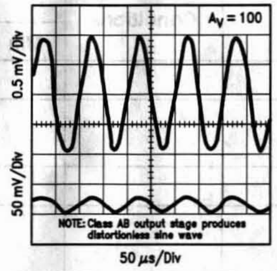
Note 5: Output will swing to ground.

Typical Performance Characteristics

Open Loop Frequency Response

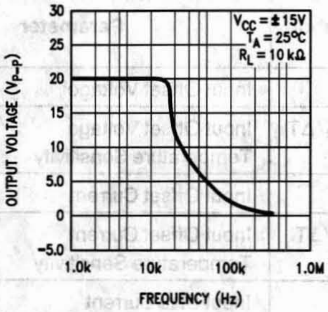


Sine Wave Response

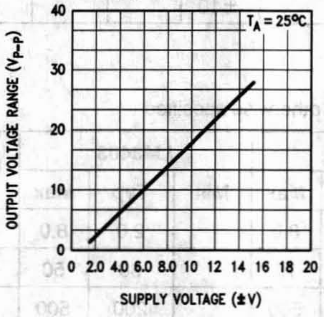


NOTE: Class AB output stage produces distortionless sine wave

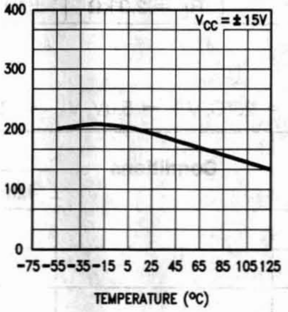
Output Voltage vs Frequency



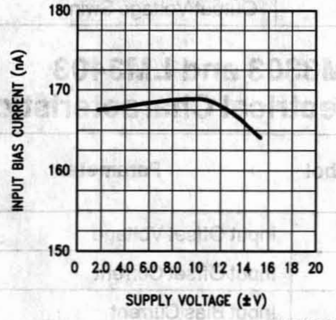
Output Swing vs Supply Voltage



Input Bias Current vs Temperature



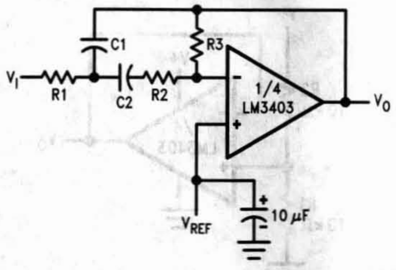
Input Bias Current vs Supply Voltage



TL/H/10064–3

Typical Applications

Multiple Feedback Bandpass Filter


C1
R3
V_I
R1
C2
R2
1/4
LM3403
V_O
V_{REF}
10 µF

TL/H/10064-4

f_o = center frequency
BW = Bandwidth
R in kΩ
C in µF

$$Q = \frac{f_o}{BW} < 10$$

$$C1 = C2 = \frac{Q}{3}$$

$R1 = R2 = 1 \quad R3 = 9Q^2 - 1$ } Using scaling factors in these expressions.

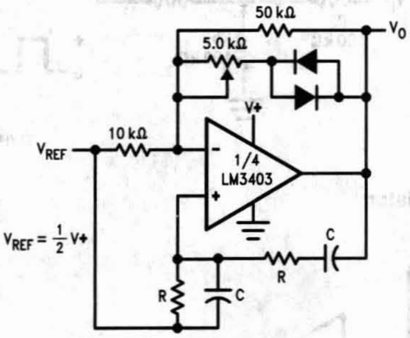
If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Design example:

given: $Q = 5$, $f_o = 1$ kHz
Let $R1 = R2 = 10$ kΩ
then $R3 = 9(5)^2 - 10$
$R3 = 215$ kΩ

$$C = \frac{5}{3} = 1.6 \text{ nF}$$

Wein Bridge Oscillator

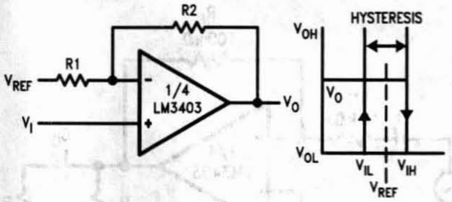

50 kΩ
5.0 kΩ
V_O
V+
10 kΩ
V_{REF}
1/4
LM3403
$V_{REF} = \frac{1}{2}$ V+
C
R
R
C

TL/H/10064-5

$$f_o = \frac{1}{2\pi RC} \text{ for } f_o = 1 \text{ kHz}$$

R = 16 kΩ
C = 0.01 µF

Comparator with Hysteresis


R2
R1
V_{REF}
V_I
1/4
LM3403
V_O
V_{OH}
HYSTERESIS
V_O
V_{OL}
V_{IL}
V_{IH}
V_{REF}

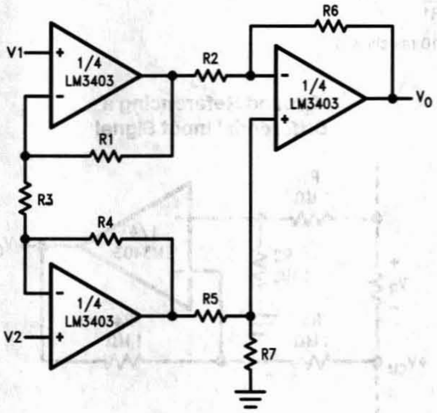
TL/H/10064-6

$$V_{IL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{IH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

High Impedance Differential Amplifier


R6
V1
1/4
LM3403
R2
1/4
LM3403
V_O
R1
R3
R4
1/4
LM3403
R5
V2
R7

TL/H/10064-7

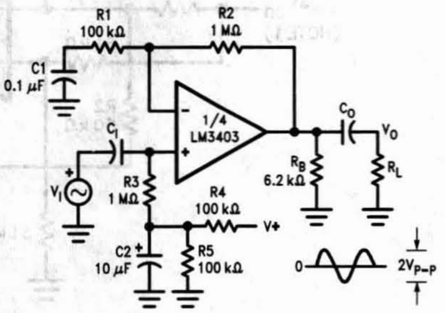
$V_{OUT} = C(1 + a + b)(V2 - V1)$

$\frac{R2}{R5} \equiv \frac{R6}{R7}$ for best CMRR

$R1 = R4$
$R2 = R5$

$$\text{Gain} = \frac{R6}{R5}\left(1 + \frac{2R1}{R3}\right) = C(1 + a + b)$$

AC Coupled Non-Inverting Amplifier


R1
100 kΩ
R2
1 MΩ
C1
0.1 µF
C_I
1/4
LM3403
C_O
V_O
V_I
R3
1 MΩ
R_B
6.2 kΩ
R_L
R4
100 kΩ
V+
C2
10 µF
R5
100 kΩ
0
$2V_{P-P}$

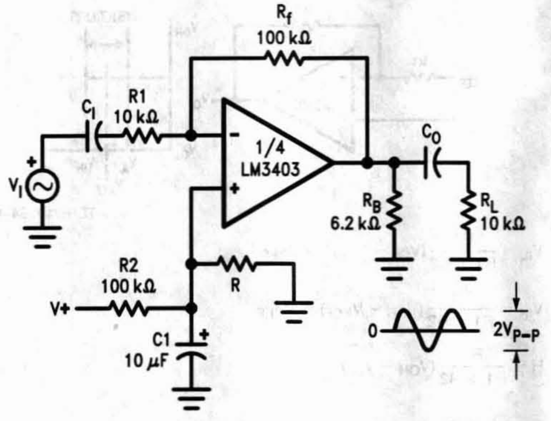
TL/H/10064-9

$$A_V = 1 + \frac{R2}{R1}$$

$A_V = 11$ (as shown)

Typical Applications (Continued)

AC Coupled Inverting Amplifier

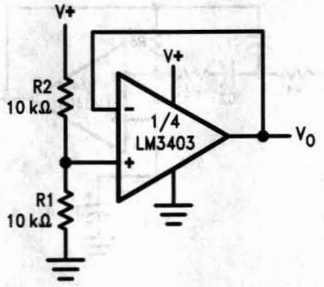

Rf
100 kΩ
CI
R1
10 kΩ
VI
1/4
LM3403
CO
RB
6.2 kΩ
RL
10 kΩ
R2
100 kΩ
R
V+
C1
10 μF
0
2VP−P

TL/H/10064-8

$A_V = \frac{Rf}{R1}$

$A_V = 10$ (as shown)

Voltage Reference

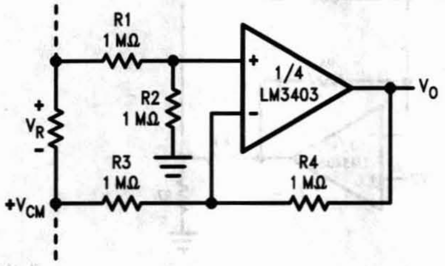

V+
R2
10 kΩ
V+
1/4
LM3403
VO
R1
10 kΩ

TL/H/10064-10

$V_O = \frac{R1}{R1 + R2}\left(= \frac{V+}{2} \text{ as shown}\right)$

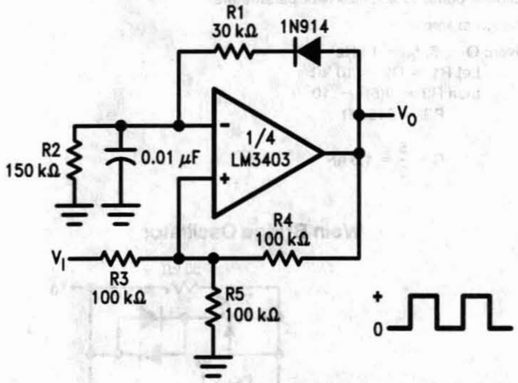
$V_O = \frac{1}{2} V+$

Ground Referencing a Differential Input Signal


R1
1 MΩ
1/4
LM3403
VO
VR
R2
1 MΩ
R3
1 MΩ
R4
1 MΩ
+VCM

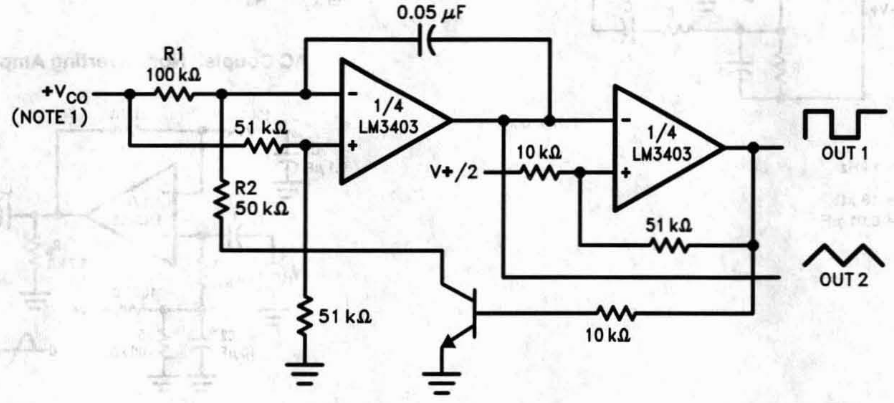
TL/H/10064-11

Pulse Generator


R1
30 kΩ
1N914
VO
R2
150 kΩ
0.01 μF
1/4
LM3403
R4
100 kΩ
VI
R3
100 kΩ
R5
100 kΩ
+
0

TL/H/10064-14

Voltage Controlled Oscillator


0.05 μF
R1
100 kΩ
+VCO
(NOTE 1)
51 kΩ
1/4
LM3403
R2
50 kΩ
V+/2
10 kΩ
1/4
LM3403
OUT 1
51 kΩ
OUT 2
51 kΩ
10 kΩ

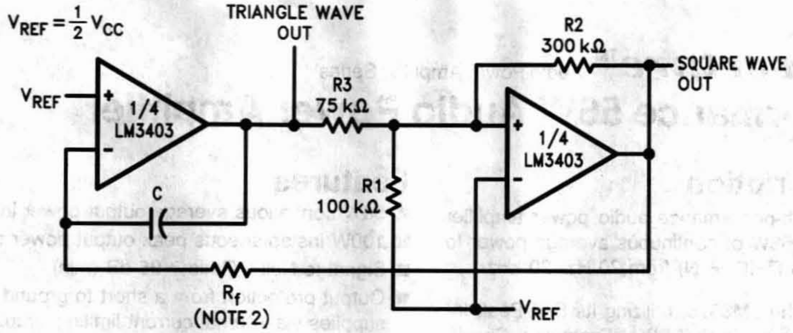
TL/H/10064-12

Note 1: Wide Control Voltage Range:

$0V \le V_{CO} \le 2\,(V \pm 1.5V)$

Typical Applications (Continued)

Function Generator

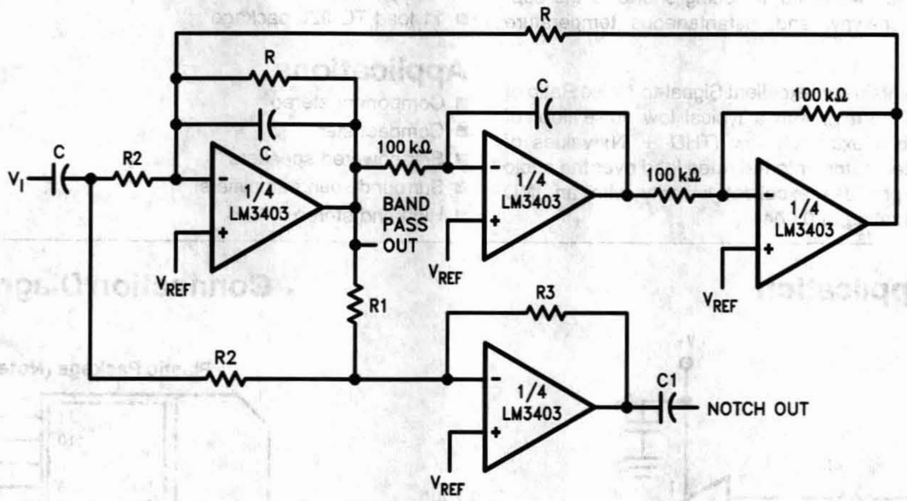


$V_{REF} = \frac{1}{2} V_{CC}$
TRIANGLE WAVE OUT
R2
300 kΩ
SQUARE WAVE OUT
V_{REF}
1/4 LM3403
R3
75 kΩ
C
R1
100 kΩ
1/4 LM3403
R_f
(NOTE 2)
V_{REF}

TL/H/10064–13

Note 2: $f = \frac{R1 + R2}{4CR_fR1}$ if $R3 = \frac{R2R1}{R2 + R1}$

Bi-Quad Filter



R
R
C
C
V_I
C
R2
1/4 LM3403
100 kΩ
BAND PASS OUT
V_{REF}
R1
1/4 LM3403
V_{REF}
100 kΩ
100 kΩ
1/4 LM3403
V_{REF}
R3
R2
1/4 LM3403
C1
NOTCH OUT
V_{REF}

TL/H/10064–15

$Q = \frac{BW}{f_o}$

where:

T_{BP} = Center Frequency Gain

T_N = Bandpass Notch Gain

$f_o = \frac{1}{2\pi RC}$, $V_{REF} = \frac{1}{2} V_{CC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_NR2$

$C1 = 10\ C$

Example:

f_o = 1000 Hz

BW = 100 Hz

T_{BP} = 1

T_N = 1

R = 160 kΩ

R1 = 1.6 MΩ

R2 = 1.6 MΩ

R3 = 1.6 MΩ

C = 0.001 μF

National Semiconductor

LM3875 *Overture*™ Audio Power Amplifier Series
High-Performance 56W Audio Power Amplifier

General Description

The LM3875 is a high-performance audio power amplifier capable of delivering 56W of continuous average power to an 8Ω load with 0.1% (THD + N) from 20 Hz–20 kHz.

The performance of the LM3875, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**) Protection Circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** Protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM3875 maintains an excellent Signal-to-Noise Ratio of greater than 95 dB(min) with a typical low noise floor of 2.0 µV. It exhibits extremely low (THD + N) values of 0.06% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

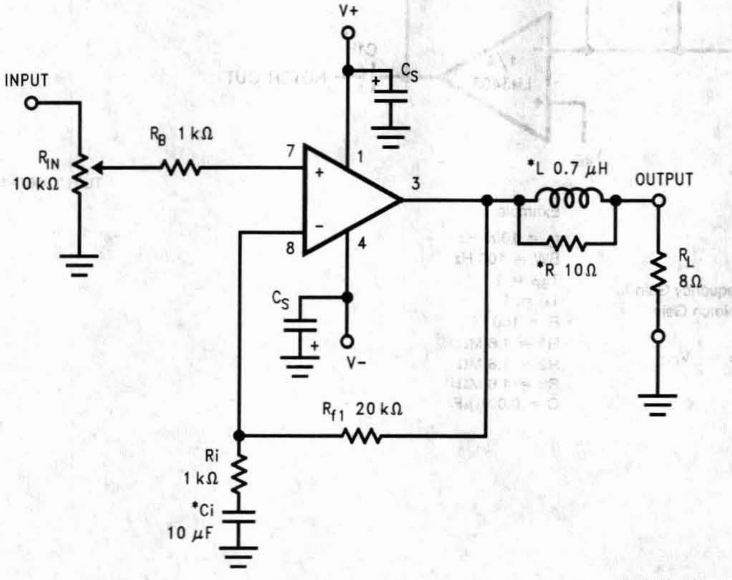
Features

- 56W continuous average output power into 8Ω
- 100W instantaneous peak output power capability
- Signal-to-Noise Ratio >95 dB (min)
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when $|V_{EE}| + |V_{CC}| \leq 12V$, thus eliminating turn-on and turn-off transients
- 11 lead TO-220 package

Applications

- Component stereo
- Compact stereo
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

Typical Application



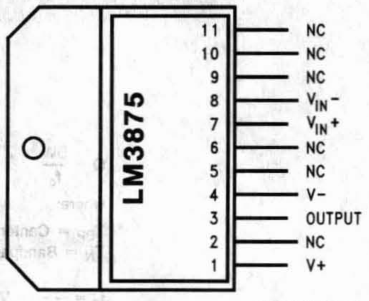
TL/H/11449-1

FIGURE 1. Typical Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component function description.

Connection Diagram

Plastic Package (Note 8)



TL/H/11449-2

Top View

Order Number LM3875T or LM3875TF
See NS Package Number TA11B for Staggered Lead Non-Isolated Package or TF11B for Staggered Lead Isolated Package

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $\lvert V^+\rvert + \lvert V^-\rvert$ (No Signal)	94V
Supply Voltage $\lvert V^+\rvert + \lvert V^-\rvert$ (Input Signal)	84V
Common Mode Input Voltage	(V^+ or V^-) and $\lvert V^+\rvert + \lvert V^-\rvert \le 80V$
Differential Input Voltage	60V
Output Current	Internally Limited
Power Dissipation (Note 3)	125W
ESD Susceptibility (Note 4)	2500V
Junction Temperature (Note 5)	150°C
Soldering Information	
T package (10 seconds)	260°C
Storage Temperature	−40°C to +150°C
Thermal Resistance	
θ_{JC}	1°C/W
θ_{JA}	43°C/W

Operating Ratings (Notes 1, 2)

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-20°C \le T_A \le +85°C$
Supply Voltage $\lvert V^+\rvert + \lvert V^-\rvert$	20V to 84V

Note: Operation is guaranteed up to 84V, however, distortion may be introduced from the **SPiKe** Protection Circuitry when operating above 70V if proper thermal considerations are not taken into account. Refer to the Thermal Considerations section for more information. (See **SPiKe** Protection Response)

Electrical Characteristics (Notes 1, 2) The following specifications apply for $V^+ = +35V$, $V^- = -35V$ with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	LM3875		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
$\lvert V^+\rvert + \lvert V^-\rvert$	Power Supply Voltage			20 84	V (Min) V (Max)
**P_O	Output Power (Continuous Average)	THD + N = 0.1% (Max) f = 1 kHz, f = 20 kHz	56	40	W (Min)
Peak P_O	Instantaneous Peak Output Power		100		W
THD + N	Total Harmonic Distortion Plus Noise	40W, 20 Hz ≤ f ≤ 20 kHz $A_V = 26$ dB	0.06		%
**SR	Slew Rate (Note 9)	$V_{IN} = 1.414$ Vrms, f = 10 kHz Square-wave, $R_L = 2\ k\Omega$	11	5	V/µs (Min)
*I+	Total Quiescent Power Supply Current	$V_{CM} = 0V$, $V_O = 0V$, $I_o = 0$ mA	30	70	mA (Max)
*V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $I_o = 0$ mA	1	10	mV (Max)
I_B	Input Bias Current	$V_{CM} = 0V$, $I_o = 0$ mA	0.2	1	µA (Max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$, $I_o = 0$ mA	0.01	0.2	µA (Max)
I_o	Output Current Limit	$\lvert V^+\rvert = \lvert V^-\rvert = 10V$, $t_{on} = 10$ ms, $V_O = 0V$	6	4	A (Min)
*V_{od}	Output Dropout Voltage (Note 10)	$\lvert V^+ - V_o\rvert$, $V^+ = 20V$, $I_o = +100$ mA $\lvert V_o - V^-\rvert$, $V^- = -20V$, $I_o = -100$ mA	1.6 2.7	5 5	V (Max) V (Max)
*PSRR	Power Supply Rejection Ratio	$V^+ = 40V$ to $20V$, $V^- = -40V$, $V_{cm} = 0V$, $I_o = 0$ mA $V^+ = 40V$, $V^- = -40V$ to $-20V$, $V_{cm} = 0V$, $I_o = 0$ mA	120 120	85 85	dB (Min)
*CMRR	Common Mode Rejection Ratio	$V^+ = 60V$ to $20V$, $V^- = -20V$ to $-60V$, $V_{cm} = 20V$ to $-20V$, $I_o = 0$ mA	120	80	dB (Min)
*A_{VOL}	Open Loop Voltage Gain	$\lvert V^+\rvert = \lvert V^-\rvert = 40V$, $R_L = 2\ k\Omega$, $\Delta V_O = 60V$	120	90	dB (Min)
GBWP	Gain-Bandwidth Product	$\lvert V^+\rvert = \lvert V^-\rvert = 40V$ $f_O = 100$ kHz, $V_{IN} = 50$ mVrms	8	2	MHz (Min)
**e_{IN}	Input Noise	IHF − A Weighting Filter $R_{IN} = 600\Omega$ (Input Referred)	2.0	8.0	µV (Max)

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Electrical Characteristics

(Notes 1, 2) The following specifications apply for $V^+ = +35V$, $V^- = -35V$ with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25°C$. (Continued)

Symbol	Parameter	Conditions	LM3875		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
SNR	Signal-to-Noise Ratio	$P_O = 1W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	98 dB		dB
		$P_O = 40W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	114 dB		dB
		$P_{pk} = 100W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	122 dB		dB
IMD	Intermodulation Distortion Test	60 Hz, 7 kHz, 4:1 (SMPTE) 60 Hz, 7 kHz, 1:1 (SMPTE)	0.004 0.006		%

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Note 1: All voltages are measured with respect to supply GND, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at case temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of $\theta_{JC} = 1.0°C/W$ (junction to case). Refer to the Thermal Resistance figure in the Application Information section under **Thermal Considerations.**

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: The operating junction temperature maximum is 150°C, however, the instantaneous Safe Operating Area temperature is 250°C.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

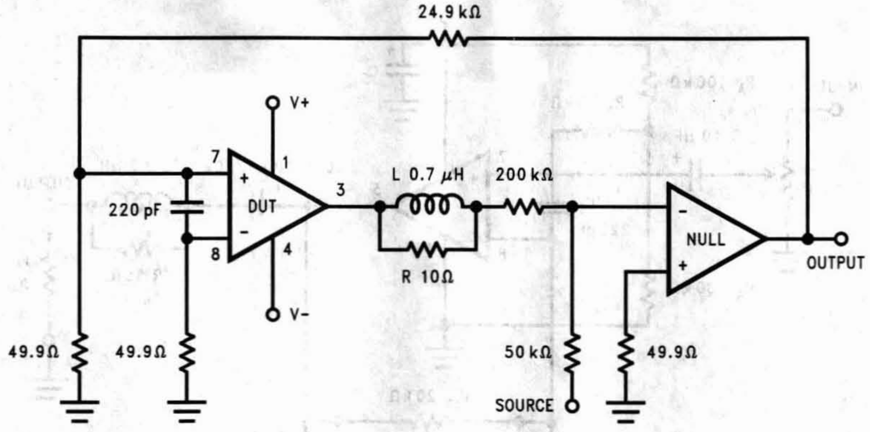
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The LM3875T package TA11B is a non-isolated package, setting the tab of the device and the heat sink at V^- potential when the LM3875 is directly mounted to the heat sink using only thermal compound. If a mica washer is used in addition to thermal compound, θ_{CS} (case to sink) is increased, but the heat sink will be isolated from V^-.

Note 9: The feedback compensation network limits the bandwidth of the closed-loop response and so the slew rate will be reduced due to the high frequency roll-off. Without feedback compensation, the slew rate is typically 16V/μs.

Note 10: The output dropout voltage is the supply voltage minus the clipping voltage. Refer to the Clipping Voltage vs. Supply Voltage graph in the **Typical Performance Characteristics** section.

Test Circuit #1 *(DC Electrical Test Circuit)


24.9 kΩ
V+
7
1
+
DUT
−
8
4
3
220 pF
L 0.7 μH
200 kΩ
R 10Ω
V−
NULL
−
+
OUTPUT
49.9Ω
49.9Ω
50 kΩ
49.9Ω
SOURCE

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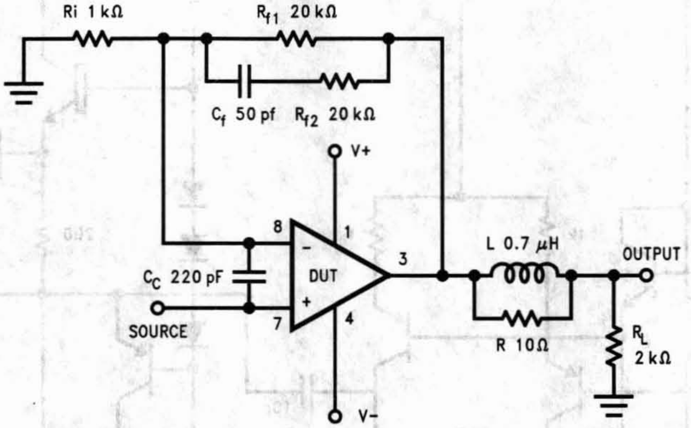
Test Circuit #2 (** AC Electrical Test Circuit)


Ri 1 kΩ
R_{f1} 20 kΩ
C_f 50 pf
R_{f2} 20 kΩ
V+
8
1
−
DUT
+
7
4
3
C_C 220 pF
SOURCE
V−
L 0.7 μH
R 10Ω
OUTPUT
R_L 2 kΩ

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Single Supply Application Circuit

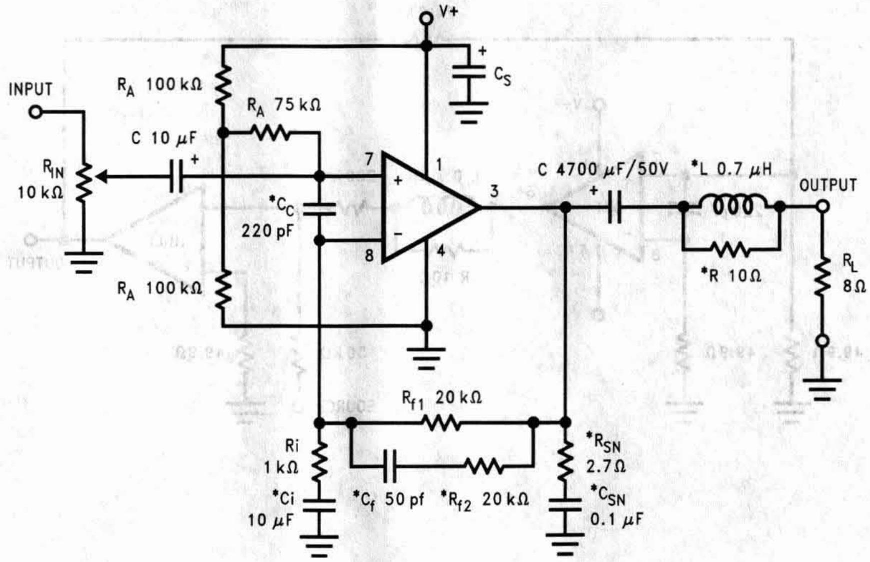
V+
+
C_S
INPUT
R_A 100 kΩ
R_A 75 kΩ
C 10 μF
+
R_{IN} 10 kΩ
7
1
+
*C_C 220 pF
−
8
4
3
C 4700 μF/50V
+
*L 0.7 μH
OUTPUT
*R 10Ω
R_L 8Ω
R_A 100 kΩ
R_{f1} 20 kΩ
Ri 1 kΩ
*R_{SN} 2.7Ω
*Ci 10 μF
*C_f 50 pf
*R_{f2} 20 kΩ
*C_{SN} 0.1 μF

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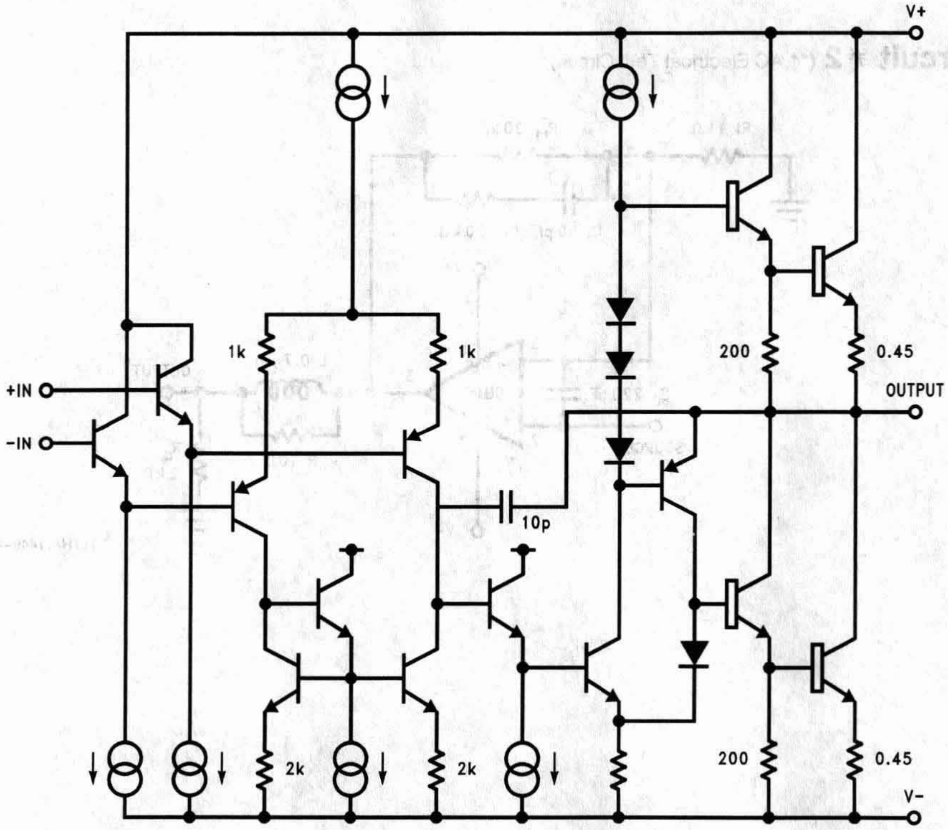
FIGURE 2. Typical Single Supply Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component function description.

Equivalent Schematic (Excluding active protection circuitry)


V+
1k
1k
200
0.45
+IN
−IN
OUTPUT
10p
2k
2k
200
0.45
V−

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External Components Description (*Figures 1* and *2*)

Components		Functional Description
1.	R_{IN}	Acts as a volume control by setting the voltage level allowed to the amplifier's input terminals.
2.	R_A	Provides DC voltage biasing for the single supply operation and bias current for the positive input terminal.
3.	C_A	Provides bias filtering.
4.	C	Provides AC coupling at the input and output of the amplifier for single supply operation.
5.	R_B	Prevents currents from entering the amplifier's non-inverting input which may be passed through to the load upon power-down of the system due to the low input impedance of the circuitry when the under-voltage circuitry is off. This phenomenon occurs when the supply voltages are below 1.5V.
6.	*C_C	Reduces the gain (bandwidth of the amplifier) at high frequencies to avoid quasi-saturation oscillations of the output transistor. The capacitor also suppresses external electromagnetic switching noise created from fluorescent lamps.
7.	Ri	Inverting input resistance to provide AC Gain in conjunction with R_{f1}.
8.	*Ci	Feedback capacitor. Ensures unity gain at DC. Also a low frequency pole (highpass roll-off) at: $f_c = 1/(2\pi \text{ Ri Ci})$.
9.	R_{f1}	Feedback resistance to provide AC Gain in conjunction with Ri.
10.	*R_{f2}	At higher frequencies feedback resistance works with C_f to provide lower AC Gain in conjunction with R_{f1} and Ri. A high frequency pole (lowpass roll-off) exists at: $f_c = [R_{f1} R_{f2}] (s + 1/R_{f2} C_f]/[(R_{f1} + R_{f2}) (s + 1/C_f (R_{f1} + R_{f2}))]$.
11.	*C_f	Compensation capacitor that works with R_{f1} and R_{f2} to reduce the AC Gain at higher frequencies.
12.	*R_{SN}	Works with C_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations.
13.	*C_{SN}	Works with R_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations. $f_c = 1/(2\pi R_{SN} C_{SN})$.
14.	*L	Provides high impedance at high frequencies so that R may decouple a highly capacitive load and reduce the Q of the series resonant circuit due to capacitive load. Also provides a low impedance at low frequencies to short out R and pass audio signals to the load.
15.	*R	
16.	C_S	Provides power supply filtering and bypassing.

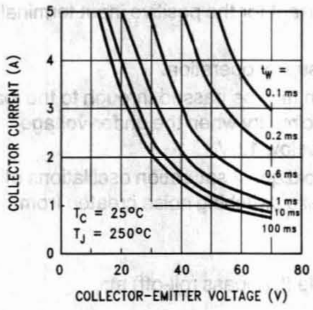
*Optional components dependent upon specific design requirements. Refer to the Application Information section for more information.

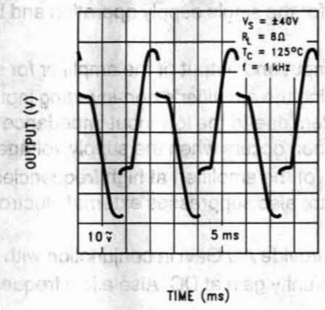
OPTIONAL EXTERNAL COMPONENT INTERACTION

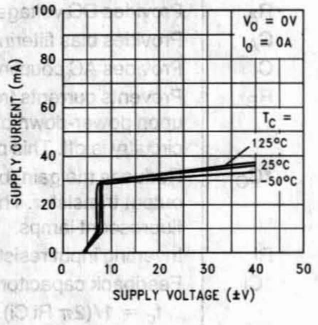
Although the optional external components have specific desired functions that are designed to reduce the bandwidth and eliminate unwanted high frequency oscillations they may cause certain undesirable effects when they interact. Interaction may occur for components whose reactances are in close proximity to one another. One example would be the coupling capacitor, C_C, and the compensation capacitor, C_f. These two components act as low impedances to certain frequencies which will couple signals from the input to the output. Please take careful note of basic amplifier component functionality when designing in these components.

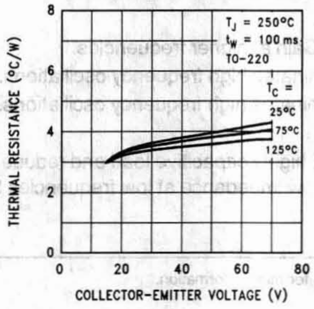
The optional external components shown in *Figure 2* and described above are applicable in both single and split voltage supply configurations.

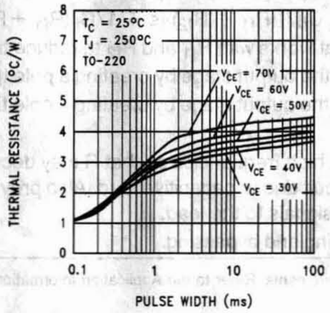
Typical Performance Characteristics

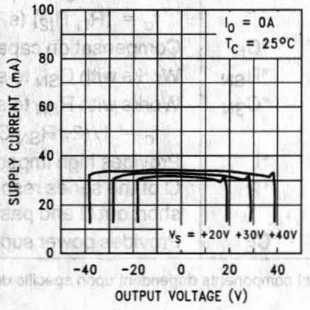

Safe Area

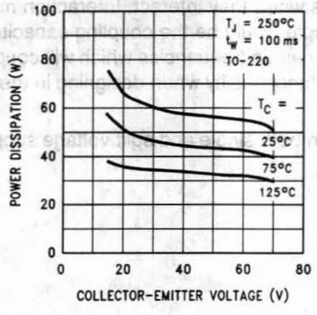

SPiKe Protection Response

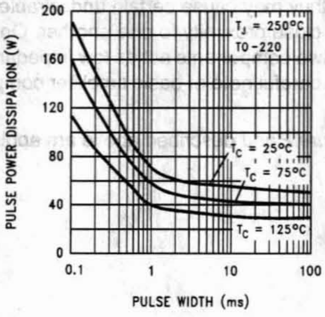

Supply Current vs Supply Voltage

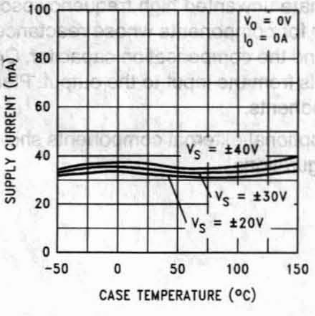

Pulse Thermal Resistance

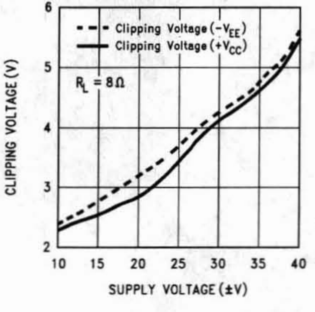

Pulse Thermal Resistance

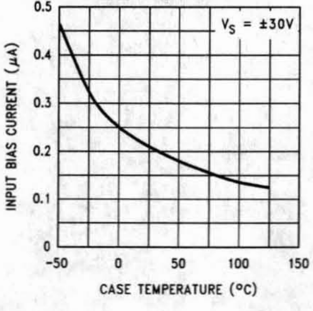

Supply Current vs Output Voltage

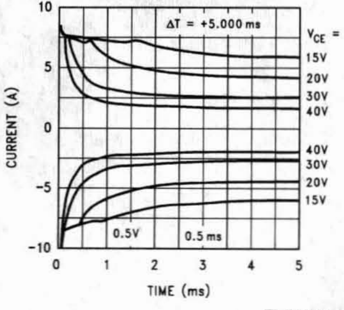

Pulse Power Limit


Pulse Power Limit


Supply Current vs Case Temperature


Clipping Voltage vs Supply Voltage


Input Bias Current vs Case Temperature


Peak Output Current

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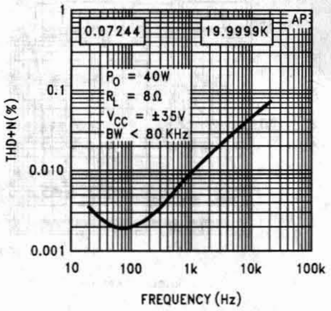
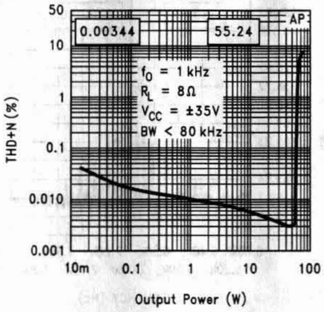
Typical Performance Characteristics (Continued)

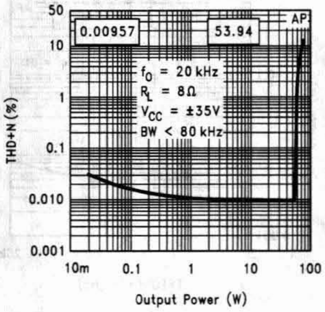
THD + N vs Frequency



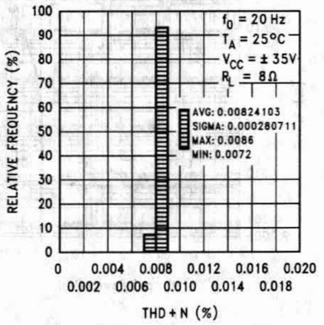
THD + N vs Output Power



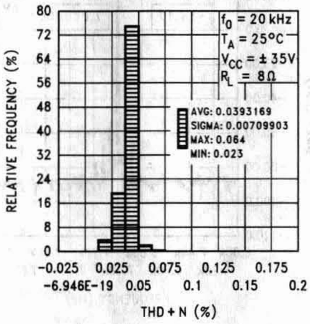
THD + N vs Output Power



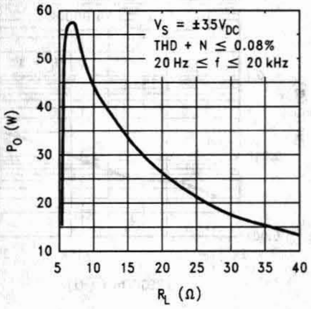
THD Distribution



THD Distribution



Output Power vs Load Resistance



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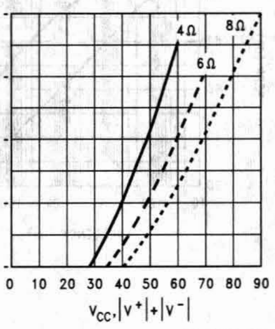
Max Heatsink Thermal Resistance (°C/W) at the Specified Ambient Temperature (°C)

T_A = 25°C	40	50	60	70	80	90	100	110	T_C, °C	P_D, W
1.3	1.0								90	50
1.6	1.2	1.0							96	45
1.9	1.6	1.3	1.1						102	40
2.4	1.9	1.7	1.4	1.1					108	35
3.0	2.5	2.1	1.8	1.5	1.1				114	30
3.8	3.2	2.8	2.4	2.0	1.6	1.2			120	25
5.1	4.3	3.8	3.3	2.8	2.3	1.8	1.3		126	20
7.1	6.1	5.5	4.8	4.1	3.5	2.8	2.1	1.5	132	15
11.3	9.8	8.8	7.8	6.8	5.8	4.8	3.8	2.8	138	10

Note: The maximum heat sink thermal resistance values, $\varnothing_{SA}$, in the table above were calculated using a $\varnothing_{CS}$ = 0.2°C/W due to thermal compound.

Maximum Power Dissipation vs Supply Voltage



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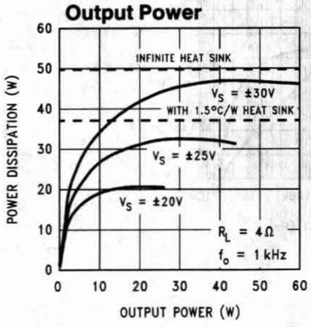
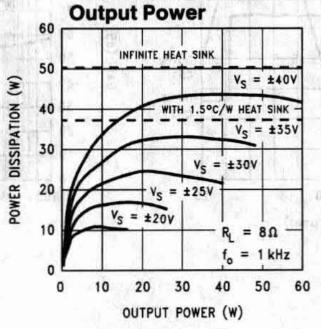
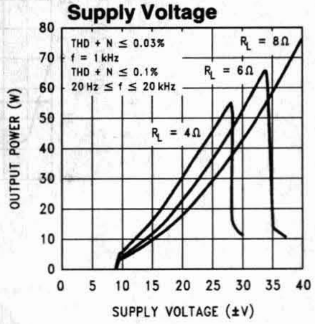
Power Dissipation vs Output Power



Power Dissipation vs Output Power



Output Power vs Supply Voltage



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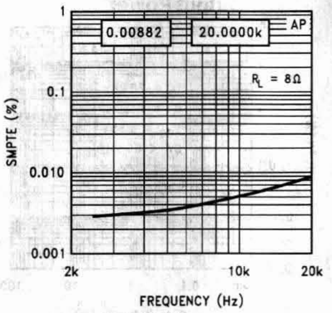
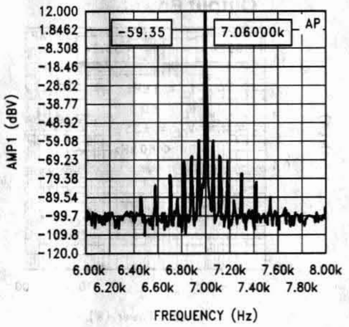
Typical Performance Characteristics (Continued)

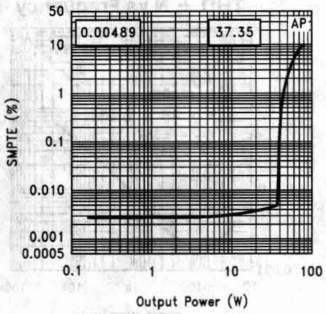
IMD 60 Hz, 4:1



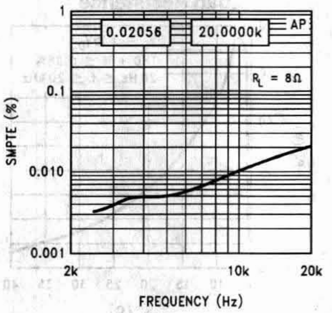
IMD 60 Hz, 7 kHz, 4:1



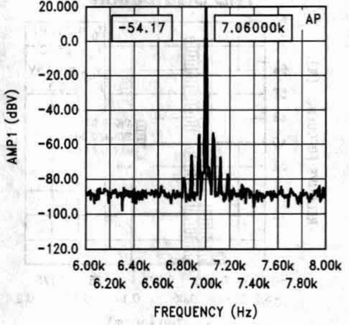
IMD 60 Hz, 7 kHz, 4:1



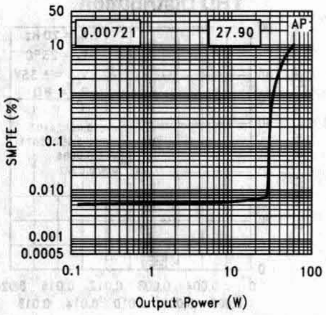
IMD 60 Hz, 1:1



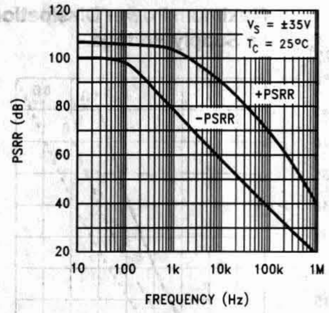
IMD 60 Hz, 7 kHz, 1:1



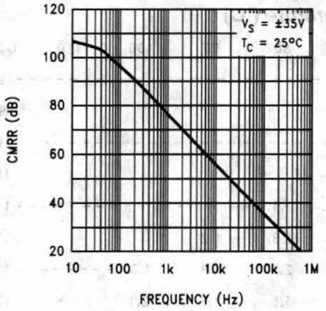
IMD 60 Hz, 7 kHz, 1:1



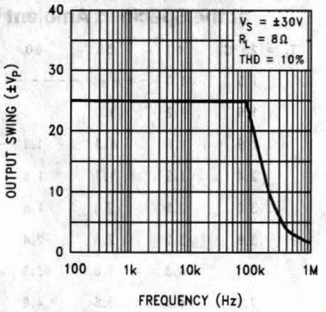
Power Supply Rejection Ratio



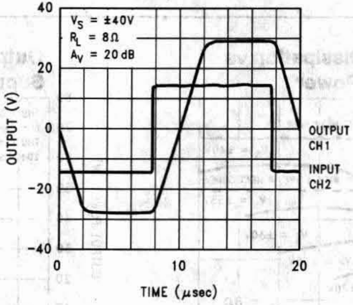
Common-Mode Rejection Ratio



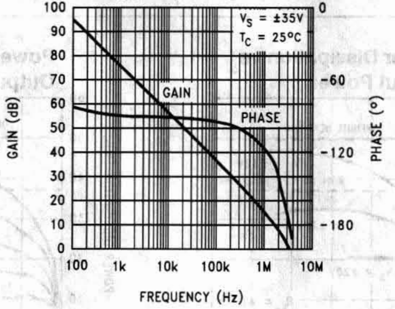
Large Signal Response



Pulse Response



Open Loop Frequency Response



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Application Information

GENERAL FEATURES

Under-Voltage Protection: Upon system power-up the under-voltage Protection Circuitry allows the power supplies and their corresponding caps to come up close to their full values before turning on the LM3875 such that no DC output spikes occur. Upon turn-off, the output of the LM3875 is brought to ground before the power supplies such that no transients occur at power-down.

Over-Voltage Protection: The LM3875 contains overvoltage protection circuitry that limits the output current to approximately 4Apeak while also providing voltage clamping, though not through internal clamping diodes. The clamping effect is quite the same, however, the output transistors are designed to work alternately by sinking large current spikes.

SPiKe Protection: The LM3875 is protected from instantaneous peak-temperature stressing by the power transistor array. The Safe Operating Area graph in the **Typical Performance Characteristics** section shows the area of device operation where the **SPiKe** Protection Circuitry is not enabled. The waveform to the right of the SOA graph exemplifies how the dynamic protection will cause waveform distortion when enabled.

Thermal Protection: The LM3875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 165°C, the LM3875 shuts down. It starts operating again when the die temperature drops to about 155°C, but if the temperature again begins to rise, shutdown will occur again at 165°C. Therefore the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 165°C and 155°C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen as discussed in the **Thermal Considerations** section, such that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

THERMAL CONSIDERATIONS

Heat Sinking

The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry does not operate under normal circumstances. The heat sink should be chosen to dissipate the maximum IC power for a given supply voltage and rated load.

With high-power pulses of longer duration than 100 ms, the case temperature will heat up drastically without the use of a heat sink. Therefore the case temperature, as measured at the center of the package bottom, is entirely dependent on heat sink design and the mounting of the IC to the heat sink. For the design of a heat sink for your audio amplifier application refer to the **Determining the Correct Heat Sink** section.

Since a semiconductor manufacturer has no control over which heat sink is used in a particular amplifier design, we can only inform the system designer of the parameters and the method needed in the determination of a heat sink. With this in mind, the system designer must choose his supply voltages, a rated load, a desired output power level, and know the ambient temperature surrounding the device. These parameters are in addition to knowing the maximum junction temperature and the thermal resistance of the IC, both of which are provided by National Semiconductor.

As a benefit to the system designer we have provided Maximum Power Dissipation vs Supply Voltages curves for various loads in the **Typical Performance Characteristics** section, giving an accurate figure for the maximum thermal resistance required for a particular amplifier design. This data was based on $\theta_{JC} = 1°C/W$ and $\theta_{CS} = 0.2°C/W$. We also provide a section regarding heat sink determination for any audio amplifier design where θ_{CS} may be a different value. It should be noted that the idea behind dissipating the maximum power within the IC is to provide the device with a low resistance to convection heat transfer such as a heat sink. Therefore, it is necessary for the system designer to be conservative in his heat sink calculations. As a rule, the lower the thermal resistance of the heat sink the higher the amount of power that may be dissipated. This is, of course, guided by the cost and size requirements of the system. Convection cooling heat sinks are available commercially, and their manufacturers should be consulted for ratings.

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, the thermal resistance will be no better than 0.5°C/W, and probably much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important and can be determined from heat sink manufacturer's specification sheets.

Should it be necessary to isolate V^- from the heat sink, an insulating washer is required. Hard washers like berylum oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound.

Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

Determining Maximum Power Dissipation

Power dissipation within the integrated circuit package is a very important parameter requiring a thorough understanding if optimum power output is to be obtained. An incorrect maximum power dissipation (P_D) calculation may result in inadequate heatsinking, causing thermal shutdown circuitry to operate and limit the output power.

1

Application Information (Continued)

The following equations can be used to accurately calculate the maximum and average integrated circuit power dissipation for your amplifier design, given the supply voltage, rated load, and output power. These equations can be directly applied to the Power Dissipation vs Output Power curves in the **Typical Performance Characteristics** section.

Equation (1) exemplifies the maximum power dissipation of the IC and equations (2) and (3) exemplify the average IC power dissipation expressed in different forms.

$$P_{DMAX} = V_{CC}^2/2\pi^2 R_L \qquad (1)$$

where V_{CC} is the total supply voltage

$$P_{DAVE} = (V_{Opk}/R_L)\,[V_{CC}/\pi - V_{Opk}/2] \qquad (2)$$

where V_{CC} is the total supply voltage and $V_{Opk} = V_{CC}/\pi$

$$P_{DAVE} = V_{CC}\,V_{Opk}/\pi R_L - V_{Opk}^2/2 R_L \qquad (3)$$

where V_{CC} is the total supply voltage.

Determining the Correct Heat Sink

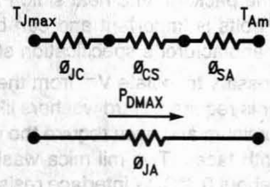
Once the maximum IC power dissipation is known for a given supply voltage, rated load, and the desired rated output power the maximum thermal resistance (in °C/W) of a heat sink can be calculated. This calculation is made using equation (4) and is based on the fact that thermal heat flow parameters are analogous to electrical current flow properties.

It is also known that typically the thermal resistance, θ_{JC} (junction to case), of the LM3875 is 1°C/W and that using Thermalloy Thermacote thermal compound provides a thermal resistance, θ_{CS} (case to heat sink), of about 0.2°C/W as explained in the **Heat Sinking** section.

Referring to the figure below, it is seen that the thermal resistance from the die (junction) to the outside air (ambient) is a combination of three thermal resistances, two of which are known, θ_{JC} and θ_{CS}. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LM3875 is equal to the following:

$$P_{DMAX} = (T_{Jmax} - T_{Amb})/\theta_{JA}$$

where $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$



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But since we know P_{DMAX}, θ_{JC}, and θ_{SC} for the application and we are looking for θ_{SA}, we have the following:

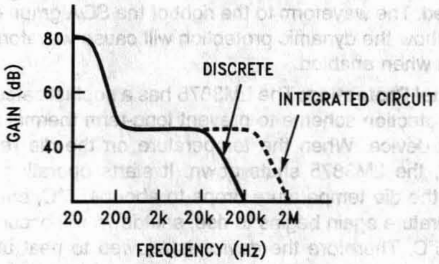
$$\theta_{SA} = [(T_{Jmax} - T_{Amb}) - P_{DMAX}(\theta_{JC} + \theta_{CS})]/P_{DMAX} \qquad (4)$$

Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier application and its corresponding parameters as described previously. If the ambient temperature that the audio amplifier is to be working under is higher than the normal 25°C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

Equations (1) and (4) are the only equations needed in the determination of the maximum heat sink thermal resistance. This is, of course, given that the system designer knows the required supply voltages to drive his rated load at a particular power output level and the parameters provided by the semiconductor manufacturer. These parameters are the junction to case thermal resistance, θ_{JC}, $T_{Jmax} = 150°C$, and the recommended Thermalloy Thermacote thermal compound resistance, θ_{CS}.

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit designs to discrete amplifier designs. Discrete transistor amps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated below.



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Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal-to-noise measurements if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth, (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a "weighting" filter.[1] A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to the frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

In addition to noise filtering, differing meter types give different noise readings. Meter responses include:

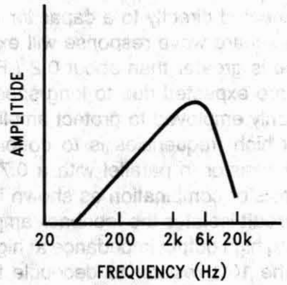
1. RMS reading,
2. average responding,
3. peak reading, and
4. quasi peak reading.

Reference 1: CCIR/ARM: *A Practical Noise Measurement Method*; by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

Application Information (Continued)

Although theoretical noise analysis is derived using true RMS based calculations, most actual measurements are taken with ARM (Average Responding Meter) test equipment.

Typical signal-to-noise figures are listed for an A-weighted filter which is commonly used in the measurement of noise. The shape of all weighting filters is similar, with the peak of the curve usually occurring in the 3 kHz–7 kHz region as shown below.



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SUPPLY BYPASSING

The LM3875 has excellent power supply rejection and does not require a regulated supply. However, to eliminate possible oscillations all op amps and power op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as "motorboating" or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10 μF or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1 μF) to prevent any high frequency feedback through the power supply lines.

If adequate bypassing is not provided the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes low distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470 μF or more.

LEAD INDUCTANCE

Power op amps are sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load.

Lead inductance can also cause voltage surges on the supplies. With long leads to the power supply, energy is stored in the lead inductance when the output is shorted. This energy can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With at least a 20 μF local bypass, these voltage surges are important only if the lead length exceeds a couple feet (>1 μH lead inductance). Twisting together the supply and ground leads minimizes the effect.

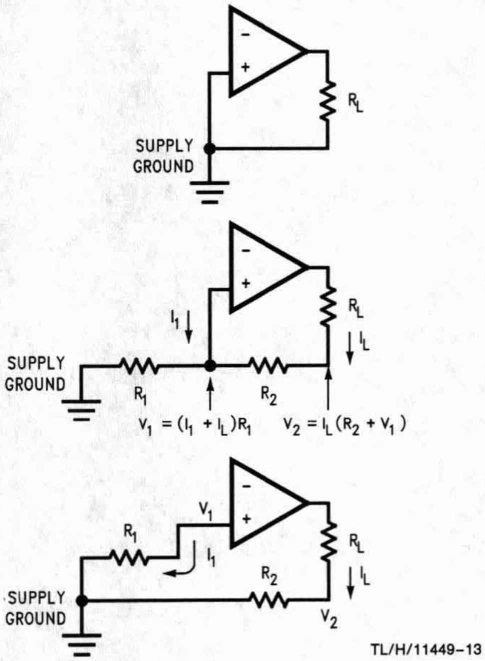
LAYOUT, GROUND LOOPS AND STABILITY

The LM3875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but as with any other high-current amplifier, the LM3875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board common ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM3875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths should be as short as possible.

In general, with fast, high-current circuitry, all sorts of problems can arise from improper grounding which again can be avoided by returning all grounds separately to a common point. Without isolating the ground signals and returning the grounds to a common point, ground loops may occur.

"Ground Loop" is the term used to describe situations occurring in ground systems where a difference in potential exists between two ground points. Ideally a ground is a ground, but unfortunately, in order for this to be true, ground conductors with zero resistance are necessary. Since real world ground leads possess finite resistance, currents running through them will cause finite voltage drops to exist. If two ground return lines tie into the same path at different points there will be a voltage drop between them. The first figure below shows a common ground example where the positive input ground and the load ground are returned to the supply ground point via the same wire. The addition of the finite wire resistance, R_2, results in a voltage difference between the two points as shown below.



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Application Information (Continued)

The load current I_L will be much larger than input bias current I_1, thus V_1 will follow the output voltage directly, i.e., in phase. Therefore the voltage appearing at the non-inverting input is effectively positive feedback and the circuit may oscillate. If there were only one device to worry about then the values of R_1 and R_2 would probably be small enough to be ignored; however, several devices normally comprise a total system. Any ground return of a separate device, whose output is in phase, can feedback in a similar manner and cause instabilities. Out of phase ground loops also are troublesome, causing unexpected gain and phase errors.

The solution to most ground loop problems is to always use a single-point ground system, although this is sometimes impractical. The third figure above is an example of a single-point ground system.

The single-point ground concept should be applied rigorously to all components and all circuits when possible. Violations of single-point grounding are most common among printed circuit board designs, since the circuit is surrounded by large ground areas which invite the temptation to run a device to the closest ground spot. As a final rule, make all ground returns low resistance and low inductance by using large wire and wide traces.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor, C_C, (on the order of 50 pF–500 pF) across the LM3875 input terminals. Refer to the **External Components Description** section relating to component interaction with C_f.

REACTIVE LOADING

It is hard for most power amplifiers to drive highly capacitive loads very effectively and normally results in oscillations or ringing on the square wave response. If the output of the LM3875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.2 μF. If highly capacitive loads are expected due to long speaker cables, a method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 0.7 μH inductor. The inductor-resistor combination as shown in the **Typical Application Circuit** isolates the feedback amplifier from the load by providing high output impedance at high frequencies thus allowing the 10Ω resistor to decouple the capacitive load and reduce the Q of the series resonant circuit. The LR combination also provides low output impedance at low frequencies thus shorting out the 10Ω resistor and allowing the amplifier to drive the series RC load (large capacitive load due to long speaker cables) directly.

Application Information (Continued)

GENERALIZED AUDIO POWER AMPLIFIER DESIGN

The system designer usually knows some of the following parameters when starting an audio amplifier design:

Desired Power Output	Input Level
Input Impedance	Load Impedance
Maximum Supply Voltage	Bandwidth

The power output and load impedance determine the power supply requirements, however, depending upon the application some system designers may be limited to certain maximum supply voltages. If the designer does have a power supply limitation, he should choose a practical load impedance which would allow the amplifier to provide the desired output power, keeping in mind the current limiting capabilities of the device. In any case, the output signal swing and current are found from (where P_O is the average output power):

$$V_{opeak} = \sqrt{2 R_L P_O} \qquad (1)$$

$$I_{opeak} = \sqrt{(2 P_O)/R_L} \qquad (2)$$

To determine the maximum supply voltage the following parameters must be considered. Add the dropout voltage (5 volts for LM3875) to the peak output swing, V_{opeak}, to get the supply rail value, (i.e. $\pm$ (V_{opeak} + Vod) at a current of I_{opeak}). The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions. Therefore, the maximum supply voltage is obtained from the following equation:

$$\text{max. supplies} \approx \pm (V_{opeak} + \text{Vod})(1 + \text{regulation})(1.1) \qquad (3)$$

The input sensitivity and the output power specs determine the minimum required gain as depicted below:

$$A_V \geq (\sqrt{P_O R_L})/(V_{IN}) = V_{orms}/V_{inrms} \qquad (4)$$

Normally the gain is set between 20 and 200; for a 40W, 8Ω audio amplifier this results in a sensitivity of 894 mV and 89 mV, respectively. Although higher gain amplifiers provide greater output power and dynamic headroom capabilities, there are certain shortcomings that go along with the so called "gain". The input referred noise floor is increased and hence the SNR is worse. With the increase in gain, there is also a reduction of the power bandwidth which results in a decrease in feedback thus not allowing the amplifier to respond as quickly to nonlinearities. This decreased ability to respond to nonlinearities increases the THD + N specification.

The desired input impedance is set by R_{IN}. Very high values can cause board layout problems and DC offsets at the output. The value for the feedback resistance, R_{f1}, should be chosen to be a relatively large value (10 kΩ–100 kΩ), and the other feedback resistance, Ri, is calculated using standard op amp configuration gain equations. Most audio amplifiers are designed from the non-inverting amplifier configuration.

DESIGN A 40W/8Ω AUDIO AMPLIFIER

Given:

Power Output	40W
Load Impedance	8Ω
Input Level	$1V_{(max)}$
Input Impedance	100 kΩ
Bandwidth	20 Hz–20 kHz ±0.25 dB

Equation (1) and (2) give:

40W/8Ω $\quad V_{opeak} = 25.3V \quad I_{opeak} = 3.16A$

Therefore the supply required is: ±30.3V @3.16A

With 15% regulation and high line the final supply voltage is ±38.3V using equation (3). At this point it is a good idea to check the Power Output vs Supply Voltage to ensure that the required output power is obtainable from the device while maintaining low THD + N. It is also good to check the Power Dissipation vs Supply Voltage to ensure that the device can handle the internal power dissipation. At the same time designing in a relatively practical sized heat sink with a low thermal resistance is also important. Refer to **Typical Performance Characteristics** graphs and the **Thermal Considerations** section for more information.

The minimum gain from equation (4) is: $A_V \geq 18$

We select a gain of 21 (Non-Inverting Amplifier); resulting in a sensitivity of 894 mV.

Letting R_{IN} equal 100 kΩ gives the required input impedance, however, this would eliminate the "volume control" unless an additional input impedance was placed in series with the 10 kΩ potentiometer that is depicted in *Figure 1*. Adding the additional 100 kΩ resistor would ensure the minimum required input impedance.

For low DC offsets at the output we let R_{f1} = 100 kΩ. Solving for Ri (Non-Inverting Amplifier) gives the following:

$$Ri = R_{f1}/(A_V - 1) = 100k/(21 - 1) = 5\ k\Omega;\ \text{use } 5.1\ k\Omega$$

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole give 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = 20\ Hz/5 = 4\ Hz$$

$$f_H = 20\ kHz \times 5 = 100\ kHz$$

At this point, it is a good idea to ensure that the Gain Bandwidth Product for the part will provide the designed gain out to the upper 3 dB point of 100 kHz. This is why the minimum GBWP of the LM3875 is important.

$$GBWP = A_V \times f3\ dB = 21 \times 100\ kHz = 2.1\ MHz$$

$$GBWP = 2.0\ MHz\ (min)\ for\ LM3875$$

Solving for the low frequency roll-off capacitor, Ci, we have:

$$Ci > 1/(2\pi\ Ri\ f_L) = 7.8\ \mu F;\ \text{use } 10\ \mu F.$$

Definition of Terms

Input Offset Voltage: The absolute value of the voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage and current.

Input Bias Current: The absolute value of the average of the two input currents with the output voltage and current at zero.

Input Offset Current: The absolute value of the difference in the two input currents with the output voltage and current at zero.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Common-Mode Rejection: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Quiescent Supply Current: The current required from the power supply to operate the amplifier with no load and the output voltage and current at zero.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Class B Amplifier: The most common type of audio power amplifier that consists of two output devices each of which conducts for 180° of the input cycle. The LM3875 is a Quasi-AB type amplifier.

Crossover Distortion: Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current providing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for ICs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion on the negative going transistion through zero crossing at the higher audio frequencies.

THD + N: Total Harmonic Distortion plus Noise refers to the measurement technique in which the fundamental component is removed by a bandreject (notch) filter and all remaining energy is measured including harmonics and noise.

Signal-to-Noise Ratio: The ratio of a system's output signal level to the system's output noise level obtained in the absence of a signal. The output reference signal is either specified or measured at a specified distortion level.

Continuous Average Output Power: The minimum sine wave continuous average power output in watts (or dBW) that can be delivered into the rated load, over the rated bandwidth, at the rated maximum total harmonic distortion.

Music Power: A measurement of the peak output power capability of an amplifier with either a signal duration sufficiently short that the amplifier power supply does not sag during the measurement, or when high quality external power supplies are used. This measurement (an IHF standard) assumes that with normal music program material the amplifier power supplies will sag insignificantly.

Peak Power: Most commonly referred to as the power output capability of an amplifier that can be delivered to the load; specified by the part's maximum voltage swing.

Headroom: The margin between an actual signal operating level (usually the power rating of the amplifier with particular supply voltages, a rated load value, and a rated THD + N figure) and the level just before clipping distortion occurs, expressed in decibels.

Large Signal Voltage Gain: The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

Output-Current Limit: The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once SPiKe protection circuitry is activated.

Output Saturation Threshold (Clipping Point): The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Power Dissipation Rating: The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

Thermal Resistance: The peak, junction-temperature rise, per unit of internal power dissipation (units in °C/W), above the case temperature as measured at the center of the package bottom.

The DC thermal resistance applies when one output transistor is operating continuously. The AC thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

Power Bandwidth: The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 3 dB below the rated output. For example, an amplifier rated at 60W with ≤0.25% THD + N, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

Gain-Bandwidth Product: The Gain-Bandwidth Product is a way of predicting the high-frequency usefulness of an op amp. The Gain-Bandwidth Product is sometimes called the unity-gain frequency or unity-gain cross frequency because the open-loop gain characteristic passes through or crosses unity gain at this frequency. Simply, we have the following relationship:

$$A_{CL1} \times f_1 = A_{CL2} \times f_2$$

Assuming that at unity-gain

$$(A_{CL1} = 1 \text{ or } 0 \text{ dB})\ fu = f_1 = \text{GBWP},$$

then we have the following:

$$\text{GBWP} = A_{CL2} \times f_2$$

Definition of Terms (Continued)

This says that once fu (GBWP) is known for an amplifier, then the open-loop gain can be found at any frequency. This is also an excellent equation to determine the 3 dB point of a closed-loop gain, assuming that you know the GBWP of the device. Refer to the diagram below.

Bi-amplification: The technique of splitting the audio frequency spectrum into two sections and using individual power amplifiers to drive a separate woofer and tweeter. Crossover frequencies for the amplifiers usually vary between 500 Hz and 1600 Hz. "Biamping" has the advantages of allowing smaller power amps to produce a given sound pressure level and reducing distortion effects produced by overdrive in one part of the frequency spectrum affecting the other part.

C.C.I.R./A.R.M.:

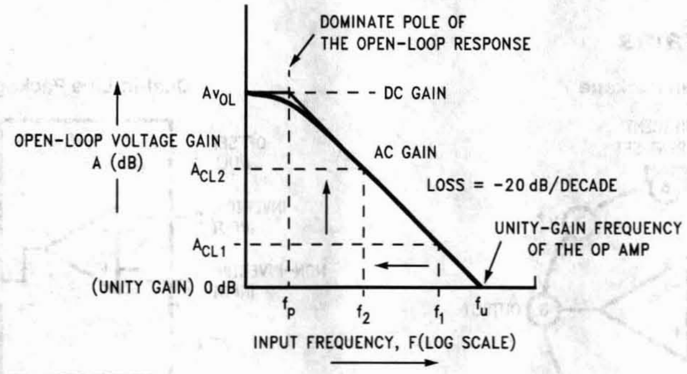
Literally: International Radio Consultative Committee
Average Responding Meter

This refers to a weighted noise measurement for a Dolby B type noise reduction system. A filter characteristic is used that gives a closer correlation of the measurement with the subjective annoyance of noise to the ear. Measurements made with this filter cannot necessarily be related to unweighted noise measurements by some fixed conversion factor since the answers obtained will depend on the spectrum of the noise source.

S.P.L.: Sound Pressure Level—usually measured with a microphone/meter combination calibrated to a pressure level of 0.0002 μBars (approximately the threshold hearing level).

$$\text{S.P.L.} = 20 \text{ Log } 10P/0.0002 \text{ dB}$$

Where P is the R.M.S sound pressure in microbars. (1 Bar = 1 atmosphere = 14.5 lb./in^2 = 194 dB S.P.L.).



TL/H/11449–14

National Semiconductor

LM4250 Programmable Operational Amplifier

General Description

The LM4250 and LM4250C are extremely versatile programmable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product. The device is a truly general purpose operational amplifier.

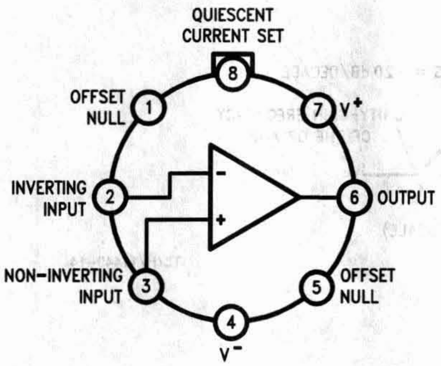
The LM4250C is identical to the LM4250 except that the LM4250C has its performance guaranteed over a 0°C to +70°C temperature range instead of the −55°C to +125°C temperature range of the LM4250.

Features

- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programmable electrical characteristics
- Offset voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

Connection Diagrams

Metal Can Package


QUIESCENT CURRENT SET
8
OFFSET NULL
1
7
V+
INVERTING INPUT
2
−
+
6
OUTPUT
NON-INVERTING INPUT
3
5
OFFSET NULL
4
V−

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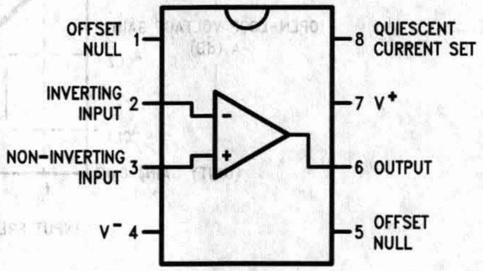
Top View

Dual-In-Line Package


OFFSET NULL 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
V− 4
8 QUIESCENT CURRENT SET
7 V+
6 OUTPUT
5 OFFSET NULL
−
+

TL/H/9300-5

Top View

Ordering Information

Temperature Range		Package	NSC Package Number
Military −55°C ≤ T_A ≤ +125°C	Commercial 0°C ≤ T_A ≤ +70°C		
	LM4250CN	8-Pin Molded DIP	N08E
	LM4250CM	8-Pin Surface Mount	M08A
LM4250J LM4250J-MIL		8-Pin Ceramic DIP	J08E
LM4250H LM4250H-MIL	LM4250CH	8-Pin Metal Can	H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 2)

	LM4250	**LM4250C**
Supply Voltage	±18V	±18V
Operating Temp. Range	−55°C ≤ T_A ≤ +125°C	0°C ≤ T_A ≤ +70°C
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
I_{SET} Current	150 nA	150 nA
Output Short Circuit Duration	Continuous	Continuous
T_{JMAX}		
H-Package	150°C	100°C
N-Package		100°C
J-Package	150°C	100°C
M-Package		100°C
Power Dissipation at T_A = 25°C		
H-Package (Still Air)	500 mW	300 mW
(400 LF/Min Air Flow)	1200 mW	1200 mW
N-Package		500 mW
J-Package	1000 mW	600 mW
M-Package		350 mW
Thermal Resistance (Typical) θ_{JA}		
H-Package (Still Air)	165°C/W	165°C/W
(400 LF/Min Air Flow)	65°C/W	65°C/W
N-Package		130°C/W
J-Package	108°C/W	108°C/W
M-Package		190°C/W
(Typical) θ_{JC}		
H-Package	21°C/W	21°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C

Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 3) 800V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Refer to RETS4250X for military specifications.

Note 3: Human body model, 1.5 kΩ in series with 100 pF.

Resistor Biasing

Set Current Setting Resistor to V⁻

	I_{SET}				
V_S	**0.1 μA**	**0.5 μA**	**1.0 μA**	**5 μA**	**10 μA**
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

Electrical Characteristics LM4250 ($-55°C \le T_A \le +125°C$ unless otherwise specified.) $T_A = T_J$

Parameter	Conditions	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 0.6V$, $R_L = 10\ k\Omega$	40k		50k	
Supply Current	$T_A = 25°C$		7.5 μA		80 μA
Power Consumption	$T_A = 25°C$		23 μW		240 μW
V_{OS}	$R_S \le 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = +125°C$ $T_A = -55°C$		5 nA 3 nA		10 nA 10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	30k		30k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±0.6V		±0.6V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	76 dB		76 dB	
Supply Current			8 μA		90 μA

Parameter	Conditions	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 10\ k\Omega$	100k		100k	
Supply Current	$T_A = 25°C$		10 μA		90 μA
Power Consumption	$T_A = 25°C$		300 μW		2.7 mW
V_{OS}	$R_S \le 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = +125°C$ $T_A = -55°C$		25 nA 3 nA		25 nA 10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	50k		50k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±12V		±12V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	76 dB		76 dB	
Supply Current			11 μA		100 μA
Power Consumption			330 μW		3 mW

Electrical Characteristics LM4250C (0°C ≤ T_A ≤ +70°C unless otherwise specified.) $T_A = T_J$

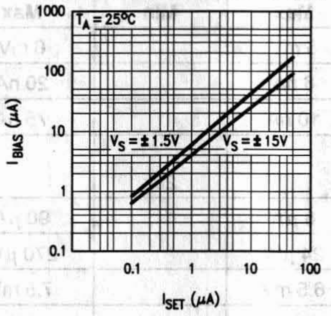
Parameter	Conditions	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 0.6V$, $R_L = 10\ k\Omega$	25k		 25k	
Supply Current	$T_A = 25°C$		8 μA		90 μA
Power Consumption	$T_A = 25°C$		24 μW		270 μW
V_{OS}	$R_S \le 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	25k		 25k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±0.6V		 ±0.6V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	74 dB		74 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

Parameter	Conditions	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 10\ k\Omega$	60k		 60k	
Supply Current	$T_A = 25°C$		11 μA		100 μA
Power Consumption	$T_A = 25°C$		330 μW		3 mW
V_{OS}	$R_S \le 100\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	50k		 50k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±12V		 ±12V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	74 dB		74 dB	
Supply Current			11 μA		100 μA
Power Consumption			330 μW		3 mW

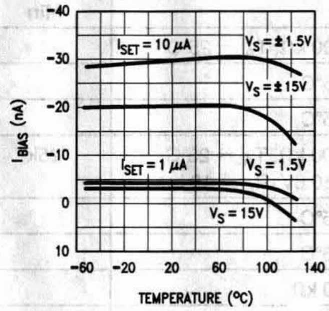
1

Typical Performance Characteristics

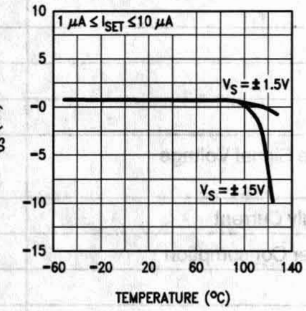
Input Bias Current vs I_{SET}



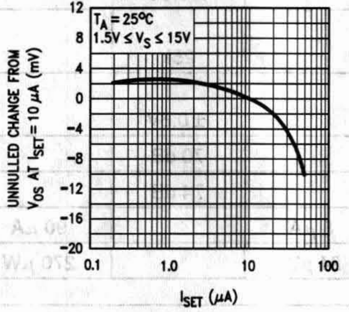
Input Bias Current vs Temperature



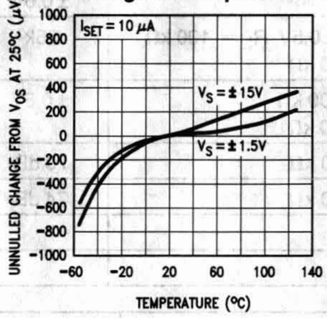
Input Offset Current vs Temperature



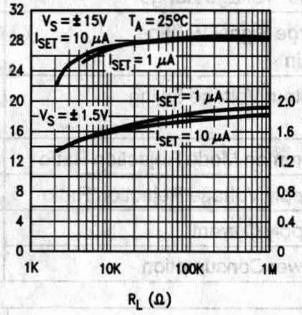
Unnulled Input Offset Voltage Change vs I_{SET}



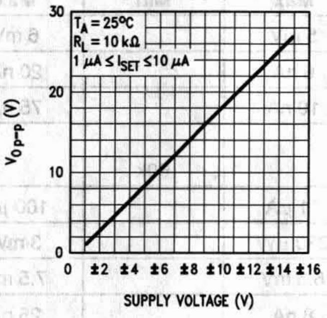
Unnulled Input Offset Voltage Change vs Temperature



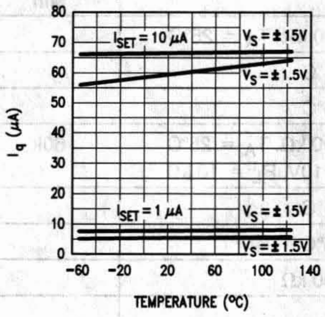
Peak to Peak Output Voltage Swing vs Load Resistance



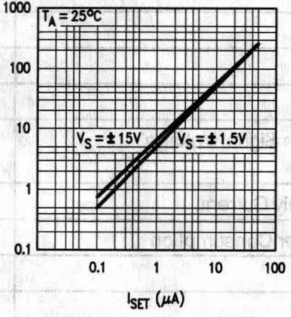
Peak to Peak Output Voltage Swing vs Supply Voltage



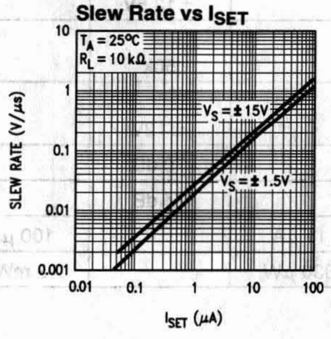
Quiescent Current (I_q) vs Temperature



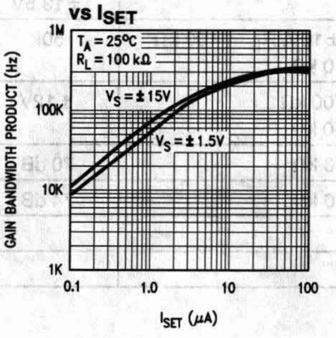
Quiescent Current (I_q) vs I_{SET}



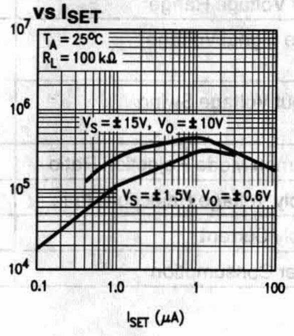
Slew Rate vs I_{SET}



Gain Bandwidth Product vs I_{SET}

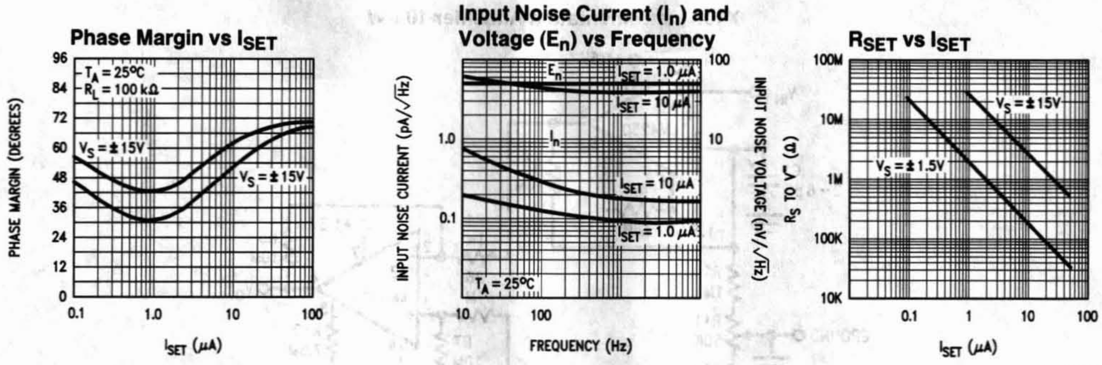


Open Loop Voltage Gain vs I_{SET}



TL/H/9300–6

Typical Performance Characteristics (Continued)


Phase Margin vs I_{SET}

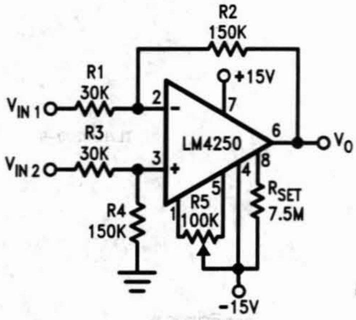
Input Noise Current (I_n) and Voltage (E_n) vs Frequency

R_{SET} vs I_{SET}

TL/H/9300-7

Typical Applications

X5 Difference Amplifier

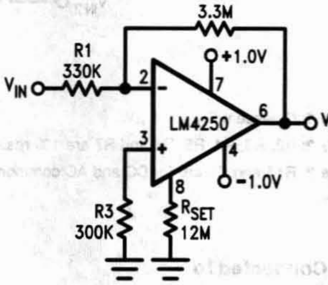


R2
150K
R1
30K
V_IN 1
R3
30K
V_IN 2
+15V
LM4250
2
3
7
6
V_O
4
8
5
1
R5
100K
R_SET
7.5M
R4
150K
−15V

Quiescent P_D = 0.6 mW

TL/H/9300-3

500 Nano-Watt X10 Amplifier

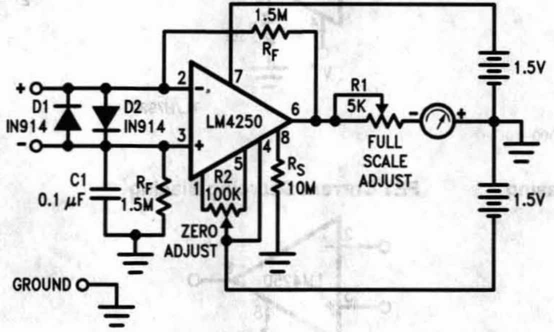


R2
3.3M
R1
330K
V_IN
+1.0V
LM4250
2
3
7
6
V_O
4
−1.0V
8
R3
300K
R_SET
12M

TL/H/9300-4

Quiescent P_D = 500 nW

Floating Input Meter Amplifier 100 nA Full Scale



1.5M
R_F
+
−
D1
IN914
D2
IN914
LM4250
2
3
7
6
1
5
4
8
C1
0.1 μF
R_F
1.5M
R2
100K
ZERO ADJUST
R_S
10M
R1
5K
FULL SCALE ADJUST
1.5V
1.5V
GROUND

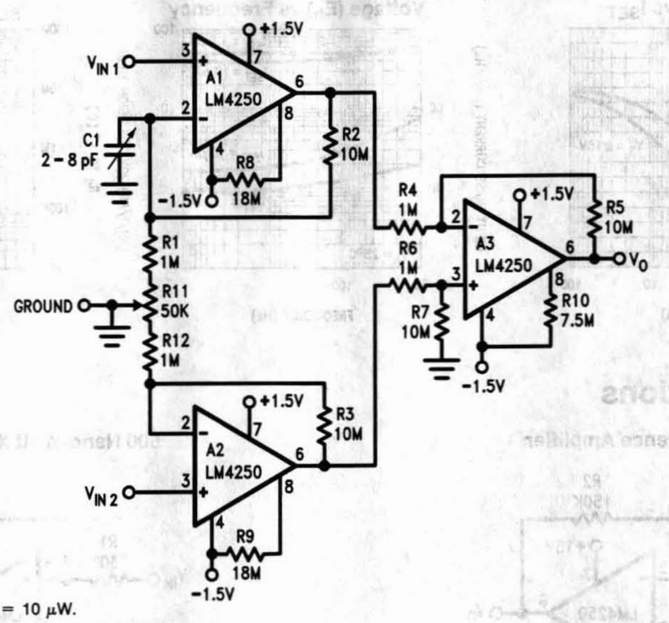
Quiescent P_D = 1.8 μW

*Meter movement (0–100 μA, 2 kΩ) marked for 0–100 nA full scale.

TL/H/9300-8

Typical Applications (Continued)

X100 Instrumentation Amplifier 10 μW


+1.5V
VIN 1
3
7
A1
LM4250
6
2
8
C1
2 – 8 pF
4
R8
18M
−1.5V
R2
10M
R4
1M
+1.5V
R5
10M
2
A3
LM4250
6
VO
R6
1M
3
8
R10
7.5M
R7
10M
4
−1.5V
R1
1M
GROUND
R11
50K
R12
1M
+1.5V
R3
10M
2
7
A2
LM4250
6
VIN 2
3
8
4
R9
18M
−1.5V

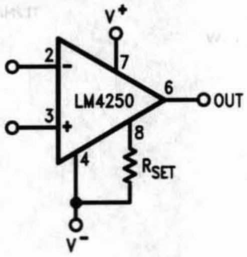
TL/H/9300-9

Note 1: Quiescent P_D = 10 μW.

Note 2: R2, R3, R4, R5, R6 and R7 are 1% resistors.

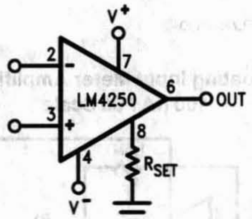
Note 3: R11 and C1 are for DC and AC common mode rejection adjustments.

R_{SET} Connected to V^-


V+
2
7
LM4250
6
OUT
3
8
4
RSET
V−

TL/H/9300-10

R_{SET} Connected to Ground


V+
2
7
LM4250
6
OUT
3
8
4
RSET
V−

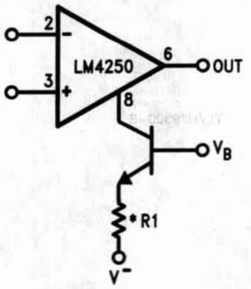
TL/H/9300-11

I_{SET} Equations:

$$I_{SET} \approx \frac{V^+ + |V^-| - 0.5}{R_{SET}} \quad \text{where } R_{SET} \text{ is connected to } V^-.$$

$$I_{SET} \approx \frac{V^+ - 0.5}{R_{SET}} \quad \text{where } R_{SET} \text{ is connected to ground.}$$

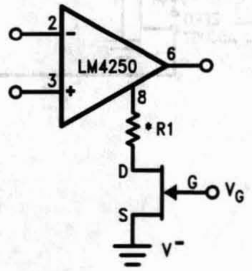
Transistor Current Sourcing Biasing


2
LM4250
6
OUT
3
8
VB
*R1
V−

*R1 limits I_{SET} maximum

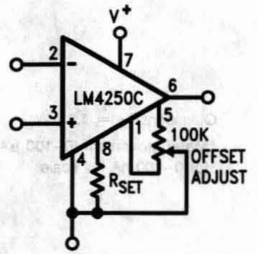
TL/H/9300-12

FET Current Sourcing Biasing


2
LM4250
6
3
8
*R1
D
G
VG
S
V−

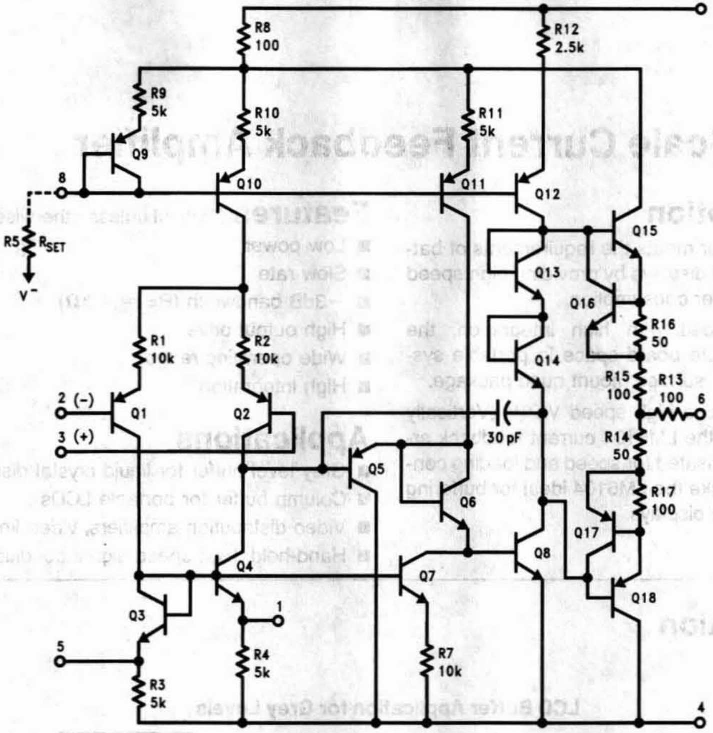
TL/H/9300-13

Offset Null Circuit


V+
2
7
6
LM4250C
3
5
1
100K
OFFSET
ADJUST
4
8
RSET
V−

TL/H/9300-14

Schematic Diagram


7
R8
100
R12
2.5k
R9
5k
R10
5k
R11
5k
8
Q9
Q10
Q11
Q12
Q15
R5
R_{SET}
V⁻
Q13
Q16
R16
50
R1
10k
R2
10k
Q14
R15
100
R13
100
6
2 (−)
Q1
Q2
30 pF
3 (+)
R14
50
Q5
Q6
R17
100
Q17
Q4
Q8
Q7
Q18
Q3
1
5
R4
5k
R7
10k
R3
5k
4

TL/H/9300–1

National Semiconductor

LM6104
Quad Gray Scale Current Feedback Amplifier

General Description

The LM6104 quad amplifier meets the requirements of battery operated liquid crystal displays by providing high speed while maintaining low power consumption.

Combining this high speed with high integration, the LM6104 conserves valuable board space in portable systems with a cost effective, surface mount quad package.

Built on National's advanced high speed VIP™ (Vertically Integrated PNP) process, the LM6104 current feedback architecture is easily compensated for speed and loading conditions. These features make the LM6104 ideal for buffering grey levels in liquid crystal displays.

Features (Typical unless otherwise noted)

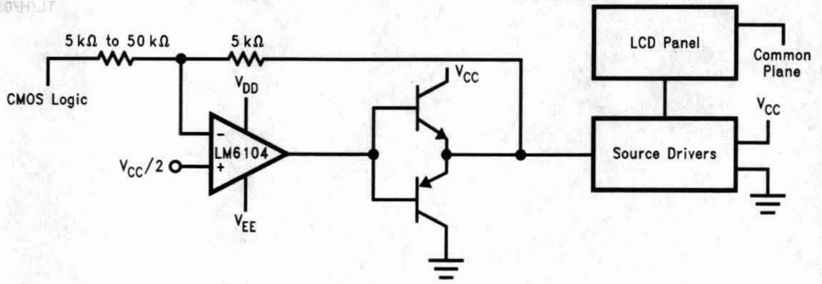
■ Low power	I_S = 875 μA/amplifier
■ Slew rate	100V/μs
■ −3dB bandwidth (R_F = 1 kΩ)	30 MHz
■ High output drive	±5V into 100Ω
■ Wide operating range	V_S = 5V to ±12V
■ High integration	Quad surface mount

Applications

- Grey level buffer for liquid crystal displays
- Column buffer for portable LCDs
- Video distribution amplifiers, video line drivers
- Hand-held, high speed signal conditioning

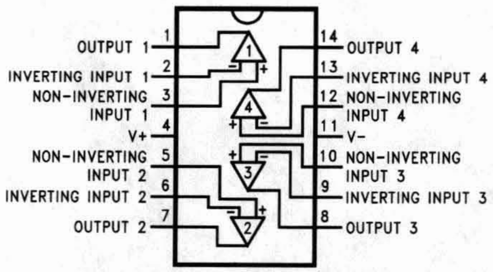
Typical Application

LCD Buffer Application for Grey Levels


5 kΩ to 50 kΩ
5 kΩ
CMOS Logic
VDD
VCC/2
LM6104
VEE
VCC
LCD Panel
Common Plane
VCC
Source Drivers

TL/H/11979-1

Connection Diagram


OUTPUT 1
INVERTING INPUT 1
NON-INVERTING INPUT 1
V+
NON-INVERTING INPUT 2
INVERTING INPUT 2
OUTPUT 2
OUTPUT 4
INVERTING INPUT 4
NON-INVERTING INPUT 4
V-
NON-INVERTING INPUT 3
INVERTING INPUT 3
OUTPUT 3
1
2
3
4
5
6
7
8
9
10
11
12
13
14

TL/H/11979-2

Order Number LM6104M
See NS Package Number M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	24V
Differential Input Voltage	±6V
Input Voltage	±Supply Voltage
Inverting Input Current	15 mA
Soldering Information	
Vapor Phase (60s)	215°C
Infrared (15s)	220°C
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Maximum Junction Temperature	150°C
ESD Rating (Note 2)	2000V

Operating Ratings

Supply Voltage Range	4.75V to 24V
Junction Temperature Range (Note 3)	
LM6104M	$-20° \le T_J \le +80°C$

Electrical Characteristics

The following specifications apply for $V+ = 8V$, $V- = -5V$, $R_L = R_F = 2\ k\Omega$ and $0° \le T_J \le 60°C$ unless otherwise noted.

Symbol	Parameter	Conditions	LM6104M		Units
			Typical (Note 4)	Limits (Note 5)	
V_{OS}	Input Offset Voltage		10	30	mV max
I_B	Inverting Input Bias Current		5.0	20	μA max
	Non-Inverting Input Bias Current		0.5	2	μA max
I_S	Supply Current	$V_O = 0V$	3.5	4.0	mA max
I_{SC}	Output Source Current	$V_O = 0V$ $I_{IN(-)} = -100\ \mu A$	60	45	mA min
	Output Sink Current	$V_O = 0V$ $I_{IN(-)} = 100\ \mu A$	60	45	mA min
V_O	Positive Output Swing	$I_{IN(-)} = -100\ \mu A$	6.5	6.1	V min
	Negative Output Swing	$I_{IN(-)} = 100\ \mu A$	−3.5	−3.1	V max
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4$ to $\pm 10V$	70	60	dB min
		100 mV pp @ 100 kHz	40	30	dB min
R_T	Transresistance		10	5	MΩ min
SR	Slew Rate	(Note 6)	100	55	V/μs min
BW	Bandwidth	$A_V = -1$ $R_{IN} = R_F = 2\ k\Omega$	7.5	5.0	MHz
	Amp-to-Amp Isolation	$R_L = 2\ k\Omega$ $F = 1\ MHz$	60		dB
CMVR	Common Mode Voltage Range		$V^+ - 1.4V$ $V^- + 1.4V$		V
CMRR	Common Mode Rejection Ratio		60		dB
t_S	Settling Time	0.05%, 5V Step, $A_V = -1$ $R_F = R_S = 2\ k\Omega$, $V_S = \pm 5V$	240		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under the conditions.

Note 2: Human body model 1.5 kΩ and 100 pF. This is a class 2 device rating.

Note 3: Thermal resistance of the SO package is 98°C/W. When operating at $T_A = 80°C$, maximum power dissipation is 700 mW.

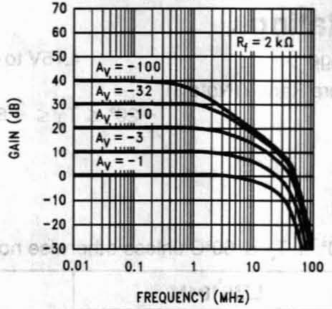
Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits guaranteed at operating temperature extremes.

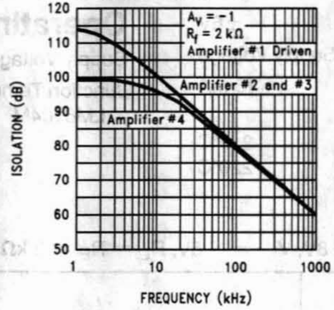
Note 6: $A_V = -1$ with $R_{IN} = R_F = 2\ k\Omega$. Slew rate is calculated from the 25% to the 75% point on both rising and falling edges. Output swing is −0.6V to +5.6V and 5.6V to 0.6V.

Typical Performance Characteristics

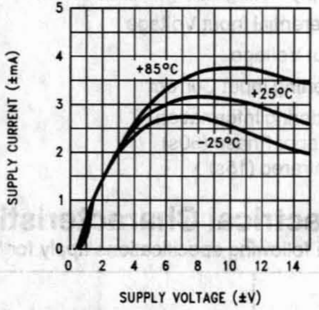
Frequency Response vs Closed Loop Gain



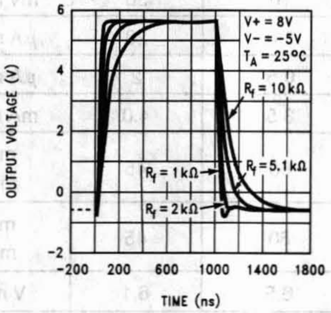
Amplifier to Amplifier Isolation



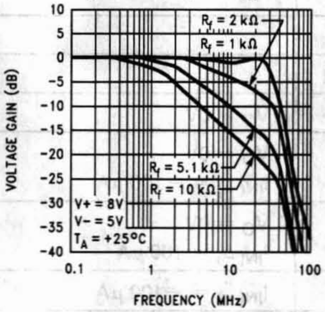
Supply Current vs Supply Voltage



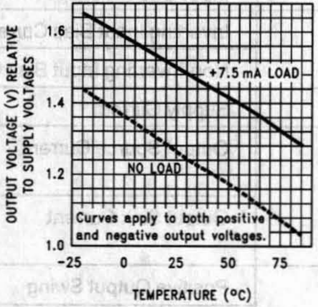
Large Signal Pulse Response
$A_V = -1$



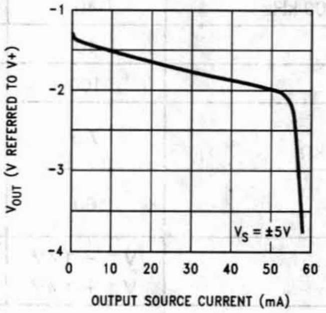
Frequency Response vs R_F
$A_V = -1, R_F = R_G$



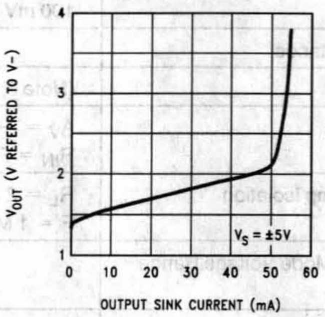
V_{OUT} Referred to Supplies
$V_S = \pm 5V$
$I_{IN} = \pm 100\ \mu A$



LM6104 Output Voltage vs Source Current



LM6104 Output Voltage vs Sink Current



TL/H/11979-3

Applications Information

CURRENT FEEDBACK TOPOLOGY

The small-signal bandwidth of conventional voltage feedback amplifiers is inversely proportional to the closed-loop gain based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6104, enables a signal bandwidth that is relatively independent of the amplifier's gain (see typical curve Frequency Response vs Closed Loop Gain).

FEEDBACK RESISTOR SELECTION: R_F

Current feedback amplifier bandwidth and slew rate are controlled by R_F. R_F and the amplifier's internal compensation capacitor set the dominant pole in the frequency response. The amplifier, therefore, always requires a feedback resistor, even in unity gain.

Bandwidth and slew rate are inversely proportional to the value of R_F (see typical curve Frequency Response vs R_F). This makes the amplifier especially easy to compensate for a desired pulse response (see typical curve Large Signal Pulse Response). Increased capacitive load driving capability is also achieved by increasing the value of R_F.

The LM6104 has guaranteed performance with a feedback resistor of 2 kΩ.

CAPACITIVE FEEDBACK

It is common to place a small lead capacitor in parallel with feedback resistance to compensate voltage feedback amplifiers. Do not place a capacitor across R_F to limit the bandwidth of current feedback amplifiers. The dynamic impedance of capacitors in the feedback path of the LM6104, as with any current feedback amplifier, will cause instability.

National Semiconductor

LM6118/LM6218
Fast Settling Dual Operational Amplifiers

General Description

The LM6118 series are monolithic fast-settling unity-gain-compensated dual operational amplifiers with ±20 mA output drive capability. The PNP input stage has a typical bias current of 200 nA, and the operating supply voltage is ±5V to ±20V.

These dual op amps use slew enhancement with special mirror circuitry to achieve fast response and high gain with low total supply current.

The amplifiers are built on a junction-isolated VIP™ (Vertically Integrated PNP) process which produces fast PNP's that complement the standard NPN's.

Features

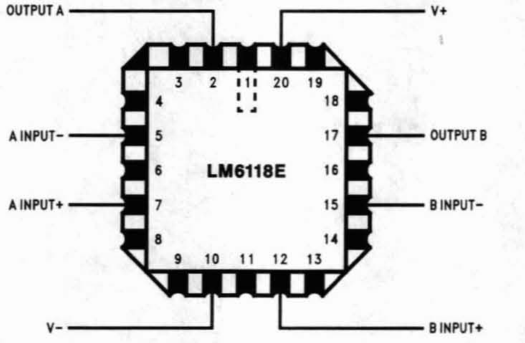
	Typical
■ Low offset voltage	0.2 mV
■ 0.01% settling time	400 ns
■ Slew rate $A_V = -1$	140 V/µs
■ Slew rate $A_V = +1$	75 V/µs
■ Gain bandwidth	17 MHz
■ Total supply current	5.5 mA
■ Output drives 50Ω load (±1V)	

Applications

- D/A converters
- Fast integrators
- Active filters

Connection Diagrams and Order Information

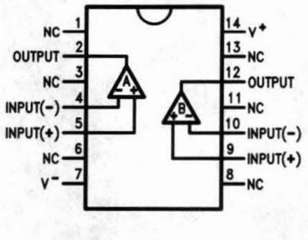
Ceramic Leadless Chip Carrier (E)


OUTPUT A
V+
3
2
1
20
19
4
18
A INPUT−
5
17
OUTPUT B
6
LM6118E
16
A INPUT+
7
15
B INPUT−
8
14
9
10
11
12
13
V−
B INPUT+

TL/H/10254–24

Order Number LM6118E/883*
See NS Package Number E20A

Small Outline Package (WM)

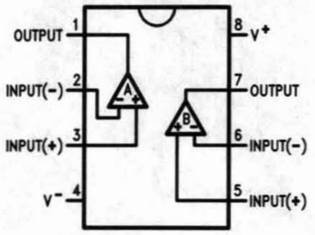

NC
1
OUTPUT
2
NC
3
INPUT(−)
4
INPUT(+)
5
NC
6
V⁻
7
A
B
14
V⁺
13
NC
12
OUTPUT
11
NC
10
INPUT(−)
9
INPUT(+)
8
NC

TL/H/10254–3

Top View

Order Number LM6218AWM or LM6218WM
See NS Package Number M14B

Dual-In-Line Package (J or N)

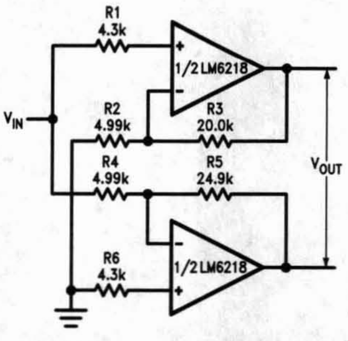

OUTPUT
1
INPUT(−)
2
INPUT(+)
3
V⁻
4
A
B
8
V⁺
7
OUTPUT
6
INPUT(−)
5
INPUT(+)

TL/H/10254–4

Top View

Order Number LM6118N, LM6118J/883*,
LM6218AN or LM6218N
See NS Package Number J08A or N08E

Typical Applications


R1
4.3k
1/2 LM6218
V_{IN}
R2
4.99k
R3
20.0k
R4
4.99k
R5
24.9k
V_{OUT}
R6
4.3k
1/2 LM6218

TL/H/10254–1

Single ended input to differential output
$A_V = 10$, BW = 3.2 MHz
40 V_{PP} Response = 1.4 MHz
$V_S = \pm 15V$

Wide-Band, Fast-Settling
40 V_{PP} Amplifier

*Available per SMD #5962-9156501

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	42V
Input Voltage	(Note 2)
Differential Input Current (Note 3)	±10 mA
Output Current (Note 4)	Internally Limited
Power Dissipation (Note 5)	500 mW
ESD Tolerance (C = 100 pF, R = 1.5 kΩ)	±2 kV
Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Temp. Range

LM6118	−55°C to +125°C
LM6218A	−40°C to +85°C
LM6218	−40°C to +85°C

Electrical Characteristics

$\pm 5V \le V_S \le \pm 20V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $I_{OUT} = 0A$, unless otherwise specified. Limits with standard type face are for $T_J = 25°C$, and **Bold Face Type** are for **Temperature Extremes.**

Parameter	Conditions	Typ 25°C	LM6118 Limits (Notes 6 & 7)	LM6218A Limits (Note 6)	LM6218 Limits (Note 6)	Units
Input Offset Voltage	$V_S = \pm 15V$	0.2	1 **2**	1 **2**	3 **4**	mV (max)
Input Offset Voltage	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	0.3	1.5 **2.5**	1.5 **2.5**	3.5 **4.5**	mV (max)
Input Offset Current	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	20	50 **250**	50 **100**	100 **200**	nA (max)
Input Bias Current	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	200	350 **950**	350 **950**	500 **1250**	nA (max)
Input Common Mode Rejection Ratio	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$ $V_S = \pm 20V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Positive Power Supply Rejection Ratio	$V^- = -15V$ $5V \le V^+ \le 20V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Negative Power Supply Rejection Ratio	$V^+ = 15V$ $-20V \le V^- \le -5V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Large Signal Voltage Gain	$V_{out} = \pm 15V$ $R_L = 10k$ $V_S = \pm 20V$	500	150 **100**	150 **100**	100 **70**	V/mV (min)
	$V_{out} = \pm 10V$ $R_L = 500$ $V_S = \pm 15V$ $(\pm 20$ mA)	200	50 **30**	50 **30**	40 **25**	V/mV (min)
V_O Output Voltage Swing	Supply = $\pm 20V$ $R_L = 10k$	17.3	±17	±17	±17	V (min)
Total Supply Current	$V_S = \pm 15V$	5.5	7 **7.5**	7 **7.5**	7 **7.5**	mA (max)
Output Current Limit	$V_S = \pm 15V$, Pulsed	65	100	100	100	mA (max)
Slew Rate, Av = −1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	140	100 **50**	100 **50**	100 **50**	V/μs (min)
Slew Rate, Av = +1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	75	50 **30**	50 **30**	50 **30**	V/μs (min)
Gain-Bandwidth Product	$V_S = \pm 15V$, $f_o = 200$ kHz	17	14	14	13	MHz (min)
0.01% Settling Time $A_V = -1$	$\Delta V_{out} = 10V$, $V_S = \pm 15V$, $R_S = R_f = 2k$, $C_f = 10$ pF	400				ns
Input Capacitance	Inverter	5				pF
	Follower	3				pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage range is $(V^+ - 1V)$ to (V^-).

Note 3: The inputs are shunted with three series-connected diodes back-to-back for input differential clamping. Therefore differential input voltages greater than about 1.8V will cause excessive current to flow unless limited to less than 10 mA.

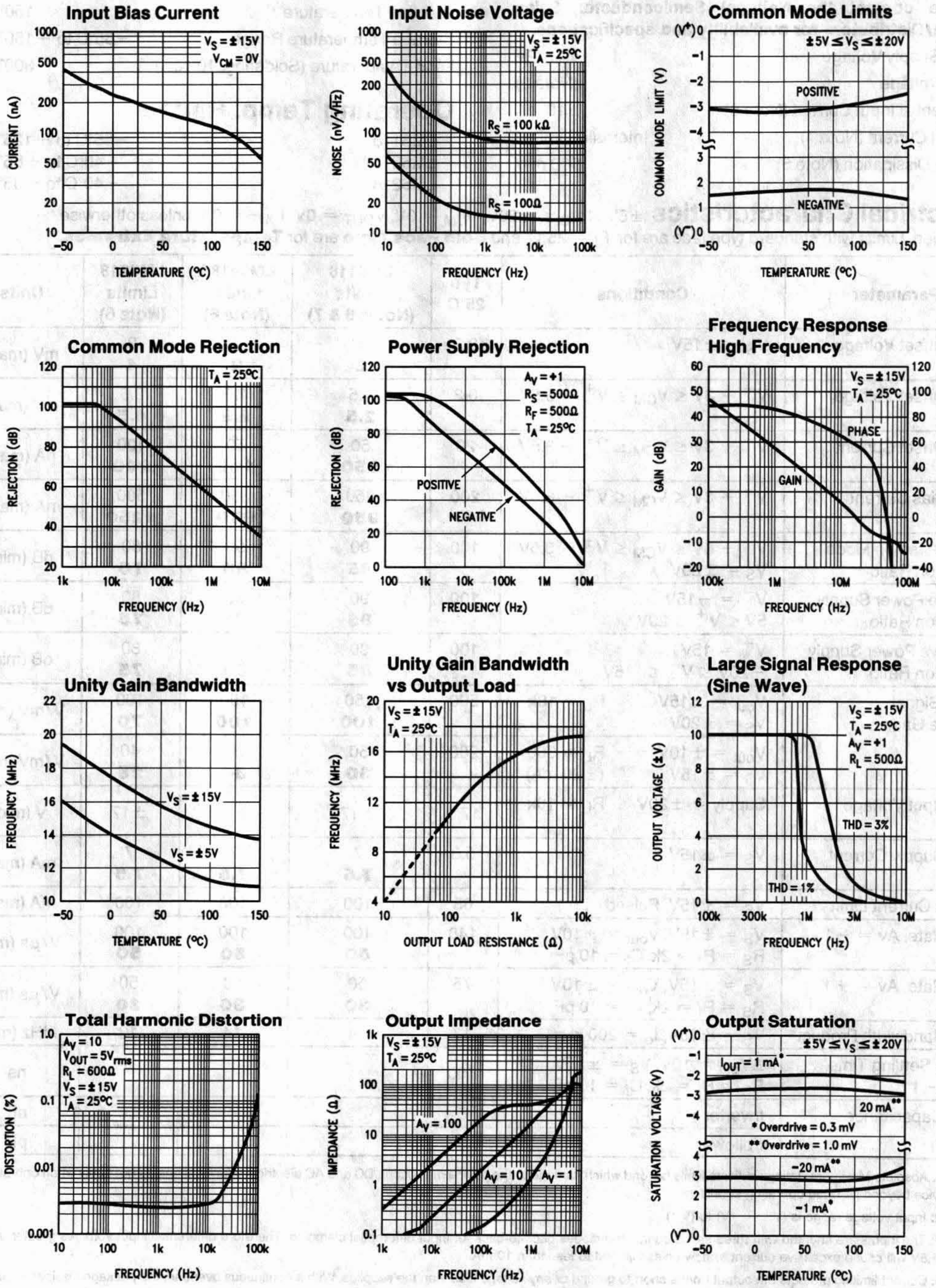
Note 4: Current limiting protects the output from a short to ground or any voltage less than the supplies. With a continuous overload, the package dissipation must be taken into account and heat sinking provided when necessary.

Note 5: Devices must be derated using a thermal resistance of 90°C/W for the N, J and WM packages.

Note 6: Limits are guaranteed by testing or correlation.

Note 7: A military RETS specification is available on request. At the time of printing, LM6118J/883 and LM6118E/883 RETS spec complied with the **Boldface** limits in this column.

Typical Performance Characteristics


Input Bias Current

Input Noise Voltage

Common Mode Limits

Common Mode Rejection

Power Supply Rejection

Frequency Response High Frequency

Unity Gain Bandwidth

Unity Gain Bandwidth vs Output Load

Large Signal Response (Sine Wave)

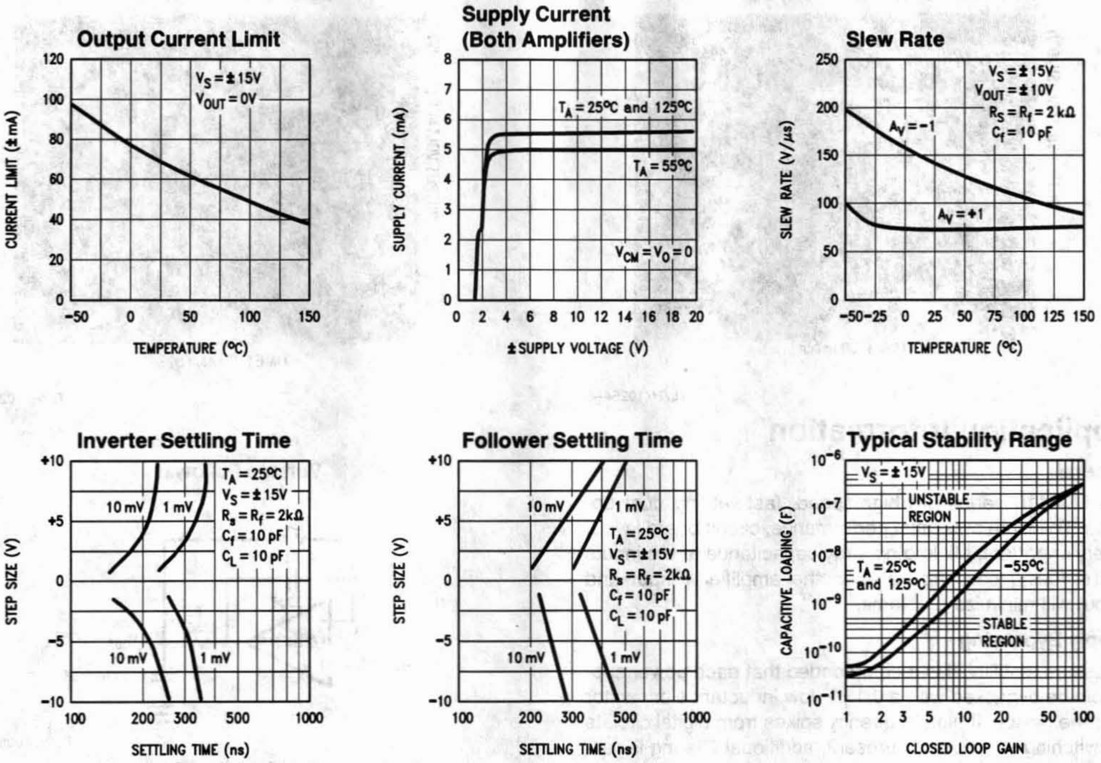
Total Harmonic Distortion

Output Impedance

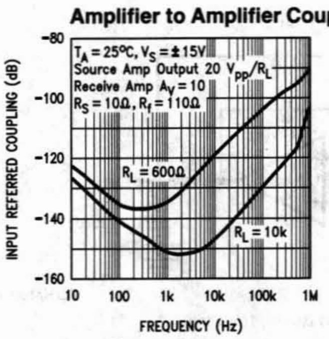
Output Saturation

TL/H/10254–5

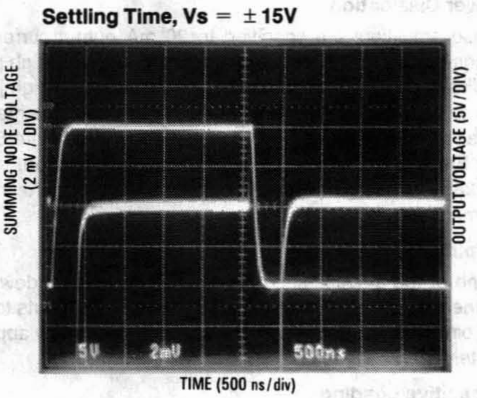
Typical Performance Characteristics (Continued)



TL/H/10254-6



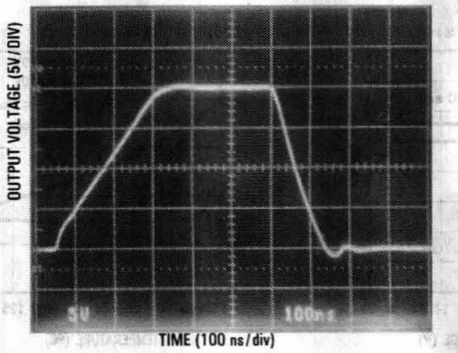
TL/H/10254-23



TL/H/10254-7

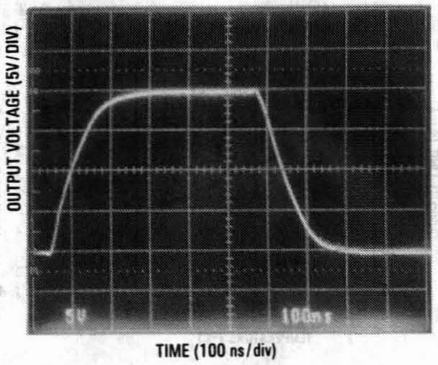
Typical Performance Characteristics (Continued)

Step Response, Av = +1, Vs = ±15V



TL/H/10254–8

Step Response, Av = −1, Vs = ±15V



TL/H/10254–9

Application Information

General

The LM6118 series are high-speed, fast-settling dual op-amps. To insure maximum performance, circuit board layout is very important. Minimizing stray capacitance at the inputs and reducing coupling between the amplifier's input and output will minimize problems.

Supply Bypassing

To assure stability, it is recommended that each power supply pin be bypassed with a 0.1 μF low inductance capacitor near the device. If high frequency spikes from digital circuits or switching supplies are present, additional filtering is recommended. To prevent these spikes from appearing at the output, R-C filtering of the supplies near the device may be necessary.

Power Dissipation

These amplifiers are specified to 20 mA output current. If accompanied with high supply voltages, relatively high power dissipation in the device will occur, resulting in high junction temperatures. In these cases the package thermal resistance must be taken into consideration. (See Note 5 under Electrical Characteristics.) For high dissipation, an N package with large areas of copper on the pc board is recommended.

Amplifier Shut Down

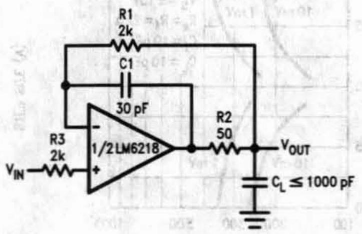
If one of the amplifiers is not used, it can be shut down by connecting both the inverting and non-inverting inputs to the V^- pin. This will reduce the power supply current by approximately 25%.

Capacitive Loading

Maximum capacitive loading is about 50 pF for a closed-loop gain of +1, before the amplifier exhibits excessive ringing and becomes unstable. A curve showing maximum capacitive loads, with different closed-loop gains, is shown in the Typical Performance Characteristics section.

To drive larger capacitive loads at low closed-loop gains, isolate the amplifier output from the capacitive load with 50Ω. Connect a small capacitor directly from the amplifier output to the inverting input. The feedback loop is closed from the isolated output with a series resistor to the inverting input.

Voltage Follower

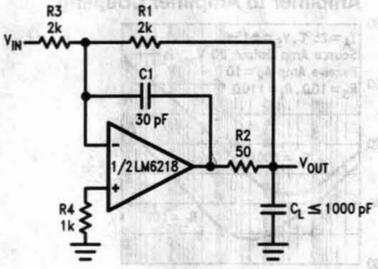


TL/H/10254–10

For C_L = 1000 pF, Small signal BW = 5 MHz

20 $V_{p\text{-}p}$ BW = 500 kHz

Inverter



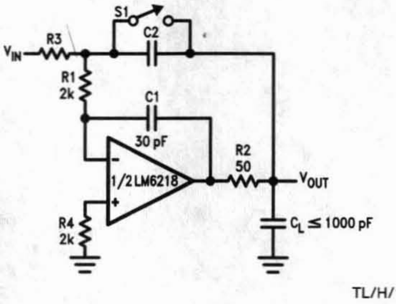
TL/H/10254–11

Settling time to 0.01%, 10V Step

For C_L = 1000 pF, settling time ≈ 1500 ns

For C_L = 300 pF, settling time ≈ 500 ns

Integrator



TL/H/10254–12

Application Information (Continued)

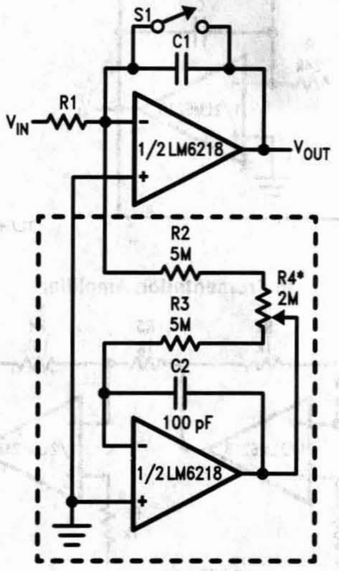
Examples of unity gain connections for a voltage follower, Inverter, and integrator driving capacitive loads up to 1000 pF are shown here. Different R1–C1 time constants and capacitive loads will have an effect on settling times.

Input Bias Current Compensation

Input bias current of the first op amp can be reduced or balanced out by the second op amp. Both amplifiers are laid out in mirror image fashion and in close proximity to each other, thus both input bias currents will be nearly identical and will track with temperature. With both op amp inputs at the same potential, a second op amp can be used to convert bias current to voltage, and then back to current feeding the first op amp using large value resistors to reduce the bias current to the level of the offset current.

Examples are shown here for an inverting application, (a) where the inputs are at ground potential, and a second circuit (b) for compensating bias currents for both inputs.

Bias Current Compensation

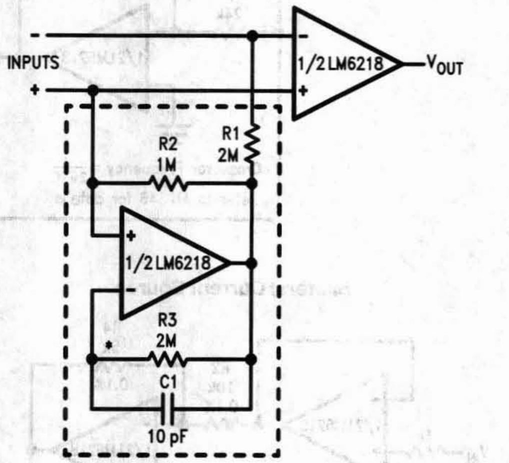


S1
C1
R1
V_{IN}
1/2 LM6218
V_{OUT}
R2
5M
R4*
2M
R3
5M
C2
100 pF
1/2 LM6218

*adjust for zero integrator drift

TL/H/10254–13

(a) Inverting Input Bias Compensation for Integrator Application



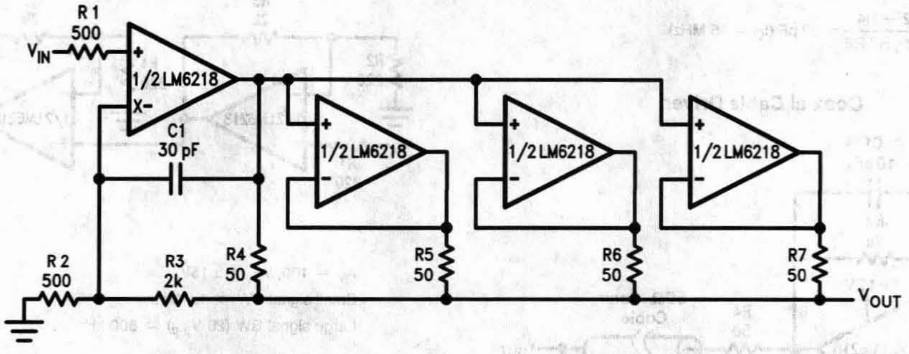
INPUTS
−
+
1/2 LM6218
V_{OUT}
R2
1M
R1
2M
1/2 LM6218
R3
2M
C1
10 pF

TL/H/10254–14

*mount resistor close to input pin to minimize stray capacitance

(b) Compensation to Both Inputs

Amplifier/Parallel Buffer



R1
500
V_{IN}
1/2 LM6218
X−
C1
30 pF
1/2 LM6218
1/2 LM6218
1/2 LM6218
R2
500
R3
2k
R4
50
R5
50
R6
50
R7
50
V_{OUT}

TL/H/10254–15

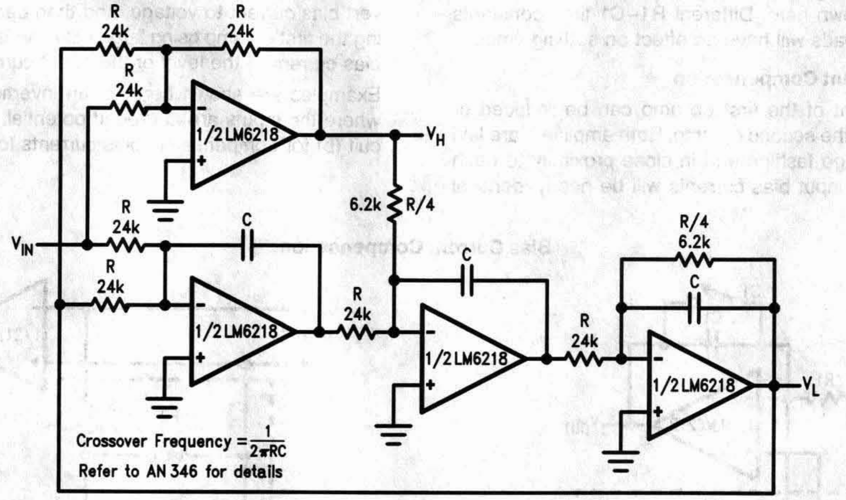
$A_V = +5$, $I_{OUT} \leq 80$ mA

$V_S = \pm 15V$, $C_L \leq 0.01\ \mu F$

Large and small signal B.W. = 1.3 MHz (THD = 3%)

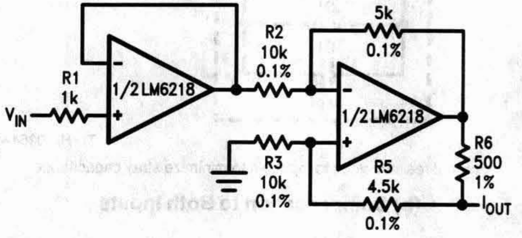
Application Information (Continued)

Constant-Voltage Crossover Network With 12 dB/Octave Slope


R
24k
R
24k
R
24k
1/2 LM6218
V_H
6.2k
R/4
V_IN
R
24k
C
R
24k
1/2 LM6218
R
24k
C
1/2 LM6218
R/4
6.2k
C
R
24k
1/2 LM6218
V_L
Crossover Frequency = 1/2πRC
Refer to AN 346 for details

TL/H/10254-16

Bilateral Current Source


R1
1k
V_IN
1/2 LM6218
R2
10k
0.1%
R4
5k
0.1%
1/2 LM6218
R3
10k
0.1%
R5
4.5k
0.1%
R6
500
1%
I_OUT

TL/H/10254-17

$V_S = \pm 15V, -10 \le V_{IN} \le 10V$

$\frac{I_{OUT}}{V_{IN}} = \frac{R4}{R2\,R6} = \frac{1\ mA}{1V}$

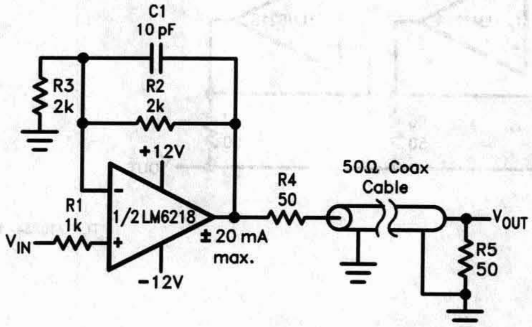
Output dynamic range $= 10V - R6\,|I_{OUT}|$

$R_L = 500\Omega$, small signal BW = 6 MHz

Large signal response = 800 kHz

C_{out} equiv. $= \frac{R2 + R4}{2\pi\, f_O\, R2\, R6} = 32\ pF\ (f_O = 15\ MHz)$

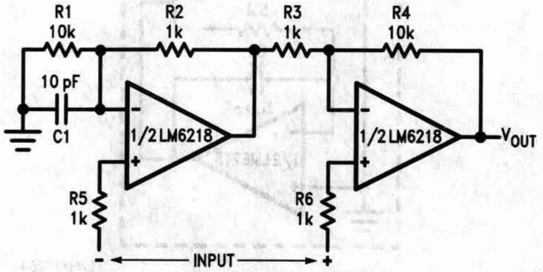
Coaxial Cable Driver


C1
10 pF
R3
2k
R2
2k
+12V
R1
1k
V_IN
1/2 LM6218
−12V
R4
50
± 20 mA
max.
50Ω Coax
Cable
V_OUT
R5
50

TL/H/10254-19

Small signal (200 mV_{p-p}) BW ≈ 5 MHz

Instrumentation Amplifier

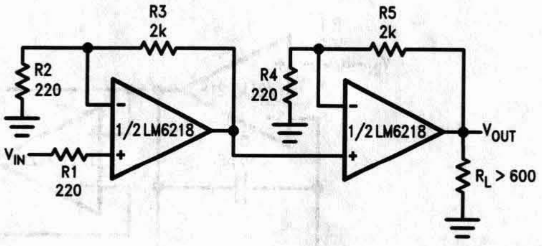

R1
10k
R2
1k
R3
1k
R4
10k
10 pF
C1
1/2 LM6218
1/2 LM6218
V_OUT
R5
1k
R6
1k
− INPUT +

TL/H/10254-18

$A_V = 10$, $V_S = \pm 15V$, All resistors 0.01%

Small signal and large signal (20 V_{P-P}) B.W. ≈ 800 kHz

150 MHz Gain-Bandwidth Amplifier


R3
2k
R5
2k
R2
220
R4
220
1/2 LM6218
1/2 LM6218
V_IN
R1
220
V_OUT
R_L > 600

TL/H/10254-20

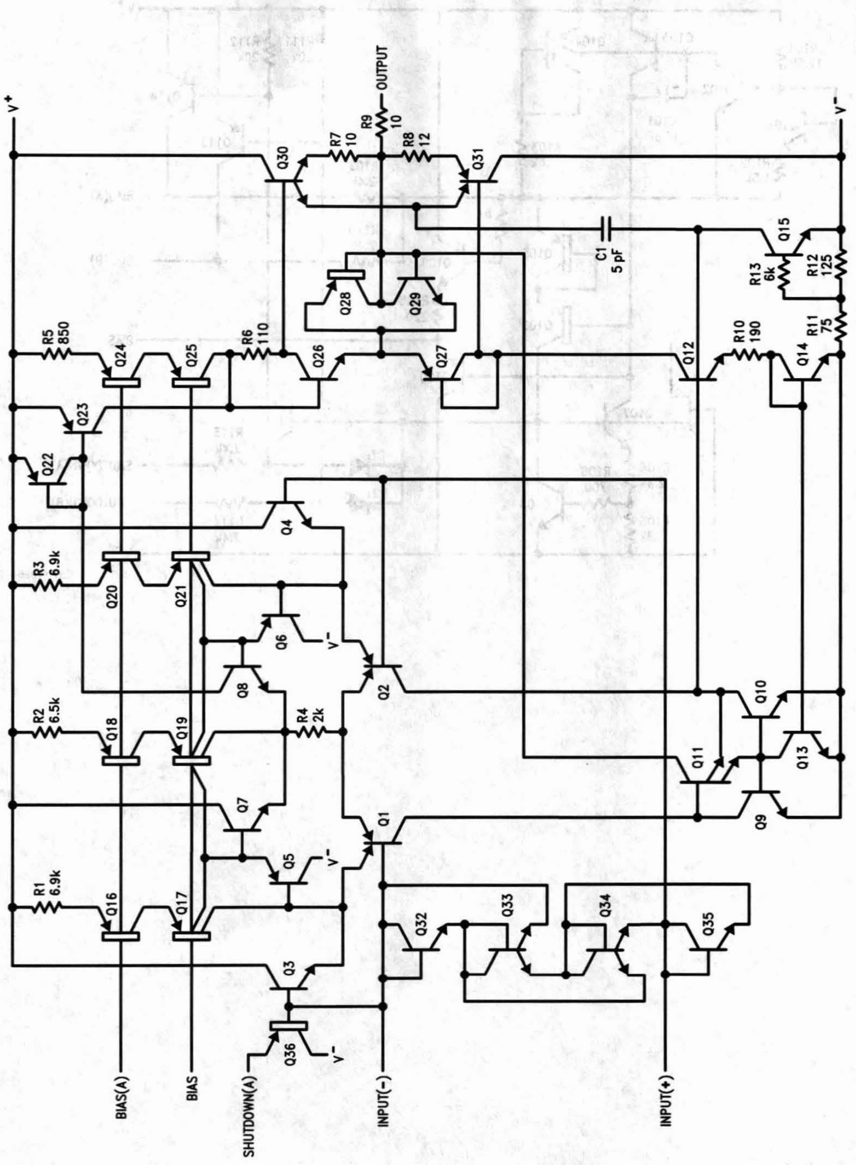
$A_V = 100$, $V_S = \pm 15V$,

Small signal BW ≈ 1.5 MHz

Large signal BW (20 V_{p-p}) ≈ 800 kHz

Schematic Diagram

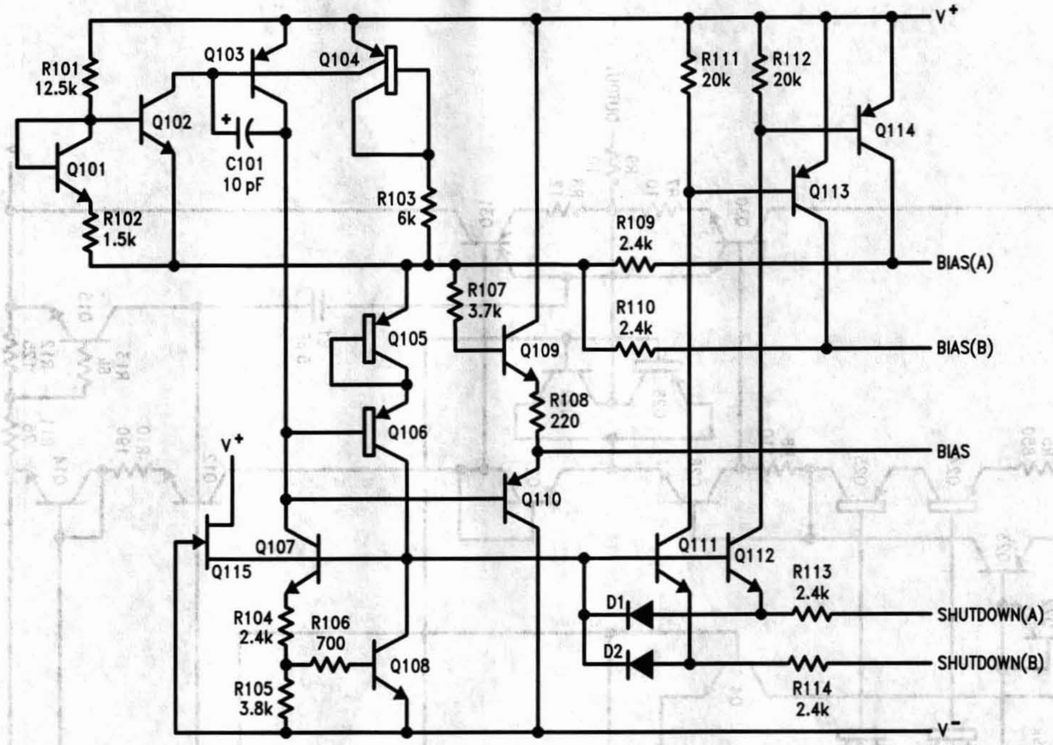
½ LM6118 (Op Amp A)


V+
V−
OUTPUT
R9
10
R7
10
R8
12
Q30
Q31
C1
5 pF
Q15
R13
6k
R12
125
R11
75
R10
190
Q14
Q12
R5
850
Q24
Q25
R6
110
Q26
Q27
Q28
Q29
Q23
Q22
Q4
R3
6.9k
Q20
Q21
Q6
Q8
Q2
Q10
Q11
Q13
R2
6.5k
Q18
Q19
R4
2k
Q7
Q1
Q9
R1
6.9k
Q16
Q17
Q5
Q3
Q36
Q32
Q33
Q34
Q35
BIAS(A)
BIAS
SHUTDOWN(A)
INPUT(−)
INPUT(+)

TL/H/10254–21

Schematic Diagram (Continued)

Bias Circuit


V+
R101
12.5k
Q103
Q104
Q102
Q101
C101
10 pF
R102
1.5k
R103
6k
R111
20k
R112
20k
Q114
Q113
R109
2.4k
BIAS(A)
R107
3.7k
Q105
Q109
R110
2.4k
BIAS(B)
R108
220
Q106
BIAS
V+
Q110
Q107
Q115
Q111
Q112
R113
2.4k
D1
SHUTDOWN(A)
R104
2.4k
R106
700
Q108
D2
SHUTDOWN(B)
R105
3.8k
R114
2.4k
V−

TL/H/10254–22

National Semiconductor

ADVANCE INFORMATION

LM6132 Dual and LM6134 Quad High Speed/Low Power 7 MHz Rail-to-Rail I/O Operational Amplifiers

General Description

Using patent pending circuit topologies, the LM6132/34 provides new levels of speed vs. power performance in applications where low voltage supplies or power limitations previously made compromise necessary. With only 550 μA/amp supply current, the 7 MHz bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

In addition, the LM6132/34 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages. The LM6132/34 can also drive large capacitive loads without oscillating.

Operating on supplies of 1.8 to over 24 volts, the LM6132/34 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

Features (For 5V Supply)

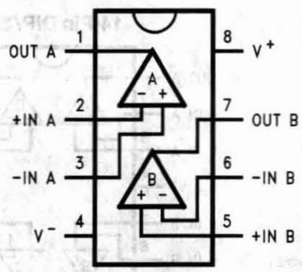
■ Rail-to-rail input CMVR	−0.25V to 5.25V (Max/Min)
■ Rail-to-rail output swing	0.01V to 4.99V (Max/Min)
■ Wide gain-bandwidth at 50 KHz	7 MHz (Typ)
■ Slew rate	12 V/μs (Typ)
■ Low supply current	550 μA/amp (Typ)
■ Wide supply range	1.8V to 24V
■ CMRR	107 dB (Typ)
■ Gain	108 dB (Typ) with R_L = 10K
■ PSRR	87 dB (Typ)

Applications

- Battery operated instrumentation
- 5V instrumentation
- Portable scanners
- Wireless communications

Connection Diagrams

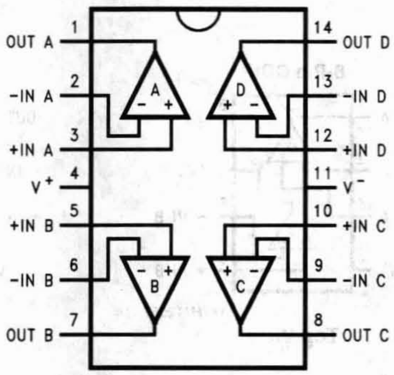
8-Pin DIP/SO



Top View

TL/H/12349-1

14-Pin DIP/SO



TL/H/12349-2

Top View

Ordering Information

Package	Temperature Range	NSC
	Industrial −40°C to +85°C	Drawing
8-Pin Molded DIP	LM6132AIN, LM6132BIN	N08E
8-Pin Small Outline	LM6132AIM, LM6132BIM	M08A
14-Pin Molded DIP	LM6134AIN, LM6134BIN	N14A
14-Pin Small Outline	LM6134AIM, LM6134BIM	M14A

National Semiconductor

LM6142 Dual and LM6144 Quad High Speed/Low Power 17 MHz Rail-to-Rail Input-Output Operational Amplifiers

General Description

Using patent pending new circuit topologies, the LM6142/44 provides new levels of performance in applications where low voltage supplies or power limitations previously made compromise necessary. Operating on supplies of 1.8V to over 24V, the LM6142/44 is an excellent choice for battery operated systems, portable instrumentation and others.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

High gain-bandwidth with 650 μA/Amplifier supply current opens new battery powered applications where previous higher power consumption reduced battery life to unacceptable levels. The ability to drive large capacitive loads without oscillating functionally removes this common problem.

Features At V_S = 5V. Typ unless noted.

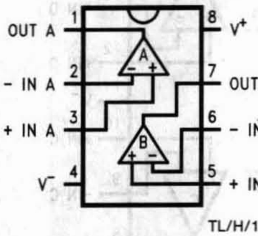
- Rail-to-rail input CMVR −0.25V to 5.25V
- Rail-to-rail output swing 0.005V to 4.995V
- Wide gain-bandwidth: 17 MHz at 50 kHz (typ)
- Slew rate:
  - Small signal, 5V/μs
  - Large signal, 30V/μs
- Low supply current 650 μA/Amplifier
- Wide supply range 1.8V to 24V
- CMRR 107 dB
- Gain 108 dB with R_L = 10k
- PSRR 87 dB

Applications

- Battery operated instrumentation
- Depth sounders/fish finders
- Barcode scanners
- Wireless communications
- Rail-to-rail in-out instrumentation amps

Connection Diagrams

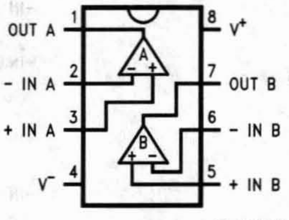
8-Pin CDIP



TL/H/12057-14

Top View

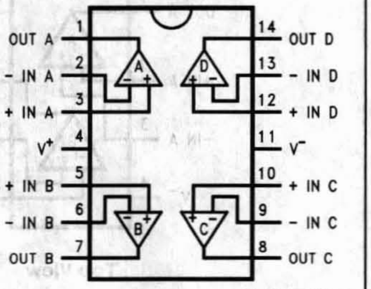
8-Pin DIP/SO



TL/H/12057-1

Top View

14-Pin DIP/SO



TL/H/12057-2

Top View

Ordering Information

Package	Temperature Range Industrial −40°C to +85°C	Temperature Range Military −55°C to +125°C	NSC Drawing
8-Pin Molded DIP	LM6142AIN, LM6142BIN		N08E
8-Pin Small Outline	LM6142AIM, LM6142BIM		M08A
14-Pin Molded DIP	LM6144AIN, LM6144BIN		N14A
14-Pin Small Outline	LM6144AIM, LM6144BIM		M14A
8-Pin CDIP		LM6142AMJ/883	D08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2500V
Differential Input Voltage	15V
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage $(V^+ - V^-)$	35V
Current at Input Pin	±10 mA
Current at Output Pin (Note 3)	±25 mA
Current at Power Supply Pin	50 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$1.8V \leq V^+ \leq 24V$
Junction Temperature Range	
LM6142, LM6144	$-40°C \leq T_J \leq +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
N Package, 14-Pin Molded DIP	81°C/W
M Package, 14-Pin Surface Mount	126°C/W

5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5.0V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to $V+/2$. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.3	1.0 **2.2**	2.5 **3.3**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**3**			μV/°C
I_B	Input Bias Current		170	250	300	nA max
		$0V \leq V_{CM} \leq 5V$	180	280 **526**	**526**	
I_{OS}	Input Offset Current		3	30 **80**	30 **80**	nA max
R_{IN}	Input Resistance, C_M		126			MΩ
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 4V$	107	84 **78**	84 **78**	dB min
		$0V \leq V_{CM} \leq 5V$	82 **79**	66 **64**	66 **64**	
PSRR	Power Supply Rejection Ratio	$5V \leq V^+ \leq 24V$	**87**	80 **78**	80 **78**	
V_{CM}	Input Common-Mode Voltage Range		−0.25	**0**	**0**	V
			5.25	**5.0**	**5.0**	
A_V	Large Signal Voltage Gain	$R_L = 10k$	270 **70**	100 **33**	80 **25**	V/mV min
V_O	Output Swing	$R_L = 100k$	0.005	0.01 **0.013**	0.01 **0.013**	V max
			4.995	4.98 **4.93**	4.98 **4.93**	V min
		$R_L = 10k$	0.02			V max
			4.97			V min
		$R_L = 2k$	0.06	0.1 **0.133**	0.1 **0.133**	V max
			4.90	4.86 **4.80**	4.86 **4.80**	V min

5.0V DC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for $T_J = 25°C$, $V^+ = 5.0V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to $V^+/2$. **Boldface limits** apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
I_{SC}	Output Short Circuit Current LM6142	Sourcing	13	10 **4.9**	8 **4**	mA min
				35	**35**	mA max
		Sinking	24	10 **5.3**	10 **5.3**	mA min
				35	**35**	mA max
I_{SC}	Output Short Circuit Current LM6144	Sourcing	8	6 **3**	6 **3**	mA min
				35	**35**	mA max
		Sinking	22	8 **4**	8 **4**	mA min
				35	**35**	mA max
I_S	Supply Current	Per Amplifier	650	800 **880**	800 **880**	μA max

5.0V AC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for $T_J = 25°C$, $V^+ = 5.0V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to $V_S/2$. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
SR	Slew Rate	$8\ V_{p\text{-}p}$ @ V_{CC} 12V $R_S > 1\ k\Omega$	25	15 **13**	13 **11**	V/μs min
GBW	Gain-Bandwidth Product	f = 50 kHz	17	10 **6**	10 **6**	MHz min
ϕ_m	Phase Margin		38			Deg
	Amp-to-Amp Isolation		130			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	16			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.22			$\frac{pA}{\sqrt{Hz}}$
T.H.D.	Total Harmonic Distortion	f = 10 kHz, $R_L = 10\ k\Omega$,	0.003			%

2.7V DC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.4	1.8 **4.3**	2.5 **4.3**	mV max
I_B	Input Bias Current		150	250 **526**	300 **526**	nA max
I_{OS}	Input Offset Current		4	30 **80**	30 **80**	nA max
R_{IN}	Input Resistance		128			MΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 1.8V$	90			dB min
		$0V \le V_{CM} \le 2.7V$	76			
PSRR	Power Supply Rejection Ratio	$3V \le V^+ \le 5V$	79			
V_{CM}	Input Common-Mode Voltage Range		−0.25	0	0	V min
			2.95	2.7	2.7	V max
A_V	Large Signal Voltage Gain	$R_L = 10k$	55			V/mV min
V_O	Output Swing	$R_L = 10\ k\Omega$	0.019	0.08 **0.112**	0.08 **0.112**	V max
			2.67	2.66 **2.25**	2.66 **2.25**	V min
I_S	Supply Current	Per Amplifier	510	800 **880**	800 **880**	μA max

2.7V AC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
GBW	Gain-Bandwidth Product	f = 50 kHz	9			MHz
ϕ_m	Phase Margin		36			Deg
G_m	Gain Margin		6			dB

24V Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 24V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V_S/2$. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1.3	2 **4.8**	3.8 **4.8**	mV max
I_B	Input Bias Current		174			nA max
I_{OS}	Input Offset Current		5			nA max
R_{IN}	Input Resistance		288			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 23V	114			dB min
		0V ≤ V_{CM} ≤ 24V	100			
PSRR	Power Supply Rejection Ratio	0V ≤ V_{CM} ≤ 24V	87			
V_{CM}	Input Common-Mode Voltage Range		−0.25	0	0	V min
			24.25	24	24	V max
A_V	Large Signal Voltage Gain	R_L = 10k	500			V/mV min
V_O	Output Swing	R_L = 10 kΩ	0.07	0.15 **0.185**	0.15 **0.185**	V max
			23.85	23.81 **23.62**	23.81 **23.62**	V min
I_S	Supply Current	Per Amplifier	750	1100 **1150**	1100 **1150**	μA max
GBW	Gain-Bandwidth Product	f = 50 kHz	18			MHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{j(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

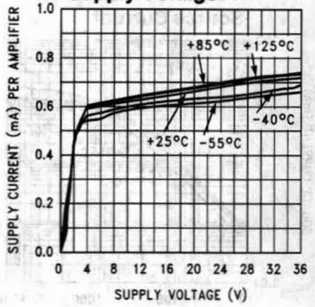
Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

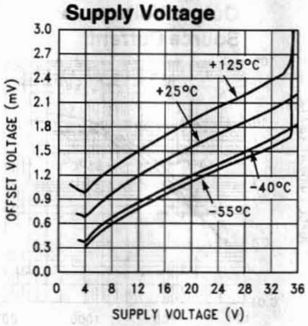
Note 7: For guaranteed military specifications see military datasheet MNLM6142AM-X.

Typical Performance Characteristics $T_A = 25°C$, $R_L = 10\ k\Omega$ Unless Otherwise Specified

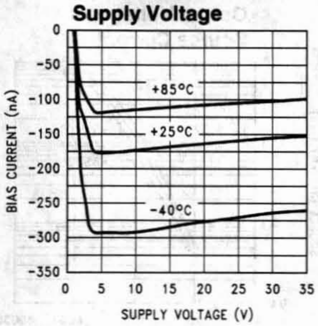
Supply Current vs Supply Voltage



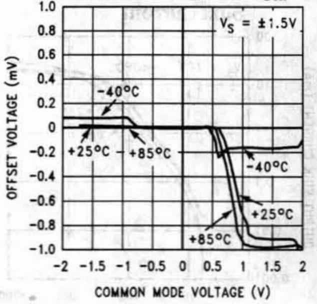
Offset Voltage vs Supply Voltage



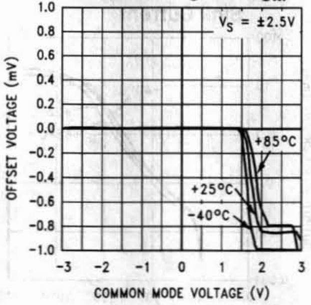
Bias Current vs Supply Voltage



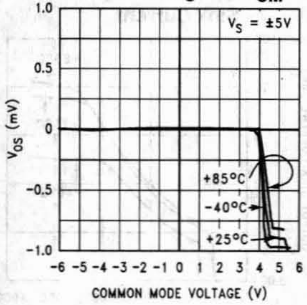
Offset Voltage vs V_{CM}



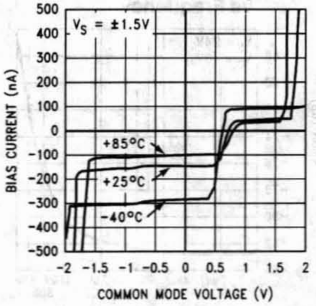
Offset Voltage vs V_{CM}



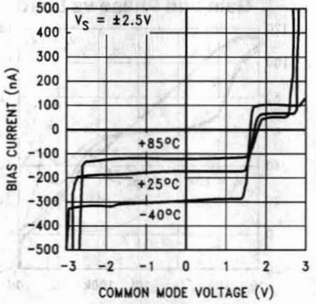
Offset Voltage vs V_{CM}



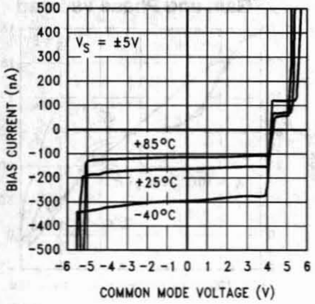
Bias Current vs V_{CM}



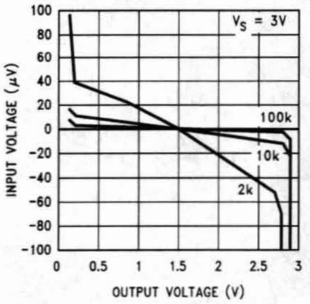
Bias Current vs V_{CM}



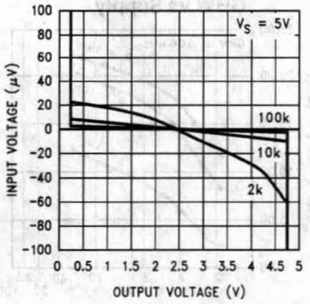
Bias Current vs V_{CM}



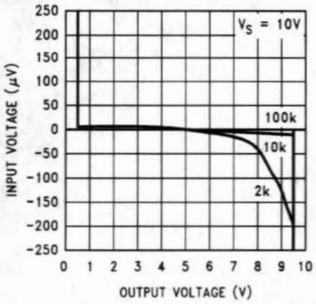
Open-Loop Transfer Function



Open-Loop Transfer Function



Open-Loop Transfer Function

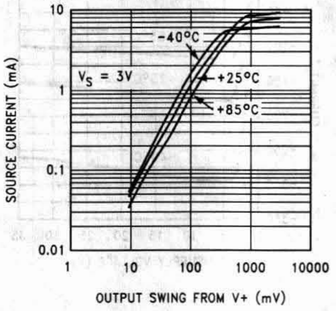


TL/H/12057–3

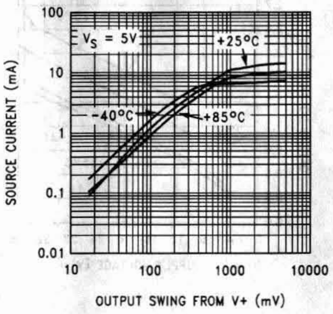
Typical Performance Characteristics

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified (Continued)

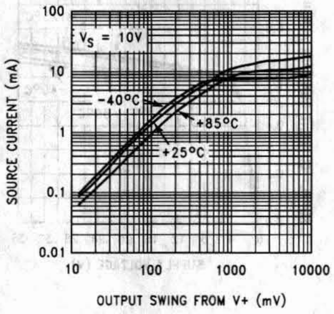
Output Voltage vs Source Current



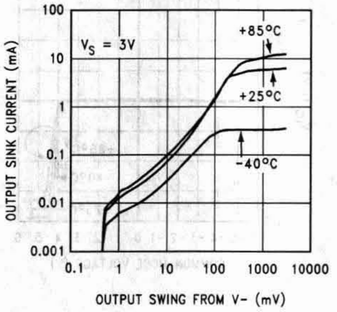
Output Voltage vs Source Current



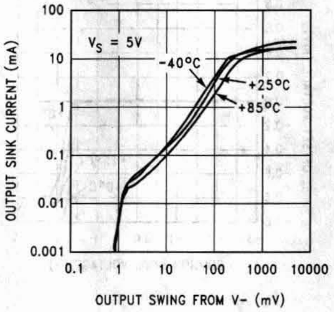
Output Voltage vs Source Current



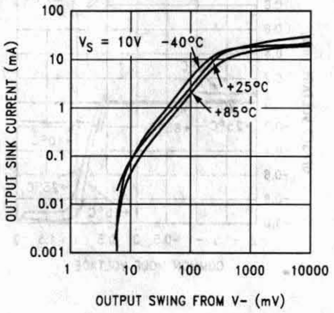
Output Voltage vs Sink Current



Output Voltage vs Sink Current

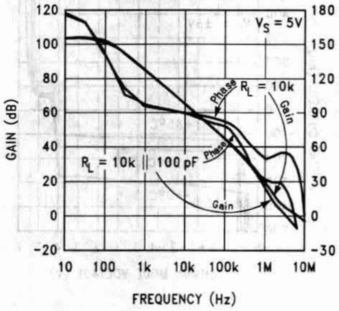


Output Voltage vs Sink Current

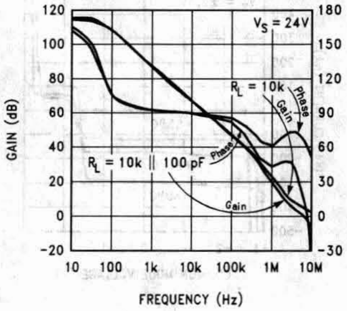


TL/H/12057–4

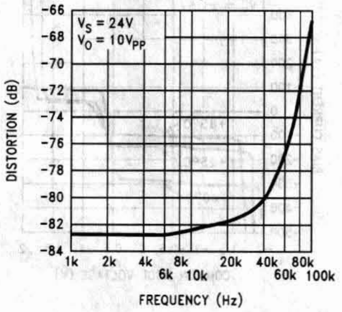
Gain and Phase vs Load



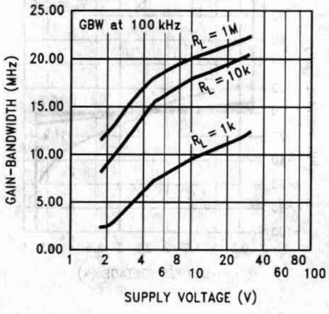
Gain and Phase vs Load



Distortion + Noise vs Frequency



GBW vs Supply

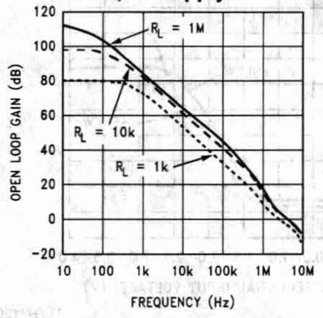


TL/H/12057–11

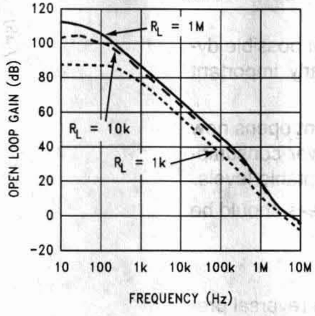
Typical Performance Characteristics

$T_A = 25°C$, $R_L = 10\ k\Omega$ Unless Otherwise Specified (Continued)

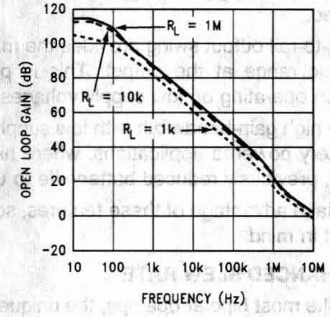
Open Loop Gain vs Load, 3V Supply



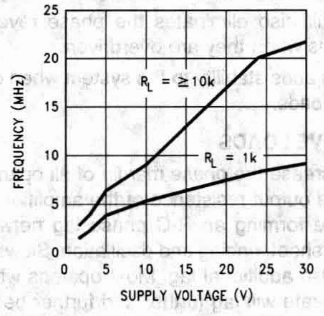
Open Loop Gain vs Load, 5V Supply



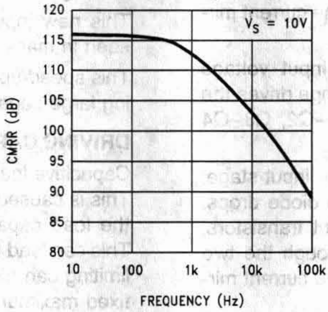
Open Loop Gain vs Load, 24V Supply



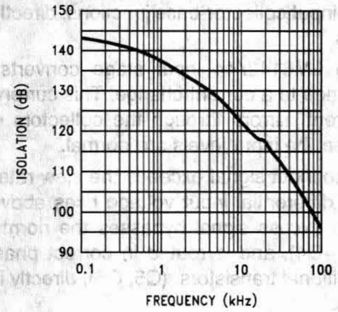
Unity Gain Freq vs V_S



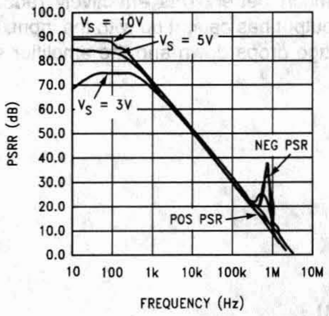
CMRR vs Frequency



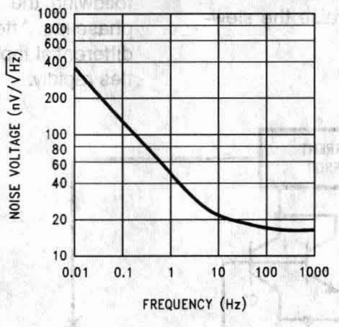
Crosstalk vs Frequency



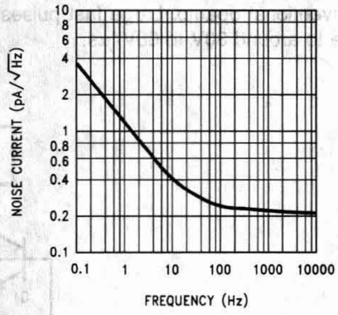
PSRR vs Frequency



Noise Voltage vs Frequency

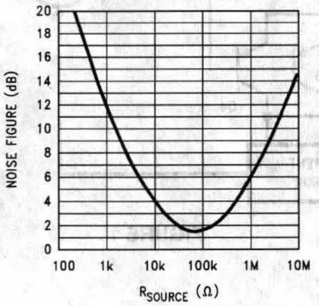


Noise Current vs Frequency



TL/H/12057-5

NE vs R Source



TL/H/12057-12

LM6142/44 Application Ideas

The LM6142 brings a new level of ease of use to opamp system design.

With greater than rail-to-rail input voltage range concern over exceeding the common-mode voltage range is eliminated.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption, previously reduced battery life to unacceptable levels.

To take advantage of these features, some ideas should be kept in mind.

ENHANCED SLEW RATE

Unlike most bipolar opamps, the unique phase reversal prevention/speed-up circuit in the input stage causes the slew rate to be very much a function of the input signal amplitude.

Figure 1 shows how excess input signal, is routed around the input collector-base junctions, directly to the current mirrors.

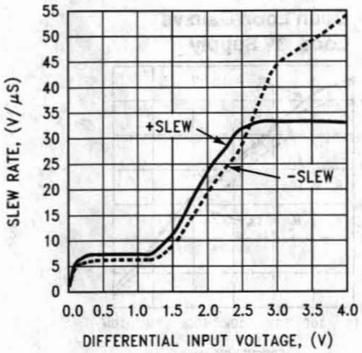
The LM6142/44 input stage converts the input voltage change to a current change. This current change drives the current mirrors through the collectors of Q1–Q2, Q3–Q4 when the input levels are normal.

If the input signal exceeds the slew rate of the input stage, the differential input voltage rises above two diode drops. This excess signal bypasses the normal input transistors, (Q1–Q4), and is routed in correct phase through the two additional transistors, (Q5, Q6), directly into the current mirrors.

This rerouting of excess signal allows the slew-rate to increase by a factor of 10 to 1 or more. (See *Figure 2*.)

As the overdrive increases, the opamp reacts better than a conventional opamp. Large fast pulses will raise the slew-rate to around 30V to 60V/µs.

Slew Rate vs Δ V_{IN}
$V_S = \pm 5V$



TL/H/12057–7

FIGURE 2

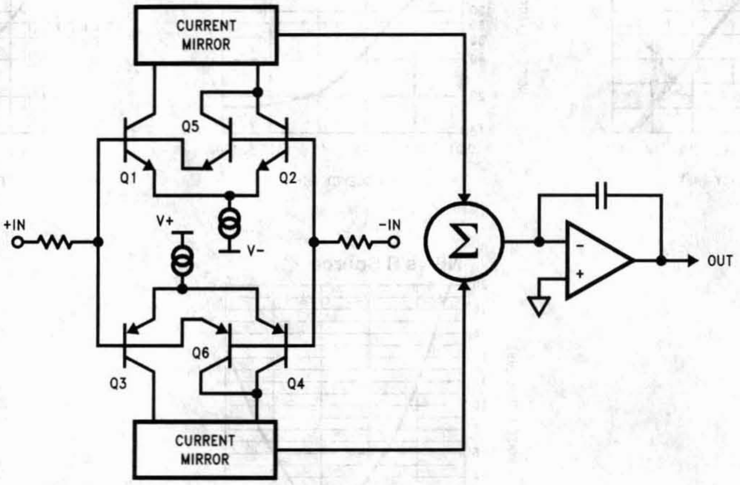
This effect is most noticeable at higher supply voltages and lower gains where incoming signals are likely to be large.

This new input circuit also eliminates the phase reversal seen in many opamps when they are overdriven.

This speed-up action adds stability to the system when driving large capacitive loads.

DRIVING CAPACITIVE LOADS

Capacitive loads decrease the phase margin of all opamps. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase lag network. This can lead to overshoot, ringing and oscillation. Slew rate limiting can also cause additional lag. Most opamps with a fixed maximum slew-rate will lag further and further behind when driving capacitive loads even though the differential input voltage raises. With the LM6142, the lag causes the slew rate to raise. The increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. After the output has caught up with the input, the differential input voltage drops down and the amplifier settles rapidly.



TL/H/12057–6

FIGURE 1

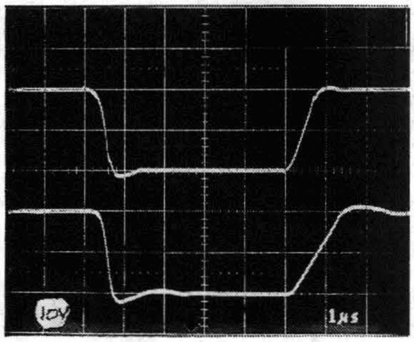
LM6142/44 Application Ideas

(Continued)

These features allow the LM6142 to drive capacitive loads as large as 1000 pF at unity gain and not oscillate. The scope photos (*Figure 3a* and *3b*) above show the LM6142 driving a I000 pF load. In *Figure 3a*, the upper trace is with no capacitive load and the lower trace is with a 1000 pF load. Here we are operating on ±12V supplies with a 20 Vp-p pulse. Excellent response is obtained with a C_f of I0 pF. In *Figure 3b*, the supplies have been reduced to ±2.5V, the pulse is 4 Vp-p and C_f is 39 pF. The best value for the compensation capacitor is best established after the board layout is finished because the value is dependent on board stray capacity, the value of the feedback resistor, the closed loop gain and, to some extent, the supply voltage.

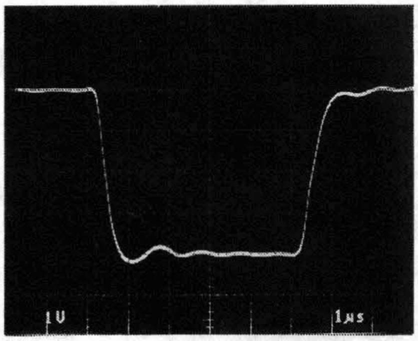
Another effect that is common to all opamps is the phase shift caused by the feedback resistor and the input capacitance. This phase shift also reduces phase margin. This effect is taken care of at the same time as the effect of the capacitive load when the capacitor is placed across the feedback resistor.

The circuit shown in *Figure 4* was used for these scope photos.



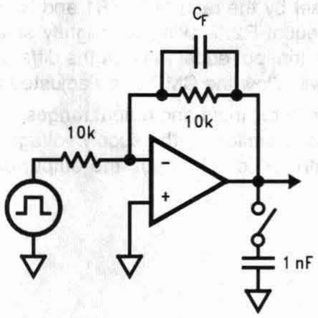
TL/H/12057–8

FIGURE 3a



TL/H/12057–9

FIGURE 3b



TL/H/12057–10

FIGURE 4

Typical Applications

FISH FINDER/ DEPTH SOUNDER.

The LM6142/44 is an excellent choice for battery operated fish finders. The low supply current, high gain-bandwidth and full rail to rail output swing of the LM6142 provides an ideal combination for use in this and similar applications.

ANALOG TO DIGITAL CONVERTER BUFFER

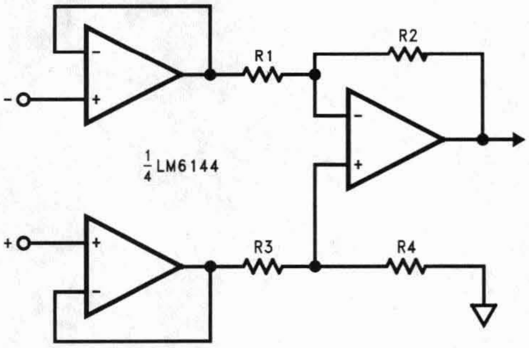
The high capacitive load driving ability, rail-to-rail input and output range with the excellent CMR of 82 dB, make the LM6142/44 a good choice for buffering the inputs of A to D converters.

3 OPAMP INSTRUMENTATION AMP WITH RAIL-TO-RAIL INPUT AND OUTPUT

Using the LM6144, a 3 opamp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6144, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage *(Figure 5).* These buffers assure that the input impedance is over 100 MΩ and they eliminate the requirement for precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1–R2 with R3–R4.



TL/H/12057–13

FIGURE 5

The gain is set by the ratio of R2/R1 and R3 should equal R1 and R4 equal R2. Making R4 slightly smaller than R2 and adding a trim pot equal to twice the difference between R2 and R4 will allow the CMR to be adjusted for optimum.

With both rail to rail input and output ranges, the inputs and outputs are only limited by the supply voltages. Remember that even with rail-to-rail output, the output can not swing past the supplies so the combined common mode voltage plus the signal should not be greater than the supplies or limiting will occur.

SPICE MACROMODEL

A SPICE macromodel of this and many other National Semiconductor opamps is available at no charge from the NSC Customer Response Group at 800-272-9959.

National Semiconductor

PRELIMINARY

LM6152 Dual and LM6154 Quad High Speed/Low Power 45 MHz Rail-to-Rail I/O Operational Amplifiers

General Description

Using patent pending circuit topologies, the LM6152/54 provides new levels of speed vs power performance in applications where low voltage supplies or power limitations made compromise necessary. With only 1.5 mA/amp supply current, the 45 MHz bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

In addition, the LM6152/54 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages. The LM6152/54 can also drive capacitive loads without oscillating.

Operating on supplies of 1.8V to over 24V, the LM6152/54 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

Features (For 5V Supply)

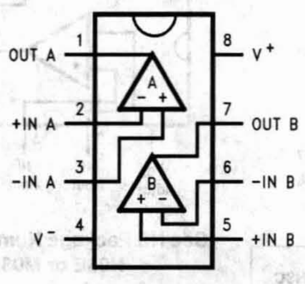
■ Rail-to-rail input CMVR	−0.25V to 5.25V (max/min)
■ Rail-to-rail output swing	0.01V to 4.99V (max/min)
■ Wide gain-bandwidth:	45 MHz (typ) @ 50 kHz
■ Slew rate	30 V/μs (typ)
■ Low supply current	1.5/Amp (typ)
■ Wide supply range	1.8V to 24V
■ Fast settling time:	
— Gain	108 dB (typ) with R_L = 10k
■ PSRR	87 dB (typ)

Applications

- Portable high speed instrumentation
- 5V signal conditioning amplifiers/ADC buffers
- Bar code scanners
- Wireless communications

Connection Diagrams

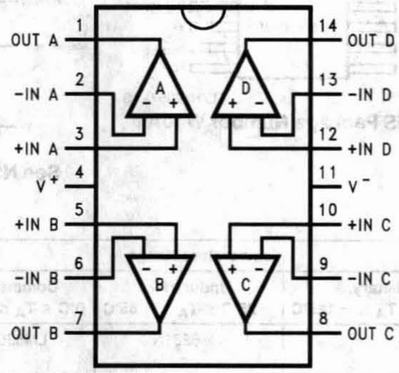
8-Pin DIP/SO



Top View

TL/H/12350–1

14-Pin DIP/SO



TL/H/12350–2

Top View

Ordering Information

Package	Temperature Range	NSC Drawing
	Industrial −40°C to +85°C	
8-Pin Molded DIP	LM6142AIN, LM6142BIN	N08E
8-Pin Small Outline	LM6142AIM, LM6142BIM	M08A
14-Pin Molded DIP	LM6144AIN, LM6144BIN	N14A
14-Pin Small Outline	LM6144AIM, LM6144BIM	M14A

National Semiconductor

LM6161/LM6261/LM6361
High Speed Operational Amplifier

General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

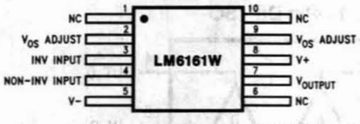
■ High slew rate	300 V/μs
■ High unity gain freq	50 MHz
■ Low supply current	5 mA
■ Fast settling	120 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	
■ Well behaved; easy to apply	

Applications

- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams

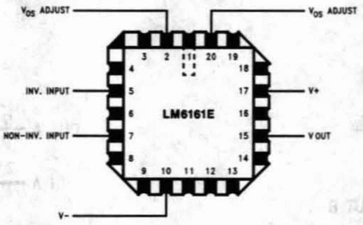
10-Lead Flatpak


NC
V_{OS} ADJUST
INV INPUT
NON-INV INPUT
V−
1
2
3
4
5
10
9
8
7
6
LM6161W
NC
V_{OS} ADJUST
V+
V_{OUTPUT}
NC

TL/H/9057–13

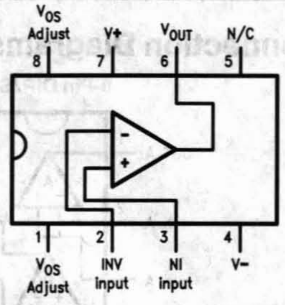
See NS Package Number W10A

20-Lead LCC


V_{OS} ADJUST
V_{OS} ADJUST
INV. INPUT
NON-INV. INPUT
V−
LM6161E
V+
V OUT
3
2
1
20
19
4
5
6
7
8
18
17
16
15
14
9
10
11
12
13

TL/H/9057–14

See NS Package Number E20A


V_{OS} Adjust
V+
V_{OUT}
N/C
8
7
6
5
−
+
1
2
3
4
V_{OS} Adjust
INV input
NI input
V−

TL/H/9057–5

See NS Package Number J08A, N08E or M08A

Temperature Range			Package	NSC Drawing
Military **$-55^{\circ}C \le T_A \le +125^{\circ}C$**	**Industrial** **$-25^{\circ}C \le T_A \le +85^{\circ}C$**	**Commercial** **$0^{\circ}C \le T_A \le +70^{\circ}C$**		
	LM6261N	LM6361N	8-Pin Molded DIP	N08E
LM6161J/883 5962-8962101PA		LM6361J	8-Pin Ceramic DIP	J08A
	LM6261M	LM6361M	8-Pin Molded Surface Mt.	M08A
LM6161E/883 5962-89621012A			20-Lead LCC	E20A
LM6161W/883 5962-8962101HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
Common-Mode Voltage Range (Note 10)	(V^+ − 0.7V) to (V^- − 7V)
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	−65°C to +150°C
Max Junction Temperature	150°C
ESD Tolerance (Notes 6 and 7)	±700V

Operating Ratings (Note 12)

Temperature Range (Note 2)	
LM6161	$-55°C \le T_J \le +125°C$
LM6261	$-25°C \le T_J \le +85°C$
LM6361	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \ge 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX}; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LM6161	LM6261	LM6361	Units
				Limit (Notes 3, 11)	Limit (Note 3)	Limit (Note 3)	
V_{OS}	Input Offset Voltage		5	7 **10**	7 **9**	20 **22**	mV Max
V_{OS} Drift	Input Offset Voltage Average Drift		10				μV/°C
I_b	Input Bias Current		2	3 **6**	3 **5**	5 **6**	μA Max
I_{OS}	Input Offset Current		150	350 **800**	350 **600**	1500 **1900**	nA Max
I_{OS} Drift	Input Offset Current Average Drift		0.4				nA/°C
R_{IN}	Input Resistance	Differential	325				kΩ
C_{IN}	Input Capacitance	A_V = +1 @ 10 MHz	1.5				pF
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 9)	750	550 **300**	550 **400**	400 **350**	V/V Min
		R_L = 10 kΩ (Note 9)	2900				V/V
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	Volts Min
			−13.2	−12.9 **−12.7**	−12.9 **−12.7**	−12.8 **−12.7**	Volts Min
		Supply = +5V (Note 4)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	Volts Min
			1.8	2.0 **2.2**	2.0 **2.2**	2.1 **2.2**	Volts Max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	94	80 **74**	80 **76**	72 **70**	dB Min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V^{\pm} \le \pm 16V$	90	80 **74**	80 **76**	72 **70**	dB Min
V_O	Output Voltage Swing	Supply = ±15V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **+13.3**	Volts Min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	Volts Min

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq$ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for T_J = T_{MIN} to T_{MAX}; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LM6161	LM6261	LM6361	Units
				Limit (Notes 3, 11)	Limit (Note 3)	Limit (Note 3)	
V_O (Continued)	Output Voltage Swing (Continued)	Supply = +5V and R_L = 2 kΩ (Note 4)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	Volts Min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	Volts Max
	Output Short Circuit Current	Source	65	30 **20**	30 **25**	30 **25**	mA Min
		Sink	65	30 **20**	30 **25**	30 **25**	mA Min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA Max

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq$ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for T_J = T_{MIN} to T_{MAX}; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LM6161	LM6261	LM6361	Units
				Limit (Notes 3, 11)	Limit (Note 3)	Limit (Note 3)	
GBW	Gain-Bandwidth Product	@ f = 20 MHz	50	40 **30**	40 **35**	35 **32**	MHz Min
		Supply = ±5V	35				MHz
SR	Slew Rate	A_V = +1 (Note 8)	300	200 **180**	200 **180**	200 **180**	V/μs Min
		Supply = ±5V (Note 8)	200				V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
t_S	Settling Time	10V Step to 0.1% A_V = −1, R_L = 2 kΩ	120				ns
ϕm	Phase Margin		45				Deg
A_D	Differential Gain	NTSC, A_V = +4	<0.1				%
ϕD	Differential Phase	NTSC, A_V = +4	0.1				Deg
$e_{np\text{-}p}$	Input Noise Voltage	f = 10 kHz	15				$nV/\sqrt{Hz}$
$i_{np\text{-}p}$	Input Noise Current	f = 10 kHz	1.5				$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/W, the molded plastic SO (M) package is 155°C/W, and the cerdip (J) package is 125°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Limits are guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (Vos Adjust) are each connected to Pin 4 (V^-) to realize maximum output swing. This connection will degrade V_{OS}, V_{OS} Drift, and Input Voltage Noise.

Note 5: $C_L \leq$ 5 pF.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vos, Ios, and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: V_{IN} = 8V step. For supply = ±5V, V_{IN} = 5V step.

Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

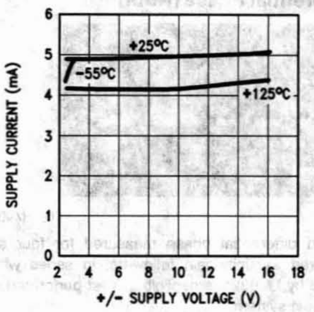
Note 10: The voltage between V^+ and either input pin must not exceed 36V.

Note 11: A military RETS electrical test specification is available on request. At the time of printing, the RETS6161X specs complied with all **Boldface** limits in this column.

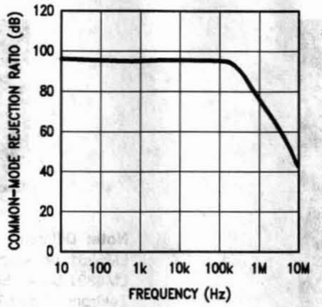
Note 12: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25°C unless otherwise specified)

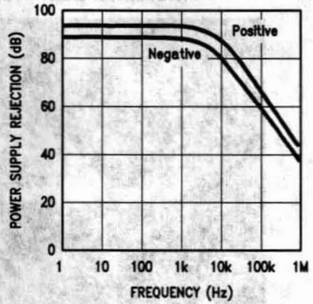
Supply Current vs Supply Voltage



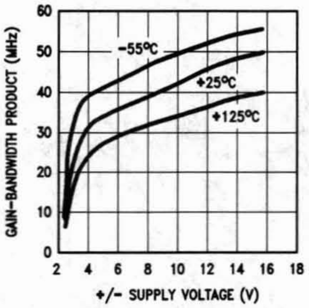
Common-Mode Rejection Ratio



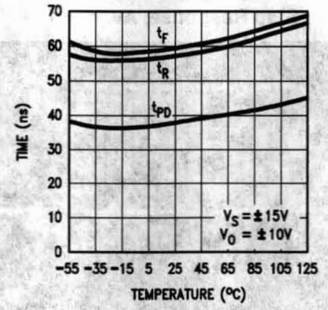
Power Supply Rejection Ratio



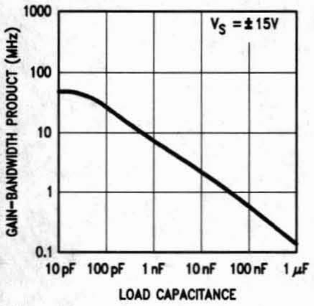
Gain-Bandwidth Product



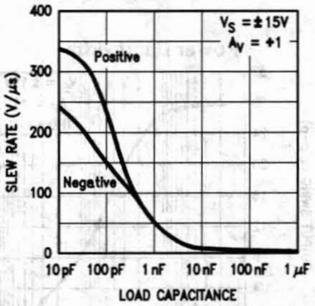
Propagation Delay Rise and Fall Times



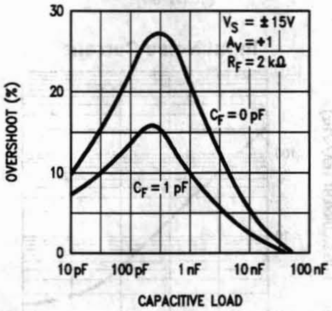
Gain-Bandwidth Product vs Load Capacitance



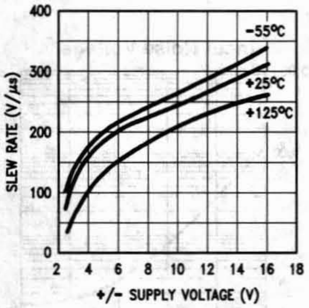
Slew Rate vs Load Capacitance



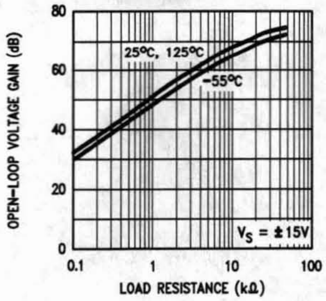
Overshoot vs Capacitive Load



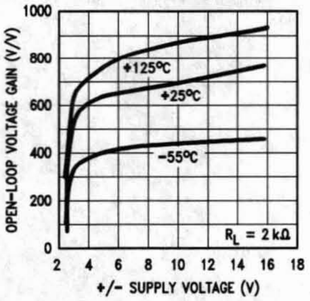
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage

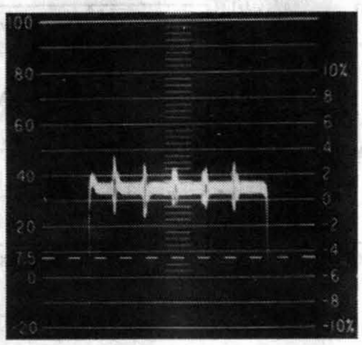


TL/H/9057-6

Typical Performance Characteristics

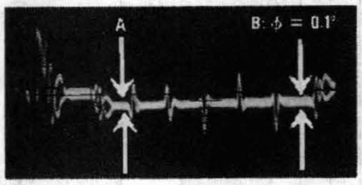
(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



TL/H/9057-7

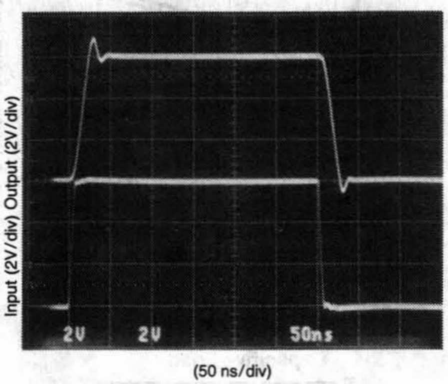
Differential Phase (Note)



TL/H/9057-8

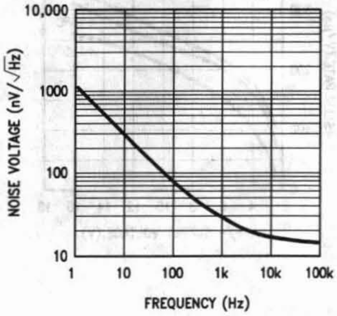
Note: Differential gain and differential phase measured for four series LM6361 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response; Av = +1

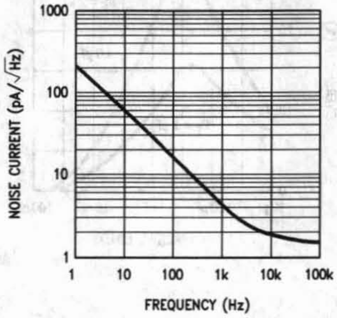


TL/H/9057-1

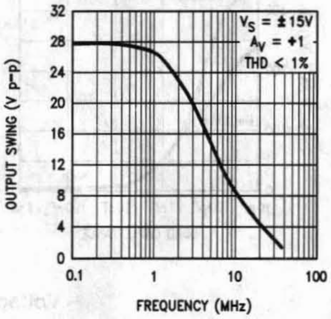
Input Noise Voltage



Input Noise Current



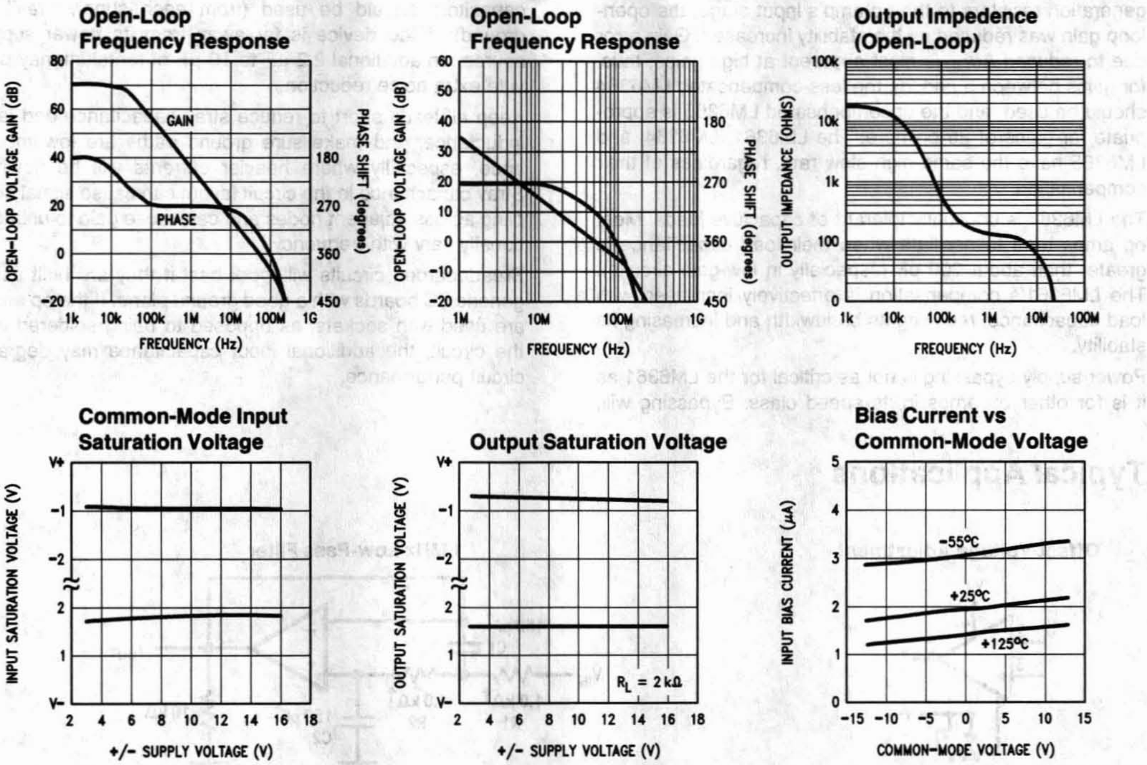
Power Bandwidth



TL/H/9057-9

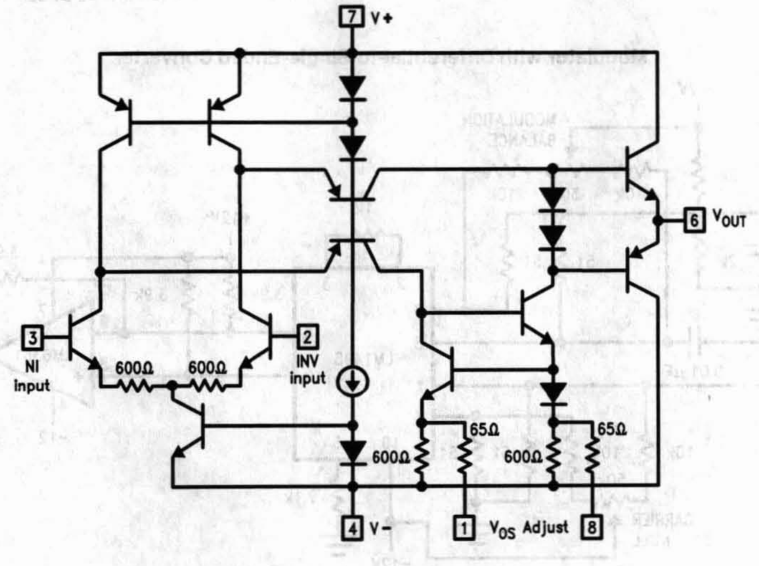
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)



TL/H/9057-12

Simplified Schematic


7 V+
6 V_{OUT}
3 NI Input
2 INV input
600Ω
600Ω
600Ω
65Ω
600Ω
65Ω
4 V−
1 V_{OS} Adjust 8

TL/H/9057-3

Applications Tips

The LM6361 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors to the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, for gains between 5 and 25, the less-compensated LM6364 should be used, and the uncompensated LM6365 is appropriate for gains of 25 or more. The LM6361, LM6364, and LM6365 have the same high slew rate, regardless of their compensation.

The LM6361 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). The LM6361's compensation is effectively increased with load capacitance, reducing its bandwidth and increasing its stability.

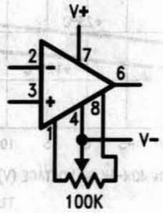
Power supply bypassing is not as critical for the LM6361 as it is for other op amps in its speed class. Bypassing will, however, improve the stability and transient response and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may provide extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling across adjacent nodes and can cause gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

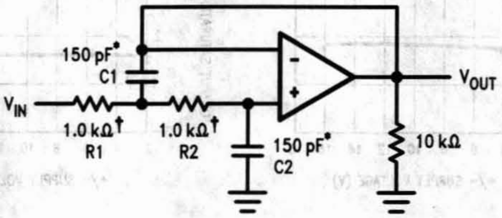
Typical Applications

Offset Voltage Adjustment


V+
2
3
7
6
4
8
1
V-
100K

TL/H/9057–4

1 MHz Low-Pass Filter


150 pF*
C1
V_{IN}
1.0 kΩ†
R1
1.0 kΩ†
R2
150 pF*
C2
V_{OUT}
10 kΩ

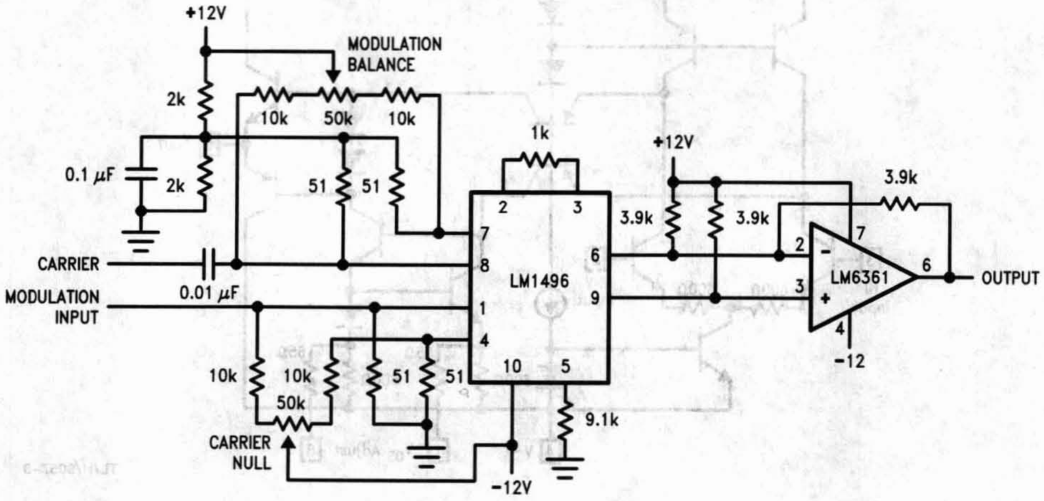
TL/H/9057–10

†1% tolerance

*Matching determines filter precision

$f_c = (2\pi \sqrt{(R1\ R2\ C1\ C2)})^{-1}$

Modulator with Differential-to-Single-Ended Converter


+12V
MODULATION BALANCE
2k
10k
50k
10k
0.1 μF
2k
51
51
1k
+12V
2
3
7
8
6
9
1
4
10
5
LM1496
3.9k
3.9k
3.9k
2
3
7
6
4
LM6361
OUTPUT
-12
CARRIER
MODULATION INPUT
0.01 μF
10k
10k
51
51
50k
CARRIER NULL
9.1k
-12V

TL/H/9057–11

National Semiconductor

LM6162/LM6262/LM6362
High Speed Operational Amplifier

General Description

The LM6362 family of high-speed amplifiers exhibits an excellent speed-power product, delivering 300 V/μs and 100 MHz gain-bandwidth product (stable for gains as low as +2 or −1) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

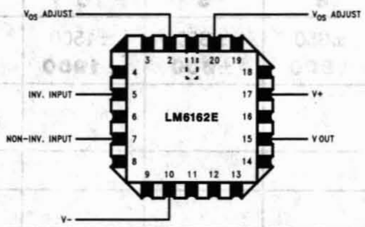
■ High slew rate	300 V/μs
■ High gain-bandwidth product	100 MHz
■ Low supply current	5 mA
■ Fast settling time	120 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	<0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	
■ Well behaved; easy to apply	

Applications

- Video amplifier
- Wide-bandwidth signal conditioning for image processing (FAX, scanners, laser printers)
- Hard disk drive preamplifier
- Error amplifier for high-speed switching regulator

Connection Diagrams

20-Lead LCC



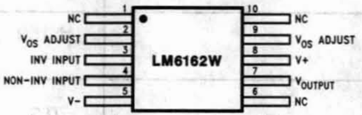
V_{OS} ADJUST
V_{OS} ADJUST
3
2
1
20
19
4
18
INV. INPUT
5
17
V+
6
LM6162E
16
NON-INV. INPUT
7
15
V OUT
8
14
9
10
11
12
13
V−

TL/H/11061-14

Top View

See NS Package Number E20A

10-Pin Ceramic Flatpak

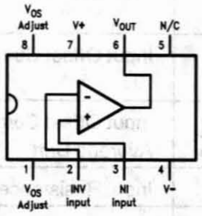


NC
1
10
NC
V_{OS} ADJUST
2
9
V_{OS} ADJUST
INV INPUT
3
8
V+
NON-INV INPUT
4
LM6162W
7
V_{OUTPUT}
V−
5
6
NC

TL/H/11061-15

Top View

See NS Package Number W10A



V_{OS} Adjust
V+
V_{OUT}
N/C
8
7
6
5
1
2
3
4
V_{OS} Adjust
INV Input
NI Input
V−

TL/H/11061-2

See NS Package Number N08E, M08A or J08A

Temperature Range			Package	NSC Drawing
Military **−55°C ≤ T_A ≤ +125°C**	**Industrial** **−25°C ≤ T_A ≤ +85°C**	**Commercial** **0°C ≤ T_A ≤ +70°C**		
LM6162N	LM6262N	LM6362N	8-Pin Molded DIP	N08E
LM6162J/883 5962-9216501PA			8-Pin Ceramic DIP	J08A
	LM6262M	LM6362M	8-Pin Molded Surface Mt.	M08A
LM6162E/883 5962-92165012A			20-Lead LCC	E20A
LM6162W/883 5962-9216501HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $(V^+ - V^-)$	36V
Differential Input Voltage (Note 2)	±8V
Common-Mode Input Voltage (Note 3)	$(V^+ - 0.7V)$ to $(V^- - 0.3V)$
Output Short Circuit to GND (Note 4)	Continuous
Soldering Information	
Dual-In-Line Package (N)	
Soldering (10 seconds)	260°C
Small Outline Package (M)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temperature Range	$-65°C \leq T_J \leq +150°C$
Max Junction Temperature	150°C
ESD Tolerance (Note 5)	±1100V

Operating Ratings

Temperature Range (Note 6)	
LM6162	$-55°C \leq T_J \leq +125°C$
LM6262	$-25°C \leq T_J \leq +85°C$
LM6362	$0°C \leq T_J \leq +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

These limits apply for supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq 100\ k\Omega$, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
V_{OS}	Input Offset Voltage		±3	±5 **±8**	±5 **±8**	±13 **±15**	mV max
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Average Drift		7				μV/°C
I_{bias}	Input Bias Current		2.2	3 **6**	3 **5**	4 **6**	μA max
I_{OS}	Input Offset Current		±150	±350 **±800**	±350 **±600**	±1500 **±1900**	nA max
$\frac{\Delta I_{OS}}{\Delta Temp}$	Input Offset Current Average Drift		0.3				nA/°C
R_{IN}	Input Resistance	Differential	180				kΩ
C_{IN}	Input Capacitance		2.0				pF
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$ (Note 9)	1400	1000 **500**	1000 **700**	800 **650**	V/V min
		$R_L = 10\ k\Omega$	6500				V/V
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	V min
			−13.2	−12.9 **−12.7**	−12.9 **−12.7**	−12.9 **−12.8**	V max
		Supply = +5V (Note 10)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	V min
			1.6	1.8 **2.0**	1.8 **2.0**	1.9 **2.0**	V max
CMRR	Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	100	83 **79**	83 **79**	76 **74**	dB min
PSRR	Power Supply Rejection Ratio	$\pm 10V \leq V_S \leq \pm 16V$	93	83 **79**	83 **79**	76 **74**	dB min
V_O	Output Voltage Swing	Supply = ±15V, $R_L = 2\ k\Omega$	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **13.3**	V min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	V max

DC Electrical Characteristics (Continued)

These limits apply for supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq$ 100 kΩ, unless otherwise specified. Limits in standard typeface are for $T_A = T_J$ = 25°C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
V_O	Output Voltage Swing	Supply = +5V and R_L = 2 kΩ (Note 10)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	V min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	V max
I_{OSC}	Output Short Circuit Current	Sourcing	65	30 **20**	30 **25**	30 **25**	mA min
		Sinking	65	30 **20**	30 **25**	30 **25**	mA min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA max

AC Electrical Characteristics

These limits apply for supply voltage = ±15V, V_{CM} = 0V, $R_L \geq$ 100 kΩ, and $C_L \leq$ 5 pF, unless otherwise specified. Limits in standard typeface are for $T_A = T_J$ = 25°C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
GBW	Gain-Bandwidth Product	f = 20 MHz	100	80 **55**	80 **65**	75 **65**	MHz min
		Supply = ±5V	70				MHz
SR	Slew Rate	A_V = +2 (Note 11)	300	200 **180**	200 **180**	200 **180**	V/μs min
		Supply = ±5V	200				V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
t_s	Settling Time	10V step, to 0.1% A_V = −1, R_L = 2 kΩ	100				ns
ϕ_m	Phase Margin	A_V = +2	45				deg
	Differential Gain	NTSC, A_V = +2	<0.1				%
	Differential Phase	NTSC, A_V = +2	<0.1				deg
e_n	Input Noise Voltage	f = 10 kHz	10				nV/$\sqrt{}$Hz
i_n	Input Noise Current	f = 10 kHz	1.2				pA/$\sqrt{}$Hz

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: The ESD protection circuitry between the inputs will begin to conduct when the differential input voltage reaches 8V.

Note 3: a) In addition, the voltage between the V^+ pin and either input pin must not exceed 36V.

b) When the voltage applied to an input pin is driven more than 0.3V below the negative supply pin voltage, a substrate diode begins to conduct. Current through this pin must then be kept less than 20 mA to limit damage from self-heating.

Note 4: Although the output current is internally limited, continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 5: This value is the average voltage that the weakest pin combinations can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model, 100 pF in series with 1500Ω.

Note 6: The typical thermal resistance, junction-to-ambient, of the molded plastic DIP (N package) is 105°C/W. For the molded plastic SO (M package), use 155°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 7: Typical values are for T_J = 25°C, and represent the most likely parametric norm.

Note 8: Limits are guaranteed, by testing or correlation.

Note 9: Voltage Gain is the total output swing (20V) divided by the magnitude of the input signal required to produce that swing.

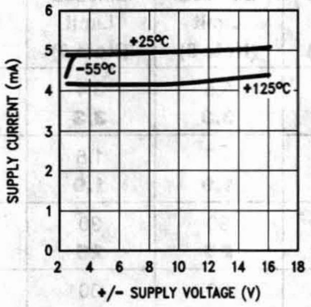
Note 10: For single-supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 and Pin 8 (V_{OS} Adjust pins) are each connected to pin 4 (V−) to realize maximum output swing. This connection will increase the offset voltage.

Note 11: V_{IN} = 10V step. For ±5V supplies, V_{IN} = 1V step.

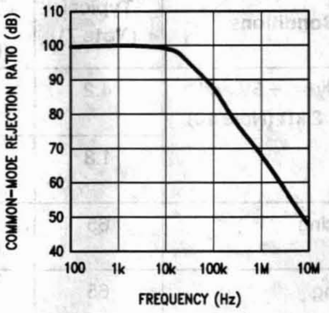
Note 12: A military RETS electrical test specification is available on request.

Typical Performance Characteristics $R_L = 10\ k\Omega$, $T_A = 25°C$ unless otherwise noted

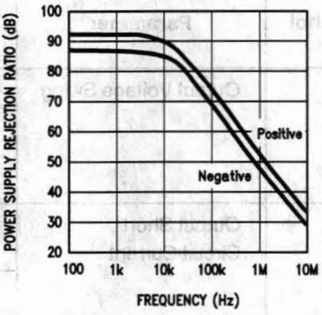
Supply Current vs Supply Voltage



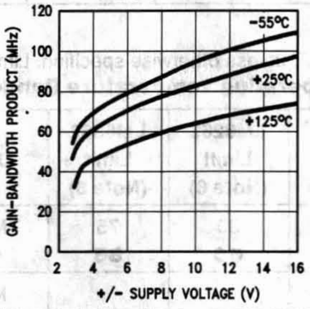
Common-Mode Rejection Ratio



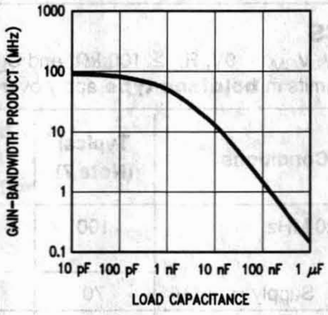
Power Supply Rejection Ratio



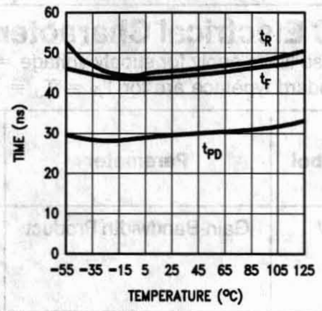
Gain-Bandwidth Product vs Supply Voltage



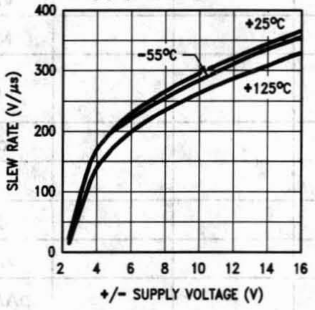
Gain-Bandwidth Product vs Load Capacitance



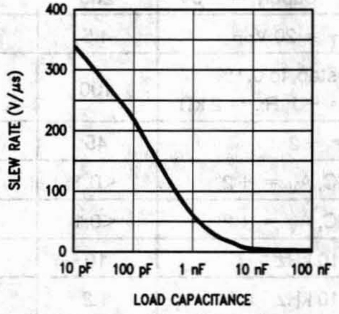
Propagation Delay, Rise and Fall Times



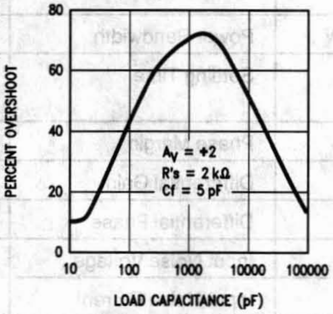
Slew Rate vs Supply Voltage



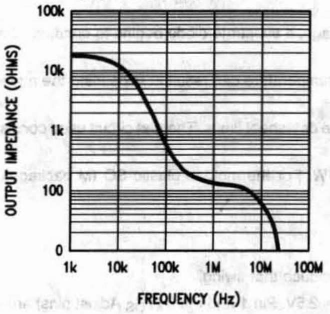
Slew Rate vs Load Capacitance



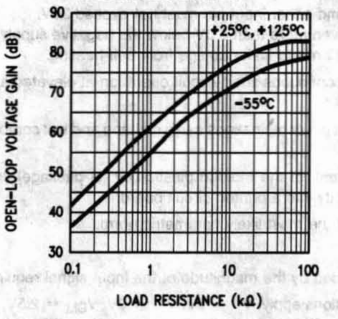
Overshoot vs Load Capacitance



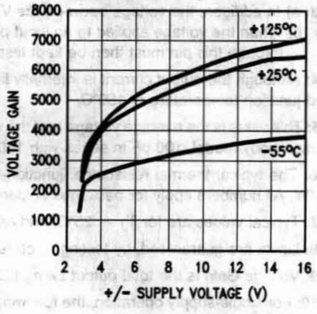
Output Impedance (Open-Loop)



Voltage Gain vs Load Resistance



Voltage Gain vs Supply Voltage

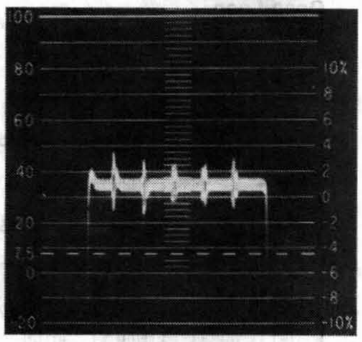


TL/H/11061–3

Typical Performance Characteristics (Continued)

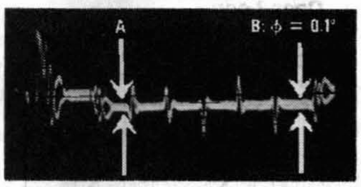
R_L = 10 kΩ, T_A = 25°C unless otherwise noted

Differential Gain (Note)



TL/H/11061-4

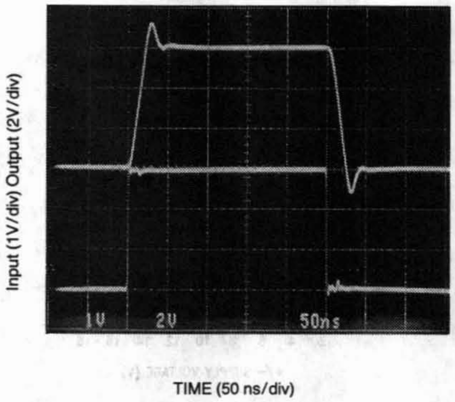
Differential Phase (Note)



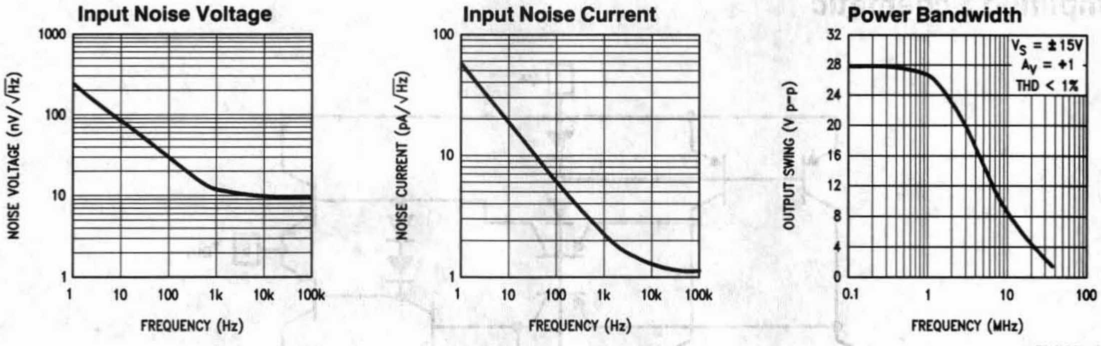
TL/H/11061-5

Note: Differential gain and differential phase measured for four series LM6362 op amps configured with gain of +2 each, in series with a 1:16 attenuator and an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response; Av = +2



TL/H/11061-6



Input Noise Voltage

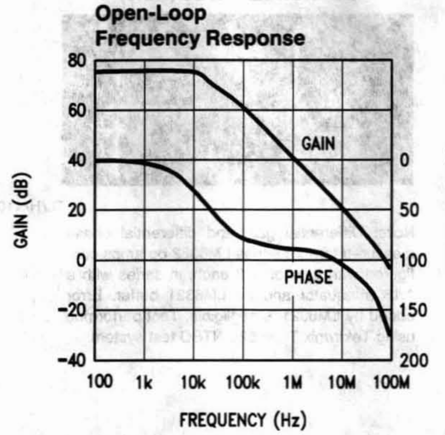
Input Noise Current

Power Bandwidth

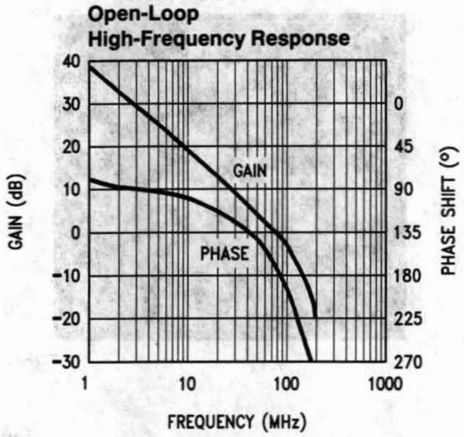
TL/H/11061-7

Typical Performance Characteristics (Continued)

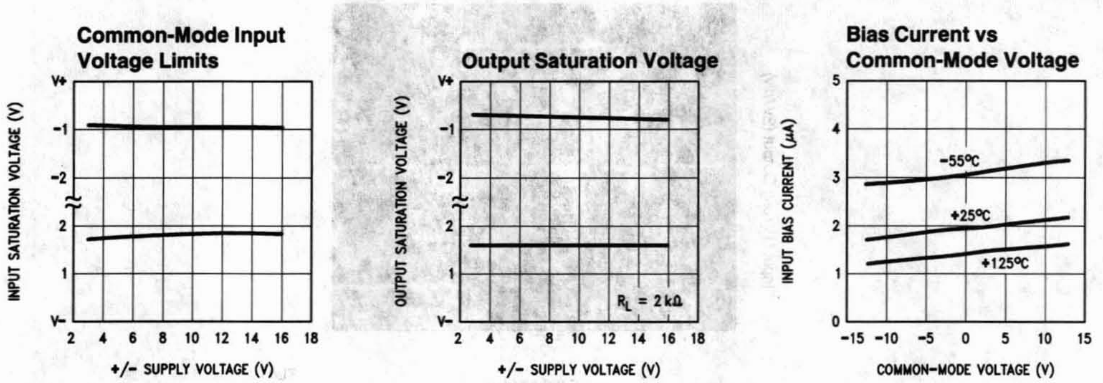
R_L = 10 kΩ, T_A = 25°C unless otherwise noted



TL/H/11061-8

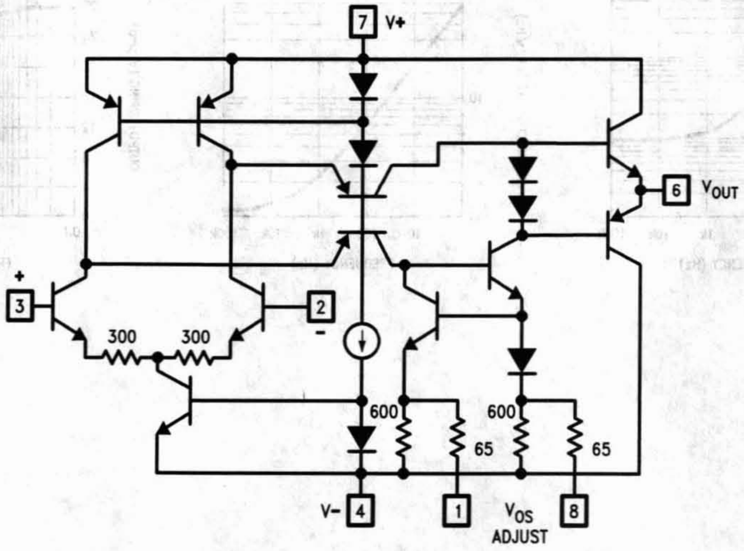


TL/H/11061-9



TL/H/11061-10

Simplified Schematic


7 V+
6 V_{OUT}
+
3
2
−
300
300
600
65
600
65
V− 4
1
V_{OS} ADJUST
8

TL/H/11061-1

Application Tips

The LM6362 has been decompensated for a wider gain-bandwidth product than the LM6361. However, the LM6362 still offers stability at gains of 2 (and −1) or greater over the specified ranges of temperature, power supply voltage, and load. Since this decompensation involved reducing the emitter-degeneration resistors in the op amp's input stage, the DC precision has been increased in the form of lower offset voltage and higher open-loop gain.

Other op amps in this family include the LM6361, LM6364, and LM6365. If unity-gain stability is required, the LM6361 should be used. The LM6364 has been decompensated for operation at gains of 5 or more, with corresponding greater gain-bandwidth product (125 MHz, typical) and DC precision. The fully-uncompensated LM6365 offers gain-bandwidth product of 725 MHz, typical, and is stable for gains of 25 or more. All parts in this family, regardless of compensation, have the same high slew rate of 300 V/μs (typ).

The LM6362 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6362 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing may occur in low-gain circuits with large capacitive loads.

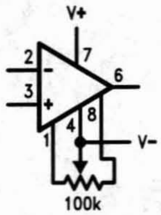
Power supply bypassing is not as critical for LM6362 as it is for other op amps in its speed class. However, bypassing will improve the stability and transient response of the LM6362, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling from one pin, input or lead to another, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit frequency response. At low gains (+2 or −1), a feedback capacitor C_f from output to inverting input will compensate for the phase lag caused by capacitance at the inverting input. Typically, values from 2 pF to 5 pF work well; however, best results can be obtained by observing the amplifier pulse response and optimizing C_f for the particular layout.

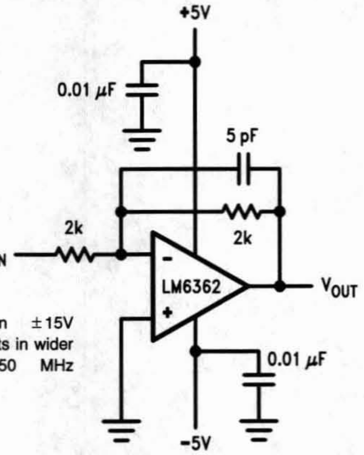
Typical Applications

Offset Voltage Adjustment



TL/H/11061-11

Inverting Amplifier, 30 MHz Bandwidth

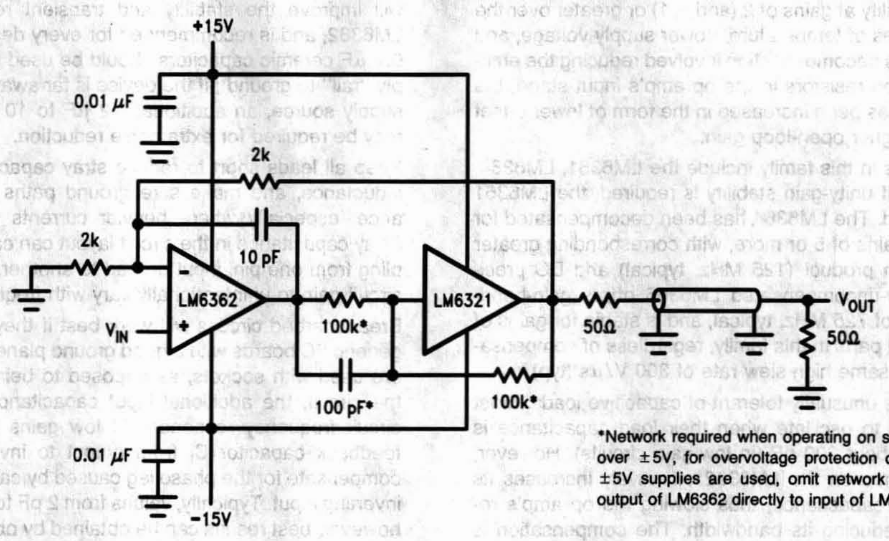


Operation on ±15V supplies results in wider bandwidth, 50 MHz (typ).

TL/H/11061-12

Typical Applications (Continued)

Video Cable Driver


+15V
0.01 µF
2k
10 pF
2k
LM6362
V_IN
100k*
100 pF*
LM6321
100k*
50Ω
V_OUT
50Ω
0.01 µF
−15V

*Network required when operating on supply voltage over ±5V, for overvoltage protection of LM6321. If ±5V supplies are used, omit network and connect output of LM6362 directly to input of LM6321.

TL/H/11061–13

National Semiconductor

LM6164/LM6264/LM6364
High Speed Operational Amplifier

General Description

The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per μs and 175 MHz GBW (stable down to gains as low as +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

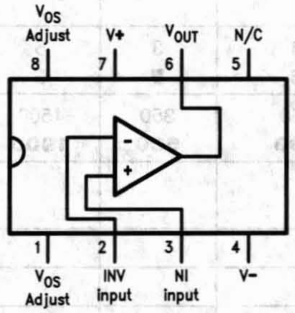
Features

■ High slew rate	300 V/μs
■ High GBW product	175 MHz
■ Low supply current	5 mA
■ Fast settling	100 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	<0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	

Applications

- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams

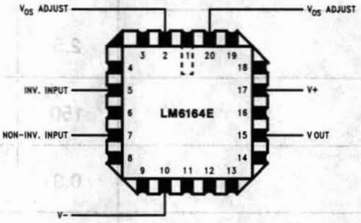


V_{OS} Adjust
V+
V_{OUT}
N/C
8
7
6
5
1
2
3
4
V_{OS} Adjust
INV Input
NI Input
V−

TL/H/9153-8

NS Package Number J08A, M08A or N08E

20-Lead LCC



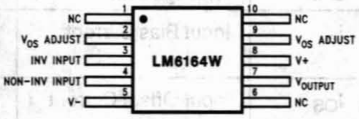
V_{OS} ADJUST
V_{OS} ADJUST
INV. INPUT
NON-INV. INPUT
V+
V OUT
V−
LM6164E
3
2
1
20
19
4
5
6
7
8
18
17
16
15
14
9
10
11
12
13

TL/H/9153-14

Top View

NS Package Number E20A

10-Lead Flatpak



NC
V_{OS} ADJUST
INV INPUT
NON-INV INPUT
V−
1
2
3
4
5
10
9
8
7
6
NC
V_{OS} ADJUST
V+
V_{OUTPUT}
NC
LM6164W

TL/H/9153-15

Top View

NS Package Number W10A

Temperature Range			Package	NSC Drawing
Military $-55°C \le T_A \le +125°C$	Industrial $-25°C \le T_A \le +85°C$	Commercial $0°C \le T_A \le +70°C$		
	LM6264N	LM6364N	8-Pin Molded DIP	N08E
LM6164J/883 5962-8962401PA			8-Pin Ceramic DIP	J08A
		LM6364M	8-Pin Molded Surface Mt.	M08A
LM6164E/883 5962-89624012A			20-Lead LCC	E20A
LM6164W/883 5962-8962401HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 6)	±8V
Common-Mode Input Voltage (Note 10)	(V^+ − 0.7V) to (V^- − 7V)
Output Short Circuit to Gnd (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temperature Range	−65°C to +150°C
Max Junction Temperature (Note 2)	150°C
ESD Tolerance (Notes 6 & 7)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6164	$-55°C \leq T_J \leq +125°C$
LM6264	$-25°C \leq T_J \leq +85°C$
LM6364	$0°C \leq T_J \leq +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6164	LM6264	LM6364	Units
				Limit (Notes 3, 11)	Limit (Note 3)	Limit (Note 3)	
V_{OS}	Input Offset Voltage		2	4 **6**	4 **6**	9 **11**	mV max
V_{OS} Drift	Input Offset Voltage Average Drift		6				μV/°C
I_b	Input Bias Current		2.5	3 **6**	3 **5**	5 **6**	μA max
I_{OS}	Input Offset Current		150	350 **800**	350 **600**	1500 **1900**	mA max
I_{OS} Drift	Input Offset Current Average Drift		0.3				nA/°C
R_{IN}	Input Resistance	Differential	100				kΩ
C_{IN}	Input Capacitance		3.0				pF
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$ (Note 9)	2.5	1.8 **0.9**	1.8 **1.2**	1.3 **1.1**	V/mV min
		$R_L = 10\ k\Omega$	9				
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	V min
			−13.5	−13.3 **−13.1**	−13.3 **−13.1**	−13.2 **−13.1**	V min
		Supply = +5V (Note 4)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	V min
			1.5	1.7 **1.9**	1.7 **1.9**	1.8 **1.9**	V max
CMRR	Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	105	86 **80**	86 **82**	80 **78**	dB min
PSRR	Power Supply Rejection Ratio	$\pm 10V \leq V\pm \leq \pm 16V$	96	86 **80**	86 **82**	80 **78**	dB min

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq$ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C. (Continued)

Symbol	Parameter	Conditions	Typ	LM6164	LM6264	LM6364	Units
				Limit (Notes 3, 11)	Limit (Note 3)	Limit (Note 3)	
V_O	Output Voltage Swing	Supply = +5V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **+13.3**	V min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	V min
		Supply = +5V and R_L = 2 kΩ (Note 9)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	V min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	V max
	Output Short Circuit Current	Source	65	30 **20**	30 **25**	30 **25**	mA min
		Sink	65	30 **20**	30 **25**	30 **25**	mA min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA min

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq$ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typ	LM6164 Limit (Notes 3, 11)	LM6264 Limit (Note 3)	LM6364 Limit (Note 3)	Units
GBW	Gain-Bandwidth Product	F = 20 MHz	175	140 **100**	140 **120**	120 **100**	MHz min
		Supply = ±5V	120				
SR	Slew Rate	A_V = +5 (Note 8)	300	200 **180**	200 **180**	200 **180**	V/µs min
		Supply = ±5V	200				
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
T_S	Settling Time	10V Step to 0.1% A_V = −4, R_L = 2 kΩ	100				ns
ϕ_m	Phase Margin	A_V = +5	45				Deg
A_D	Differential Gain	NTSC, A_V = +10	<0.1				%
ϕ_D	Differential Phase	NTSC, A_V = +10	<0.1				Deg
e_{np-p}	Input Noise Voltage	F = 10 kHz	8				nV/√Hz
i_{np-p}	Input Noise Current	F = 10 kHz	1.5				pA/√Hz

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Limits are guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}.

Note 5: $C_L \leq$ 5 pF.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: V_{IN} = 4V step. For supply = ±5V, V_{IN} = 1V step.

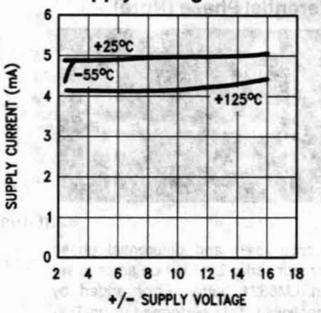
Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Note 10: The voltage between V+ and either input pin must not exceed 36V.

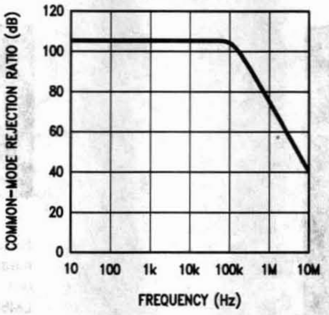
Note 11: A military RETS electrical test specification is available on request. At the time of printing, the LM6164J/883 RETS spec complied with the **Boldface** limits in this column. The LM6164J/883 may also be procured as Standard Military Drawing #5962-8962401PA.

Typical Performance Characteristics (R$_L$ = 10 kΩ, T$_A$ = 25°C unless otherwise specified)

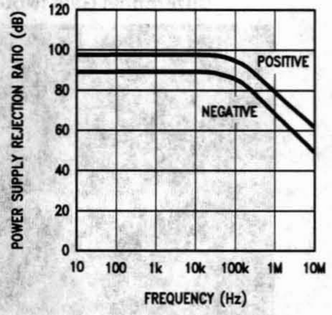
Supply Current vs Supply Voltage



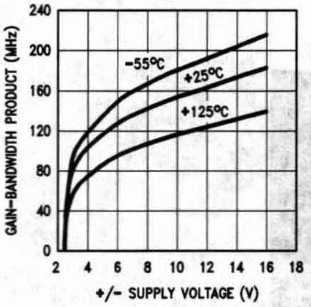
Common-Mode Rejection Ratio



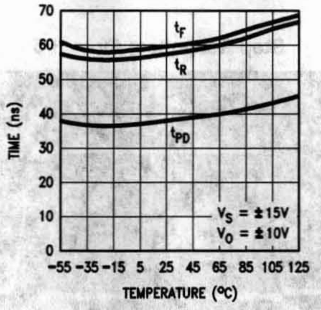
Power Supply Rejection Ratio



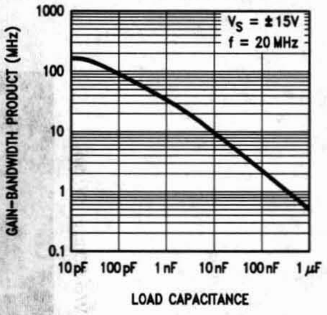
Gain-Bandwidth Product



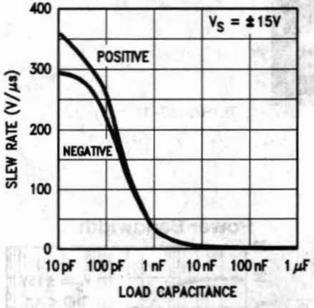
Propagation Delay Rise and Fall Time



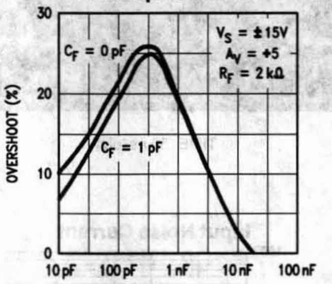
Gain-Bandwidth Product vs Load Capacitance



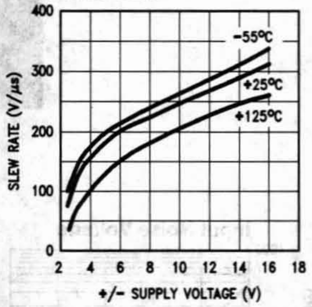
Slew Rate vs Load Capacitance



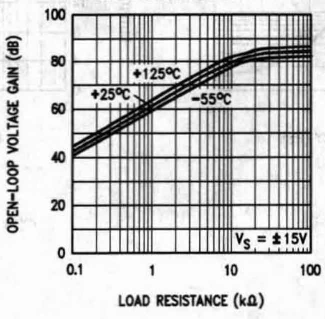
Overshoot vs Load Capacitance



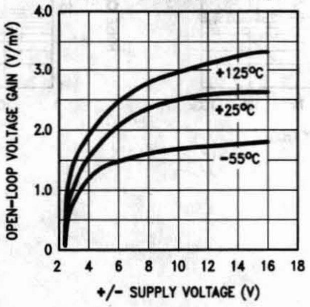
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage

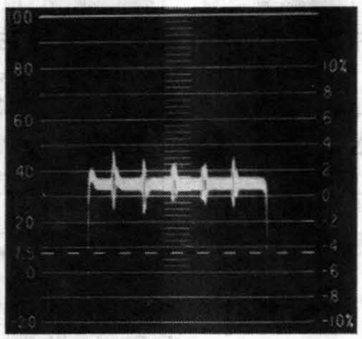


TL/H/9153–5

Typical Performance Characteristics

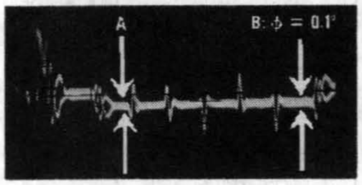
(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



TL/H/9153-6

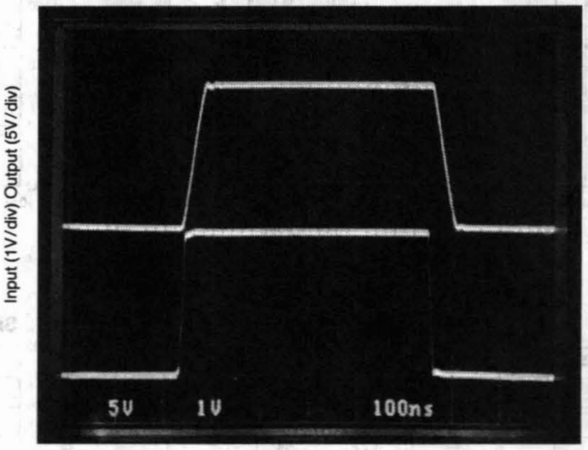
Differential Phase (Note)



TL/H/9153-7

Note: Differential gain and differential phase measured for four series LM6364 op amps in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system. Configured with a gain of +5 (each output attenuated by 80%)

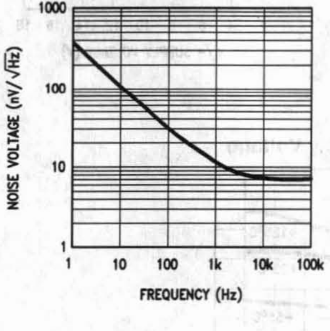
Step Response; Av = +5



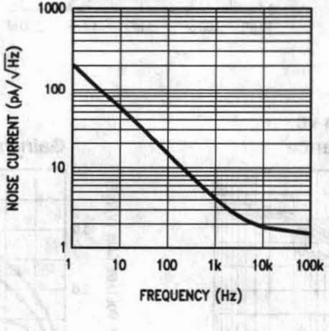
TL/H/9153-1

TIME (50 ns/div)

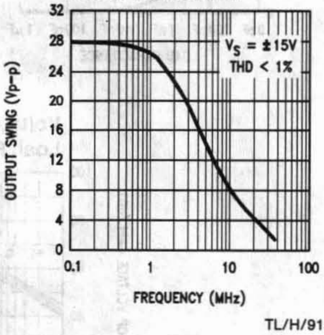
Input Noise Voltage



Input Noise Current



Power Bandwidth

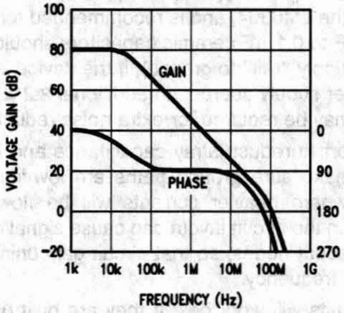


TL/H/9153-9

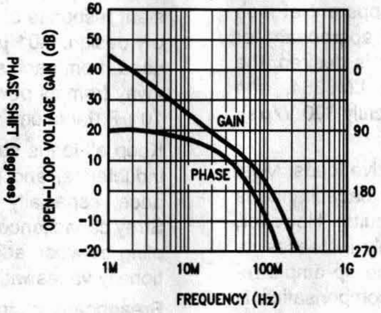
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

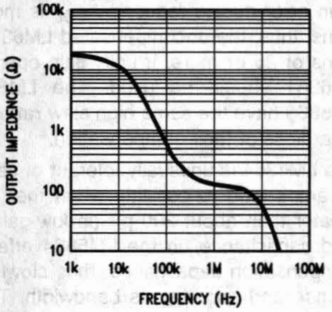
Open-Loop Frequency Response



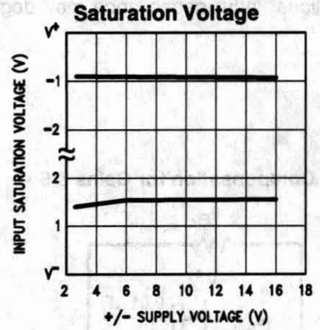
Open-Loop Frequency Response



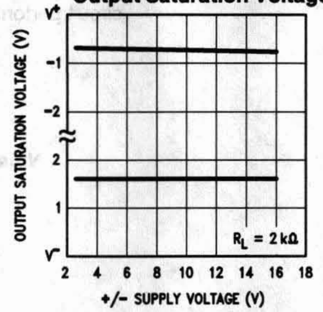
Output Resistance Open-Loop



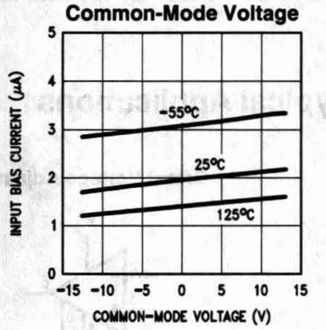
Common-Mode Input Saturation Voltage



Output Saturation Voltage

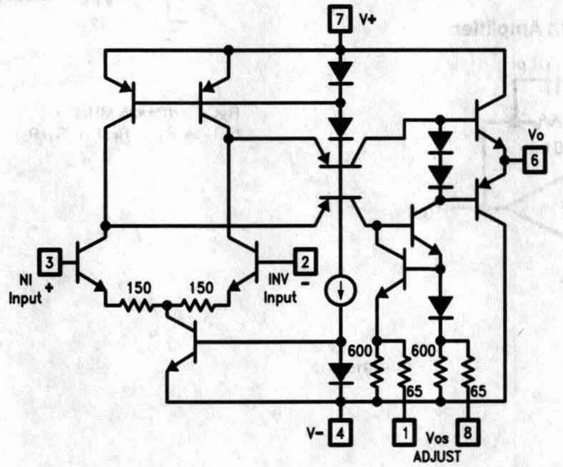


Bias Current vs Common-Mode Voltage



TL/H/9153-13

Simplified Schematic


7 V+
Vo
6
3
NI +
Input
150
150
2
INV −
Input
600
600
65
65
V− 4
1
Vos
8
ADJUST

TL/H/9153-3

Applications Tips

The LM6364 has been compensated for gains of 5 or greater (over specified ranges of temperature, power supply voltage, and load). Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, the uncompensated LM6365 is appropriate for gains of 25 or more. If unity-gain operation is desired, the LM6361 should be used. The LM6361, LM6364, and LM6365 have the same high slew rate (typically 300 V/μs), regardless of their compensation.

The LM6364 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6364 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing or oscillation may occur in low-gain circuits with large capacitive loads. To overcompensate the LM6364 for operation at gains less than 5, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 5.

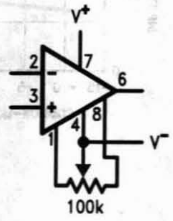
Power supply bypassing will improve the stability and transient response of the LM6364, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, so that circuit gain unintentionally varies with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

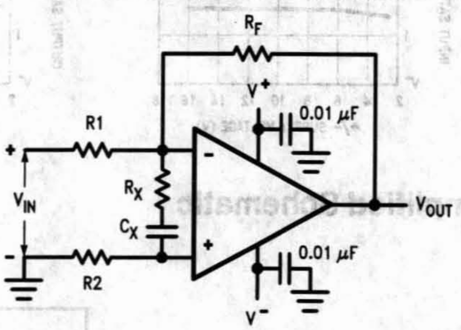
Typical Applications

Offset Voltage Adjustment



TL/H/9153-10

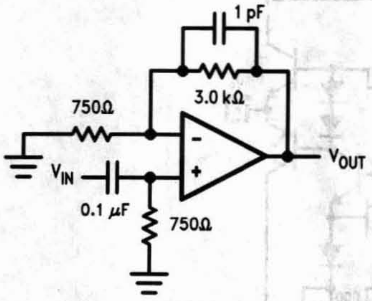
Noise-Gain Compensation for Gains ≤5



TL/H/9153-11

$R_XC_X \geq (2\pi \bullet 25\text{ MHz})^{-1}$
$5\,R_X = R_1 + R_F(1 + R_1/R_2)$

Video-Bandwidth Amplifier



TL/H/9153-12

National Semiconductor

LM6165/LM6265/LM6365 High Speed Operational Amplifier

General Description

The LM6165 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 725 MHz GBW (stable for gains as low as +25) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

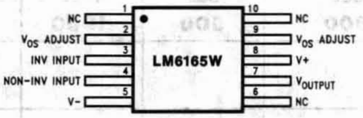
■ High slew rate	300 V/μs
■ High GBW product	725 MHz
■ Low supply current	5 mA
■ Fast settling	80 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	<0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	

Applications

- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams

10-Lead Flatpak
Top View

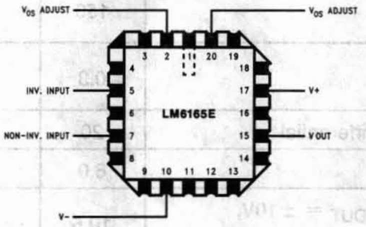


NC
V_OS ADJUST
INV INPUT
NON-INV INPUT
V−
1
2
3
4
5
10
9
8
7
6
LM6165W
NC
V_OS ADJUST
V+
V_OUTPUT
NC

TL/H/9152–14

Order Number LM6165W/883
See NS Package Number W10A

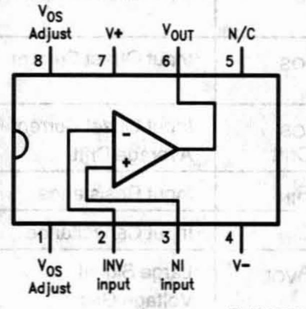
20-Lead LCC
Top View



V_OS ADJUST
V_OS ADJUST
INV. INPUT
NON-INV. INPUT
V−
V+
VOUT
LM6165E
3
2
1
20
19
4
5
6
7
8
18
17
16
15
14
9
10
11
12
13

TL/H/9152–15

Order Number LM6165E/883
See NS Package Number E20A



V_OS Adjust
V+
V_OUT
N/C
8
7
6
5
1
2
3
4
V_OS Adjust
INV Input
NI Input
V−

TL/H/9152–8

Order Number LM6165J/883
See NS Package Number J08A

Order Number LM6365M
See NS Package Number M08A

Order Number LM6265N or LM6365N
See NS Package Number N08E

Temperature Range			Package	NSC Drawing
Military $-55^\circ C \leq T_A \leq +125^\circ C$	Industrial $-25^\circ C \leq T_A \leq +85^\circ C$	Commercial $0^\circ C \leq T_A \leq +70^\circ C$		
	LM6265N	LM6365N	8-Pin Molded DIP	N08E
LM6165J/883 5962-8962501PA			8-Pin Ceramic DIP	J08A
		LM6365M	8-Pin Molded Surface Mt.	M08A
LM6165E/883 5962-89625012A			20-Lead LCC	E20A
LM6165W883 5962-8962501HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 6)	±8V
Common-Mode Voltage Range (Note 10)	(V^+ − 0.7V) to (V^- − 7V)
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	−65°C to +150°C
Max Junction Temperature (Note 2)	150°C
ESD Tolerance (Notes 6 and 7)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6165, LM6165J/883	$-55°C \le T_J \le +125°C$
LM6265	$-25°C \le T_J \le +85°C$
LM6365	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $V_{CM} = 0$, $R_L \ge 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6165 Limit (Notes 3, 11)	LM6265 Limit (Note 3)	LM6365 Limit (Note 3)	Units
V_{OS}	Input Offset Voltage		1	3 **4**	3 **4**	6 **7**	mV Max
V_{OS} Drift	Input Offset Voltage Average Drift		3				μV/°C
I_b	Input Bias Current		2.5	3 **6**	3 **5**	5 **6**	μA Max
I_{OS}	Input Offset Current		150	350 **800**	350 **600**	1500 **1900**	nA Max
I_{OS} Drift	Input Offset Current Average Drift		0.3				nA/°C
R_{IN}	Input Resistance	Differential	20				kΩ
C_{IN}	Input Capacitance		6.0				pF
A_{VOL}	Large Signal Voltage Gain (Note 9)	$V_{OUT} = \pm10V$, $R_L = 2\ k\Omega$	10.5	7.5 **5.0**	7.5 **6.0**	5.5 **5.0**	V/mV Min
		$R_L = 10\ k\Omega$	38				
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	V Min
			−13.6	−13.4 **−13.2**	−13.4 **−13.2**	−13.3 **−13.2**	V Min
		Supply = +5V (Note 4)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	V Min
			1.4	1.6 **1.8**	1.6 **1.8**	1.7 **1.8**	V Max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	102	88 **82**	88 **84**	80 **78**	dB Min
PSRR	Power Supply Rejection Ratio	$\pm10V \le V^{\pm} \le \pm16V$	104	88 **82**	88 **84**	80 **78**	dB Min
V_O	Output Voltage Swing	Supply = ±15V, $R_L = 2\ k\Omega$	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **+13.3**	V Min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	V Min

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq$ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{Max}; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typ	LM6165 Limit (Notes 3, 11)	LM6265 Limit (Note 3)	LM6365 Limit (Note 3)	Units
V_O (Continued)	Output Voltage Swing (Continued)	Supply = +5V R_L = 2 kΩ (Note 4)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	V Min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	V Max
	Output Short Circuit Current	Source	65	30 **20**	30 **25**	30 **25**	mA Min
		Sink	65	30 **20**	30 **25**	30 **25**	mA Min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA Max

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq$ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C. (Note 5)

Symbol	Parameter	Conditions	Typ	LM6165 Limit (Notes 3, 11)	LM6265 Limit (Note 3)	LM6365 Limit (Note 3)	Units
GBW	Gain Bandwidth Product	F = 20 MHz	725	575 **350**	575	500	MHz Min
		Supply = ±5V	500				
SR	Slew Rate	A_V = +25 (Note 8)	300	200 **180**	200	200	V/μs Min
		Supply = ±5V	200				
PBW	Power Bandwidth Product	V_{OUT} = 20 V_{PP}	4.5				MHz
t_S	Settling Time	10V Step to 0.1% A_V = −25, R_L = 2 kΩ	80				ns
ϕ_m	Phase Margin	A_V = +25	45				Deg
A_D	Differential Gain	NTSC, A_V = +25	<0.1				%
ϕ_D	Differential Phase	NTSC, A_V = +25	<0.1				Deg
$e_{np\text{-}p}$	Input Noise Voltage	F = 10 kHz	5				nV/$\sqrt{Hz}$
$i_{np\text{-}p}$	Input Noise Current	F = 10 kHz	1.5				pA/$\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, and the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: All limits guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, V_{CM} = 2.5C, V_{OUT} = 2.5V. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}.

Note 5: $C_L \leq$ 5 pF.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exeeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: V_{IN} = 0.8V step. For supply = ±5V, V_{IN} = 0.2V step.

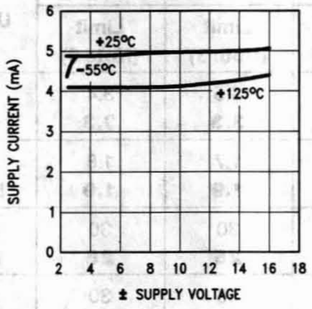
Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Note 10: The voltage between V^+ and either input pin must not exceed 36V.

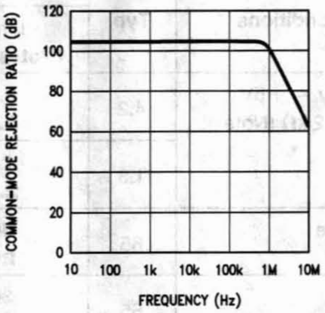
Note 11: A military RETS electrical test specification is available on request. At the time of printing, the LM6165J/883 RETS spec complied with the **Boldface** limits in this column. The LM6165J/883 may also be procured as Standard Military Drawing #5962-8962501PA.

Typical Performance Characteristics $R_L = 10\ k\Omega$, $T_A = 25°C$ unless otherwise specified

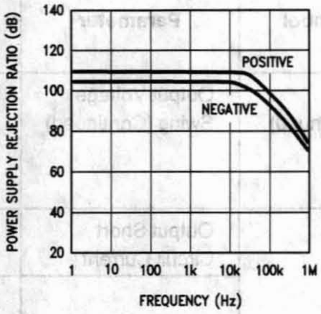
Supply Current vs Supply Voltage



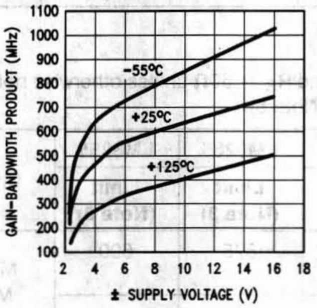
Common-Mode Rejection Ratio



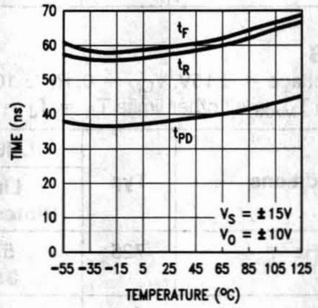
Power Supply Rejection Ratio



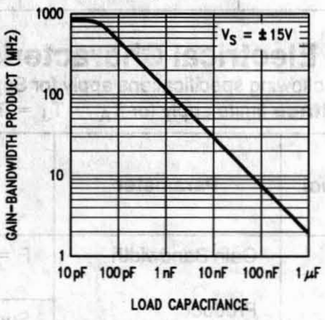
Gain-Bandwidth Product



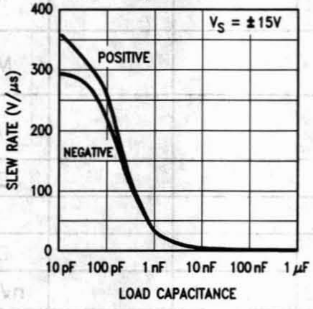
Propagation Delay, Rise and Fall Times



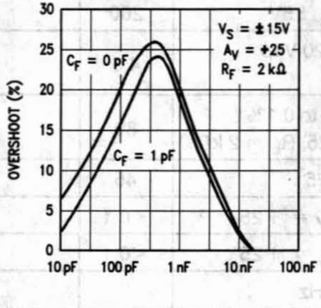
Gain-Bandwidth Product vs Load Capacitance



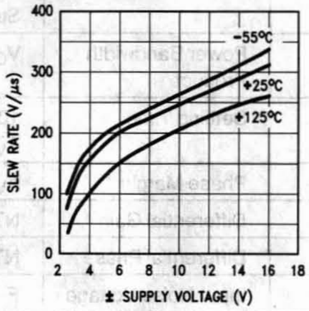
Slew Rate vs Load Capacitance



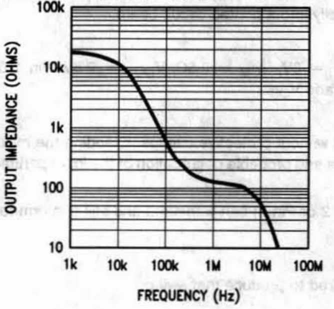
Overshoot vs Capacitive Load



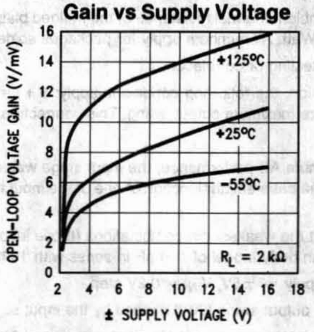
Slew Rate



Output Impedance (Open-Loop)



Gain vs Supply Voltage

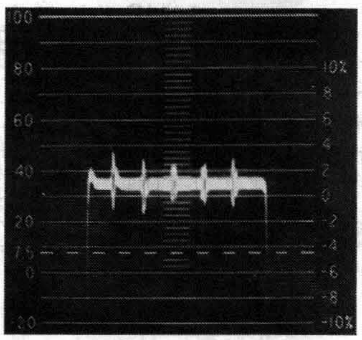


TL/H/9152–5

Typical Performance Characteristics (Continued)

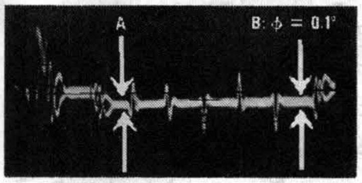
R_L = 10 kΩ, T_A = 25°C unless otherwise specified

Differential Gain (Note)



TL/H/9152-6

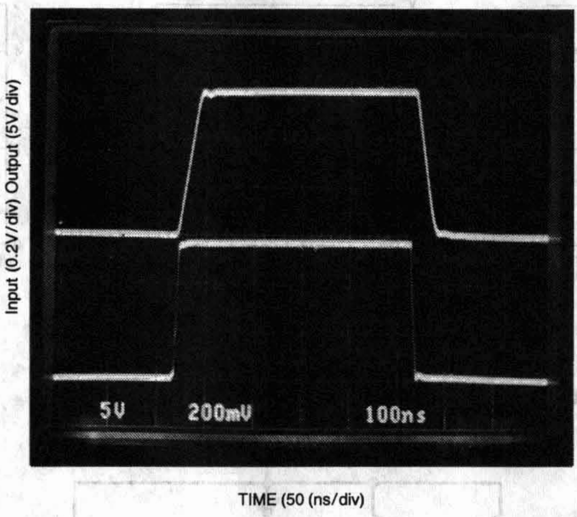
Differential Phase (Note)



TL/H/9152-7

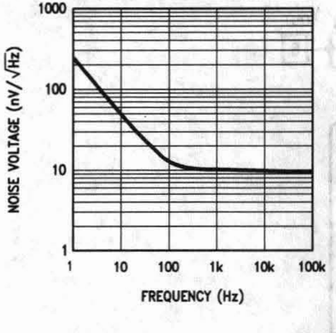
Note: Differential gain and differential phase measured for four series LM6365 op amps configured with gain of +25 (each output attenuated by 96%), in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response; Av = +25

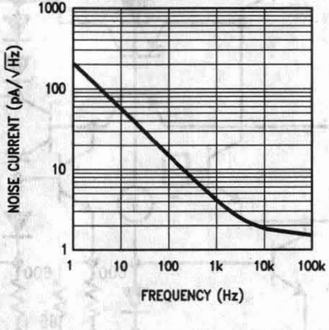


TL/H/9152-1

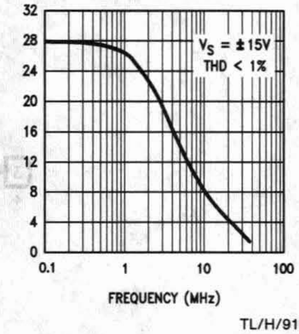
Input Noise Voltage



Input Noise Current



Power Bandwidth

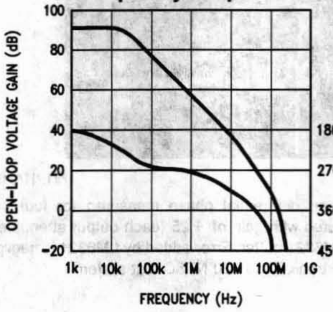


TL/H/9152-9

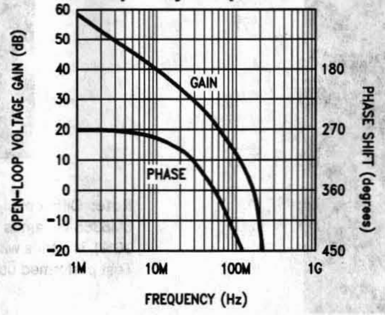
Typical Performance Characteristics (Continued)

R_L = 10 kΩ, T_A = 25°C unless otherwise specified

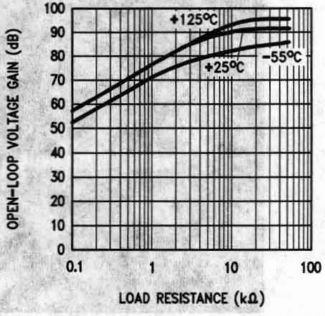
Open-Loop Frequency Response



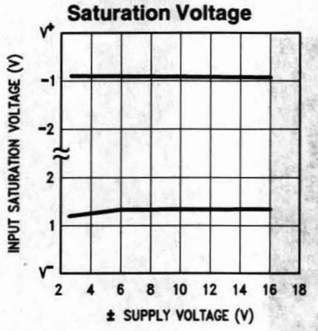
Open-Loop Frequency Response



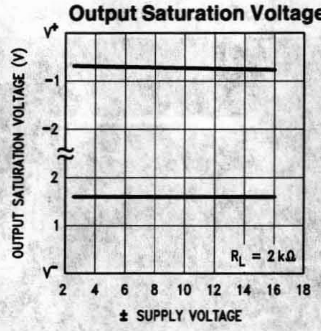
Voltage Gain vs Load Resistance



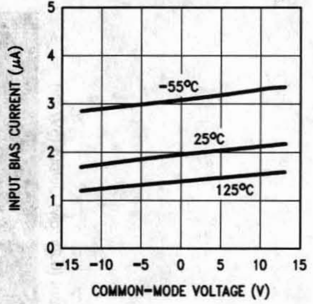
Common-Mode Input Saturation Voltage



Output Saturation Voltage

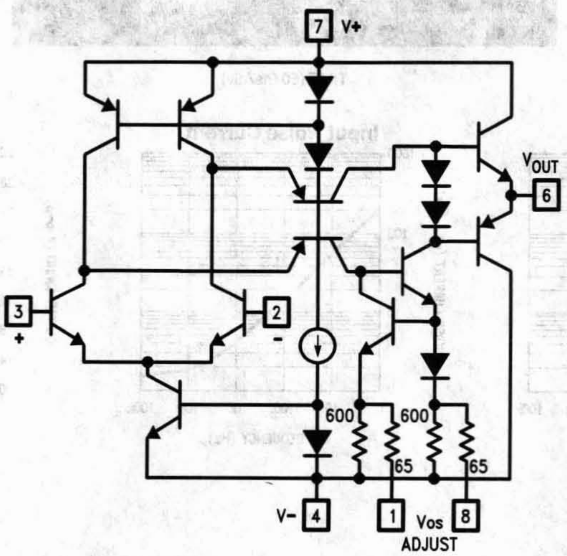


Bias Current vs Common-Mode Voltage



TL/H/9152-10

Simplified Schematic



TL/H/9152-3

Applications Tips

The LM6365 is stable for gains of 25 or greater. The LM6361 and LM6364, specified in separate datasheets, are compensated versions of the LM6365. The LM6361 is unity-gain stable, while the LM6364 is stable for gains as low as 5. The LM6361, and LM6364 have the same high slew rate as the LM6365, typically 300 V/μs.

To use the LM6365 for gains less than 25, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 25.

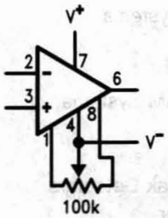
Power supply bypassing will improve stability and transient response of the LM6365, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); an additional 2.2 μF to 10 μF (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

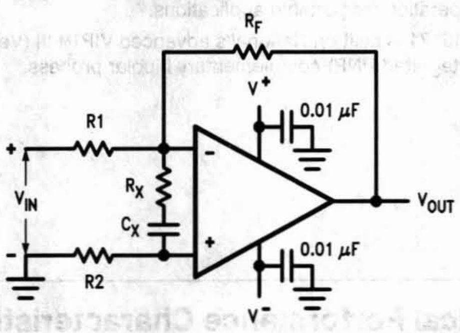
Typical Applications

Offset Voltage Adjustment



TL/H/9152–11

Noise-Gain Compensation



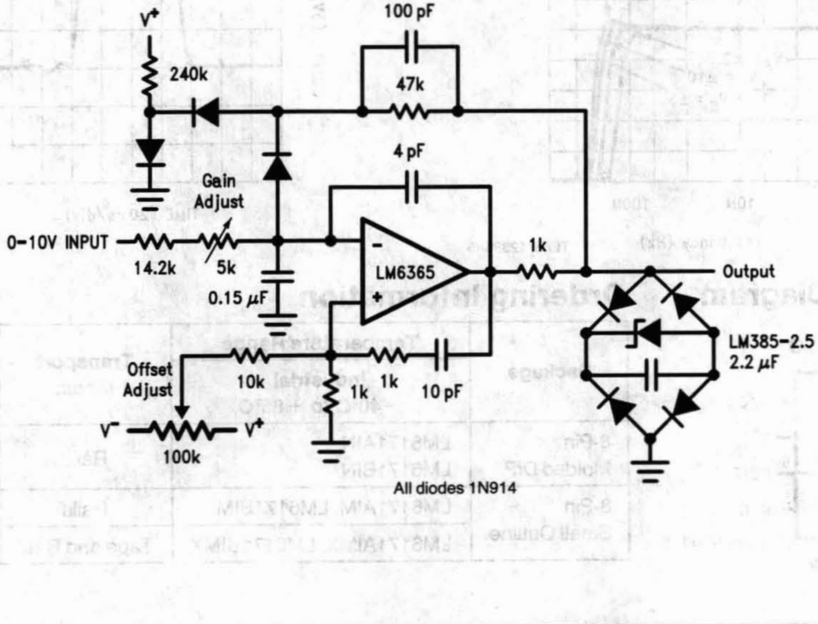
TL/H/9152–12

$R_X C_X \geq 1/(2\pi \bullet 25\ \text{MHz})$

$[R1 + R_F (1 + R1/R2)] = 25\ R_X$

1 MHz Voltage-to-Frequency Converter

($f_{OUT} = 1$ MHz for $V_{IN} = 10V$)



All diodes 1N914

TL/H/9152–13

National Semiconductor

LM6171 High Speed Low Power Low Distortion Voltage Feedback Amplifier

General Description

The LM6171 is a high speed unity-gain stable voltage feedback amplifier. It offers a high slew rate of 3600V/μs and a unity-gain bandwidth of 100 MHz while consuming only 2.5 mA of supply current. The LM6171 has very impressive AC and DC performance which is a great benefit for high speed signal processing and video applications.

The ±15V power supplies allow for large signal swings and give greater dynamic range and signal-to-noise ratio. The LM6171 has high output current drive, low SFDR and THD, ideal for ADC/DAC systems. The LM6171 is specified for ±5V operation for portable applications.

The LM6171 is built on National's advanced VIP™ III (Vertically Integrated PNP) complementary bipolar process.

Features (Typical Unless Otherwise Noted)

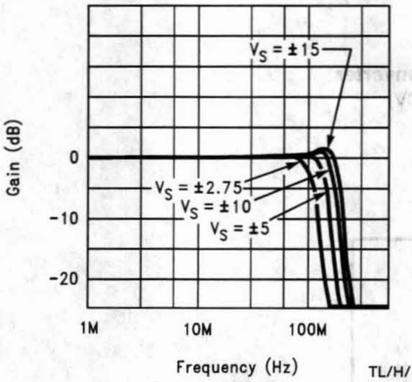
■ Easy-To-Use Voltage Feedback Topology	
■ Very High Slew Rate	3600V/μs
■ Wide Unity-Gain-Bandwidth Product	100 MHz
■ −3 dB Frequency @ $A_V = +2$	62 MHz
■ Low Supply Current	2.5 mA
■ High CMRR	110 dB
■ High Open Loop Gain	90 dB
■ Specified for ±15V and ±5V Operation	

Applications

- Multimedia Broadcast Systems
- Line Drivers, Switchers
- Video Amplifiers
- NTSC, PAL® and SECAM Systems
- ADC/DAC Buffers
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- Instrumentation Amplifier
- Active Filters

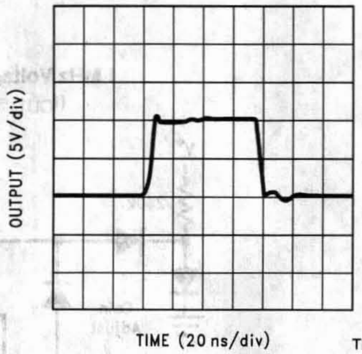
Typical Performance Characteristics

Closed Loop Frequency Response vs Supply Voltage ($A_V = +1$)



TL/H/12336-5

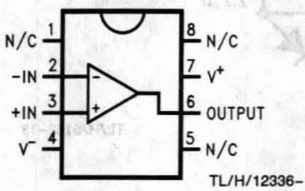
Large Signal Pulse Response $A_V = +1, V_S = \pm 15$



TL/H/12336-9

Connection Diagram

8-Pin DIP/SO



TL/H/12336-1

Top View

Ordering Information

Package	Temperature Range Industrial −40°C to +85°C	Transport Media	NSC Drawing
8-Pin Molded DIP	LM6171AIN LM6171BIN	Rails	N08E
8-Pin Small Outline	LM6171AIM, LM6171BIM	Rails	M08A
	LM6171AIMX, LM6171BIMX	Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2.5 kV
Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 11)	±10V
Common-Mode Voltage Range	$V^+ - 1.4V$ to $V^- + 1.4V$
Output Short Circuit to Ground (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.75V \le V^+ \le 18V$
Junction Temperature Range	
LM6171AI, LM6171BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	108°C/W
M Package, 8-Pin Surface Mount	172°C/W

±15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = +15V$, $V^- = -15V$, $V_{CM} = 0V$, and $R_L = 1\ k\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6171AI Limit (Note 6)	LM6171BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1.5	3 **5**	6 **8**	mV max
TC V_{OS}	Input Offset Voltage Average Drift		6			μV/°C
I_B	Input Bias Current		1	3 **4**	3 **4**	μA max
I_{OS}	Input Offset Current		0.03	2 **3**	2 **3**	μA max
R_{IN}	Input Resistance	Common Mode	40			MΩ
		Differential Mode	4.9			
R_O	Open Loop Output Resistance		14			Ω
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	110	80 **75**	75 **70**	dB min
PSRR	Power Supply Rejection Ratio	$V_S = \pm 15V - \pm 5V$	95	85 **80**	80 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 60 dB	±13.5			V
A_V	Large Signal Voltage Gain (Note 7)	$R_L = 1\ k\Omega$	90	80 **70**	80 **70**	dB min
		$R_L = 100\Omega$	83	70 **60**	70 **60**	dB min
V_O	Output Swing	$R_L = 1\ k\Omega$	13.3	12.5 **12**	12.5 **12**	V min
			−13.3	−12.5 **−12**	−12.5 **−12**	V max
		$R_L = 100\Omega$	11.6	9 **8.5**	9 **8.5**	V min
			−10.5	−9 **−8.5**	−9 **−8.5**	V max

±15V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = +15V$, $V^- = -15V$, $V_{CM} = 0V$, and $R_L = 1\ k\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6171AI Limit (Note 6)	LM6171BI Limit (Note 6)	Units
	Continuous Output Current (Open Loop) (Note 8)	Sourcing, $R_L = 100\Omega$	116	90 **85**	90 **85**	mA min
		Sinking, $R_L = 100\Omega$	105	90 **85**	90 **85**	mA max
	Continuous Output Current (in Linear Region)	Sourcing, $R_L = 10\Omega$	100			mA
		Sinking, $R_L = 10\Omega$	80			mA
I_{SC}	Output Short Circuit Current	Sourcing	135			mA
		Sinking	135			mA
I_S	Supply Current		2.5	4 **4.5**	4 **4.5**	mA max

±15V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = +15V$, $V^- = -15V$, $V_{CM} = 0V$, and $R_L = 1\ k\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6171AI Limit (Note 6)	LM6171BI Limit (Note 6)	Units
SR	Slew Rate (Note 9)	$A_V = +2$, $V_{IN} = 13\ V_{PP}$	3600			$V/\mu s$
		$A_V = +2$, $V_{IN} = 10\ V_{PP}$	3000			
GBW	Unity Gain-Bandwidth Product		100			MHz
	−3 dB Frequency	$A_V = +1$	160			MHz
		$A_V = +2$	62			MHz
ϕm	Phase Margin		40			deg
t_s	Settling Time (0.1%)	$A_V = -1$, $V_{OUT} = \pm 5V$ $R_L = 500\Omega$	35			ns
	Propagation Delay	$V_{IN} = \pm 5V$, $R_L = 500\Omega$, $A_V = -2$	6			ns
A_D	Differential Gain (Note 10)		0.03			%
ϕ_D	Differential Phase (Note 10)		0.5			deg
e_n	Input-Referred Voltage Noise	f = 1 kHz	12			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	1			$\frac{pA}{\sqrt{Hz}}$

±5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = +5V$, $V^- = -5V$, $V_{CM} = 0V$, and $R_L = 1\ k\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6171AI Limit (Note 6)	LM6171BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1.2	3 **5**	6 **8**	mV max
TC V_{OS}	Input Offset Voltage Average Drift		4			μV/°C
I_B	Input Bias Current		1	2.5 **3.5**	2.5 **3.5**	μA max
I_{OS}	Input Offset Current		0.03	1.5 **2.2**	1.5 **2.2**	μA max
R_{IN}	Input Resistance	Common Mode	40			MΩ
		Differential Mode	4.9			
R_O	Open Loop Output Resistance		14			Ω
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 2.5V$	105	80 **75**	75 **70**	dB min
PSRR	Power Supply Rejection Ratio	$V_S = \pm 15V$ to $\pm 5V$	95	85 **80**	80 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 60 dB	±3.7			V
A_V	Large Signal Voltage Gain (Note 7)	$R_L = 1\ k\Omega$	84	75 **65**	75 **65**	dB min
		$R_L = 100\Omega$	80	70 **60**	70 **60**	dB min
V_O	Output Swing	$R_L = 1\ k\Omega$	3.5	3.2 **3**	3.2 **3**	V min
			−3.4	−3.2 **−3**	−3.2 **−3**	V max
		$R_L = 100\Omega$	3.2	2.8 **2.5**	2.8 **2.5**	V min
			−3.0	−2.8 **−2.5**	−2.8 **−2.5**	V max
	Continuous Output Current (Open Loop) (Note 8)	Sourcing, $R_L = 100\Omega$	32	28 **25**	28 **25**	mA min
		Sinking, $R_L = 100\Omega$	30	28 **25**	28 **25**	mA max
I_{SC}	Output Short Circuit Current	Sourcing	130			mA
		Sinking	100			mA
I_S	Supply Current		2.3	3 **3.5**	3 **3.5**	mA max

±5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = +5V$, $V^- = -5V$, $V_{CM} = 0V$, and $R_L = 1\ k\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6171AI Limit (Note 6)	LM6171BI Limit (Note 6)	Units
SR	Slew Rate (Note 9)	$A_V = +2$, $V_{IN} = 3.5\ V_{PP}$	750			V/μs
GBW	Unity Gain-Bandwidth Product		70			MHz
	−3 dB Frequency	$A_V = +1$	130			MHz
		$A_V = +2$	45			
ϕm	Phase Margin		57			deg
t_s	Settling Time (0.1%)	$A_V = -1$, $V_{OUT} = +1V$, $R_L = 500\Omega$	48			ns
	Propagation Delay	$V_{IN} = \pm 1V$, $R_L = 500\Omega$, $A_V = -2$	8			ns
A_D	Differential Gain (Note 10)		0.04			%
ϕ_D	Differential Phase (Note 10)		0.7			deg
e_n	Input-Referred Voltage Noise	f = 1 kHz	11			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	1			$\frac{pA}{\sqrt{Hz}}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For $V_S = \pm 15V$, $V_{OUT} = \pm 5V$. For $V_S = +5V$, $V_{OUT} = \pm 1V$.

Note 8: The open loop output current is the output swing with the 100Ω load resistor divided by that resistor.

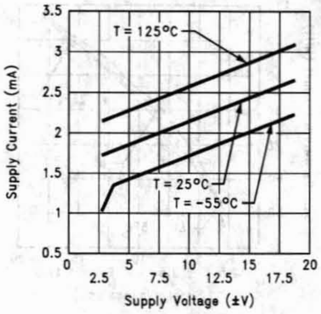
Note 9: Slew rate is the average of the rising and falling slew rates.

Note 10: Differential gain and phase are measured with $A_V = +2$, $V_{IN} = 1\ V_{PP}$ at 3.58 MHz and both input and output 75Ω terminated.

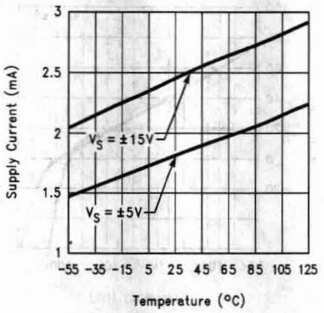
Note 11: Differential input voltage is measured at $V_S = \pm 15V$.

Typical Performance Characteristics Unless otherwise noted, $T_A = 25°C$

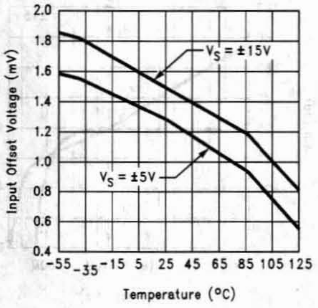
Supply Current vs Supply Voltage



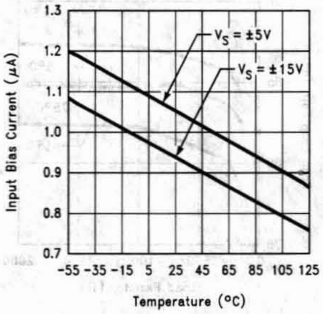
Supply Current vs Temperature



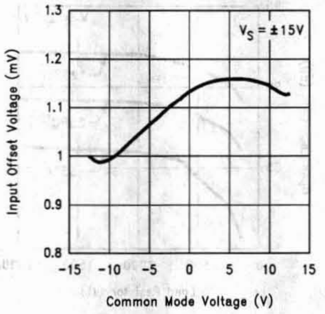
Input Offset Voltage vs Temperature



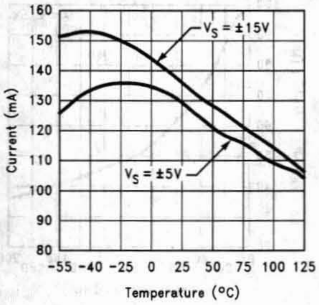
Input Bias Current vs Temperature



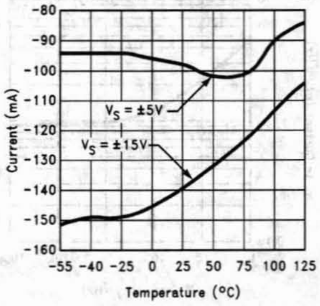
Input Offset Voltage vs Common Mode Voltage



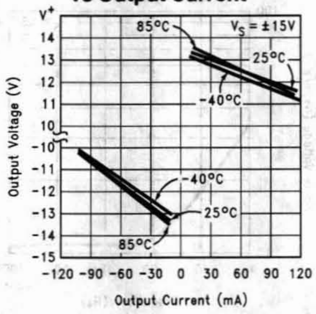
Short Circuit Current vs Temperature (Sourcing)



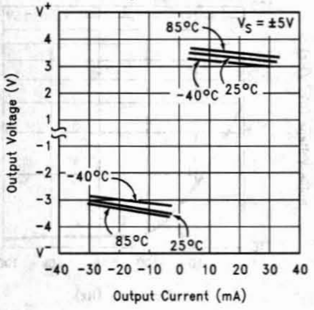
Short Circuit Current vs Temperature (Sinking)



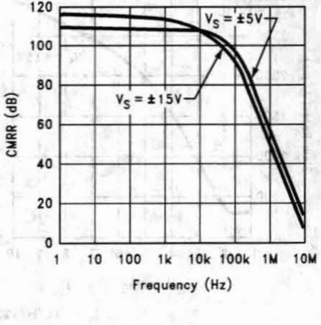
Output Voltage vs Output Current



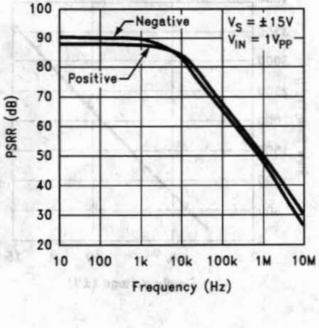
Output Voltage vs Output Current



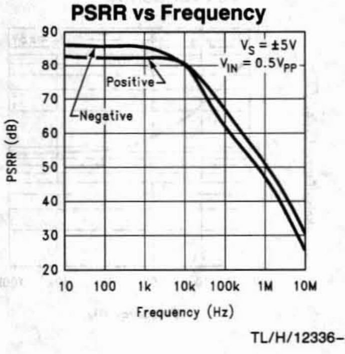
CMRR vs Frequency



PSRR vs Frequency

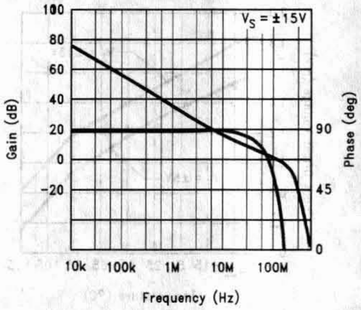


PSRR vs Frequency

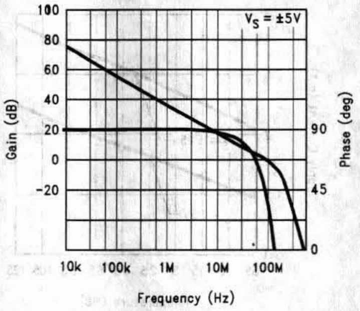


TL/H/12336–3

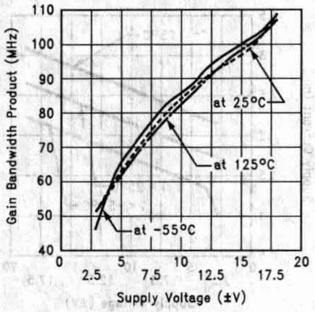
Typical Performance Characteristics Unless otherwise noted, $T_A = 25°C$ (Continued)



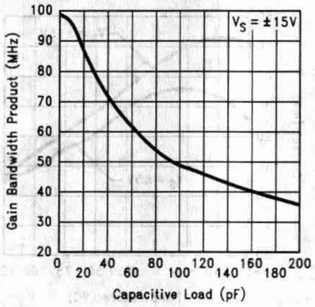
Open Loop Frequency Response



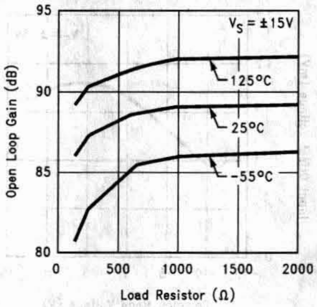
Open Loop Frequency Response



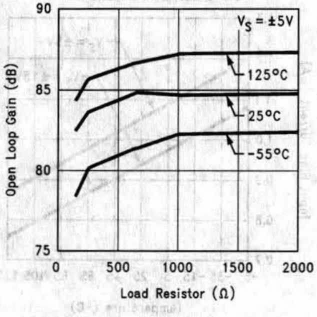
Gain Bandwidth Product vs Supply Voltage



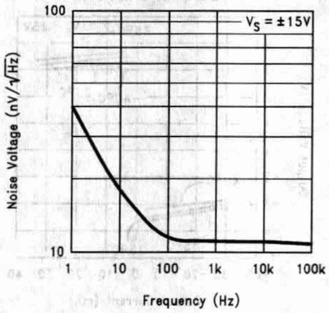
Gain Bandwidth Product vs Load Capacitance



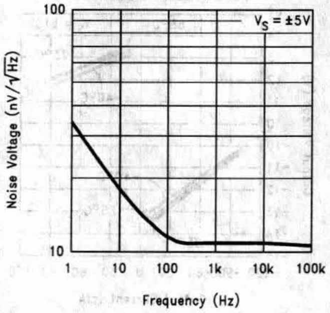
Large Signal Voltage Gain vs Load



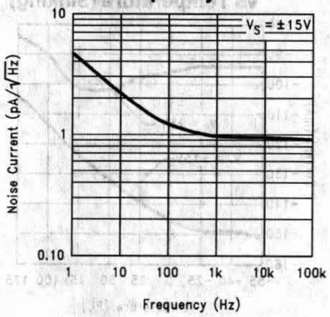
Large Signal Voltage Gain vs Load



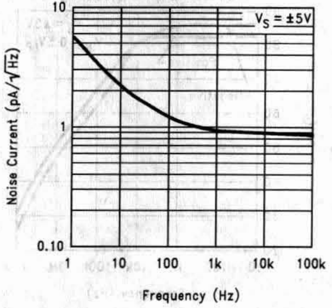
Input Voltage Noise vs Frequency



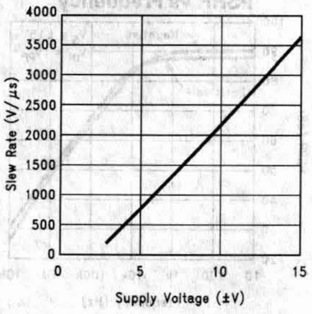
Input Voltage Noise vs Frequency



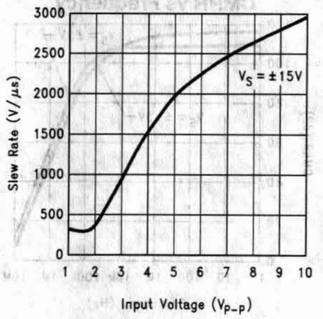
Input Current Noise vs Frequency



Input Current Noise vs Frequency



Slew Rate vs Supply Voltage



Slew Rate vs Input Voltage

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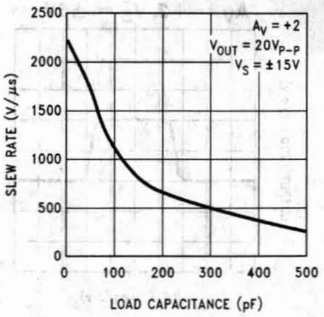
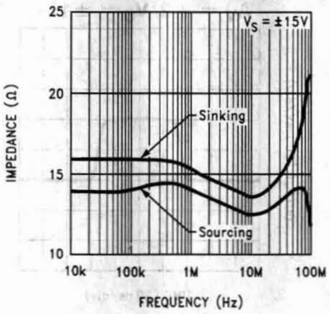
Typical Performance Characteristics Unless otherwise noted, T_A = 25°C (Continued)

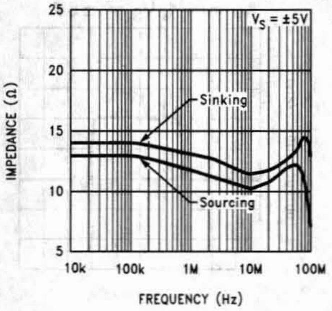
Slew Rate vs Load Capacitance



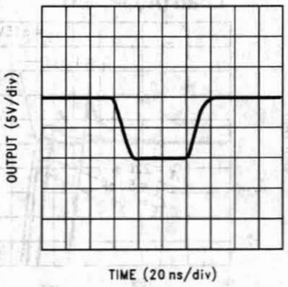
Open Loop Output Impedance vs Frequency



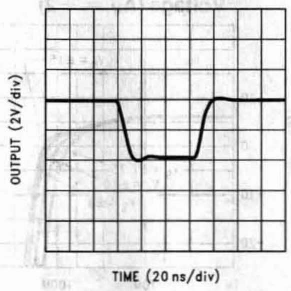
Open Loop Output Impedance vs Frequency



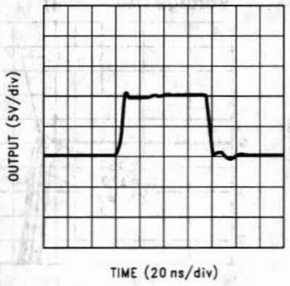
Large Signal Pulse Response $A_V = -1, V_S = \pm 15V$



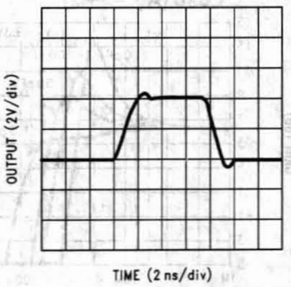
Large Signal Pulse Response $A_V = -1, V_S = \pm 5V$



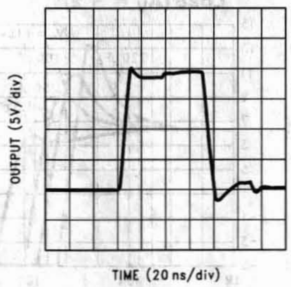
Large Signal Pulse Response $A_V = +1, V_S = \pm 15V$



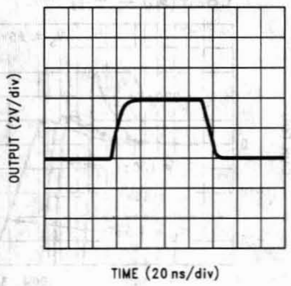
Large Signal Pulse Response $A_V = +1, V_S = \pm 5V$



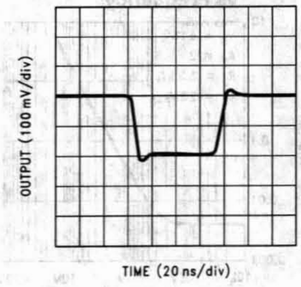
Large Signal Pulse Response $A_V = +2, V_S = \pm 15V$



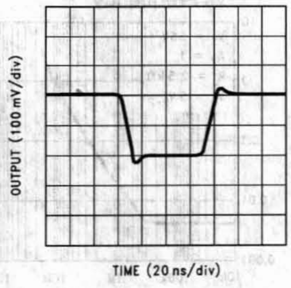
Large Signal Pulse Response $A_V = +2, V_S = \pm 5V$



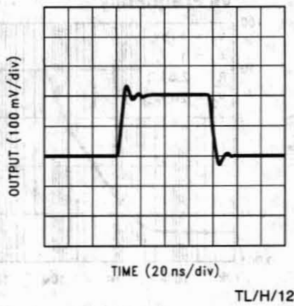
Small Signal Pulse Response $A_V = -1, V_S = \pm 15V$



Small Signal Pulse Response $A_V = -1, V_S = \pm 5V$



Small Signal Pulse Response $A_V = +1, V_S = \pm 15V$



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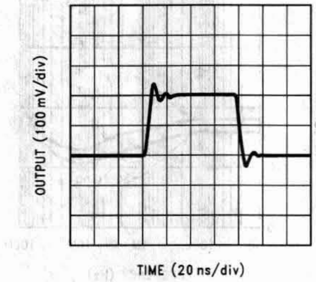
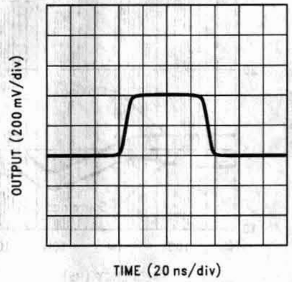
Typical Performance Characteristics Unless otherwise noted, T_A = 25°C (Continued)

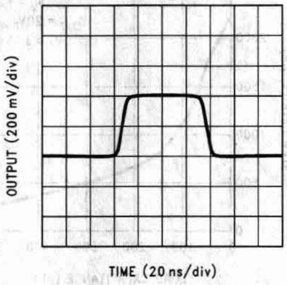
Small Signal Pulse Response A_V = +1, V_S = ±5V



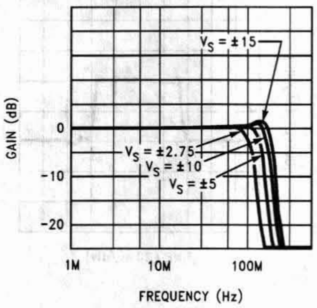
Small Signal Pulse Response A_V = +2, V_S = ±15V



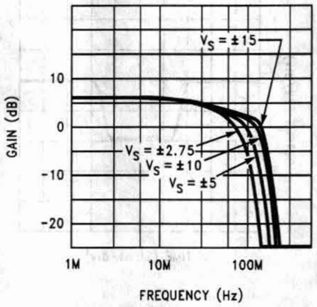
Small Signal Pulse Response A_V = +2, V_S = ±5V



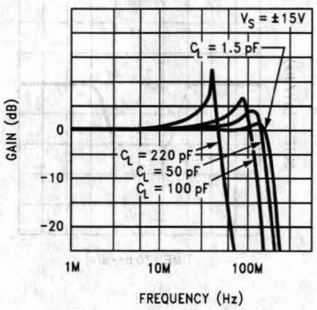
Closed Loop Frequency Response vs Supply Voltage (A_V = +1)



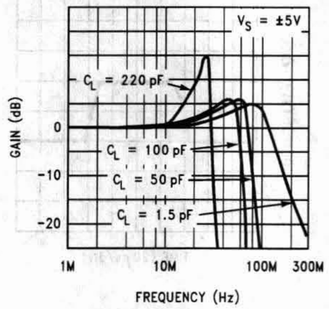
Closed Loop Frequency Response vs Supply Voltage (A_V = +2)



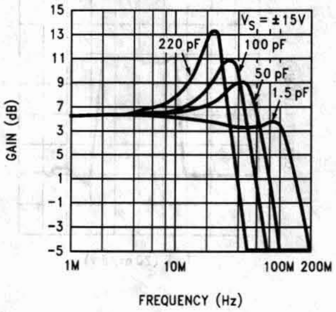
Closed Loop Frequency Response vs Capacitive Load (A_V = +1)



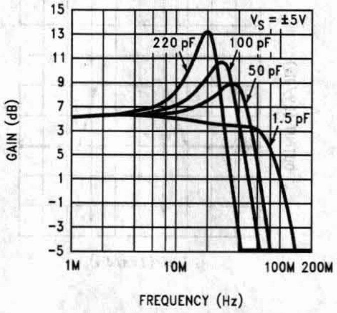
Closed Loop Frequency Response vs Capacitive Load (A_V = +1)



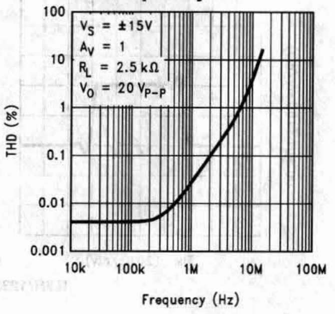
Closed Loop Frequency Response vs Capacitive Load (A_V = +2)



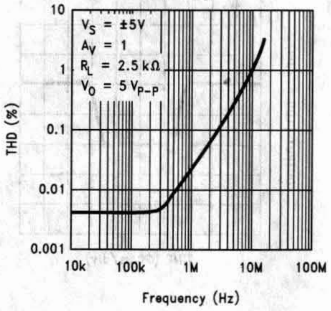
Closed Loop Frequency Response vs Capacitive Load (A_V = +2)



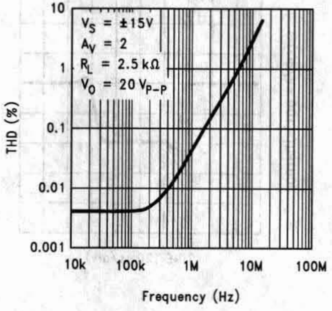
Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency



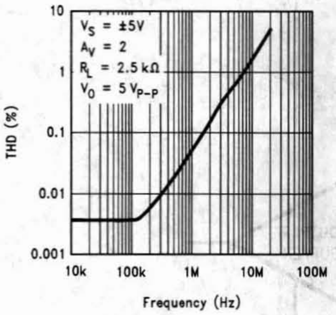
Total Harmonic Distortion vs Frequency



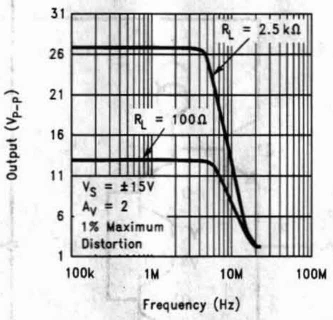
TL/H/12336–7

Typical Performance Characteristics Unless otherwise noted, $T_A = 25°C$ (Continued)

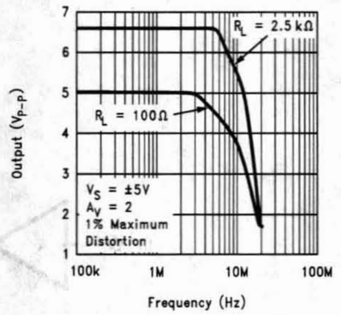
Total Harmonic Distortion vs Frequency



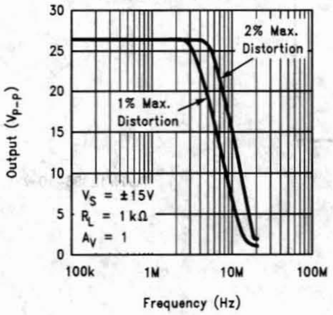
Undistorted Output Swing vs Frequency



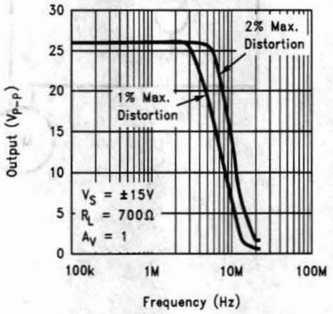
Undistorted Output Swing vs Frequency



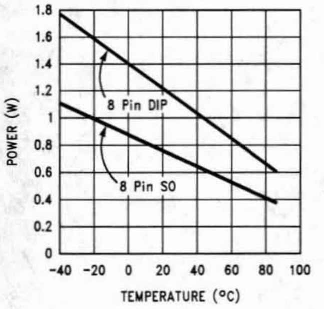
Undistorted Output Swing vs Frequency



Undistorted Output Swing vs Frequency



Total Power Dissipation vs Ambient Temperature



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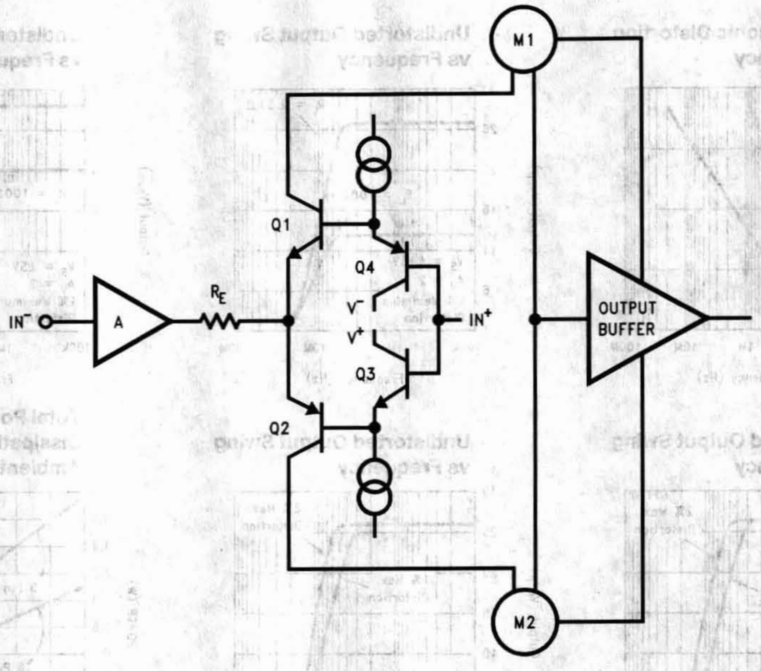
LM6171 Simplified Schematic


M1
Q1
Q4
V⁻
V⁺
Q3
Q2
IN⁻
A
R_E
IN⁺
OUTPUT BUFFER
M2

TL/H/12336-10

Application Information

LM6171 Performance Discussion

The LM6171 is a high speed, unity-gain stable voltage feedback amplifier. It consumes only 2.5 mA supply current while providing a gain-bandwidth product of 100 MHz and a slew rate of 3600V/µs. It also has other great features such as low differential gain and phase and high output current. The LM6171 is a good choice in high speed circuits.

The LM6171 is a true voltage feedback amplifier. Unlike current feedback amplifiers (CFAs) with a low inverting input impedance and a high non-inverting input impedance, both inputs of voltage feedback amplifiers (VFAs) have high impedance nodes. The low impedance inverting input in CFAs will couple with feedback capacitor and cause oscillation. As a result, CFAs cannot be used in traditional op amp circuits such as photodiode amplifiers, I-to-V converters and integrators.

LM6171 Circuit Operation

The class AB input stage in LM6171 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM6171 Simplfied Schematic, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

LM6171 Slew Rate Characteristic

The slew rate of LM6171 is determined by the current available to charge and discharge an internal high impedance node capacitor. The current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor such as 1 kΩ to the input of LM6171, the bandwidth is reduced to help lower the overshoot.

Layout Consideration

PRINTED CIRCUIT BOARDS AND HIGH SPEED OP AMPS

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy and frustrating to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

USING PROBES

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

COMPONENTS SELECTION AND FEEDBACK RESISTOR

It is important in high speed applications to keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For LM6171, a feedback resistor of 510Ω gives optimal performance.

Compensation for Input Capacitance

The combination of an amplifier's input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F$$

can be used to cancel that pole. For LM6171, a feedback capacitor of 2 pF is recommended. *Figure 1* illustrates the compensation circuit.

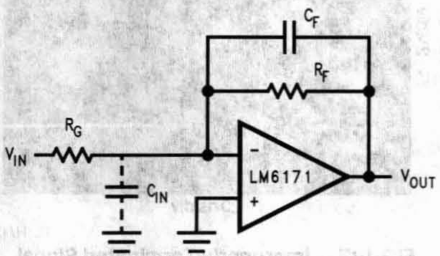


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FIGURE 1. Compensating for Input Capacitance

Power Supply Bypassing

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01 µF ceramic capacitors directly to power supply pins and 2.2 µF tantalum capacitors close to the power supply pins.

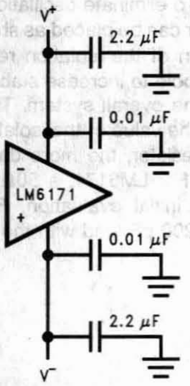

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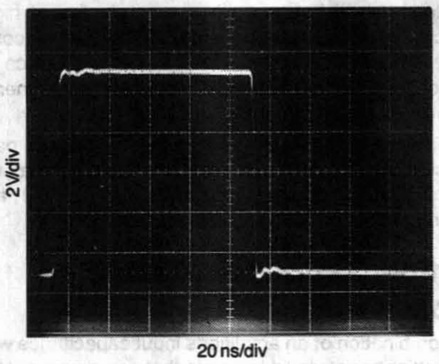
FIGURE 2. Power Supply Bypassing

Application Information (Continued)

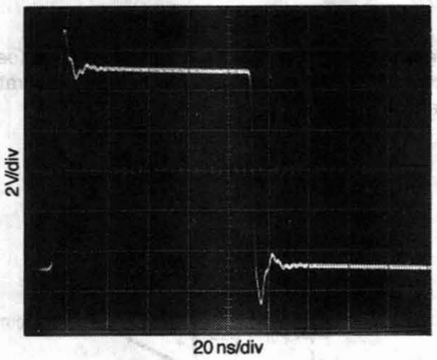
Termination

In high frequency applications, reflections occur if signals are not properly terminated. *Figure 3* shows a properly terminated signal while *Figure 4* shows an improperly terminated signal.



TL/H/12336–14

FIGURE 3. Properly Terminated Signal



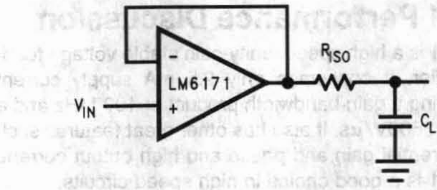
TL/H/12336–15

FIGURE 4. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

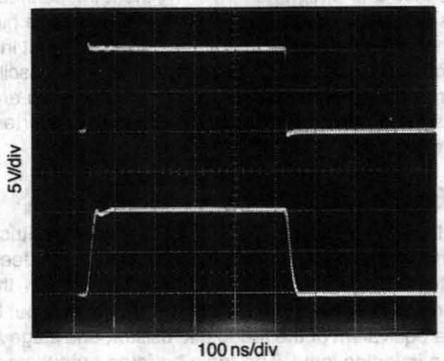
Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown below in *Figure 5.* The combination of the isolation resistor and the load capacitor forms a pole to increase stablility by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM6171, a 50Ω isolation resistor is recommended for initial evaluation. *Figure 6* shows the LM6171 driving a 200 pF load with the 50Ω isolation resistor.



TL/H/12336–13

FIGURE 5. Isolation Resistor Used to Drive Capacitive Load



TL/H/12336–16

FIGURE 6. The LM6171 Driving a 200 pF Load with a 50Ω Isolation Resistor

Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A)/\theta_{JA}$$

Where P_D is the power dissipation in a device

$T_{J(max)}$ is the maximum junction temperature

T_A is the ambient temperature

θ_{JA} is the thermal resistance of a particular package

For example, for the LM6171 in a SO-8 package, the maximum power dissipation at 25°C ambient temperature is 730 mW.

Thermal resistance, θ_{JA}, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher θ_{JA} becomes. The 8-pin DIP package has a lower thermal resistance (108°C/W) than that of 8-pin SO (172°C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L$$

P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

P_Q = supply current × total supply voltage with no load

P_L = output current × (voltage difference between supply voltage and output voltage of the same supply)

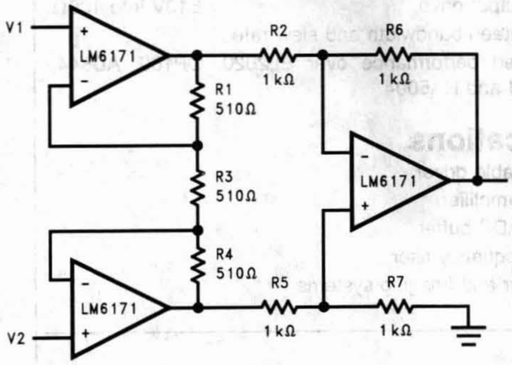
Application Information (Continued)

For example, the total power dissipated by the LM6171 with $V_S = \pm 15V$ and output voltage of 10V into 1 kΩ load resistor (one end tied to ground) is

$$\begin{aligned} P_D &= P_Q + P_L \\ &= (2.5\ mA) \times (30V) + (10\ mA) \times (15V - 10V) \\ &= 75\ mW + 50\ mW \\ &= 125\ mW \end{aligned}$$

Application Circuits

Fast Instrumentation Amplifier



V1
+
LM6171
−
R2
1 kΩ
R6
1 kΩ
R1
510Ω
R3
510Ω
−
LM6171
+
V_OUT
R4
510Ω
−
LM6171
+
V2
R5
1 kΩ
R7
1 kΩ

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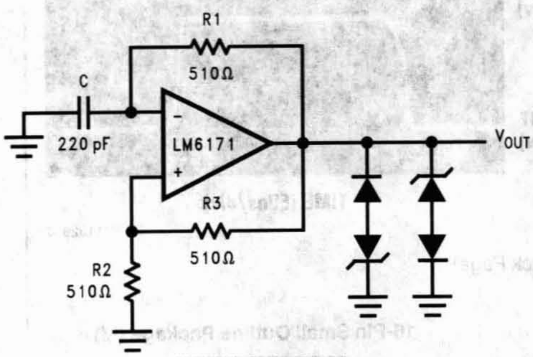
$V_{IN} = V2 - V1$

if R6 = R2, R7 = R5 and R1 = R4

$$\frac{V_{OUT}}{V_{IN}} = \frac{R6}{R2}\left(1 + 2\frac{R1}{R3}\right) = 3$$

Multivibrator



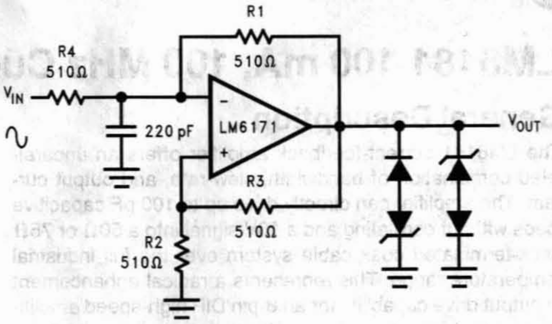
R1
510Ω
C
220 pF
−
LM6171
+
V_OUT
R3
510Ω
R2
510Ω

TL/H/12336–18

$$f = \frac{1}{2\left(R1C \ln\left(1 + 2\frac{R2}{R3}\right)\right)}$$

f = 4 MHz

Pulse Width Modulator



R1
510Ω
R4
510Ω
V_IN
220 pF
−
LM6171
+
V_OUT
R3
510Ω
R2
510Ω

TL/H/12336–19

Design Kit

A design kit is available for the LM6171. The design kit contains:

- High Speed Evaluation Board
- LM6171 in 8-pin DIP Package
- LM6171 Datasheet
- Pspice Macromodel Diskette With the LM6171 Macromodel
- An Amplifier Selection Guide

Pitch Pack

A pitch pack is available for the LM6171. The pitch pack contains:

- High Speed Evaluation Board
- LM6171 in 8-pin DIP Package
- LM6171 Datasheet
- Pspice Macromodel Diskette With the LM6171 Macromodel

Contact your local National Semiconductor sales office to obtain a pitch pack.

National Semiconductor

LM6181 100 mA, 100 MHz Current Feedback Amplifier

General Description

The LM6181 current-feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. The amplifier can directly drive up to 100 pF capacitive loads without oscillating and a 10V signal into a 50Ω or 75Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for an 8-pin DIP high-speed amplifier making it ideal for video applications.

Built on National's advanced high-speed VIP™ II (Vertically Integrated PNP) process, the LM6181 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at $A_V = -1$, 60 MHz at $A_V = -10$. With a slew rate of 2000V/μs, 2nd harmonic distortion of −50 dBc at 10 MHz and settling time of 50 ns (0.1%) the LM6181 dynamic performance makes it ideal for data acquisition, high speed ATE, and precision pulse amplifier applications.

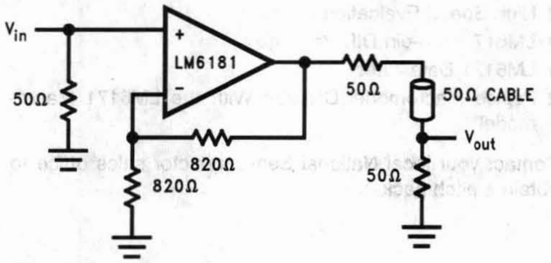
Features (Typical unless otherwise noted)

■ Slew rate	2000 V/μs
■ Settling time (0.1%)	50 ns
■ Characterized for supply ranges	±5V and ±15V
■ Low differential gain and phase error	0.05%, 0.04°
■ High output drive	±10V into 100Ω
■ Guaranteed bandwidth and slew rate	
■ Improved performance over EL2020, OP160, AD844, LT1223 and HA5004	

Applications

- Coax cable driver
- Video amplifier
- Flash ADC buffer
- High frequency filter
- Scanner and Imaging systems

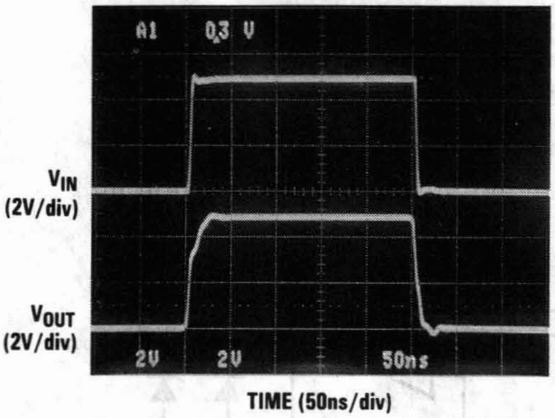
Typical Application



V_{in}
50Ω
+
−
LM6181
50Ω
50Ω CABLE
V_{out}
820Ω
820Ω
50Ω

TL/H/11328–1

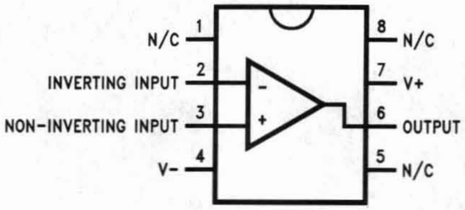
Cable Driver



TL/H/11328–2

Connection Diagrams (For Ordering Information See Back Page)

8-Pin Dual-In-Line Package (N)/ Small Outline (M-8)

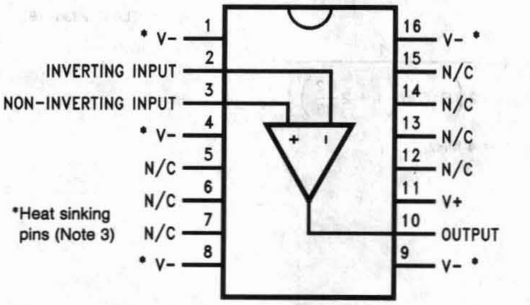


N/C 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
V− 4
8 N/C
7 V+
6 OUTPUT
5 N/C
−
+

TL/H/11328–3

Order Number LM6181IN, LM6181AIN, LM6181AMN, LM6181AIM-8, LM6181IM-8 or LM6181AMJ/883
See NS Package Number J08A, M08A or N08E

16-Pin Small Outline Package (M)



• V− 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
• V− 4
N/C 5
N/C 6
N/C 7
• V− 8
16 V− •
15 N/C
14 N/C
13 N/C
12 N/C
11 V+
10 OUTPUT
9 V− •
+
−
*Heat sinking pins (Note 3)

TL/H/11328–4

Order Number LM6181IM or LM6181AIM
See NS Package Number M16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Differential Input Voltage	±6V
Input Voltage	±Supply Voltage
Inverting Input Current	15 mA
Soldering Information	
Dual-In-Line Package (N) Soldering (10 sec)	260°C
Small Outline Package (M)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Output Short Circuit	(Note 7)
Storage Temperature Range	$-65°C \leq T_J \leq +150°C$
Maximum Junction Temperature	150°C
ESD Rating (Note 2)	±3000V

Operating Ratings

Supply Voltage Range	7V to 32V
Junction Temperature Range (Note 3)	
LM6181AM	$-55°C \leq T_J \leq +125°C$
LM6181AI, LM6181I	$-40°C \leq T_J \leq +85°C$
Thermal Resistance (θ_{JA}, θ_{JC})	
8-pin DIP (N)	102°C/W, 42°C/W
8-pin SO (M-8)	153°C/W, 42°C/W
16-pin SO (M)	70°C/W, 38°C/W

±15V DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $R_F = 820\Omega$, and $R_L = 1\ k\Omega$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
V_{OS}	Input Offset Voltage		2.0	3.0 **4.0**	2.0	3.0 **3.5**	3.5	5.0 **5.5**	mV max
TC V_{OS}	Input Offset Voltage Drift		5.0		5.0		5.0		μV/°C
I_B	Inverting Input Bias Current		2.0	5.0 **12.0**	2.0	5.0 **12.0**	5.0	10 **17.0**	μA max
	Non-Inverting Input Bias Current		0.5	1.5 **3.0**	0.5	1.5 **3.0**	2.0	3.0 **5.0**	
TC I_B	Inverting Input Bias Current Drift		30		30		30		nA/°C
	Non-Inverting Input Bias Current Drift		10		10		10		
I_B PSR	Inverting Input Bias Current Power Supply Rejection	$V_S = \pm4.5V, \pm16V$	0.3	0.5 **3.0**	0.3	0.5 **3.0**	0.3	0.75 **4.5**	μA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	$V_S = \pm4.5V, \pm16V$	0.05	0.5 **1.5**	0.05	0.5 **1.5**	0.05	0.5 **3.0**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	$-10V \leq V_{CM} \leq +10V$	0.3	0.5 **0.75**	0.3	0.5 **0.75**	0.3	0.75 **1.0**	
	Non-Inverting Input Bias Current Common Mode Rejection	$-10V \leq V_{CM} \leq +10V$	0.1	0.5 **0.5**	0.1	0.5 **0.5**	0.1	0.5 **0.5**	
CMRR	Common Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	60	50 **50**	60	50 **50**	60	50 **50**	dB min
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V, \pm16V$	80	70 **70**	80	70 **70**	80	70 **65**	dB min
R_O	Output Resistance	$A_V = -1$, f = 300 kHz	0.2		0.2		0.2		Ω
R_{IN}	Non-Inverting Input Resistance		10		10		10		MΩ min
V_O	Output Voltage Swing	$R_L = 1\ k\Omega$	12	11 **11**	12	11 **11**	12	11 **11**	V min
		$R_L = 100\Omega$	11	10 **7.5**	11	10 **8.0**	11	10 **8.0**	
I_{SC}	Output Short Circuit Current		130	100 **75**	130	100 **85**	130	100 **85**	mA min

± 15V DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, R_F = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
Z_T	Transimpedance	R_L = 1 kΩ	1.8	1.0 **0.5**	1.8	1.0 **0.5**	1.8	0.8 **0.4**	MΩ min
		R_L = 100Ω	1.4	0.8 **0.4**	1.4	0.8 **0.4**	1.4	0.7 **0.35**	
I_S	Supply Current	No Load, V_O = 0V	7.5	10 **10**	7.5	10 **10**	7.5	10 **10**	mA max
V_{CM}	Input Common Mode Voltage Range		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V

± 15V AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, R_F = 820Ω, R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	100		100		100		MHz min
		A_V = +10	80		80		80		
		A_V = −1	100	80	100	80	100	80	
		A_V = −10	60		60		60		
PBW	Power Bandwidth	A_V = −1, V_O = 5 V_{PP}	60		60		60		
SR	Slew Rate	Overdriven	2000		2000		2000		V/µs min
		A_V = −1, V_O = ±10V, R_L = 150Ω (Note 6)	1400	1000	1400	1000	1400	1000	
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±5V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	5		5		5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	6		6		6		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/$\sqrt{Hz}$
$i_{n(-)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/$\sqrt{Hz}$
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		nV/$\sqrt{Hz}$
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−50		−50		−50		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−50		
	Differential Gain	R_L = 150Ω A_V = +2 NTSC	0.05		0.05		0.05		%
	Differential Phase	R_L = 150Ω A_V = +2 NTSC	0.04		0.04		0.04		Deg

± 5V DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±5V, R_F = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
V_{OS}	Input Offset Voltage		1.0	2.0 **3.0**	1.0	2.0 **2.5**	1.0	3.0 **3.5**	mV max
TC V_{OS}	Input Offset Voltage Drift		2.5		2.5		2.5		µV/°C
I_B	Inverting Input Bias Current		5.0	10 **22**	5.0	10 **22**	5.0	17.5 **27.0**	µA max
	Non-Inverting Input Bias Current		0.25	1.5 **1.5**	0.25	1.5 **1.5**	0.25	3.0 **5.0**	
TC I_B	Inverting Input Bias Current Drift		50		50		50		nA/°C
	Non-Inverting Input Bias Current Drift		3.0		3.0		3.0		
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.3	0.5 **0.5**	0.3	0.5 **0.5**	0.3	1.0 **1.0**	µA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.05	0.5 **0.5**	0.05	0.5 **0.5**	0.05	0.5 **0.5**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	$-2.5V \le V_{CM} \le +2.5V$	0.3	0.5 **1.0**	0.3	0.5 **1.0**	0.3	1.0 **1.5**	
	Non-Inverting Input Bias Current Common Mode Rejection	$-2.5V \le V_{CM} \le +2.5V$	0.12	0.5 **1.0**	0.12	0.5 **0.5**	0.12	0.5 **0.5**	
CMRR	Common Mode Rejection Ratio	$-2.5V \le V_{CM} \le +2.5V$	57	50 **47**	57	50 **47**	57	50 **47**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.0V, ±6.0V	80	70 **70**	80	70 **70**	80	64 **64**	
R_O	Output Resistance	A_V = −1, f = 300 kHz	0.25		0.25		0.25		Ω
R_{IN}	Non-Inverting Input Resistance		8		8		8		MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	2.6	2.25 **2.2**	2.6	2.25 **2.25**	2.6	2.25 **2.25**	V min
		R_L = 100Ω	2.2	2.0 **2.0**	2.2	2.0 **2.0**	2.2	2.0 **2.0**	
I_{SC}	Output Short Circuit Current		100	75 **70**	100	75 **70**	100	75 **70**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.4	0.75 **0.35**	1.4	0.75 **0.4**	1.0	0.6 **0.3**	MΩ min
		R_L = 100Ω	1.0	0.5 **0.25**	1.0	0.5 **0.25**	1.0	0.4 **0.2**	
I_S	Supply Current	No Load, V_O = 0V	6.5	8.5 **8.5**	6.5	8.5 **8.5**	6.5	8.5 **8.5**	mA max
V_{CM}	Input Common Mode Voltage Range		$V^+ - 1.7V$ $V^- + 1.7V$		$V^+ - 1.7V$ $V^- + 1.7V$		$V^+ - 1.7V$ $V^- + 1.7V$		V

±5V AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±5V, R_F = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM Typical (Note 4)	LM6181AM Limit (Note 5)	LM6181AI Typical (Note 4)	LM6181AI Limit (Note 5)	LM6181I Typical (Note 4)	LM6181I Limit (Note 5)	Units
BW	Closed Loop Bandwidth −3 dB	A_V = +2	50		50		50		MHZ min
		A_V = +10	40		40		40		
		A_V = −1	55	35	55	35	55	35	
		A_V = −10	35		35		35		
PBW	Power Bandwidth	A_V = −1, V_O = 4 V_{PP}	40		40		40		
SR	Slew Rate	A_V = −1, V_O = ±2V, R_L = 150Ω (Note 6)	500	375	500	375	500	375	V/µs min
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±2V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	8.5		8.5		8.5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	8		8		8		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(-)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		nV/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−45		−45		−45		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−55		
	Differential Gain	R_L = 150Ω A_V = +2 NTSC	0.063		0.063		0.063		%
	Differential Phase	R_L = 150Ω A_V = +2 NTSC	0.16		0.16		0.16		Deg

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model 100 pF and 1.5 kΩ.

Note 3: The typical junction-to-ambient thermal resistance of the molded plastic DIP(N) package soldered directly into a PC board is 102°C/W. The junction-to-ambient thermal resistance of the S.O. surface mount (M) package mounted flush to the PC board is 70°C/W when pins 1, 4, 8, 9 and 16 are soldered to a total 2 in^2 1 oz. copper trace. The 16-pin S.O. (M) package must have pin 4 and at least one of pins 1, 8, 9, or 16 connected to V^- for proper operation. The typical junction-to-ambient thermal resistance of the S.O. (M-8) package soldered directly into a PC board is 153°C/W.

Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

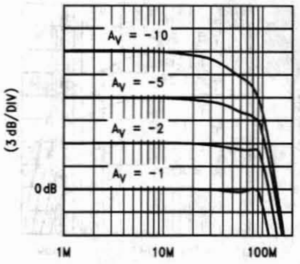
Note 6: Measured from +25% to +75% of output waveform.

Note 7: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±130 mA over a long term basis may adversely affect reliability.

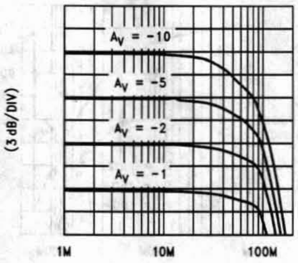
Note 8: For guaranteed Military Temperature Range parameters see RETS6181X.

Typical Performance Characteristics T_A = 25°C unless otherwise noted

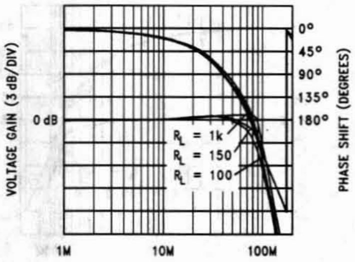
CLOSED-LOOP FREQUENCY RESPONSE
V_S = ±15V; R_f = 820Ω;
R_L = 1 kΩ



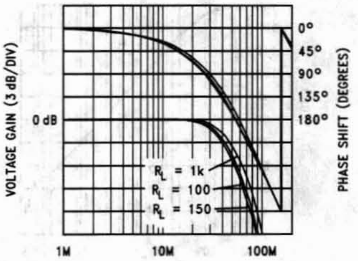
CLOSED-LOOP FREQUENCY RESPONSE
V_S = ±15V; R_f = 820Ω;
R_L = 150Ω



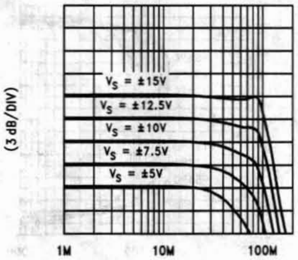
UNITY GAIN FREQUENCY RESPONSE
V_S = ±15V; A_V = +1;
R_f = 820Ω



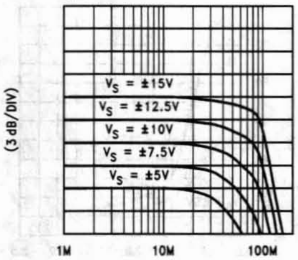
UNIT GAIN FREQUENCY RESPONSE
V_S = ±5V; A_V = +1;
R_f = 820Ω



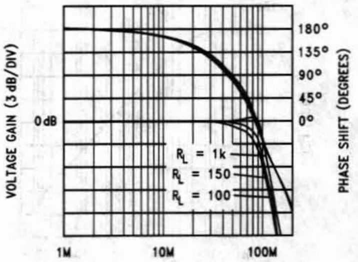
FREQUENCY RESPONSE vs SUPPLY VOLTAGE
A_V = −1; R_f = 820Ω;
R_L = 1 kΩ



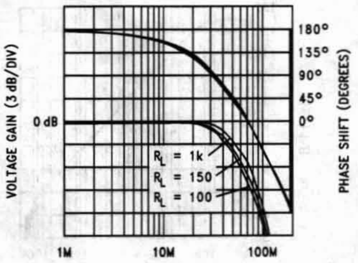
FREQUENCY RESPONSE vs SUPPLY VOLTAGE
A_V = −1; R_f = 820Ω;
R_L = 150Ω



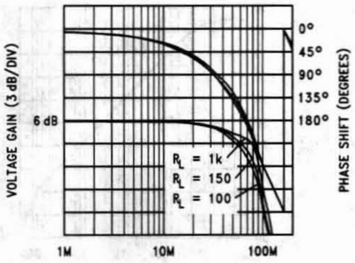
INVERTING GAIN FREQUENCY RESPONSE
V_S = ±15V; A_V = −1;
R_f = 820Ω



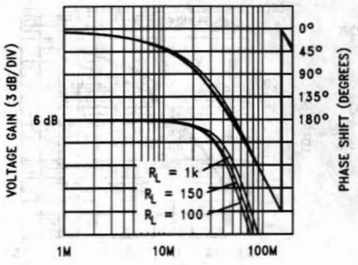
INVERTING GAIN FREQUENCY RESPONSE
V_S = ±5V; A_V = −1;
R_f = 820Ω



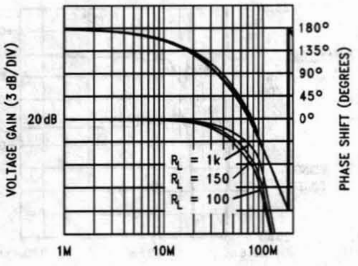
NON-INVERTING GAIN FREQUENCY RESPONSE
V_S = ±15V; A_V = +2;
R_f = 820Ω



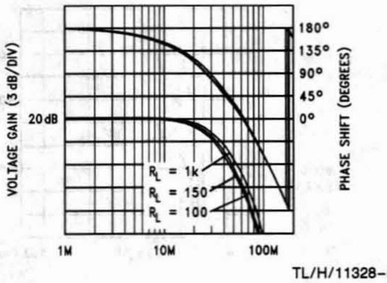
NON-INVERTING GAIN FREQUENCY RESPONSE
V_S = ±5V; A_V = +2;
R_f = 820Ω



INVERTING GAIN FREQUENCY RESPONSE
V_S = ±15V; A_V = −10;
R_f = 820Ω



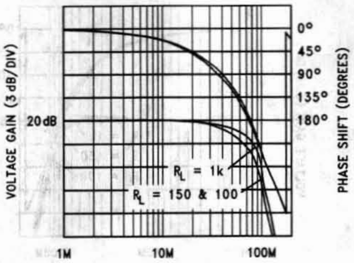
INVERTING GAIN FREQUENCY RESPONSE
V_S = ±5V; A_V = −10;
R_f = 820Ω



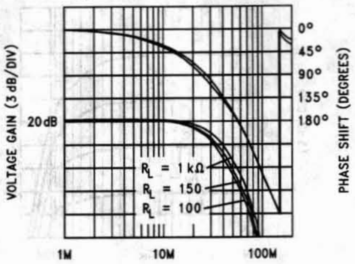
TL/H/11328–5

Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

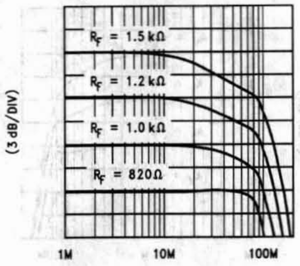
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = +10$;
$R_f = 820\Omega$



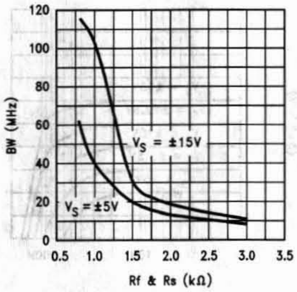
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = +10$;
$R_f = 820\Omega$



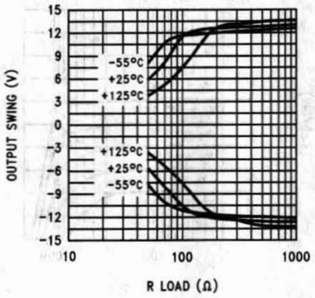
NON-INVERTING GAIN FREQUENCY COMPENSATION
$V_S = \pm 15V$; $A_V = +2$;
$R_L = 150\Omega$



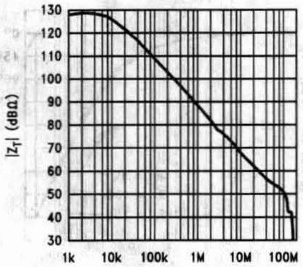
BANDWIDTH vs R_f & R_S
$A_V = -1$, $R_L = 1 k\Omega$



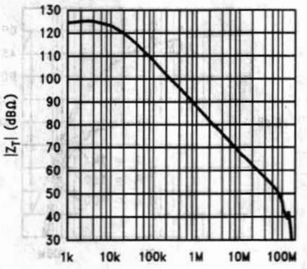
OUTPUT SWING vs R_{LOAD} PULSED, $V_S = \pm 15V$,
$I_{IN} = \pm 200\ \mu A$, $V_{IN+} = 0V$



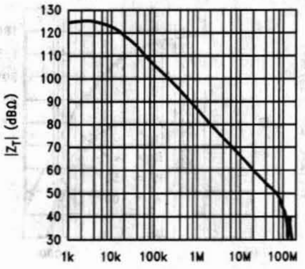
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 15V$
$R_L = 1 k\Omega$



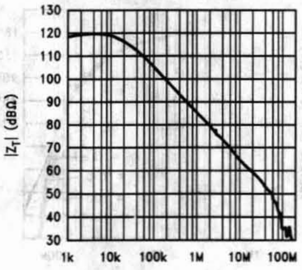
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 15V$
$R_L = 100\Omega$



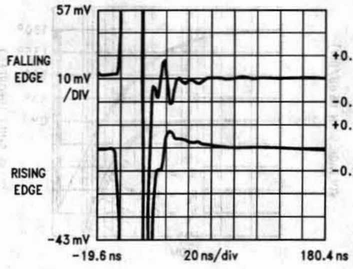
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 5V$
$R_L = 1 k\Omega$



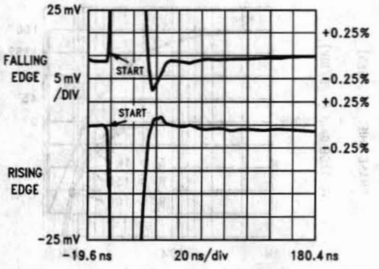
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 5V$
$R_L = 100\Omega$



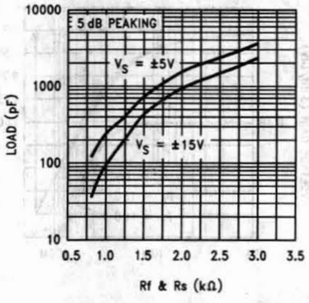
SETTLING RESPONSE
$V_S = \pm 15V$; $R_L = 150\Omega$;
$V_O = \pm 5V$; $A_V = -1$



SETTLING RESPONSE
$V_S = \pm 5V$; $R_L = 150\Omega$;
$V_O = \pm 2V$; $A_V = -1$



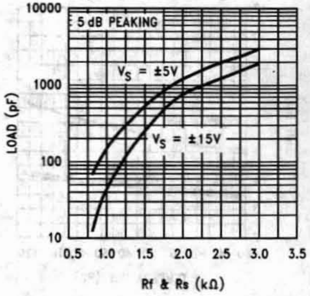
SUGGESTED R_f and R_S for C_L
$A_V = -1$; $R_L = 150\Omega$



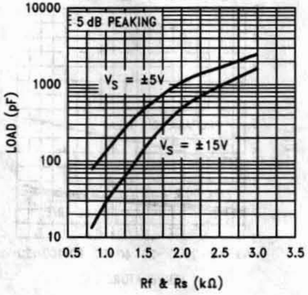
TL/H/11328–6

Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

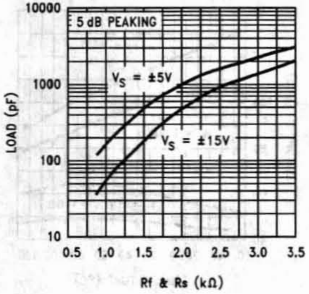
SUGGESTED R_f and R_S FOR C_L $A_V = -1$



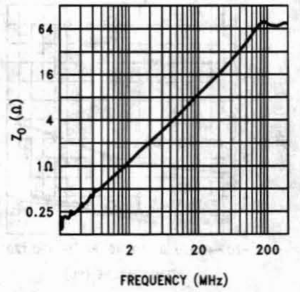
SUGGESTED R_f and R_S FOR C_L $A_V = +2$; $R_L = 150\Omega$



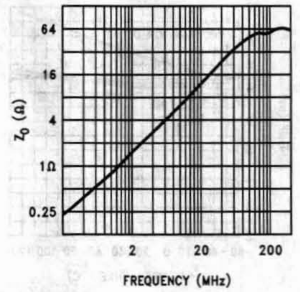
SUGGESTED R_f and R_S FOR C_L $A_V = +2$



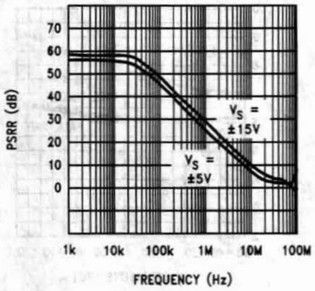
OUTPUT IMPEDANCE vs FREQ $V_S = \pm 15V$; $A_V = -1$ $R_f = 820\Omega$



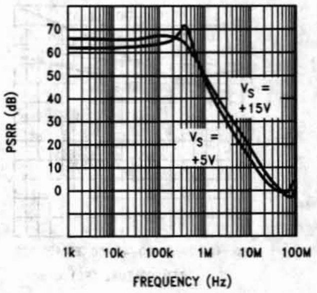
OUTPUT IMPEDANCE vs FREQ $V_S = \pm 5V$; $A_V = -1$ $R_f = 820\Omega$



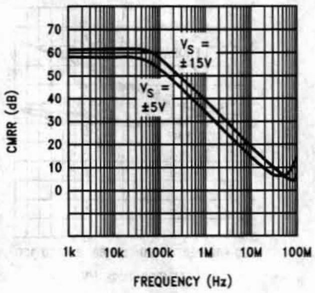
PSRR ($V_S{}^+$) vs FREQUENCY



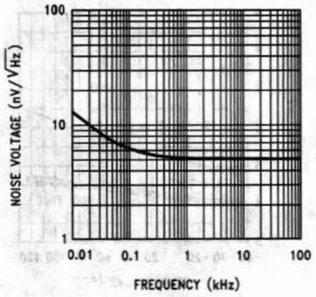
PSRR ($V_S{}^-$) vs FREQUENCY



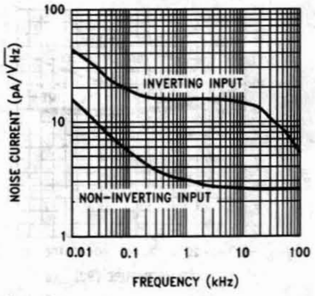
CMRR vs FREQUENCY



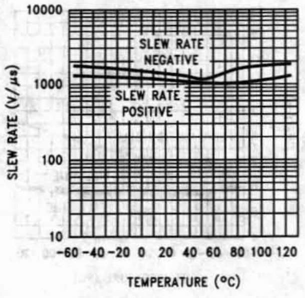
INPUT VOLTAGE NOISE vs FREQUENCY



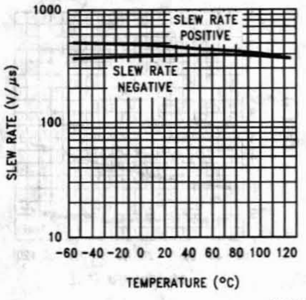
INPUT CURRENT NOISE vs FREQUENCY



SLEW RATE vs TEMPERATURE $A_V = -1$; $R_L = 150\Omega$, $V_S = \pm 15V$



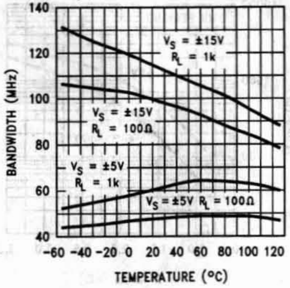
SLEW RATE vs TEMPERATURE $A_V = -1$; $R_L = 150\Omega$, $V_S = \pm 5V$



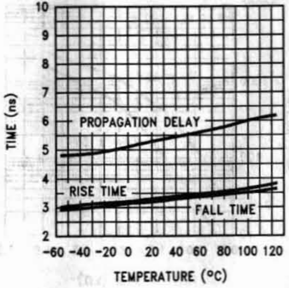
TL/H/11328–7

Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

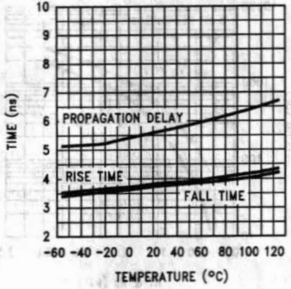
−3 dB BANDWIDTH vs TEMPERATURE $A_V = -1$



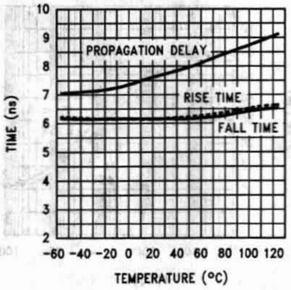
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm15V$; $R_L = 1\ k\Omega$



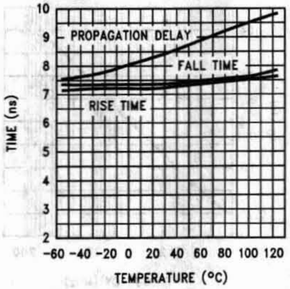
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm15V$; $R_L = 100\Omega$



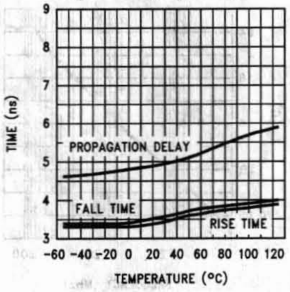
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm5V$; $R_L = 1\ k\Omega$



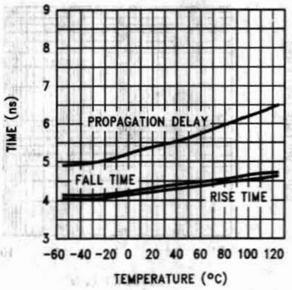
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm5V$; $R_L = 100\Omega$



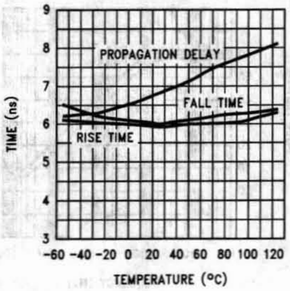
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm15V$; $R_L = 1\ k\Omega$



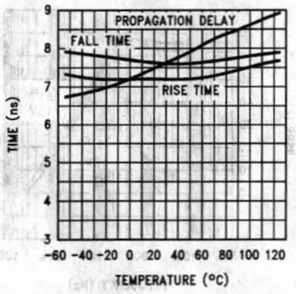
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm15V$; $R_L = 100\Omega$



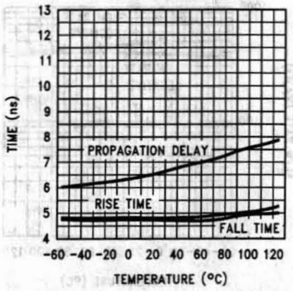
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm5V$; $R_L = 1\ k\Omega$



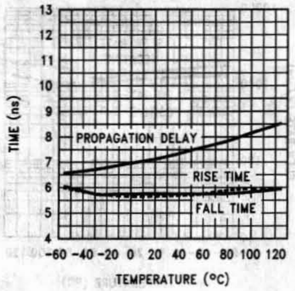
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm5V$; $R_L = 100\Omega$



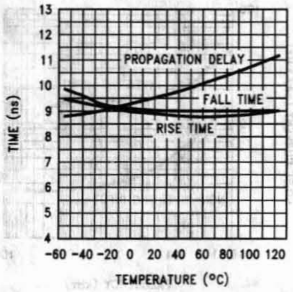
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$ $V_S = \pm15V$; $R_L = 1\ k\Omega$



SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$ $V_S = \pm15V$; $R_L = 100\Omega$

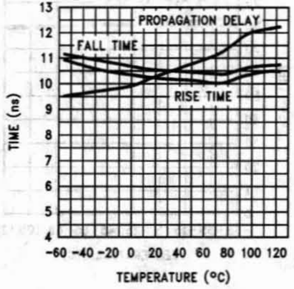


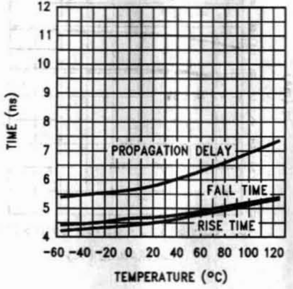
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$ $V_S = \pm5V$; $R_L = 1\ k\Omega$

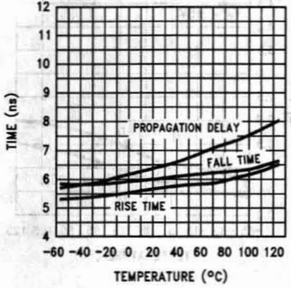


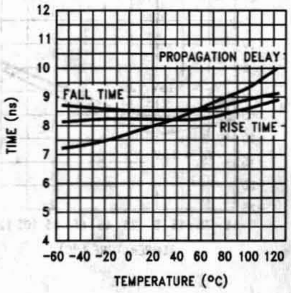
TL/H/11328–29

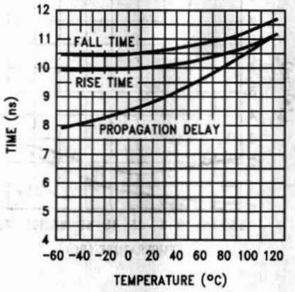
Typical Performance Characteristics T_A = 25°C unless otherwise noted (Continued)

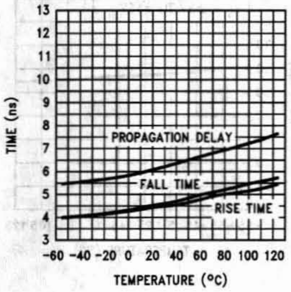

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$
$V_S = \pm5V$; $R_L = 100\Omega$

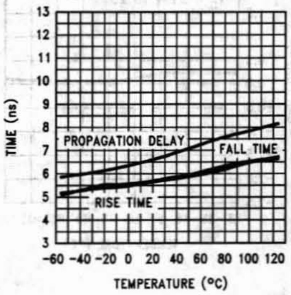

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -10$
$V_S = \pm15V$; $R_L = 1\ k\Omega$

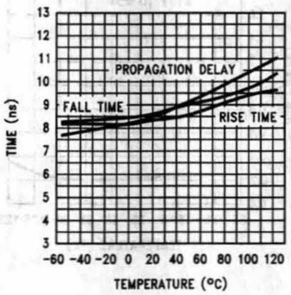

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -10$
$V_S = \pm15V$; $R_L = 100\Omega$

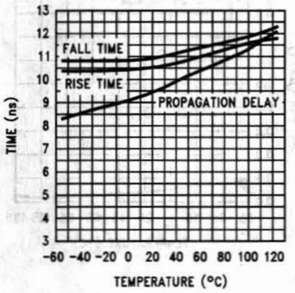

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -10$
$V_S = \pm5V$; $R_L = 1\ k\Omega$

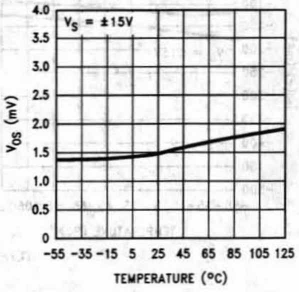

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -10$
$V_S = \pm5V$; $R_L = 100\Omega$

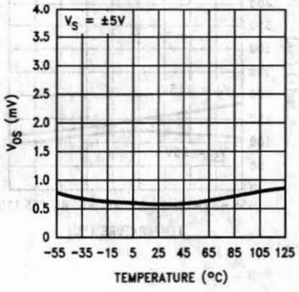

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +10$
$V_S = \pm15V$; $R_L = 1\ k\Omega$

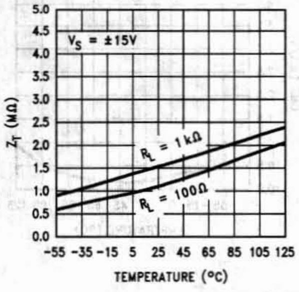

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +10$
$V_S = \pm15V$; $R_L = 100\Omega$


SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +10$
$V_S = \pm5V$; $R_L = 1\ k\Omega$


SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +10$
$V_S = \pm5V$; $R_L = 100\Omega$


OFFSET VOLTAGE vs TEMPERATURE

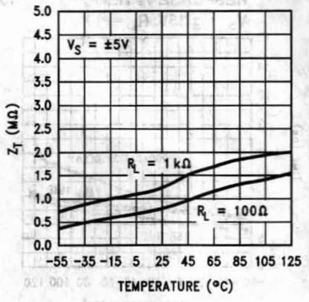

OFFSET VOLTAGE vs TEMPERATURE


TRANSIMPEDANCE vs TEMPERATURE

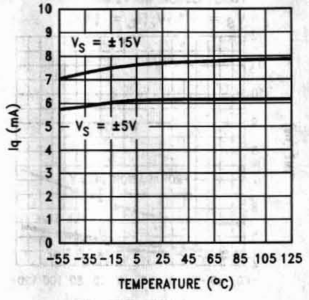
TL/H/11328–8

Typical Performance Characteristics T_A = 25°C unless otherwise noted (Continued)

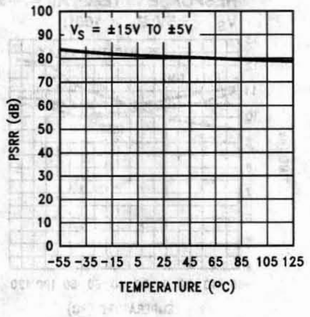
TRANSIMPEDANCE vs TEMPERATURE



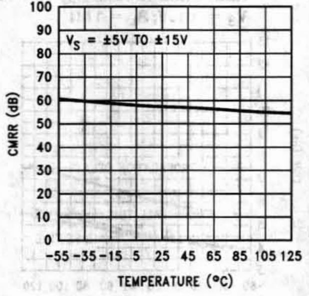
QUIESCENT CURRENT vs TEMPERATURE



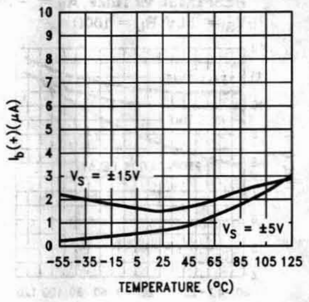
PSRR vs TEMPERATURE



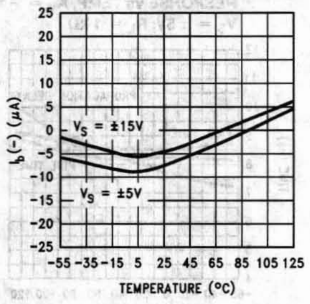
CMRR vs TEMPERATURE



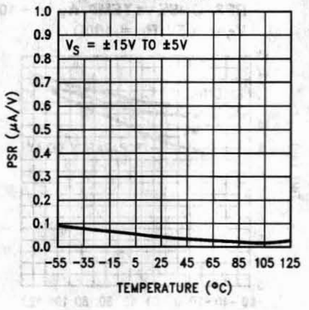
NON-INVERTING BIAS CURRENT vs TEMPERATURE



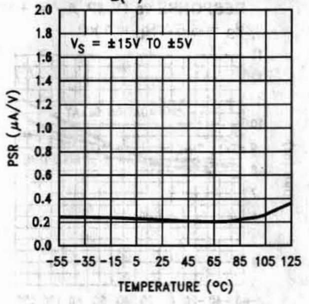
INVERTING BIAS CURRENT vs TEMPERATURE



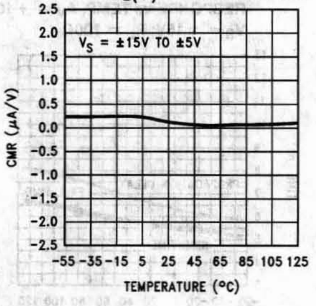
PSR $I_{B(+)}$ vs TEMPERATURE



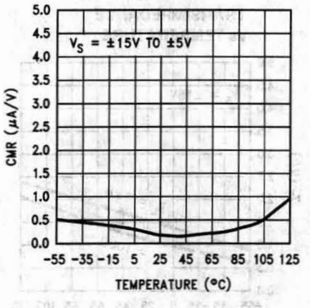
PSR $I_{B(-)}$ vs TEMPERATURE



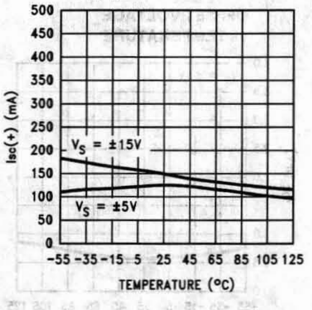
CMR $I_{B(+)}$ vs TEMPERATURE



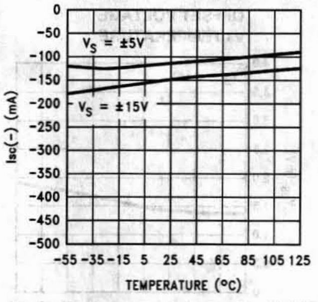
CMR $I_{B(-)}$ vs TEMPERATURE



$I_{SC(+)}$ vs TEMPERATURE



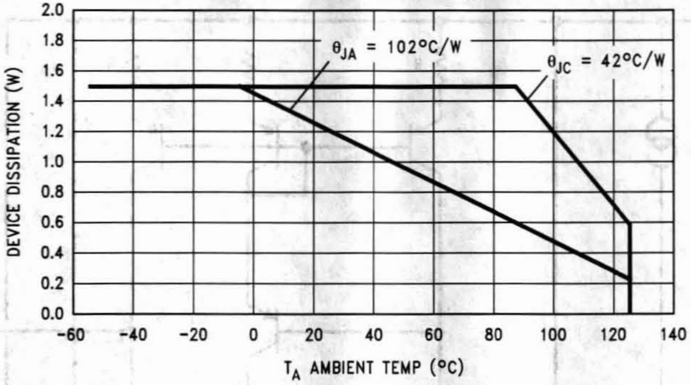
$I_{SC(-)}$ vs TEMPERATURE



TL/H/11328–9

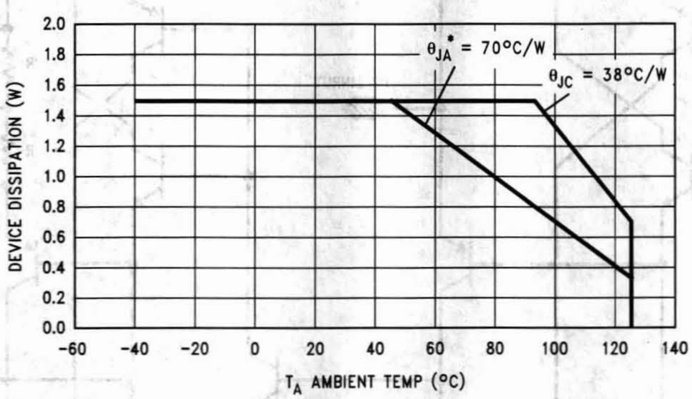
Typical Performance Characteristics

Absolute Maximum Power Derating Curves



TL/H/11328-30

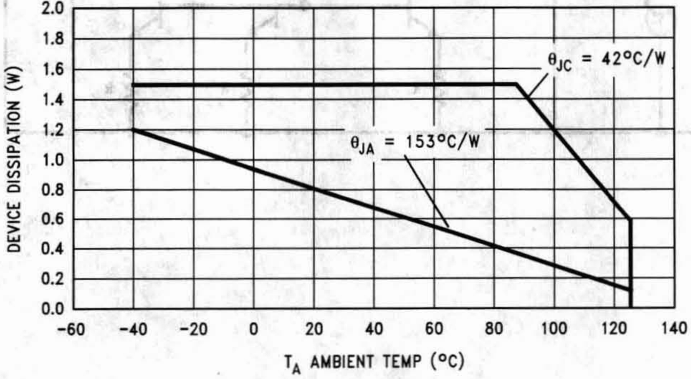
N-Package



TL/H/11328-31

M-Package

*θ_{JA} = Thermal Resistance with 2 square inches of 1 ounce Copper tied to Pins 1, 8, 9 and 16.

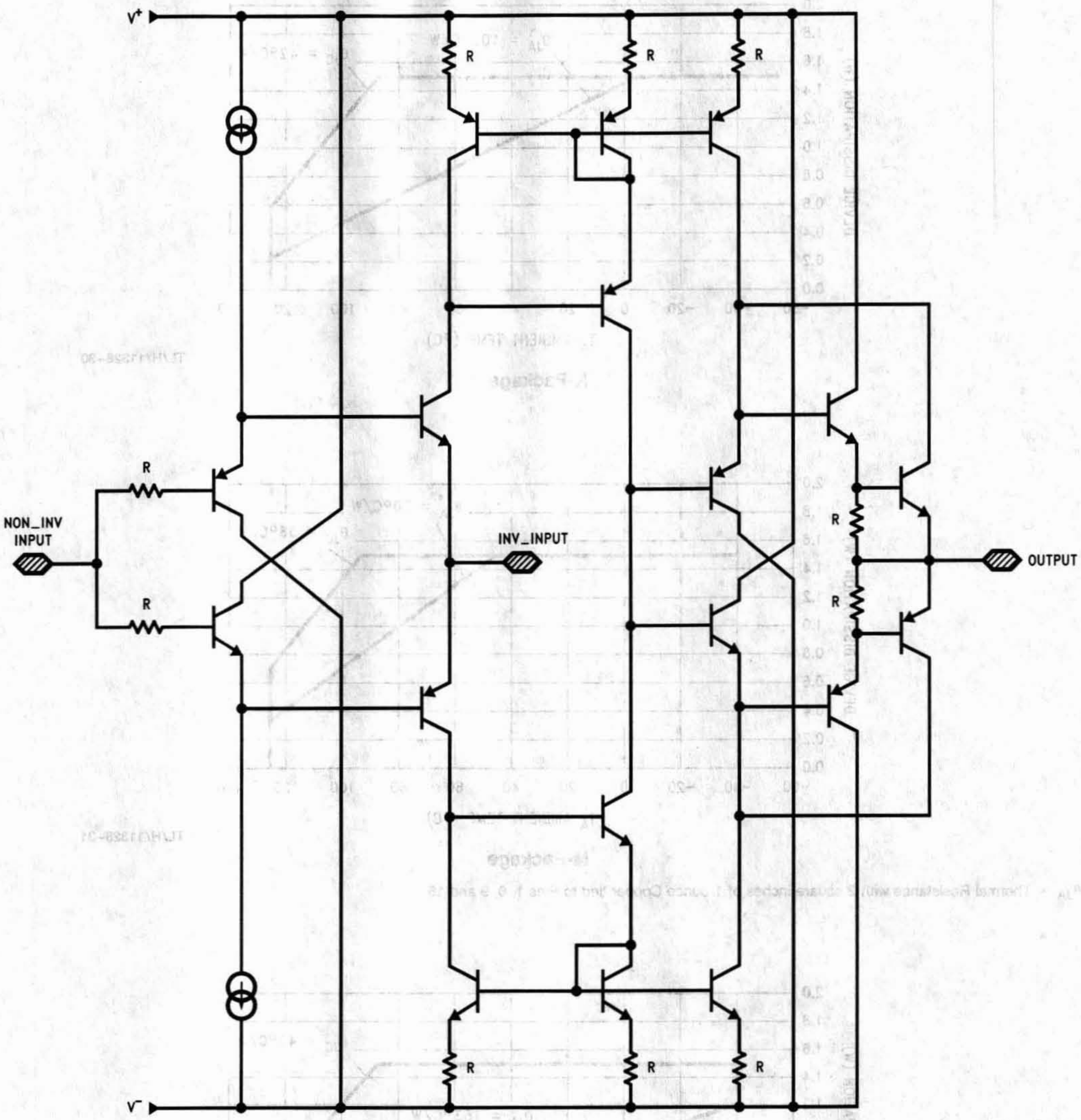


TL/H/11328-33

M-8 Package

Typical Performance Characteristics (Continued)

Simplified Schematic

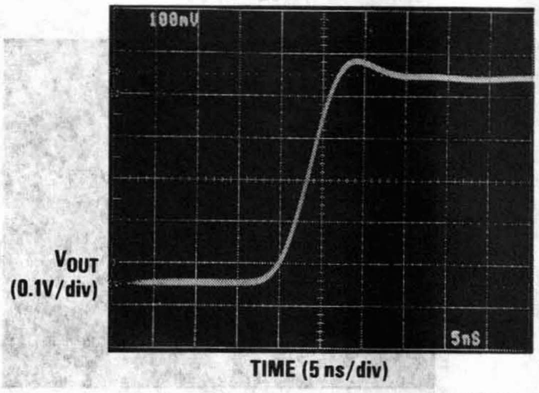

V+
R
R
R
R
NON_INV
INPUT
R
INV_INPUT
R
OUTPUT
R
R
R
R
V−

TL/H/11328–32

Typical Applications

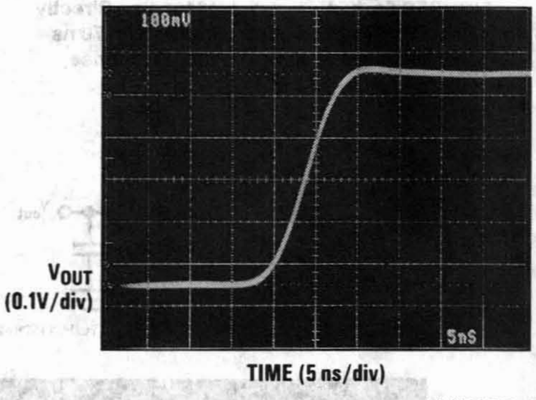
CURRENT FEEDBACK TOPOLOGY

For a conventional voltage feedback amplifier the resulting small-signal bandwidth is inversely proportional to the desired gain to a first order approximation based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6181, transcends this limitation to offer a signal bandwidth that is relatively independent of the closed-loop gain. *Figures 1a* and *1b* illustrate that for closed loop gains of −1 and −5 the resulting pulse fidelity suggests quite similar bandwidths for both configurations.



TL/H/11328–12

1a

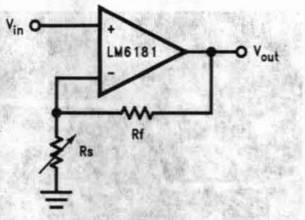


TL/H/11328–13

1b

FIGURES 1a, 1b: Variation of Closed Loop Gain from −1 to −5 Yields Similar Responses

The closed-loop bandwidth of the LM6181 depends on the feedback resistance, R_f. Therefore, R_S and not R_f, must be varied to adjust for the desired closed-loop gain as in *Figure 2.*



TL/H/11328–14

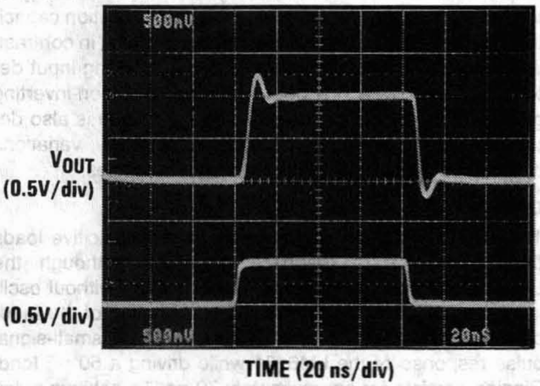
FIGURE 2. R_S Is Adjusted to Obtain the Desired Closed Loop Gain, A_{VCL}

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

A fundamental requirement for high-speed amplifier design is adequate bypassing of the power supply. It is critical to maintain a wideband low-impedance to ground at the amplifiers supply pins to insure the fidelity of high speed amplifier transient signals. 10 μF tantalum and 0.1 μF ceramic bypass capacitors are recommended for each supply pin. The bypass capacitors should be placed as close to the amplifier pins as possible (0.5″ or less).

FEEDBACK RESISTOR SELECTION: R_f

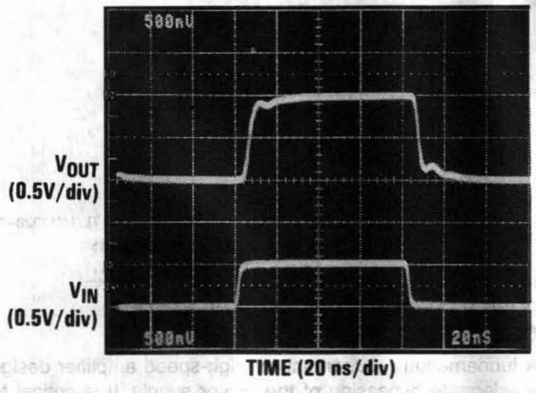
Selecting the feedback resistor, R_f, is a dominant factor in compensating the LM6181. For general applications the LM6181 will maintain specified performance with an 820Ω feedback resistor. Although this value will provide good results for most applications, it may be advantageous to adjust this value slightly. Consider, for instance, the effect on pulse responses with two different configurations where both the closed-loop gains are 2 and the feedback resistors are 820Ω, and 1640Ω, respectively. *Figures 3a* and *3b* illustrate the effect of increasing R_f while maintaining the same closed-loop gain—the amplifier bandwidth decreases. Accordingly, larger feedback resistors can be used to slow down the LM6181 (see −3 dB bandwidth vs R_f typical curves) and reduce overshoot in the time domain response. Conversely, smaller feedback resistance values than 820Ω can be used to compensate for the reduction of bandwidth at high closed loop gains, due to 2nd order effects. For example *Figure 4* illustrates reducing R_f to 500Ω to establish the desired small signal response in an amplifier configured for a closed loop gain of 25.



TL/H/11328–15

3a: R_f = 820Ω

Typical Applications (Continued)



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3b: $R_f = 1640\Omega$

FIGURES 3a, b: Increasing Compensation with Increasing R_f

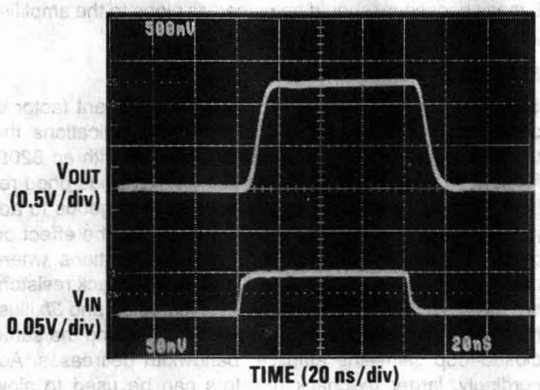

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FIGURE 4: Reducing R_f for Large Closed Loop Gains, $R_f = 500\Omega$

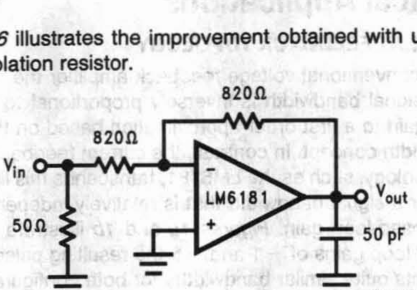
SLEW RATE CONSIDERATIONS

The slew rate characteristics of current feedback amplifiers are different than traditional voltage feedback amplifiers. In voltage feedback amplifiers slew rate limiting or non-linear amplifier behavior is dominated by the finite availability of the 1st stage tail current charging the compensation capacitor. The slew rate of current feedback amplifiers, in contrast, is not constant. Transient current at the inverting input determines slew rate for both inverting and non-inverting gains. The non-inverting configuration slew rate is also determined by input stage limitations. Accordingly, variations of slew rates occur for different circuit topologies.

DRIVING CAPACITIVE LOADS

The LM6181 can drive significantly larger capacitive loads than many current feedback amplifiers. Although the LM6181 can directly drive as much as 100 pF without oscillating, the resulting response will be a function of the feedback resistor value. *Figure 5* illustrates the small-signal pulse response of the LM6181 while driving a 50 pF load. Ringing persists for approximately 70 ns. To achieve pulse responses with less ringing either the feedback resistor can be increased (see typical curves Suggested R_f and R_S for C_L), or resistive isolation can be used (10Ω–51Ω typically works well). Either technique, however, results in lowering the system bandwidth.

Figure 6 illustrates the improvement obtained with using a 47Ω isolation resistor.



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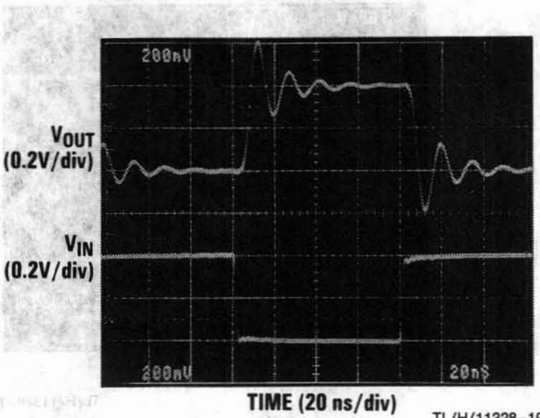
5a



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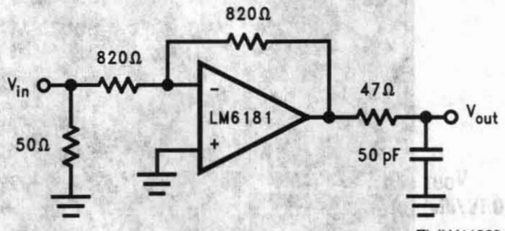
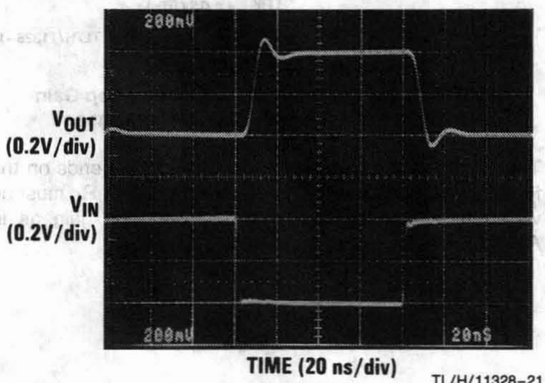
5b

FIGURES 5a, b: $A_V = -1$, LM6181 Can Directly Drive 50 pF of Load Capacitance with 70 ns of Ringing Resulting in Pulse Response



TL/H/11328-20

6a



TL/H/11328-21

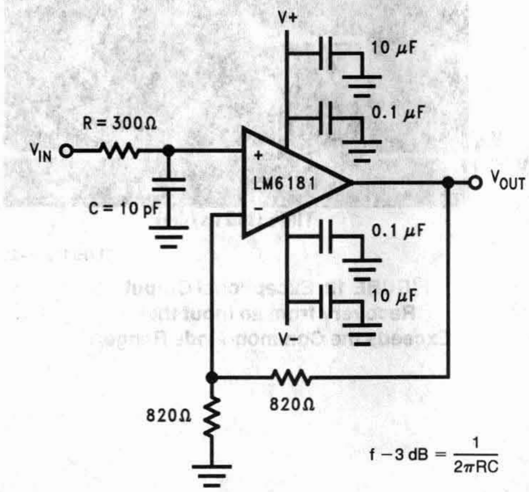
6b

FIGURES 6a, b: Resistive Isolation of C_L Provides Higher Fidelity Pulse Response. R_f and R_S Could Be Increased to Maintain $A_V = -1$ and Improve Pulse Response Characteristics.

Typical Applications (Continued)

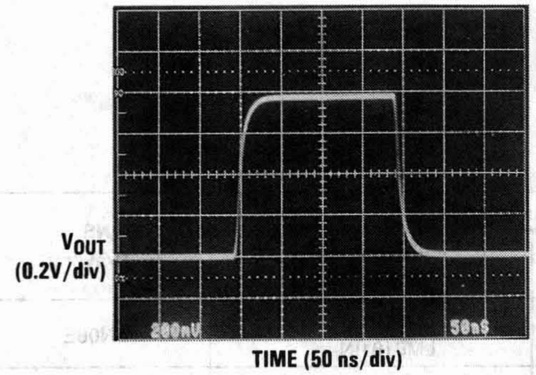
CAPACITIVE FEEDBACK

For voltage feedback amplifiers it is quite common to place a small lead compensation capacitor in parallel with feedback resistance, R_f. This compensation serves to reduce the amplifier's peaking in the frequency domain which equivalently tames the transient response. To limit the bandwidth of current feedback amplifiers, do not use a capacitor across R_f. The dynamic impedance of capacitors in the feedback loop reduces the amplifier's stability. Instead, reduced peaking in the frequency response, and bandwidth limiting can be accomplished by adding an RC circuit, as illustrated in *Figure 7b.*



TL/H/11328-22

7a



7b

TL/H/11328-23

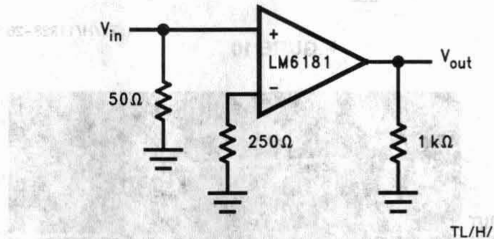
FIGURES 7a, b: RC Limits Amplifier Bandwidth to 50 MHz, Eliminating Peaking in the Resulting Pulse Response

Typical Performance Characteristics

OVERDRIVE RECOVERY

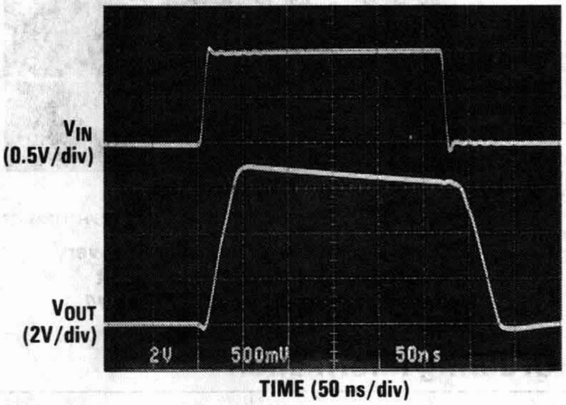
When the output or input voltage range of a high speed amplifier is exceeded, the amplifier must recover from an overdrive condition. The typical recovery times for open-loop, closed-loop, and input common-mode voltage range overdrive conditions are illustrated in *Figures 9, 11* and *12,* respectively.

The open-loop circuit of *Figure 8* generates an overdrive response by allowing the ±0.5V input to exceed the linear input range of the amplifier. Typical positive and negative overdrive recovery times shown in *Figure 9* are 5 ns and 25 ns, respectively.



TL/H/11328-24

FIGURE 8

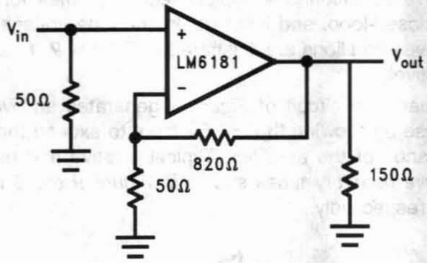


TL/H/11328-25

FIGURE 9. Open-Loop Overdrive Recovery Time of 5 ns, and 25 ns from Test Circuit in *Figure 8*

Typical Performance Characteristics (Continued)

The large closed-loop gain configuration in *Figure 10* forces the amplifier output into overdrive. *Figure 11* displays the typical 30 ns recovery time to a linear output value.



TL/H/11328-26

FIGURE 10

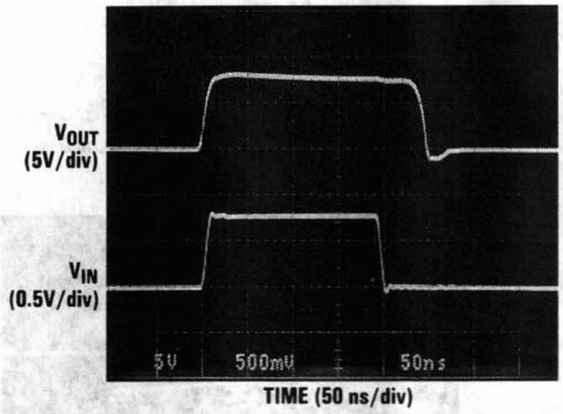


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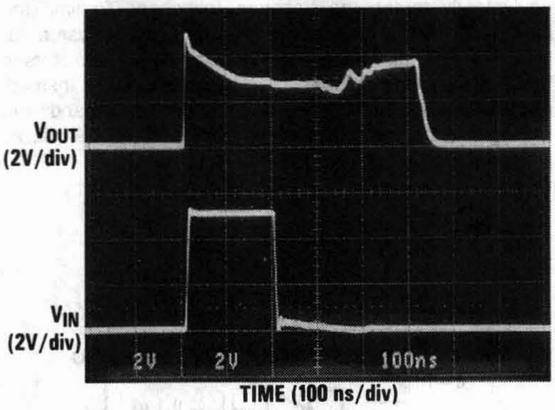
FIGURE 11. Closed-Loop Overdrive Recovery Time of 30 ns from Exceeding Output Voltage Range from Circuit in *Figure 10*

The common-mode input of the circuit in *Figure 10* is exceeded by a 5V pulse resulting in a typical recovery time of 310 ns shown in *Figure 12*. The LM6181 supply voltage is ±5V.



TL/H/11328-28

FIGURE 12. Exceptional Output Recovery from an Input that Exceeds the Common-Mode Range

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-Pin Molded DIP	LM6181AMN	LM6181AIN LM6181IN	N08E
8-Pin Small Outline Molded Package		LM6181AIM-8 LM6181IM-8	M08A
16-Pin Small Outline		LM6181AIM LM6181IM	M16A
8-Pin Ceramic DIP	LM6181AMJ/883		J08A

National Semiconductor

LM6182 Dual 100 mA Output, 100 MHz Current Feedback Amplifier

General Description

The LM6182 dual current feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. Each amplifier can directly drive a 2V signal into a 50Ω or 75Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for a dual 8-pin high-speed amplifier making it ideal for video applications.

Built on National's advanced high-speed VIP II™ (Vertically Integrated PNP) process, the LM6182 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at Av = −1, 60 MHz at Av = −10. With a slew rate of 2000 V/μsec, 2nd harmonic distortion of −50 dBc at 10 MHz and settling time of 50 ns (0.1%), the two independent amplifiers of the LM6182 offer performance that is ideal for data acquisition, high-speed ATE, and precision pulse amplifier applications.

See the LM6181 data sheet for a single amplifier with these same features.

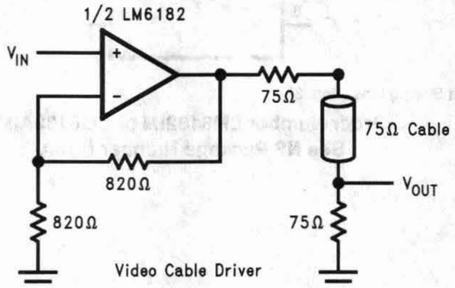
Features (Typical unless otherwise noted)

■ Slew Rate	2000 V/μs
■ Closed Loop Bandwidth	100 MHz
■ Settling Time (0.1%)	50 ns
■ Low Differential Gain and Phase Error $R_L = 150\Omega$	0.05%, 0.04°
■ Low Offset Voltage	2 mV
■ High Output Drive	±10V into 150Ω
■ Characterized for Supply Ranges	±5V and ±15V
■ Improved Performance over OP260 and LT1229	

Applications

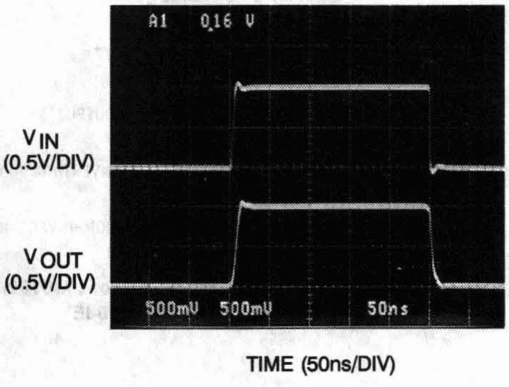
- Coax Cable Driver
- Professional Studio Video Equipment
- Flash ADC Buffer
- PC and Workstation Video Boards
- Facsimile and Imaging Systems

Typical Application



Video Cable Driver

TL/H/11926-1



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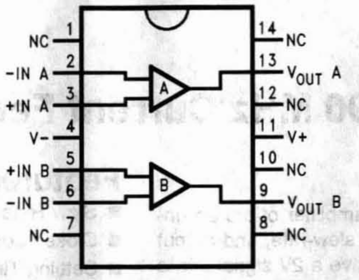
Connection Diagrams

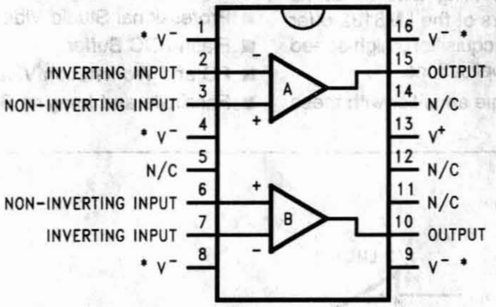
Dual-In-Line Package (J)


NC 1
−IN A 2
+IN A 3
V− 4
+IN B 5
−IN B 6
NC 7
A
B
14 NC
13 VOUT A
12 NC
11 V+
10 NC
9 VOUT B
8 NC

TL/H/11926-51

Order Number LM6182AMJ/883
See NS Package Number J14A

Small Outline Package (M)


• V− 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
• V− 4
N/C 5
NON-INVERTING INPUT 6
INVERTING INPUT 7
• V− 8
A
B
16 V− •
15 OUTPUT
14 N/C
13 V+
12 N/C
11 N/C
10 OUTPUT
9 V− •

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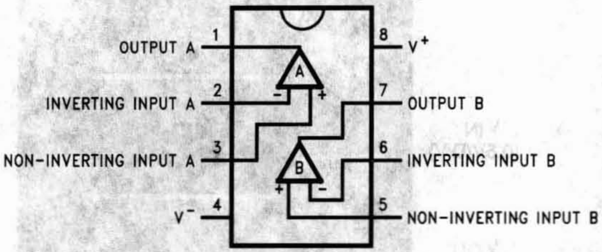
*Heat Sinking Pins (Note 3)

Order Number LM6182IM or LM6182AIM
See NS Package Number M16A

Dual-In-Line Package (N)


OUTPUT A 1
INVERTING INPUT A 2
NON-INVERTING INPUT A 3
V− 4
A
B
8 V+
7 OUTPUT B
6 INVERTING INPUT B
5 NON-INVERTING INPUT B

TL/H/11926-3

Order Number LM6182IN, LM6182AIN or LM6182AMN
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Differential Input Voltage	±6V
Input Voltage	±Supply Voltage
Inverting Input Current	15 mA
Output Short Circuit	(Note 4)
Soldering Information	
Dual-In-Line Package (N) Soldering (10s)	260°C
Small Outline Package (M)	
Vapor Phase (60s)	215°C
Infrared (15s)	220°C
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Junction Temperature	150°C
ESD Rating (Note 2)	±2000V

Operating Ratings

Supply Voltage Range	7V to 32V
Junction Temperature Range (Note 3)	
LM6182AM	$-55°C \le T_J \le +125°C$
LM6182AI, LM6182I	$-40°C \le T_J \le +85°C$

±15V DC Electrical Characteristics

The following specifications apply for supply voltage = ±15V, Vcm = V_O = 0V, R_f = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LM6182AM Limit (Note 6)	LM6182AI Limit (Note 6)	LM6182I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		2.0	3.0 **4.0**	3.0 **3.5**	5.0 **5.5**	mV max
TCV_{OS}	Input Offset Voltage Drift		5.0				μV/°C
I_B	Inverting Input Bias Current		2.0	5.0 **12.0**	5.0 **12.0**	10.0 **17.0**	μA max
	Non-Inverting Input Bias Current		0.75	2.0 **4.0**	2.0 **4.0**	3.0 **5.0**	
TCI_B	Inverting Input Bias Current Drift		30				nA/°C
	Non-Inverting Input Bias Current Drift		10				
I_B PSR	Inverting Input Bias Current Power Supply Rejection	$\pm4.5V \le V_S \le \pm16V$	0.1	0.5 **3.0**	0.5 **3.0**	0.75 **4.5**	μA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	$\pm4.5V \le V_S \le \pm16V$	0.05	0.5 **1.5**	0.5 **1.5**	0.5 **3.0**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	$-10V \le V_{CM} \le +10V$	0.15	0.5 **1.0**	0.5 **1.0**	0.75 **1.5**	
	Non-Inverting Input Bias Current Common Mode Rejection	$-10V \le V_{CM} \le +10V$	0.1	0.5 **1.0**	0.5 **1.0**	0.5 **1.5**	
CMRR	Common Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	60	50 **47**	50 **47**	50 **47**	dB min
PSRR	Power Supply Rejection Ratio	$\pm4.5V \le V_S \le \pm16V$	80	70 **67**	70 **67**	70 **65**	dB min
R_O	Output Resistance	$A_V = -1$ f = 300 kHz	0.2				Ω
R_{IN}	Non-Inverting Input Resistance		10				MΩ
V_O	Output Voltage Swing	R_L = 1 kΩ	12	11 **10**	11 **10**	11 **10**	V min
		R_L = 150Ω	11	9.5 **5.6**	9.5 **6.0**	9.5 **6.0**	

± 15V DC Electrical Characteristics (Continued)

The following specifications apply for supply voltage = ±15V, Vcm = V_O = 0V, R_f = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LM6182AM Limit (Note 6)	LM6182AI Limit (Note 6)	LM6182I Limit (Note 6)	Units
I_{SC}	Output Short Circuit Current		100	70 **37.5**	70 **40**	70 **40**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.8	1.0 **0.4**	1.0 **0.5**	0.8 **0.4**	MΩ min
		R_L = 150Ω	1.4	0.8 **0.3**	0.8 **0.35**	0.7 **0.3**	
I_S	Supply Current	No Load, V_{IN} = 0V Both Amplifiers	15	20 **22**	20 **22**	20 **22**	mA max
V_{CM}	Input Common Mode Voltage Range		$V^+ - 1.7V$ $V^- + 1.7V$				V

± 15V AC Electrical Characteristics

The following specifications apply for supply voltage = ±15V, Vcm = V_O = 0V, R_f = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LM6182AM Limit (Note 6)	LM6182AI Limit (Note 6)	LM6182I Limit (Note 6)	Units
Xt	Crosstalk Rejection	(Note 7)	93				dB
BW	Closed Loop Bandwidth −3 dB	A_V = +2	100				MHz
		A_V = +10	75				
		A_V = −1	100				
		A_V = −10	60				
	Closed Loop Bandwidth 0.1 dB Flat, R_{SOURCE} = 200Ω	A_V = +2, R_L = 150Ω	35				
PBW	Power Bandwidth	A_V = −1, V_O = 5 V_{PP}	60				
SR	Slew Rate	Overdriven	2000				V/μs min
		A_V = −1, V_O = ±10V R_L = 150Ω, (Note 8)	1400	1000	1000	1000	
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±5V R_L = 150Ω	50				ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	5				
t_p	Propagation Delay Time	V_O = 1 V_{PP}	6				
in(+)	Non-Inverting Input Noise Current Density	f = 1 kHz	3				pA/√Hz
in(−)	Inverting Input Noise Current Density	f = 1 kHz	16				pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4				nV/√Hz
	Second Harmonic Distortion	V_O = 2 V_{PP}, f = 10 MHz A_V = +2	-50				dBc
	Third Harmonic Distortion	V_O = 2 V_{PP}, f = 10 MHz A_V = +2	-55				
	Differential Gain	R_L = 150Ω A_V = +2, NTSC	0.05				%
	Differential Phase	R_L = 150Ω A_V = +2, NTSC	0.04				Deg
THD	Total Harmonic Distortion	V_O = 2 V_{PP}, A_V = +2, f = 10 MHz, R_L = 150Ω	0.58				%

±5V DC Electrical Characteristics

The following specifications apply for supply voltage = ±5V, Vcm = V_O = 0V, R_f = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LM6182AM	LM6182AI	LM6182I	Units
				Limit (Note 6)	Limit (Note 6)	Limit (Note 6)	
V_{OS}	Input Offset Voltage		1.0	2.0 **3.0**	2.0 **2.5**	3.0 **3.5**	mV max
TCV_{OS}	Input Offset Voltage Drift		2.5				μV/°C
I_B	Inverting Input Bias Current		5.0	10 **22**	10 **22**	17.5 **27.0**	μA max
	Non-Inverting Input Bias Current		0.25	1.5 **3.0**	1.5 **3.0**	3.0 **5.0**	
TCI_B	Inverting Input Bias Current Drift		50				nA/°C
	Non-Inverting Input Bias Current Drift		3.0				
I_B PSR	Inverting Input Bias Current Power Supply Rejection	±4V ≤ V_S ≤ ±6V	0.3	0.5 **1.0**	0.5 **1.0**	0.75 **1.5**	μA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	±4V ≤ V_S ≤ ±6V	0.05	0.5 **1.0**	0.5 **1.0**	0.5 **1.5**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.3	0.5 **1.0**	0.5 **1.0**	1.0 **1.5**	
	Non-Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.12	0.5 **1.0**	0.5 **1.0**	0.5 **1.5**	
CMRR	Common Mode Rejection Ratio	−2.5V ≤ V_{CM} ≤ +2.5V	57	50 **47**	50 **47**	50 **47**	dB min
PSRR	Power Supply Rejection Ratio	±4V ≤ V_S ≤ ±6V	80	70 **67**	70 **67**	64 **60**	
R_O	Output Resistance	A_V = −1 f = 300 kHz	0.25				Ω
R_{IN}	Non-Inverting Input Resistance		8				MΩ
V_O	Output Voltage Swing	R_L = 1 kΩ	2.6	2.25 **2.0**	2.25 **2.0**	2.25 **2.0**	V min
		R_L = 150Ω	2.2	2.0 **1.8**	2.0 **1.8**	2.0 **1.8**	
I_{SC}	Output Short Circuit Current		100	65 **35**	65 **40**	65 **40**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.4	0.75 **0.3**	0.75 **0.35**	0.6 **0.3**	MΩ min
		R_L = 150Ω	1.0	0.5 **0.2**	0.5 **0.25**	0.4 **0.2**	
I_S	Supply Current	No Load, V_{IN} = 0V Both Amplifiers	13	17 **18.5**	17 **18.5**	17 **18.5**	mA max
V_{CM}	Input Common Mode Voltage Range		$V^+ - 1.7V$ $V^- + 1.7V$				V

±5V AC Electrical Characteristics

The following specifications apply for supply voltage = ±5V, Vcm = V_O = 0V, R_f = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LM6182AM Limit (Note 6)	LM6182AI Limit (Note 6)	LM6182I Limit (Note 6)	Units
Xt	Crosstalk Rejection	(Note 7)	92				dB
BW	Closed Loop Bandwidth −3 dB	A_V = +2	50				MHz
		A_V = +10	40				
		A_V = −1	55				
		A_V = −10	35				
	Closed Loop Bandwidth 0.1 dB Flat, R_{SOURCE} = 200Ω	A_V = +2, R_L = 150Ω	15				
PBW	Power Bandwidth	A_V = −1, V_O = 4 V_{PP}	40				
SR	Slew Rate	A_V = −1, V_O = ±2V R_L = 150Ω, (Note 8)	500	375	375	375	V/µs min
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±2V R_L = 150Ω	50				ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	8.5				
t_p	Propagation Delay Time	V_O = 1 V_{PP}	8				
in(+)	Non-Inverting Input Noise Current Density	f = 1 kHz	3				pA/√Hz
in(−)	Inverting Input Noise Current Density	f = 1 kHz	16				pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4				nV/√Hz
	Second Harmonic Distortion	V_O = 2 V_{PP}, f = 10 MHz A_V = +2	-45				dBc
	Third Harmonic Distortion	V_O = 2 V_{PP}, f = 10 MHz A_V = +2	-55				
	Differential Gain	R_L = 150Ω A_V = +2, NTSC	0.06				%
	Differential Phase	R_L = 150Ω A_V = +2, NTSC	0.16				Deg
THD	Total Harmonic Distortion	V_O = 2 V_{PP}, A_V = +2, f = 5 MHz, R_L = 150Ω	0.36				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model 100 pF and 1.5 kΩ.

Note 3: The typical junction-to-ambient thermal resistance of the molded plastic DIP(N) soldered directly into a PC board is 95°C/W. The junction-to-ambient thermal resistance of the S.O. surface mount (M) package mounted flush to the PC board is 70°C/W when pins 1,4,8,9 and 16 are soldered to a total of 2 in^2 1 oz copper trace. The S.O. (M) package must have pin 4 and at least one of pins 1,8,9, or 16 connected to V− for proper operation.

Note 4: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowable junction temperature of 150°C. Each amplifier of the LM6182 is short circuit current limited to 100 mA typical.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**boldface type**).

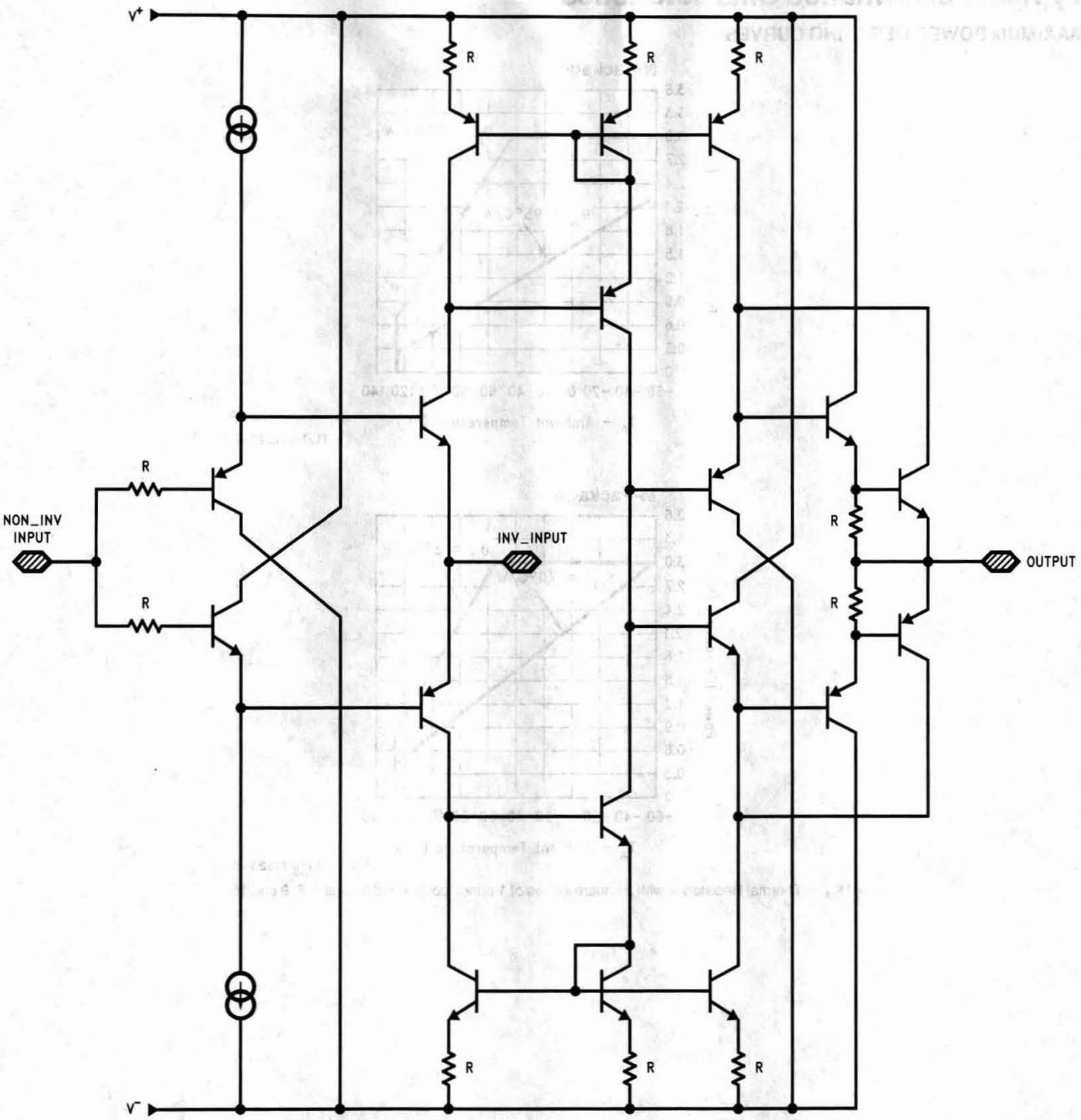
Note 7: Each amp excited in turn with 100 kHz to produce Vo = 2 Vpp. Results are input referred.

Note 8: Measured from +25% to +75% of output waveform.

Note 9: Also available per the Standard Military Drawing, 5962-9460301MCA.

Note 10: For guaranteed military specifications see military datasheet MNLM6182AM-X.

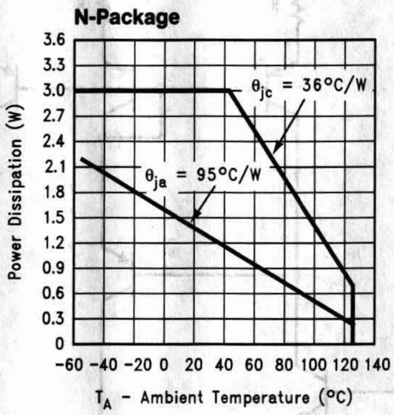
Simplified Schematic 1/2 LM6182


V⁺
V⁻
R
NON_INV INPUT
INV_INPUT
OUTPUT

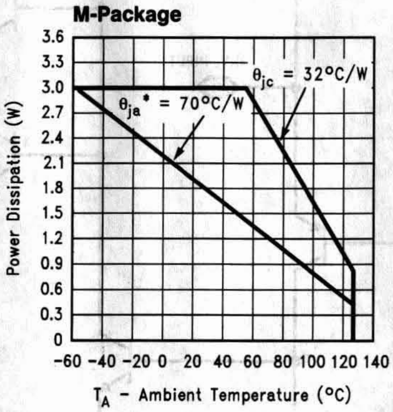
TL/H/11926–6

Typical Performance Characteristics

MAXIMUM POWER DERATING CURVES



TL/H/11926-7



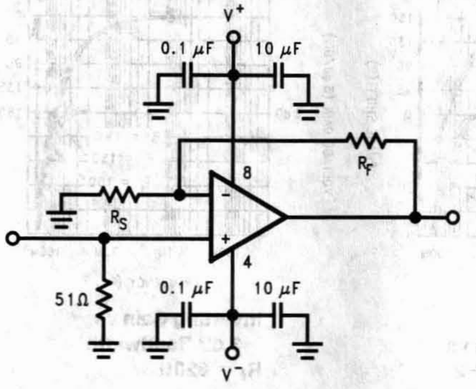
TL/H/11926-8

*θ_{ja} = Thermal Resistance with 2 square inches of 1 ounce copper tied to pins 1, 8, 9 and 16

Typical Performance Characteristics (Continued)

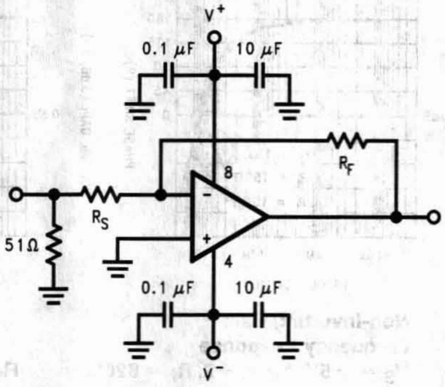
TYPICAL PERFORMANCE TEST CIRCUITS

Non-Inverting: Small Signal Pulse Response, Slew Rate, −3 dB Bandwidth


V+
0.1 μF
10 μF
R_F
8
R_S
−
+
4
51Ω
0.1 μF
10 μF
V−

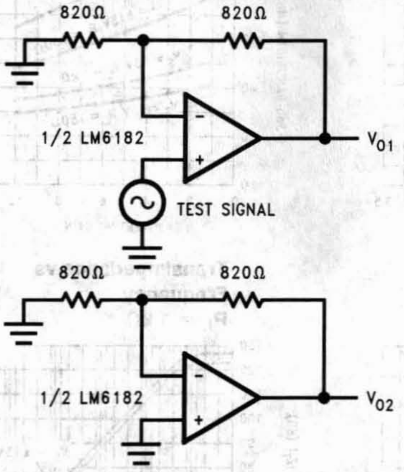
TL/H/11926–9

Inverting: Small Signal Pulse Response, Slew Rate, −3 dB Bandwidth


V+
0.1 μF
10 μF
R_F
8
R_S
−
+
51Ω
4
0.1 μF
10 μF
V−

TL/H/11926–10

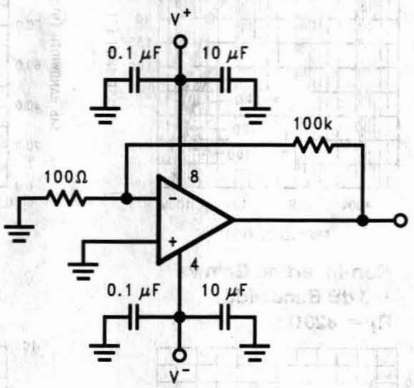
Amplifier-to-Amplifier Isolation


820Ω
820Ω
1/2 LM6182
V01
TEST SIGNAL
820Ω
820Ω
1/2 LM6182
V02

TL/H/11926–11

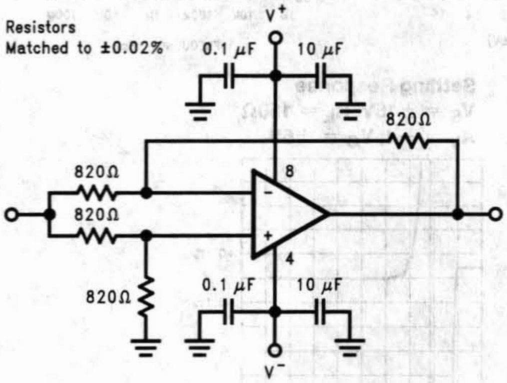
X_T (Crosstalk Rejection) $= \frac{V_{01}}{V_{02}}$

Input Voltage Noise


V+
0.1 μF
10 μF
100k
100Ω
8
−
+
4
0.1 μF
10 μF
V−

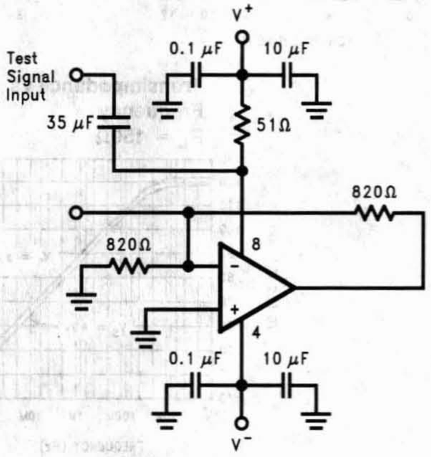
TL/H/11926–12

CMRR


Resistors
Matched to ±0.02%
V+
0.1 μF
10 μF
820Ω
820Ω
820Ω
8
−
+
4
820Ω
0.1 μF
10 μF
V−

TL/H/11926–13

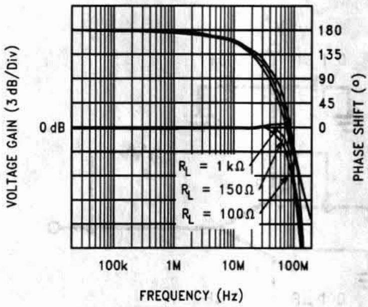
PSRR (V_{S+})


V+
0.1 μF
10 μF
Test
Signal
Input
35 μF
51Ω
820Ω
820Ω
8
−
+
4
0.1 μF
10 μF
V−

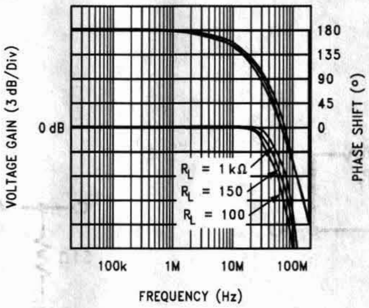
TL/H/11926–14

Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25°C$ unless otherwise noted.

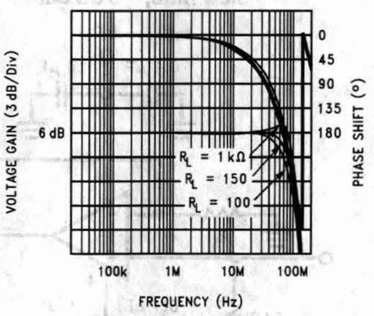
Inverting Gain Frequency Response $V_S = \pm 15V, A_V = -1, R_f = 820\Omega$



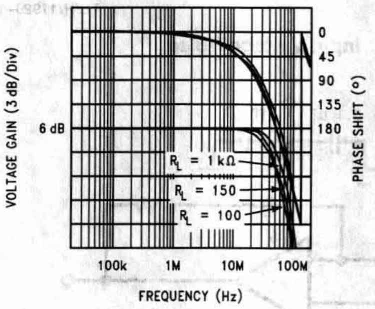
Inverting Gain Frequency Response $V_S = \pm 5V, A_V = -1, R_f = 820\Omega$



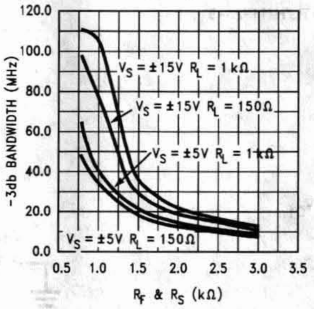
Non-Inverting Gain Frequency Response $V_S = \pm 15V, A_V = +2, R_f = 820\Omega$



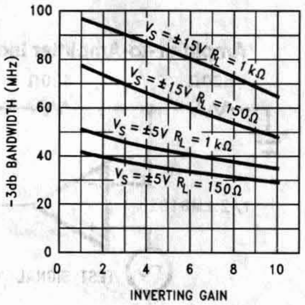
Non-Inverting Gain Frequency Response $V_S = \pm 5V, A_V = +2, R_f = 820\Omega$



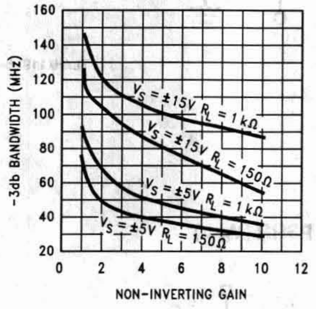
−3 dB Bandwidth vs R_f and R_s, $A_V = +2$



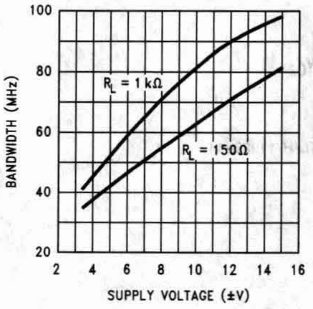
Inverting Gain vs −3 dB Bandwidth $R_f = 820\Omega$



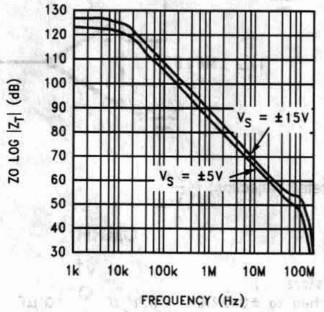
Non-Inverting Gain vs −3 dB Bandwidth $R_f = 820\Omega$



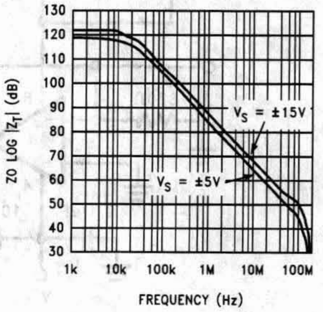
−3 dB Bandwidth vs Supply Voltage $A_V = -1$



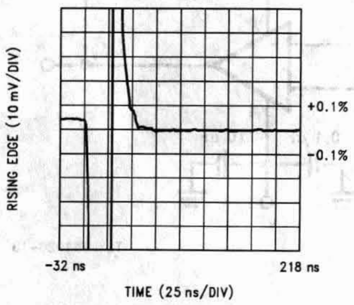
Transimpedance vs Frequency $R_L = 1\text{ k}\Omega$



Transimpedance vs Frequency $R_L = 150\Omega$



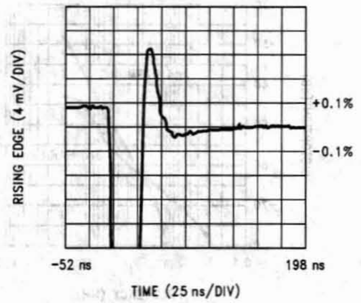
Settling Response $V_S = \pm 15V, R_L = 150\Omega$ $A_V = -1, V_O = \pm 5V$



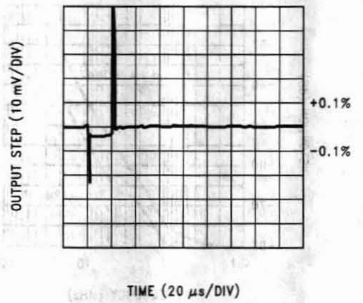
TL/H/11926–15

Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25°C$ unless otherwise noted.

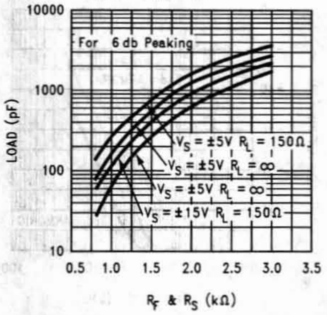
Settling Response $V_S = \pm 5V$, $R_L = 150\Omega$ $A_V = -1$, $V_O = \pm 2V$



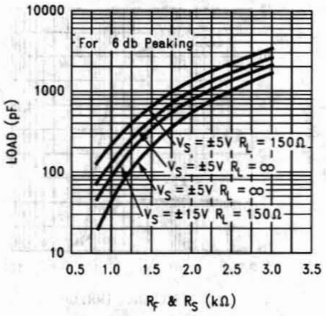
Long Term Settling Time Response $V_S = \pm 15V$, $R_L = 150\Omega$, $A_V = -1$, $V_O = \pm 5V$



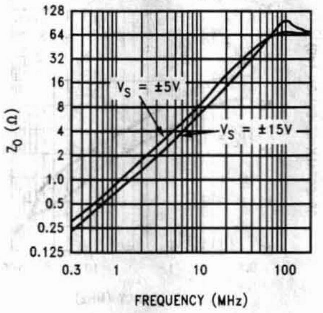
Suggested R_f and R_s for C_L, $A_V = -1$



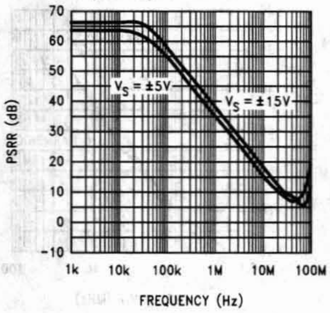
Suggested R_f and R_s for C_L, $A_V = +2$



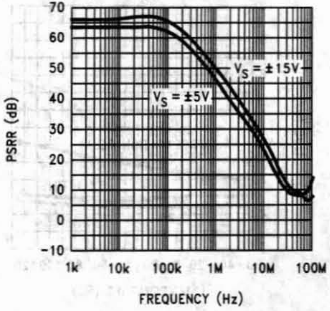
Output Impedance vs Frequency $A_V = -1$, $R_L = 820\Omega$



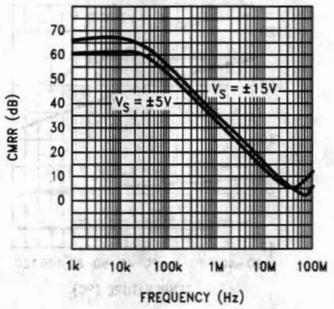
PSRR (V_{S+}) vs Frequency, $A_V = 2$, $R_f = R_s = 820\Omega$



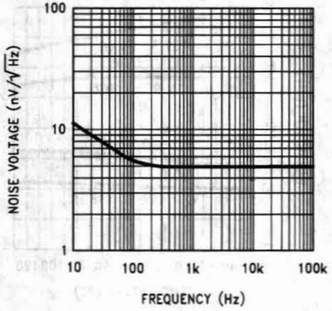
PSRR (V_{S-}) vs Frequency, $A_V = 2$, $R_f = R_s = 820\Omega$



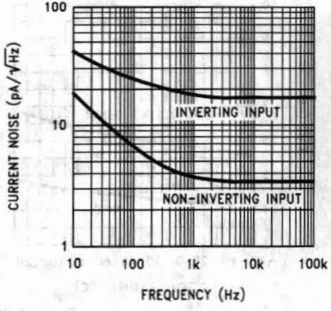
CMRR vs Frequency $R_f = R_s = 820\Omega$



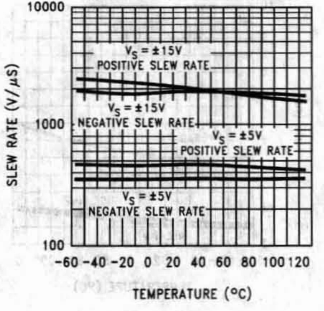
Input Voltage Noise vs Frequency



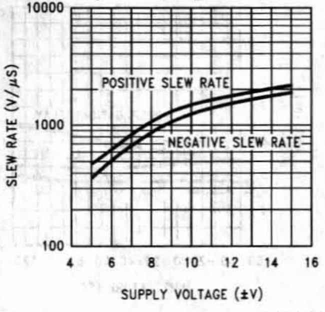
Input Current Noise vs Frequency



Slew Rate vs Temperature $A_V = -1$, $R_L = 150\Omega$



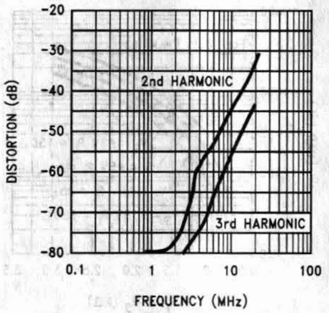
Slew Rate vs Supply Voltage $A_V = -1$, $R_L = 150\Omega$



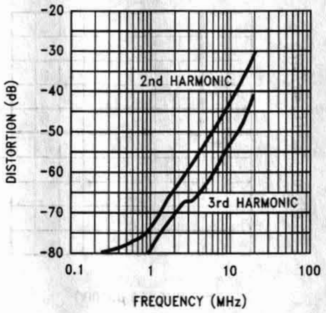
TL/H/11926–16

Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25°C$ unless otherwise noted.

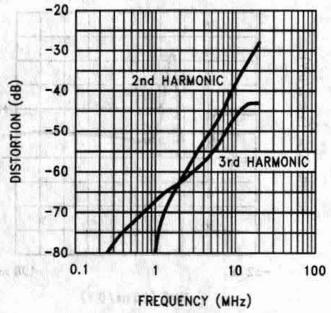
Distortion vs Frequency $V_S = \pm 15V, A_V = +2, R_L = 150\Omega, V_O = 2Vp\text{-}p$



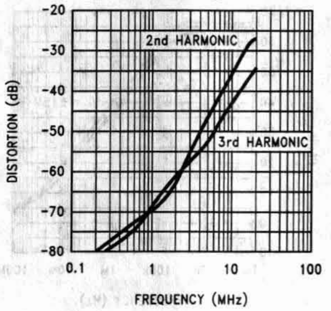
Distortion vs Frequency $V_S = \pm 15V, A_V = -1, R_L = 150\Omega, V_O = 2Vp\text{-}p$



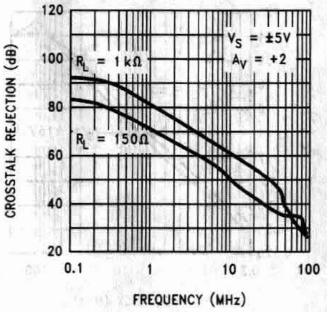
Distortion vs Frequency $V_S = \pm 5V, A_V = +2, R_L = 150\Omega, V_O = 2Vp\text{-}p$



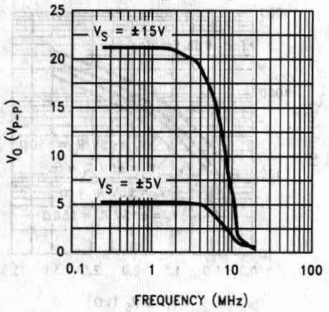
Distortion vs Frequency $V_S = \pm 5V, A_V = -1, R_L = 150\Omega, V_O = 2Vp\text{-}p$



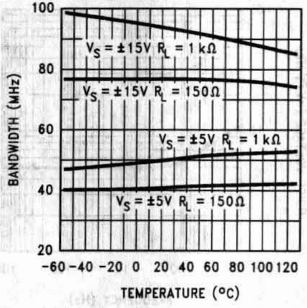
Crosstalk Rejection vs Frequency



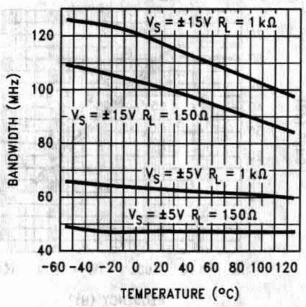
Maximum Output Voltage Swing vs Frequency (THD ≤ 1%)



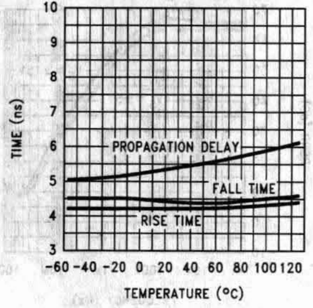
−3 dB Bandwidth vs Temperature, $A_V = -1$



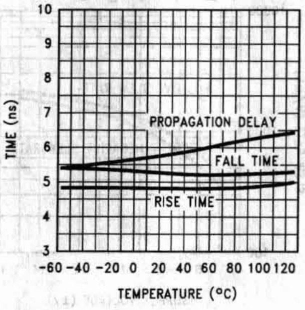
−3 dB Bandwidth vs Temperature, $A_V = +2$



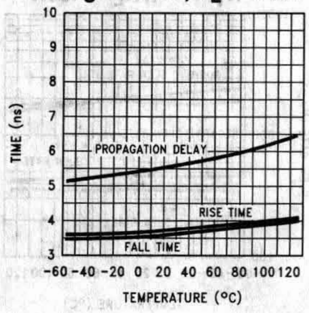
Small Signal Pulse Response vs Temperature, $A_V = -1$, $V_S = \pm 15V, R_L = 1 k\Omega$



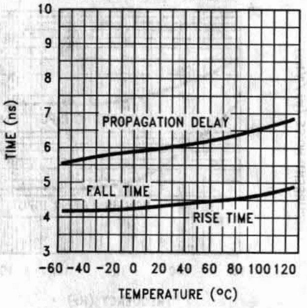
Small Signal Pulse Response vs Temperature, $A_V = -1$, $V_S = \pm 15V, R_L = 150\Omega$



Small Signal Pulse Response vs Temperature, $A_V = +2$, $V_S = \pm 15V, R_L = 1 k\Omega$



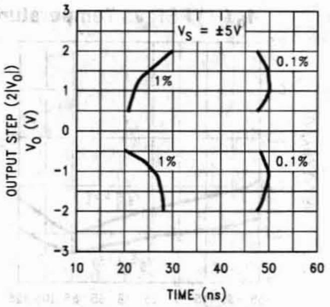
Small Signal Pulse Response vs Temperature, $A_V = +2$, $V_S = \pm 15V, R_L = 150\Omega$



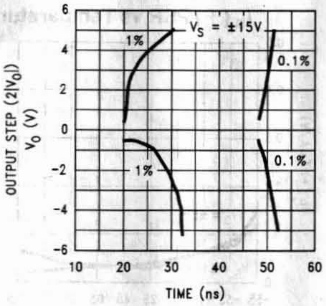
TL/H/11926-17

Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25°C$ unless otherwise noted.

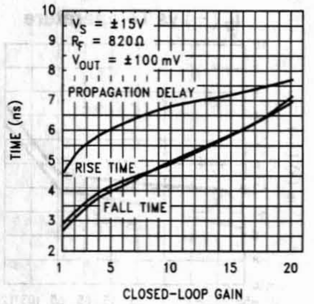
Settling Time vs Output Step, $R_F = 820\Omega$ $R_L = 150\Omega$, $A_V = -1$



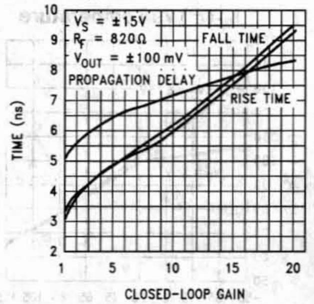
Settling Time vs Output Step, $R_F = 820\Omega$ $R_L = 150\Omega$, $A_V = -1$



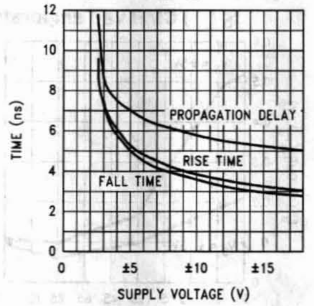
Small Signal Pulse Response vs Closed-Loop Gain $R_L = 1k$



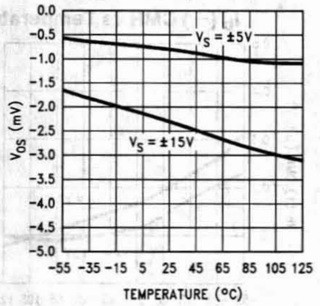
Small Signal Pulse Response vs Closed-Loop Gain $R_L = 150\Omega$



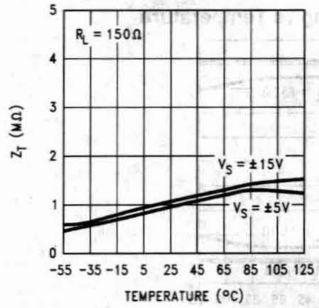
Small Signal Pulse Response vs Supply Voltage $A_V = +2$, $R_L = 1k$



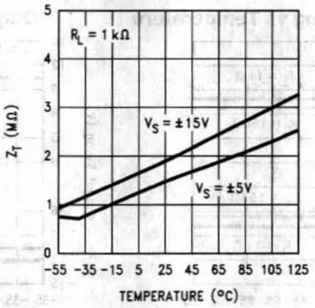
V_{OS} vs Temperature



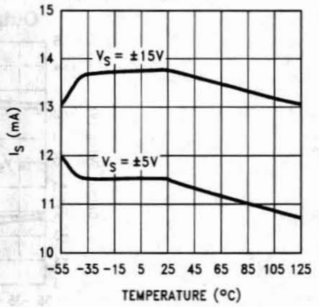
Z_t vs Temperature



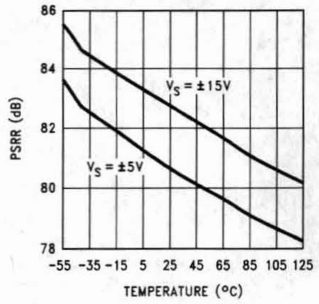
Z_t vs Temperature



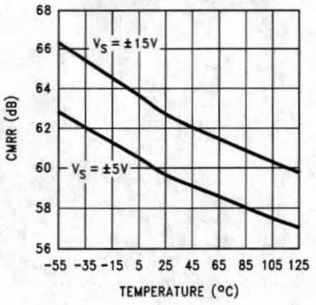
I_s vs Temperature



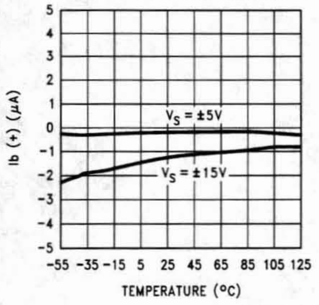
PSRR vs Temperature



CMRR vs Temperature



I_b (+) vs Temperature

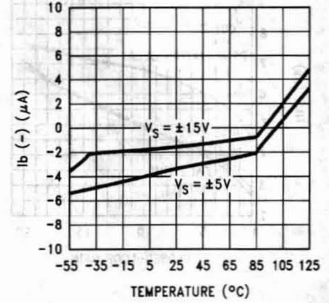


TL/H/11926-18

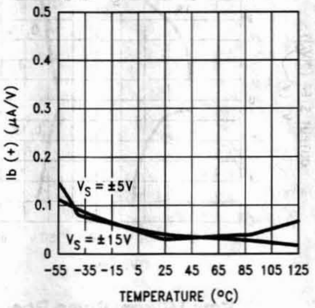
Typical Performance Characteristics

V_S = ±15V and T_A = 25°C unless otherwise noted. (Continued)

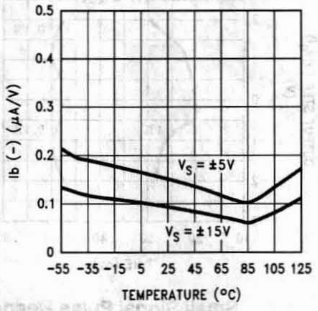
I_b (−) vs Temperature



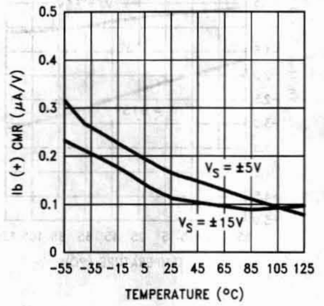
I_b (+) PSR vs Temperature



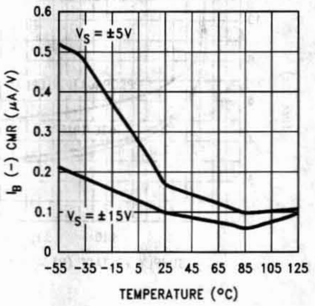
I_b (−) PSR vs Temperature



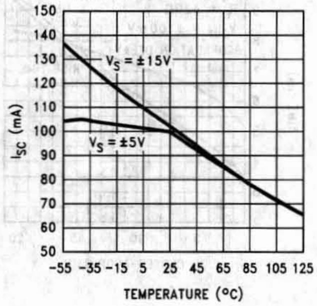
I_b (+) CMR vs Temperature



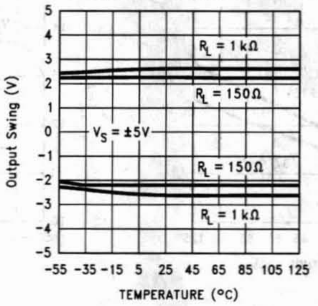
I_b (−) CMR vs Temperature



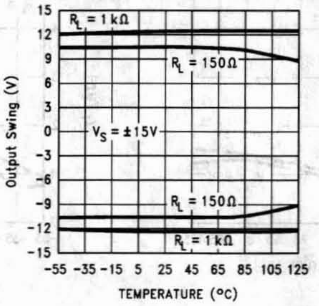
I_{sc}(±) vs Temperature



Output Swing vs Temperature



Output Swing vs Temperature

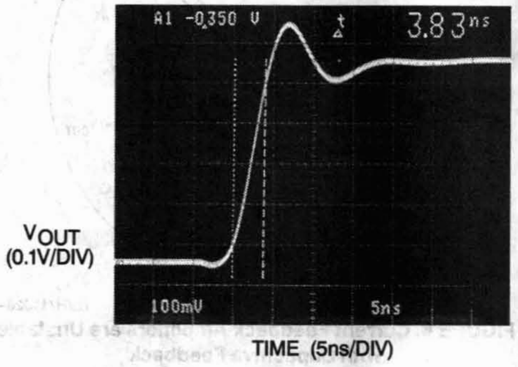


TL/H/11926–19

Typical Applications

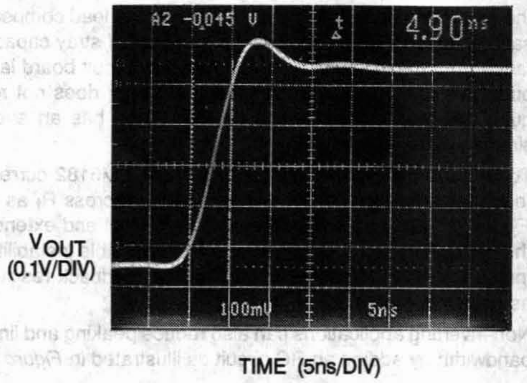
CURRENT FEEDBACK TOPOLOGY

For a conventional voltage feedback amplifier the resulting small-signal bandwidth is inversely proportional to the desired gain to a first order approximation based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6182, transcends this limitation to offer a signal bandwidth that is relatively independent of the closed loop gain. *Figures 1A* and *1B* illustrate that for closed loop gains of −1 and −5 the resulting pulse fidelity suggests quite similiar bandwidths for both configurations.



TL/H/11926–20

1A. $A_V = -1$



TL/H/11926–21

1B. $A_V = -5$

FIGURE 1A, 1B. Variation of Closed-Loop Gain from −1 to −5 Yields Similar Responses.

FEEDBACK RESISTOR SELECTION: R_f

Selecting the feedback resistor, R_f, is a dominant factor in compensating the LM6182. For general applications the LM6182 will maintain specified performance with an 820Ω feedback resistor. The closed-loop bandwidth of the LM6182 depends on the feedback resistance, R_f. Therefore, Rs, and not R_f, is varied to adjust for the desired closed-loop gain as demonstrated in *Figure 2.*

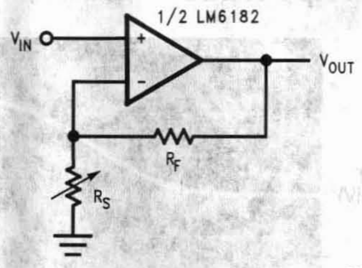


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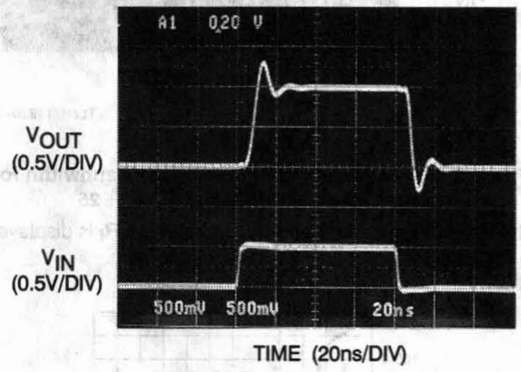
FIGURE 2. R_f Sets Amplifier Bandwidth and R_s is Adjusted to Obtain the Desired Closed-Loop Gain, A_V.

Although this R_f value will provide good results for most applications, it may be advantageous to adjust this value slightly. Consider, for instance, the effect on pulse responses with two different configurations where both the closed-loop gains are +2 and the feedback resistors are 820Ω, and 1640Ω, respectively. *Figures 3A* and *3B* illustrate the effect of increasing R_f while maintaining the same closed-loop gain – the amplifier bandwidth decreases. Accordingly, larger feedback resistors can be used to slow down the LM6182 and reduce overshoot in the time domain response. Conversely, smaller feedback resistance values than 820Ω can be used to compensate for the reduction of bandwidth at high closed-loop gains, due to 2nd order effects. For example *Figures 4A* and *4B* illustrate reducing R_f to 500Ω to establish the desired small signal response in an amplifier configured for a closed-loop gain of +25.



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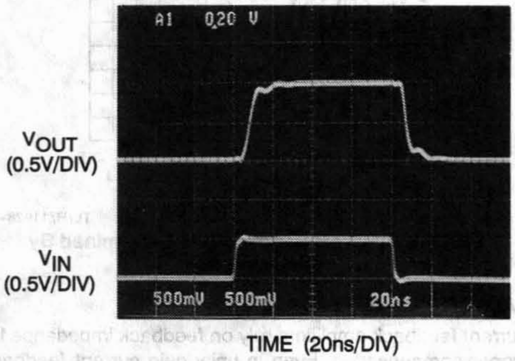
3A. R_f = 820Ω



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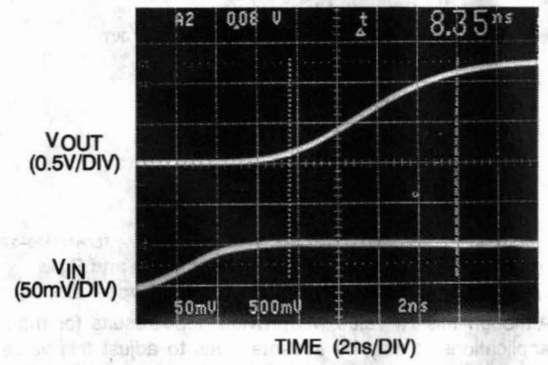
3B. R_f = 1640Ω

FIGURE 3A, 3B. Increase Compensation by Increasing R_f, A_V = +2

Typical Applications (Continued)



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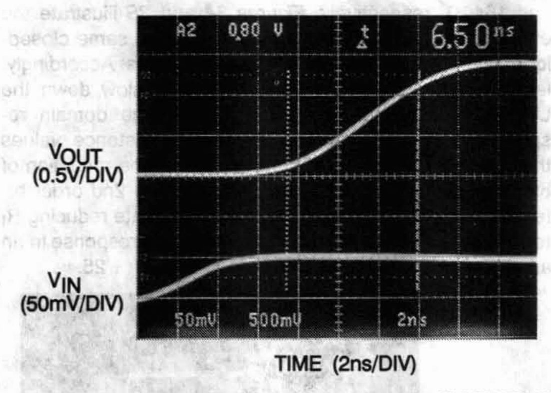
4A. $R_f = 820\Omega$



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4B. $R_f = 500\Omega$

FIGURE 4A, 4B. Reducing R_f to Increase Bandwidth for Large Closed-Loop Gains, $A_V = +25$

The extent of the amplifier's dependence on R_f is displayed in Figure 5 for one particular closed-loop gain.

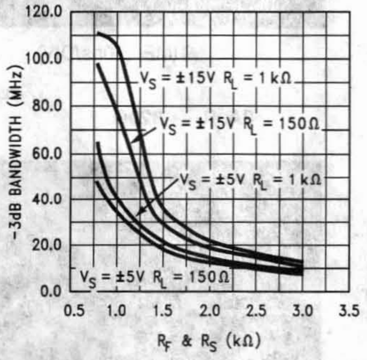

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FIGURE 5. −3 dB Bandwidth Is Determined By Selecting R_f.

CAPACITIVE FEEDBACK

Current feedback amplifiers rely on feedback impedance for proper compensation. Even in unity gain current feedback amplifiers require a feedback resistor. LM6182 performance is specified for a feedback resistance of 820Ω. Decreasing the feedback impedance below 820Ω extends the amplifier's bandwidth leading to possible instability. Capacitive feedback should therefore not be used because the impedance of a capacitor decreases with increasing frequency.

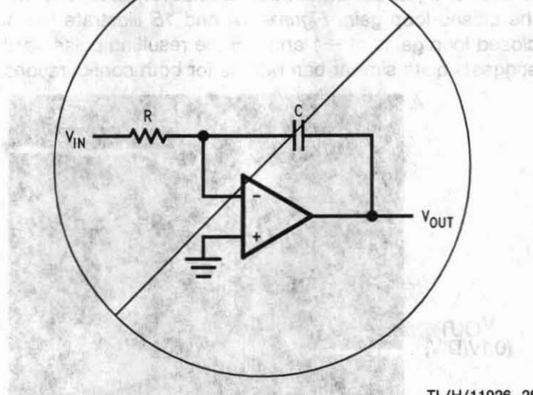

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FIGURE 6. Current Feedback Amplifiers are Unstable with Capacitive Feedback

For voltage feedback amplifiers it is quite common to place a small lead compensation capacitor in parallel with feedback resistance, R_f. This compensation serves to reduce the amplifier's peaking. One application of the lead compensation capacitor is to counteract the effects of stray capacitance from the inverting input to ground in circuit board layouts. The LM6182 current feedback amplifier does not require this lead compensation capacitor and has an even simpler, more elegant solution.

To limit the bandwidth and peaking of the LM6182 current feedback amplifier, do not use a capacitor across R_f as in *Figure 7.* This actually has the opposite effect and extends the bandwidth of the amplifier leading to possible instability. Instead, simply increase the value of the feedback resistor as shown in *Figure 3.*

Non-inverting applications can also reduce peaking and limit bandwidth by adding an RC circuit as illustrated in *Figure 8.*

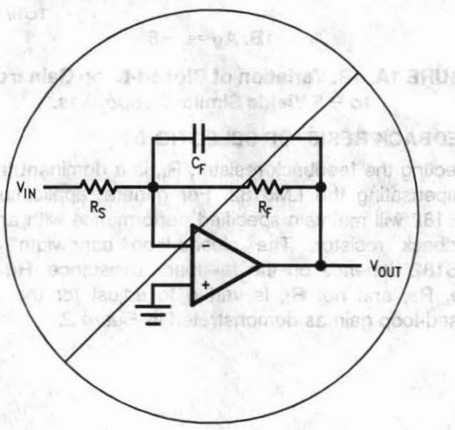

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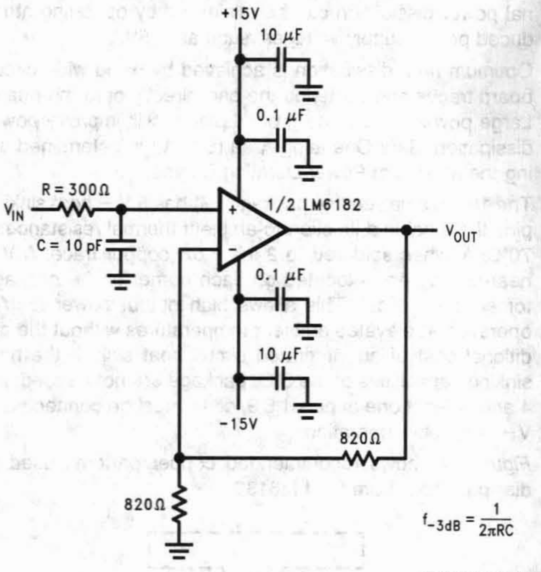
FIGURE 7. Compensation Capacitors Are Not Used with the LM6182, Instead Simply Increase R_f to Compensate

Typical Applications (Continued)



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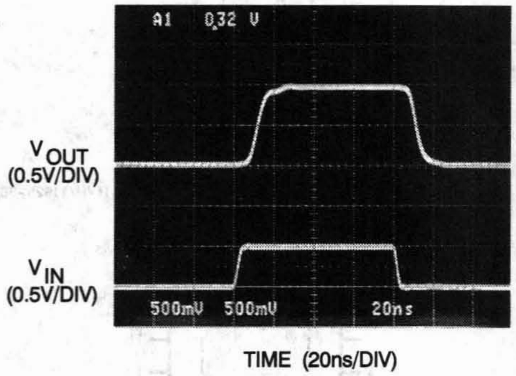
8A



TL/H/11926-31

8B

FIGURE 8A, 8B. RC Limits Amplifier Bandwidth to 50 MHz, Eliminating Peaking in the Resulting Pulse Response as Compared to *Figure 3A*

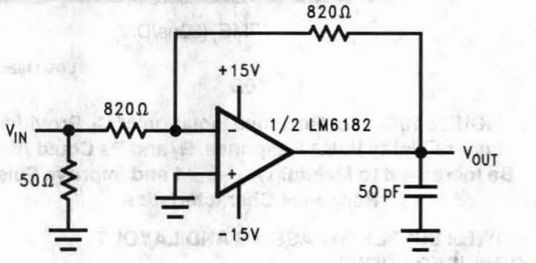
SLEW RATE CONSIDERATIONS

The slew rate characteristics of current feedback amplifiers are different than traditional voltage feedback amplifiers. In voltage feedback amplifiers, slew rate limiting or non-linear amplifier behavior is dominated by the finite availability of the 1st stage tail current charging the compensation capacitor. The slew rate of current feedback amplifiers, in contrast, is not constant. Transient current at the inverting input is proportional to the current available to the amplifier's compensation capacitor. The current feedback amplifier is therefore not traditionally slew rate limited. This enables large slew rates responses of 2000 V/μs. The non-inverting configuration slew rate is also determined by input stage limitations. Accordingly, variations of slew rates occur for different circuit topologies.

DRIVING CAPACITIVE LOADS

The LM6182 can drive significantly larger capacitive loads than many current feedback amplifiers. This is extremely valuable for simplifying the design of coax-cable drivers. Although the LM6182 can directly drive as much as 100 pF of load capacitance without oscillating, the resulting response will be a function of the feedback resistor value. *Figure 9B* illustrates the small-signal pulse response of the LM6182 while driving a 50 pF load. Ringing persists for approximately 100 ns. To achieve pulse responses with less ringing either the feedback resistor can be increased (see Typical Performance Characteristics "Suggested R_f and Rs for C_L"), or resistive isolation can be used (10Ω–51Ω typically works well). Either technique, however, results in lowering the system bandwidth.

Figure 10B illustrates the improvement obtained by using a 47Ω isolation resistor.



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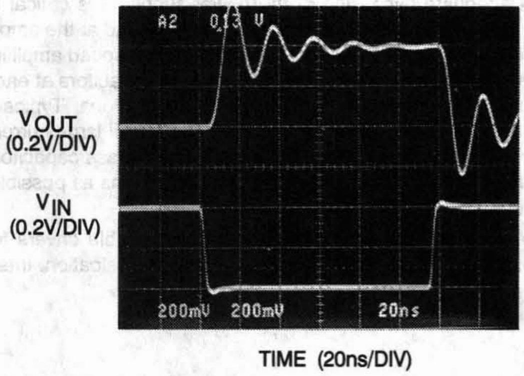
9A



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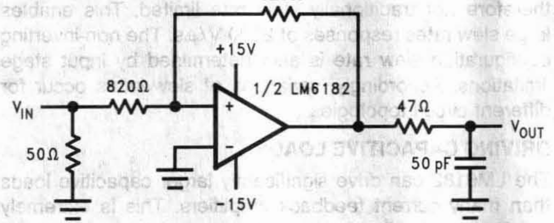
9B

FIGURE 9A, 9B. $A_V = -1$, LM6182 Can Directly Drive 50 pF of Load Capacitance with 100 ns of Ringing Resulting in Pulse Response

Typical Applications (Continued)



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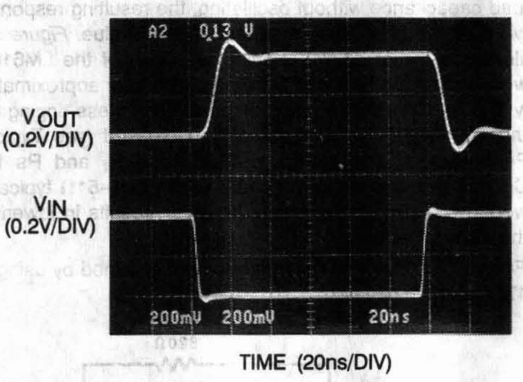
10A



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10B

FIGURE 10A, 10B. Resistive Isolation of C_L Provides Higher Fidelity Pulse Response. R_f and Rs Could Also Be Increased to Maintain $A_V = -1$ and Improve Pulse Response Characteristics.

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

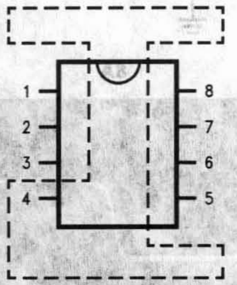
A fundamental requirement for high-speed amplifier design is adequate bypassing of the power supply. It is critical to maintain a wideband low-impedance to ground at the amplifiers supply pins to insure the fidelity of high speed amplifier transient signals. 0.1 μF ceramic bypass capacitors at each supply pin are sufficient for many applications. Typically 10 μF tantalum capacitors are also required if large current transients are delivered to the load. The bypass capacitors should be placed as close to the amplifier pins as possible, such as 0.5″ or less.

Applications requiring high output power, cable drivers for example, cause increased internal power dissipation. Internal power dissipation can be minimized by operating at reduced power supply voltages, such as ±5V.

Optimum heat dissipation is achieved by using wide circuit board traces and soldering the part directly onto the board. Large power supply and ground planes will improve power dissipation. Safe Operating Area (S.O.A.) is determined using the Maximum Power Derating Curves.

The 16-pin small outline package (M) has 5 V− heat sinking pins that enable a junction-to-ambient thermal resistance of 70°C/W when soldered to 2 in^2 1 oz. copper trace. A V− heat sinking pin is located on each corner of the package for ease of layout. This allows high output power and/or operation at elevated ambient temperatures without the additional cost of an integrated circuit heat sink. If the heat sinking capabilities of the S.O. package are not needed, pin 4 and at least one of pins 1,8,9, or 16 must be connected to V− for proper operation.

Figure 11 shows recommended copper patterns used to dissipate heat from the LM6182.



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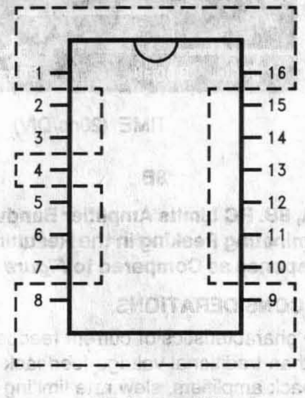
8-pin DIP (N)



TL/H/11926-37

16-pin S.O. (M)

FIGURE 11. Copper Heatsink Layouts

Typical Applications (Continued)

CROSSTALK REJECTION

The LM6182 has an excellant crosstalk rejection value of 62 dB at 10 MHz. This value is made possible because the LM6182 amplifiers share no common circuitry other than the supply. High frequency crosstalk that does appear is primarily caused by the magnetic and capacitive coupling of the internal bond wires. Bond wires connect the die to the package lead frame. The amount of current flowing through the bond wires is proportional to the amount of crosstalk. Therefore, crosstalk rejection ratings will degrade when driving heavy loads. *Figure 12* and shows a 10 dB difference for two different loads.

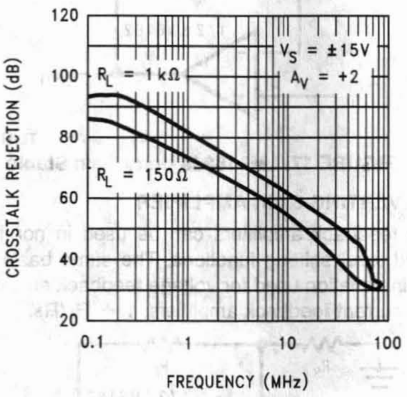


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FIGURE 12. Crosstalk Rejection

The LM6182 crosstalk effect is minimized in applications that cascade the amplifiers by preceding amplifier A with amplifier B.

START-UP TIME

Using the circuit in *Figure 13*, the LM6182 demonstrated a start-up time of 50 ns.

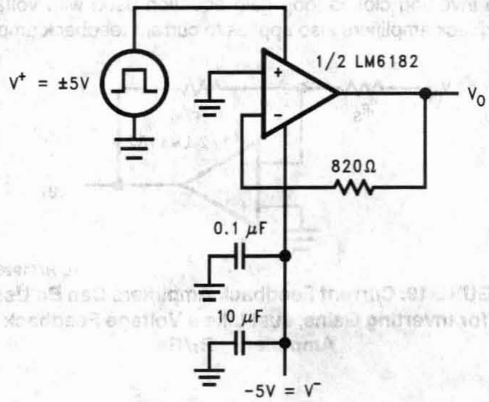

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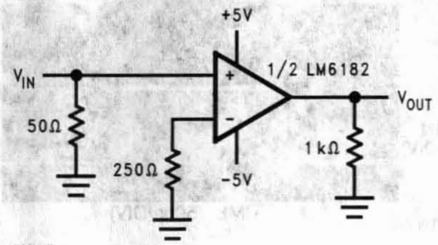
FIGURE 13. Start-Up Test Circuit

OVERDRIVE RECOVERY

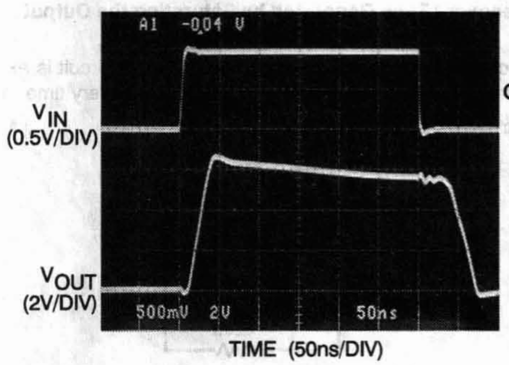
The LM6182 is an excellent choice for high speed applications needing fast overdrive recovery. Nanosecond recovery times allow the LM6182 to protect subsequent stages from excessive input saturation and possible damage.

When the output or input voltage range of a high speed amplifier is exceeded, the amplifier must recover from an overdrive condition. The non-linear output voltage remains as long as the overdrive condition persists. Linear operation resumes after the overdrive condition is removed. Overdrive recovery time is the delay before an amplifier returns to linear operation. The typical recovery times for exceeding open loop, closed loop, and input commom-mode voltage ranges are illustrated in *Figures 14, 15,* and *16.*

The open-loop circuit of *Figure 14* generates an overdrive response by allowing the ±0.5V input to exceed the linear input range of the amplifier. Typical positive and negative overdrive recovery times are 5 ns and 30 ns, respectively.



TL/H/11926-41

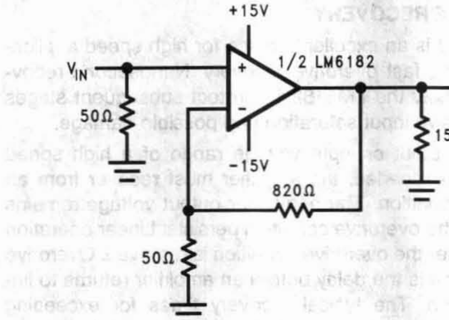


TL/H/11926-42

FIGURE 14. Open Loop Overdrive Recovery Times of 5 ns and 30 ns

The large closed-loop gain configuration in *Figure 15* forces the amplifier output into overdrive. The typical recovery time to a linear output value is 15 ns.

Typical Applications (Continued)



TL/H/11926-43

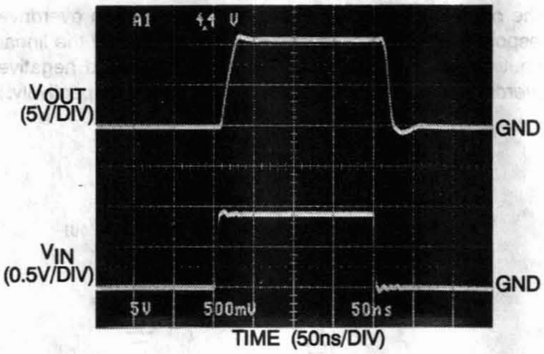


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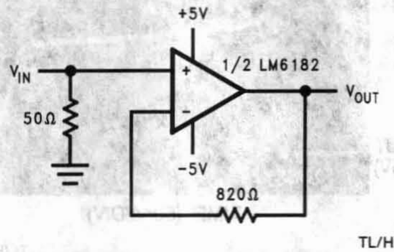
FIGURE 15. 15 ns Closed Loop Output Overdrive Recovery Time Generated by Saturating the Output Stage of the LM6182

The common-mode input range of a unity-gain circuit is exceeded by a 4V pulse resulting in a typical recovery time of 20 ns shown in *Figure 16*.



TL/H/11926-45

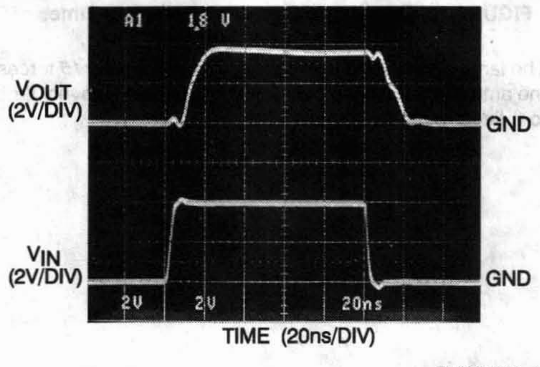


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FIGURE 16. Output Recovery from an Input that Exceeds the Common-Mode Range

SPICE MACROMODEL

A spice macromodel is available for the LM6182. Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Application Circuits

UNITY GAIN AMPLIFIER

The LM6182 current feedback amplifier is unity gain stable. The feedback resistor, R_f, is required to maintain the LM6182's dynamic performance.

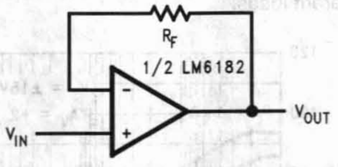

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FIGURE 17. LM6182 Is Unity Gain Stable

NON-INVERTING GAIN AMPLIFIER

Current feedback amplifiers can be used in non-inverting gain and level shifting functions. The same basic closed-loop gain equation used for voltage feedback amplifiers applies to current feedback amplifiers: $1 + R_f/Rs$.

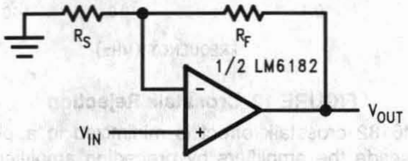

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FIGURE 18. Non-Inverting Closed Loop Gain is Determined with the Same Equation Voltage Feedback Amplifiers Use: $1 + R_f/Rs$

INVERTING GAIN AMPLIFIER

The inverting closed loop gain equation used with voltage feedback amplifiers also applies to current feedback amplifiers.

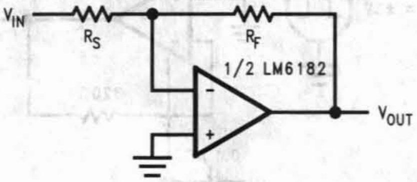

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FIGURE 19. Current Feedback Amplifiers Can Be Used for Inverting Gains, Just Like a Voltage Feedback Amplifier: $-R_f/Rs$

Typical Application Circuits (Continued)

SUMMING AMPLIFIER

The current feedback topology of the LM6182 provides significant performance advantages over a conventional voltage feedback amplifier used in a standard summing circuit. Using a voltage feedback amplifier, the bandwidth of the summing circuit in *Figure 20* is limited by the highest gain needed for either signal V1 or V2. If the LM6182 amplifier is used instead, wide circuit bandwidth can be maintained relatively independent of gain requirements.

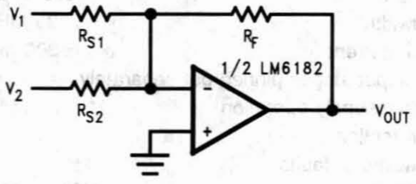

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FIGURE 20. LM6182 Allows the Summing Circuit to Meet the Requirements of Wide Bandwidth Systems Independent of Signal Gain

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-pin Molded DIP	LM6182AMN	LM6182AIN LM6182IN	N08E
16-pin Small Outline		LM6182AIM LM6182IM	M16A

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office or Distributors for availability and specifications.

National Semiconductor

LM6313 High Speed, High Power Operational Amplifier

General Description

The LM6313 is a high-speed, high-power operational amplifier. This operational amplifier features a 35 MHz small signal bandwidth, and 250 V/µs slew rate. A compensation pin is included for adjusting the open loop bandwidth. The input stage (A1) and output stage (A2) are pinned out separately, and can be used independently. The operational amplifier is designed for low impedance loads and will deliver ±300 mA. The LM6313 has both overcurrent and thermal shutdown protection with an error flag to signal both these fault conditions.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

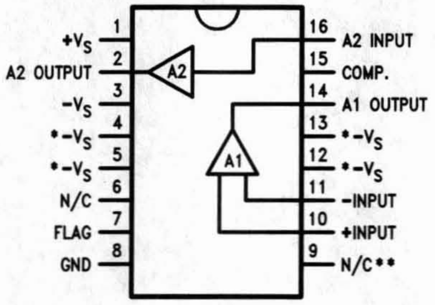
■ High slew rate	250 V/µs
■ Wide bandwidth	35 MHz
■ Peak output current	±300 mA
■ Input and output stages pinned out separately	
■ Single or dual supply operation	
■ Thermal protection	
■ Error flag warns of faults	
■ Wide supply voltage range	±5V to ±15V

Applications

- High speed ATE pin driver
- Data acquisition
- Driving capacitive loads
- Flash A-D input driver
- Precision 50Ω–75Ω video line driver
- Laser diode driver

Connection Diagram

Dual-In-Line Package



TL/H/10521-1

Top View

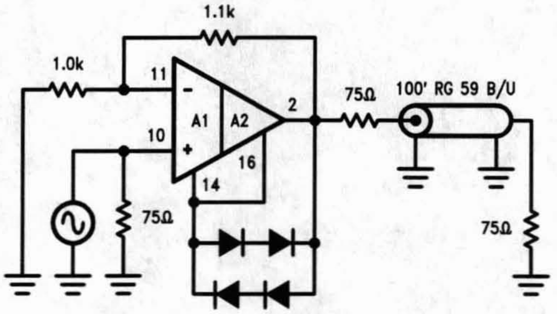
Order Number LM6313N
See NS Package Number N16A

*Heat sink pins

See Note 5 and Applications.

**Do not ground or otherwise connect to this pin.

Typical Application



TL/H/10521-2

Absolute Maximum Ratings (Note 1)

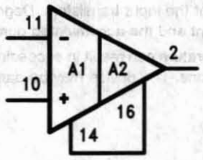
Total Supply Voltage ($+V_S$ to $-V_S$)	36V (±18)
A1 Differential Input Voltage (Note 2)	±7V
A1 Input Voltage	(V^+ −0.7) to (V^- −7V)
A2 Input to Output Voltage	±7V
A2 Input Voltage	$\pm V_S$
Flag Output Voltage	GND to $+V_S$
Short-Circuit to Ground	(Note 3)
Storage Temperature Range	$-65°C \leq T \leq +150°C$

Lead Temperature (Soldering, 5 seconds)	260°C
ESD Tolerance (Note 4)	
Pins 10 and 11	±600V
All Other Pins	±1500V
Operating Temperature Range	
LM6313N	0°C to 70°C
Thermal Derating Information (Note 5)	
θ_{JA}	40°C/W
T_J (Max)	125°C

Operational Amplifier DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. V_{CM} = 0V, R_S = 50Ω, the circuit configured as in *Figure 1*.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
V_{OS}	Input Offset Voltage		5	20	**22**	mV (Max)
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift		10			μV/°C
I_b	Input Bias Current		2	5	**7**	μA (Max)
I_{OS}	Input Offset Current		0.15	1.5	**1.9**	μA (Max)
$\Delta I_{OS}/\Delta T$	Average Input Offset Current Drift		0.4			nA/°C
R_{IN}	Input Resistance	Differential	325			kΩ
C_{IN}	Input Capacitance	A_V = +1, f = 10 MHz	2.2			pF
V_{CM}	Common-Mode Voltage Range		+14.2 −13.2	+13.8 −12.8	**+13.7** **−12.7**	V (Min)
A_{V1}	Voltage Gain 1	R_L = 1 kΩ, V_O = ±10V	6000	2500	**2000**	V/V (Min)
A_{V2}	Voltage Gain 2	R_L = 50Ω, V_O = ±8V	5000	2000	**1500**	
CMRR	Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	90	72	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	$\pm 5V \leq V_S \leq \pm 16V$	90	72	**70**	dB (Min)
V_{O1}	Output Voltage Swing 1	R_L = 1 kΩ	13.1	11.8	**11.2**	±V (Min)
V_{O2}	Output Voltage Swing 2	R_L = 100Ω	12.0	10.5	**10.0**	
V_{O3}	Output Voltage Swing 3	R_L = 50Ω	11.0	9.0	**8.5**	
I_S	Supply Current	T_J = 0°C			**24**	mA (Max)
		T_J = 25°C	18	23		
		T_J = 125°C			**21**	
I_{SC}	Peak Short-Circuit Output	(See *Figure 3*)	300			mA



TL/H/10521-3

FIGURE 1

Electrical Characteristics (Continued)

Operational Amplifier AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = 25°C$, and Supply Voltage $V_S = \pm 15V$. **Boldface** limits apply at temperature extremes. $V_{CM} = 0V$, $R_S = 50\Omega$, the circuit configured as in *Figure 1*.

Symbol	Parameter	Conditions	Typical	Units
GBW	Gain-Bandwidth Product	@ f = 30 MHz	35	MHz
SR	Slew Rate	$A_V = -1$, $R_L = 50\Omega$ (Note 6)	250	V/µs
PBW	Power Bandwidth	$V_{OUT} = 20\ V_{PP}$	3.0	MHz
t_S	Settling Time	10V Step to 0.1% (See *Figure 2*)	200	ns
	Phase Margin	$A_V = -1$, $R_L = 1\ k\Omega$, $C_L = 50\ pF$	53	Deg
	Differential Gain		0.1	%
	Differential Phase		0.1	Deg
e_n	Input Noise Voltage	f = 10 kHz	14	nV/√Hz
i_n	Input Noise Current	f = 10 kHz	1.8	pA/√Hz

A1 DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = 25°C$, and Supply Voltage $V_S = \pm 15V$. **Boldface** limits apply at temperature extremes. $V_{CM} = 0V$, $R_S = 50\Omega$.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$ $V_{OUT} = \pm 10V$, $R_L = \infty$	650 6000	300 2500	**250** **2000**	V/V (Min)
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	90	72	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	$\pm 5V \le \pm V_S \le +16V$	90	72	**70**	dB (Min)
I_{SC}	Output Short Circuit Current		±60	±30	**±25**	mA (Min)

A1 AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = 25°C$, and Supply Voltage $V_S = \pm 15V$. **Boldface** limits apply at temperature extremes. $R_S = 50\Omega$.

Symbol	Parameter	Conditions	Typical	25°C Limit	Units
GBW	Gain-Bandwidth	f = 30 MHz	37	25	MHz (Min)
SR	Slew Rate	$A_V = +1$, $R_L = 100\ k\Omega$, $\pm 4\ V_{IN}$, $\pm 2\ V_{OUT}$	250	150	V/µs (Min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test condition listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors. Degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise) is proportional to the level of the externally limited breakdown current and the accumulated duration of the breakdown condition.

Note 3: Continuous short-circuit operation of A1 at elevated temperature can result in exceeding the maximum allowed junction temperature of 125°C. A2 contains current limit and thermal shutdown to protect against fault conditions. The device may be damaged by shorts to the supplies.

Note 4: Human body model, C = 100 pF, $R_S = 1500\Omega$.

Electrical Characteristics (Continued)

A2 DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
A_{V1}	Voltage Gain 1	R_L = 1 kΩ, V_{IN} = ±10V	0.99	0.97	**0.95**	V/mV (Min)
A_{V2}	Voltage Gain 2	R_L = 50Ω, V_{IN} = ±10V	0.9	0.85	**0.82**	V/V (Min)
V_{OS}	Offset Voltage	R_L = 1 kΩ	15	70	**100**	mV (Max)
I_b	Input Bias Current	R_L = 1 kΩ, R_S = 10 kΩ	1	6	**8**	μA (Max)
R_{IN}	Input Resistance	R_L = 50Ω	5			MΩ
C_{IN}	Input Capacitance		3.5			pF
R_O	Output Resistance	I_{OUT} = ±10 mA	3.5	5.0	**8.0**	Ω (Min)
V_O	Voltage Output Swing	R_L = 1 kΩ R_L = 100Ω R_L = 50Ω	13.7 12.5 11.0	13.0 10.5 9.0	**12.7** **10.0** **8.5**	V (Min)
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±16V	70	60	**50**	dB (Min)

A2 AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	Units
SR 1 SR 2	Slew Rate 1 Slew Rate 2	V_{IN} = ±11V, R_L = 1 kΩ V_{IN} = ±11V, R_L = 50Ω (Note 7)	1200 750	 550	V/μs (Min)
BW	−3 dB Bandwidth	V_{IN} = ±100 mVpp R_L = 50Ω, C_L ≤ 10 pF	65	30	MHz (Min)
t_r, t_f	Rise Time Fall Time	R_L = 1 kΩ, C_L ≤ 10 pF V_O = 100 mVpp	8		ns
P_D	Propagation Delay	R_L = 50Ω, C_L ≤ 10 pF V_O = 100 mVpp	4		ns
	Overshoot	R_L = 1 kΩ, C_L = 100 pF R_L = 50Ω, C_L = 1000 pF	13 21		%

Additional (A2) Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
V_{OL}	Flag Pin Output Low Voltage	I_{SINK} Flag Pin = 500 μA	220	340	**400**	mV (Max)
I_{OH}	Flag Pin Output High Current	V_{OH} Flag Pin = 15V (Note 8)	0.01	10	**20**	μA (Max)

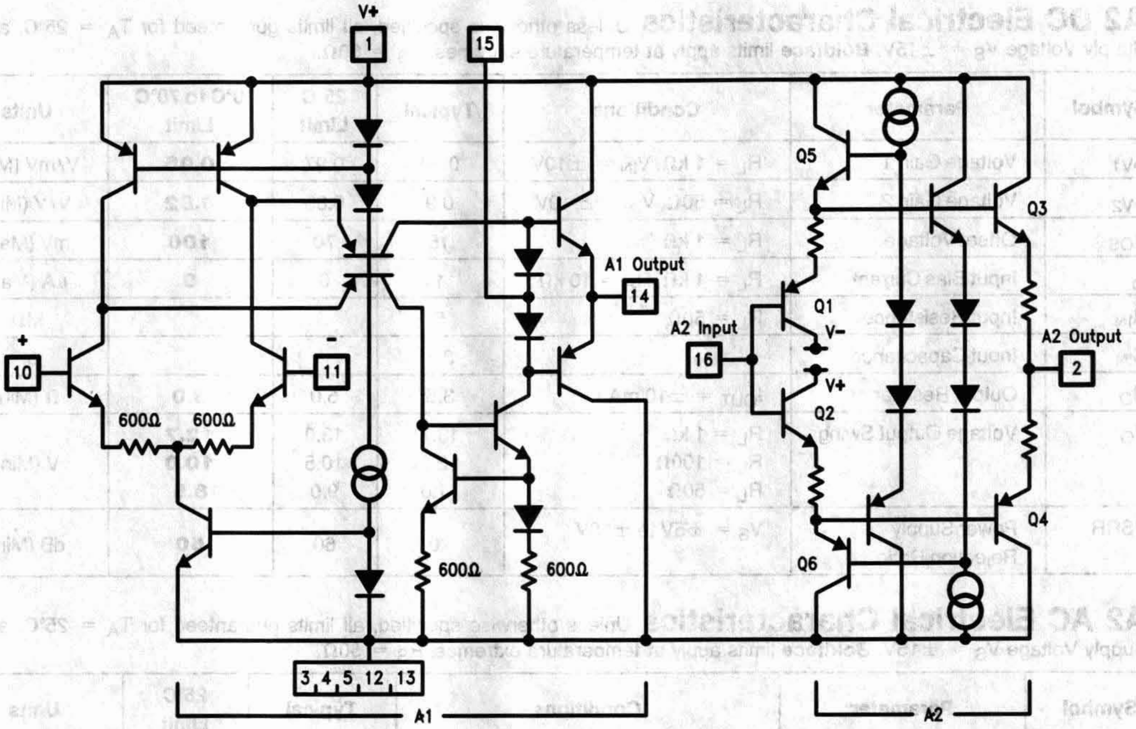
Note 5: For operation at elevated temperature, these devices must be derated to insure $T_J \leq 125°C$. $T_J = T_A + (P_D \times \theta_{JA})$. θ_{JA} for the N package mounted flush to the PCB, is 40°C/W when pins 4, 5, 12 and 13 are soldered to a total of 2 in^2 of copper trace.

Note 6: Measured between ±5V.

Note 7: V_{IN} = ±9V step input, measured between ±5V out.

Note 8: The error flag is set during current limit or thermal shut-down. The flag is an open collector, low on fault.

Simplified Schematic


V+
1
15
A1 Output
14
A2 Input
16
Q1
Q2
Q3
Q4
Q5
Q6
V−
V+
A2 Output
2
+
10
−
11
600Ω
600Ω
600Ω
600Ω
3, 4, 5, 12, 13
A1
A2

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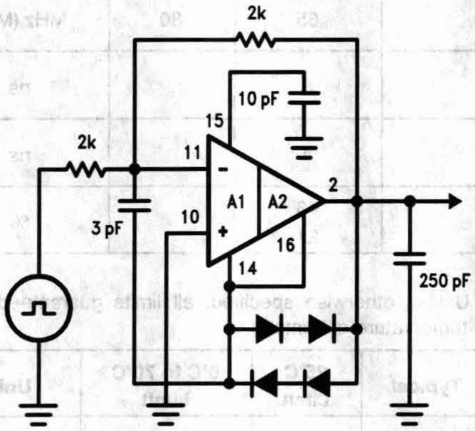
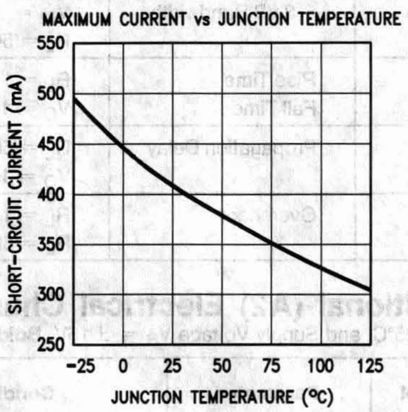
Settling Time Test Circuit


2k
10 pF
15
2k
11
−
A1
A2
2
10
+
16
14
3 pF
250 pF

TL/H/10521–5

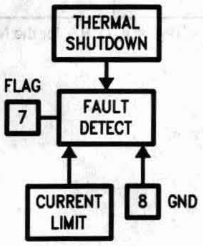
FIGURE 2



TL/H/10521–6

FIGURE 3

Protection Circuit Block Diagram

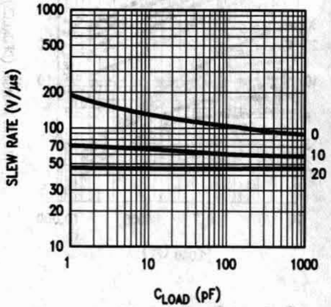

THERMAL SHUTDOWN
FLAG
7
FAULT DETECT
CURRENT LIMIT
8
GND

TL/H/10521–7

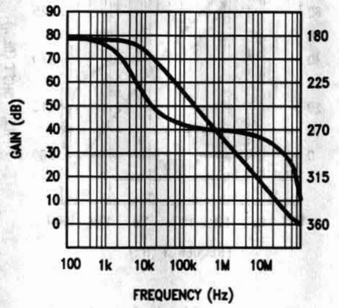
Typical Performance Characteristics Op Amp

(Unless otherwise specified, $T_A = 25°C$, $V_S = \pm 15V$, and $R_L = 10\ k\Omega$.)

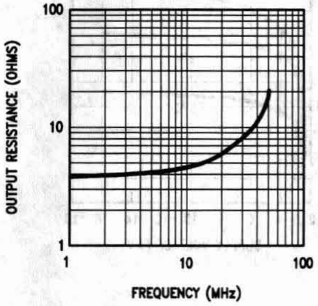
Slew Rate vs Capacitive Load



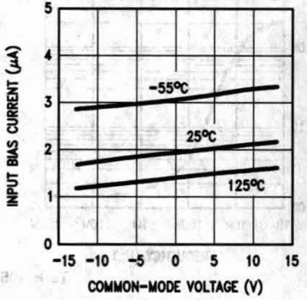
Bode Plot



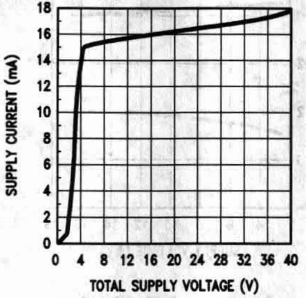
Output Resistance (Open Loop)



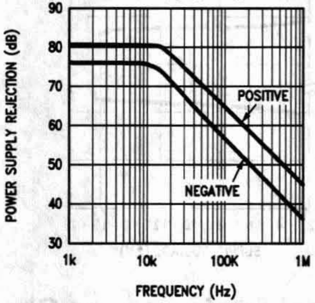
Bias Current vs Common-Mode Voltage



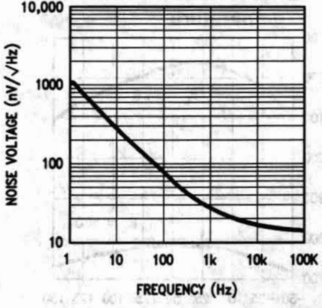
Supply Current vs Supply Voltage



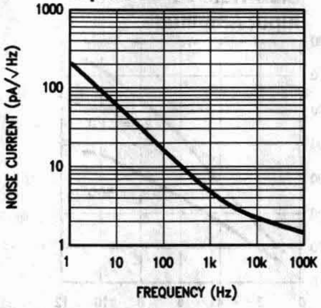
Power Supply Rejection



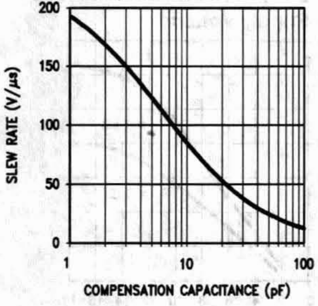
Input Noise Voltage



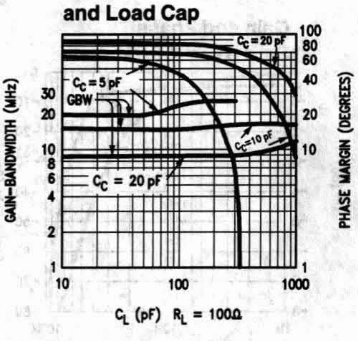
Input Noise Current



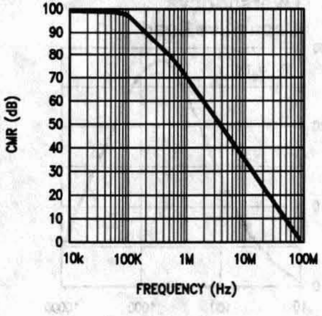
Slew Rate vs Compensation



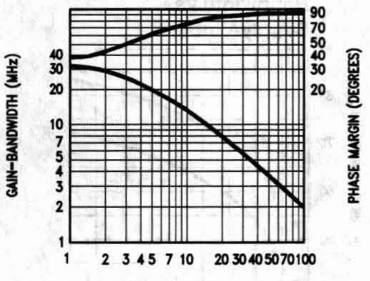
Gain-Bandwidth, Phase Margin vs Comp Cap and Load Cap



CMR vs Frequency



GBW and Phase Margin vs Comp Cap

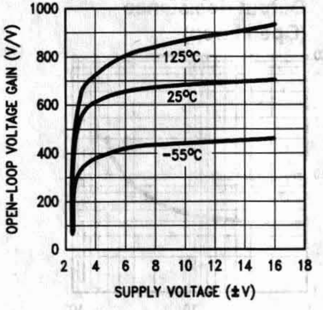


TL/H/10521–8

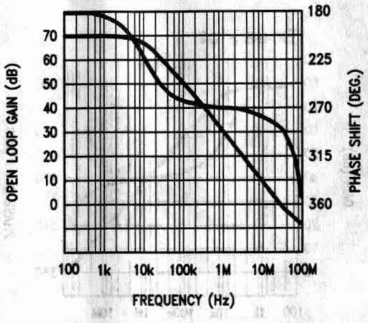
Typical Performance Characteristics A1 Only

(Unless otherwise specified, T_A = 25°C, V_S = ±15V, and R_L = 10 kΩ.)

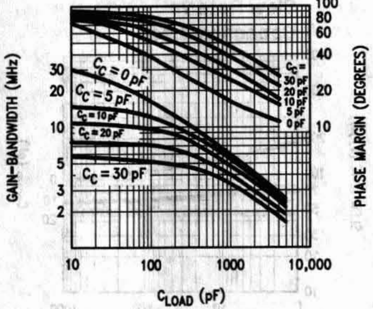
Gain vs Supply Voltage



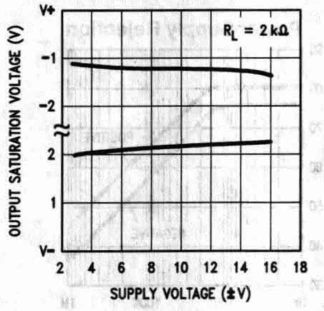
Bode Plot



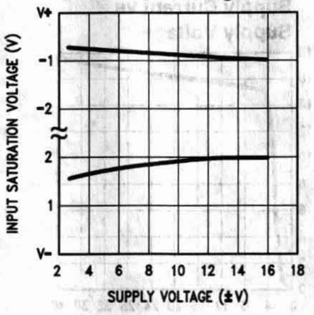
Gain-Bandwidth and Phase Margin vs Load Capacity



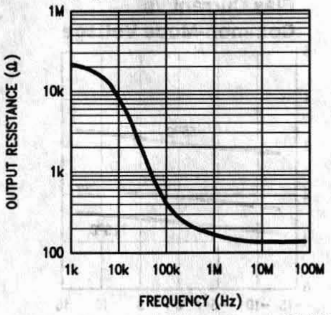
Output Saturation Voltage



Common-Mode Input Saturation Voltage



Output Resistance (Open Loop)

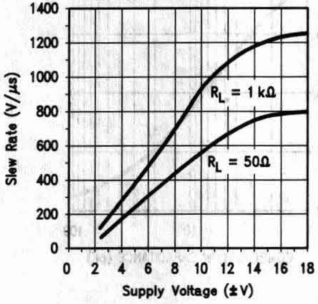


TL/H/10521–9

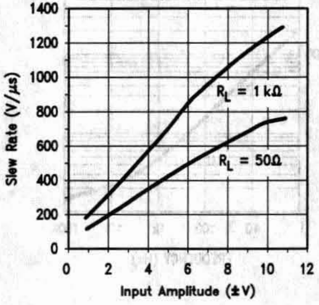
Typical Performance Characteristics A2 Only

(Unless otherwise specified, T_A = 25°C and V_S = ±15V.)

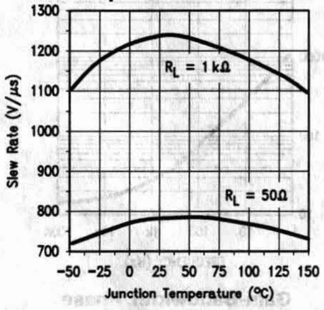
Slew Rate vs Supply Voltage



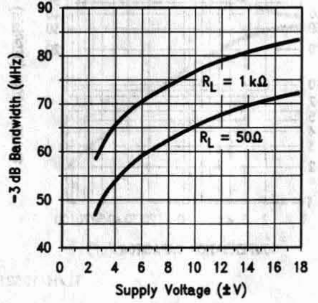
Slew Rate vs Input Amplitude



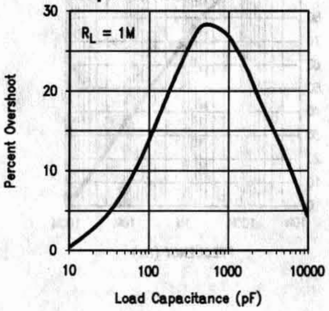
Slew Rate vs Temperature



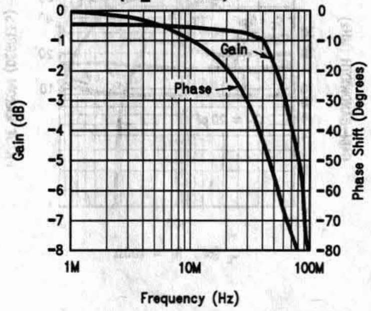
Bandwidth vs Supply Voltage



Overshoot vs Capacitive Load



Gain and Phase Shift (R_L = 50Ω)



TL/H/10521–10

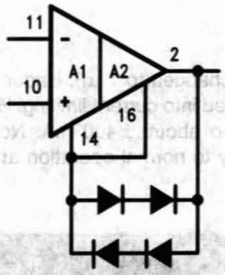
Application Hints

The LM6313 is a high-speed, high power operational amplifier that is designed for driving low-impedance loads such as 50Ω and 75Ω cables. Available in the standard, low cost, 16-pin DIP, this amplifier will drive back terminated video cables with up to 10 Vp-p. The ability to add additional compensation allows the LM6313 to drive capacitive loads of any size at bandwidths previously possible only with very expensive hybrid devices.

The LM6313 is excellent for driving high-speed flash A-to-D converters that require low-impedance drive at high frequencies. At 1 MHz, when used as a buffer, the LM6313 output impedance is below 0.1Ω. This very low output impedance also means that cables can be accurately back-terminated by just placing the characteristic impedance in series with the LM6313 output.

OVER-VOLTAGE PROTECTION

If the LM6313 is being operated on supply voltages of greater than ±5V, the possibility of damaging the output stage transistors exists. At higher supply voltages, if the output is shorted or excessive power dissipation causes the output stage to shut down, the maximum A2 input-to-output voltage, can be exceeded. This occurs when the input stage tries to drive the output while the output is at ground. To prevent this from happening, an easy solution is to place diodes around the output stage (See *Figure 4*). This will limit the maximum differential voltage to about 1.3V. Any signal diode, such as the 1N914 or the 1N4148 will work fine.



TL/H/10521-11

FIGURE 4

HEAT SINKING

When driving a low impedance load such as 50Ω, and operating from ±15V supplies, the internal power dissipation of the LM6313 can rise above 3W. To prevent overheating of the chip, which would cause the thermal protection circuitry to shut the system down, the following guidelines should be followed:

1. Reduce the supply voltage. The LM6313 will operate with little change in performance, except output voltage swing, on ±5V supplies. This will reduce the dissipation to the level where no precautions against overheating are necessary for loads of 10Ω or more.
2. Solder pins 4, 5, 12 and 13 to copper traces which are at least 0.100 inch wide and have a total area of at least 2 square inches, to obtain a θ_{JA} of 40°C/W. These four pins are connected to the back of the chip and will be at V−. They should not be used as a V− connection unless pin 3 is also connected to this same point.

SUPPLY BYPASSING

Because of the large currents required to drive low-impedance loads, supply bypassing as close as possible to the I.C. is important. At 50 MHz, a few inches of wire or circuit trace can have 20Ω or 30Ω of inductive reactance. This inductance in series with a 0.1 μF bypass capacitor can resonate at 1 MHz to 2 MHz and just appear as an inductor at higher frequencies. A 0.1 μF and a 10μF to 15 μF capacitor connected in parallel and as close as possible to the LM6313 supply pins, from each supply to ground, will give best performance.

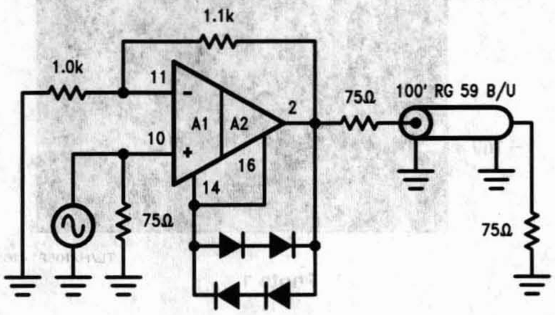
SELECTION OF COMPENSATION CAPACITOR

The compensation pin, pin 15, makes it possible to drive any load at any closed loop gain without stability problems. In most cases, where the gain is −1 or greater and the load is resistive, no compensation capacitor is required. When used at unity gain or when driving reactive loads, a small capacitor of 5 pF to 20 pF will insure optimum performance. The easiest way to determine the best value of compensation capacitor is to temporarily connect a trimmer capacitor (typical range of 2 pF to 15 pF) between pin 15, and ground, and adjust it for little or no overshoot at the output while driving the input with a square wave.

If the actual load capacitance is known, the typical graphs "Gain-Bandwidth and Phase Margin vs. Load Capacitance" can be used to select a value.

VIDEO CABLE DRIVER

The LM6313 is ideally suited for driving 50Ω or 75Ω cables. Unlike a buffer that requires a separate gain stage to make up for the losses involved in termination, the LM6313 gain can be set to 1 plus the line losses when the transmission line is end-terminated. If back-termination is needed, adding the line impedance in series with the output and raising the gain to 2 plus the expected line losses will provide a 0 dB loss system. *Figure 5* illustrates the back and end terminated video system including compensation for line losses. The excellent stability of the LM6313 with changes in supply voltages allow running the amplifier on unregulated supplies. The typical change in phase shift when the supplies are changed from ±5V to ±15V is less than 3° at 10 MHz.



TL/H/10521-12

FIGURE 5

Application Hints (Continued)

LASER DIODE MODULATOR

Figure 6 is a minimum component count example of a video modulator for a CW laser diode. This example biases the diode at 200 mA and modulates the current at ±200 mA per volt of signal. If it is desired to reduce power consumption and ±5V supplies are available, all that is necessary is to change R2 to 5 kΩ and R4 to 15Ω.

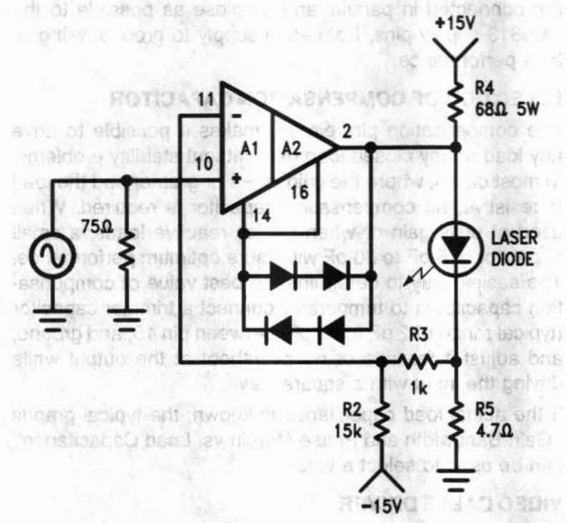


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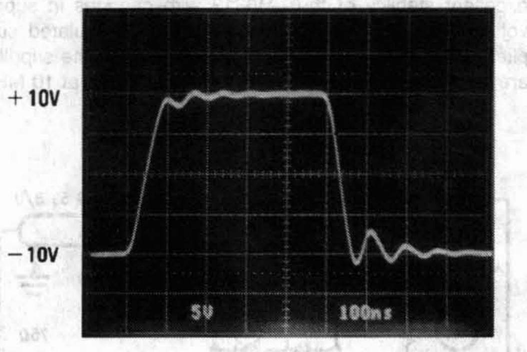
FIGURE 6

In photo 1, C_L is 1000 pF. The LM6313 is slewing at 250 V/µs, from −5V to +5V. The slew rate is 450 V/µs from +5V to −5V. This requires the op amp to deliver 450 mA into the load and remain stable.

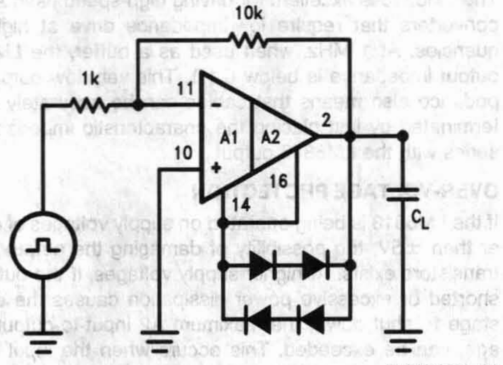


TL/H/10521–16

Photo 1

CAPACITIVE LOAD DRIVING

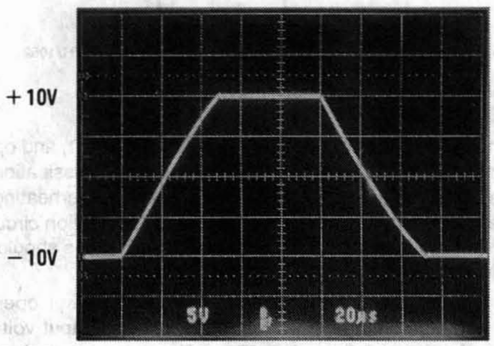
Figure 7 is the circuit used to demonstrate the ability of the LM6313 to drive capacitive loads at speeds not previously possible with monolithic op amps.



TL/H/10521–14

FIGURE 7

In photo 2, C_L is changed to 1 µF. Under these conditions, the op amp is forced into current limiting. Here the current is internally limited to about ±400 mA. Note the rapid and complete recovery to normal operation at the end of slewing.



TL/H/10521–15

Photo 2

National Semiconductor

ADVANCE INFORMATION

LM7121
Tiny Very High Speed Low Power Voltage Feedback Amplifier

General Description

The LM7121 is a high performance operational amplifier which addresses the increasing AC performance needs of video and imaging applications. Its tiny size and low power make it ideal for portable applications.

The LM7121 can operate over a wide dynamic range of supply voltages, from ±15V to ±5V. It offers an excellent speed-power product delivering 1000V/μs and 200 MHz unity gain stability. Another key feature of this operational amplifier is stability while driving unlimited capacitive loads.

Due to its Tiny S0T23-5 package, the LM7121 is ideal for designs where space and weight are the critical parameters. The benefits of the tiny package are evident in small portable electronic devices, such as cameras, and PC video cards. Tiny amplifiers are so small that they can be placed anywhere on a board close to the signal source or near the input to an A/D converter.

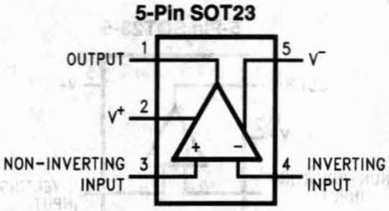
Features (Typical unless otherwise noted)

- Easy to use Voltage Feedback Topology
- Stable with unlimited capacitive loads
- Tiny SOT23-5 package—typical circuit layout takes half the space of SO-8 designs
- Unity Gain Frequency 200 MHz
- Slew Rate 1000V/μs
- Characterized for Supply Voltages ±5V and ±15V
- Low Supply Current 5 mA

Applications

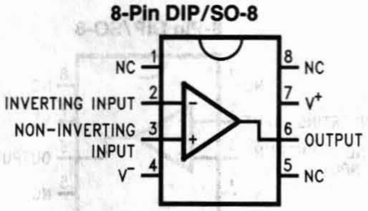
- Scanners, Color Fax, Digital copier
- Portable Video Equipment
- Cable Drivers
- Digital Cameras
- ADC/DAC Buffers

Connection Diagram



TL/H/12348-1

Top View



TL/H/12348-2

Top View

Ordering Information

Package	Temperature Range Industrial, −40°C to +85°C	NSC Drawing Number	Transport Media
8-Pin Molded DIP	LM7121AIN, LM7121BIN	N08E	Rails
8-Pin Small Outline	LM7121AIM, LM7121BIM	M08A	Rails
	LM7121AIMX, LM7121BIMX		Tape and Reel
5-Pin SOT 23-5	LM7121AIM5, LM7121BIM5	MA05A	Rails
	LM7121AIM5X, LM7121BIM5X		Tape and Reel

National Semiconductor

LM7131
Tiny High Speed Single Supply Operational Amplifier

General Description

The LM7131 is a high speed bipolar operational amplifier available in a tiny SOT23-5 package. This makes the LM7131 ideal for space and weight critical designs. Single supply voltages of 3V and 5V provides good video performance, wide bandwidth, low distortion, and high PSRR and CMRR. This makes the amplifier an excellent choice for desktop and portable video and computing applications. The amplifier is supplied in DIPs, surface mount 8-pin packages, and tiny SOT23-5 packages.

Tiny amplifiers are so small they can be placed anywhere on a board close to the signal source or next to an A-to-D input. Good high speed performance at low voltage makes the LM7131 a preferred part for battery powered designs.

Features

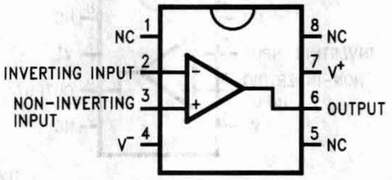
- Tiny SOT23-5 package saves space-typical circuit layouts take half the space of SO-8 designs.
- Guaranteed specs at 3V, 5V, and ±5V supplies
- Typical supply current 7.0 mA at 5V, 6.5 mA at 3V
- 4V output swing with +5V single supply
- Typical total harmonic distortion of 0.1% at 4 MHz
- 70 MHz Gain-Bandwidth Product
- 90 MHz −3 dB bandwidth at 3V and 5V, Gain = +1
- Designed to drive popular video A/D converters
- 40 mA output can drive 50Ω loads
- Differential gain and phase 0.25% and 0.75° at A_V = +2

Applications

- Driving video A/D converters
- Video output for portable computers and PDAs
- Desktop teleconferencing
- High fidelity digital audio
- Video cards

Connection Diagrams

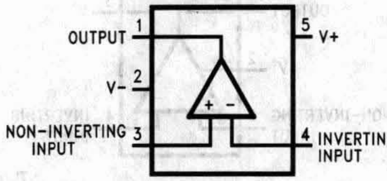
8-Pin DIP/SO-8



TL/H/12313-1

Top View

5-Pin SOT23-5



TL/H/12313-2

Top View

Package	Ordering Information	NSC Drawing Number	Package Marking	Supplied as
8-Pin DIP	LM7131ACN	N08E	LM7131ACN	rails
8-Pin DIP	LM7131BCN	N08E	LM7131BCN	rails
8-Pin SO-8	LM7131ACM	M08A	LM7131ACM	rails
8-Pin SO-8	LM7131BCM	M08A	LM7131BCM	rails
8-Pin SO-8	LM7131ACMX	M08A	LM7131ACM	2.5k units tape and reel
8-Pin SO-8	LM7131BCMX	M08A	LM7131BCM	2.5k units tape and reel
5-Pin SOT 23-5	LM7131ACM5	MA05A	A02A	250 units on tape and reel
5-Pin SOT 23-5	LM7131BCM5	MA05A	A02B	250 units on tape and reel
5-Pin SOT 23-5	LM7131ACM5X	MA05A	A02A	3k units tape and reel
5-Pin SOT 23-5	LM7131BCM5X	MA05A	A02B	3k units tape and reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Differential Input Voltage	±2.0
Voltage at Input/Output Pin	$(V^+) + 0.1V, (V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	12V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±80 mA
Current at Power Supply Pin	±80 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings

Supply Voltage ($V^+ - V^-$)	$2.7V \le V \le 12V$
Junction Temperature Range	
LM7131AC, LM7131BC	$0°C \le T_J \le +70°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
SO-8 Package, 8-Pin Surface Mount	165°C/W
M05A Package, 5-Pin Surface Mount	325°C/W

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.02	2 **4**	7 **10**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		10			μV/°C
I_B	Input Bias Current		20	30 **40**	30 **40**	μA max
I_{OS}	Input Offset Current		0.35	3.5 **5**	3.5 **5**	μA max
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 0.85V$ (Video Levels)	75	60 **55**	60 **55**	dB min
CMRR	Common Mode Rejection Ratio	$0.85V \le V_{CM} \le 1.7V$ (Mid-Range)	70	55 **50**	55 **50**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 3V, V^- = 0V$ $V^+ = 3V$ to $6.5V$	75	65 **60**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$V^- = -3V, V^+ = 0V$ $V^- = -3V$ to $-6.5V$	75	65 **60**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 3V$ For CMRR ≥ 50 dB	0.0	0.0 **0.00**	0.0 **0.00**	V min
			2.0	1.70 **1.60**	1.70 **1.60**	V max
A_{VOL}	Voltage Gain	$R_L = 150\Omega, V_O = 0.250V$ to $1.250V$	60	55 **50**	55 **50**	dB
C_{IN}	Common-Mode Input Capacitance		2			pF

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
V_O	Output Swing High	$V^+ = 3V$, $R_L = 150\Omega$ terminated at 0V	2.6	2.3 **2.0**	2.3 **2.0**	V min
	Low	$V^+ = 3V$, $R_L = 150\Omega$ terminated at 0V	0.05	0.15 **0.20**	0.15 **0.20**	V max
	High	$V^+ = 3V$, $R_L = 150\Omega$ terminated at 1.5V	2.6	2.3 **2.0**	2.3 **2.0**	V min
	Low	$V^+ = 3V$, $R_L = 150\Omega$ terminated at 1.5V	0.5	0.8 **1.0**	0.8 **1.0**	V max
V_O	Output Swing High	$V^+ = 3V$, $R_L = 600\Omega$ terminated at 0V	2.73			V max
V_O	Output Swing Low	$V^+ = 3V$, $R_L = 600\Omega$ terminated at 0V	0.06			V max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0V$	65	45 **40**	45 **40**	mA min
		Sinking, $V_O = 3V$	40	25 **20**	25 **20**	mA min
I_S	Supply Current	$V^+ = +3V$	6.5	8.0 **8.5**	8.0 **8.5**	mA max

3V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	$F = 4$ MHz, $A_V = +2$ $R_L = 150\Omega$, $V_O = 1.0V_{PP}$	0.1			%
	Differential Gain	(Note 10)	0.45			%
	Differential Phase	(Note 10)	0.6			°
SR	Slew Rate	$R_L = 150\Omega$, $C_L = 5$ pF (Note 7)	120			V/µS
SR	Slew Rate	$R_L = 150\Omega$, $C_L = 20$ pF (Note 7)	100			V/µS
GBW	Gain-Bandwidth Product		70			MHz
	Closed-Loop − 3 dB Bandwidth		90			MHz

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.02	2 **4**	7 **10**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		10			µV/°C
I_B	Input Bias Current		20	30 **40**	30 **40**	µA max
I_{OS}	Input Offset Current		0.35	3.5 **5**	3.5 **5**	µA max
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 1.85V$ (Video Levels)	75	65 **60**	65 **60**	dB min
CMRR	Common Mode Rejection Ratio	$1.85V \le V_{CM} \le 3.7V$ (Mid-Range)	70	55 **50**	55 **50**	dB min
+ PSRR	Positive Power Supply Rejection Ratio	$V^+ = 5V, V^- = 0V$ $V^+ = 5V$ to $10V$	75	65 **60**	65 **60**	dB min
− PSRR	Negative Power Supply Rejection Ratio	$V^- = -5V, V^+ = 0V$ $V^- = -5V$ to $-10V$	75	65 **60**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ For CMRR ≥ 50 dB	0.0	− 0.0 **0.00**	− 0.0 **0.00**	V min
			4.0	3.70 **3.60**	3.70 **3.60**	V max
A_{VOL}	Voltage Gain	$R_L = 150\Omega$, $V_O =$ 0.250V to 2.250V	70	60 **55**	60 **55**	dB min
C_{IN}	Common-Mode Input Capacitance		2			pF
V_O	Output Swing High	$V^+ = 5V$, $R_L = 150\Omega$ terminated at 0V	4.5	4.3 **4.0**	4.3 **4.0**	V min
	Low	$V^+ = 5V$, $R_L = 150\Omega$ terminated at 0V	0.08	0.15 **0.20**	0.15 **0.20**	V max
	High	$V^+ = 5V$, $R_L = 150\Omega$ terminated at 2.5V	4.5	4.3 **4.0**	4.3 **4.0**	V min
	Low	$V^+ = 5V$, $R_L = 150\Omega$ terminated at 2.5V	0.5	0.8 **1.0**	0.8 **1.0**	V max
V_O	Output Swing High	$V^+ = 5V$, $R_L = 600\Omega$ terminated at 0V	4.70			V max
V_O	Ouptut Swing Low	$V^+ = 5V$, $R_L = 600\Omega$ terminated at 0V	0.07			V max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0V$	65	45 **40**	45 **40**	mA min
		Sinking, $V_O = 5V$	40	25 **20**	25 **20**	mA min
I_S	Supply Current	$V^+ = +5V$	7.0	8.5 **9.0**	8.5 **9.0**	mA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	$F = 4$ MHz, $A_V = +2$ $R_L = 150\Omega$, $V_O = 2.0V_{PP}$	0.1			%
	Differential Gain	(Note 10)	0.25			%
	Differential Phase	(Note 10)	0.75			°
SR	Slew Rate	$R_L = 150\Omega$, $C_L = 5$ pF (Note 8)	150			V/µs
SR	Slew Rate	$R_L = 150\Omega$, $C_L = 20$ pF (Note 8)	130			V/µs
GBW	Gain-Bandwidth Product		70			MHz
	Closed-Loop −3 dB Bandwidth		90			MHz
e_n	Input-Referred Voltage Noise	f = 1 kHz	11			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	3.3			$\frac{pA}{\sqrt{Hz}}$

±5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 5V$, $V_{CM} = V_O = 0V$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.02	2 **4**	7 **10**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		10			µV/°C
I_B	Input Bias Current		20	30 **40**	30 **40**	µA max
I_{OS}	Input Offset Current		0.35	3.5 **5**	3.5 **5**	µA max
CMRR	Common Mode Rejection Ratio	$-5V \le V_{CM} \le 3.7V$	75	65 **60**	65 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 5V$, $V^- = 0V$ $V^+ = 5V$ to $10V$	75	65 **60**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$V^- = -5V$, $V^+ = 0V$ $V^- = -5V$ to $-10V$	75	65 **60**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$, $V^- = -5V$ For CMRR ≥ 60 dB	−5.0	−5.0 **−5.0**	−5.0 **−5.0**	V min
			4.0	3.70 **3.60**	3.70 **3.60**	V max
A_{VOL}	Voltage Gain	$R_L = 150\Omega$, $V_O = -2.0$ to $+2.0$	70	55 **50**	55 **50**	dB

±5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 5V$, $V_{CM} = V_O = 0V$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
C_{IN}	Common-Mode Input Capacitance		2			pF
V_O	Output Swing High	$V^+ = 5V$, $V^- = -5V$ $R_L = 150\Omega$ terminated at 0V	4.5	4.3 **4.0**	4.3 **4.0**	V min
	Low		−4.5	−3.5 **−2.5**	−3.5 **−2.5**	V max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = -5V$	65	45 **40**	45 **40**	mA min
		Sinking, $V_O = 5V$	40	25 **20**	25 **20**	mA min
I_S	Supply Current	$V^+ = +5V$, $V^- = -5V$	7.5	9 **10**	9 **10**	mA max

±5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 5V$, $V_{CM} = V_O = 0V$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	F = 4 MHz, $A_V = -2$ $R_L = 150\Omega$, $V_O = 4.0V_{PP}$	1.5			%
	Differential Gain	(Note 10)	0.25			%
	Differential Phase	(Note 10)	1.0			°
SR	Slew Rate	$R_L = 150\Omega$, $C_L = 5\ pF$ (Note 9)	150			V/μs
SR	Slew Rate	$R_L = 150\Omega$, $C_L = 20\ pF$ (Note 9)	130			V/μs
GBW	Gain-Bandwidth Product		70			MHz
	Closed-Loop −3 dB Bandwidth		90			MHz

Note 1: Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Connected as voltage follower with 1.5V step input. Number specified is the slower of the positive and negative slew rates. $V^+ = 3V$ and $R_L = 150\Omega$ connected to 1.5V. Amp excited with 1 kHz to produce $V_O = 1.5\ V_{PP}$.

Note 8: Connected as Voltage Follower with 4.0V step input. Number specified is the slower of the positive and negative slew rates. $V^+ = 5V$ and $R_L = 150\Omega$ connected to 2.5V. Amp excited with 1 kHz to produce $V_O = 4\ V_{PP}$.

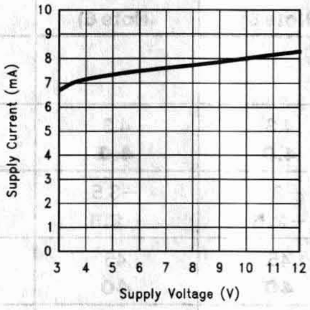
Note 9: Connected as Voltage Follower with 4.0V step input. Number specified is the slower of the positive and negative slew rates. $V^+ = 5V$, $V^- = -5V$ and $R_L = 150\Omega$ connected to 0V. Amp excited with 1 kHz to produce $V_O = 4\ V_{PP}$.

Note 10: Differential gain and phase measured with a 4.5 MHz signal into a 150Ω load, Gain = +2.0, between 0.6V and 2.0V output.

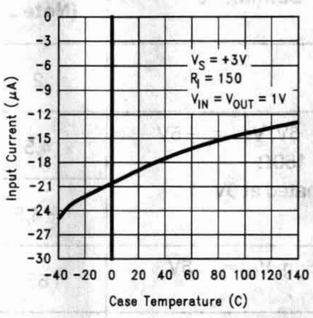
1

Typical Performance Characteristics

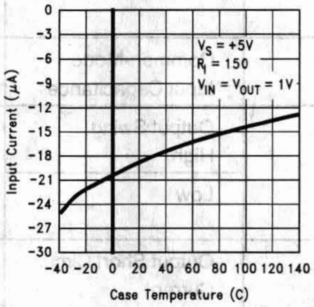
LM7131 Supply Current vs Supply Voltage



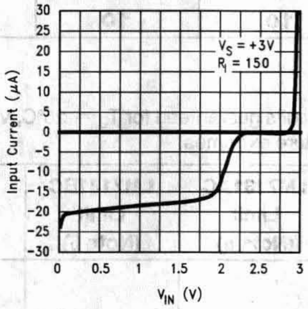
LM7131 Input Current vs Temperature @ 3V



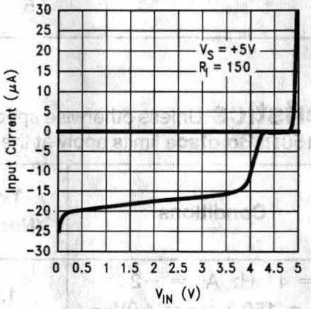
LM7131 Input Current vs Temperature @ 5V



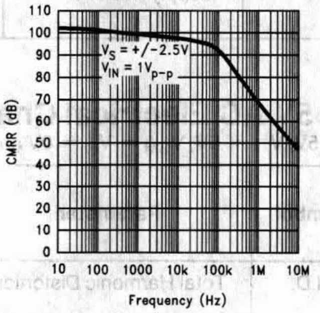
LM7131 Input Current vs Input Voltage @ 3V



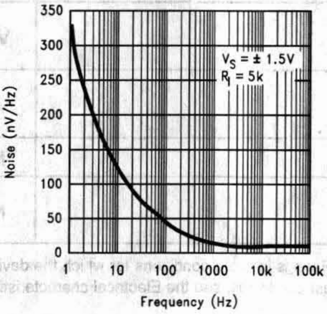
LM7131 Input Current vs Input Voltage @ 5V



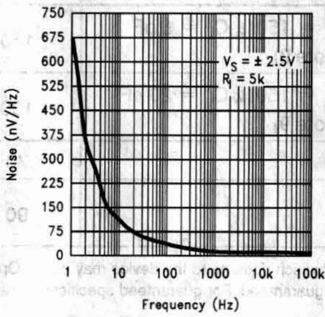
LM7131 CMRR vs Frequency @ 5V



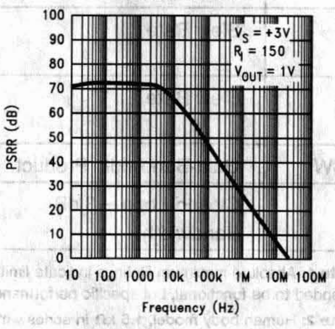
LM7131 Voltage Noise vs Frequency @ 3V



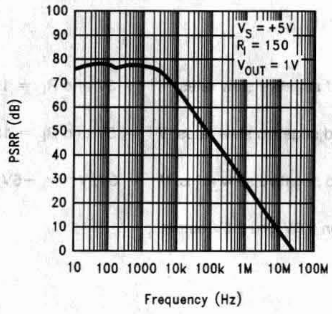
LM7131 Voltage Noise vs Frequency @ 5V



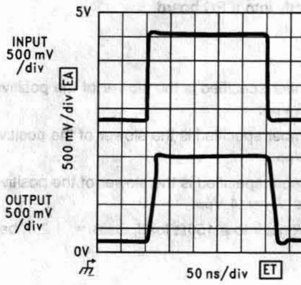
LM7131 PSRR vs Frequency @ 3V



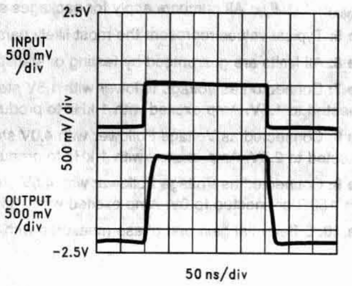
LM7131 PSRR vs Frequency @ 5V



LM7131 Cable Driver A_V = +1 @ +3V



LM7131 Cable Driver A_V = +2 @ +3V



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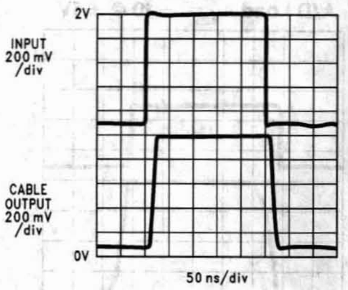
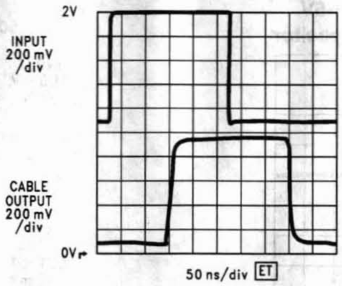
Typical Performance Characteristics (Continued)

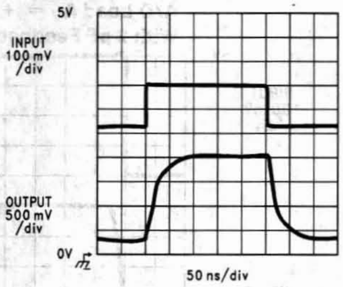
LM7131 Driving 5′ RG-59 $A_V = +2$ @ $+3V$



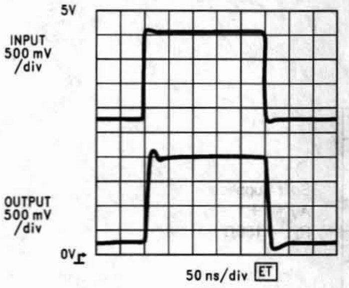
LM7131 Driving 75′ RG-59 $A_V = +2$ @ $+3V$



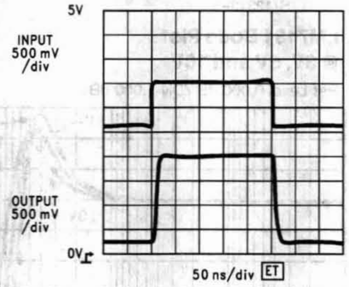
LM7131 Cable Driver $A_V = +10$ @ $+3V$



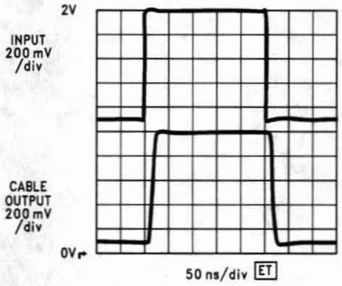
LM7131 Cable Driver $A_V = +1$ @ $+5V$



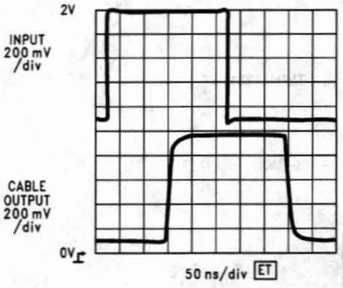
LM7131 Cable Driver $A_V = +2$ @ $+5V$



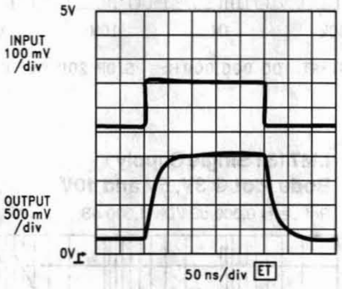
LM7131 Driving 5′ RG-59 $A_V = +2$ @ $+5V$



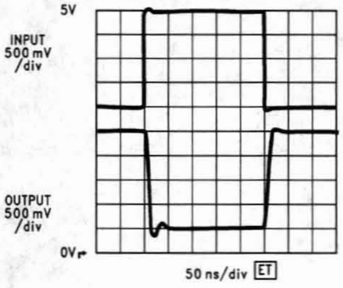
LM7131 Driving 75′ RG-59 $A_V = +2$ @ $+5V$



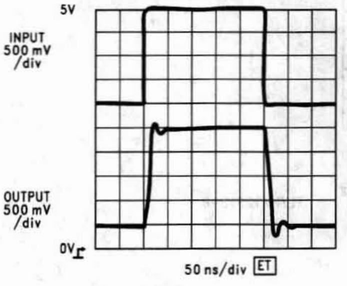
LM7131 Cable Driver $A_V = +10$ @ $+5V$



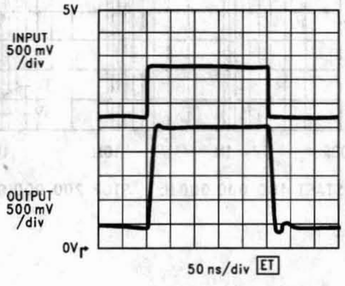
LM7131 Driving Flash A/D Load $A_V = -1$ @ $+5V$



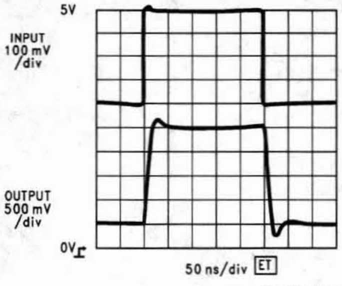
LM7131 Driving Flash A/D Load $A_V = +1$ @ $+5V$



LM7131 Driving Flash A/D Load $A_V = +2$ @ $+5V$



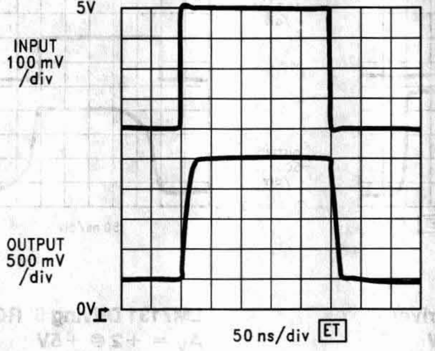
LM7131 Driving Flash A/D Load $A_V = +5$ @ $+5V$



TL/H/12313–4

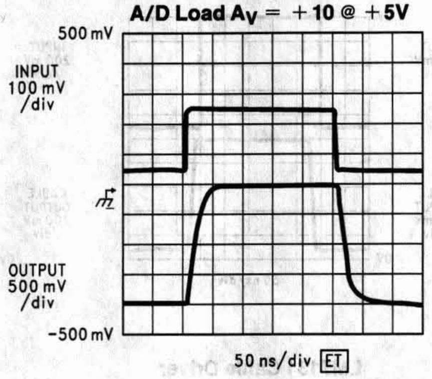
Typical Performance Characteristics (Continued)

LM7131 Driving Flash A/D Load $A_V = +5$ @ $+5V$ With 2 pF Feedback Capacitor



TL/H/12313–5

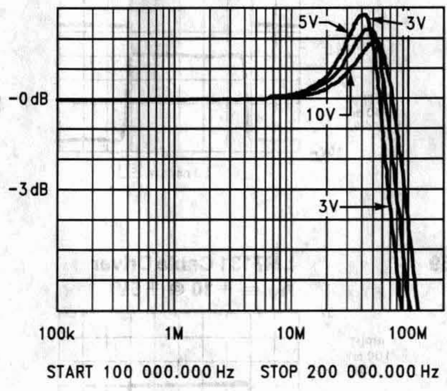
LM7131 Driving Flash A/D Load $A_V = +10$ @ $+5V$



TL/H/12313–6

LM7131 Bode Plot @ 3V, 5V and 10V

Ref Level 0.000 dB /Div 1.000 dB

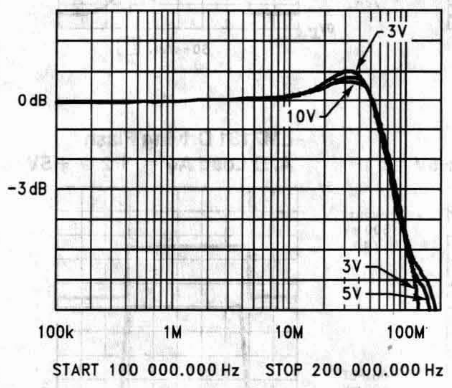


Split Supplies
$A_V = +1$
$R_L = 150\Omega$

TL/H/12313–7

LM7131 Single Supply Bode Plot @ 3V, 5V and 10V

Ref Level 0.000 dB /Div 1.000 dB



Single Supplies
$A_V = +1$
$R_L = 150\Omega$

TL/H/12313–8

Application Information

GENERAL INFORMATION

The LM7131 is a high speed complementary bipolar amplifier which provides high performance at single supply voltages. The LM7131 will operate at ±5V split supplies, +5V single supplies, and +3V single supplies. It can provide improved performance for ±5V designs with an easy transition to +5V single supply. The LM7131 is a voltage feedback amplifier which can be used in most operational amplifier circuits.

The LM7131 is available in three package types: DIPs for through hole designs, SO-8 surface mount packages and the SOT23-5 Tiny package for space and weight savings.

The LM7131 has been designed to meet some of the most demanding requirements for single supply amplifiers—driving analog to digital converters and video cable driving. The output stage of the LM7131 has been specially designed for the dynamic load presented by analog to digital converters. The LM7131 is capable of a 4V output range with a +5V single supply. The LM7131's drive capability and good differential gain and phase make quality video possible from a small package with only a +5V supply.

BENEFITS OF THE LM7131

The LM7131 can make it possible to amplify high speed signals with a single +5V or +3V supply, saving the cost of split power supplies.

EASY DESIGN PATH FROM ±5V to +5V SYSTEMS

The DIP and SO-8 packages and similar ±5V and single supply specifications means the LM7131 may be able to replace many more expensive or slower op amps, and then be used for an easy transition to 5V single supply systems. This could provide a migration path to lower voltages for the amplifiers in system designs, reducing the effort and expense of testing and re-qualifying different op amps for each new design.

In addition to providing a design migration path, the three packages types have other advantages.

The DIPs can be used for easy prototyping and through hole boards. The SO-8 for surface mount board designs, and using the SOT23-5 for a smaller surface mount package can save valuable board space.

SPECIFIC ADVANTAGES OF SOT23-5 (TINY PACKAGE)

The SOT23-5 (Tiny) package can save board space and allow tighter layouts. The low profile can help height limited designs, such as sub-notebook computers, consumer video equipment, personal digital assistants, and some of the thicker PCMCIA cards. The small size can improve signal integrity in noisy environments by placing the amplifier closer to the signal source. The tiny amp can fit into tight spaces and weighs little. This makes it possible to design the LM7131 into places where amplifiers could not previously fit.

The LM7131 can be used to drive coils and transformers referenced to virtual ground, such as magnetic tape heads and disk drive write heads. The small size of the SOT23-5 package can allow it to be placed with a pre-amp inside of some rotating helical scan video head (VCR) assemblies. This avoids long cable runs for low level video signals, and can result in higher signal fidelity.

Additional space savings parts are available in tiny packages from National Semiconductor, including low power amplifiers, precision voltage references, and voltage regulators.

Notes on Performance Curves and Datasheet Limits

Important:

Performance curves represent an average of parts, and are not limits.

SUPPLY CURRENT vs SUPPLY VOLTAGE

Note that this curve is nearly straight, and rises slowly as the supply voltage increases.

INPUT CURRENT vs INPUT VOLTAGE

This curve is relatively flat in the 200 mV to 4V input range, where the LM7131 also has good common mode rejection.

COMMON MODE VOLTAGE REJECTION

Note that there are two parts to the CMRR specification of the datasheet for 3V and 5V. The common mode rejection ratio of the LM7131 has been maximized for signals near ground (typical of the active part of video signals, such as those which meet the RS-170 levels). This can help provide rejection of unwanted noise pick-up by cables when a balanced input is used with good input resistor matching. The mid-level CMRR is similar to that of other single supply op amps.

BODE PLOTS (GAIN vs FREQUENCY FOR $A_V = +1$)

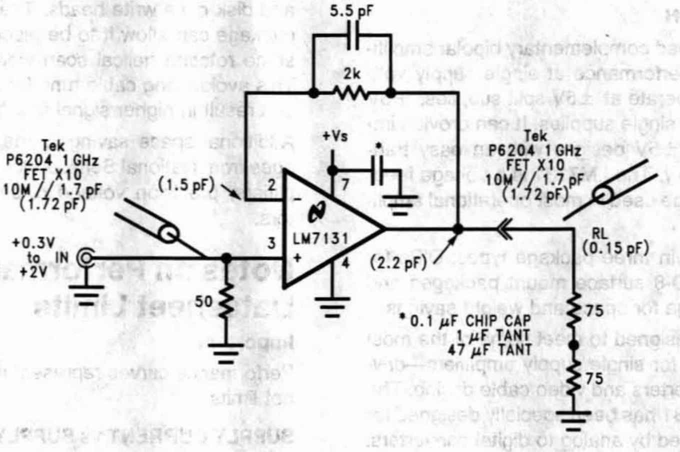
The gain vs. frequency plots for a non-inverting gain of 1 show the three voltages with the 150Ω load connected in two ways. For the single supply graphs, the load is connected to the most negative rail, which is ground. For the split supply graphs, the load is connected to a voltage halfway between the two supply rails.

DRIVING CABLES

Pulse response curves for driving 75Ω back terminate cables are shown for both 3V and 5V supplies. Note the good pulse fidelity with straight 150 loads, five foot (1.5 meter) and 75 foot (22 meter) cable runs. The bandwidth is reduced when used in a gain of ten ($A_V = +10$). Even in a gain of ten configuration, the output settles to < 1% in about 100 ns, making this useful for amplifying small signals at a sensor or signal source and driving a cable to the main electronics section which may be located away from the signal source. This will reduce noise pickup.

Please refer to *Figures 1–5* for schematics of test setups for cable driving.

Application Information (Continued)


5.5 pF
2k
+Vs
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
(1.5 pF)
2
7
*
6
LM7131
3
4
+0.3V
to
+2V
IN
(2.2 pF)
50
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
RL
(0.15 pF)
* 0.1 μF CHIP CAP
1 μF TANT
47 μF TANT
75
75

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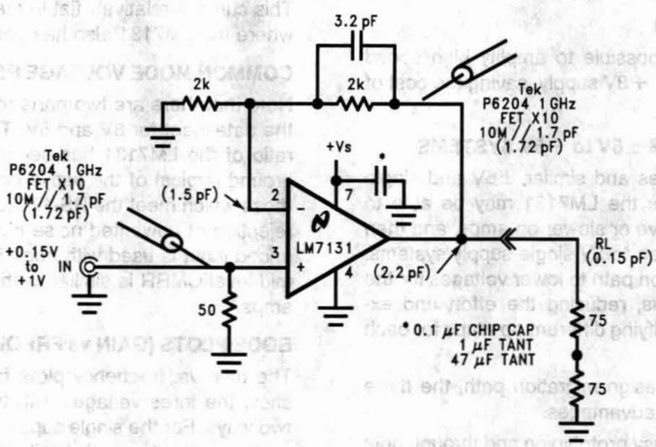
Numbers in parentheses are measured fixture capacitances w/o DUT and load.

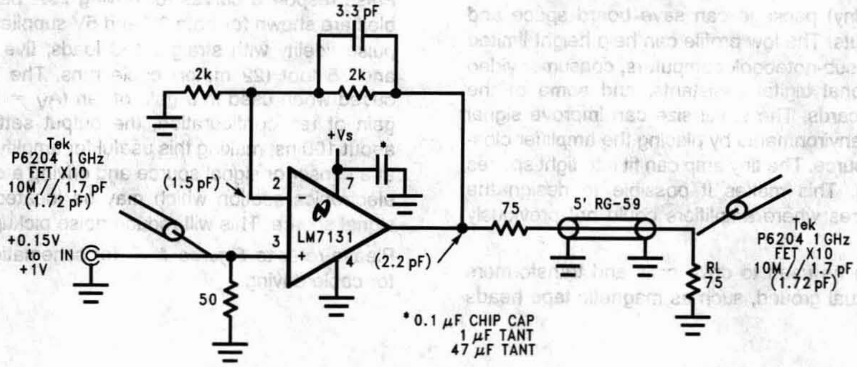
FIGURE 1. Cable Driver $A_V = +1$


3.2 pF
2k
2k
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
+Vs
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
(1.5 pF)
2
7
*
6
LM7131
3
4
+0.15V
to
+1V
IN
(2.2 pF)
50
RL
(0.15 pF)
* 0.1 μF CHIP CAP
1 μF TANT
47 μF TANT
75
75

TL/H/12313–10

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 2. Cable Driver $A_V = +2$

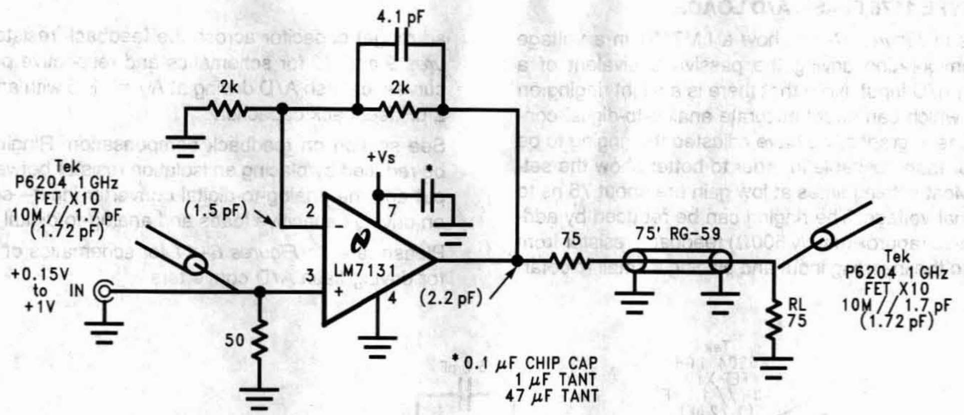

3.3 pF
2k
2k
+Vs
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
(1.5 pF)
2
7
*
6
LM7131
3
4
+0.15V
to
+1V
IN
(2.2 pF)
50
75
5′ RG-59
RL
75
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
* 0.1 μF CHIP CAP
1 μF TANT
47 μF TANT

TL/H/12313–11

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 3. Cable Driver 5′ RG-59

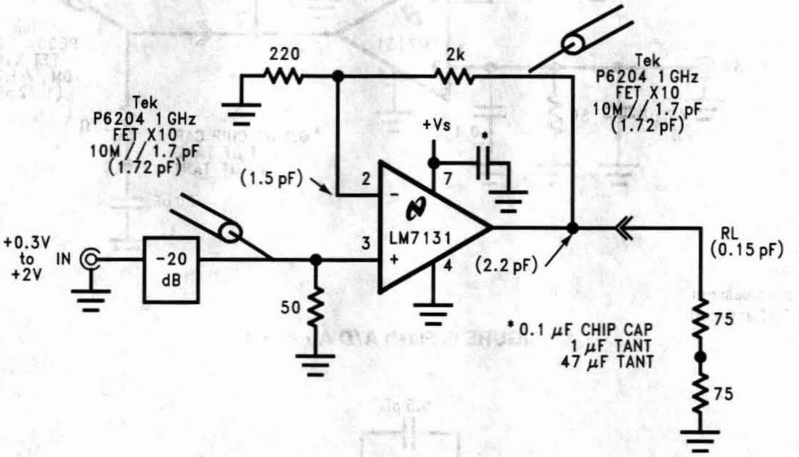
Application Information (Continued)


4.1 pF
2k
2k
+Vs
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
(1.5 pF)
2
7
-
LM7131
+
3
4
+0.15V
to
+1V
IN
50
(2.2 pF)
75
75' RG-59
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
RL
75
*0.1 μF CHIP CAP
1 μF TANT
47 μF TANT

TL/H/12313-12

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 4. Cable Driver 75′ RG-59


220
2k
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
+Vs
(1.5 pF)
2
7
-
LM7131
+
3
4
+0.3V
to
+2V
IN
-20
dB
50
(2.2 pF)
RL
(0.15 pF)
75
75
*0.1 μF CHIP CAP
1 μF TANT
47 μF TANT

TL/H/12313-13

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 5. Cable Driver Gain of 10 $A_V = +10$

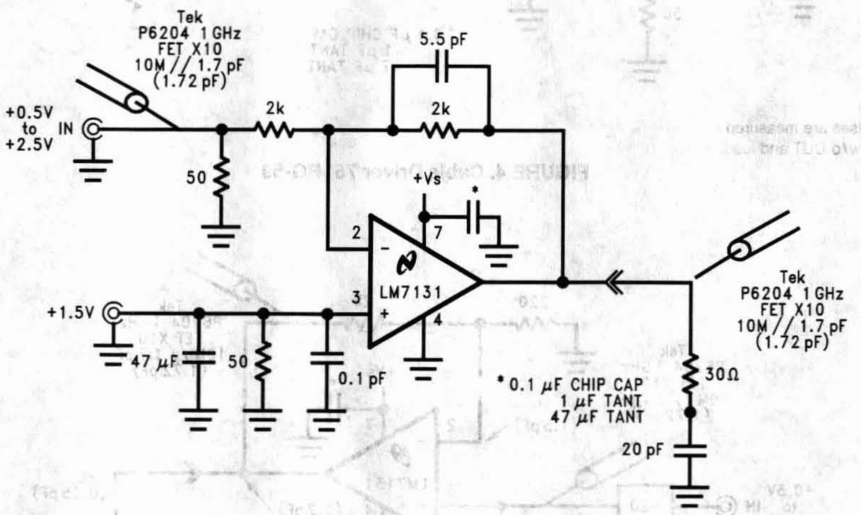
Application Information (Continued)

DRIVING TYPE 1175 FLASH A/D LOADS

The circuits in *Figures 6–11* show a LM7131 in a voltage follower configuration driving the passive equivalent of a typical flash A/D input. Note that there is a slight ringing on the output, which can affect accurate analog-to-digital conversion. In these graphs, we have adjusted the ringing to be a little larger than desirable in order to better show the settling time. Most settling times at low gain are about 75 ns to < 1% of final voltage. The ringing can be reduced by adding a low value (approximately 500Ω) feedback resistor from the output to the inverting input and placing a small (picofarad range) capacitor across the feedback resistor. See *Figures 9* and *10* for schematics and respective performance curves for flash A/D driving at $A_V = +5$ with and without a 2 pF feedback capacitor.

See section on feedback compensation. Ringing can also be reduced by placing an isolation resistor between the output and the analog-to-digital converter input—see sections on driving capacitive loads and analog-to-digital converters.

Please refer to *Figures 6–11* for schematics of test setups for driving flash A/D converters.

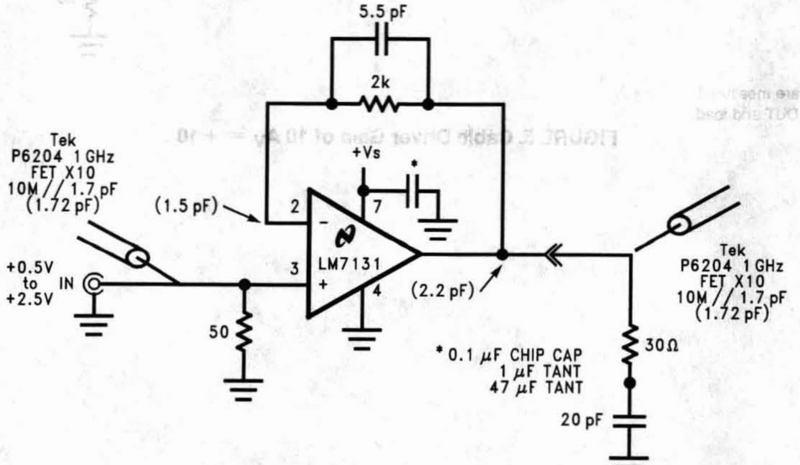


Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
5.5 pF
+0.5V
to
+2.5V
IN
2k
2k
50
+Vs
*
7
2
LM7131
3
4
+1.5V
47 μF
50
0.1 pF
*0.1 μF CHIP CAP
1 μF TANT
47 μF TANT
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
30Ω
20 pF

TL/H/12313–14

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 6. Flash A/D $A_V = -1$



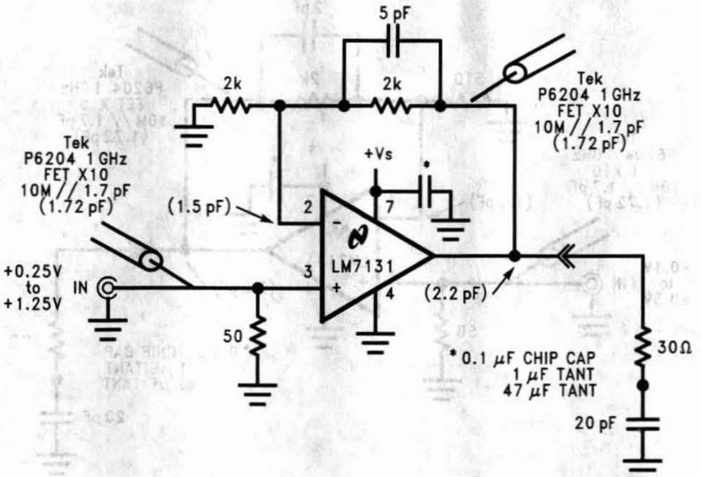
5.5 pF
2k
+Vs
*
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
(1.5 pF)
2
7
3
LM7131
4
+0.5V
to
+2.5V
IN
(2.2 pF)
50
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
*0.1 μF CHIP CAP
1 μF TANT
47 μF TANT
30Ω
20 pF

TL/H/12313–15

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 7. Flash A/D $A_V = +1$

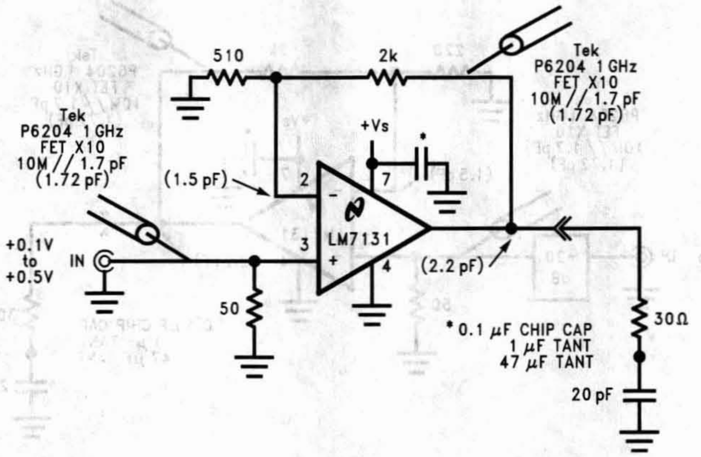
Application Information (Continued)


5 pF
2k
2k
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
+Vs
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
(1.5 pF)
2
7
3
LM7131
4
+0.25V
to
+1.25V
IN
(2.2 pF)
50
* 0.1 μF CHIP CAP
1 μF TANT
47 μF TANT
30Ω
20 pF

TL/H/12313-16

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 8. Flash A/D $A_V = +2$

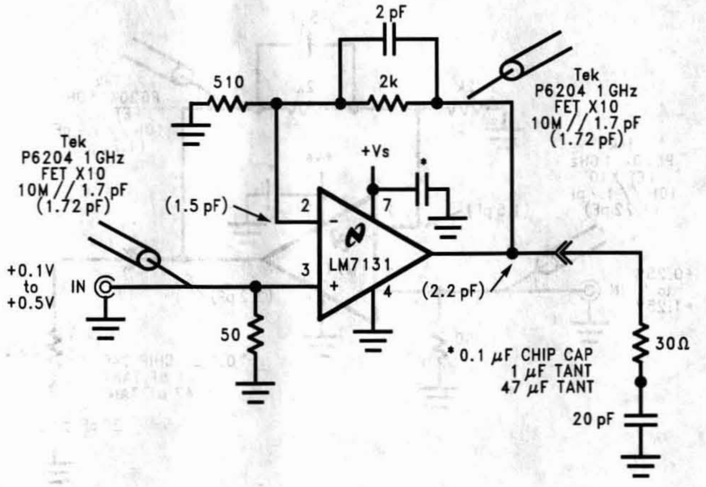

510
2k
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
+Vs
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
(1.5 pF)
2
7
3
LM7131
4
+0.1V
to
+0.5V
IN
(2.2 pF)
50
* 0.1 μF CHIP CAP
1 μF TANT
47 μF TANT
30Ω
20 pF

TL/H/12313-17

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 9. Flash A/D $A_V = +5$

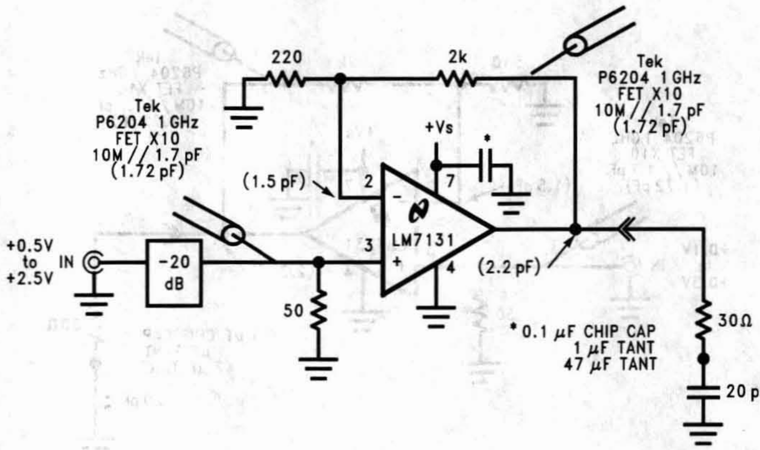
Application Information (Continued)


2 pF
510
2k
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
+Vs
*
(1.5 pF)
2
7
3
4
LM7131
+0.1V
to
+0.5V
IN
50
(2.2 pF)
30Ω
* 0.1 µF CHIP CAP
1 µF TANT
47 µF TANT
20 pF

TL/H/12313–18

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 10. Flash A/D $A_V = +5$ with Feedback Capacitor


220
2k
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
Tek
P6204 1 GHz
FET X10
10M // 1.7 pF
(1.72 pF)
+Vs
*
(1.5 pF)
2
7
3
4
LM7131
+0.5V
to
+2.5V
IN
−20
dB
50
(2.2 pF)
30Ω
* 0.1 µF CHIP CAP
1 µF TANT
47 µF TANT
20 pF

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Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 11. Flash A/D $A_V = +10$

Using the LM7131

LIMITS AND PRECAUTIONS

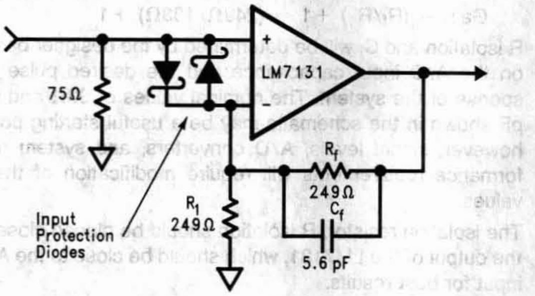
Supply Voltage

The absolute maximum supply voltage which may be applied to the LM7131 is 12V. Designers should not design for more than 10V nominal, and carefully check supply tolerances under all conditions so that the voltages do not exceed the maximum.

Differential Input Voltage

Differential input voltage is the difference in voltage between the non-inverting (+) input and the inverting input (−) of the op amp. The absolute maximum differential input voltage is ±2V across the inputs. This limit also applies when there is no power supplied to the op amp. This may not be a problem in most conventional op amp designs, however, designers should avoid using the LM7131 as comparator or forcing the inputs to different voltages. In some designs, diode protection may be needed between the inputs. See *Figure 12*.

Gain of +2



TL/H/12313-20

FIGURE 12

Output Short Circuits

The LM7131 has output short circuit protection, however, it is not designed to withstand continuous short circuits, very fast high energy transient voltage or current spikes, or shorts to any voltage beyond the power supply rails. Designs should reduce the number and energy level of any possible output shorts, especially when used with ±5V supplies.

A resistor in series with the output, such as the 75Ω resistor used to back terminate 75Ω cables, will reduce the effects of shorts. For outputs which will send signals off the PC board additional protection devices, such as diodes to the power rails, zener-type surge suppressors, and varistors may be useful.

Thermal Management

Note that the SOT23-5 (Tiny) package has less power dissipation capability (325°/W) than the S0-8 and DIP packages (115°/W). This may cause overheating with ±5 supplies and heavy loads at high ambient temps. This is less of a problem when using +5V single supplies.

Example:

Driving a 150Ω load to 2.0V at a 40°C (104 °F) ambient temperature. (This is common external maximum temperature for office environments. Temperatures inside equipment may be higher.)

No load power-
No load LM7131 supply current - 9.0 mA
Supply voltage is 5.0V
No load LM7131 power - 9.0 mA x 5.0V = 45 mW
Power with load-
Current out is 2.0V/150 Ω = 13.33 mA
Voltage drop in LM7131 is 5.0V (supply) − 2.0V (output) = 3.0V
Power dissipation 13.33 mA x 3.0V = 40 mW
Total Power = 45 mW + 40 mW = 85 mW = 0.085
Temperature Rise = 0.085 W x 325°/W = 27.625 degrees
Junction temperature at 40° ambient = 40 + 27.625 = 67.6225°.
This device is within the 0° to 70° specification limits.

The 325°/W value is based on still air and the pc board land pattern shown in this datasheet. Actual power dissipation is sensitive to PC board connections and airflow.

SOT23-5 power dissipation may be increased by airflow or by increasing the metal connected to the pads, especially the center pin (pin number 2, V−) on the left side of the SOT23-5. This pin forms the mounting paddle for the die inside the SOT23-5, and can be used to conduct heat away from the die. The land pad for pin 2 can be made larger and/or connected to power planes in a multilayer board. Additionally, it should be noted that difficulty in meeting performance specifications for the LM7131 is most common at cold temperatures. While excessively high junction temperatures will degrade LM7131 performance, testing has confirmed that most specifications are met at a junction temperature of 85°C.

See "Understanding Integrated Circuit Package Power Capabilities", Application Note AN-336, which may be found in the appendix of the Operational Amplifier Databook.

Layout and Power Supply Bypassing

Since the LM7131 is a high speed (over 50 MHz) device, good high speed circuit layout practices should be followed. This should include the use of ground planes, adequate power supply bypassing, removing metal from around the input pins to reduce capacitance, and careful routing of the output signal lines to keep them away from the input pins.

The power supply pins should be bypassed on both the negative and positive supply inputs with capacitors placed close to the pins. Surface mount capacitors should be used for best performance, and should be placed as close to the pins as possible. It is generally advisable to use two capacitors at each supply voltage pin. A small surface mount capacitor with a value of around 0.01 microfarad (10 nF), usually a ceramic type with good RF performance, should be placed closest to the pin. A larger capacitor, in usually in the range of 1.0 μF to 4.7 μF, should also be placed near the pin. The larger capacitor should be a device with good RF characteristics and low ESR (equivalent series resistance) for best results. Ceramic and tantalum capacitors generally work well as the larger capacitor.

For single supply operation, if continuous low impedance ground planes are available, it may be possible to use bypass capacitors between the +5V supply and ground only, and reduce or eliminate the bypass capacitors on the V− pin.

Using the LM7131 (Continued)

Capacitive Load Driving

The phase margin of the LM7131 is reduced by driving large capacitive loads. This can result in ringing and slower settling of pulse signals. This ringing can be reduced by placing a small value resistor (typically in the range of 22Ω–100Ω) between the LM7131 output and the load. This resistor should be placed as close as practical to the LM7131 output. When driving cables, a resistor with the same value as the characteristic impedance of the cable may be used to isolate the cable capacitance from the output. This resistor will reduce reflections on the cable.

Input Current

The LM7131 has typical input bias currents in the 15 μA to 25 μA range. This will not present a problem with the low input impedances frequently used in high frequency and video circuits. For a typical 75Ω input termination, 20 μA of input current will produce a voltage across the termination resistor of only 1.5 mV. An input impedance of 10 kΩ, however, would produce a voltage of 200 mV, which may be large compared to the signal of interest. Using lower input impedances is recommended to reduce this error source.

Feedback Resistor Values and Feedback Compensation

Using large values of feedback resistances (roughly 2k) with low gains (such gains of 2) will result in degraded pulse response and ringing. The large resistance will form a pole with the input capacitance of the inverting input, delaying feedback to the amplifier. This will produce overshoot and ringing. To avoid this, the gain setting resistors should be scaled to lower values (below 1k) At higher gains (> 5) larger values of feedback resistors can be used.

Overshoot and ringing of the LM7131 can be reduced by adding a small compensation capacitor across the feed back resistor. For the LM7131 values in pF to tens of pF range are useful initial values. Too large a value will reduce the circuit bandwidth and degrade pulse response.

Since the small stray capacitance from the circuit layout, other components, and specific circuit bandwidth requirements will vary, it is often useful to select final values based on prototypes which are similar in layout to the production circuit boards.

Reflections

The output slew rate of the LM7131 is fast enough to produce reflected signals in many cables and long circuit traces. For best pulse performance, it may be necessary to terminate cables and long circuit traces with their characteristic impedance to reduce reflected signals.

Reflections should not be confused with overshoot. Reflections will depend on cable length, while overshoot will depend on load and feedback resistance and capacitance. When determining the type of problem, often removing or drastically shortening the cable will reduce or eliminate reflections. Overshoot can exist without a cable attached to the op amp output.

Driving Flash A/D Converters (Video Converters)

The LM7131 has been optimized to drive flash analog to digital converters in a +5V only system. Different flash A/D converters have different voltage input ranges. The LM7131 has enough gain-bandwidth product to amplify standard video level signals to voltages which match the optimum input range of many types of A/D converters.

For example, the popular 1175 type 8-bit flash A/D converter has a preferred input range from 0.6V to 2.6V. If the input signal has an active video range (excluding sync levels) of approximately 700 mV, a circuit like the one in *Figure 13* can be used to amplify and drive an A/D. The 10 μF capacitor blocks the DC components, and allows the + input of the LM7131 to be biased through R clamp so that the minimum output is equal to V_{RB} of the A/D converter. The gain of the circuit is determined as follows:

Output Signal Range = 2.6V (V top) = 0.6V (V bottom) = 2.0V

Gain = Output Signal Range/Input Signal = 2.857 = 2.00/0.700

Gain = $(R_f/R_1) + 1 = (249\Omega/133\Omega) + 1$

R isolation and C_f will be determined by the designer based on the A/D input capacitance and the desired pulse response of the system. The nominal values of 33Ω and 5.6 pF shown in the schematic may be a useful starting point, however, signal levels, A/D converters, and system performance requirements will require modification of these values.

The isolation resistor, R isolation should be placed close to the output of the LM7131, which should be close to the A/D input for best results.

R clamp is connected to a voltage level which will result in the bottom of the video signal matching the Vrb level of the A/D converter. This level will need to be set by clamping the black level of the video signal. The clamp voltage will depend on the level and polarity of the video signal. Detecting the sync signal can be done by a circuit such as the LM1881 Video Sync Separator.

Important Note: This is an illustration of a conceptual use of the LM7131, not a complete design. The circuit designer will need to modify this for input protection, sync, and possibly some type of gain control for varying signal levels.

Some A/D converters have wide input ranges where the lower reference level can be adjusted. With these converters, best distortion results are obtained if the lower end of the output range is about 250 mV or more above the V− input of the LM7131 more. The upper limit can be as high as 4.0V with good results.

Driving the ADC12062 +5V 12-BIT A/D Converter

Figure 14 shows the LM7131 driving a National ADC12062 12 bit analog to digital converter. Both devices can be powered from a single +5V supply, lowering system complexity and cost. With the lowest signal voltage limited to 300 mV and a 3.8V peak-to-peak 100 KHz signal, bench tests have shown distortion less than −75 db, signal to noise ratios greater than 66 db, and SINAD (signal to noise + distortion) values greater than 65 db. For information on the latest single supply analog-to-digital converters, please contact your National Semiconductor representative.

Using the LM7131 (Continued)

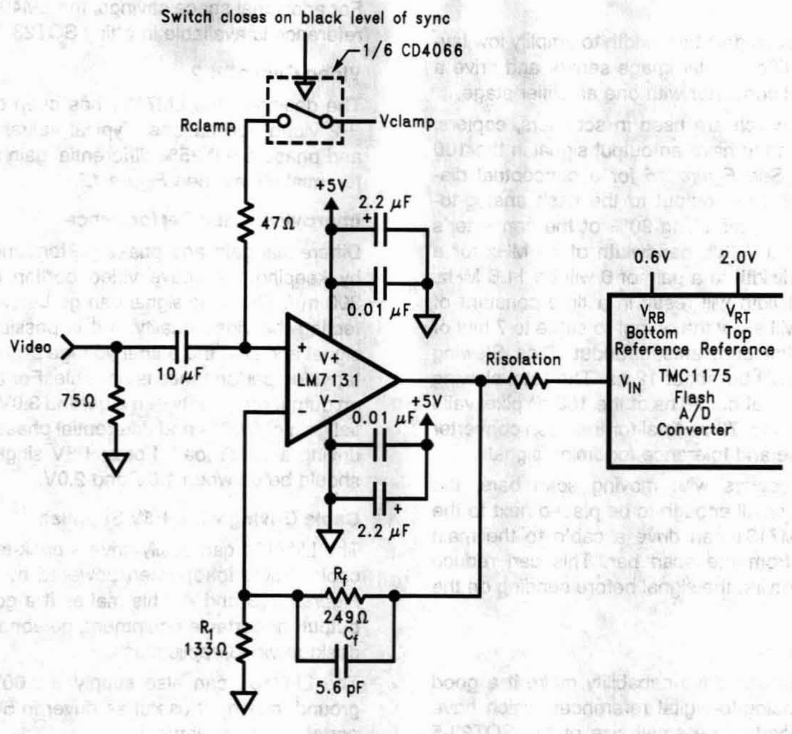

Switch closes on black level of sync
1/6 CD4066
Rclamp
Vclamp
+5V
47Ω
2.2 µF
0.01 µF
Video
10 µF
75Ω
+
V+
LM7131
V−
−
0.01 µF
+5V
2.2 µF
Risolation
0.6V
2.0V
V_{RB}
Bottom
Reference
V_{RT}
Top
Reference
V_{IN}
TMC1175
Flash
A/D
Converter
R_f
249Ω
C_f
5.6 pF
R_I
133Ω

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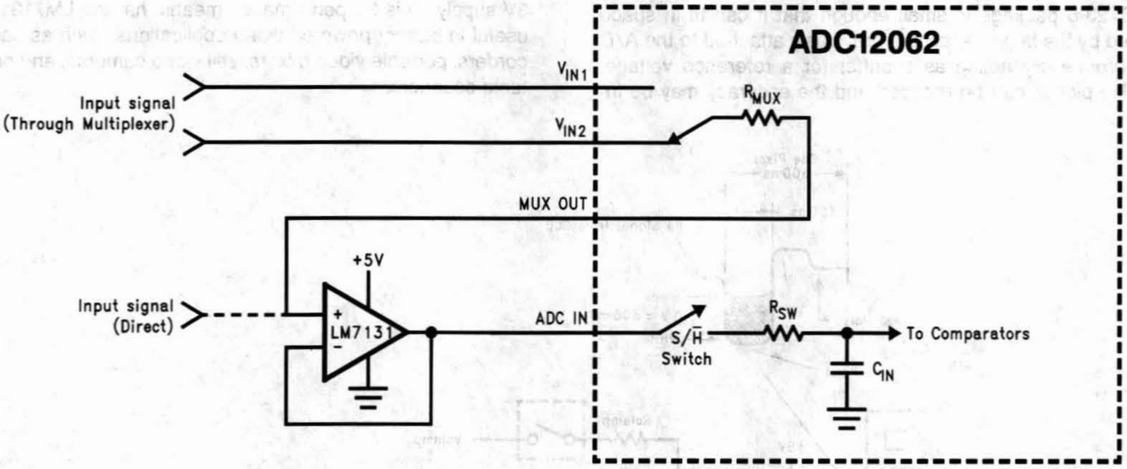
FIGURE 13


ADC12062
V_{IN1}
Input signal
(Through Multiplexer)
V_{IN2}
R_{MUX}
MUX OUT
+5V
Input signal
(Direct)
+
LM7131
−
ADC IN
S/$\overline{H}$
Switch
R_{SW}
To Comparators
C_{IN}

TL/H/12313-22

FIGURE 14. Buffering the Input with an LM7131 High Speed Op Amp

Using the LM7131 (Continued)

CCD Amplifiers

The LM7131 has enough gain bandwidth to amplify low level signals from a CCD or similar image sensor and drive a flash analog-to-digital converter with one amplifier stage.

Signals from CCDs, which are used in scanners, copiers, and digital cameras, often have an output signal in the 100 mV−300 mV range. See *Figure 15* for a conceptual diagram. With a gain of 6 the output to the flash analog-to-digital converter is 1.8V, matching 90% of the converter's 2V input range. With a −3db bandwidth of 70 MHz for a gain of +1, the bandwidth at a gain of 6 will be 11.6 MHz. This 11.6 MHz bandwidth will result in a time constant of about 13.6 ns. This will allow the output to settle to 7 bits of accuracy within 4.9 time constants, or about 66 ns. Slewing time for a 1.8V step will be about 12 ns. The total slewing and settling time will be about 78 ns of the 150 ns pixel valid time. This will leave about 72 ns total for the flash converter signal acquisition time and tolerance for timing signals.

For scanners and copiers with moving scan bars, the SOT23-5 package is small enough to be placed next to the light sensor. The LM7131 can drive a cable to the main electronics section from the scan bar. This can reduce noise pickup by amplifying the signal before sending on the cable.

A/D Reference Drivers

The LM7131's output and drive capability make it a good choice for driving analog-to-digital references which have suddenly changing loads. The small size of the SOT23-5 package allow the LM7131 to be placed very close to the A/D reference pin, maximizing response. The small size avoids the penalty of increased board space. Often the SOT23-5 package is small enough that it can fit in space used by the large capacitors previously attached to the A/D reference. By acting as a buffer for a reference voltage, noise pickup can be reduced and the accuracy may be increased.

For additional space savings, the LM4040 precision voltage reference is available in a tiny SOT23-3 package.

Video Gain of +2

The design of the LM7131 has been optimized for gain of +2 video applications. Typical values for differential gain and phase are 0.25% differential gain and 0.75 degree differential phase. See *Figure 12*.

Improving Video Performance

Differential gain and phase performance can be improved by keeping the active video portion of the signal above 300 mV. The sync signal can go below 300 mV without affecting the video quality. If it is possible to AC couple the signal and shift the output voltage slightly higher, much better video performance is possible. For a +5V single supply, an output range between 2.0V and 3.0V can have a differential gain of 0.07% and differential phase of 0.3 degree when driving a 150Ω load. For a +3V single supply, the output should be between 1.0V and 2.0V.

Cable Driving with +5V Supplies

The LM7131 can easily drive a back-terminated 75Ω video cable (150Ω load) when powered by a +5V supply. See *Figures 2*, *3* and *4*. This makes it a good choice for video output for portable equipment, personal digital devices, and desktop video applications.

The LM7131 can also supply +2.00V to a 50Ω load to ground, making it useful as driver in 50Ω systems such as portable test equipment.

Cable Driving with +3V Supplies

The LM7131 can drive 150Ω to 2.00V when supplied by a 3V supply. This 3V performance means that the LM7131 is useful in battery powered video applications, such as camcorders, portable video mixers, still video cameras, and portable scanners.

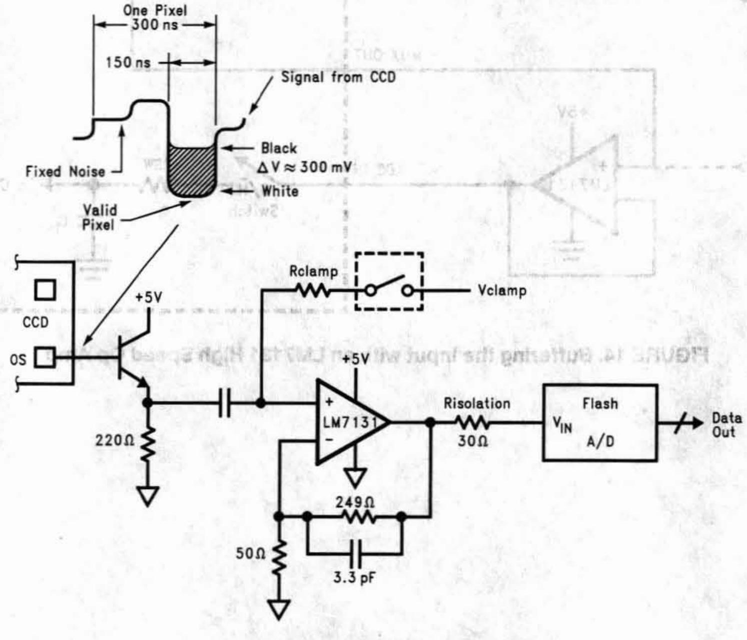


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FIGURE 15. CCD Amplifier

Using the LM7131 (Continued)

Audio and High Frequency Signal Processing

The LM7131 is useful for high fidelity audio and signal processing. A typical LM7131 is capable of driving 2V across 150Ω (referenced to ground) at less than 0.1% distortion at 4 MHz when powered by a single 5V supply.

Use with 2.5V Virtual Ground Systems with +5V Single Supply Power

Many analog systems which must work on a single +5V supply use a 'virtual ground' - a reference voltage for the signal processing which is usually between +5V and 0V. This virtual ground is usually halfway between the top and bottom supply rails. This is usually +2.5V for +5V systems and +1.5V for +3V systems.

The LM7131 can be used in single supply/virtual ground systems driving loads referenced to 2.5V. The output swing specifications in the data sheet show the tested voltage limits for driving a 150Ω load to a virtual ground supply for +3V and +5V. A look at the output swing specifications shows that for heavy loads like 150 ohms, the output will swing as close as one diode drop (roughly, 0.7V) to the supply rail. This leaves a relatively wide range for +5V systems and a somewhat narrow range for +3V systems. One way to increase this output range is to have the output load referenced to ground—this will allow the output to swing lower. Another is to use higher load impedances. The output swing specifications show typical numbers for swing with loads of 600Ω to ground. Note that these typical numbers are similar to those for a 150Ω load. These typical numbers are an indication of the maximum DC performance of the LM7131.

The sinking output of the LM7131 is somewhat lower than the amplifier's sourcing capability. This means that the LM7131 will not drive as much current into a load tied to 2.5 V as it will drive into a load tied to 0V.

Good AC performance will require keeping the output further away from the supply rails. For a +5V supply and relatively high impedance load (analog-to-digital converter input) the following are suggested as an initial starting range for achieving high (> 60 dB) AC accuracy

Upper output level—
Approximately 0.8V to 1V below the positive (V+) rail.
Lower output level—
Approximately 200 mV–300 mV above the negative rail.

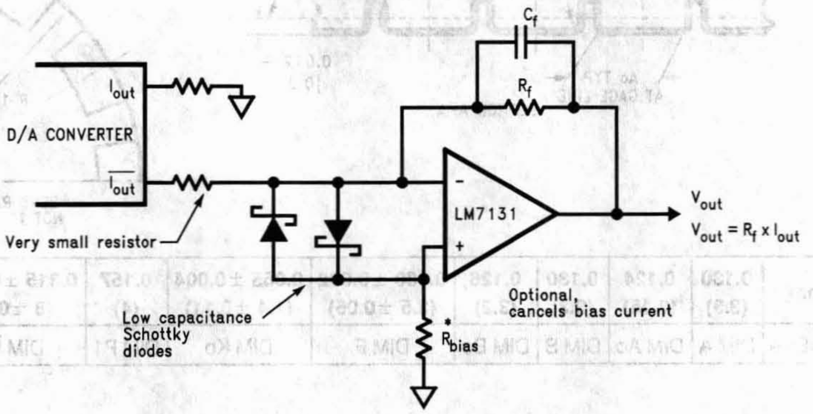
The LM7131 very useful in virtual ground systems as an output device for output loads which are referenced to 0V or the lower rail. It is also useful as a driver for capacitive loads, such as sample and hold circuits, and audio analog to digital converters. If fast amplifiers with rail-to-rail output ranges are needed, please see the National Semiconductor LM6142 datasheet.

D/A Output Amplifier

The LM7131 can be used as an output amplifier for fast digital-to-analog converters. When using the LM7131 with converters with an output voltage range which may exceed the differential input voltage limit of ±2V, it may be necessary to add protection diodes to the inputs. See *Figure 16*. For high speed applications, it may be useful to consider low capacitance schottky diodes. Additional feedback capacitance may be needed to control ringing due to the additional input capacitance from the D/A and protection diodes. When used with current output D/As, the input bias currents may produce a DC offset in the output. This offset may be canceled by a resistor between the positive input and ground.

Spice Macromodel

A SPICE macromodel of the LM7131 and many other National Semiconductor op amps is available at no charge from your National Semiconductor representative.



TL/H/12313-24

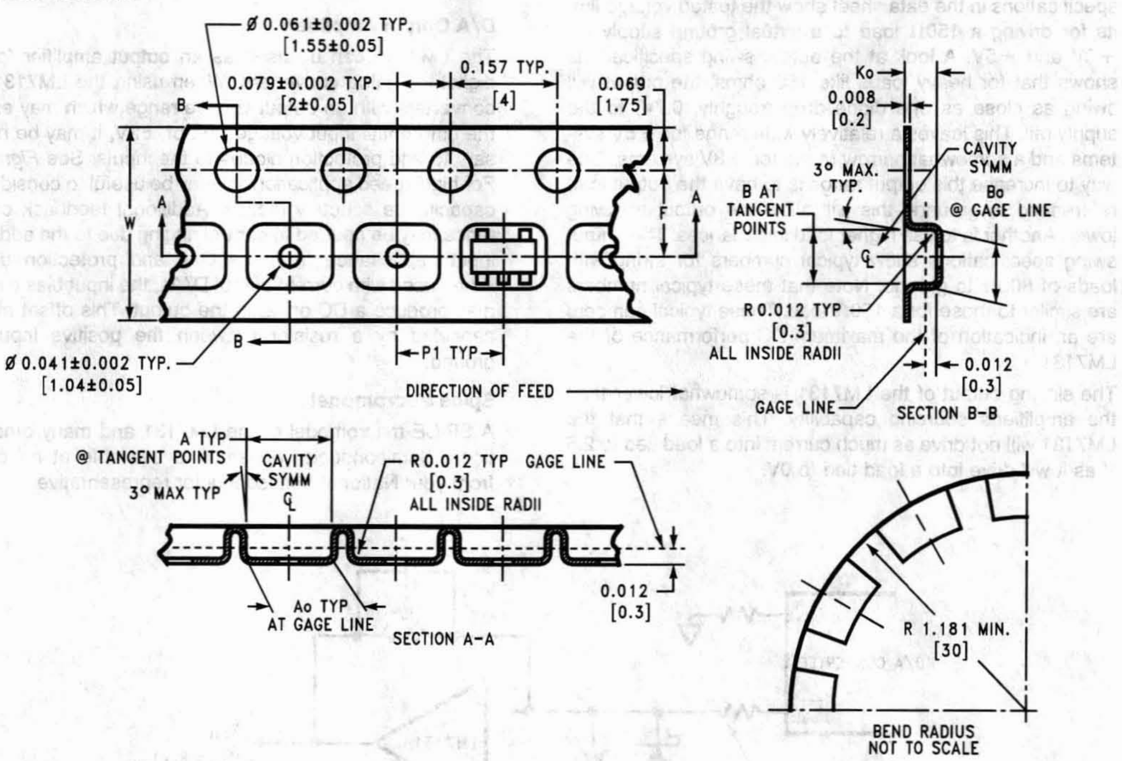
FIGURE 16. D/A Ouput Amplifier

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavaties	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

TAPE DIMENSIONS



Ø 0.061±0.002 TYP.
[1.55±0.05]
0.079±0.002 TYP.
[2±0.05]
0.157 TYP.
[4]
0.069
[1.75]
B
W
A
F
A
B
P1 TYP
Ø 0.041±0.002 TYP.
[1.04±0.05]
DIRECTION OF FEED
Ko
0.008
[0.2]
CAVITY
SYMM
3° MAX.
TYP.
B AT
TANGENT
POINTS
Bo
@ GAGE LINE
℄
R 0.012 TYP
[0.3]
ALL INSIDE RADII
0.012
[0.3]
GAGE LINE
SECTION B-B
A TYP
@ TANGENT POINTS
3° MAX TYP
CAVITY
SYMM
℄
R 0.012 TYP
[0.3]
ALL INSIDE RADII
GAGE LINE
0.012
[0.3]
Ao TYP
AT GAGE LINE
SECTION A-A
R 1.181 MIN.
[30]
BEND RADIUS
NOT TO SCALE

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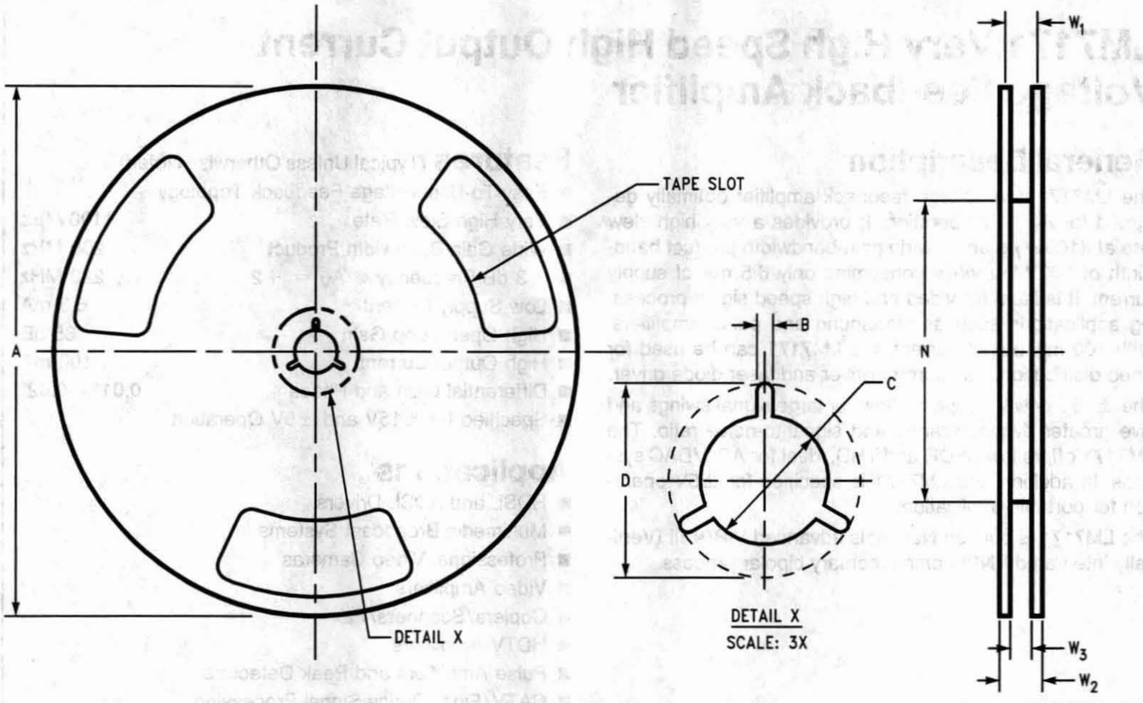
8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

SOT-23-5 Tape and Reel Specification (Continued)

REEL DIMENSIONS


TAPE SLOT
A
B
C
D
N
DETAIL X
DETAIL X
SCALE: 3X
W1
W3
W2

TL/H/12313-26

Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/ − 0.000 8.4 + 1.50/ − 0.00	0.567 14.40	W1 + 0.078/ − 0.039 W1 + 2.00/ − 1.00

National Semiconductor

ADVANCE INFORMATION

LM7171 Very High Speed High Output Current Voltage Feedback Amplifier

General Description

The LM7171 is a voltage feedback amplifier optimally designed for $A_V > 1$ operation. It provides a very high slew rate at 4100V/μs and a wide gain-bandwidth product bandwidth of 200 MHz while consuming only 6.5 mA of supply current. It is ideal for video and high speed signal processing applications such as ultrasound and pulse amplifiers. With 100 mA output current, the LM7171 can be used for video distribution, transformer driver and laser diode driver.

The ±15V power supplies allow for large signal swings and give greater dynamic range and signal-to-noise ratio. The LM7171 offers low SFDR and THD, ideal for ADC/DAC systems. In addition, the LM7171 is specified for ±5V operation for portable applications.

The LM7171 is built on Nationals advanced VIP™ III (Vertically integrated PNP) complementary bipolar process.

Features (Typical Unless Otherwise Noted)

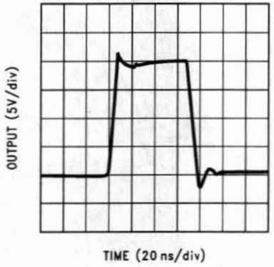
Easy-To-Use Voltage Feedback Topology	
Very High Slew Rate	4100V/μs
Wide Gain-Bandwidth Product	200 MHz
−3 dB Frequency @ $A_V = +2$	220 MHz
Low Supply Current	6.5 mA
High Open Loop Gain	85 dB
High Output Current	100 mA
Differential Gain and Phase	0.01%, 0.02°
Specified for ±15V and ±5V Operation	

Applications

- HDSL and ADSL Drivers
- Multimedia Broadcast Systems
- Professional Video Cameras
- Video Amplifiers
- Copiers/Scanners/Fax
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- CATV/Fiber Optics Signal Processing

Typical Performance

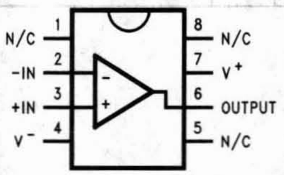
Large Signal Pulse Response
$A_V = +2, V_S = \pm 15V$



TL/H/12351-7

Connection Diagrams

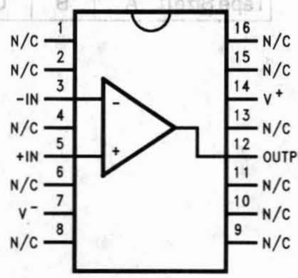
8-Pin DIP/SO



TL/H/12351-1

Top View

16-Pin Wide Body SO



TL/H/12351-2

Top View

Ordering Information

Package	Temperature Range		Transport Media	NSC Drawing
	Industrial −40°C to +85°C	Military −55°C to +125°C		
8-Pin DIP	LM7171AIN, LM7171BIN		Rails	N08E
8-Pin CDIP		5962-9553601QPA*	Rails	J08A
8-Pin Small Outline	LM7171AIM, LM7171BIM		Rails	M08A
	LM7171AIMX, LM7171BIMX		Tape and Reel	
16-Pin Small Outline	LM7171AIWM, LM7171BIWM		Rails	M16B
	LM7171AWMX, LM7171BWMX		Tape and Reel	

*For the military temperature grade, please refer to the Military Datasheet: MNLM7171AMJ/883

National Semiconductor

LM13600 Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

General Description

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers which are especially designed to complement the dynamic range of the amplifiers are provided.

Features

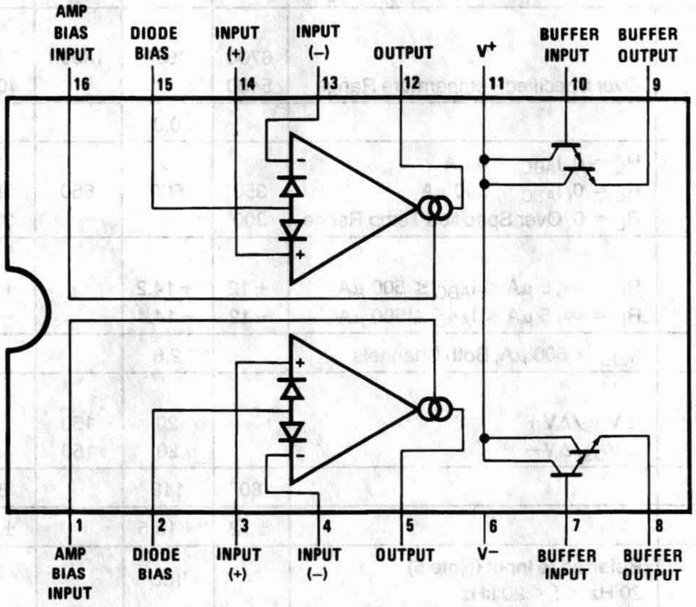
- g_m adjustable over 6 decades
- Excellent g_m linearity
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal-to-noise ratio

Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

Connection Diagram

Dual-In-Line and Small Outline Packages



AMP BIAS INPUT
16
DIODE BIAS
15
INPUT (+)
14
INPUT (−)
13
OUTPUT
12
V+
11
BUFFER INPUT
10
BUFFER OUTPUT
9
1
AMP BIAS INPUT
2
DIODE BIAS
3
INPUT (+)
4
INPUT (−)
5
OUTPUT
6
V−
7
BUFFER INPUT
8
BUFFER OUTPUT
+
−

TL/H/7980-2

Top View

Order Number LM13600M, LM13600N or LM13600AN
See NS Package Number M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 1)	
LM13600	36 V_{DC} or $\pm 18V$
LM13600A	44 V_{DC} or $\pm 22V$
Power Dissipation (Note 2) $T_A = 25°C$	570 mW
Differential Input Voltage	±5V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_{ABC})	2 mA
Output Short Circuit Duration	Continuous
Buffer Output Current (Note 3)	20 mA

Operating Temperature Range	0°C to +70°C
DC Input Voltage	$+V_S$ to $-V_S$
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM13600 Min	LM13600 Typ	LM13600 Max	LM13600A Min	LM13600A Typ	LM13600A Max	Unit
Input Offset Voltage (V_{OS})			0.4	4		0.4	1	mV
	Over Specified Temperature Range						2	mV
	$I_{ABC} = 5\ \mu A$		0.3	4		0.3	1	mV
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 µA		0.5	5		0.5	2	mV
Input Offset Change	$5\ \mu A \le I_{ABC} \le 500\ \mu A$		0.1	3		0.1	1	mV
Input Offset Current			0.1	0.6		0.1	0.6	µA
Input Bias Current			0.4	5		0.4	5	µA
	Over Specified Temperature Range		1	8		1	7	µA
Forward Transconductance (g_m)		6700	9600	13000	7700	9600	12000	µmh
	Over Specified Temperature Range	5400			4000			µmh
g_m Tracking			0.3			0.3		dB
Peak Output Current	$R_L = 0$, $I_{ABC} = 5\ \mu A$		5		3	5	7	µA
	$R_L = 0$, $I_{ABC} = 500\ \mu A$	350	500	650	350	500	650	µA
	$R_L = 0$, Over Specified Temp Range	300			300			µA
Peak Output Voltage								
Positive	$R_L = \infty$, $5\ \mu A \le I_{ABC} \le 500\ \mu A$	+12	+14.2		+12	+14.2		V
Negative	$R_L = \infty$, $5\ \mu A \le I_{ABC} \le 500\ \mu A$	−12	−14.4		−12	−14.4		V
Supply Current	$I_{ABC} = 500\ \mu A$, Both Channels		2.6			2.6		mA
V_{OS} Sensitivity								
Positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	µV/V
Negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	µV/V
CMRR		80	110		80	110		dB
Common Mode Range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 kHz		100			100		dB
Differential Input Current	$I_{ABC} = 0$, Input = ±4V		0.02	100		0.02	10	nA
Leakage Current	$I_{ABC} = 0$ (Refer to Test Circuit)		0.2	100		0.2	5	nA

Electrical Characteristics (Note 4) (Continued)

Parameter	Conditions	LM13600			LM13600A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Resistance		10	26		10	26		kΩ
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μs
Buffer Input Current	(Note 5), Except $I_{ABC} = 0\ \mu A$		0.2	0.4		0.2	0.4	μA
Peak Buffer Output Voltage	(Note 5)	10			10			V

Note 1: For selections to a supply voltage above ±22V, contact factory.

Note 2: For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in still air.

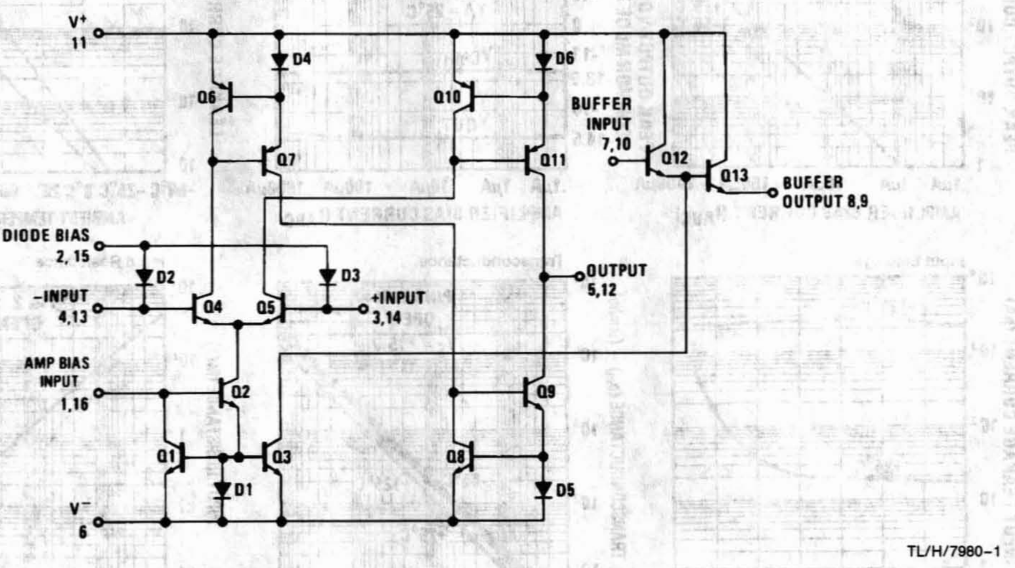
Note 3: Buffer output current should be limited so as to not exceed package dissipation.

Note 4: These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current (I_{ABC}) = 500 μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 5: These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500\ \mu A$, $R_{OUT} = 5\ k\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

Schematic Diagram

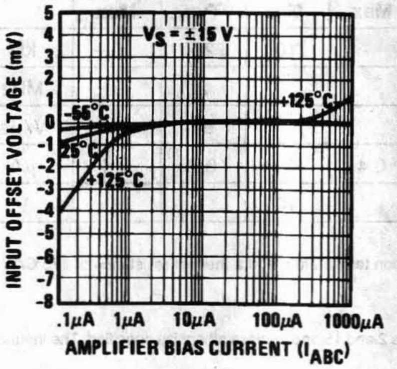
One Operational Transconductance Amplifier


V+
11
D4
Q6
Q7
Q10
D6
BUFFER
INPUT
7,10
Q11
Q12
Q13
BUFFER
OUTPUT 8,9
DIODE BIAS
2, 15
D2
D3
−INPUT
4,13
Q4
Q5
+INPUT
3,14
OUTPUT
5,12
AMP BIAS
INPUT
1,16
Q2
Q9
Q1
Q3
Q8
D1
D5
V−
6

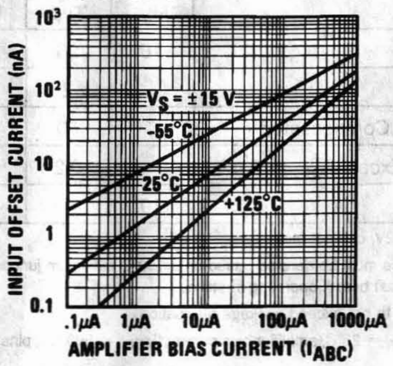
TL/H/7980–1

Typical Performance Characteristics

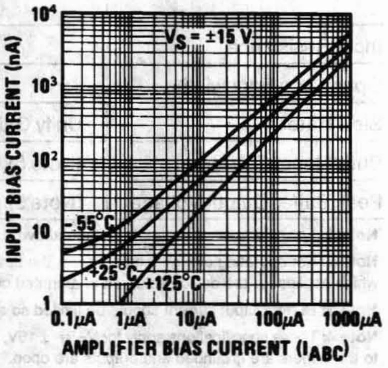
Input Offset Voltage



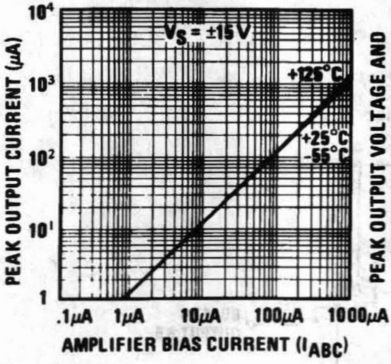
Input Offset Current



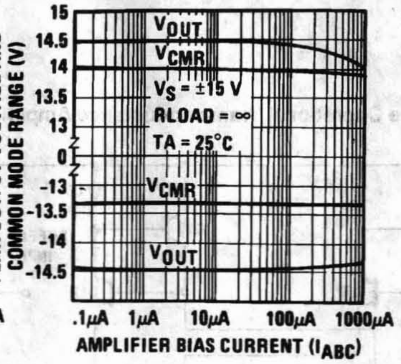
Input Bias Current



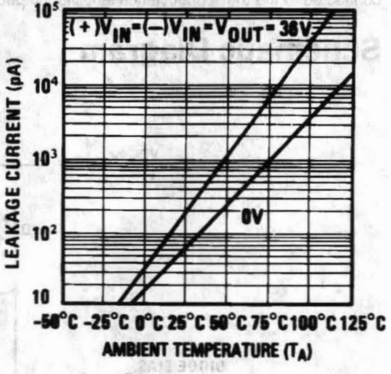
Peak Output Current



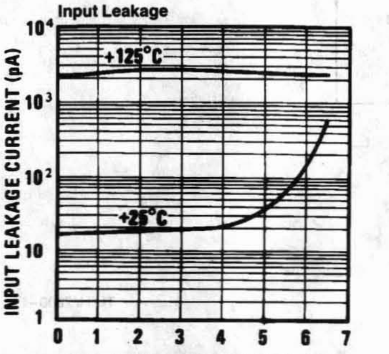
Peak Output Voltage and Common Mode Range



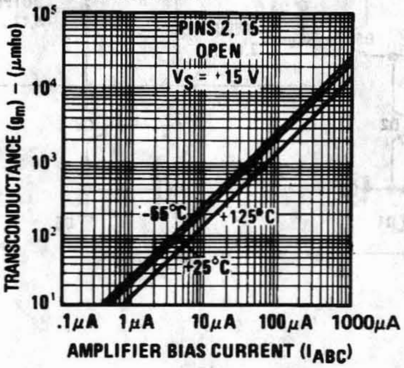
Leakage Current



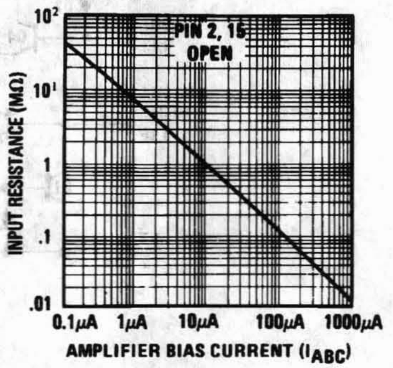
Input Leakage



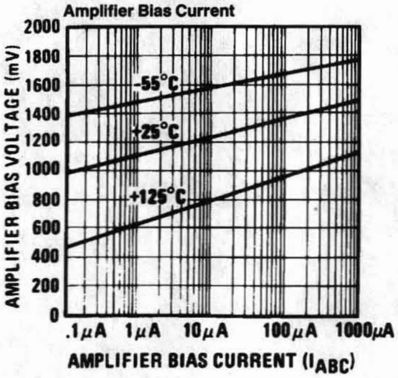
Transconductance



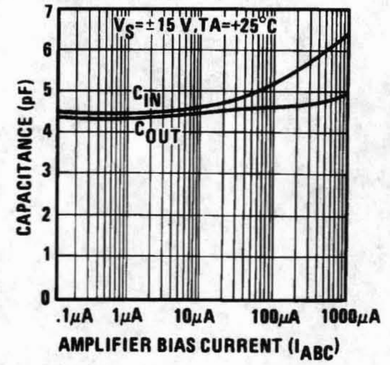
Input Resistance



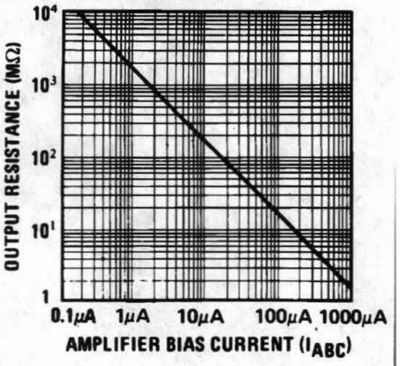
Amplifier Bias Voltage vs Amplifier Bias Current



Input and Output Capacitance

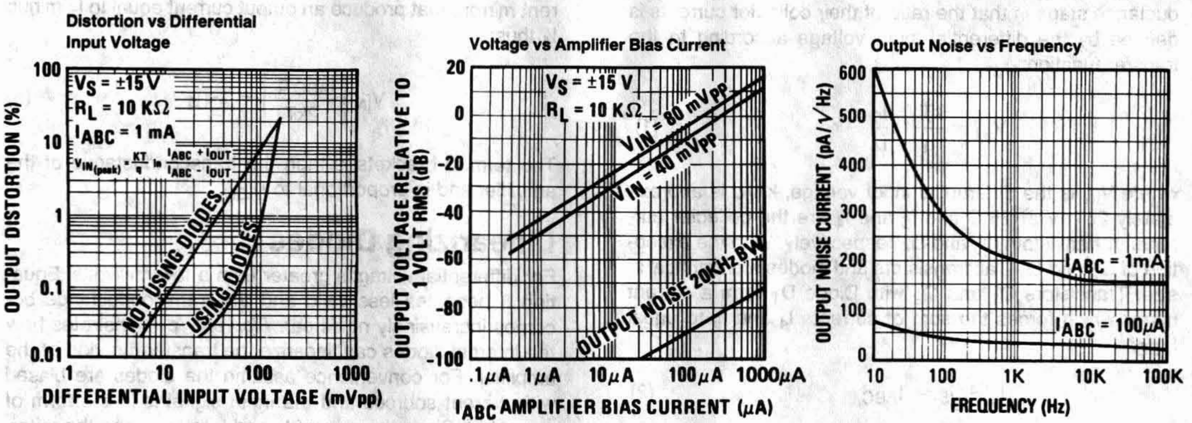


Output Resistance



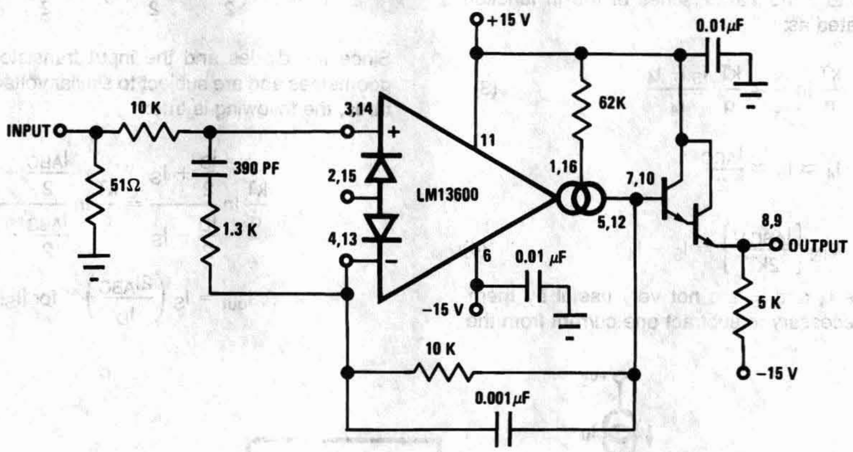
TL/H/7980–3

Typical Performance Characteristics (Continued)



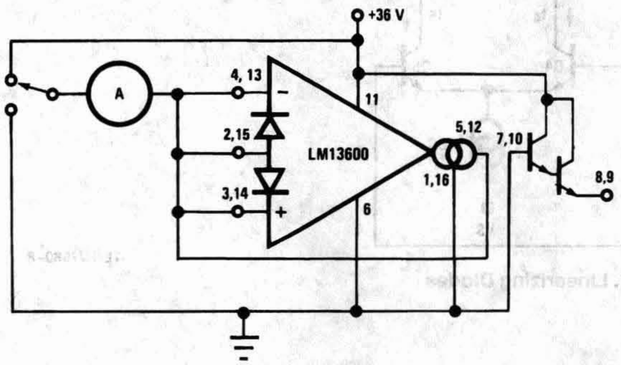
TL/H/7980-4

Unity Gain Follower


+15 V
0.01μF
62K
INPUT
10 K
3,14
+
390 PF
51Ω
2,15
1.3 K
4,13
−
LM13600
11
1,16
7,10
5,12
8,9
OUTPUT
6
0.01 μF
−15 V
5 K
−15 V
10 K
0.001μF

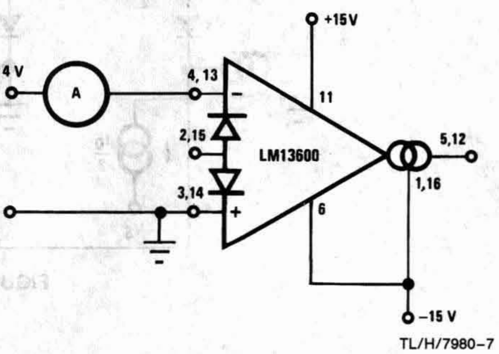
TL/H/7980-5

Leakage Current Test Circuit


+36 V
A
4, 13
−
2,15
LM13600
3,14
+
11
6
5,12
1,16
7,10
8,9

TL/H/7980-6

Differential Input Current Test Circuit


+15V
±4 V
A
4, 13
−
2,15
LM13600
3,14
+
11
6
5,12
1,16
−15 V

TL/H/7980-7

Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \qquad (1)$$

where V_{IN} is the differential input voltage, kT/q is approximately 26 mV at 25°C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC}:

$$I_4 + I_5 = I_{ABC} \qquad (2)$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \qquad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN} \left[\frac{I_{ABC}\, q}{2kT} \right] = I_5 - I_4 \qquad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN} \left[\frac{I_{ABC}\, q}{2kT} \right] = I_{OUT} \qquad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC}.

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. *Figure 1* demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S. Since the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2},\ I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{out}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left(\frac{2 I_{ABC}}{I_D} \right) \quad \text{for } |I_S| < \frac{I_D}{2} \qquad (6)$$

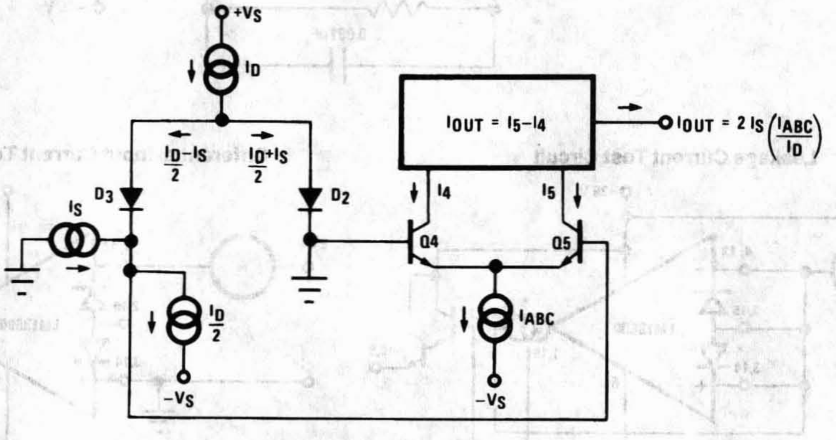


FIGURE 1. Linearizing Diodes

Linearizing Diodes (Continued)

Notice that in deriving Equation 6 no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

Controlled Impedance Buffers

The upper limit of transconductance is defined by the maximum value of I_{ABC} (2 mA). The lowest value of I_{ABC} for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_{ABC}, a buffer which has very low input bias current is desirable. An FET follower satisfies the low input current requirement, but is somewhat non-linear for large voltage swing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of I_{ABC}, the buffer's input current is minimal. At higher levels of I_{ABC}, transistor Q_3 biases up Q_{12} with a current proportional to I_{ABC} for fast slew rate. When I_{ABC} is changed, the DC level of the Darlington output buffer will shift. In audio applications where I_{ABC} is changed suddenly, this shift may produce an audible "pop". For these applications the LM13700 may produce superior results.

Applications—Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in *Figure 3*. This circuit is similar to *Figure 1* and operates the same. The potentiometer in *Figure 2* is adjusted to minimize the effects of the control signal at the output.

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} *(Figure 2)* until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

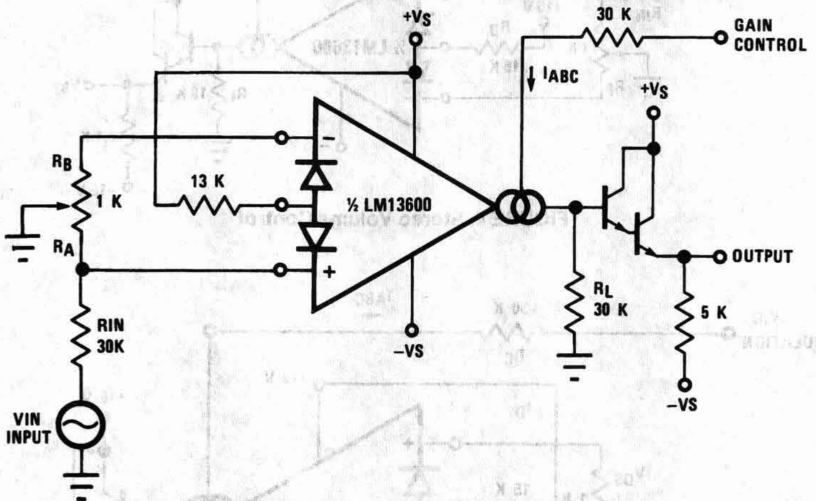


FIGURE 2. Voltage Controlled Amplifier

TL/H/7980-9

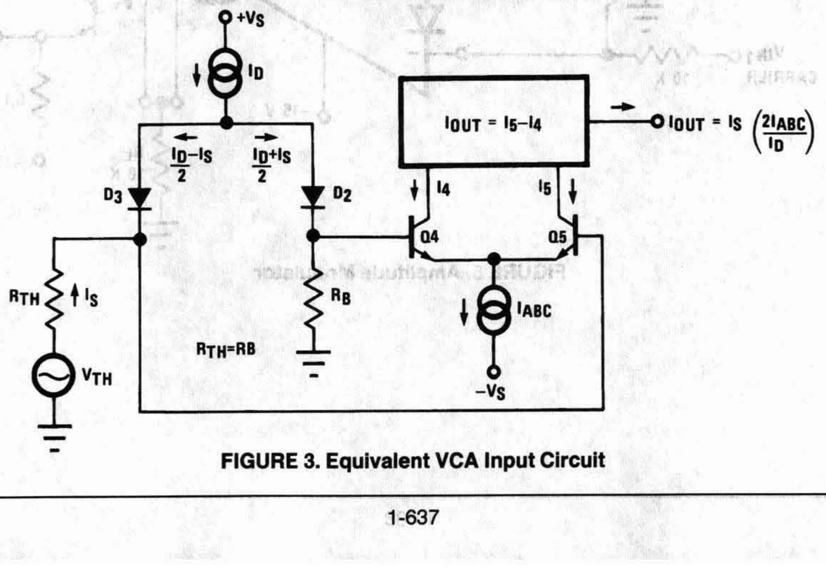


FIGURE 3. Equivalent VCA Input Circuit

TL/H/7980-10

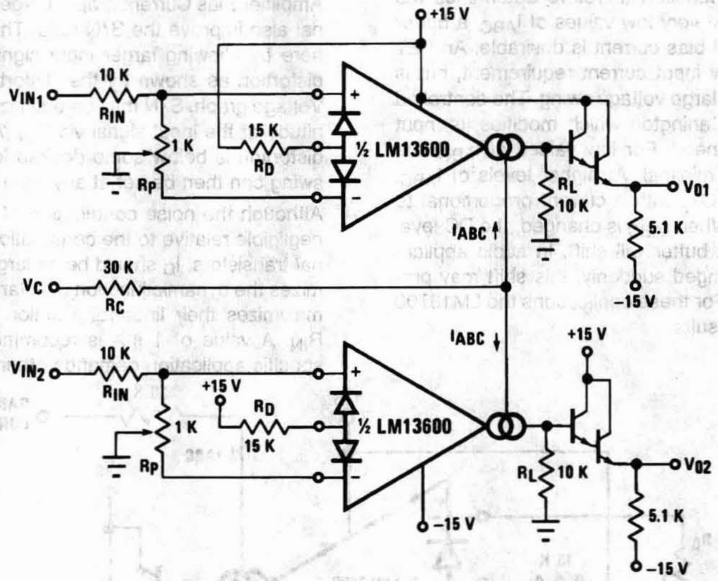
Stereo Volume Control

The circuit of Figure 4 uses the excellent matching of the two LM13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. R_P is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for *Figure 2* as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in *Figure 5*, where:

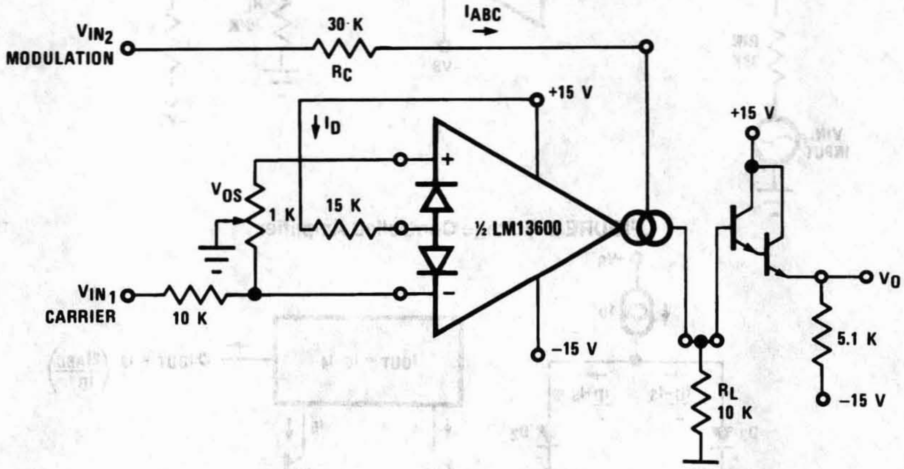
$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^- + 1.4V)}{R_C}$$



+15 V
10 K
V_{IN1}
R_{IN}
1 K
R_P
15 K
R_D
½ LM13600
R_L
10 K
V_{01}
5.1 K
−15 V
I_{ABC}
V_C
30 K
R_C
+15 V
10 K
V_{IN2}
R_{IN}
+15 V
R_D
1 K
15 K
R_P
½ LM13600
R_L
10 K
V_{02}
5.1 K
−15 V
−15 V

TL/H/7980–11

FIGURE 4. Stereo Volume Control



V_{IN2}
MODULATION
30 K
R_C
I_{ABC}
+15 V
I_D
V_{OS}
1 K
15 K
½ LM13600
V_{IN1}
CARRIER
10 K
−15 V
+15 V
V_O
5.1 K
−15 V
R_L
10 K

TL/H/7980–12

FIGURE 5. Amplitude Modulator

Stereo Volume Control (Continued)

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C/2\ (V^- + 1.4V)$ into I_O. The circuit of *Figure 6* adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O.

Noting that the gain of the LM13600 amplifier of *Figure 3* may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC}, *Figure 7* shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3\ V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

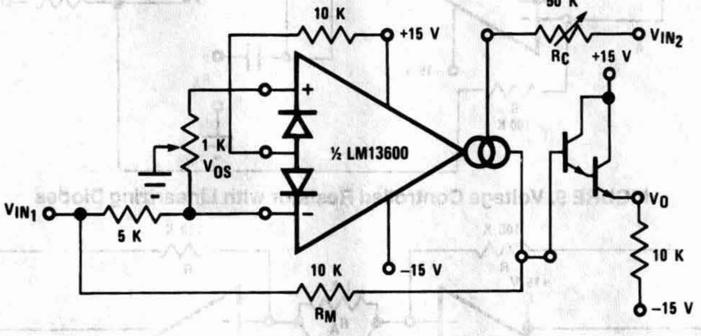
Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in *Figure 8*. A signal voltage applied at R_X generates a V_{IN} to the LM13600 which is then multiplied by the g_m of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

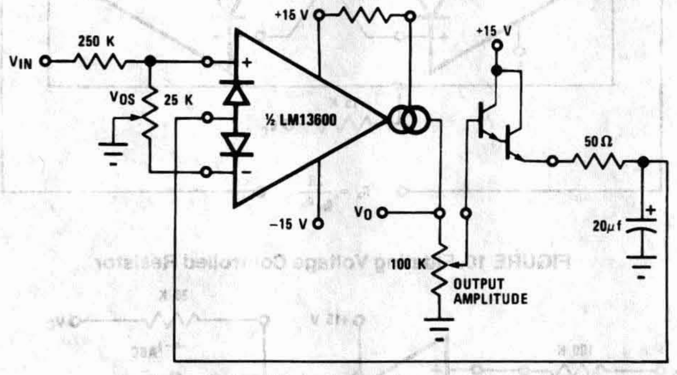
where $g_m \approx 19.2\ I_{ABC}$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13600 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in *Figure 10*, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13600.


10 K
+15 V
50 K
V_{IN2}
R_C
+15 V
1 K
V_{OS}
½ LM13600
V_{IN1}
5 K
10 K
−15 V
R_M
V_O
10 K
−15 V

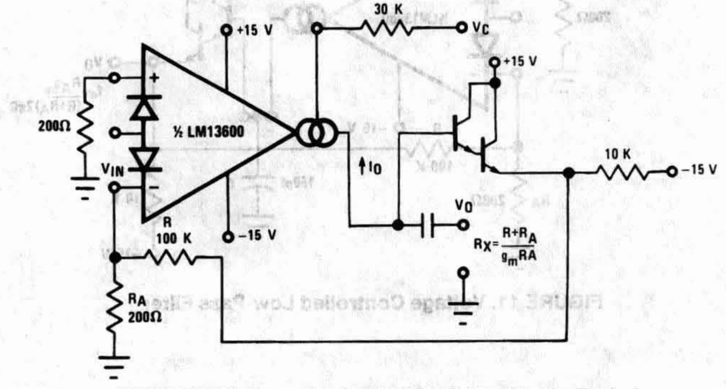
TL/H/7980-13

FIGURE 6. Four-Quadrant Multiplier


30 K
+15 V
250 K
V_{IN}
V_{OS}
25 K
½ LM13600
+15 V
50Ω
−15 V
V_O
20µf
100 K
OUTPUT
AMPLITUDE

TL/H/7980-14

FIGURE 7. AGC Amplifier


+15 V
30 K
V_C
+15 V
200Ω
½ LM13600
V_{IN}
I_O
10 K
−15 V
V_O
R
100 K
−15 V
$R_X = \frac{R+R_A}{g_m R_A}$
R_A
200Ω

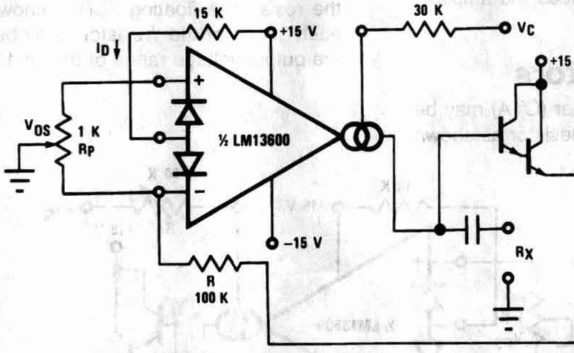
TL/H/7980-15

FIGURE 8. Voltage Controlled Resistor, Single-Ended

Voltage Controlled Filters

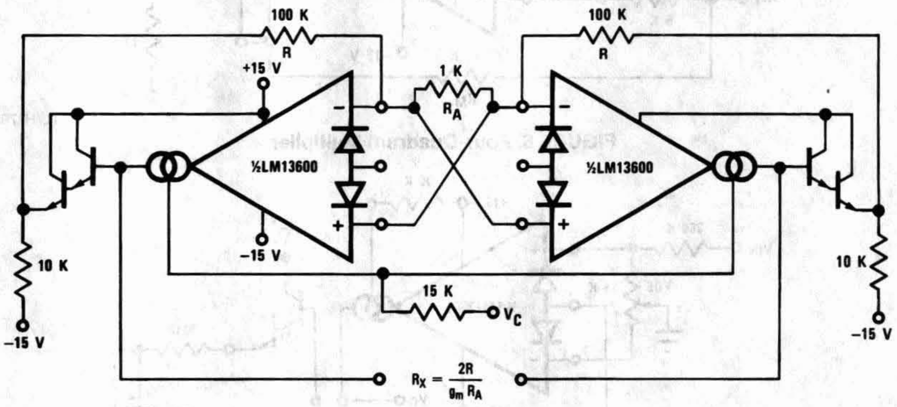
OTA's are extremely useful for implementing voltage controlled filters, with the LM13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of *Figure 11* performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a −3 dB point defined by the given equation, where g_m is again 19.2 × I_{ABC} at room temperature. *Figur* *12* shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher ord filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of *Figure 13* and the state variable filter of *Figure 14*. Due to the excellent g_m tracking of the two amplifiers and the varied bias of the buffer Darlingtons, these filters perform well over several decades of frequency.


15 K
+15 V
I_D
30 K
V_C
+15 V
V_{OS}
1 K
R_P
½ LM13600
10 K
−15 V
−15 V
R_X
R
100 K

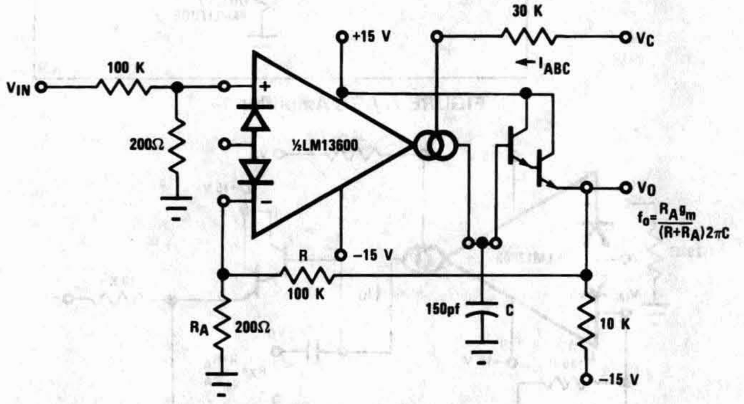
TL/H/7980-16

FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes


100 K
R
100 K
R
+15 V
1 K
R_A
½LM13600
½LM13600
10 K
−15 V
−15 V
15 K
V_C
10 K
−15 V
$R_X = \frac{2R}{g_m R_A}$

TL/H/7980-1

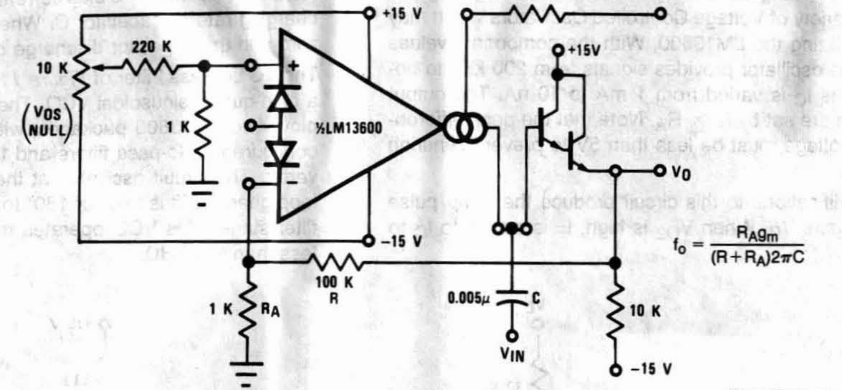
FIGURE 10. Floating Voltage Controlled Resistor


+15 V
30 K
V_C
I_{ABC}
100 K
V_{IN}
200Ω
½LM13600
V_O
$f_o = \frac{R_A g_m}{(R+R_A)2\pi C}$
R
−15 V
100 K
R_A
200Ω
150pf
C
10 K
−15 V

TL/H/7980-18

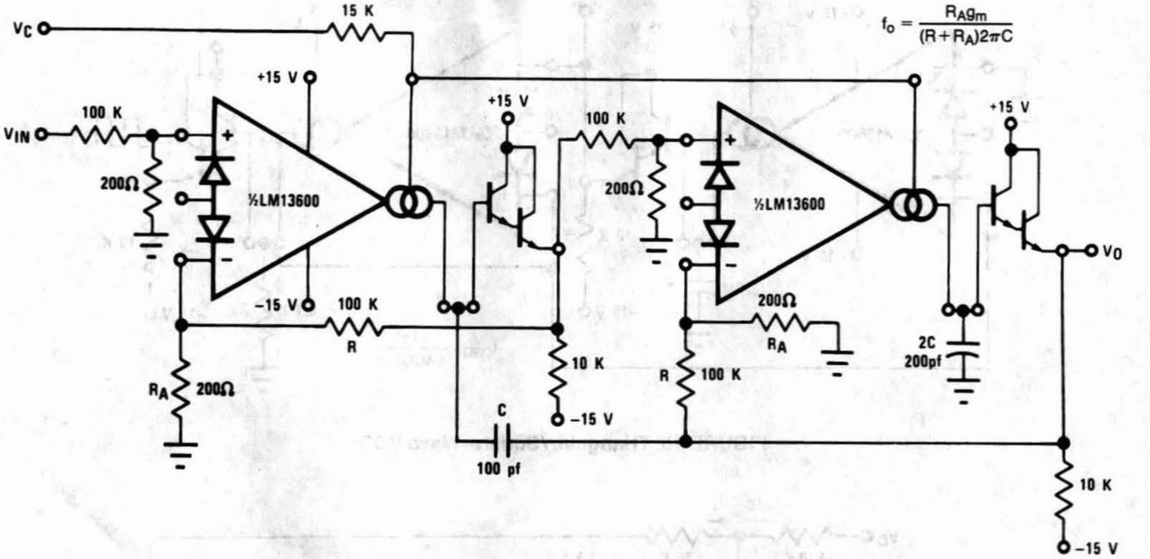
FIGURE 11. Voltage Controlled Low-Pass Filter

Voltage Controlled Filters (Continued)


+15 V
30 K
+15V
10 K
220 K
(VOS NULL)
1 K
½LM13600
+
−
−15 V
V_O
$f_o = \frac{R_A g_m}{(R+R_A)2\pi C}$
100 K
R
1 K
R_A
0.005µ
C
V_{IN}
10 K
−15 V

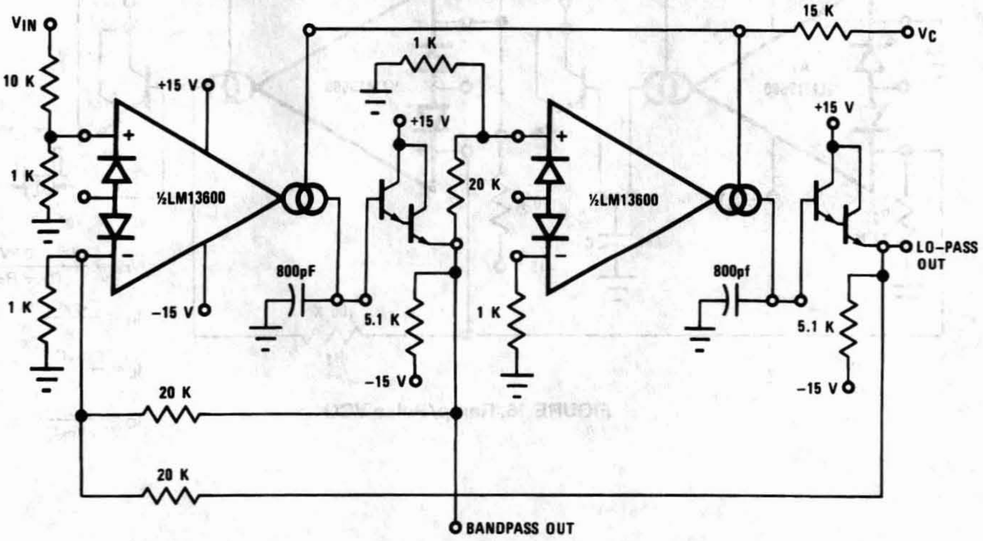
TL/H/7980–19

FIGURE 12. Voltage Controlled Hi-Pass Filter


V_C
15 K
$f_o = \frac{R_A g_m}{(R+R_A)2\pi C}$
+15 V
V_{IN}
100 K
200Ω
½LM13600
−15 V
100 K
R
R_A
200Ω
+15 V
100 K
200Ω
½LM13600
200Ω
R_A
10 K
−15 V
C
100 pf
R
100 K
2C
200pf
+15 V
V_O
10 K
−15 V

TL/H/7980–20

FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter


V_{IN}
10 K
1 K
1 K
+15 V
½LM13600
−15 V
1 K
15 K
V_C
+15 V
20 K
800pF
5.1 K
−15 V
1 K
½LM13600
+15 V
800pf
5.1 K
−15 V
LO-PASS OUT
20 K
20 K
BANDPASS OUT

TL/H/7980–21

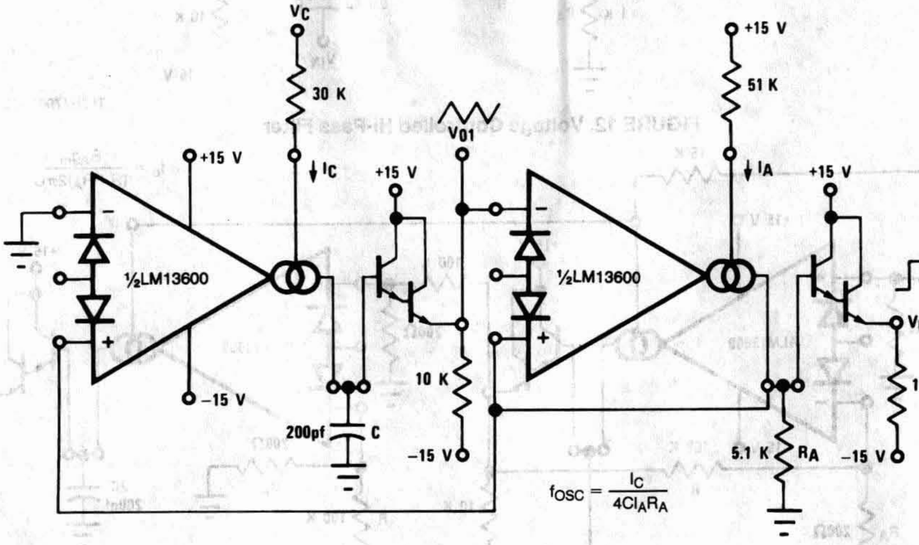
FIGURE 14. Voltage Controlled State Variable Filter

Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of *Figure 15* is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of *Figure 16*. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to inc charging rate of capacitor C. When V_{O2} is low, I_F to zero and the capacitor discharge current is set by I_C.

The VC Lo-Pass Filter of *Figure 11* may be used to produce a high-quality sinusoidal VCO. The circuit of *Figure 16* employs two LM13600 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

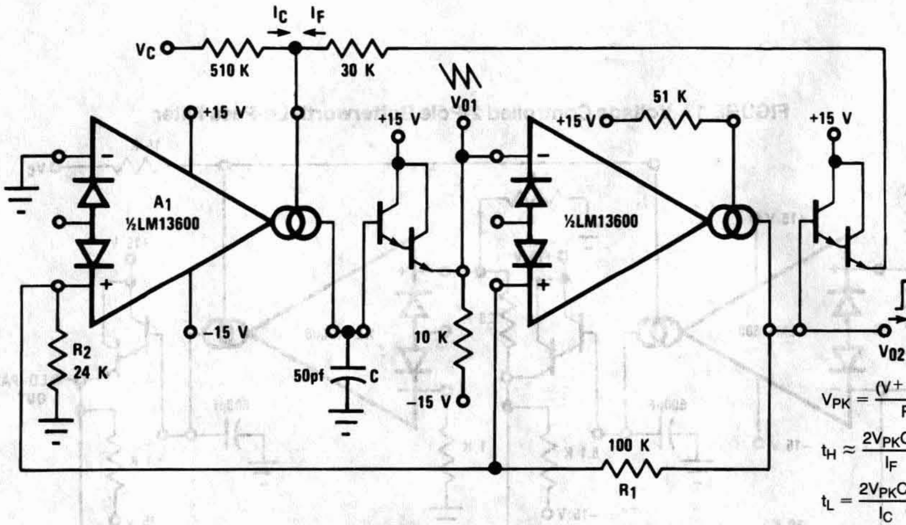


VC
30 K
IC
+15 V
+15 V
VO1
½LM13600
200pf
C
10 K
−15 V
−15 V
+15 V
51 K
IA
+15 V
½LM13600
VO2
10 K
5.1 K
RA
−15 V

$$f_{OSC} = \frac{I_C}{4CI_AR_A}$$

TL/H/7980-22

FIGURE 15. Triangular/Square-Wave VCO



IC
IF
VC
510 K
30 K
+15 V
VO1
+15 V
51 K
+15 V
+15 V
A1
½LM13600
½LM13600
−15 V
R2
24 K
50pf
C
10 K
−15 V
tH
tL
VO2
100 K
R1

$$V_{PK} = \frac{(V^+ - 0.8V)R_2}{R_1 + R_2}$$

$$t_H \approx \frac{2V_{PK}C}{I_F}$$

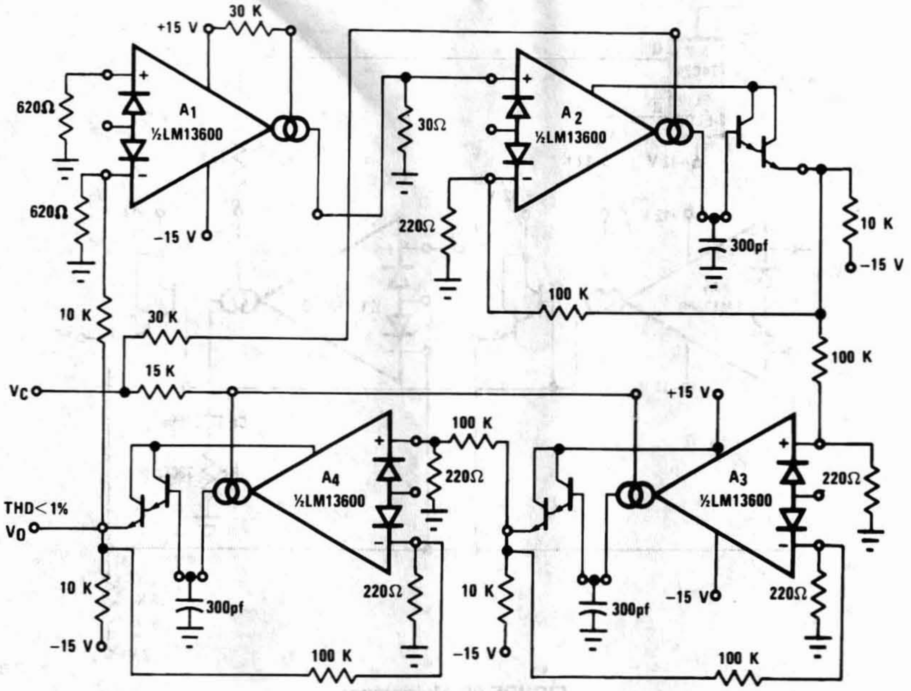
$$t_L = \frac{2V_{PK}C}{I_C}$$

$$f_O \approx \frac{I_C}{2V_{PK}C} \text{ for } I_C \ll I_F$$

TL/H/7980-23

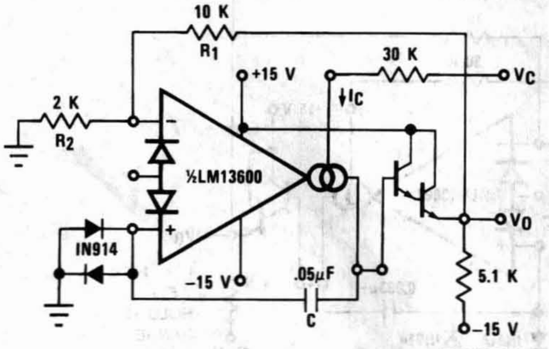
FIGURE 16. Ramp/Pulse VCO

Voltage Controlled Oscillators (Continued)


+15 V
30 K
620Ω
620Ω
A1
½LM13600
−15 V
30Ω
A2
½LM13600
220Ω
300pf
10 K
−15 V
100 K
10 K
30 K
15 K
100 K
Vc
+15 V
100 K
A4
½LM13600
220Ω
A3
½LM13600
220Ω
THD<1%
Vo
10 K
300pf
220Ω
10 K
300pf
−15 V
220Ω
−15 V
100 K
−15 V
100 K

TL/H/7980-24

FIGURE 17. Sinusoidal VCO


10 K
R1
+15 V
30 K
Vc
Ic
2 K
R2
½LM13600
Vo
IN914
−15 V
.05µF
C
5.1 K
−15 V

TL/H/7980-25

FIGURE 18. Single Amplifier VCO

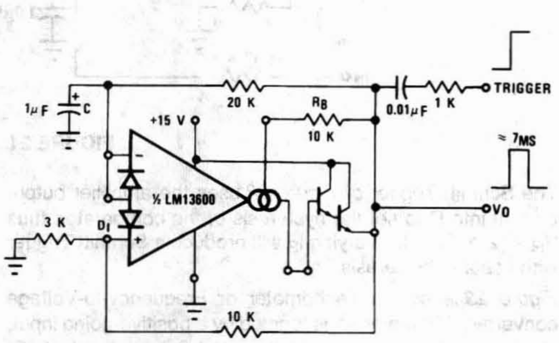
Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is increased by shorting the diode bias pin to the inverting input so than an additional discharge current flows through D_I when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

The operation of the multiplexer of *Figure 20* is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13600 slew rate into 150 pF when the (V_{IN1}-V_{IN2}) differential is at its maximum allowable value of 5V.

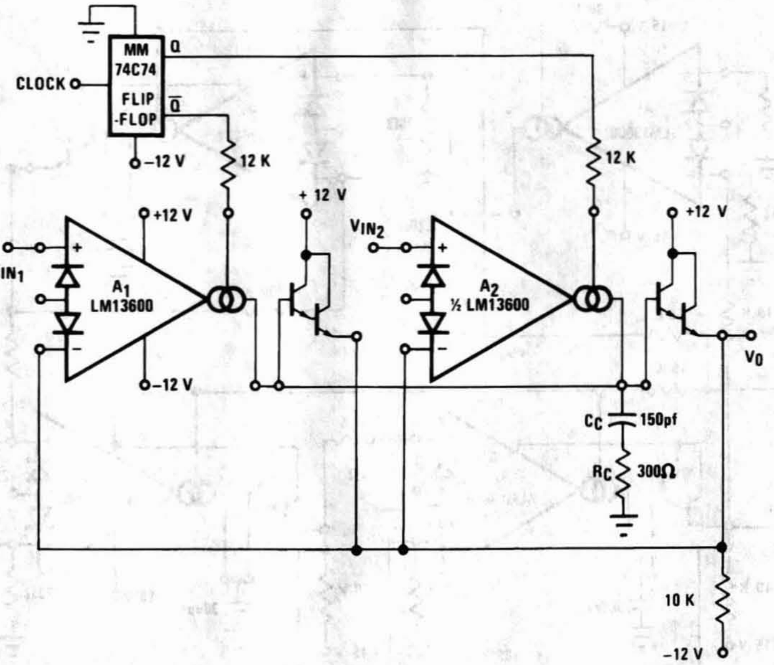
The Phase-Locked Loop of *Figure 21* uses the four-quadrant multiplier of *Figure 6* and the VCO of *Figure 18* to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.


1µF
C
20 K
RB
10 K
0.01µF
1 K
TRIGGER
≈7MS
+15 V
½ LM13600
3 K
DI
VO
10 K

TL/H/7980-26

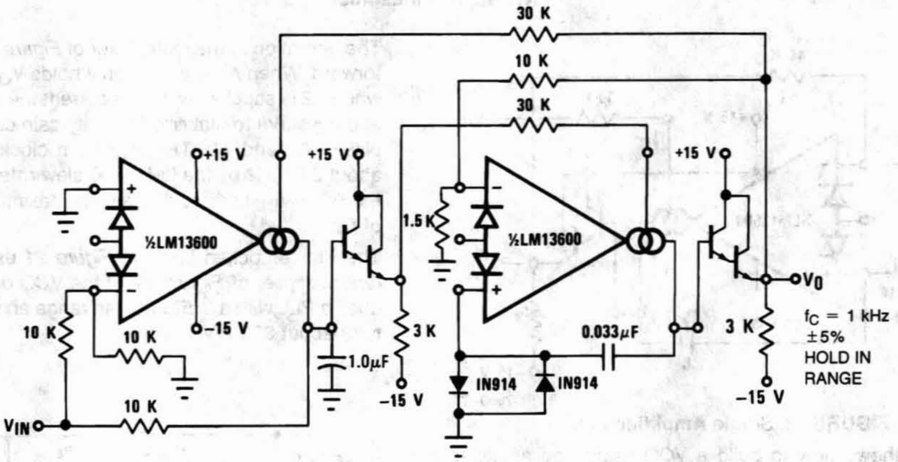
FIGURE 19. Zero Stand-By Power Timer

Additional Applications (Continued)


MM
74C74
FLIP
-FLOP
Q
$\overline{Q}$
CLOCK
−12 V
12 K
12 K
+12 V
+ 12 V
+12 V
−12 V
V_{IN_1}
A_1
LM13600
V_{IN_2}
A_2
½ LM13600
V_O
C_C
150pf
R_C
300Ω
10 K
−12 V

TL/H/7980-27

FIGURE 20. Multiplexer


30 K
10 K
30 K
+15 V
+15 V
+15 V
½LM13600
½LM13600
1.5 K
−15 V
10 K
10 K
10 K
V_{IN}
1.0μF
3 K
−15 V
0.033μF
IN914
IN914
3 K
V_O
f_C = 1 kHz
±5%
HOLD IN
RANGE
−15 V

TL/H/7980-28

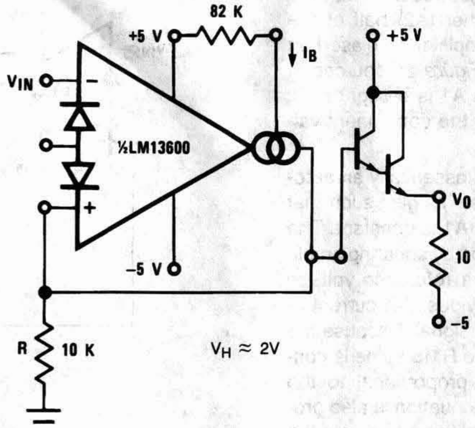
FIGURE 21. Phase Lock Loop

The Schmitt Trigger of *Figure 22* uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\ C_t$ is sourced into C_f and R_t. This once-per-cycle charge is then balanced by the current of V_O/R_t. The maximum f_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13600. D1 is added to provide a discharge path for C_t when A1 switches low.

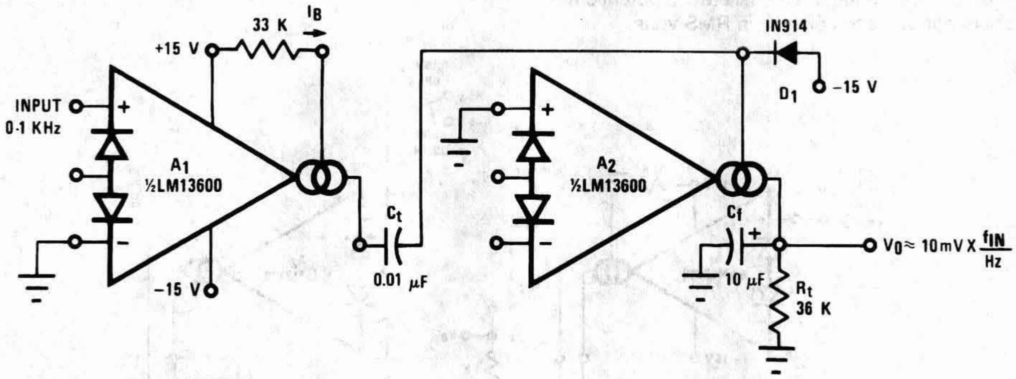
The Peak Detector of *Figure 24* uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to V_{IN}PK. One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A2 since the A1 Darlington will be turned on and off with A1. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

Additional Applications (Continued)


82 K
+5 V
I_B
+5 V
V_IN
–
½LM13600
+
–5 V
V_O
10 K
–5 V
R
10 K
V_H ≈ 2V

TL/H/7980-29

FIGURE 22. Schmitt Trigger


33 K
I_B
+15 V
INPUT
0-1 KHz
+
A1
½LM13600
–
–15 V
C_t
0.01 μF
+
A2
½LM13600
–
IN914
D1
–15 V
C_f
10 μF
R_t
36 K
V_O ≈ 10mV X f_IN/Hz

TL/H/7980-30

FIGURE 23. Tachometer

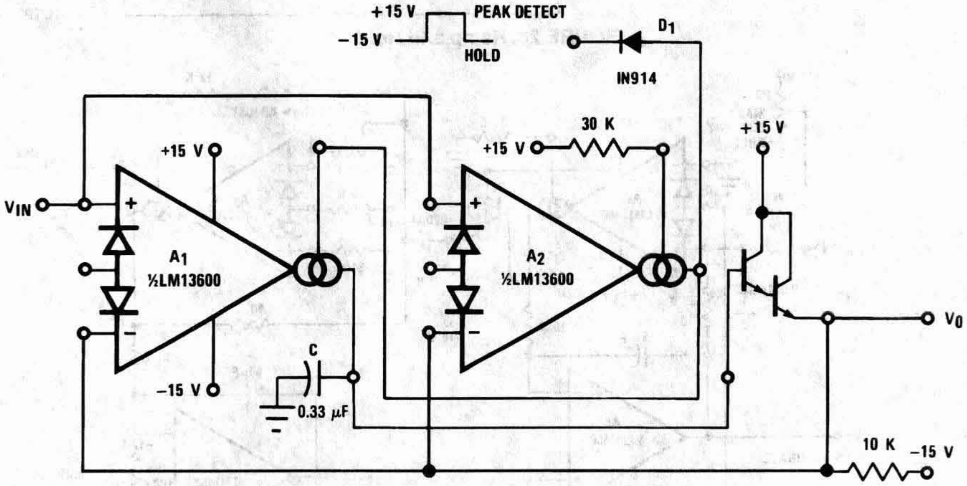

+15 V
–15 V
PEAK DETECT
HOLD
D1
IN914
30 K
+15 V
+15 V
+15 V
V_IN
+
A1
½LM13600
–
–15 V
C
0.33 μF
+
A2
½LM13600
–
V_O
10 K
–15 V

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FIGURE 24. Peak Detector and Hold Circuit

Additional Applications (Continued)

The Sample-Hold circuit of *Figure 25* also requires that the Darlington buffer used be from the other (A2) half of the package and that the corresponding amplifier be biased on continuously. The Ramp-and-Hold of *Figure 26* sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1 V/ms for the component values shown.

The true-RMS converter of *Figure 27* is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

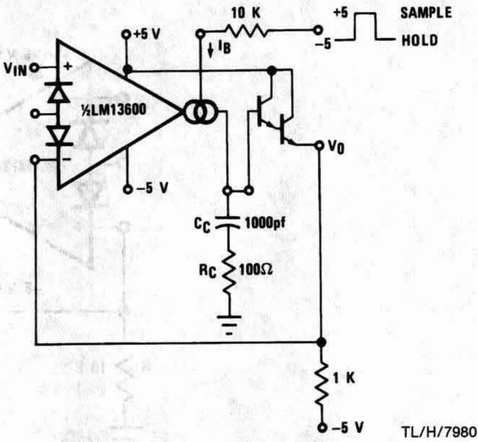
10 K
+5
SAMPLE
HOLD
−5
+5 V
I_B
V_{IN}
½LM13600
V_O
−5 V
C_C
1000pf
R_C
100Ω
1 K
−5 V

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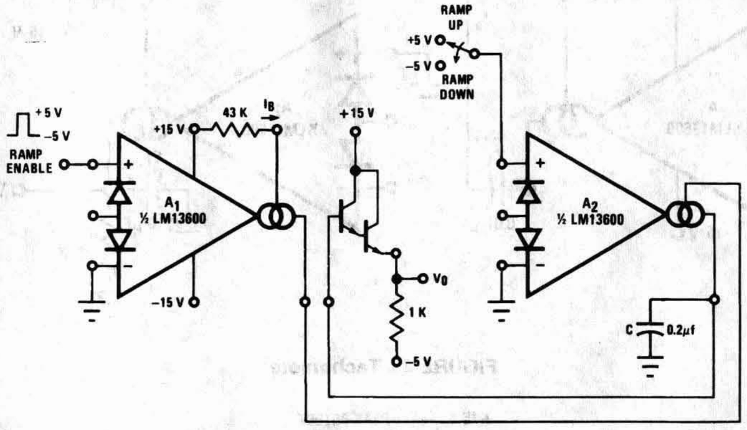
FIGURE 25. Sample-Hold Circuit


RAMP UP
+5 V
−5 V
RAMP DOWN
+5 V
−5 V
RAMP ENABLE
+15 V
43 K
I_B
+15 V
A_1
½ LM13600
−15 V
A_2
½ LM13600
V_O
1 K
−5 V
C
0.2µf

TL/H/7980–33

FIGURE 26. Ramp and Hold

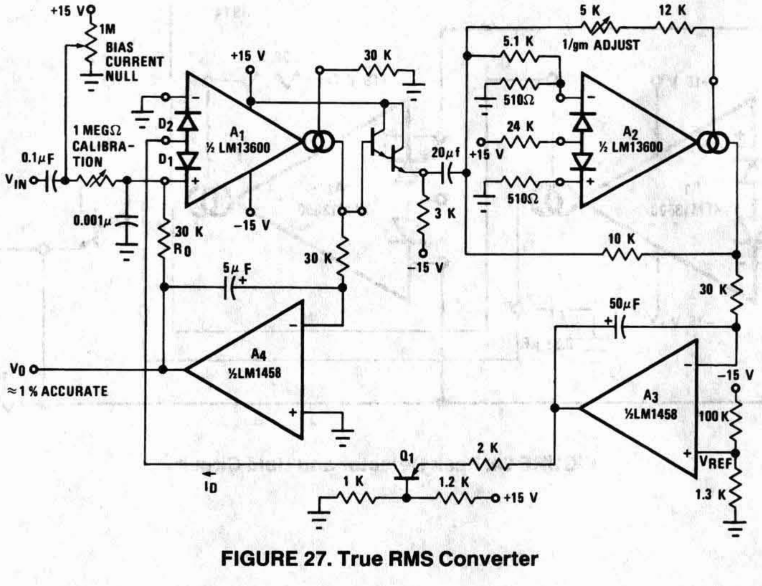

+15 V
1M
BIAS CURRENT NULL
+15 V
30 K
5 K
12 K
5.1 K
1/gm ADJUST
510Ω
D_2
D_1
A_1
½ LM13600
1 MEGΩ
CALIBRA-TION
0.1µF
V_{IN}
0.001µ
30 K
R_O
−15 V
20µf
+15 V
24 K
A_2
½ LM13600
510Ω
3 K
−15 V
10 K
5µF
30 K
30 K
50µF
A_4
½LM1458
V_O
≈1% ACCURATE
A_3
½LM1458
−15 V
100 K
V_{REF}
1.3 K
Q_1
2 K
I_D
1 K
1.2 K
+15 V

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FIGURE 27. True RMS Converter

Additional Applications (Continued)

The circuit of *Figure 28* is a voltage reference of variable temperature coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The log amplifier of *Figure 29* responds to the ratio of currents through buffer transistors Q3 and Q4. Zero temperature dependence for V_{OUT} is ensured because the TC of the A2 transfer function is equal and opposite to the TC of the logging transistors Q3 and Q4.

The wide dynamic range of the LM13600 allows easy control of the output pulse width in the Pulse Width Modulator of *Figure 30.*

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of *Figure 31* provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1, R2 network so that A1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A1 is:

$$V_{IN}1 = \frac{-2kTI_3}{qI_2} = \frac{2kTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_B1 = \frac{(R_1+R_2)\,V_{IN}1}{R_1}$$

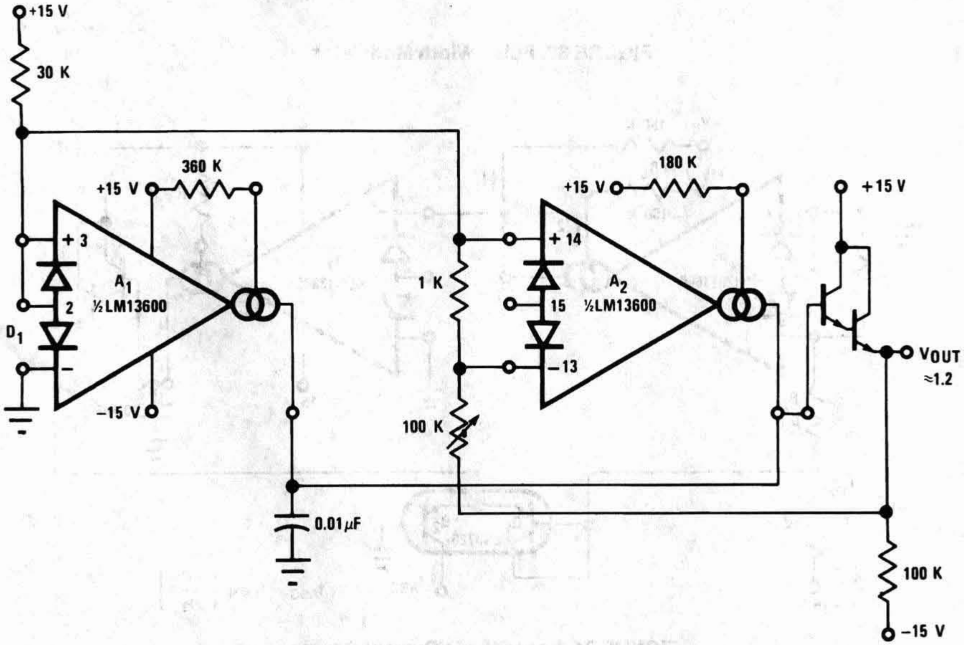
The ratio of the Q1 and Q2 collector currents is defined by:

$$V_B1 = \frac{kT}{q}\ln\frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q}\ln\frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 \exp\left[\frac{2(R_1+R_2)\,V_C}{R_1I_2R_C}\right]$$

This logarithmic current can be used to bias the circuit of *Figure 4* provide a temperature independent stereo attenuation characteristic.



+15 V
30 K
360 K
+15 V
+ 3
A1
½LM13600
2
D1
−15 V
1 K
180 K
+15 V
+ 14
A2
15
½LM13600
−13
100 K
+15 V
VOUT
≈1.2
0.01µF
100 K
−15 V

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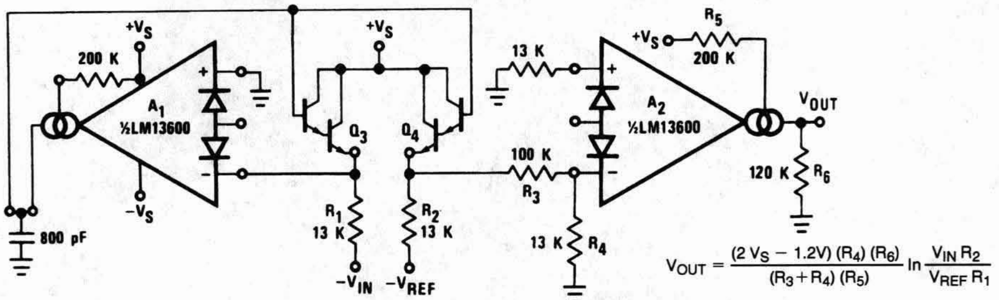
FIGURE 28. Delta VBE Reference



+VS
200 K
A1
½LM13600
−VS
800 pF
+VS
Q3
Q4
R1
13 K
R2
13 K
−VIN
−VREF
13 K
100 K
R3
13 K
R4
+VS
R5
200 K
A2
½LM13600
VOUT
120 K
R6

$$V_{OUT} = \frac{(2\,V_S - 1.2V)\,(R_4)\,(R_6)}{(R_3+R_4)\,(R_5)} \ln \frac{V_{IN}\,R_2}{V_{REF}\,R_1}$$

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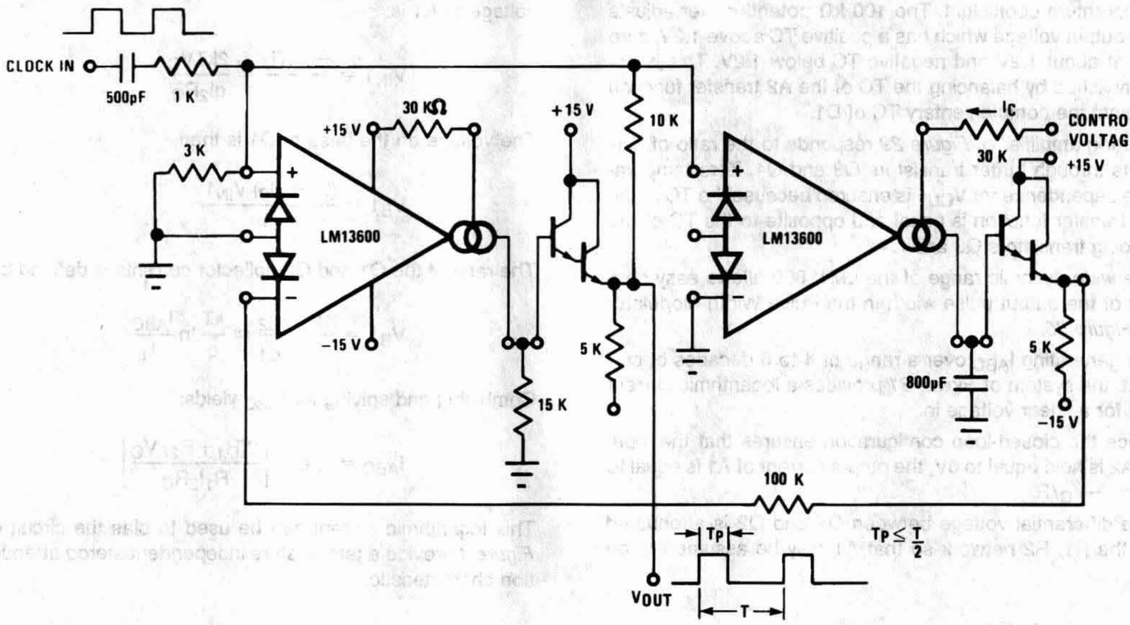
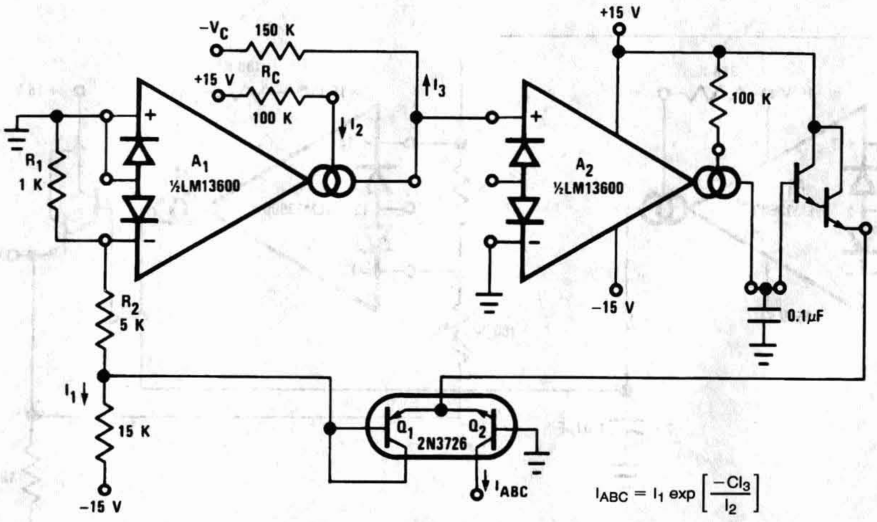
FIGURE 29. Log Amplifier

Additional Applications (Continued)


CLOCK IN
500pF
1 K
3 K
+15 V
30 KΩ
LM13600
−15 V
+15 V
10 K
15 K
5 K
100 K
Tp
Tp ≤ T/2
T
VOUT
CONTROL VOLTAGE
IC
30 K
+15 V
LM13600
800pF
5 K
−15 V

TL/H/7980–37

FIGURE 30. Pulse Width Modulator


−VC
150 K
+15 V
RC
100 K
I2
I3
R1
1 K
A1
½LM13600
R2
5 K
I1
15 K
−15 V
+15 V
100 K
A2
½LM13600
−15 V
0.1μF
Q1
Q2
2N3726
IABC

$$I_{ABC} = I_1 \exp\left[\frac{-CI_3}{I_2}\right]$$

TL/H/7980–38

FIGURE 31. Logarithmic Current Source

National Semiconductor

LM13700/LM13700A
Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

General Description

The LM13700 series consists of two current controlled transconductance amplifiers, each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. High impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers. The output buffers of the LM13700 differ from those of the LM13600 in that their input bias currents (and hence their output DC levels) are independent of I_{ABC}. This may result in performance superior to that of the LM13600 in audio applications.

Features

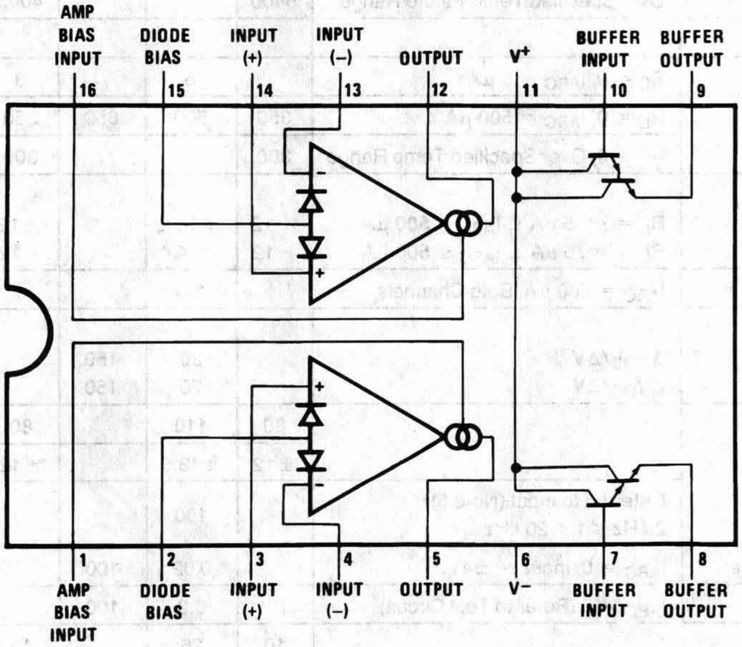
- g_m adjustable over 6 decades
- Excellent g_m linearity
- Excellent matching between amplifiers
- Linearizing diodes
- High impedance buffers
- High output signal-to-noise ratio

Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample-and-hold circuits

Connection Diagram

Dual In-Line and Small Outline Packages


AMP BIAS INPUT
DIODE BIAS
INPUT (+)
INPUT (−)
OUTPUT
V+
BUFFER INPUT
BUFFER OUTPUT
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
AMP BIAS INPUT
DIODE BIAS
INPUT (+)
INPUT (−)
OUTPUT
V−
BUFFER INPUT
BUFFER OUTPUT
+
−

TL/H/7981–2

Top View

Order Number LM13700M, LM13700N or LM13700AN
See NS Package Number M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 1)	
LM13700	36 V_{DC} or ±18V
LM13700A	44 V_{DC} or ±22V
Power Dissipation (Note 2) $T_A = 25°C$	
LM13700N, LM13700AN	570 mW
Differential Input Voltage	±5V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_{ABC})	2 mA
Output Short Circuit Duration	Continuous
Buffer Output Current (Note 3)	20 mA
Operating Temperature Range	
LM13700N, LM13700AN	0°C to +70°C
DC Input Voltage	$+V_S$ to $-V_S$
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM13700			LM13700A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{OS})			0.4	4		0.4	1	mV
	Over Specified Temperature Range						2	
	$I_{ABC} = 5\ \mu A$		0.3	4		0.3	1	
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 µA		0.5	5		0.5	2	mV
Input Offset Change	$5\ \mu A \le I_{ABC} \le 500\ \mu A$		0.1	3		0.1	1	mV
Input Offset Current			0.1	0.6		0.1	0.6	µA
Input Bias Current	Over Specified Temperature Range		0.4	5		0.4	5	µA
			1	8		1	7	
Forward Transconductance (g_m)		6700	9600	13000	7700	9600	12000	µmho
	Over Specified Temperature Range	5400			4000			
g_m Tracking			0.3			0.3		dB
Peak Output Current	$R_L = 0$, $I_{ABC} = 5\ \mu A$		5		3	5	7	µA
	$R_L = 0$, $I_{ABC} = 500\ \mu A$	350	500	650	350	500	650	
	$R_L = 0$, Over Specified Temp Range	300			300			
Peak Output Voltage								
Positive	$R_L = \infty$, $5\ \mu A \le I_{ABC} \le 500\ \mu A$	+12	+14.2		+12	+14.2		V
Negative	$R_L = \infty$, $5\ \mu A \le I_{ABC} \le 500\ \mu A$	−12	−14.4		−12	−14.4		V
Supply Current	$I_{ABC} = 500\ \mu A$, Both Channels		2.6			2.6		mA
V_{OS} Sensitivity								
Positive	$\Delta V_{OS}/\Delta V^+$		20	150		20	150	µV/V
Negative	$\Delta V_{OS}/\Delta V^-$		20	150		20	150	µV/V
CMRR		80	110		80	110		dB
Common Mode Range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 kHz		100			100		dB
Differential Input Current	$I_{ABC} = 0$, Input = ±4V		0.02	100		0.02	10	nA
Leakage Current	$I_{ABC} = 0$ (Refer to Test Circuit)		0.2	100		0.2	5	nA
Input Resistance		10	26		10	26		kΩ

Electrical Characteristics (Note 4) (Continued)

Parameter	Conditions	LM13700			LM13700A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μs
Buffer Input Current	(Note 5)		0.5	2		0.5	2	μA
Peak Buffer Output Voltage	(Note 5)	10			10			V

Note 1: For selections to a supply voltage above ±22V, contact factory.

Note 2: For operation at ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM13700N, 90°C/W; LM13700M, 110°C/W.

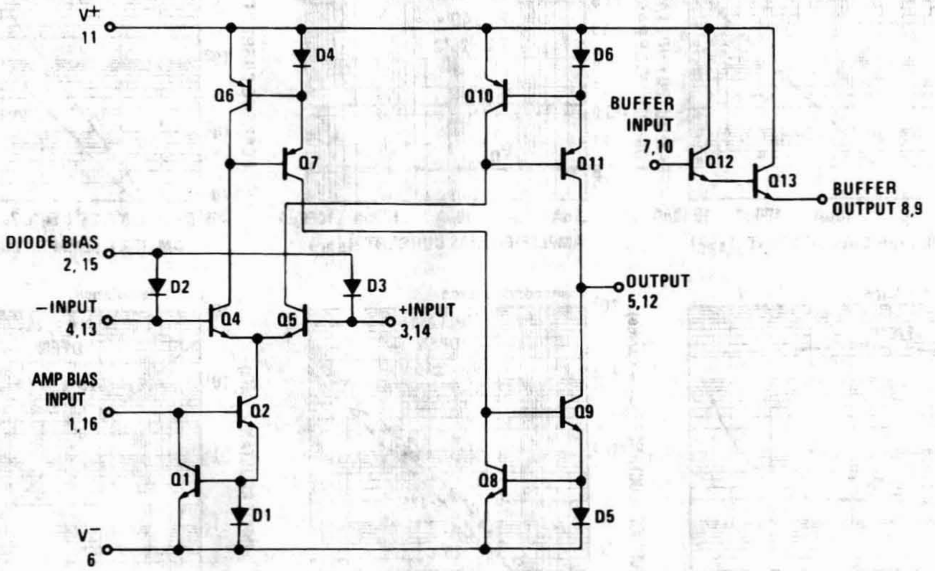
Note 3: Buffer output current should be limited so as to not exceed package dissipation.

Note 4: These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current (I_{ABC}) = 500 μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 5: These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500\ \mu A$, $R_{OUT} = 5\ k\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

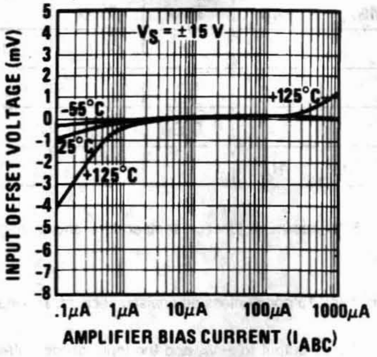
Schematic Diagram

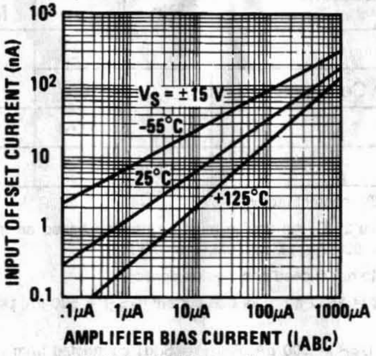
One Operational Transconductance Amplifier

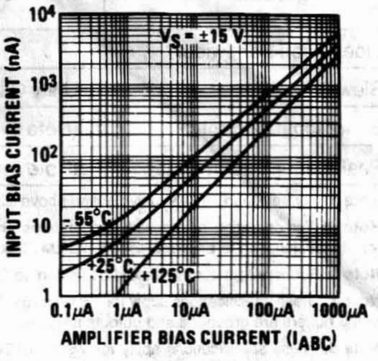

V+
11
D4
Q6
Q7
Q10
D6
BUFFER INPUT
7,10
Q11
Q12
Q13
BUFFER OUTPUT 8,9
DIODE BIAS
2, 15
D2
D3
OUTPUT
5,12
−INPUT
4,13
Q4
Q5
+INPUT
3,14
AMP BIAS INPUT
1,16
Q2
Q9
Q1
Q8
D1
D5
V−
6

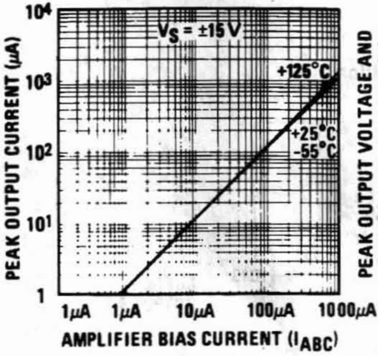
TL/H/7981-1

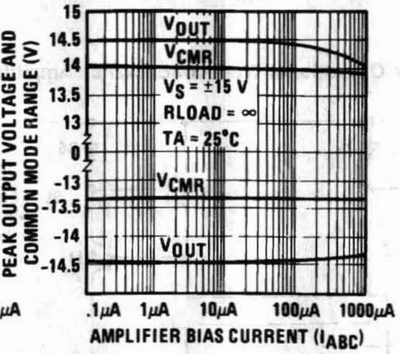
Typical Performance Characteristics

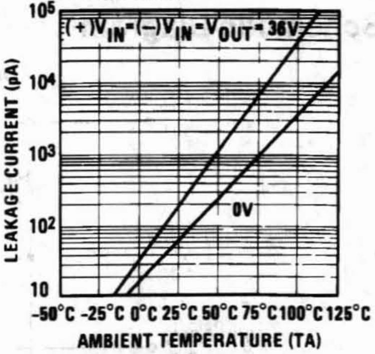

Input Offset Voltage

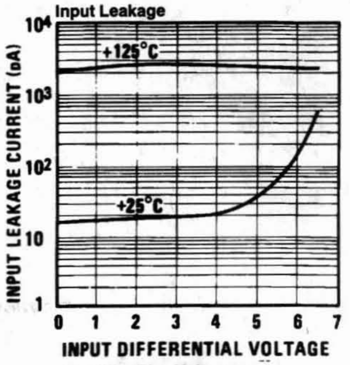

Input Offset Current

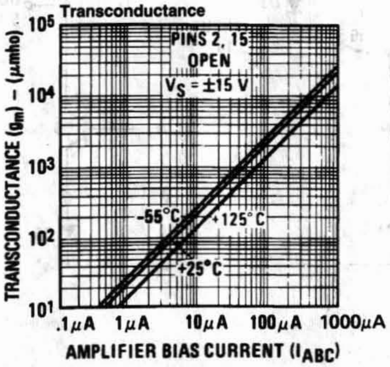

Input Bias Current

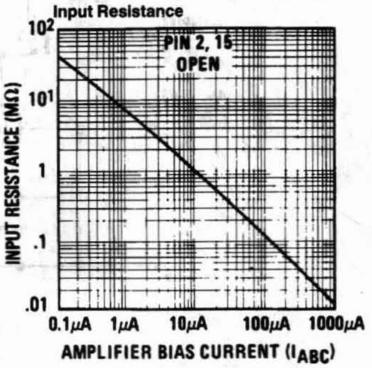

Peak Output Current

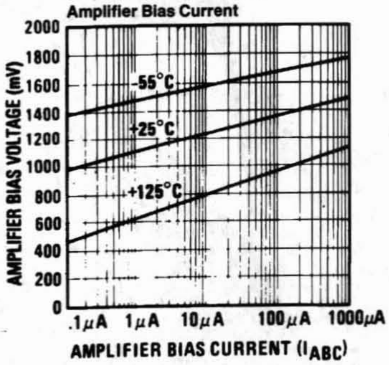

Peak Output Voltage and Common Mode Range

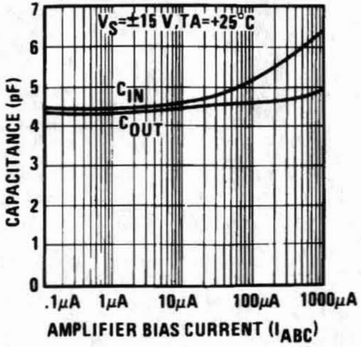

Leakage Current

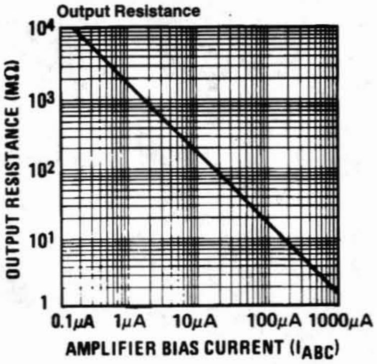

Input Leakage


Transconductance


Input Resistance

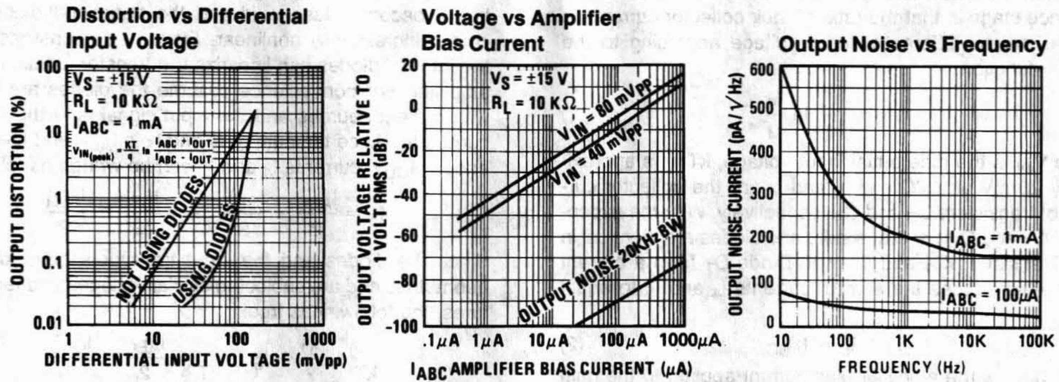

Amplifier Bias Voltage vs Amplifier Bias Current


Input and Output Capacitance


Output Resistance

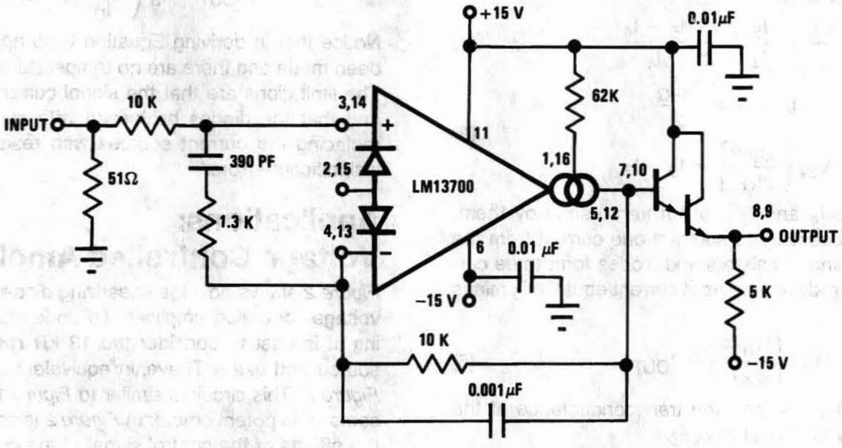
TL/H/7981–3

Typical Performance Characteristics (Continued)



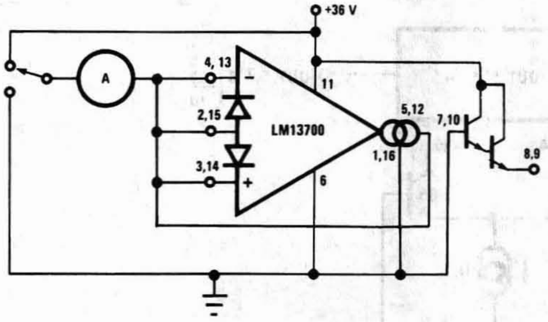
TL/H/7981–4

Unity Gain Follower


+15 V
0.01μF
62K
10 K
3,14
INPUT
390 PF
2,15
51Ω
1.3 K
4,13
11
LM13700
1,16
7,10
5,12
8,9
OUTPUT
6
0.01 μF
−15 V
5 K
−15 V
10 K
0.001μF

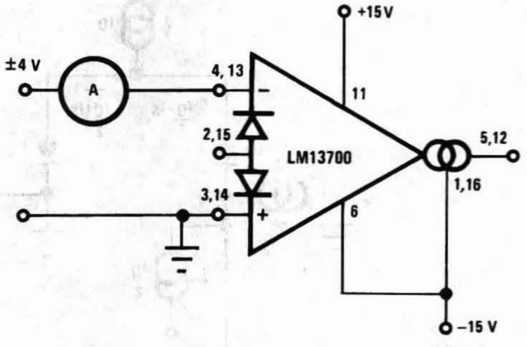
TL/H/7981–5

Leakage Current Test Circuit


+36 V
A
4, 13
11
2,15
LM13700
5,12
7,10
3,14
1,16
8,9
6

TL/H/7981–6

Differential Input Current Test Circuit


+15V
±4 V
A
4, 13
11
2,15
LM13700
5,12
1,16
3,14
6
−15 V

TL/H/7981–7

Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

where V_{IN} is the differential input voltage, kT/q is approximately 26 mV at 25°C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC};

$$I_4 + I_5 = I_{ABC} \quad (2)$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN}\left[\frac{I_{ABC}q}{2kT}\right] = I_5 - I_4 \quad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN}\left[\frac{I_{ABC}q}{2kT}\right] = I_{OUT} \quad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC}.

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. *Figure 1* demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S. Since the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \; I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

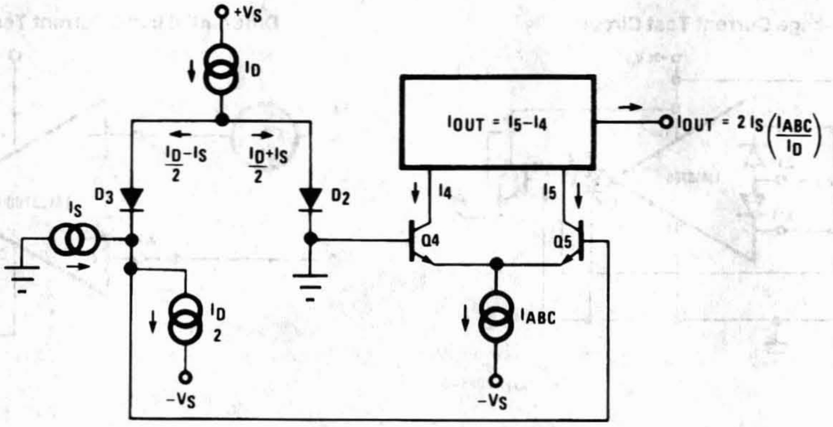
$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}}$$

$$\therefore I_{OUT} = I_S \left(\frac{2I_{ABC}}{I_D}\right) \text{ for } |I_S| < \frac{I_D}{2} \quad (6)$$

Notice that in deriving Equation 6 no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

Applications: Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in *Figure 3*. This circuit is similar to *Figure 1* and operates the same. The potentiometer in *Figure 2* is adjusted to minimize the effects of the control signal at the output.



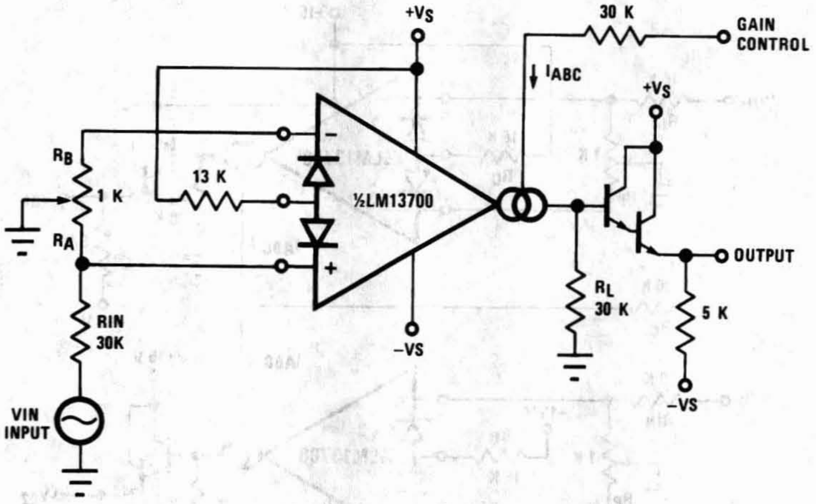
TL/H/7981-8

FIGURE 1. Linearizing Diodes

Applications:
Voltage Controlled Amplifiers (Continued)

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} *(Figure 2)* until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

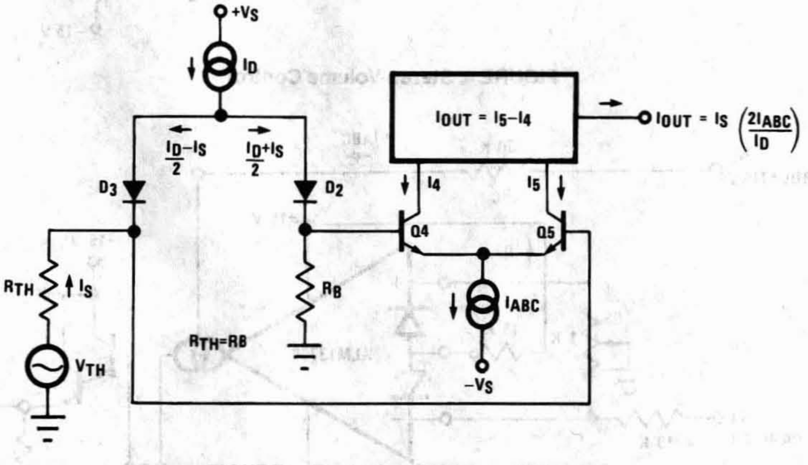
Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.



+VS
30 K
GAIN CONTROL
IABC
+VS
RB
1 K
13 K
½LM13700
RA
OUTPUT
RL
30 K
5 K
RIN
30K
-VS
-VS
VIN
INPUT

TL/H/7981–9

FIGURE 2. Voltage Controlled Amplifier



+VS
ID
IOUT = I5–I4
IOUT = IS (2IABC / ID)
ID–IS / 2
ID+IS / 2
D3
D2
I4
I5
Q4
Q5
RTH
IS
RB
IABC
RTH=RB
VTH
-VS

TL/H/7981–10

FIGURE 3. Equivalent VCA Input Circuit

Stereo Volume Control

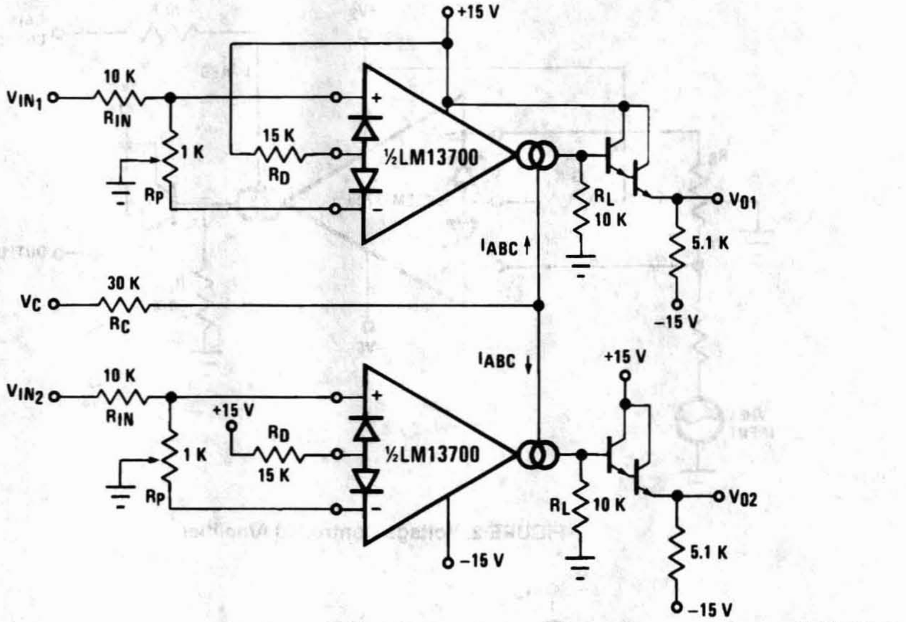
The circuit of *Figure 4* uses the excellent matching of the two LM13700 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. R_P is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for *Figure 2* as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in *Figure 5*, where:

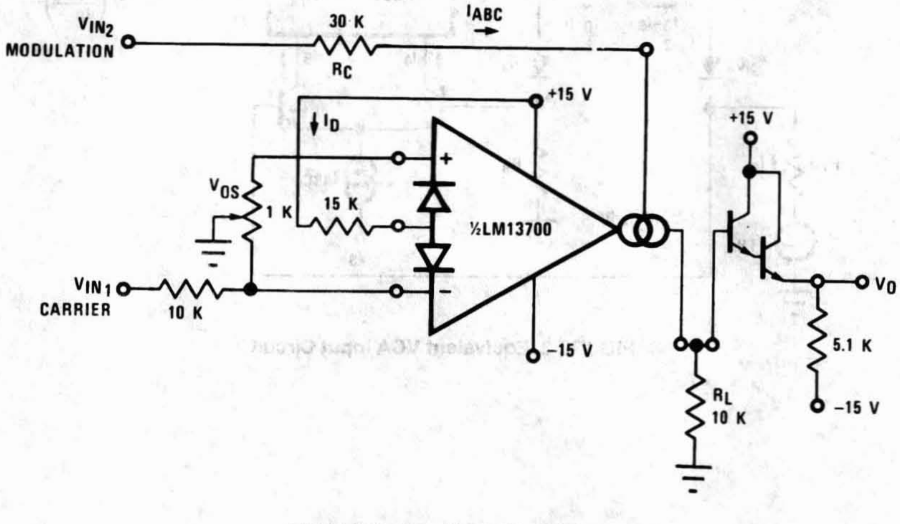
$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^- + 1.4V)}{R_C}$$

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C / 2(V^- + 1.4V)$ into I_O. The circuit of *Figure 6* adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O.


+15 V
10 K
VIN1
RIN
1 K
RP
15 K
RD
+
−
½LM13700
RL
10 K
VO1
5.1 K
IABC
−15 V
30 K
VC
RC
IABC
+15 V
10 K
VIN2
RIN
+15 V
RD
1 K
15 K
RP
½LM13700
RL
10 K
VO2
5.1 K
−15 V
−15 V

TL/H/7981–11

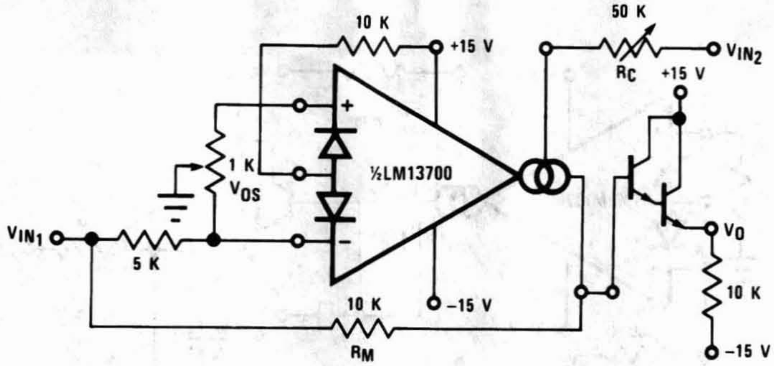
FIGURE 4. Stereo Volume Control


VIN2
MODULATION
30 K
RC
IABC
+15 V
ID
VOS
1 K
15 K
+
−
½LM13700
VIN1
CARRIER
10 K
−15 V
+15 V
VO
5.1 K
−15 V
RL
10 K

TL/H/7981–12

FIGURE 5. Amplitude Modulator

Stereo Volume Control (Continued)



TL/H/7981–13

FIGURE 6. Four-Quadrant Multiplier

Noting that the gain of the LM13700 amplifier of *Figure 3* may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC}, *Figure 7* shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

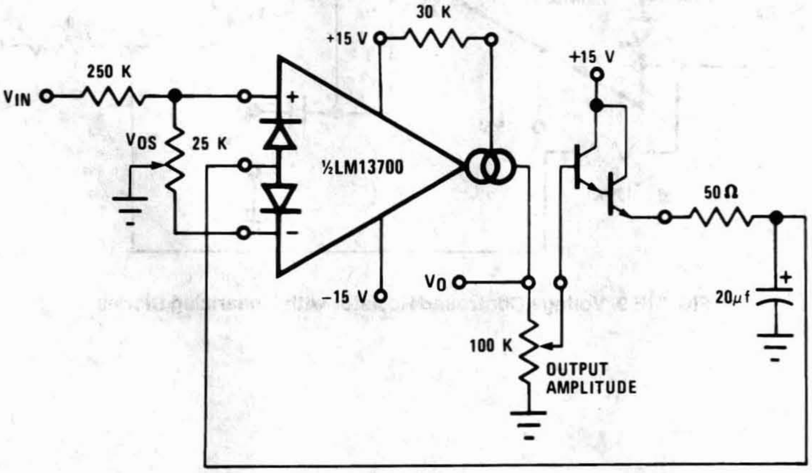
Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in *Figure 8*. A signal voltage applied at R_X generates a V_{IN} to the LM13700 which is then multiplied by the g_m of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2 I_{ABC}$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13700 input.

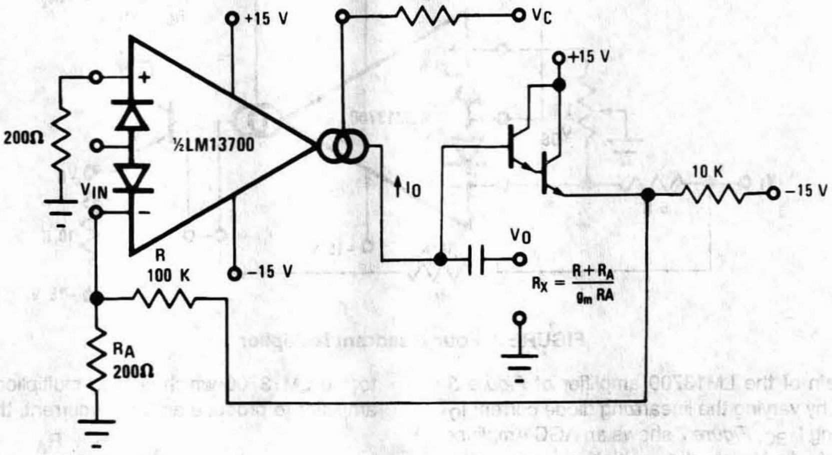
Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in *Figure 10*, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13700.



TL/H/7981–14

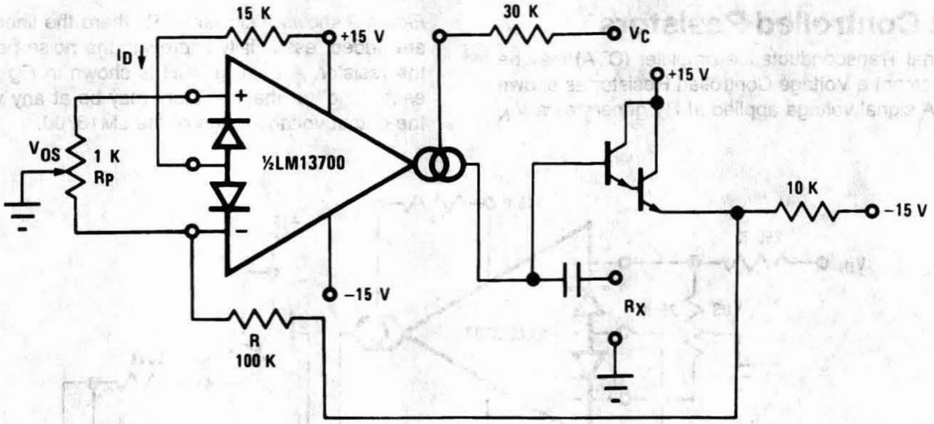
FIGURE 7. AGC Amplifier

Voltage Controlled Resistors (Continued)


+15 V
30 K
VC
+15 V
200Ω
½LM13700
+
−
VIN
IO
10 K
−15 V
R
100 K
−15 V
VO
$R_X = \frac{R+R_A}{g_m R_A}$
RA
200Ω

TL/H/7981–15

FIGURE 8. Voltage Controlled Resistor, Single-Ended


15 K
+15 V
30 K
VC
ID
+15 V
+
VOS
1 K
RP
½LM13700
−
10 K
−15 V
−15 V
RX
R
100 K

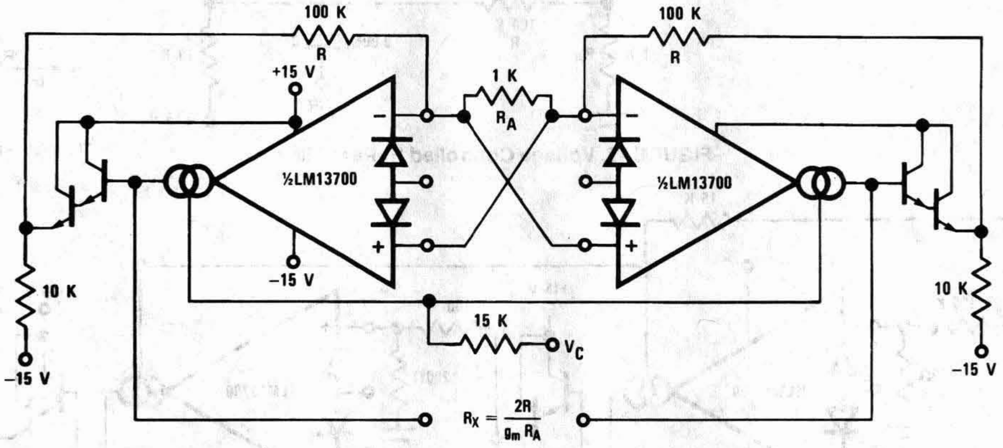
TL/H/7981–16

FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes

Voltage Controlled Filters

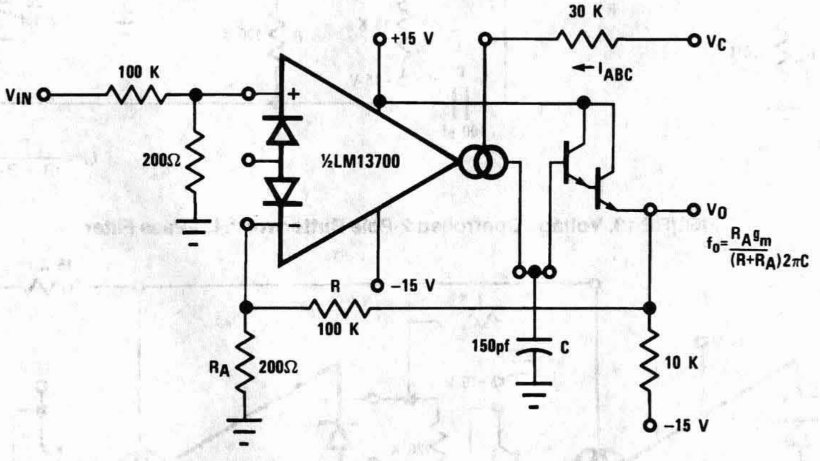
OTA's are extremely useful for implementing voltage controlled filters, with the LM13700 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of *Figure 11* performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a −3 dB point defined by the given equation, where g_m is again 19.2 × I_{ABC} at room temperature. *Figure 12* shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of *Figure 13* and the state variable filter of *Figure 14*. Due to the excellent g_m tracking of the two amplifiers, these filters perform well over several decades of frequency.


100 K
R
+15 V
1 K
R_A
½LM13700
−15 V
10 K
−15 V
100 K
R
½LM13700
10 K
−15 V
15 K
V_C
$R_X = \frac{2R}{g_m R_A}$

TL/H/7981–17

FIGURE 10. Floating Voltage Controlled Resistor


V_IN
100 K
200Ω
+15 V
½LM13700
−15 V
30 K
V_C
I_ABC
V_O
$f_0 = \frac{R_A g_m}{(R+R_A)2\pi C}$
R
100 K
R_A
200Ω
150pf
C
10 K
−15 V

TL/H/7981–18

FIGURE 11. Voltage Controlled Low-Pass Filter

Voltage Controlled Filters (Continued)

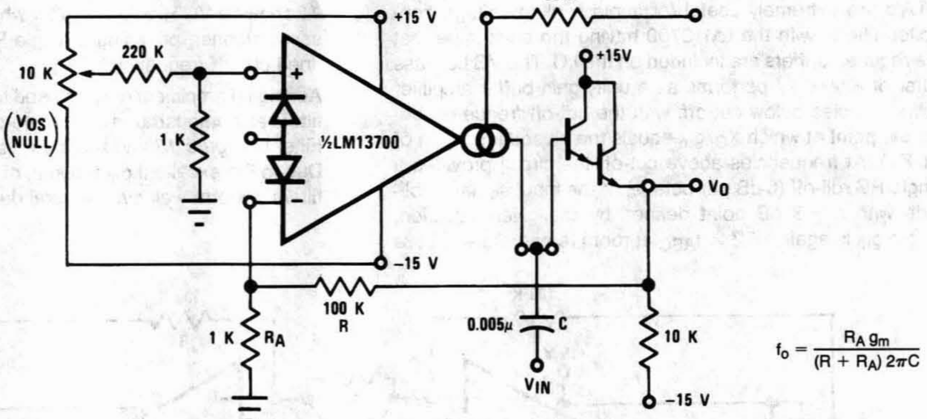

+15 V
30 K
220 K
10 K
+
(VOS NULL)
1 K
½LM13700
+15V
VO
–15 V
100 K
R
1 K
RA
0.005µ
C
VIN
10 K
–15 V
$f_o = \frac{R_A g_m}{(R + R_A) 2\pi C}$

FIGURE 12. Voltage Controlled Hi-Pass Filter

TL/H/7981-19

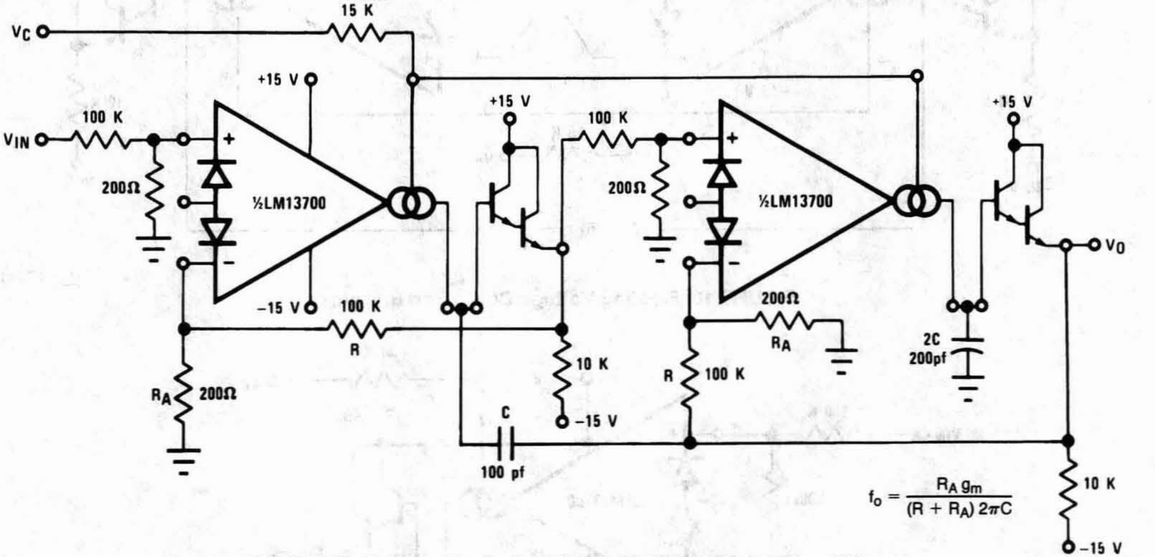

VC
15 K
+15 V
VIN
100 K
200Ω
½LM13700
–15 V
100 K
R
RA
200Ω
+15 V
10 K
–15 V
C
100 pf
100 K
200Ω
½LM13700
200Ω
RA
R
100 K
+15 V
VO
2C
200pf
10 K
–15 V
$f_o = \frac{R_A g_m}{(R + R_A) 2\pi C}$

FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter

TL/H/7981-20

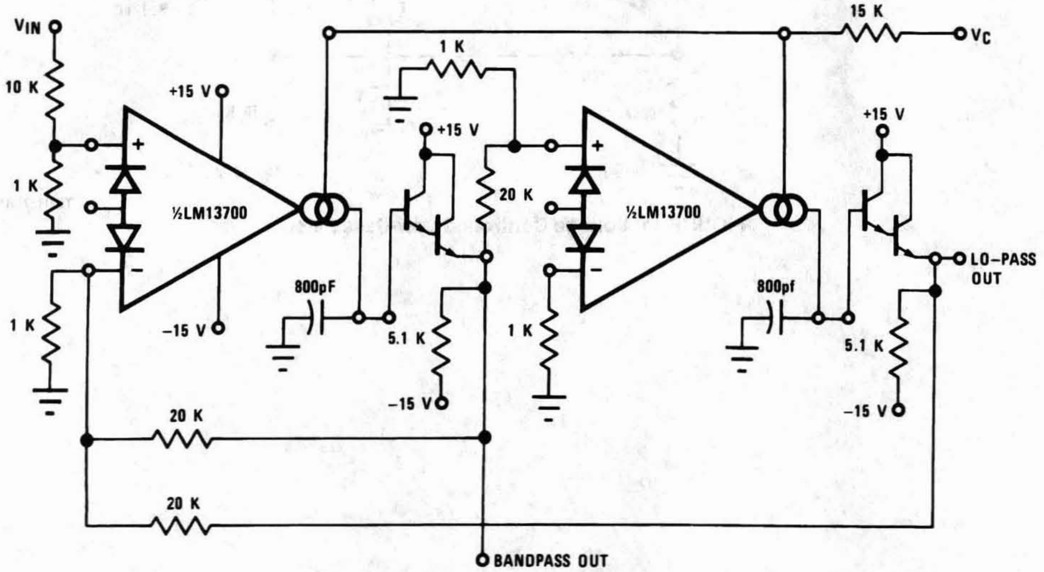

VIN
10 K
1 K
1 K
+15 V
½LM13700
–15 V
800pF
1 K
+15 V
20 K
5.1 K
–15 V
15 K
VC
1 K
½LM13700
800pf
+15 V
5.1 K
–15 V
LO-PASS OUT
20 K
20 K
BANDPASS OUT

FIGURE 14. Voltage Controlled State Variable Filter

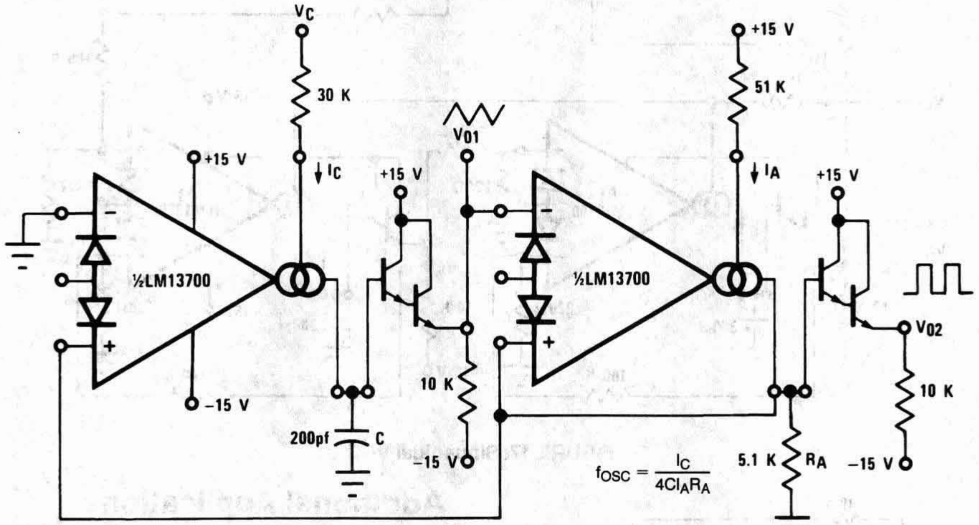
TL/H/7981-21

Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of *Figure 15* is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13700. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of *Figure 16*. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

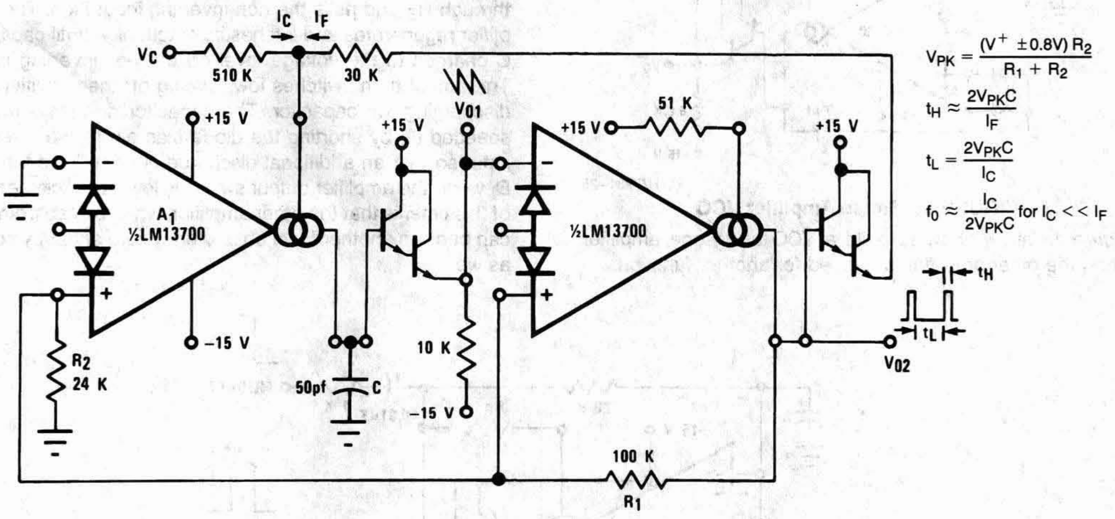
The VC Lo-Pass Filter of *Figure 11* may be used to produce a high-quality sinusoidal VCO. The circuit of *Figure 16* employs two LM13700 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.


VC
30 K
IC
+15 V
+15 V
VO1
½LM13700
−15 V
200pf
C
10 K
−15 V
+15 V
51 K
IA
+15 V
½LM13700
VO2
10 K
5.1 K
RA
−15 V

$$f_{OSC} = \frac{I_C}{4CI_AR_A}$$

FIGURE 15. Triangular/Square-Wave VCO

TL/H/7981–22


IC
IF
VC
510 K
30 K
VO1
+15 V
+15 V
A1
½LM13700
−15 V
R2
24 K
50pf
C
10 K
−15 V
51 K
+15 V
+15 V
½LM13700
tH
tL
VO2
100 K
R1

$$V_{PK} = \frac{(V^+ \pm 0.8V)\,R_2}{R_1 + R_2}$$

$$t_H \approx \frac{2V_{PK}C}{I_F}$$

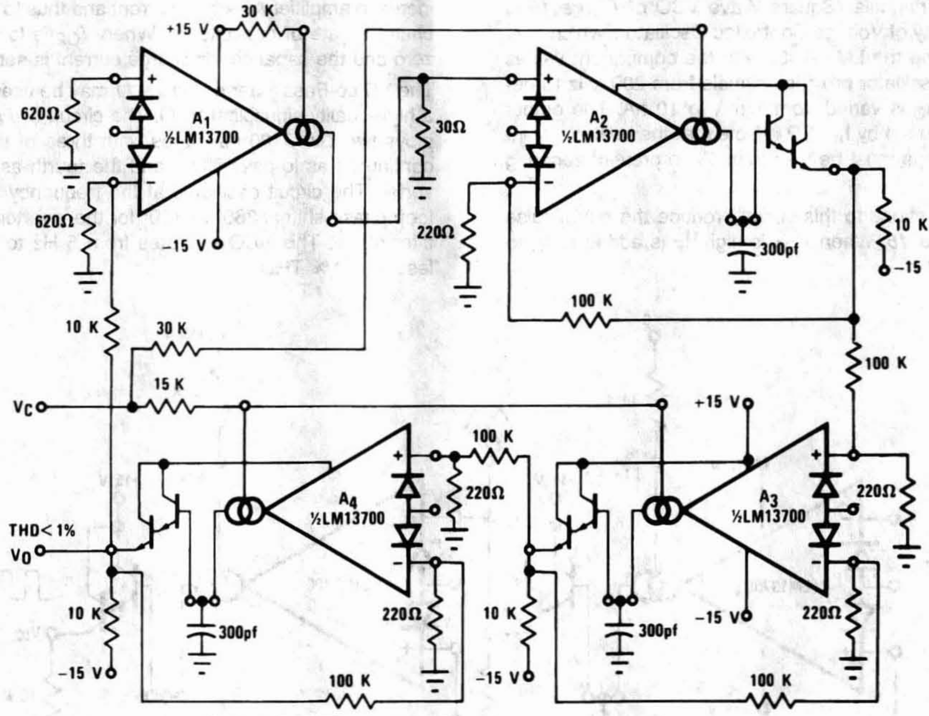
$$t_L = \frac{2V_{PK}C}{I_C}$$

$$f_0 \approx \frac{I_C}{2V_{PK}C} \text{ for } I_C << I_F$$

FIGURE 16. Ramp/Pulse VCO

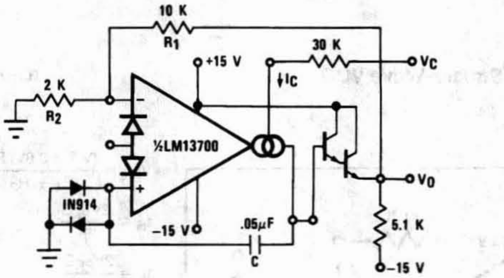
TL/H/7981–23

Voltage Controlled Oscillators (Continued)


+15 V
30 K
620Ω
A1
½LM13700
620Ω
-15 V
30Ω
220Ω
A2
½LM13700
10 K
300pf
-15 V
100 K
10 K
30 K
15 K
VC
100 K
+15 V
THD<1%
VO
100 K
A4
½LM13700
220Ω
300pf
220Ω
10 K
-15 V
100 K
A3
½LM13700
220Ω
10 K
300pf
-15 V
220Ω
-15 V
100 K

TL/H/7981-24

FIGURE 17. Sinusoidal VCO


10 K
R1
+15 V
30 K
VC
IC
2 K
R2
½LM13700
VO
IN914
-15 V
.05μF
C
5.1 K
-15 V

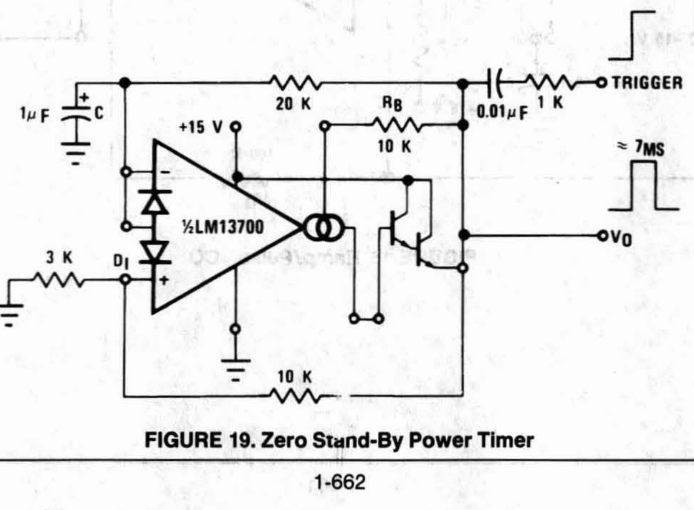
TL/H/7981-25

FIGURE 18. Single Amplifier VCO

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_I when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.


1μF
C
20 K
0.01μF
1 K
TRIGGER
RB
10 K
+15 V
≈ 7MS
½LM13700
VO
3 K
DI
10 K

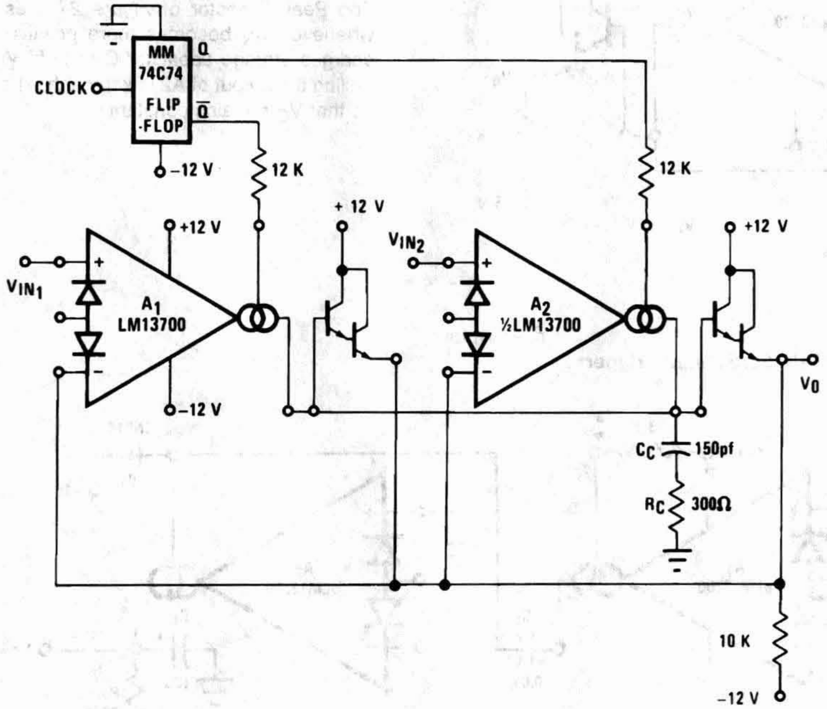
TL/H/7981-26

FIGURE 19. Zero Stand-By Power Timer

Additional Applications (Continued)

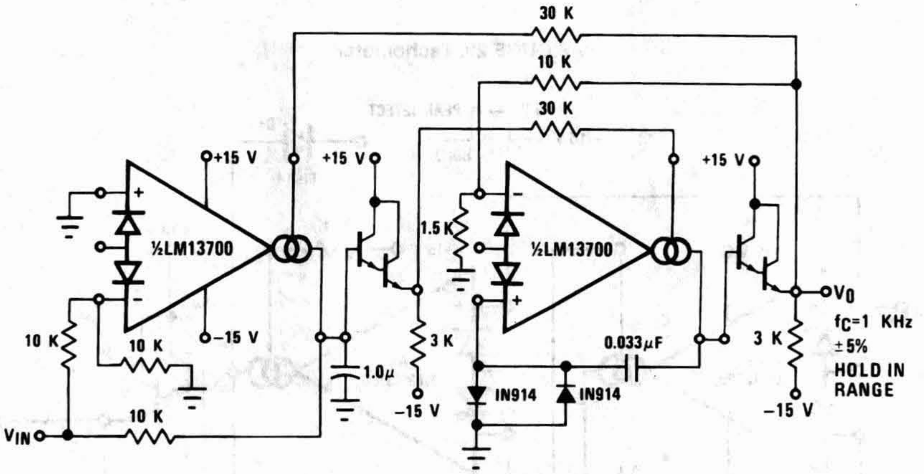
The operation of the multiplexer of *Figure 20* is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13700 slew rate into 150 pF when the ($V_{IN1}-V_{IN2}$) differential is at its maximum allowable value of 5V.

The Phase-Locked Loop of *Figure 21* uses the four-quadrant multiplier of *Figure 6* and the VCO of *Figure 18* to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.


MM
74C74
FLIP
-FLOP
Q
Q̄
CLOCK
−12 V
12 K
12 K
+12 V
+ 12 V
+12 V
V_{IN1}
A1
LM13700
−12 V
V_{IN2}
A2
½LM13700
V_O
C_C
150pf
R_C
300Ω
10 K
−12 V

TL/H/7981-27

FIGURE 20. Multiplexer

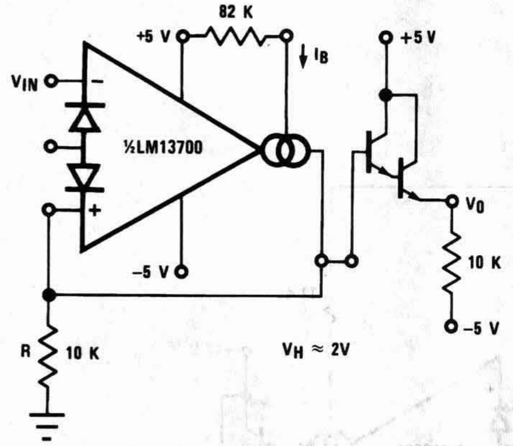

30 K
10 K
30 K
+15 V
+15 V
+15 V
½LM13700
½LM13700
1.5 K
−15 V
10 K
10 K
10 K
V_{IN}
1.0μ
3 K
−15 V
0.033μF
IN914
IN914
3 K
−15 V
V_O
f_C=1 KHz
±5%
HOLD IN
RANGE

TL/H/7981-28

FIGURE 21. Phase Lock Loop

Additional Applications (Continued)

The Schmitt Trigger of *Figure 22* uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

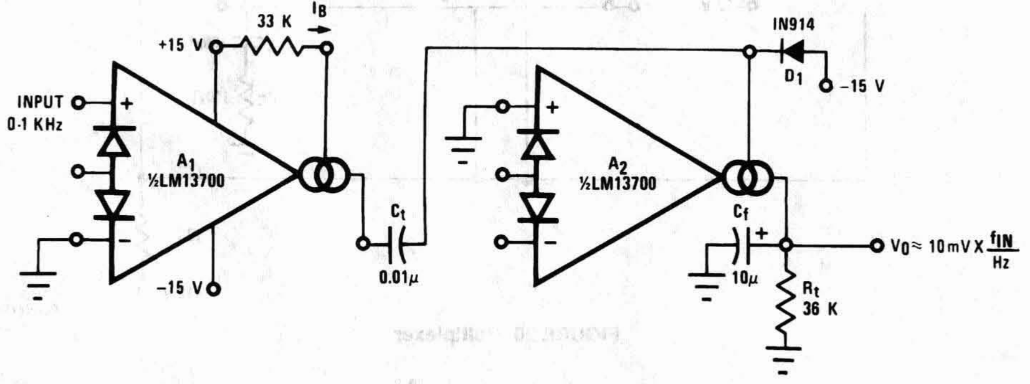

82 K
+5 V
I_B
+5 V
V_{IN}
½LM13700
V_O
10 K
−5 V
−5 V
R
10 K
$V_H \approx 2V$

TL/H/7981–29

FIGURE 22. Schmitt Trigger

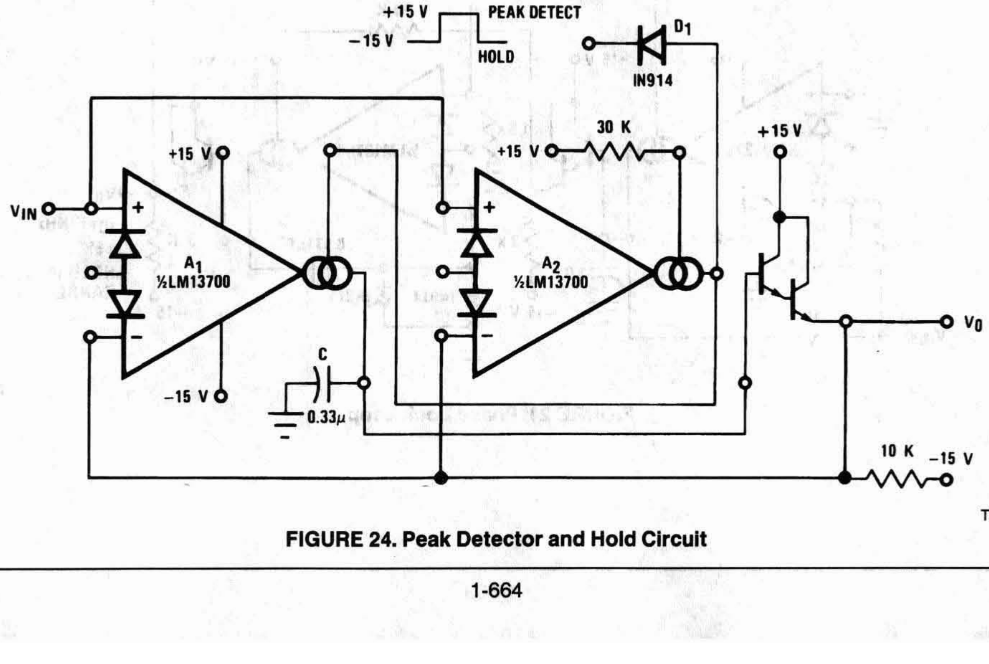
Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\ C_t$ is sourced into C_f and R_t. This once per cycle charge is then balanced by the current of V_O/R_t. The maximum F_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13700. D1 is added to provide a discharge path for C_t when A1 switches low.

The Peak Detector of *Figure 24* uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to V_{IN} PK. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.


33 K
I_B
+15 V
INPUT
0-1 KHz
A_1
½LM13700
−15 V
C_t
0.01µ
IN914
D_1
−15 V
A_2
½LM13700
C_f
10µ
$V_O \approx 10mV \times \frac{f_{IN}}{Hz}$
R_t
36 K

TL/H/7981–30

FIGURE 23. Tachometer


+15 V
−15 V
PEAK DETECT
HOLD
D_1
IN914
30 K
+15 V
+15 V
+15 V
V_{IN}
A_1
½LM13700
A_2
½LM13700
−15 V
C
0.33µ
V_O
10 K
−15 V

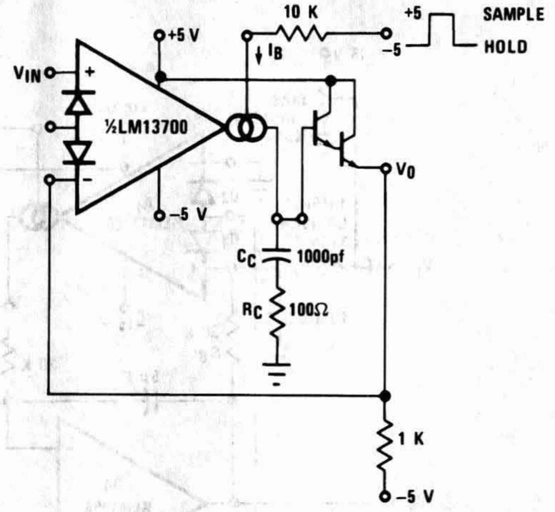
TL/H/7981–31

FIGURE 24. Peak Detector and Hold Circuit

Additional Applications (Continued)

The Ramp-and-Hold of *Figure 26* sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1V/ms for the component values shown.

The true-RMS converter of *Figure 27* is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.



+5 V
10 K
+5
SAMPLE
−5
HOLD
I_B
V_IN
½LM13700
V_O
−5 V
C_C
1000pf
R_C
100Ω
1 K
−5 V

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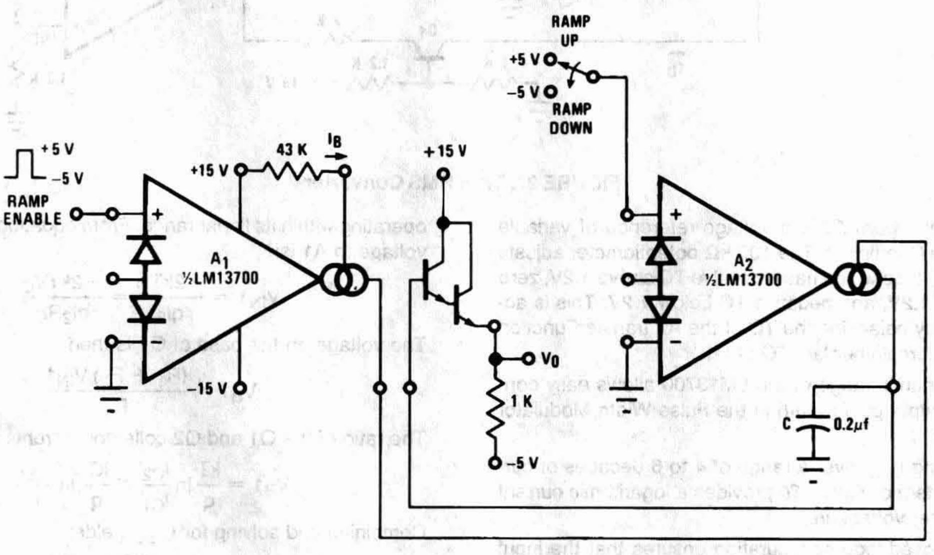
FIGURE 25. Sample-Hold Circuit



RAMP
UP
+5 V
−5 V
RAMP
DOWN
+5 V
−5 V
RAMP
ENABLE
+15 V
43 K
I_B
+15 V
A_1
½LM13700
−15 V
V_O
1 K
−5 V
A_2
½LM13700
C
0.2μf

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FIGURE 26. Ramp and Hold

Additional Applications (Continued)

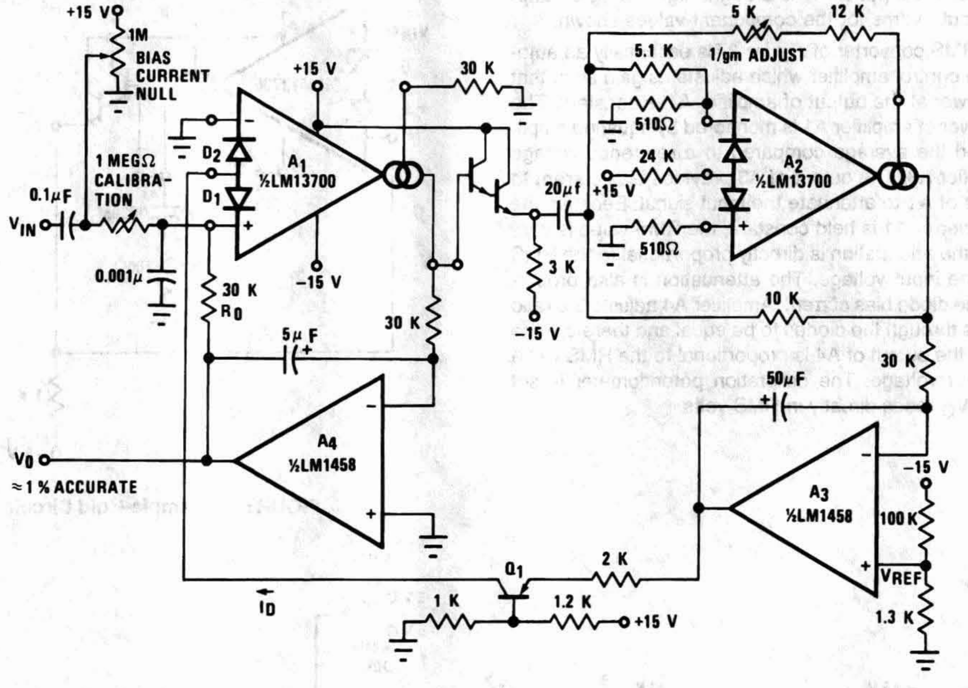
+15 V
1M
BIAS CURRENT NULL
+15 V
30 K
1 MEGΩ CALIBRATION
D2
D1
A1
½LM13700
0.1μF
VIN
0.001μ
30 K
R0
-15 V
5μ F
30 K
A4
½LM1458
V0
≈1 % ACCURATE
5 K
12 K
5.1 K
1/gm ADJUST
510Ω
24 K
A2
½LM13700
20μf
+15 V
510Ω
3 K
-15 V
10 K
30 K
50μF
-15 V
A3
½LM1458
100 K
VREF
1.3 K
Q1
2 K
1 K
1.2 K
+15 V
ID

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FIGURE 27. True RMS Converter

The circuit of *Figure 28* is a voltage reference of variable Temperature Coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V, and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The wide dynamic range of the LM13700 allows easy control of the output pulse width in the Pulse Width Modulator of *Figure 29*.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of *Figure 30* provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1,R2 network so that A1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A1 is:

$$V_{IN}1 = \frac{-2kTI_3}{qI_2} = \frac{-2kTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_B1 = \frac{(R_1 + R_2)\,V_{IN}1}{R_1}$$

The ratio of the Q1 and Q2 collector currents is defined by:

$$V_B1 = \frac{kT}{q} \ln \frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q} \ln \frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 \exp \frac{2(R_1 + R_2)\,V_C}{R_1\,I_2\,R_C}$$

This logarithmic current can be used to bias the circuit of *Figure 4* to provide temperature independent stereo attenuation characteristic.

Additional Applications (Continued)

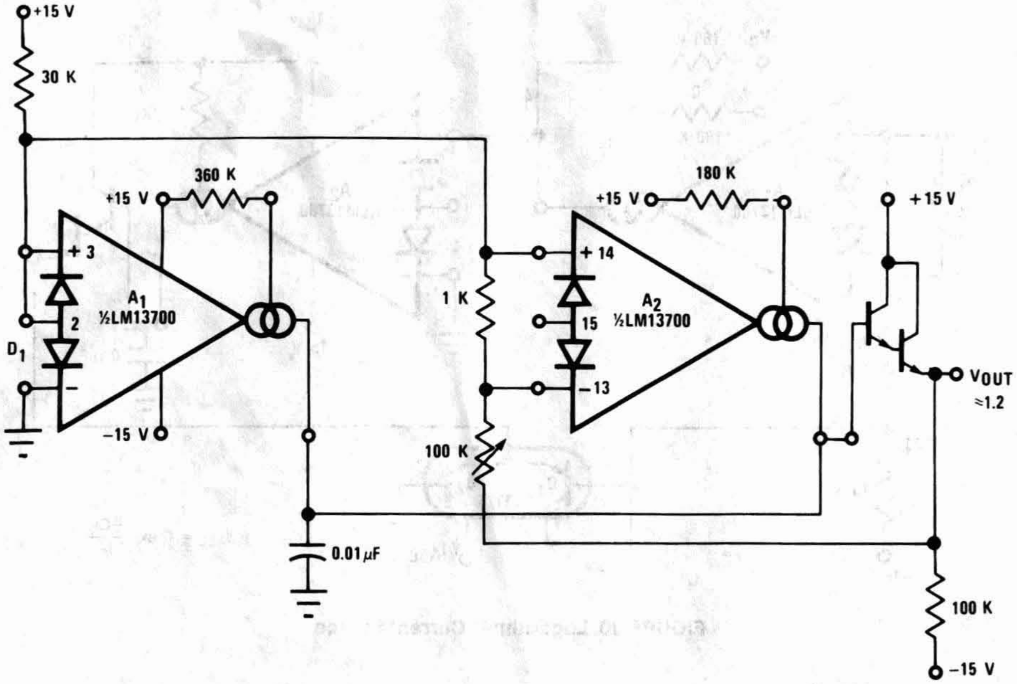
+15 V
30 K
360 K
+15 V
+ 3
2
A1
½LM13700
D1
−
−15 V
1 K
100 K
0.01 μF
180 K
+15 V
+ 14
15
A2
½LM13700
− 13
+15 V
VOUT
≈1.2
100 K
−15 V

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FIGURE 28. Delta VBE Reference

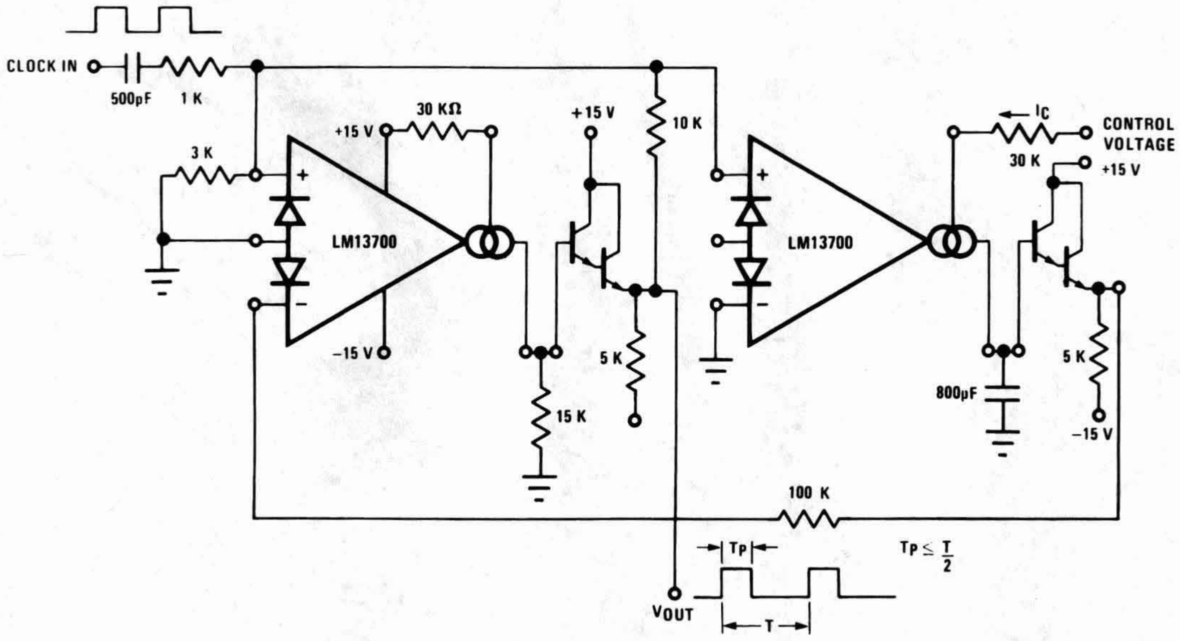
CLOCK IN
500pF
1 K
3 K
30 KΩ
+15 V
+
−
LM13700
−15 V
+15 V
10 K
15 K
5 K
+
−
LM13700
IC
CONTROL VOLTAGE
30 K
+15 V
800pF
5 K
−15 V
100 K
Tp
Tp ≤ T/2
VOUT
T

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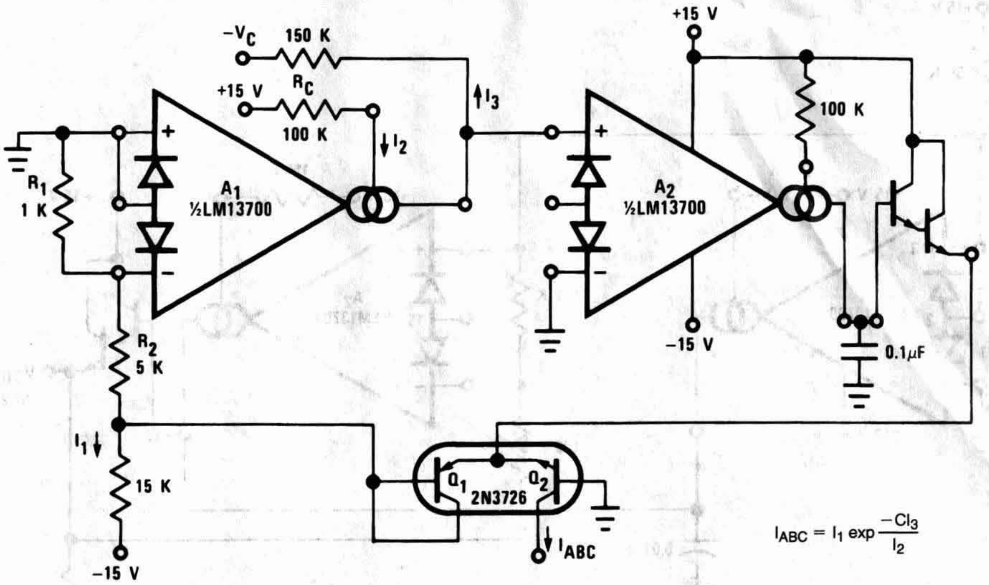
FIGURE 29. Pulse Width Modulator

Additional Applications (Continued)



$-V_C$
150 K
+15 V
R_C
100 K
I_2
I_3
R_1
1 K
A_1
½LM13700
A_2
½LM13700
+15 V
100 K
−15 V
0.1μF
R_2
5 K
I_1
15 K
−15 V
Q_1
Q_2
2N3726
I_{ABC}

$$I_{ABC} = I_1 \exp \frac{-CI_3}{I_2}$$

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FIGURE 30. Logarithmic Current Source

National Semiconductor

LMC660
CMOS Quad Operational Amplifier

General Description

The LMC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC662 datasheet for a dual CMOS operational amplifier with these same features.

Features

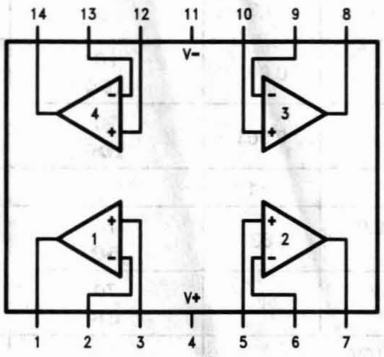
- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 2 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- I_{SS} = 375 μA/amplifier; independent of V^+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Available in extended temperature range (−40°C to +125°C); ideal for automotive applications
- Available to Standard Military Drawing specification

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-Hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram

14-Pin DIP/SO



TL/H/8767–1

Ordering Information

Package	Temperature Range				NSC Drawing	Transport Media
	Military −55°C to +125°C	Extended −40°C +125°C	Industrial −40°C to +85°C	Commercial 0°C to +70°C		
14-Pin Ceramic DIP	LMC660AMJ/883				J14A	Rail
14-Pin Small Outline		LMC660EM	LMC660AIM	LMC660CM	M14A	Rail Tape and Reel
14-Pin Molded DIP		LMC660EN	LMC660AIN	LMC660CN	N14A	Rail
14-Pin Side Brazed Ceramic DIP	LMC660AMD				D14E	Rail

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Supply Voltage	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 1)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Voltage at Input/Output Pins	$(V^+) + 0.3V, (V^-) - 0.3V$
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 2)
Junction Temperature	150°C
ESD tolerance (Note 8)	1000V

Operating Ratings

Temperature Range	
LMC660AMJ/883, LMC660AMD	$-55°C \le T_J \le +125°C$
LMC660AI	$-40°C \le T_J \le +85°C$
LMC660C	$0°C \le T_J \le +70°C$
LMC660E	$-40°C \le T_J \le +125°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}) (Note 11)	
14-Pin Ceramic DIP	90°C/W
14-Pin Molded DIP	85°C/W
14-Pin SO	115°C/W
14-Pin Side Brazed Ceramic DIP	90°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AMD LMC660AMJ/883	LMC660AI	LMC660C	LMC660E	Units
			Limit (Notes 4, 9)	Limit (Note 4)	Limit (Note 4)	Limit (Note 4)	
Input Offset Voltage		1	3 **3.5**	3 **3.3**	6 **6.3**	6 **6.5**	mV max
Input Offset Voltage Average Drift		1.3					μV/°C
Input Bias Current		0.002	20 **100**	**4**	**2**	**60**	pA max
Input Offset Current		0.001	20 **100**	**2**	**1**	**60**	pA max
Input Resistance		>1					TeraΩ
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70 **68**	70 **68**	63 **62**	63 **60**	dB min
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70 **68**	70 **68**	63 **62**	63 **60**	dB min
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84 **82**	84 **83**	74 **73**	74 **70**	dB min
Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	−0.1 **0**	V max
		$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.4$**	$V^+ - 2.3$ **$V^+ - 2.6$**	V min
Large Signal Voltage Gain	$R_L = 2 k\Omega$ (Note 5) Sourcing	2000	400 **300**	440 **400**	300 **200**	200 **100**	V/mV min
	Sinking	500	180 **70**	180 **120**	90 **80**	90 **40**	V/mV min
	$R_L = 600\Omega$ (Note 5) Sourcing	1000	200 **150**	220 **200**	150 **100**	100 **75**	V/mV min
	Sinking	250	100 **35**	100 **60**	50 **40**	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AMD LMC660AMJ/883	LMC660AI	LMC660C	LMC660E	Units
			Limit (Notes 4, 9)	Limit (Note 4)	Limit (Note 4)	Limit (Note 4)	
Output Swing	$V^+ = 5V$ $R_L = 2\ k\Omega$ to $V^+/2$	4.87	4.82 **4.77**	4.82 **4.79**	4.78 **4.76**	4.78 **4.70**	V min
		0.10	0.15 **0.19**	0.15 **0.17**	0.19 **0.21**	0.19 **0.25**	V max
	$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$	4.61	4.41 **4.24**	4.41 **4.31**	4.27 **4.21**	4.27 **4.10**	V min
		0.30	0.50 **0.63**	0.50 **0.56**	0.63 **0.69**	0.63 **0.75**	V max
	$V^+ = 15V$ $R_L = 2\ k\Omega$ to $V^+/2$	14.63	14.50 **14.40**	14.50 **14.44**	14.37 **14.32**	14.37 **14.25**	V min
		0.26	0.35 **0.43**	0.35 **0.40**	0.44 **0.48**	0.44 **0.55**	V max
	$V^+ = 15V$ $R_L = 600\Omega$ to $V^+/2$	13.90	13.35 **13.02**	13.35 **13.15**	12.92 **12.76**	12.92 **12.60**	V min
		0.79	1.16 **1.42**	1.16 **1.32**	1.45 **1.58**	1.45 **1.75**	V max
Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **12**	16 **14**	13 **11**	13 **9**	mA min
	Sinking, $V_O = 5V$	21	16 **12**	16 **14**	13 **11**	13 **9**	mA min
Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19 **19**	28 **25**	23 **21**	23 **15**	mA min
	Sinking, $V_O = 13V$ (Note 12)	39	19 **19**	28 **24**	23 **20**	23 **15**	mA min
Supply Current	All Four Amplifiers $V_O = 1.5V$	1.5	2.2 **2.9**	2.2 **2.6**	2.7 **2.9**	2.7 **3.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AMD LMC660AMJ/883	LMC660AI	LMC660C	LMC660E	Units
			Limit (Notes 4, 9)	Limit (Note 4)	Limit (Note 4)	Limit (Note 4)	
Slew Rate	(Note 6)	1.1	0.8 **0.5**	0.8 **0.6**	0.8 **0.7**	0.8 **0.4**	V/μs min
Gain-Bandwidth Product		1.4	**0.5**				MHz
Phase Margin		50					Deg
Gain Margin		17					dB
Amp-to-Amp Isolation	(Note 7)	130					dB
Input Referred Voltage Noise	F = 1 kHz	22					$nV/\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002					$pA/\sqrt{Hz}$
Total Harmonic Distortion	$F = 10\ kHz, A_V = -10$ $R_L = 2\ k\Omega, V_O = 8\ V_{PP}$ $V^+ = 15V$	0.01					%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}) - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Typical values represent the most likely parametric norm. Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 6: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15V$ and $R_L = 10\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Note 9: A military RETS electrical test specification is available on request. At the time of printing, the LMC660AMJ/883 RETS spec complied fully with the boldface limits in this column. The LMC660AMJ/883 may also be procured to a Standard Military Drawing specification.

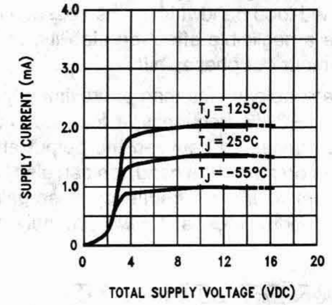
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

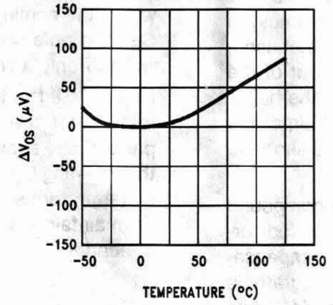
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

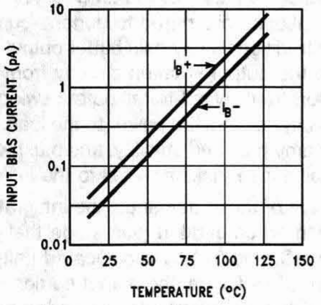
Supply Current vs Supply Voltage



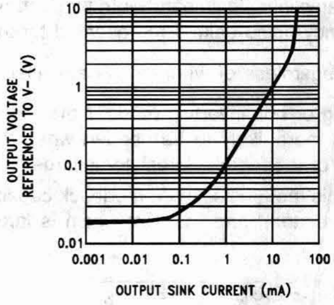
Offset Voltage



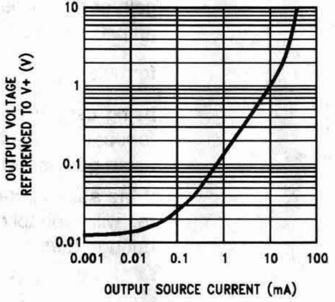
Input Bias Current



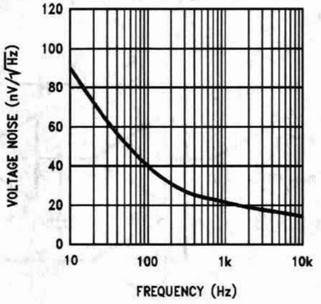
Output Characteristics Current Sinking



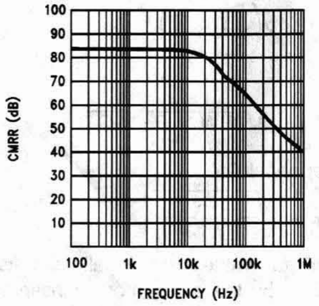
Output Characteristics Current Sourcing



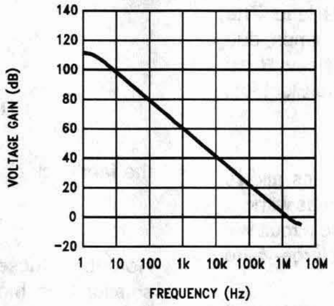
Input Voltage Noise vs Frequency



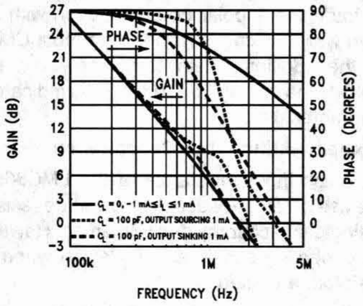
CMRR vs Frequency



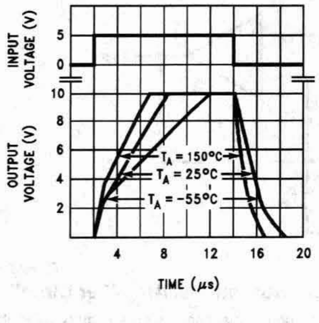
Open-Loop Frequency Response



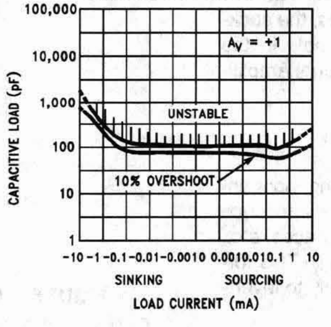
Frequency Response vs Capacitive Load



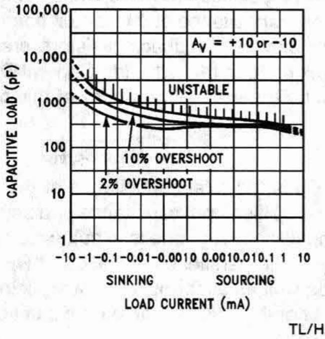
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/8767–3

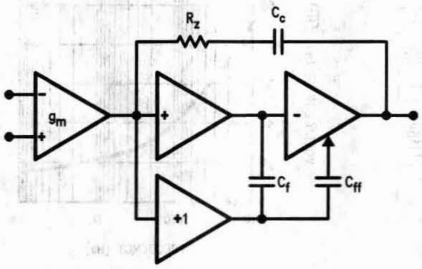
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

Amplifier Topology

The topology chosen for the LMC660, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and Cff) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/8767–4

FIGURE 1. LMC660 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

Compensating Input Capacitance

The high input resistance of the LMC660 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit, *Figure 2* the frequency of this pole is

$$fp = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capcitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \le \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where $\left(\frac{R_F}{R_{IN}} + 1\right)$ is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula $\left(\frac{R_F}{R_{IN}} + 1\right)$ regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \ge 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

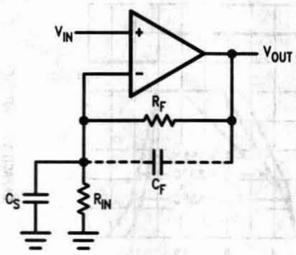
$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S}$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$



TL/H/8767–6

FIGURE 2. General Operational Amplifier Circuit

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

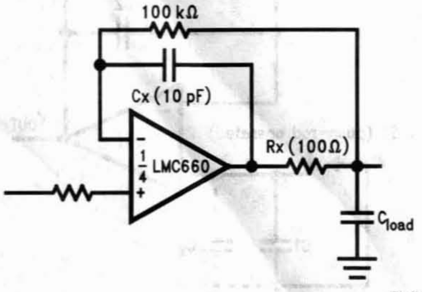
Application Hints (Continued)

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

Capacitive Load Tolerance

Like many other op amps, the LMC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See Typical Performance Characteristics.

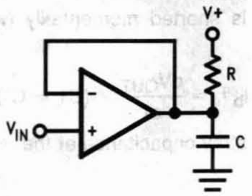
The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 3a,* the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/8767-5

FIGURE 3a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 3b).* Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



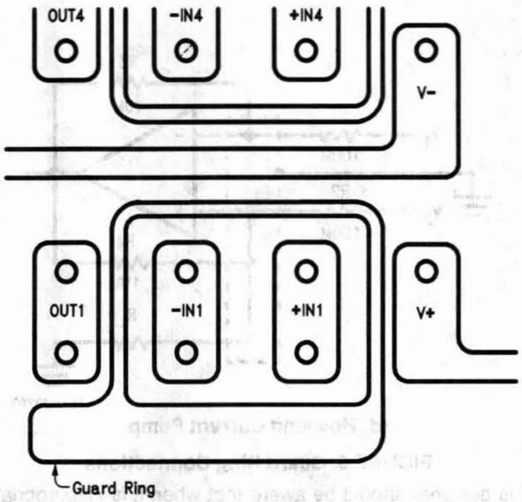
TL/H/8767-23

FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

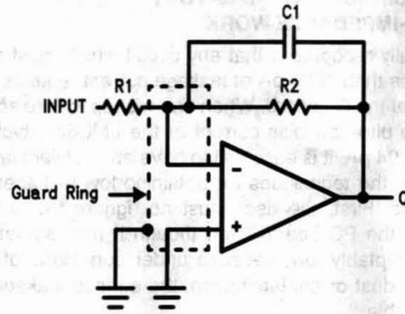
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 4.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 5a, 5b, 5c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 5d.*



TL/H/8767-16

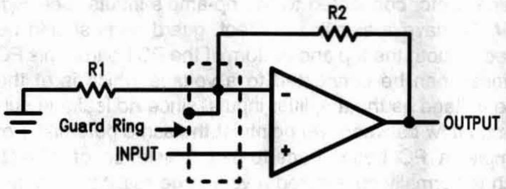
FIGURE 4. Example, using the LMC660, of Guard Ring in P.C. Board Layout

Application Hints (Continued)


C1
R1
R2
INPUT
Guard Ring
OUTPUT
-
+

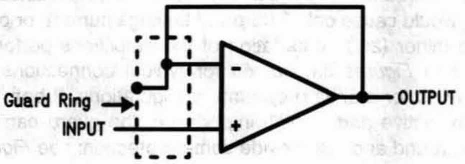
TL/H/8767-17

(a) Inverting Amplifier


R2
R1
Guard Ring
INPUT
OUTPUT
-
+

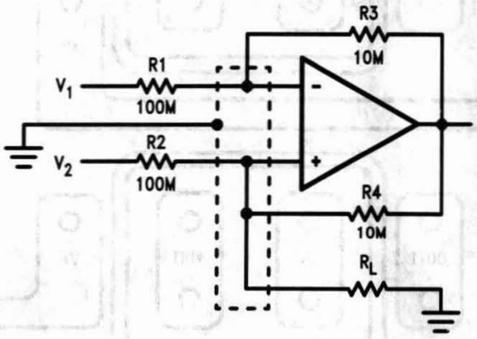
TL/H/8767-18

(b) Non-Inverting Amplifier


Guard Ring
INPUT
OUTPUT
-
+

TL/H/8767-19

(c) Follower

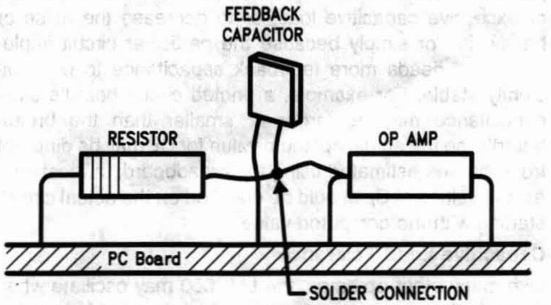

R3
10M
R1
V1
100M
R2
V2
100M
R4
10M
RL
-
+

TL/H/8767-20

(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.


FEEDBACK CAPACITOR
RESISTOR
OP AMP
PC Board
SOLDER CONNECTION

TL/H/8767-21

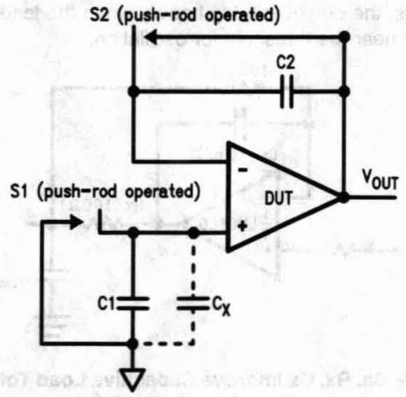
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b^- = \frac{dV_{OUT}}{dt} \times C2.$$


S2 (push-rod operated)
C2
S1 (push-rod operated)
DUT
VOUT
C1
CX
-
+

TL/H/8767-22

FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

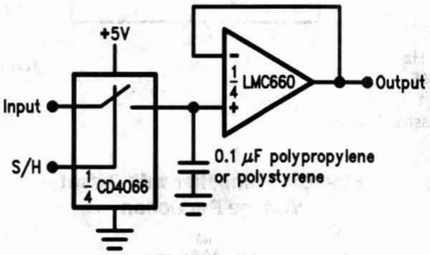
$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_X)$$

where C_X is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0$ VDC)

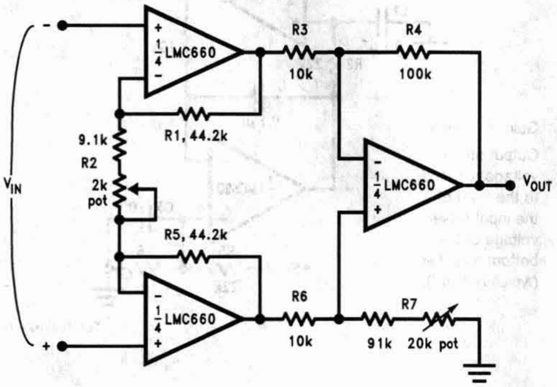
Additional single-supply applications ideas can be found in the LM324 datasheet. The LMC660 is pin-for-pin compatible with the LM324 and offers greater bandwidth and input resistance over the LM324. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC660 is smaller than that of the LM324.

Low-Leakage Sample-and-Hold


+5V
Input
S/H
$\frac{1}{4}$ CD4066
$\frac{1}{4}$ LMC660
Output
0.1 µF polypropylene or polystyrene

TL/H/8767–7

Instrumentation Amplifier


–
+
V_{IN}
$\frac{1}{4}$ LMC660
$\frac{1}{4}$ LMC660
$\frac{1}{4}$ LMC660
R3 10k
R4 100k
R1, 44.2k
9.1k
R2 2k pot
R5, 44.2k
R6 10k
R7 91k 20k pot
V_{OUT}

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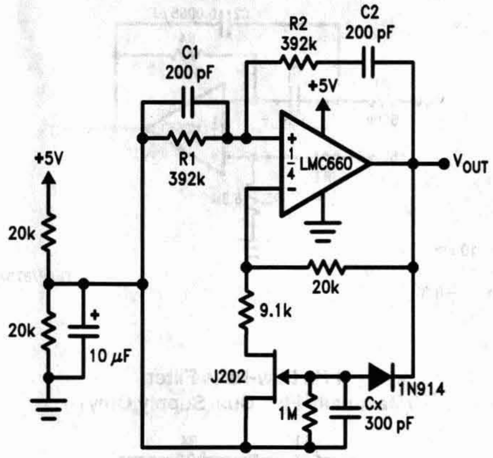
If R1 = R5, R3 = R6, and R4 = R7; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affect CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator


C2 200 pF
R2 392k
C1 200 pF
+5V
R1 392k
$\frac{1}{4}$ LMC660
V_{OUT}
+5V
20k
20k
10 µF
20k
9.1k
J202
1N914
1M
Cx 300 pF

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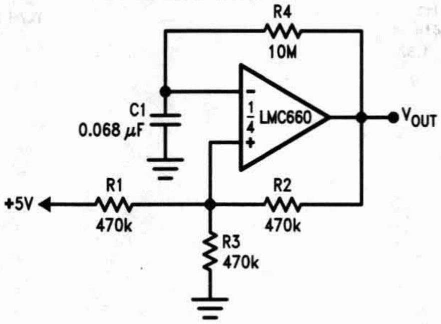
Oscillator frequency is determined by R1, R2, C1, and C2:

$f_{osc} = 1/2\pi RC$, where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator


R4 10M
C1 0.068 µF
$\frac{1}{4}$ LMC660
V_{OUT}
+5V
R1 470k
R2 470k
R3 470k

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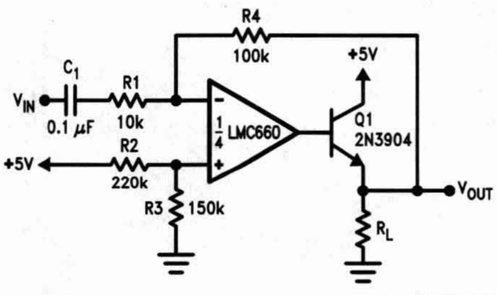
Power Amplifier


R4 100k
+5V
C_1 0.1 µF
V_{IN}
R1 10k
R2 220k
+5V
$\frac{1}{4}$ LMC660
Q1 2N3904
V_{OUT}
R3 150k
R_L

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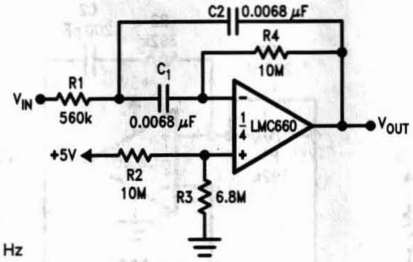
Typical Single-Supply Applications (V+ = 5.0 VDC) (Continued)

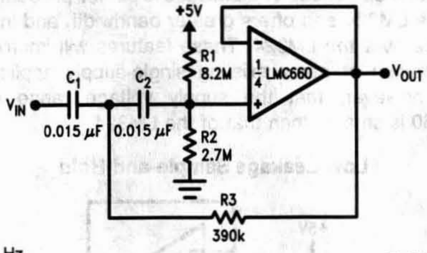
10 Hz Bandpass Filter


C2
0.0068 μF
R4
10M
V_IN
R1
560k
C1
0.0068 μF
1/4 LMC660
V_OUT
+5V
R2
10M
R3
6.8M

$f_O = 10$ Hz
Q = 2.1
Gain = −8.8

TL/H/8767–12

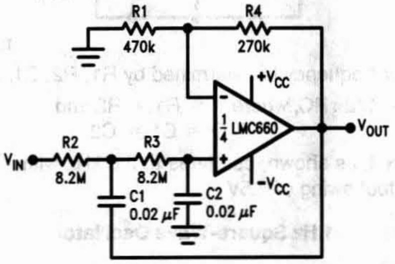
10 Hz High-Pass Filter


+5V
R1
8.2M
1/4 LMC660
V_OUT
V_IN
C1
C2
0.015 μF
0.015 μF
R2
2.7M
R3
390k

$f_c = 10$ Hz
d = 0.895
Gain = 1
2 dB passband ripple

TL/H/8767–13

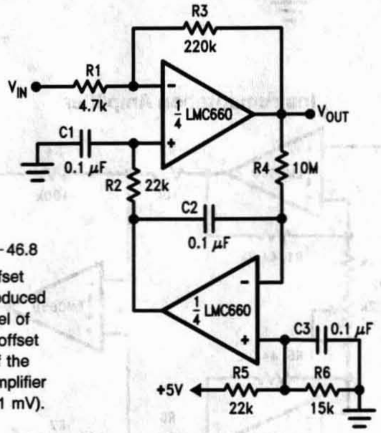
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)


R1
470k
R4
270k
+V_CC
1/4 LMC660
V_OUT
V_IN
R2
8.2M
R3
8.2M
C1
0.02 μF
C2
0.02 μF
−V_CC

$f_c = 1$ Hz
d = 1.414
Gain = 1.57

TL/H/8767–14

High Gain Amplifier with Offset Voltage Reduction


R3
220k
V_IN
R1
4.7k
1/4 LMC660
V_OUT
C1
0.1 μF
R2
22k
R4
10M
C2
0.1 μF
1/4 LMC660
C3
0.1 μF
+5V
R5
22k
R6
15k

Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

TL/H/8767–15

National Semiconductor

LMC662
CMOS Dual Operational Amplifier

General Description

The LMC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC660 datasheet for a Quad CMOS operational amplifier with these same features.

Features

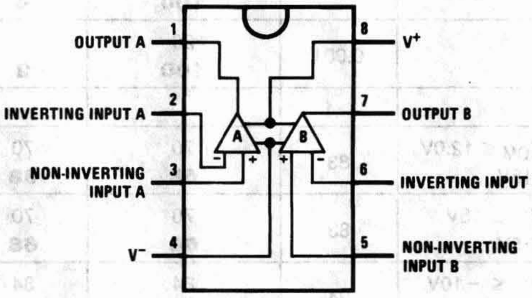
■ Rail-to-rail output swing	
■ Specified for 2 kΩ and 600Ω loads	
■ High voltage gain	126 dB
■ Low input offset voltage	3 mV
■ Low offset voltage drift	1.3 μV/°C
■ Ultra low input bias current	2 fA
■ Input common-mode range includes V^-	
■ Operating range from +5V to +15V supply	
■ I_{SS} = 400 μA/amplifier; independent of V^+	
■ Low distortion	0.01% at 10 kHz
■ Slew rate	1.1 V/μs
■ Available in extended temperature range (−40°C to +125°C); ideal for automotive applications	
■ Available to a Standard Military Drawing specification	

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram

8-Pin DIP/SO



TL/H/9763-1

Ordering Information

Package	Temperature Range				NSC Drawing	Transport Media
	Military	Extended	Industrial	Commercial		
8-Pin Ceramic DIP	LMC662AMJ/883				J08A	Rail
8-Pin Small Outline		LMC662EM	LMC662AIM	LMC662CM	M08A	Rail, Tape and Reel
8-Pin Molded DIP		LMC662EN	LMC662AIN	LMC662CN	N08E	Rail
8-Pin Side Brazed Ceramic DIP	LMC662AMD				D08C	Rail

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 1)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Voltage at Input/Output Pins	(V^+) +0.3V, (V^-) −0.3V
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 2)
Junction Temperature	150°C
ESD Tolerance (Note 8)	1000V

Operating Ratings (Note 3)

Temperature Range	
LMC662AMJ/883,	
LMC662AMD	$-55°C \le T_J \le +125°C$
LMC662AI	$-40°C \le T_J \le +85°C$
LMC662C	$0°C \le T_J \le +70°C$
LMC662E	$-40°C \le T_J \le +125°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}) (Note 11)	
8-Pin Ceramic DIP	100°C/W
8-Pin Molded DIP	101°C/W
8-Pin SO	165°C/W
8-Pin Side Brazed Ceramic DIP	100°C/W

DC Electrical Characteristics

unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC662AMJ/883 LMC662AMD	LMC662AI	LMC662C	LMC662E	Units
			Limit (Note 4, 9)	Limit (Note 4)	Limit (Note 4)	Limit (Note 4)	
Input Offset Voltage		1	3 **3.5**	3 **3.3**	6 **6.3**	6 **6.5**	mV max
Input Offset Voltage Average Drift		1.3					μV/°C
Input Bias Current		0.002	20 **100**	**4**	**2**	**60**	pA max
Input Offset Current		0.001	20 **100**	**2**	**1**	**60**	pA max
Input Resistance		>1					TeraΩ
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70 **68**	70 **68**	63 **62**	63 **60**	dB min
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70 **68**	70 **68**	63 **62**	63 **60**	dB min
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84 **82**	84 **83**	74 **73**	74 **70**	dB min
Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	−0.1 **0**	V max
		$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.4$**	$V^+ - 2.3$ **$V^+ - 2.6$**	V min
Large Signal Voltage Gain	$R_L = 2\,k\Omega$ (Note 5) Sourcing	2000	400 **300**	440 **400**	300 **200**	200 **100**	V/mV min
	Sinking	500	180 **70**	180 **120**	90 **80**	90 **40**	V/mV min
	$R_L = 600\Omega$ (Note 5) Sourcing	1000	200 **150**	220 **200**	150 **100**	100 **75**	V/mV min
	Sinking	250	100 **35**	100 **60**	50 **40**	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC662AMJ/883 LMC662AMD	LMC662AI	LMC662C	LMC662E	Units
			Limit (Note 4, 9)	Limit (Note 4)	Limit (Note 4)	Limit (Note 4)	
Output Swing	$V^+ = 5V$ $R_L = 2\ k\Omega$ to $V^+/2$	4.87	4.82 **4.77**	4.82 **4.79**	4.78 **4.76**	4.78 **4.70**	V min
		0.10	0.15 **0.19**	0.15 **0.17**	0.19 **0.21**	0.19 **0.25**	V max
	$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$	4.61	4.41 **4.24**	4.41 **4.31**	4.27 **4.21**	4.27 **4.10**	V min
		0.30	0.50 **0.63**	0.50 **0.56**	0.63 **0.69**	0.63 **0.75**	V max
	$V^+ = 15V$ $R_L = 2\ k\Omega$ to $V^+/2$	14.63	14.50 **14.40**	14.50 **14.44**	14.37 **14.32**	14.37 **14.25**	V min
		0.26	0.35 **0.43**	0.35 **0.40**	0.44 **0.48**	0.44 **0.55**	V max
	$V^+ = 15V$ $R_L = 600\Omega$ to $V^+/2$	13.90	13.35 **13.02**	13.35 **13.15**	12.92 **12.76**	12.92 **12.60**	V min
		0.79	1.16 **1.42**	1.16 **1.32**	1.45 **1.58**	1.45 **1.75**	V max
Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **12**	16 **14**	13 **11**	13 **9**	mA min
	Sinking, $V_O = 5V$	21	16 **12**	16 **14**	13 **11**	13 **9**	mA min
Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19 **19**	28 **25**	23 **21**	23 **15**	mA min
	Sinking, $V_O = 13V$ (Note 12)	39	19 **19**	28 **24**	23 **20**	23 **15**	mA min
Supply Current	Both Amplifiers $V_O = 1.5V$	0.75	1.3 **1.8**	1.3 **1.5**	1.6 **1.8**	1.6 **1.9**	mA max

AC Electrical Characteristics

unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC662AMJ/883 LMC662AMD Limit (Note 4, 9)	LMC662AI Limit (Note 4)	LMC662C Limit (Note 4)	LMC662E Limit (Note 4)	Units
Slew Rate	(Note 6)	1.1	0.8 **0.5**	0.8 **0.6**	0.8 **0.7**	0.8 **0.4**	V/μs min
Gain-Bandwidth Product		1.4					MHz
Phase Margin		50					Deg
Gain Margin		17					dB
Amp-to-Amp Isolation	(Note 7)	130					dB
Input-Referred Voltage Noise	F = 1 kHz	22					nV/$\sqrt{Hz}$
Input-Referred Current Noise	F = 1 kHz	0.0002					pA/$\sqrt{Hz}$
Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} V^+ = 15V	0.01					%

Note 1: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Typical values represent the most likely parametric norm. Limits are guaranteed by testing or correlation.

Note 5: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 6: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. V^+ = 15V and R_L = 10 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Note 9: A military RETS electrical test specification is available on request. At the time of printing, the LMC662AMJ/883 RETS spec complied fully with the boldface limits in this column. The LMC662AMJ/883 may also be procured to a Standard Military Drawing specification.

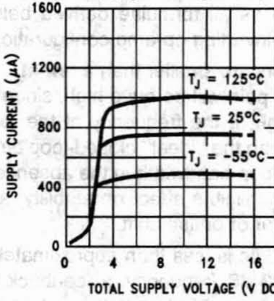
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

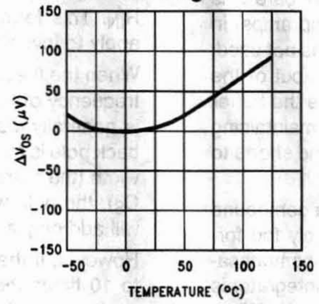
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

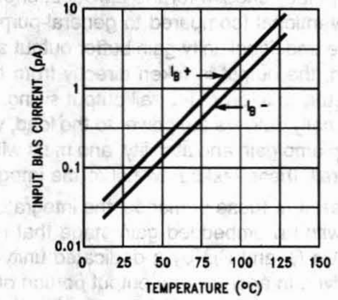
Supply Current vs Supply Voltage



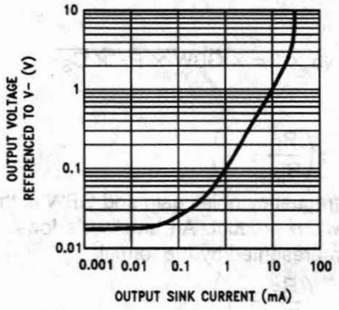
Offset Voltage



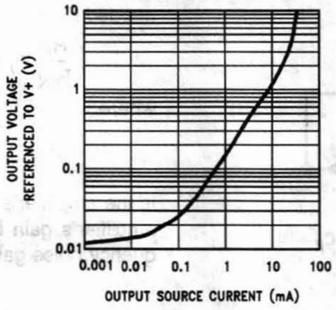
Input Bias Current



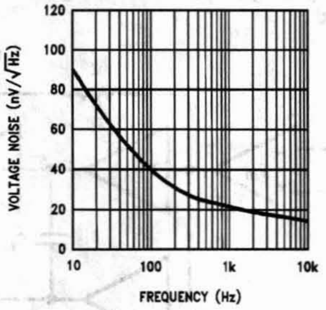
Output Characteristics Current Sinking



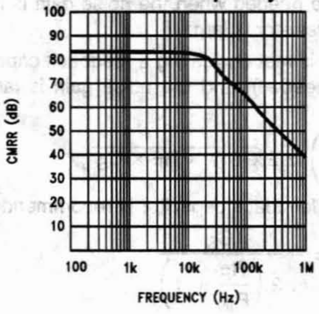
Output Characteristics Current Sourcing



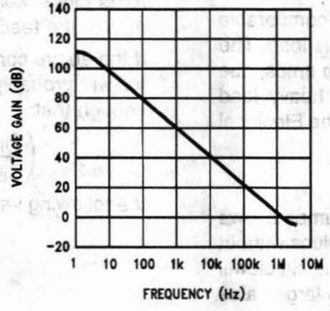
Input Voltage Noise vs Frequency



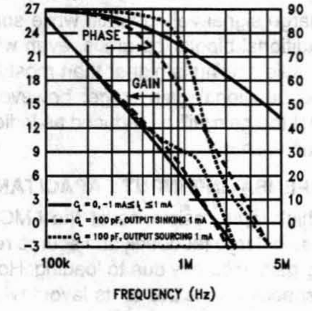
CMRR vs Frequency



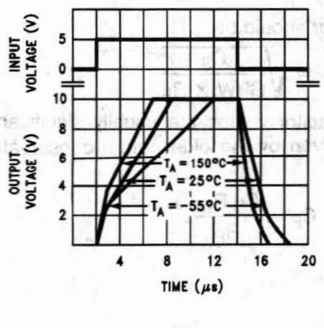
Open-Loop Frequency Response



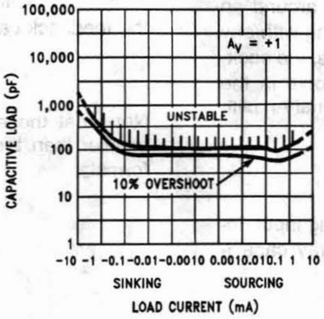
Frequency Response vs Capacitive Load



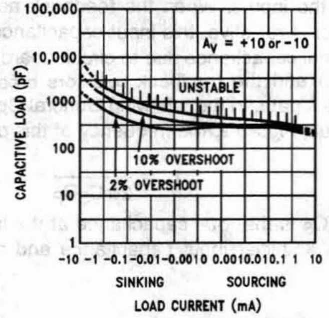
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



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Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

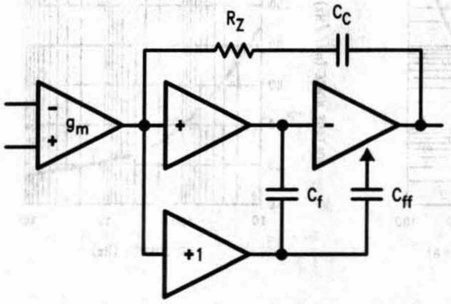
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC662, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/9763–4

FIGURE 1. LMC662 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC662 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier Circuit, *Figure 2*, the frequency of this pole is

$$f_P = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability, a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \le \sqrt{6 \times 2\pi \times \text{GBW} \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

regardless of whether the amplifier is being used in an inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \ge 2\sqrt{\text{GBW} \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{\text{GBW} \times R_F \times C_S},$$

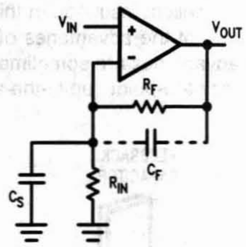
the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{\text{GBW} \times R_F}}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}.$$

Application Hints (Continued)



TL/H/9763-6

FIGURE 2. General Operational Amplifier Circuit

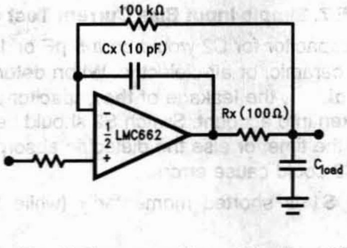
C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistor.

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the value of C_F should be checked on the actual circuit, starting with the computed value.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC662 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

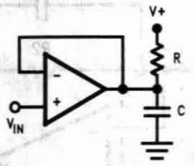
The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 3a*, the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/9763-5

FIGURE 3a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 3b)*. Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



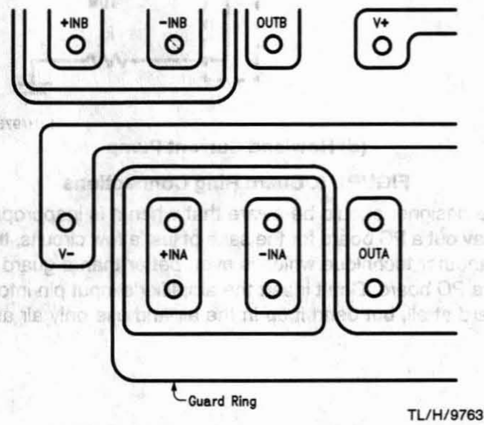
TL/H/9763-23

FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

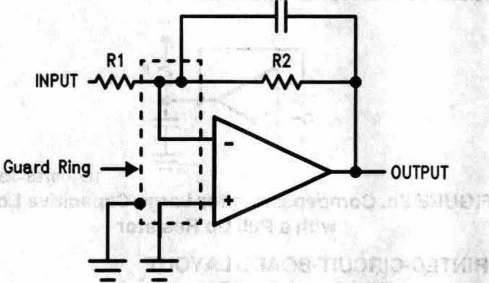
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC662's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 4*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC662's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 5a*, *5b*, *5c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 5d.*



TL/H/9763-16

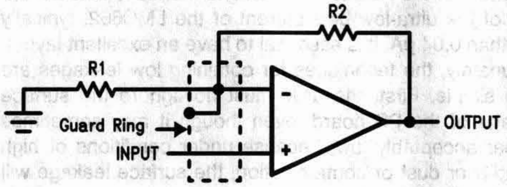
FIGURE 4. Example, using the LMC660, of Guard Ring in P.C. Board Layout

Application Hints (Continued)


C1
R1
R2
INPUT
Guard Ring
OUTPUT
-
+

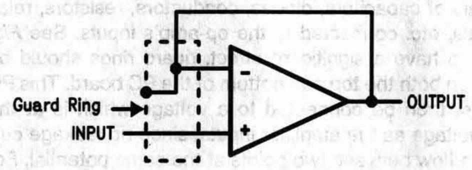
TL/H/9763-17

(a) Inverting Amplifier


R2
R1
Guard Ring
INPUT
OUTPUT
-
+

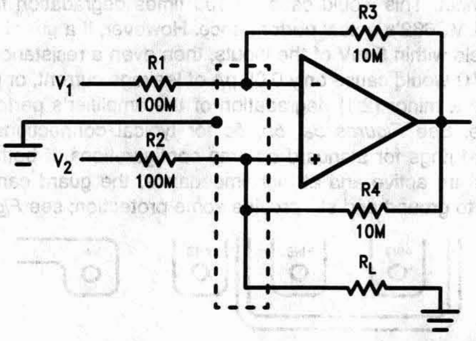
TL/H/9763-18

(b) Non-Inverting Amplifier


Guard Ring
INPUT
OUTPUT
-
+

TL/H/9763-19

(c) Follower

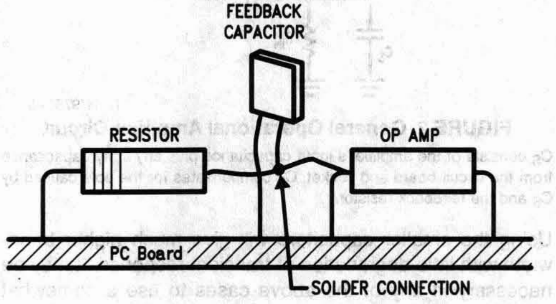

R3
10M
R1
V1
100M
R2
V2
100M
R4
10M
RL
-
+

TL/H/9763-20

(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.


FEEDBACK CAPACITOR
RESISTOR
OP AMP
PC Board
SOLDER CONNECTION

TL/H/9763-21

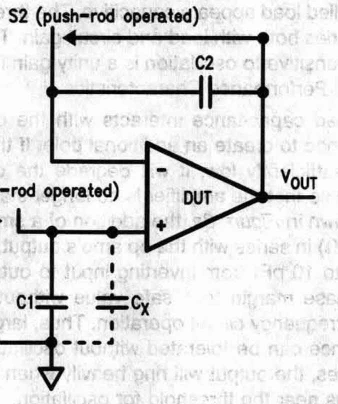
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b^- = \frac{dV_{OUT}}{dt} \times C2.$$


S2 (push-rod operated)
C2
S1 (push-rod operated)
DUT
VOUT
C1
Cx
-
+

TL/H/9763-22

FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

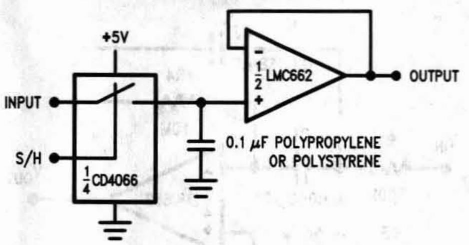
$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

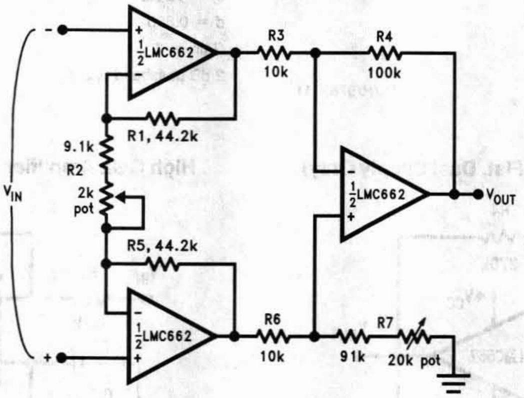
Additional single-supply applications ideas can be found in the LM358 datasheet. The LMC662 is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LM662 is smaller than that of the LM358.

Low-Leakage Sample-and-Hold


+5V
INPUT
S/H
1/4 CD4066
1/2 LMC662
OUTPUT
0.1 μF POLYPROPYLENE
OR POLYSTYRENE

TL/H/9763-15

Instrumentation Amplifier


-
+
V_IN
1/2 LMC662
1/2 LMC662
1/2 LMC662
R3
10k
R4
100k
R1, 44.2k
9.1k
R2
2k pot
R5, 44.2k
R6
10k
R7
91k
20k pot
V_OUT

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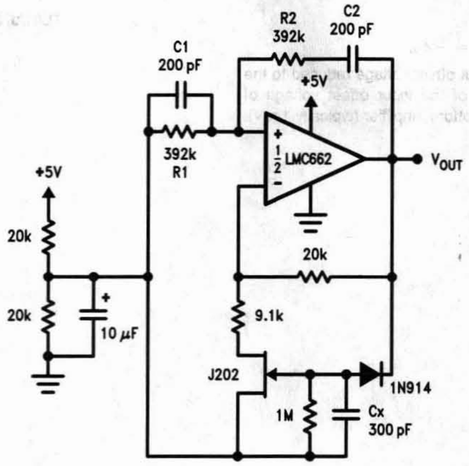
If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator


R2
392k
C2
200 pF
C1
200 pF
+5V
392k
R1
1/2 LMC662
V_OUT
+5V
20k
20k
10 μF
20k
9.1k
J202
1N914
1M
Cx
300 pF

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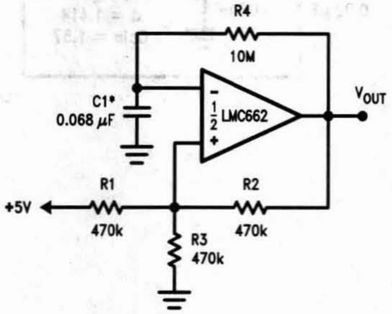
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

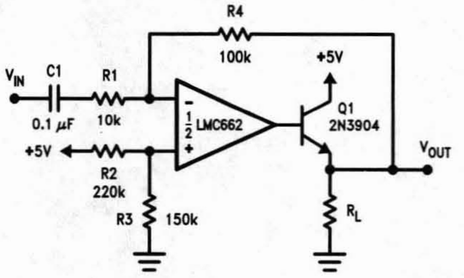
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator


R4
10M
C1*
0.068 μF
1/2 LMC662
V_OUT
+5V
R1
470k
R2
470k
R3
470k

TL/H/9763-9

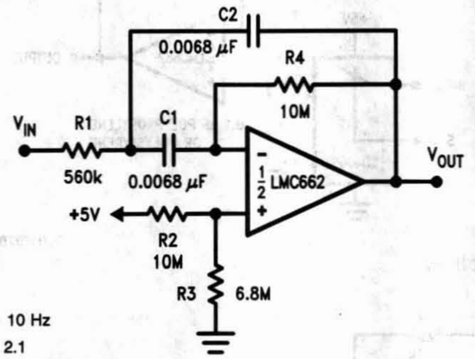
Power Amplifier


R4
100k
+5V
V_IN
C1
0.1 μF
R1
10k
1/2 LMC662
Q1
2N3904
V_OUT
+5V
R2
220k
R3
150k
R_L

TL/H/9763-10

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

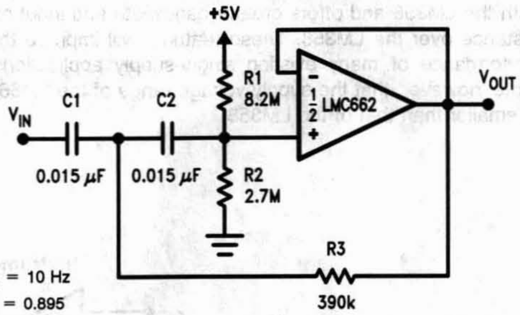
10 Hz Bandpass Filter


C2
0.0068 μF
R4
10M
V_{IN}
R1
560k
C1
0.0068 μF
1/2 LMC662
V_{OUT}
+5V
R2
10M
R3
6.8M

$f_O = 10$ Hz
Q = 2.1
Gain = −8.8

TL/H/9763–11

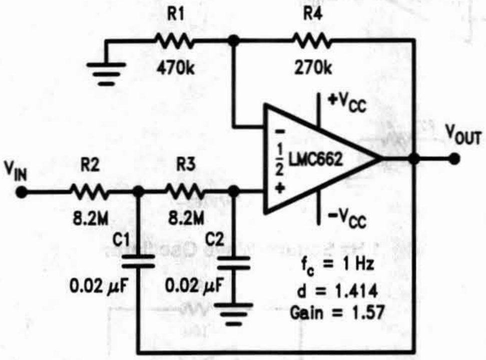
10 Hz High-Pass Filter


+5V
R1
8.2M
C1
C2
V_{IN}
0.015 μF
0.015 μF
R2
2.7M
1/2 LMC662
V_{OUT}
R3
390k

$f_c = 10$ Hz
d = 0.895
Gain = 1
2 dB passband ripple

TL/H/9763–12

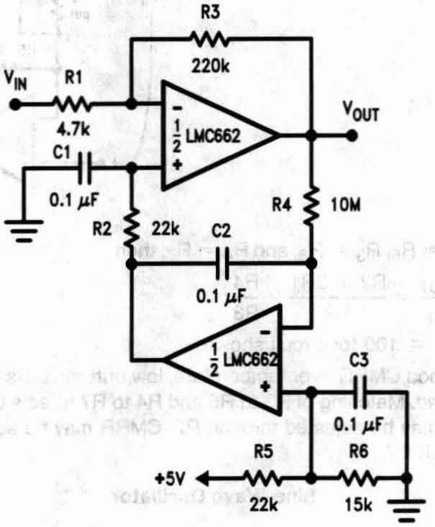
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)


R1
470k
R4
270k
+V_{CC}
V_{OUT}
V_{IN}
R2
8.2M
R3
8.2M
1/2 LMC662
−V_{CC}
C1
0.02 μF
C2
0.02 μF

$f_c = 1$ Hz
d = 1.414
Gain = 1.57

TL/H/9763–13

High Gain Amplifier with Offset Voltage Reduction


R3
220k
V_{IN}
R1
4.7k
C1
0.1 μF
1/2 LMC662
V_{OUT}
R4
10M
R2
22k
C2
0.1 μF
1/2 LMC662
C3
0.1 μF
R5
22k
R6
15k
+5V

TL/H/9763–14

Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

National Semiconductor

LMC6001 Ultra Ultra-Low Input Current Amplifier

General Description

Featuring 100% tested input currents of 25 fA max., low operating power, and ESD protection of 2000V, the LMC6001 achieves a new industry benchmark for low input current operational amplifiers. By tightly controlling the molding compound, National is able to offer this ultra-low input current in a lower cost molded package.

To avoid long turn-on settling times common in other low input current opamps, the LMC6001A is tested 3 times in the first minute of operation. Even units that meet the 25 fA limit are rejected if they drift.

Because of the ultra-low input current noise of 0.13 fA/$\sqrt{\text{Hz}}$, the LMC6001 can provide almost noiseless amplification of high resistance signal sources. Adding only 1 dB at 100 kΩ, 0.1 dB at 1 MΩ and 0.01 dB or less from 10 MΩ to 2,000 MΩ, the LMC6001 is an almost noiseless amplifier.

The LMC6001 is ideally suited for electrometer applications requiring ultra-low input leakage such as sensitive photodetection transimpedance amplifiers and sensor amplifiers. Since input referred noise is only 22 nV/$\sqrt{\text{Hz}}$, the LMC6001 can achieve higher signal to noise ratio than JFET input type electrometer amplifiers. Other applications of the LMC6001 include long interval integrators, ultra-high input impedance instrumentation amplifiers, and sensitive electrical-field measurement circuits.

Features (Max limit, 25°C unless otherwise noted)

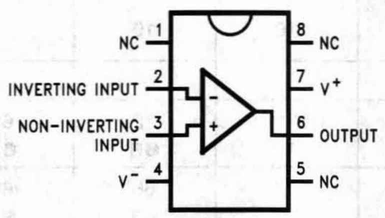
■ Input current (100% tested)	25 fA
■ Input current over temp.	2 pA
■ Low power	750 μA
■ Low V_{OS}	350 μV
■ Low noise	22 nV/$\sqrt{\text{Hz}}$ @1 kHz Typ.

Applications

- Electrometer amplifier
- Photodiode preamplifier
- Ion detector
- A.T.E. leakage testing

Connection Diagrams

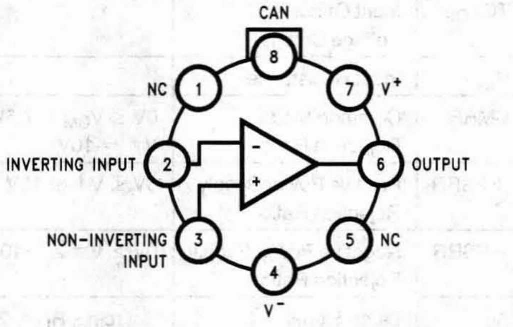
8-Pin DIP



TL/H/11887-1

Top View

8-Pin Metal Can



TL/H/11887-2

Top View

Ordering Information

Package	Industrial Temperature Range −40°C to +85°C	NSC Package Drawing
8-Pin Molded DIP	LMC6001AIN, LMC6001BIN, LMC6001CIN	N08E
8-Pin Metal Can	LMC6001AIH, LMC6001BIH	H08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	−0.3V to +16V
Output Short Circuit to V^+	(Notes 2, 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)
ESD Tolerance (Note 9)	2 kV

Operating Ratings (Note 1)

Temperature Range LMC6001AI, LMC6001BI, LMC6001CI	$-40°C \leq T_J \leq +85°C$
Supply Voltage	$4.5V \leq V^+ \leq 15.5V$
Thermal Resistance (Note 11)	
θ_{JA}, N Package	100°C/W
θ_{JA}, H Package	145°C/W
θ_{JC}, H Package	45°C/W
Power Dissipation	(Note 8)

DC Electrical Characteristics

Limits in standard typeface guaranteed for $T_J = 25°C$ and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, and $R_L > 1M$.

Symbol	Parameter	Conditions	Typical (Note 4)	Limits (Note 5)			Units
				LMC6001AI	LMC6001BI	LMC6001CI	
I_B	Input Current	Either Input, $V_{CM} = 0V$, $V_S = \pm 5V$	10	25 **2000**	100 **4000**	1000 **4000**	fA
I_{OS}	Input Offset Current		5	**1000**	**2000**	**2000**	
V_{OS}	Input Offset Voltage			0.35 **1.0**	1.0 **1.7**	1.0 **2.0**	mV
		$V_S = \pm 5V$, $V_{CM} = 0V$		0.7 **1.35**	1.35 **2.0**	1.35	
TCV_{OS}	Input Offset Voltage Drift		2.5	10	10		μV/°C
R_{IN}	Input Resistance		>1				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 7.5V$ $V^+ = 10V$	83	75 **72**	72 **68**	66 **63**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V^+ \leq 15V$	83	73 **70**	66 **63**	66 **63**	
−PSRR	Negative Power Supply Rejection Ratio	$0V \geq V^- \geq -10V$	94	80 **77**	74 **71**	74 **71**	
A_V	Large Signal Voltage Gain	Sourcing, $R_L = 2\ k\Omega$ (Note 6)	1400	400 **300**	300 **200**	300 **200**	V/mV min
		Sinking, $R_L = 2\ k\Omega$ (Note 6)	350	180 **100**	90 **60**	90 **60**	

DC Electrical Characteristics

Limits in standard typeface guaranteed for $T_J = 25°C$ and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, and $R_L > 1M$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 4)	Limits (Note 5)			Units
				LM6001AI	LM6001BI	LM6001CI	
V_{CM}	Input Common-Mode Voltage	$V^+ = 5V$ and 15V For CMRR ≥ 60 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V min
V_O	Output Swing	$V^+ = 5V$ $R_L = 2\ k\Omega$ to 2.5V	4.87	4.80 **4.73**	4.75 **4.67**	4.75 **4.67**	V min
			0.10	0.14 **0.17**	0.20 **0.24**	0.20 **0.24**	V max
		$V^+ = 15V$ $R_L = 2\ k\Omega$ to 7.5V	14.63	14.50 **14.34**	14.37 **14.25**	14.37 **14.25**	V min
			0.26	0.35 **0.45**	0.44 **0.56**	0.44 **0.56**	V max
I_O	Output Current	Sourcing, $V^+ = 5V$, $V_O = 0V$	22	16 **10**	13 **8**	13 **8**	mA min
		Sinking, $V^+ = 5V$, $V_O = 5V$	21	16 **13**	13 **10**	13 **10**	
		Sourcing, $V^+ = 15V$, $V_O = 0V$	30	28 **22**	23 **18**	23 **18**	
		Sinking, $V^+ = 15V$, $V_O = 13V$ (Note 10)	34	28 **22**	23 **18**	23 **18**	
I_S	Supply Current	$V^+ = 5V$, $V_O = 1.5V$	450	750 **900**	750 **900**	750 **900**	μA max
		$V^+ = 15V$, $V_O = 7.5V$	550	850 **950**	850 **950**	850 **950**	

AC Electrical Characteristics

Limits in standard typeface guaranteed for $T_J = 25°C$ and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Typical (Note 4)	Limits (Note 5)			Units
				LM6001AI	LM6001BI	LM6001CI	
SR	Slew Rate	(Note 7)	1.5	0.8 **0.6**	0.8 **0.6**	0.8 **0.6**	V/μs min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕf_m	Phase Margin		50				Deg
G_M	Gain Margin		17				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.13				$fA/\sqrt{Hz}$
THD	Total Harmonic Distortion	F = 10 kHz, $A_V = -10$, $R_L = 100\ k\Omega$, $V_O = 8\ V_{PP}$	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 7: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Limit specified is the lower of the positive and negative slew rates.

Note 8: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

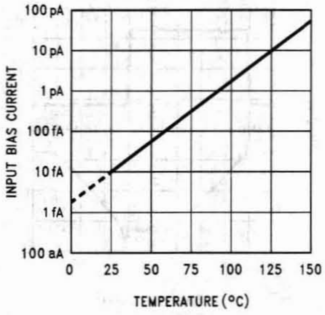
Note 9: Human body model, 1.5 kΩ in series with 100 pF.

Note 10: Do not connect the output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

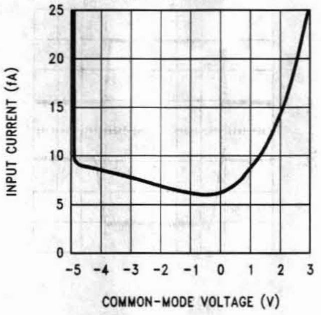
Note 11: All numbers apply for packages soldered directly into a printed circuit board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, unless otherwise specified

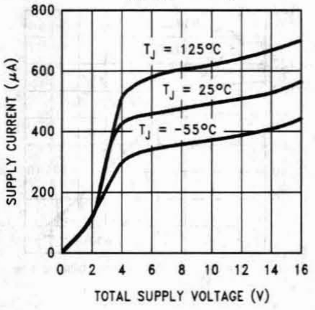
Input Current vs Temperature



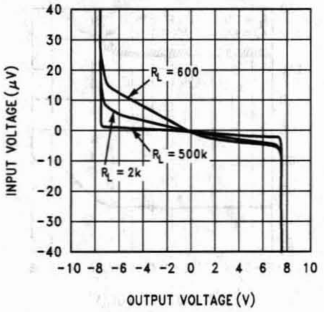
Input Current vs V_{CM} $V_S = \pm 5V$



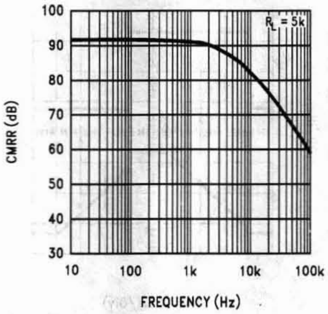
Supply Current vs Supply Voltage



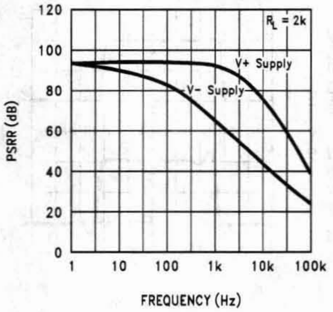
Input Voltage vs Output Voltage



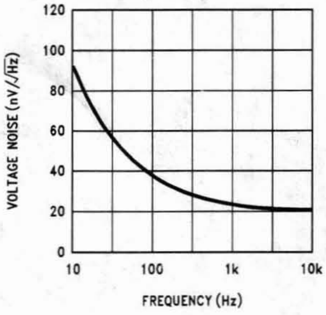
Common Mode Rejection Ratio vs Frequency



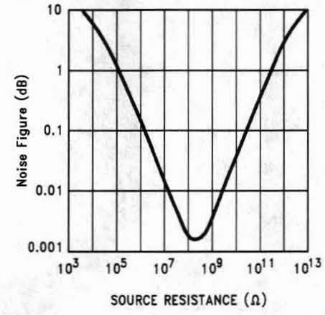
Power Supply Rejection Ratio vs Frequency



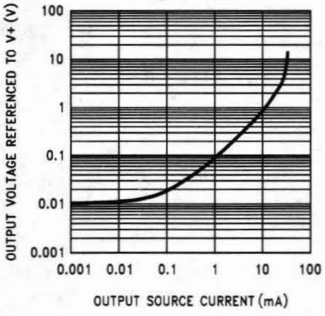
Input Voltage Noise vs Frequency



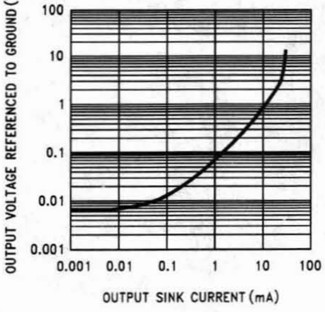
Noise Figure vs Source Resistance



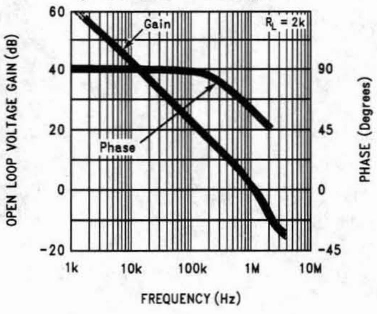
Output Characteristics Sourcing Current



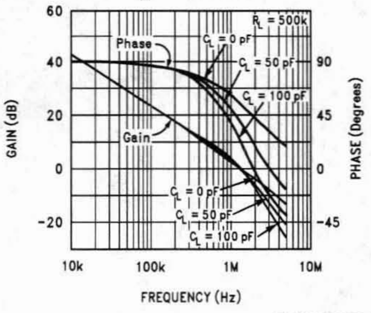
Output Characteristics Sinking Current



Gain and Phase Response vs Temperature (−55°C to +125°C)

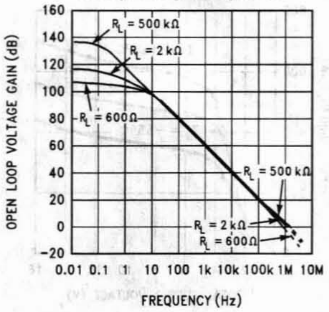


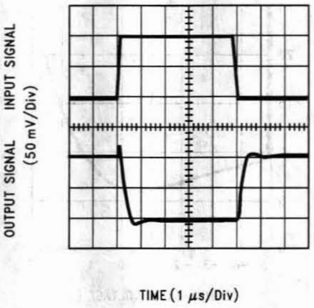
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$

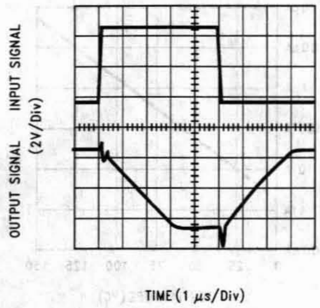


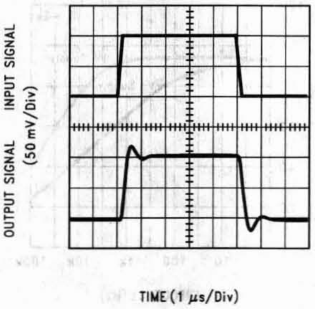
TL/H/11887-3

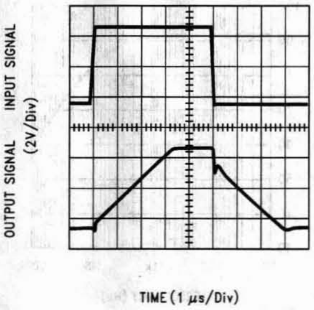
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, unless otherwise specified

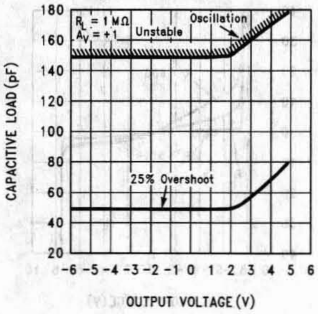

Open Loop Frequency Response


Inverting Small Signal Pulse Response


Inverting Large Signal Pulse Response


Non-Inverting Small Signal Pulse Response


Non-Inverting Large Signal Pulse Response


Stability vs Capacitive Load

TL/H/11887-4

Applications Hints

AMPLIFIER TOPOLOGY

The LMC6001 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional op-amps. These features make the LMC6001 both easier to design with, and provide higher speed than products typically found in this low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6001.

Although the LMC6001 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors with even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6001 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

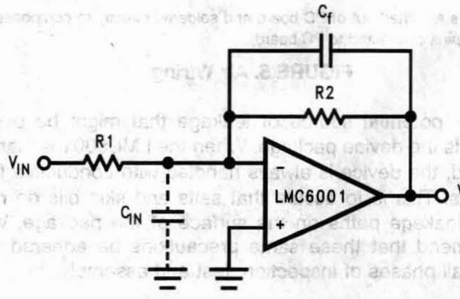
The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1\, C_{IN} \leq R_2\, C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.



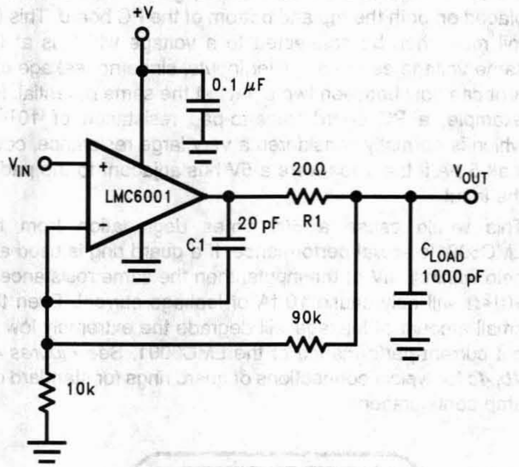
TL/H/11887–5

FIGURE 1. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see Typical Curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

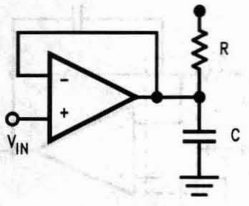


TL/H/11887–6

FIGURE 2a. LMC6001 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pullup resistor to V+ *(Figure 2b)*. Typically a pullup resistor conducting 500 µA or more will significantly improve capacitive load responses. The value of the pullup resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pullup resistor (see Electrical Characteristics).



TL/H/11887–7

FIGURE 2b. Compensating for Large Capacitive Loads with a Pullup Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

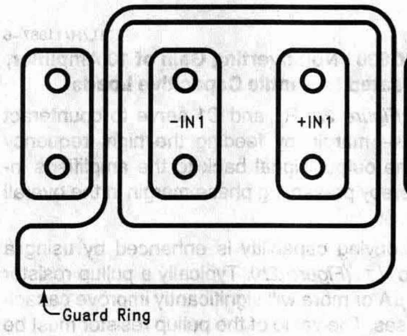
It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6001, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface

Applications Hints (Continued)

leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

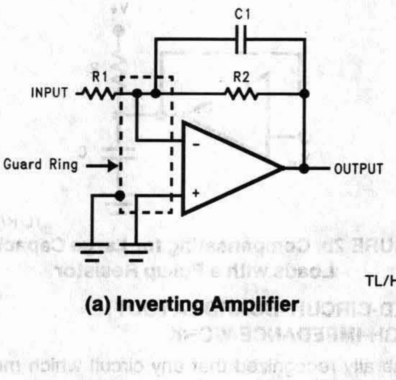
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6001's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc., connected to the op-amp's inputs, as in *Figure 3.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input.

This would cause a 500 times degradation from the LMC6001's actual performance. If a guard ring is used and held within 1 mV of the inputs, then the same resistance of $10^{12}\Omega$ will only cause 10 fA of leakage current. Even this small amount of leakage will degrade the extremely low input current performance of the LMC6001. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations.



TL/H/11887-8

FIGURE 3. Examples of Guard Ring in PC Board Layout



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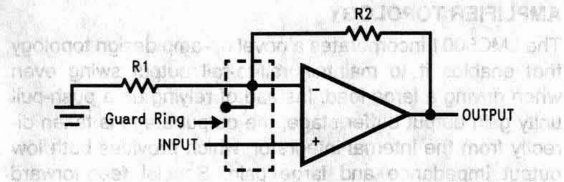
(a) Inverting Amplifier



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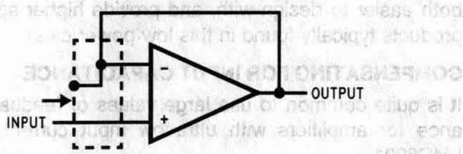
(b) Non-Inverting Amplifier



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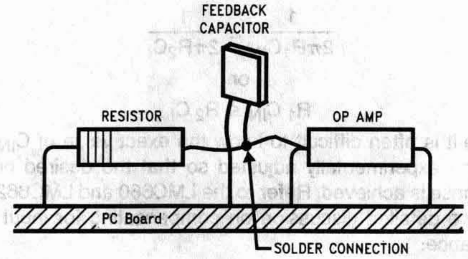
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5.*



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring

Another potential source of leakage that might be overlooked is the device package. When the LMC6001 is manufactured, the device is always handled with conductive finger cots. This is to assure that salts and skin oils do not cause leakage paths on the surface of the package. We recommend that these same precautions be adhered to, during all phases of inspection, test and assembly.

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6001 is designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

Typical Applications

The extremely high input resistance, and low power consumption, of the LMC6001 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, electrostatic field detectors and gas chromotographs.

Two Opamp, Temperature Compensated pH Probe Amplifier

The signal from a pH probe has a typical resistance between 10 MΩ and 1000 MΩ. Because of this high value, it is very important that the amplifier input currents be as small as possible. The LMC6001 with less than 25 fA input current is an ideal choice for this application.

The theoretical output of the standard Ag/AgCl pH probe is 59.16 mV/pH at 25°C with 0V out at a pH of 7.00. This output is proportional to absolute temperature. To compensate for this, a temperature compensating resistor, R1, is placed in the feedback loop. This cancels the temperature dependence of the probe. This resistor must be mounted where it will be at the same temperature as the liquid being measured.

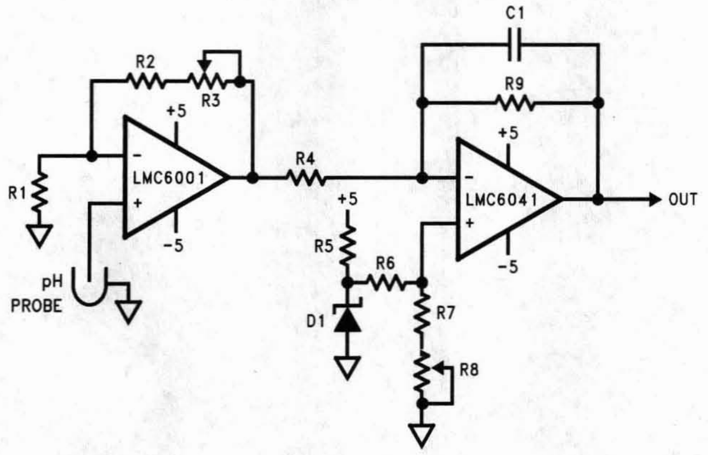
The LMC6001 amplifies the probe output providing a scaled voltage of ±100 mV/pH from a pH of 7. The second opamp, a micropower LMC6041 provides phase inversion and offset so that the output is directly proportional to pH, over the full range of the probe. The pH reading can now be directly displayed on a low cost, low power digital panel meter. Total current consumption will be about 1 mA for the whole system.

The micropower dual operational amplifier, LMC6042, would optimize power consumption but not offer these advantages:

1. The LMC6001A guarantees a 25 fA limit on input current at 25°C.
2. The input ESD protection diodes in the LMC6042 are only rated at 500V while the LMC6001 has much more robust protection that is rated at 2000V.

The setup and calibration is simple with no interactions to cause problems.

1. Disconnect the pH probe and with R3 set to about midrange and the noninverting input of the LMC6001 grounded, adjust R8 until the output is 700 mV.
2. Apply −414.1 mV to the noninverting input of the LMC6001. Adjust R3 for and output of 1400 mV. This completes the calibration. As real pH probes may not perform exactly to theory, minor gain and offset adjustments should be made by trimming while measuring a precision buffer solution.



R1 100k + 3500 ppm/°C*
R2 68.1k
R3, 8 5k
R4, 9 100k
R5 36.5k
R6 619k
R7 97.6k
D1 LM4040D1Z-2.5
C1 2.2 μF

*(Micro-ohm style 144 or similar)

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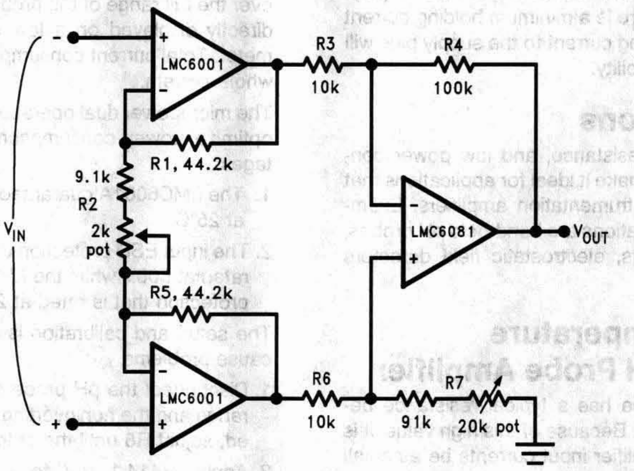
FIGURE 6. pH Probe Amplifier

Ultra-Low Input Current Instrumentation Amplifier

Figure 7 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 MΩ imbalance in source resistance. Input current is less than 20 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



-
+
LMC6001
R3
10k
R4
100k
R1, 44.2k
9.1k
R2
2k pot
V_{IN}
LMC6081
V_{OUT}
R5, 44.2k
LMC6001
R6
10k
R7
91k
20k pot
+

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If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.85k$).

FIGURE 7. Instrumentation Amplifier

National Semiconductor

LMC6022
Low Power CMOS Dual Operational Amplifier

General Description

The LMC6022 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V$^-$, low input bias current, and voltage gain (into 100k and 5 kΩ loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6024 datasheet for a CMOS quad operational amplifier with these same features.

Features

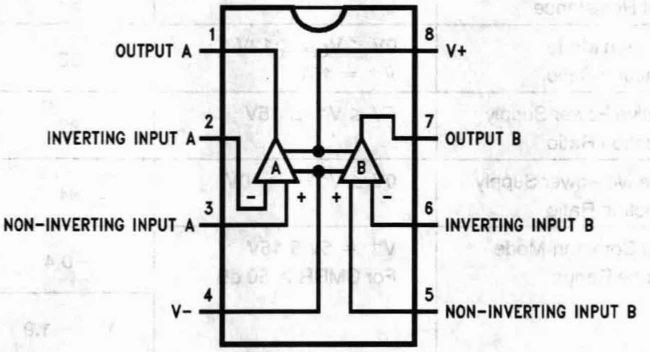
■ Specified for 100 kΩ and 5 kΩ loads	
■ High voltage gain	120 dB
■ Low offset voltage drift	2.5 μV/°C
■ Ultra low input bias current	40 fA
■ Input common-mode range includes V$^-$	
■ Operating range from +5V to +15V supply	
■ Low distortion	0.01% at 1 kHz
■ Slew rate	0.11 V/μs
■ Micropower operation	0.5 mW

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls

Connection Diagram

8-Pin DIP/SO



TL/H/11236-1

Top View

Ordering Information

Temperature Range Industrial $-40°C \leq T_J \leq +85°C$	Package	NSC Drawing	Transport Media
LMC6022IN	8-Pin Molded DIP	N08E	Rail
LMC6022IM	8-Pin Small Outline	M08A	Rail Tape and Reel

Absolute Maximum Ratings (Note 1)

Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	1000V
Voltage at Output/Input Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Current at Output Pin	± 18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Current at Input Pin	± 5 mA
Output Short Circuit to V^-	(Note 2)
Output Short Circuit to V^+	(Note 12)

Operating Ratings

Temperature Range	$-40°C \leq T_J \leq +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.5		μV/°C
I_B	Input Bias Current		0.04	**200**	pA max
I_{OS}	Input Offset Current		0.01	**100**	pA max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 12V$ $V^+ = 15V$	83	63 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V^+ \leq 15V$	83	63 **61**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \leq V^- \leq -10V$	94	74 **73**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.5$**	V min
A_V	Large Signal Voltage Gain	$R_L = 100\ k\Omega$ (Note 7) Sourcing	1000	200 **100**	V/mV min
		Sinking	500	90 **40**	V/mV min
		$R_L = 5\ k\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV min
		Sinking	250	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
V_O	Output Voltage Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.40 **4.43**	V min
			0.004	0.06 **0.09**	V max
		$V^+ = 5V$ $R_L = 5\ k\Omega$ to 2.5V	4.940	4.20 **4.00**	V min
			0.040	0.25 **0.35**	V max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.970	14.00 **13.90**	V min
			0.007	0.06 **0.09**	V max
		$V^+ = 15V$ $R_L = 5\ k\Omega$ to 7.5V	14.840	13.70 **13.50**	V min
			0.110	0.32 **0.40**	V max
I_O	Output Current	$V^+ = 5V$ Sourcing, $V_O = 0V$	22	13 **9**	mA min
		Sinking, $V_O = 5V$ (Note 2)	21	13 **9**	mA min
		$V^+ = 15V$ Sourcing, $V_O = 0V$	40	23 **15**	mA min
		Sinking, $V_O = 13V$ (Note 12)	39	23 **15**	mA min
I_S	Supply Current	Both Amplifiers $V_O = 1.5V$	86	140 **165**	μA max

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless other otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.11	0.05 **0.03**	V/μs min
GBW	Gain-Bandwidth Product		0.35		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	42		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or correlation.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$, and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

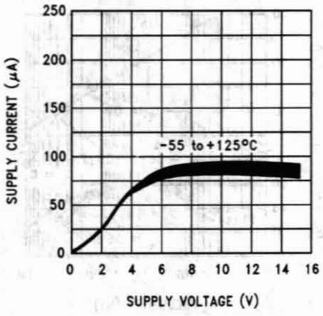
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

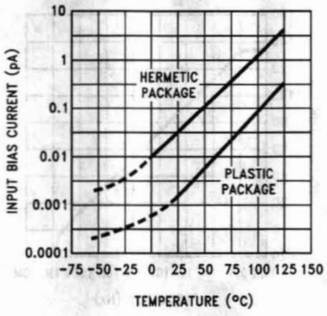
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

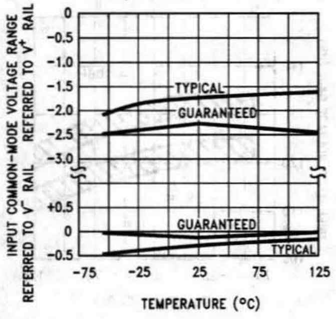
Supply Current vs Supply Voltage



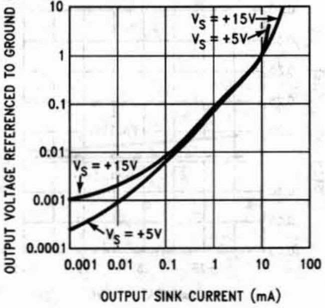
Input Bias Current vs Temperature



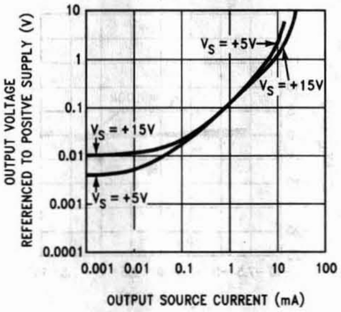
Input Common-Mode Voltage Range vs Temperature



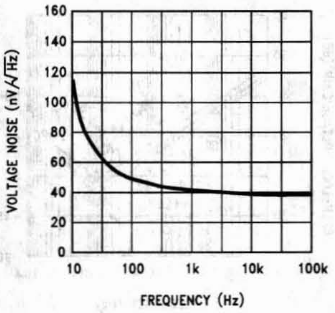
Output Characteristics Current Sinking



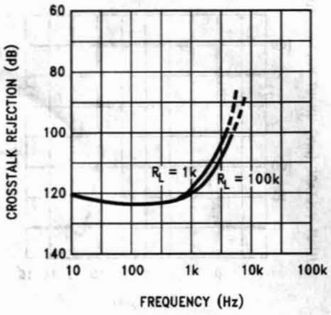
Output Characteristics Current Sourcing



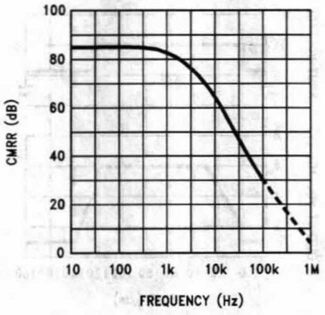
Input Voltage Noise vs Frequency



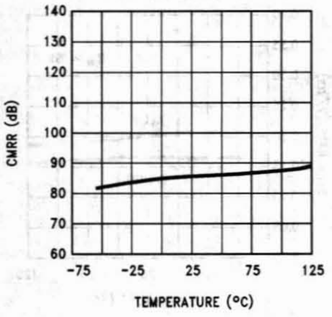
Crosstalk Rejection vs Frequency



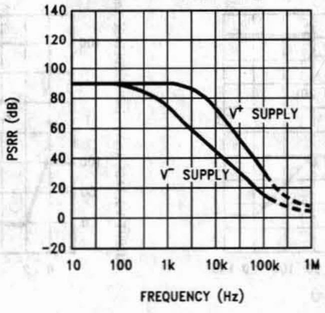
CMRR vs Frequency



CMRR vs Temperature



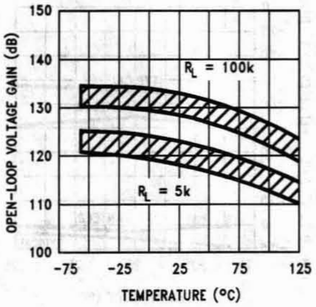
Power Supply Rejection Ratio vs Frequency



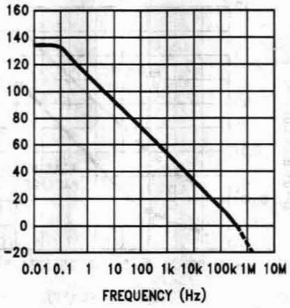
TL/H/11236–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

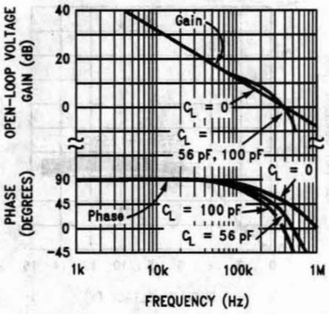
Open-Loop Voltage Gain vs Temperature



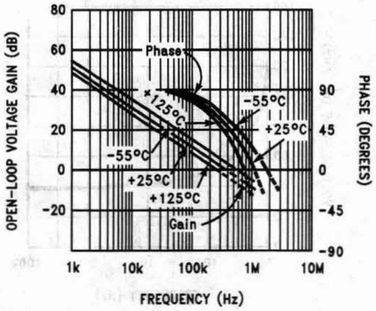
Open-Loop Frequency Response



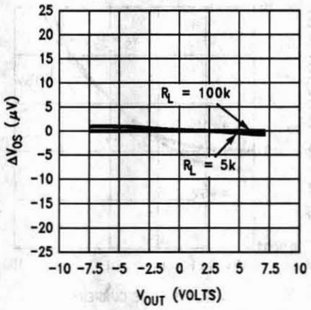
Gain and Phase Responses vs Load Capacitance



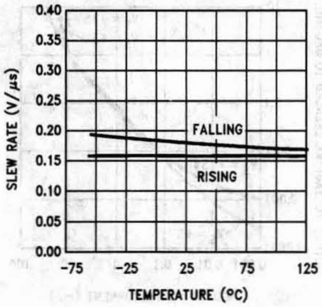
Gain and Phase Responses vs Temperature



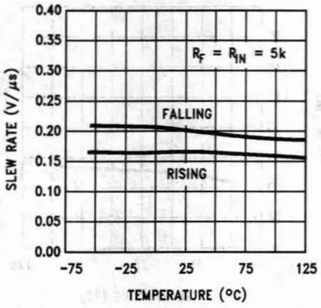
Gain Error (V_{OS} vs V_{OUT})



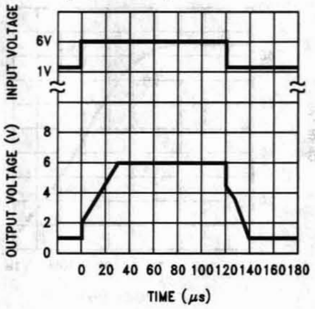
Non-Inverting Slew Rate vs Temperature



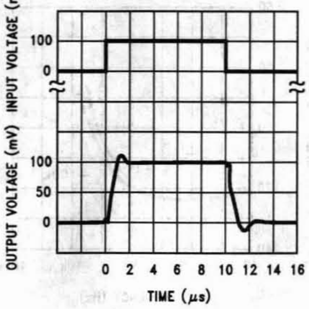
Inverting Slew Rate vs Temperature



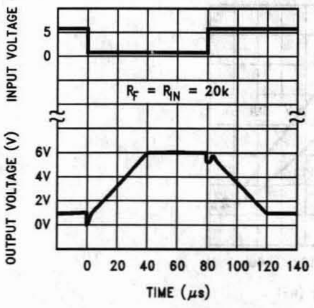
Large-Signal Pulse Non-Inverting Response (A_V = +1)



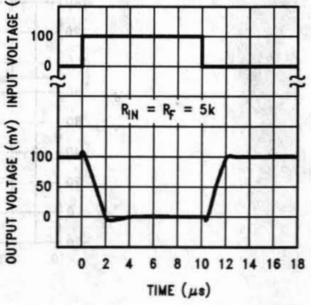
Non-Inverting Small Signal Pulse Response (A_V = +1)



Inverting Large-Signal Pulse Response

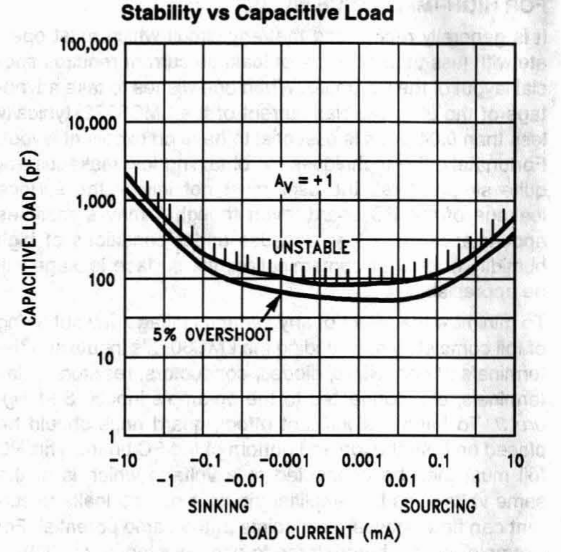


Inverting Small-Signal Pulse Response

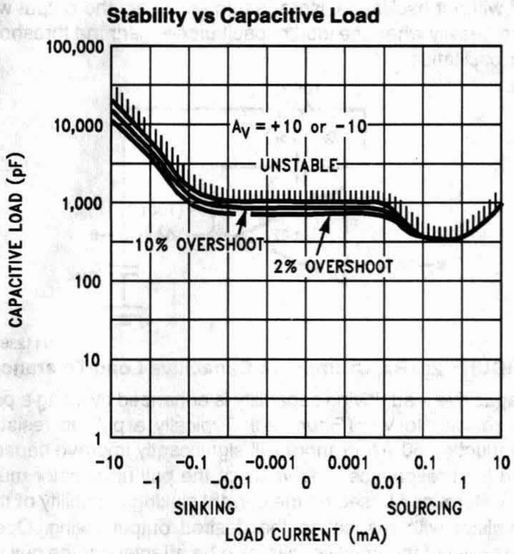


TL/H/11236–3

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ (Continued)



TL/H/11236-4



TL/H/11236-5

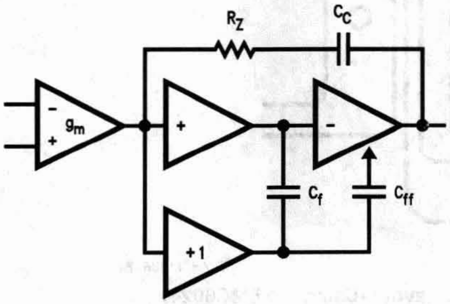
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6022 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/11236-6

FIGURE 1. LMC6022 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6022 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

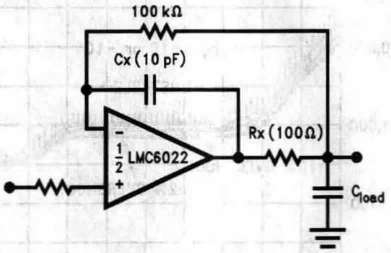


FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V+ (*Figure 2b*). Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

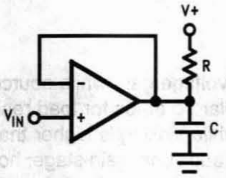


FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6022, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6022's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6022's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 4d*.

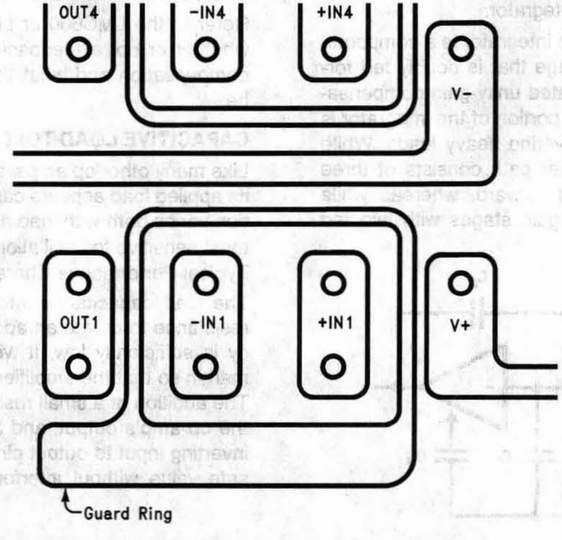
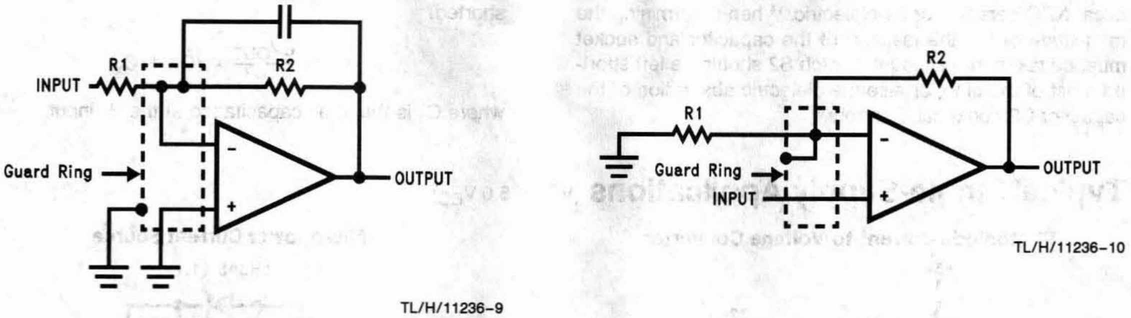


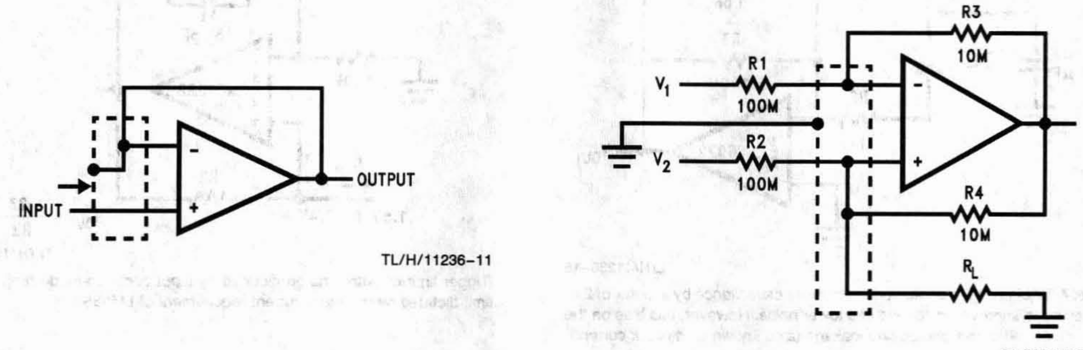
FIGURE 3. Example of Guard Ring in P.C. Board Layout (Using the LMC6024)

Application Hints (Continued)


C1
R1
R2
INPUT
Guard Ring
OUTPUT
TL/H/11236-9
R2
R1
Guard Ring
INPUT
OUTPUT
TL/H/11236-10

(a) Inverting Amplifier

(b) Non-Inverting Amplifier

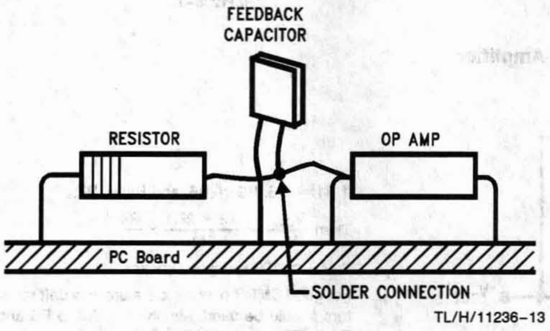

INPUT
OUTPUT
TL/H/11236-11
R3
10M
V_1
R1
100M
R2
V_2
100M
R4
10M
R_L
TL/H/11236-12

(c) Follower

(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.


FEEDBACK
CAPACITOR
RESISTOR
OP AMP
PC Board
SOLDER CONNECTION
TL/H/11236-13

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 6* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^{-} = \frac{dV_{OUT}}{dt} \times C2.$$

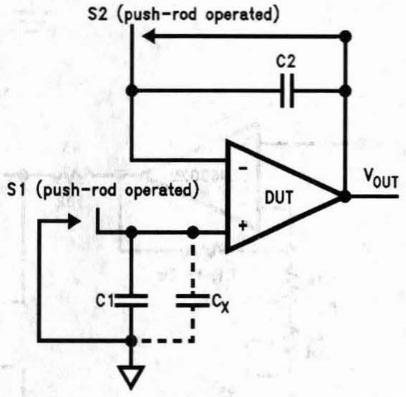

S2 (push-rod operated)
C2
S1 (push-rod operated)
DUT
V_{OUT}
C1
C_X
TL/H/11236-14

FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

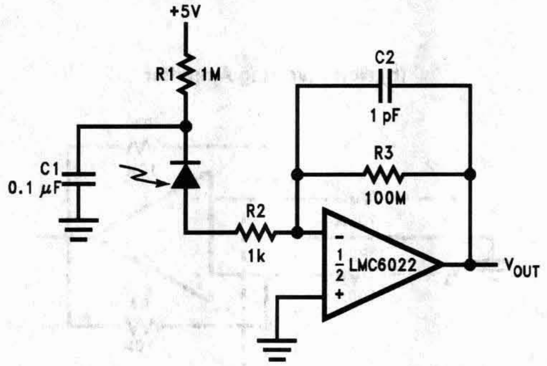
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

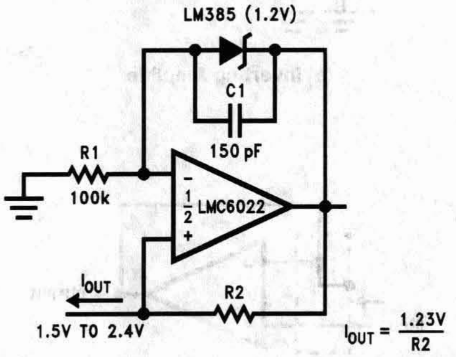
Photodiode Current-to-Voltage Converter


+5V
R1
1M
C2
1 pF
R3
100M
C1
0.1 μF
R2
1k
1/2 LMC6022
VOUT

TL/H/11236–15

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

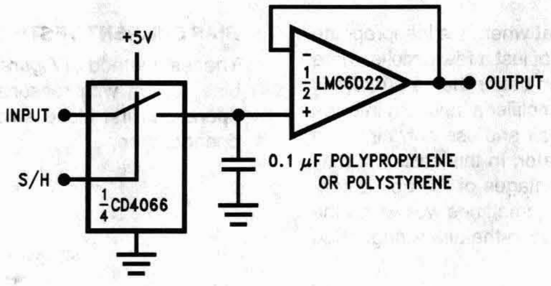
Micropower Current Source


LM385 (1.2V)
C1
150 pF
R1
100k
1/2 LMC6022
IOUT
R2
1.5V TO 2.4V
IOUT = 1.23V / R2

TL/H/11236–16

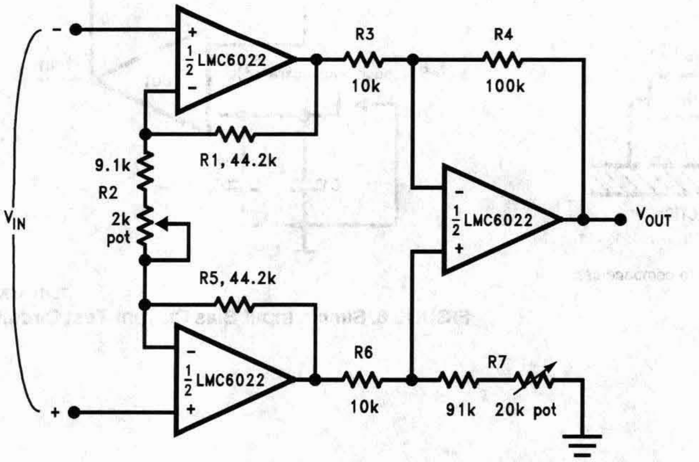
(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold


+5V
INPUT
S/H
1/4 CD4066
1/2 LMC6022
OUTPUT
0.1 μF POLYPROPYLENE OR POLYSTYRENE

TL/H/11236–17

Instrumentation Amplifier


−
+
VIN
1/2 LMC6022
R3
10k
R4
100k
R1, 44.2k
9.1k
R2
2k pot
R5, 44.2k
R6
10k
R7
91k
20k pot
VOUT

If R1 = R5, R3 = R6, and R4 = R7;

Then $\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$

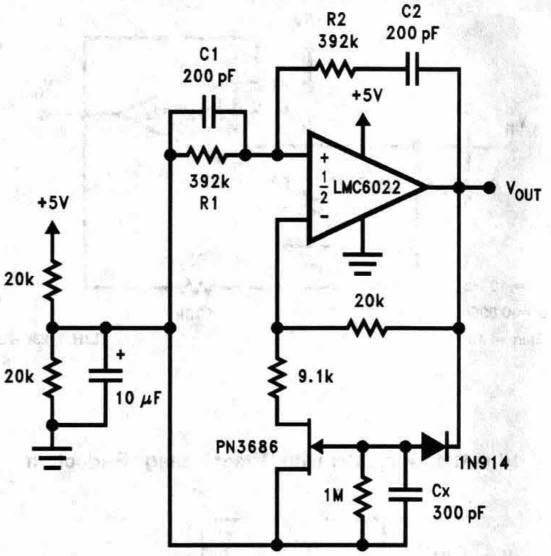
$\therefore A_V \approx 100$ for circuit shown

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

TL/H/11236–18

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Sine-Wave Oscillator


R2
392k
C2
200 pF
C1
200 pF
+5V
392k
R1
+
1/2 LMC6022
−
V_OUT
+5V
20k
20k
20k
+
10 µF
9.1k
PN3686
1N914
1M
Cx
300 pF

TL/H/11236–19

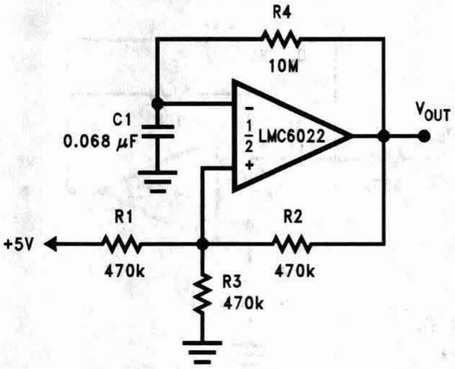
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

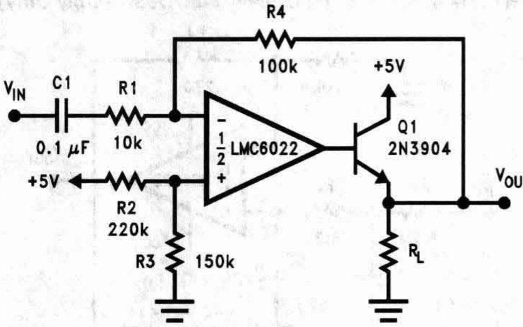
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator


R4
10M
C1
0.068 µF
−
1/2 LMC6022
+
V_OUT
R1
470k
R2
470k
+5V
R3
470k

TL/H/11236–20

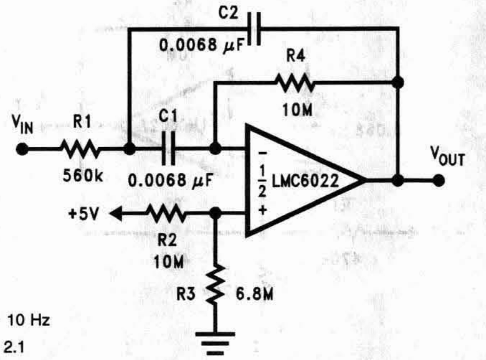
Power Amplifier


R4
100k
+5V
V_IN
C1
0.1 µF
R1
10k
−
1/2 LMC6022
+
Q1
2N3904
+5V
R2
220k
V_OUT
R3
150k
R_L

TL/H/11236–21

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

10 Hz Bandpass Filter


C2
0.0068 μF
R4
10M
V_IN
R1
560k
C1
0.0068 μF
1/2 LMC6022
V_OUT
+5V
R2
10M
R3
6.8M

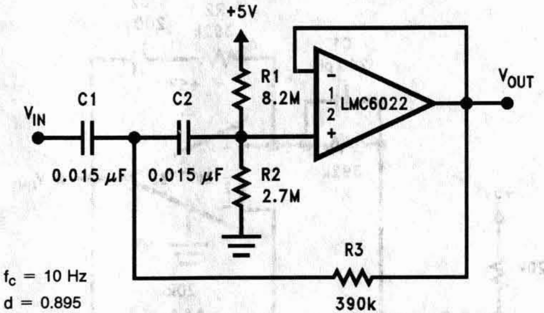
$f_O = 10$ Hz

Q = 2.1

Gain = −8.8

TL/H/11236–22

10 Hz High-Pass Filter (2 dB Dip)


+5V
R1
8.2M
1/2 LMC6022
V_OUT
V_IN
C1
0.015 μF
C2
0.015 μF
R2
2.7M
R3
390k

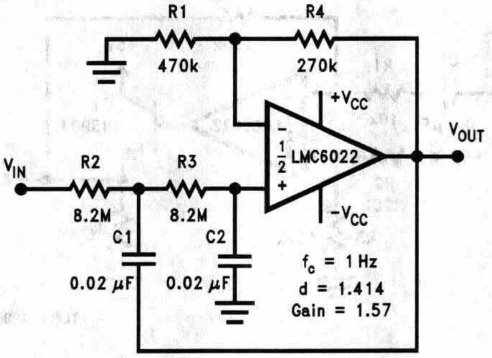
$f_c = 10$ Hz

d = 0.895

Gain = 1

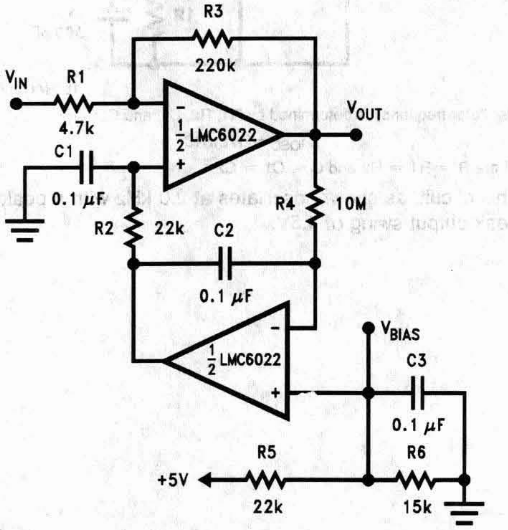
TL/H/11236–23

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)


R1
470k
R4
270k
+V_CC
1/2 LMC6022
V_OUT
V_IN
R2
8.2M
R3
8.2M
−V_CC
C1
0.02 μF
C2
0.02 μF
f_c = 1 Hz
d = 1.414
Gain = 1.57

TL/H/11236–24

High Gain Amplifier with Offset Voltage Reduction


R3
220k
V_IN
R1
4.7k
1/2 LMC6022
V_OUT
C1
0.1 μF
R4
10M
R2
22k
C2
0.1 μF
1/2 LMC6022
V_BIAS
C3
0.1 μF
R5
22k
R6
15k
+5V

Gain = −46.8

TL/H/11236–25

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

National Semiconductor

LMC6024
Low Power CMOS Quad Operational Amplifier

General Description

The LMC6024 is a CMOS quad operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V−, low input bias current and voltage gain (into 100 kΩ and 5 kΩ loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6022 datasheet for a CMOS dual operational amplifier with these same features.

Features

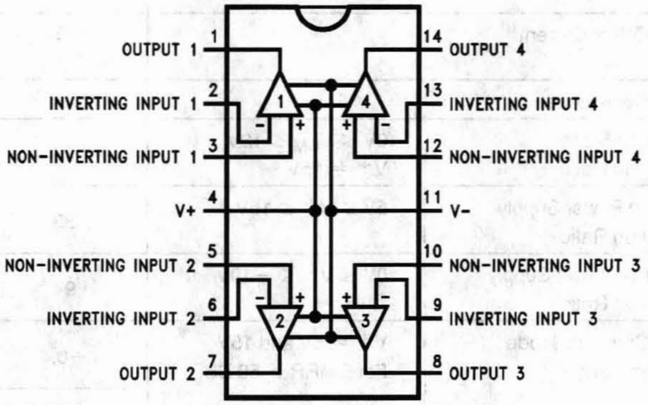
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low offset voltage drift 2.5 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode range includes V−
- Operating range from +5V to +15V supply
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/μs
- Micropower operation 1 mW

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls

Connection Diagram

14-Pin DIP/SO


OUTPUT 1
1
INVERTING INPUT 1
2
NON-INVERTING INPUT 1
3
V+
4
NON-INVERTING INPUT 2
5
INVERTING INPUT 2
6
OUTPUT 2
7
14
OUTPUT 4
13
INVERTING INPUT 4
12
NON-INVERTING INPUT 4
11
V−
10
NON-INVERTING INPUT 3
9
INVERTING INPUT 3
8
OUTPUT 3
1
2
3
4
−
+

Top View

TL/H/11235–1

Ordering Information

Temperature Range	Package	NSC Drawing	Transport Media
Industrial −40°C ≤ T_J ≤ +85°C			
LMC6024IN	14-Pin Molded DIP	N14A	Rail
LMC6024IM	14-Pin Small Outline	M14A	Rail Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Voltage at Output/Input Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Junction Temperature	150°C
ESD Tolerance (Note 4)	1000V
Power Dissipation	(Note 3)

Operating Ratings

Temperature Range	$-40°C \leq T_J \leq +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
14-Pin DIP	85°C/W
14-Pin SO	115°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6024I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV Max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.5		μV/°C
I_B	Input Bias Current		0.04	 **200**	pA Max
I_{OS}	Input Offset Current		0.01	 **100**	pA Max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 12V$ $V^+ = 15V$	83	63 **61**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V^+ \leq 15V$	83	63 **61**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \leq V^- \leq -10V$	94	74 **73**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 DB	−0.4	−0.1 **0**	V Max
			$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V Min
A_V	Large Signal Voltage Gain	$R_L = 100\ k\Omega$ (Note 7) Sourcing	1000	200 **100**	V/mV Min
		Sinking	500	90 **40**	V/mV Min
		$R_L = 5\ k\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV Min
		Sinking	250	50 **20**	V/mV Min

DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6024I Limit (Note 6)	Units
V_O	Output Voltage Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.40 **4.43**	V Min
			0.004	0.06 **0.09**	V Max
		$V^+ = 5V$ $R_L = 5\ k\Omega$ to 2.5V	4.940	4.20 **4.00**	V Min
			0.040	0.25 **0.35**	V Max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.970	14.00 **13.90**	V Min
			0.007	0.06 **0.09**	V Max
		$V^+ = 15V$ $R_L = 5\ k\Omega$ to 7.5V	14.840	13.70 **13.50**	V Min
			0.110	0.32 **0.40**	V Max
I_O	Output Current	$V^+ = 5V$ Sourcing, $V_O = 0V$	22	13 **9**	mA Min
		Sinking $V_O = 5V$ (Note 2)	21	13 **9**	mA Min
		$V^+ = 15V$ Sourcing, $V_O = 0V$	40	23 **15**	mA Min
		Sinking, $V_O = 13V$ (Note 12)	39	23 **15**	mA Min
I_S	Supply Current	All Four Amplifiers $V_O = 1.5V$	160	240 **280**	μA Max

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6024I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.11	0.05 **0.03**	V/μs Min
GBW	Gain-Bandwidth Product		0.35		MHz
θ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	42		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversly affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharge through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or correlation.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$, and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred, $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

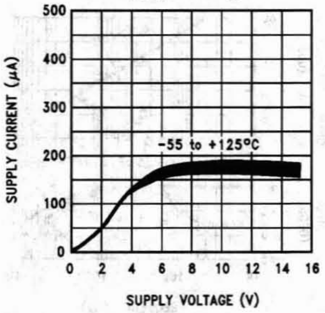
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

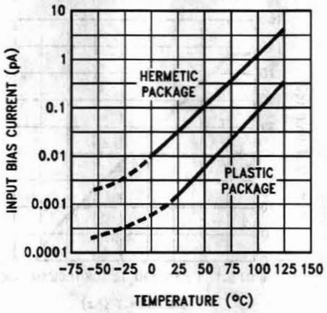
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

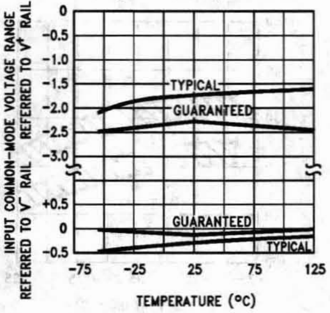
Supply Current vs Supply Voltage



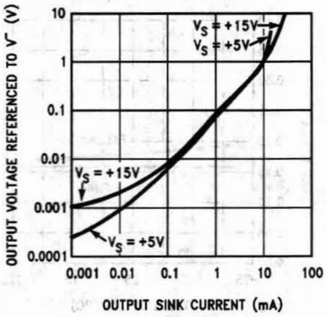
Input Bias Current vs Temperature



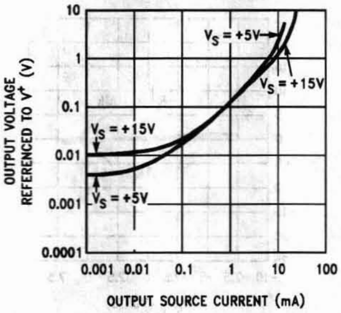
Common-Mode Voltage Range vs Temperature



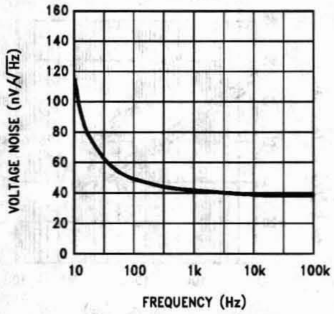
Output Characteristics Current Sinking



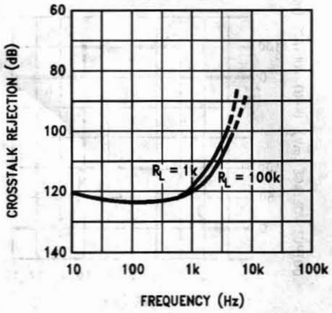
Output Characteristics Current Sourcing



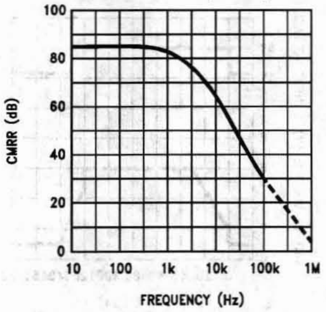
Input Voltage Noise vs Frequency



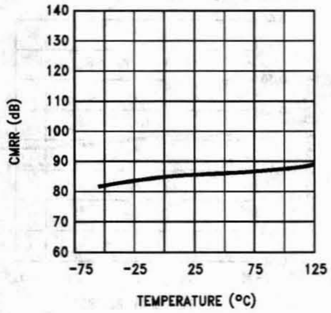
Crosstalk Rejection vs Frequency



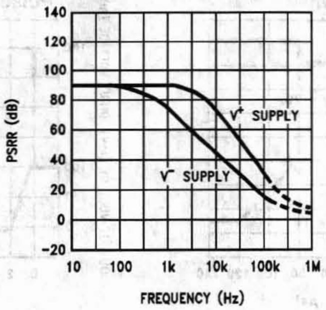
CMRR vs Frequency



CMRR vs Temperature



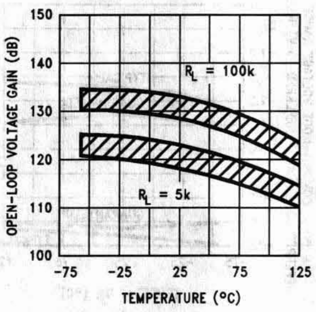
Power Supply Rejection Ratio vs Frequency



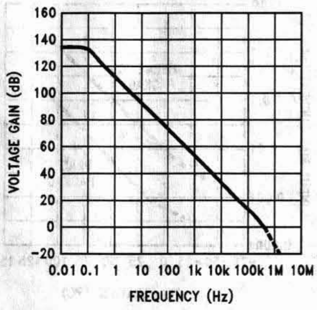
TL/H/11235-2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

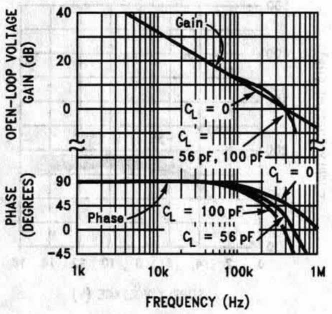
Open-Loop Voltage Gain vs Temperature



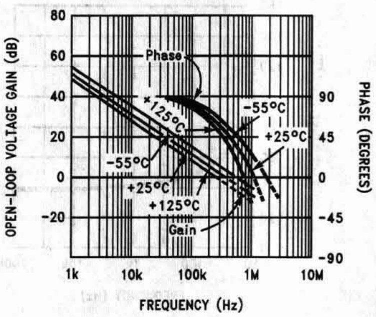
Open-Loop Frequency Response



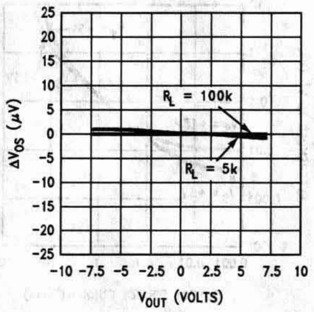
Gain and Phase Responses vs Load Capacitance



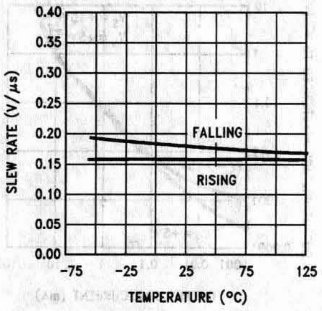
Gain and Phase Responses vs Temperature



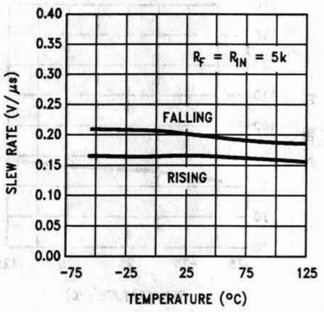
Gain Error (V_{OS} vs V_{OUT})



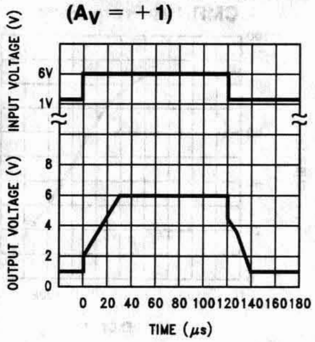
Non-Inverting Slew Rate vs Temperature



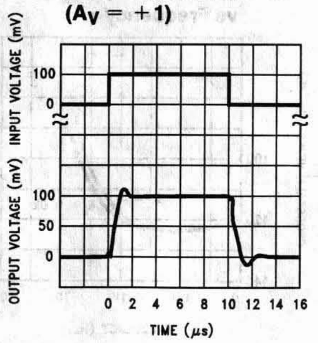
Inverting Slew Rate vs Temperature



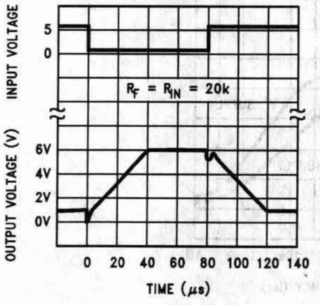
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



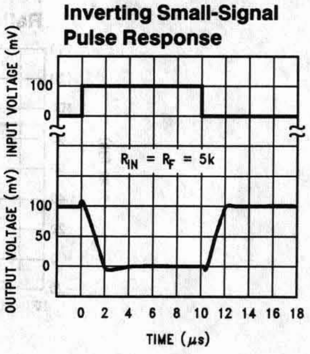
Non-Inverting Small Signal Pulse Response ($A_V = +1$)



Inverting Large-Signal Pulse Response

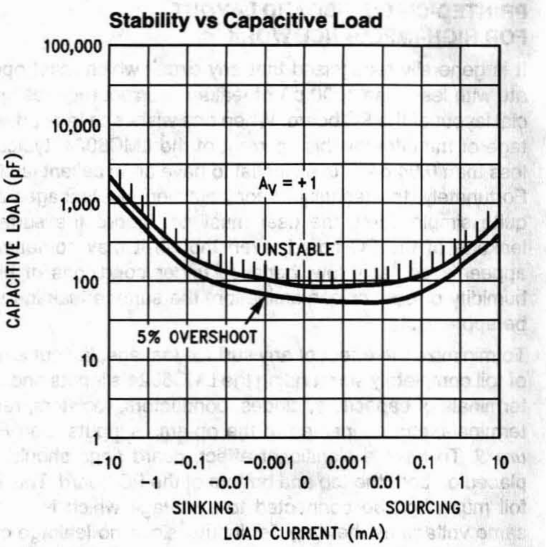


Inverting Small-Signal Pulse Response

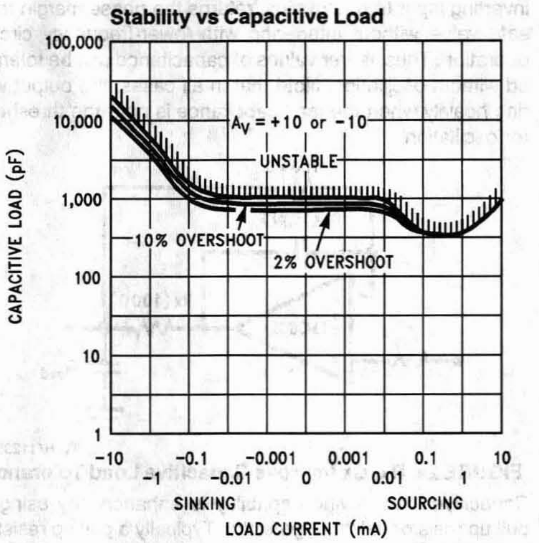


TL/H/11235–3

Typical Performance Characteristics V_S = ±7.5V, T_A = 25°C unless otherwise specified (Continued)


Stability vs Capacitive Load

TL/H/11235-4


Stability vs Capacitive Load

TL/H/11235-5

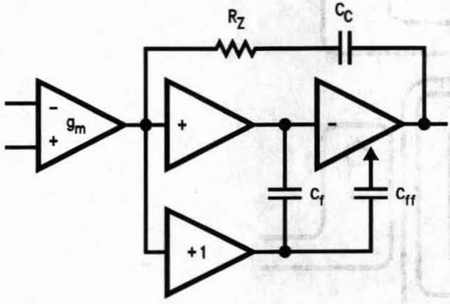
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6024 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/11235-6

FIGURE 1. LMC6024 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characterisitics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6024 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from

Application Hints (Continued)

inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capcitance is near the threshold for oscillation.

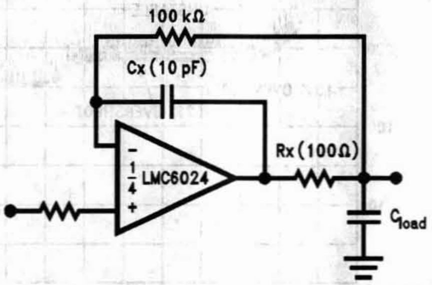


FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 2b)*. Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

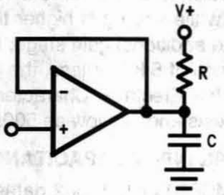


FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6024, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6024's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6024's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 4d*.

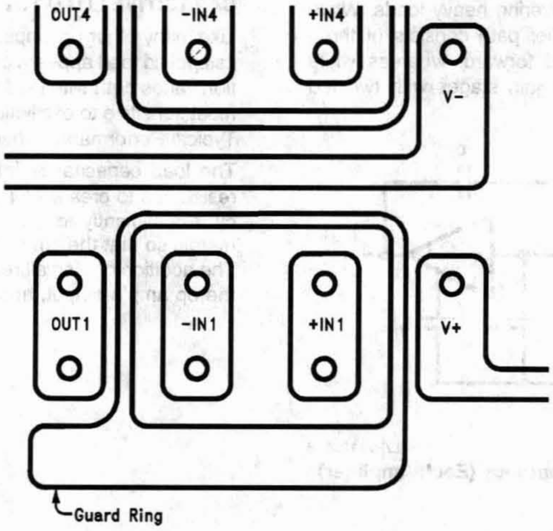
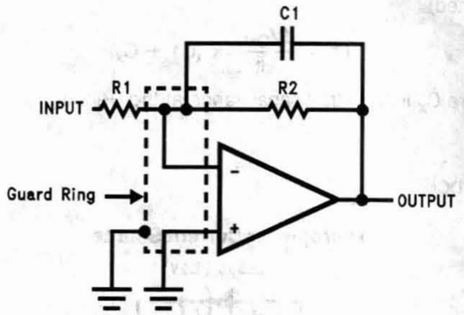


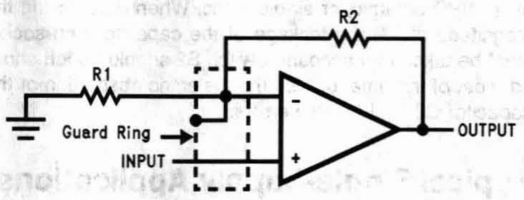
FIGURE 3. Example of Guard Ring in P.C. Board Layout (Using the LMC6024)

Application Hints (Continued)


C1
R1
R2
INPUT
Guard Ring
OUTPUT
-
+

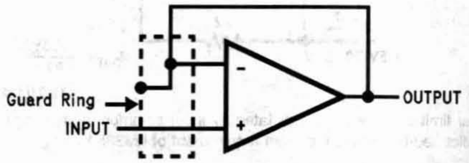
TL/H/11235-9

(a) Inverting Amplifier


R2
R1
Guard Ring
INPUT
OUTPUT
-
+

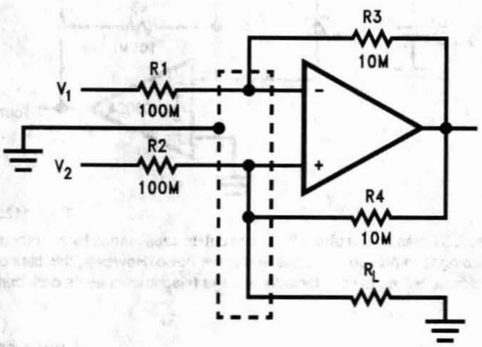
TL/H/11235-10

(b) Non-Inverting Amplifier


Guard Ring
INPUT
OUTPUT
-
+

TL/H/11235-11

(c) Follower

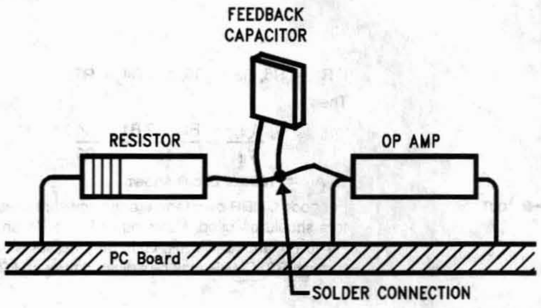

R3
10M
V1
R1
100M
R2
V2
100M
R4
10M
RL
-
+

TL/H/11235-12

(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.


FEEDBACK CAPACITOR
RESISTOR
OP AMP
PC Board
SOLDER CONNECTION

TL/H/11235-13

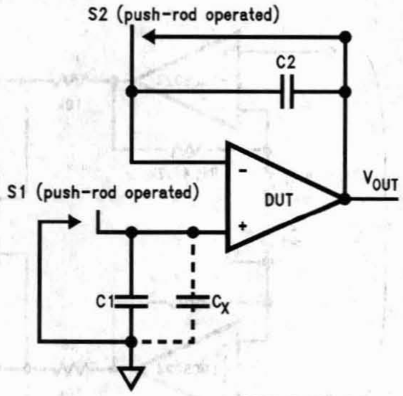
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 6* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^{-} = \frac{dV_{OUT}}{dt} \times C2.$$


S2 (push-rod operated)
C2
S1 (push-rod operated)
DUT
VOUT
C1
CX
-
+

TL/H/11235-14

FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

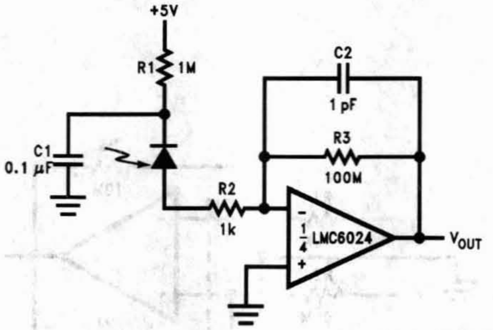
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

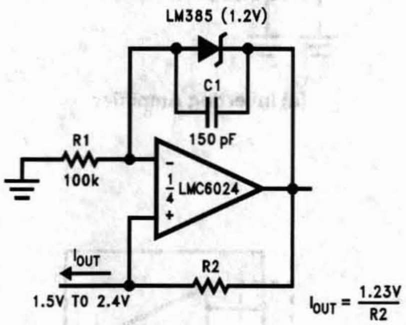
Photodiode Current-to-Voltage Converter


+5V
R1
1M
C2
1 pF
R3
100M
C1
0.1 µF
R2
1k
$\frac{1}{4}$ LMC6024
V_{OUT}

TL/H/11235–15

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

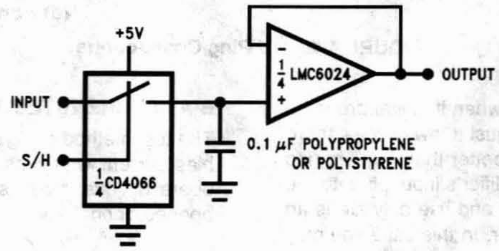
Micropower Current Source


LM385 (1.2V)
C1
150 pF
R1
100k
$\frac{1}{4}$ LMC6024
I_{OUT}
R2
1.5V TO 2.4V
$I_{OUT} = \frac{1.23V}{R2}$

TL/H/11235–16

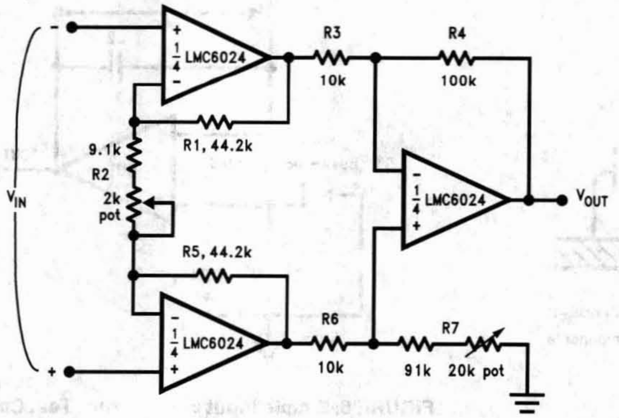
(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold


+5V
INPUT
S/H
$\frac{1}{4}$CD4066
$\frac{1}{4}$ LMC6024
OUTPUT
0.1 µF POLYPROPYLENE
OR POLYSTYRENE

TL/H/11235–17

Instrumentation Amplifier


−
+
V_{IN}
$\frac{1}{4}$ LMC6024
R3
10k
R4
100k
R1, 44.2k
9.1k
R2
2k
pot
R5, 44.2k
R6
10k
R7
91k
20k pot
V_{OUT}

If R1 = R5, R3 = R6, and R4 = R7;
Then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2\,R1}{R2} \times \frac{R4}{R3}$$

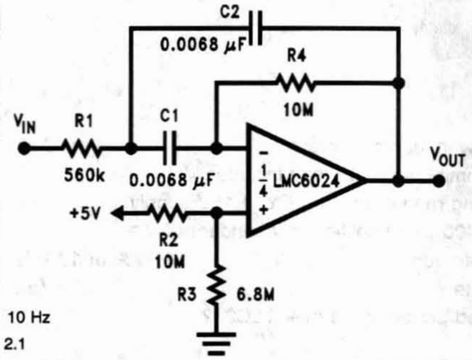
$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

TL/H/11235–18

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

10 Hz Bandpass Filter


C2
0.0068 μF
R4
10M
VIN
R1
560k
C1
0.0068 μF
VOUT
1/4 LMC6024
+5V
R2
10M
R3
6.8M

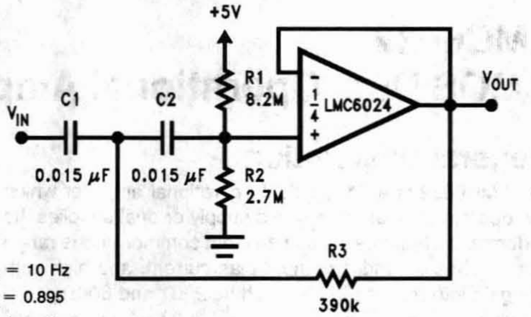
$f_O = 10$ Hz

$Q = 2.1$

Gain = −8.8

TL/H/11235–19

10 Hz High-Pass Filter (2 dB Dip)


+5V
R1
8.2M
VOUT
1/4 LMC6024
VIN
C1
C2
0.015 μF
0.015 μF
R2
2.7M
R3
390k

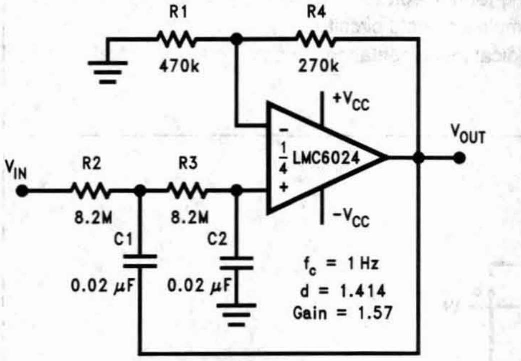
$f_c = 10$ Hz

$d = 0.895$

Gain = 1

TL/H/11235–20

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)


R1
470k
R4
270k
+VCC
VOUT
1/4 LMC6024
−VCC
VIN
R2
8.2M
R3
8.2M
C1
0.02 μF
C2
0.02 μF

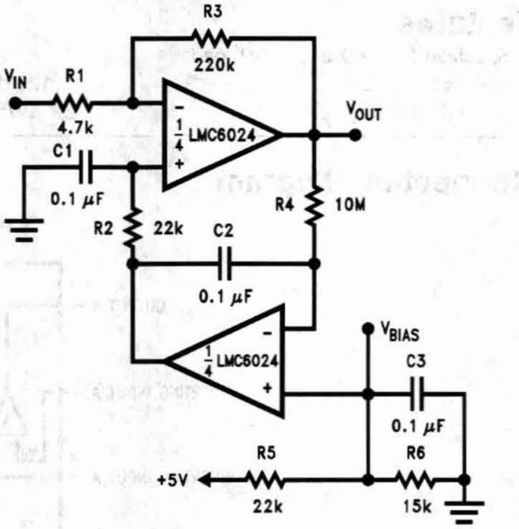
$f_c = 1$ Hz

$d = 1.414$

Gain = 1.57

TL/H/11235–21

High Gain Amplifier with Offset Voltage Reduction


R3
220k
VIN
R1
4.7k
VOUT
1/4 LMC6024
C1
0.1 μF
R4
10M
R2
22k
C2
0.1 μF
1/4 LMC6024
VBIAS
C3
0.1 μF
R5
22k
+5V
R6
15k

Gain = −46.8

TL/H/11235–22

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

National Semiconductor

LMC6032
CMOS Dual Operational Amplifier

General Description

The LMC6032 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches ground, low input bias current, and high voltage gain into realistic loads, such as 2 kΩ and 600Ω.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6034 datasheet for a CMOS quad operational amplifier with these same features. For higher performance characteristics refer to the LMC662.

Features

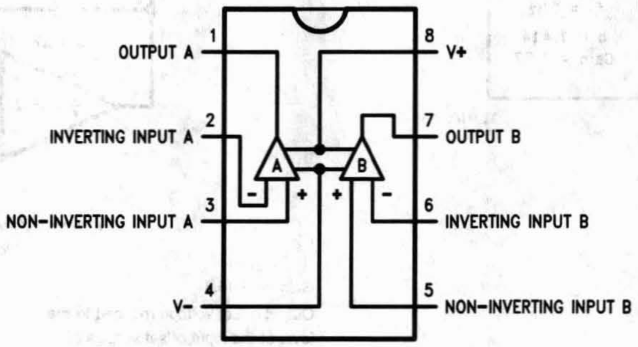
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low offset voltage drift 2.3 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode range includes V$^-$
- Operating range from +5V to +15V supply
- I_{SS} = 400 μA/amplifier; independent of V$^+$
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Improved performance over TLC272

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Medical instrumentation

Connection Diagram

8-Pin DIP/SO



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Top View

Ordering Information

Temperature Range Industrial −40°C ≤ T_J ≤ +85°C	Package	NSC Drawing	Transport Media
LMC6032IN	8-Pin Molded DIP	N08E	Rail
LMC6032IM	8-Pin Small Outline	M08A	Rail Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	1000V
Power Dissipation	(Note 3)
Voltage at Output/Input Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA

Operating Ratings (Note 1)

Temperature Range	$-40°C \leq T_J \leq +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 11)
Thermal Resistance (θ_{JA}), (Note 12)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = 1.5V$, $V_{OUT} = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6032I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.3		μV/°C
I_B	Input Bias Current		0.04	**200**	pA max
I_{OS}	Input Offset Current		0.01	**100**	pA max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 12V$ $V^+ = 15V$	83	63 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V^+ \leq 15V$ $V_O = 2.5V$	83	63 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \leq V^- \leq -10V$	94	74 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ **V^+ − 2.6**	V min
A_V	Large Signal Voltage Gain	$R_L = 2\ k\Omega$ (Note 7) Sourcing	2000	200 **100**	V/mV min
		Sinking	500	90 **40**	V/mV min
		$R_L = 600\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV min
		Sinking	250	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = 1.5V$, $V_{OUT} = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6032I Limit (Note 6)	Units
V_O	Output Voltage Swing	$V^+ = 5V$ $R_L = 2\ k\Omega$ to 2.5V	4.87	4.20 **4.00**	V min
			0.10	0.25 **0.35**	V max
		$V^+ = 5V$ $R_L = 600\Omega$ to 2.5V	4.61	4.00 **3.80**	V min
			0.30	0.63 **0.75**	V max
		$V^+ = 15V$ $R_L = 2\ k\Omega$ to 7.5V	14.63	13.50 **13.00**	V min
			0.26	0.45 **0.55**	V max
		$V^+ = 15V$ $R_L = 600\Omega$ to 7.5V	13.90	12.50 **12.00**	V min
			0.79	1.45 **1.75**	V max
I_O	Output Current	$V^+ = 5V$ Sourcing, $V_O = 0V$	22	13 **9**	mA min
		Sinking, $V_O = 5V$	21	13 **9**	mA min
		$V^+ = 15V$ Sourcing, $V_O = 0V$	40	23 **15**	mA min
		Sinking, $V_O = 13V$ (Note 10)	39	23 **15**	mA min
I_S	Supply Current	Both Amplifiers $V_O = 1.5V$	0.75	1.6 **1.9**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = 1.5V$, $V_{OUT} = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6032I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.1	0.8 **0.4**	V/μs min
GBW	Gain-Bandwidth Product		1.4		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		$pA/\sqrt{Hz}$
THD	Total Harmonic Distortion	F = 10 kHz, $A_V = -10$ $R_L = 2\ k\Omega$, $V_O = 8\ V_{PP}$ ±5V Supply	0.01		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$, and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. $V^+ = 15V$ and $R_L = 10\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

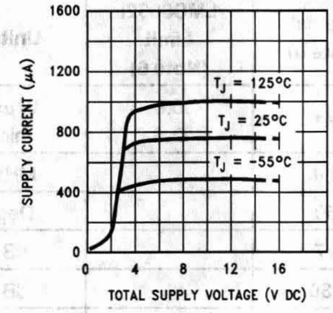
Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability may be adversely affected.

Note 11: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

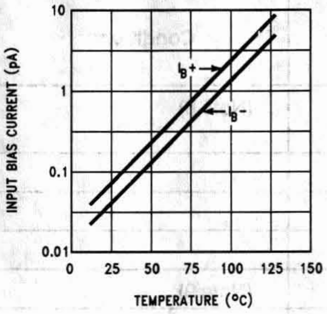
Note 12: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

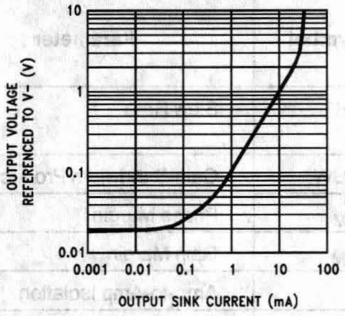
Supply Current vs Supply Voltage



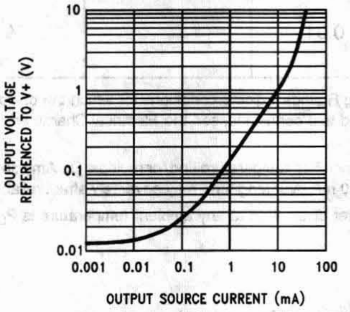
Input Bias Current



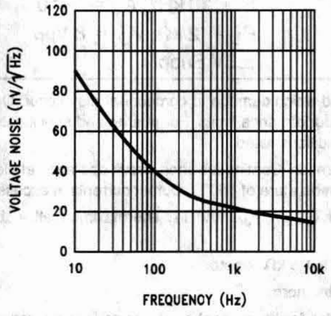
Output Characteristics Current Sinking



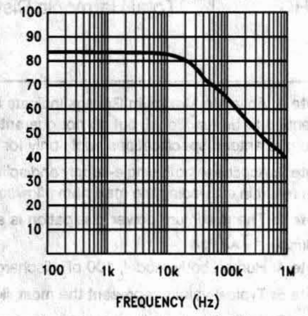
Output Characteristics Current Sourcing



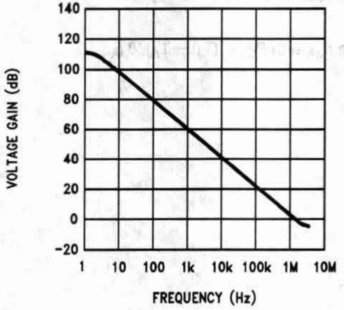
Input Voltage Noise vs Frequency



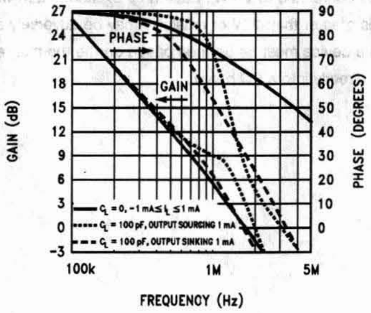
CMRR vs Frequency



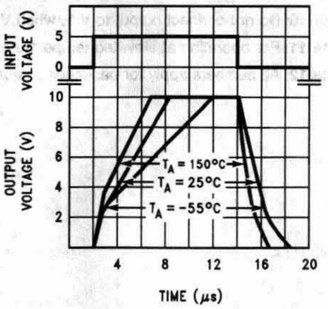
Open-Loop Frequency Response



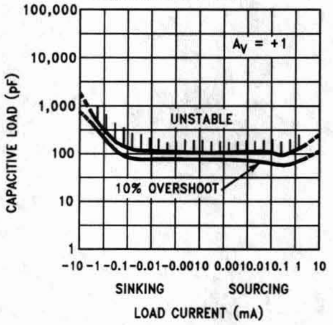
Frequency Response vs Capacitive Load



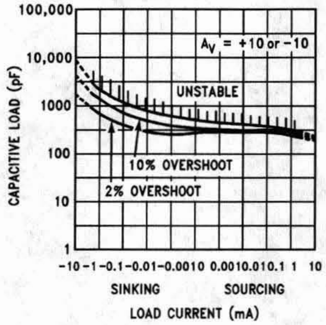
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



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Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6032, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow a larger output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

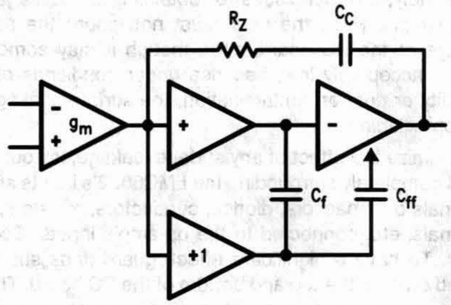

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FIGURE 1. LMC6032 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC6032 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier Circuit, *Figure 2*, the frequency of this pole is

$$f_P = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability, a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

regardless of whether the amplifier is being used in an inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S},$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}.$$

Application Hints (Continued)

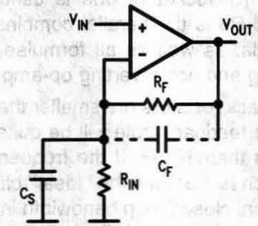

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FIGURE 2. General Operational Amplifier Circuit

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistor.

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the value of C_F should be checked on the actual circuit, starting with the computed value.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6032 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 3a*, the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

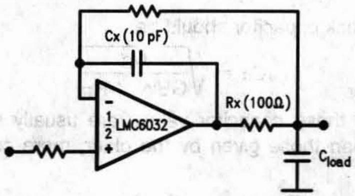

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FIGURE 3a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V+ (*Figure 3b*). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

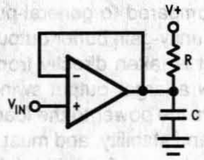

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FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6032, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6032's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 4*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6032's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 5a, 5b, 5c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 5d*.

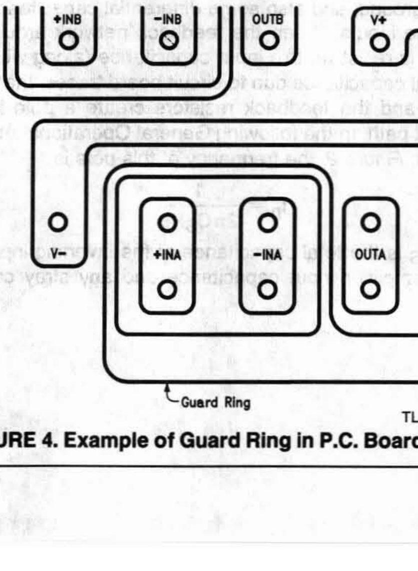

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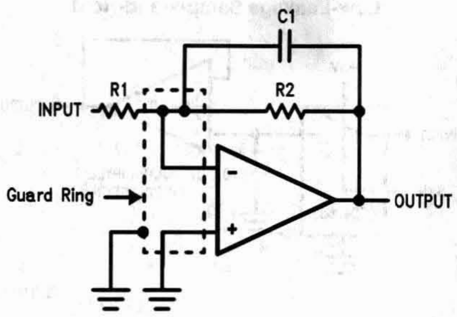
FIGURE 4. Example of Guard Ring in P.C. Board Layout

Application Hints (Continued)


C1
R1
R2
INPUT
Guard Ring
OUTPUT

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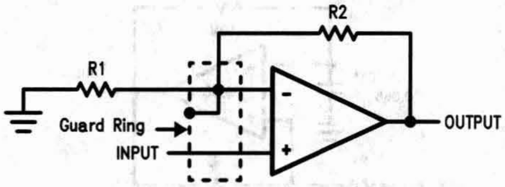
(a) Inverting Amplifier


R2
R1
Guard Ring
INPUT
OUTPUT

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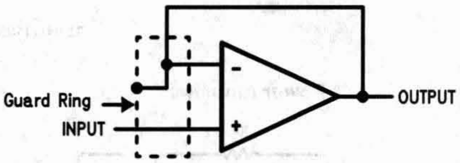
(b) Non-Inverting Amplifier


Guard Ring
INPUT
OUTPUT

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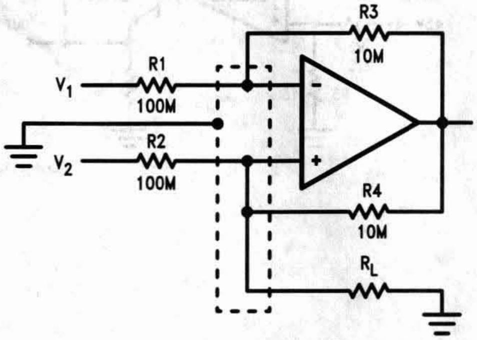
(c) Follower


R3
10M
R1
V_1
100M
R2
V_2
100M
R4
10M
R_L

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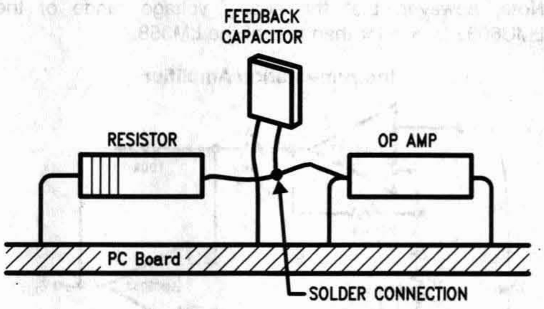
(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.


FEEDBACK CAPACITOR
RESISTOR
OP AMP
PC Board
SOLDER CONNECTION

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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b^- = \frac{dV_{OUT}}{dt} \times C2.$$

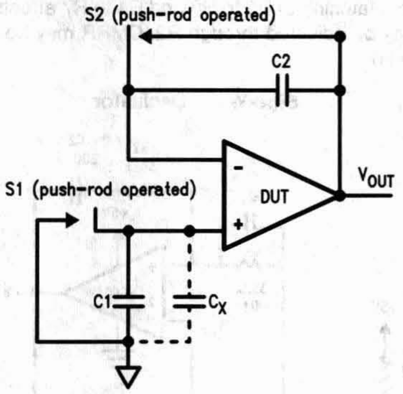
S2 (push-rod operated)
C2
S1 (push-rod operated)
DUT
V_{OUT}
C1
C_X

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FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

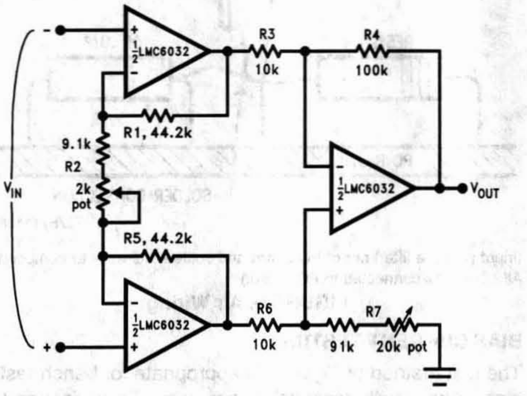
$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Additional single-supply applications ideas can be found in the LM358 datasheet. The LMC6032 is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC6032 is smaller than that of the LM358.

Instrumentation Amplifier



$\frac{1}{2}$LMC6032
R3
10k
R4
100k
R1, 44.2k
9.1k
R2
2k pot
V_{IN}
R5, 44.2k
R6
10k
R7
91k
20k pot
V_{OUT}

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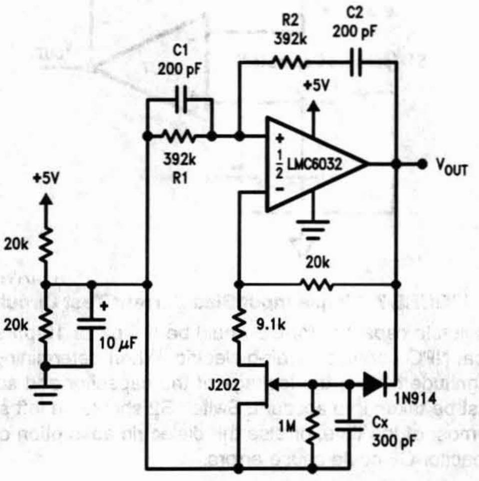
$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3} \quad \text{if } R1 = R5;\ R3 = R6,\ \text{and } R4 = R7.$$

$$= 100 \text{ for circuit shown.}$$

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator



R2
392k
C2
200 pF
C1
200 pF
+5V
392k
R1
$\frac{1}{2}$ LMC6032
V_{OUT}
+5V
20k
20k
10 μF
20k
9.1k
J202
1N914
1M
Cx
300 pF

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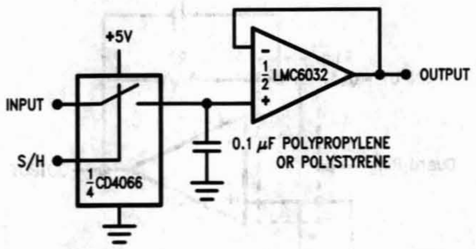
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.0V.

Low-Leakage Sample-and-Hold



+5V
INPUT
S/H
$\frac{1}{4}$CD4066
$\frac{1}{2}$ LMC6032
OUTPUT
0.1 μF POLYPROPYLENE OR POLYSTYRENE

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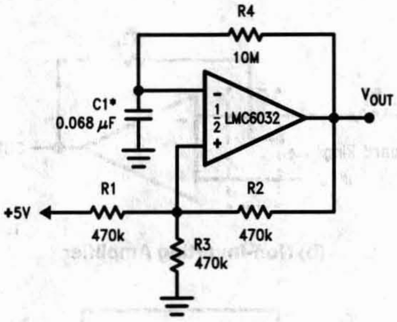
1 Hz Square-Wave Oscillator



R4
10M
C1*
0.068 μF
$\frac{1}{2}$ LMC6032
V_{OUT}
R1
470k
R2
470k
+5V
R3
470k

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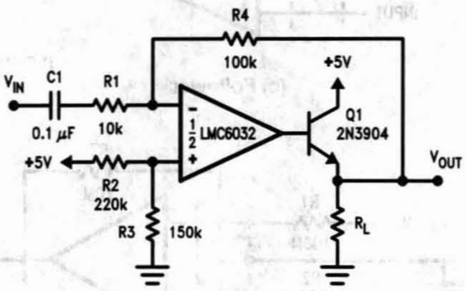
Power Amplifier



R4
100k
+5V
V_{IN}
C1
0.1 μF
R1
10k
$\frac{1}{2}$ LMC6032
Q1
2N3904
V_{OUT}
+5V
R2
220k
R3
150k
R_L

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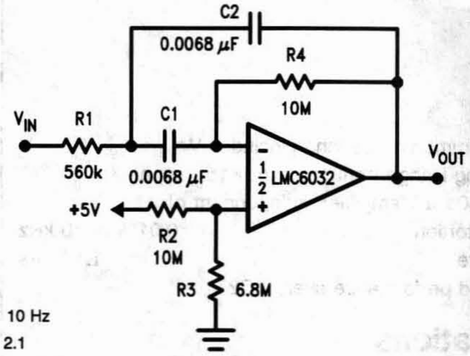
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

10 Hz Bandpass Filter


C2
0.0068 μF
R4
10M
V_{IN}
R1
560k
C1
0.0068 μF
$\frac{1}{2}$ LMC6032
V_{OUT}
+5V
R2
10M
R3
6.8M

$f_O = 10$ Hz
Q = 2.1
Gain = −8.8

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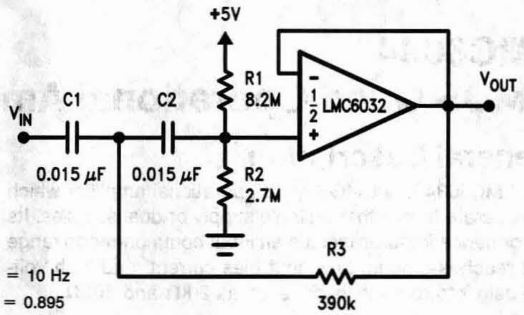
10 Hz High-Pass Filter


+5V
R1
8.2M
V_{OUT}
V_{IN}
C1
0.015 μF
C2
0.015 μF
R2
2.7M
$\frac{1}{2}$ LMC6032
R3
390k

$f_c = 10$ Hz
d = 0.895
Gain = 1
2 dB passband ripple

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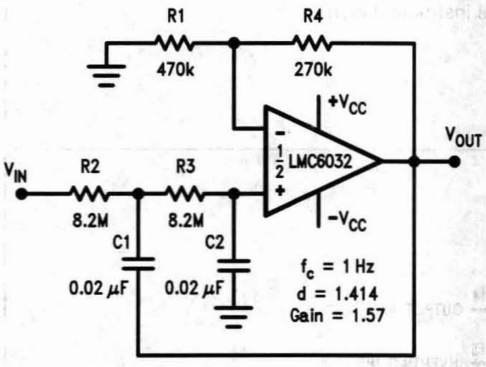
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)


R1
470k
R4
270k
$+V_{CC}$
V_{OUT}
V_{IN}
R2
8.2M
R3
8.2M
$\frac{1}{2}$ LMC6032
$-V_{CC}$
C1
0.02 μF
C2
0.02 μF

$f_c = 1$ Hz
d = 1.414
Gain = 1.57

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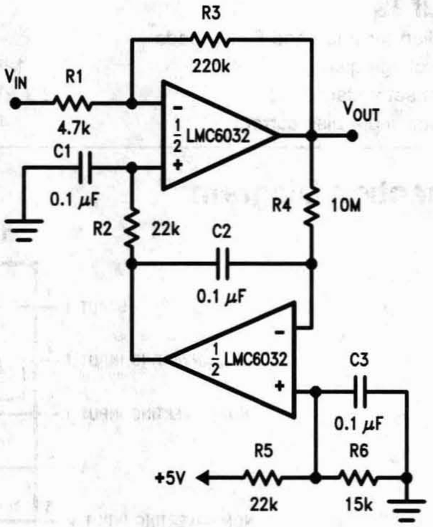
High Gain Amplifier with Offset Voltage Reduction


R3
220k
V_{IN}
R1
4.7k
$\frac{1}{2}$ LMC6032
V_{OUT}
C1
0.1 μF
R4
10M
R2
22k
C2
0.1 μF
$\frac{1}{2}$ LMC6032
C3
0.1 μF
R5
22k
R6
15k
+5V

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Gain = −46.8
Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

National Semiconductor

LMC6034
CMOS Quad Operational Amplifier

General Description

The LMC6034 is a CMOS quad operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches ground, low input bias current, and high voltage gain into realistic loads, such as 2 kΩ and 600Ω.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6032 datasheet for a CMOS dual operational amplifier with these same features. For higher performance characteristics refer to the LMC660.

Features

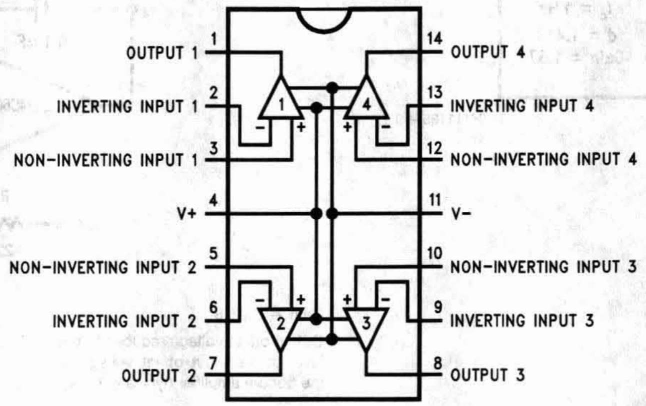
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low offset voltage drift 2.3 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode range includes V−
- Operating Range from +5V to +15V supply
- I_{SS} = 400 μA/amplifier; independent of V+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Improved performance over TLC274

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Medical instrumentation

Connection Diagram

14-Pin DIP/SO


OUTPUT 1
INVERTING INPUT 1
NON-INVERTING INPUT 1
V+
NON-INVERTING INPUT 2
INVERTING INPUT 2
OUTPUT 2
1
2
3
4
5
6
7
14
13
12
11
10
9
8
OUTPUT 4
INVERTING INPUT 4
NON-INVERTING INPUT 4
V−
NON-INVERTING INPUT 3
INVERTING INPUT 3
OUTPUT 3
1
2
3
4
−
+

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Top View

Ordering Information

Temperature Range Industrial −40°C ≤ T_J ≤ +85°C	Package	NSC Drawing	Transport Media
LMC6034IN	14-Pin Molded DIP	N14A	Rail
LMC6034IM	14-Pin Small Outline	M14A	Rail Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Volt)age
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	(Note 3)
Voltage at Output/Input Pin	(V^+) +0.3V, (V^-) −0.3V
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Junction Temperature (Note 3)	150°C
ESD Tolerance (Note 4)	1000V

Operating Ratings (Note 1)

Temperature Range	$-40°C \le T_J \le +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 11)
Thermal Resistance (θ_{JA}), (Note 12)	
14-Pin DIP	85°C/W
14-Pin SO	115°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = 1.5V$, $V_{OUT} = 2.5V$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6034I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.3		μV/°C
I_B	Input Bias Current		0.04	**200**	pA max
I_{OS}	Input Offset Current		0.01	**100**	pA max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$ $V^+ = 15V$	83	63 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	63 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ **V^+ − 2.6**	V min
A_V	Large Signal Voltage Gain	$R_L = 2\ k\Omega$ (Note 7) Sourcing	2000	200 **100**	V/mV min
		Sinking	500	90 **40**	V/mV min
		$R_L = 600\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV min
		Sinking	250	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = 1.5V$, $V_{OUT} = 2.5V$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6034I Limit (Note 6)	Units
V_O	Output Voltage Swing	$V^+ = 5V$ $R_L = 2\ k\Omega$ to 2.5V	4.87	4.20 **4.00**	V min
			0.10	0.25 **0.35**	V max
		$V^+ = 5V$ $R_L = 600\Omega$ to 2.5V	4.61	4.00 **3.80**	V min
			0.30	0.63 **0.75**	V max
		$V^+ = 15V$ $R_L = 2\ k\Omega$ to 7.5V	14.63	13.50 **13.00**	V min
			0.26	0.45 **0.55**	V max
		$V^+ = 15V$ $R_L = 600\Omega$ to 7.5V	13.90	12.50 **12.00**	V min
			0.79	1.45 **1.75**	V max
I_O	Output Current	$V^+ = 5V$ Sourcing, $V_O = 0V$	22	13 **9**	mA min
		Sinking, $V_O = 5V$	21	13 **9**	mA min
		$V^+ = 15V$ Sourcing, $V_O = 0V$	40	23 **15**	mA min
		Sinking, $V_O = 13V$ (Note 10)	39	23 **15**	mA min
I_S	Supply Current	All Four Amplifiers $V_O = 1.5V$	1.5	2.7 **3.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = 1.5V$, $V_{OUT} = 2.5V$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6034I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.1	0.8 **0.4**	V/μs min
GBW	Gain-Bandwidth Product		1.4		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		$pA/\sqrt{Hz}$
THD	Total Harmonic Distortion	$F = 10 kHz, A_V = -10$ $R_L = 2 k\Omega, V_O = 8 V_{PP}$ ±5V Supply	0.01		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$, and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. $V^+ = 15V$ and $R_L = 10 k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13 V_{PP}$.

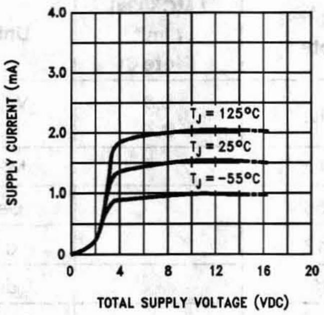
Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability may be adversely affected.

Note 11: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

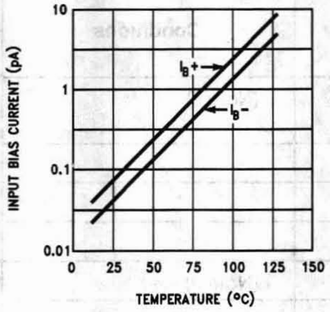
Note 12: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

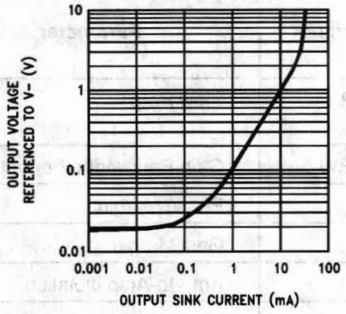
Supply Current vs Supply Voltage



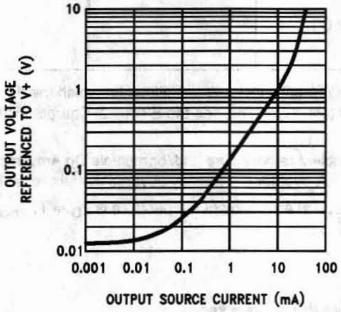
Input Bias Current



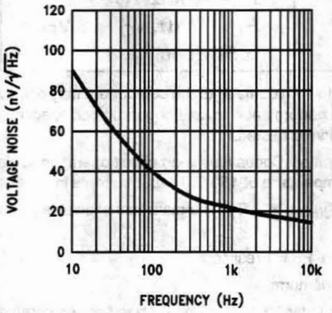
Output Characteristics Current Sinking



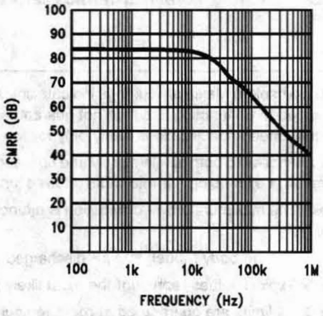
Output Characteristics Current Sourcing



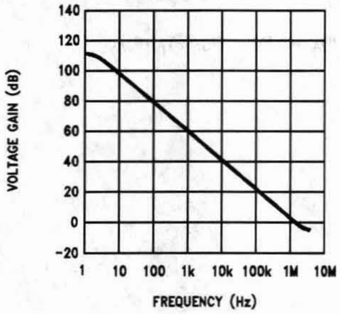
Input Voltage Noise vs Frequency



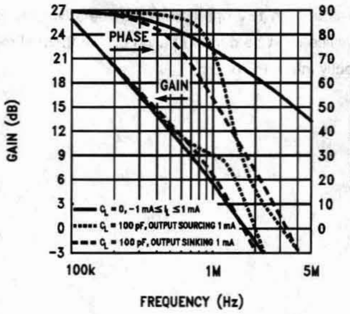
CMRR vs Frequency



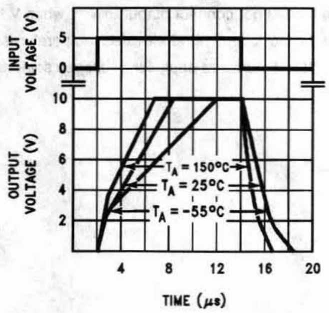
Open-Loop Frequency Response



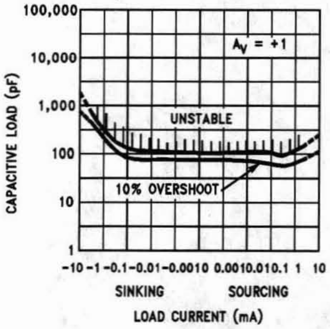
Frequency Response vs Capacitive Load



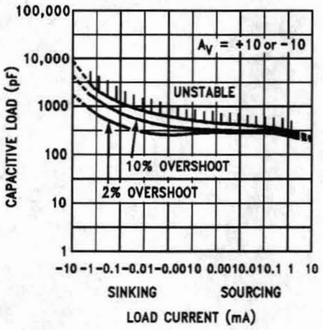
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



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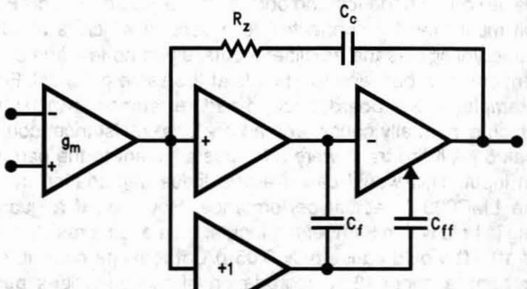
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Applications Hint

Amplifier Topolgy

The topology chosen for the LMC6034, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow a larger output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and Cff) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/11134-3

FIGURE 1. LMC6034 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

Compensating Input Capacitance

The high input resistance of the LMC6034 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit, *Figure 2* the frequency of this pole is

$$fp = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capcitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where $\left(\frac{R_F}{R_{IN}} + 1\right)$ is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula $\left(\frac{R_F}{R_{IN}} + 1\right)$ regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

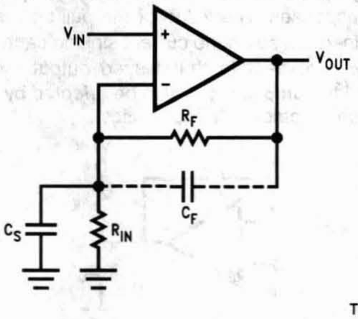
$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S}$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$



TL/H/11134-4

FIGURE 2. General Operational Amplifier Circuit

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

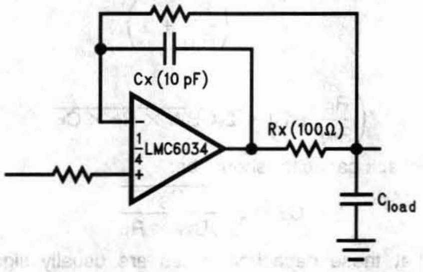
Applications Hint (Continued)

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

Capacitive Load Tolerance

Like many other op amps, the LMC6034 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See Typical Performance Characteristics.

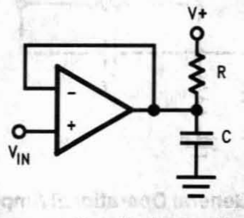
The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 3a,* the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/11134–5

FIGURE 3a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 3b*). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



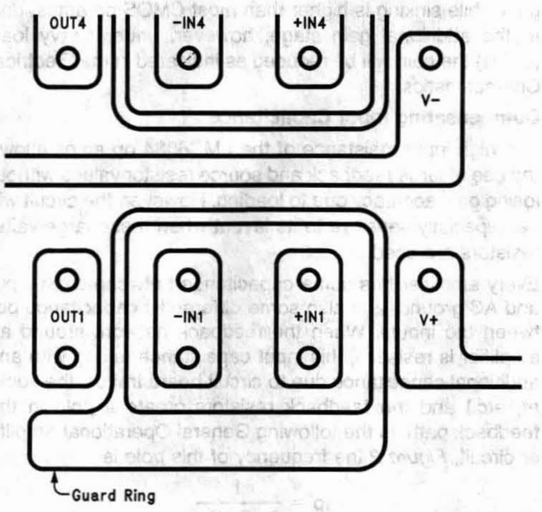
TL/H/11134–22

FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6034, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

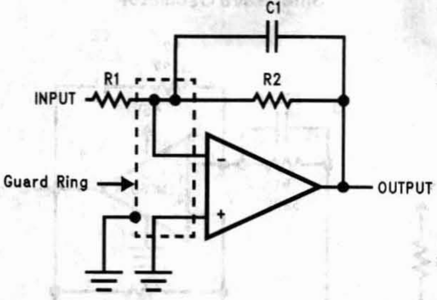
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6034's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 4.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6034's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 5a, 5b, 5c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 5d.*



TL/H/11134–6

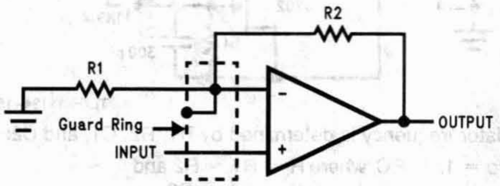
FIGURE 4. Example of Guard Ring in P.C. Board Layout

Application Hints (Continued)


C1
R1
R2
INPUT
Guard Ring
OUTPUT
-
+

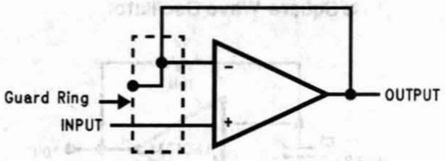
TL/H/11134-7

(a) Inverting Amplifier


R2
R1
Guard Ring
INPUT
OUTPUT
-
+

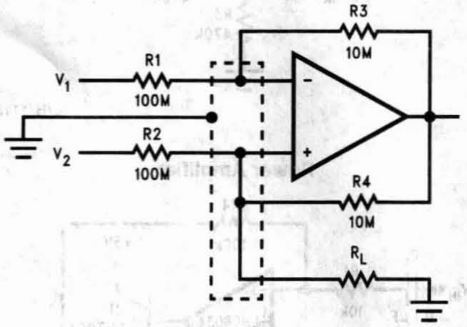
TL/H/11134-8

(b) Non-Inverting Amplifier


Guard Ring
INPUT
OUTPUT
-
+

TL/H/11134-9

(c) Follower

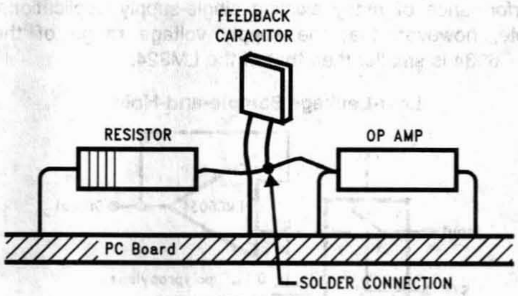

R3
10M
R1
100M
V1
R2
100M
V2
R4
10M
RL
-
+

TL/H/11134-10

(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.


FEEDBACK
CAPACITOR
RESISTOR
OP AMP
PC Board
SOLDER CONNECTION

TL/H/11134-11

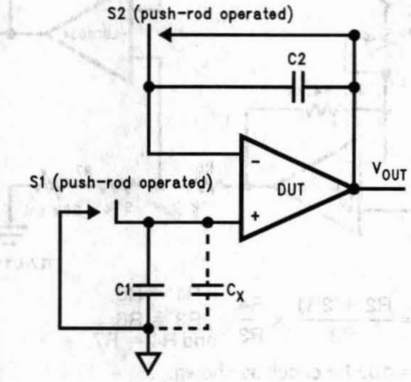
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b^- = \frac{dV_{OUT}}{dt} \times C2.$$


S2 (push-rod operated)
C2
S1 (push-rod operated)
DUT
VOUT
C1
Cx
-
+

TL/H/11134-12

FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

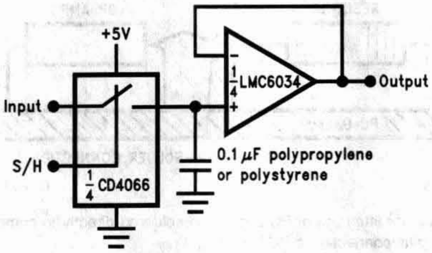
$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications (V^+ = 5.0 VDC)

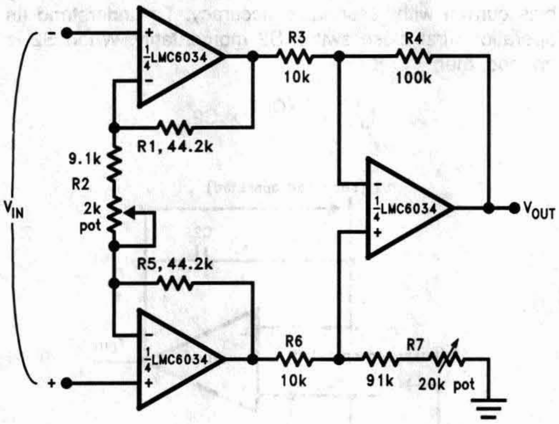
Additional single-supply applications ideas can be found in the LM324 datasheet. The LMC6034 is pin-for-pin compatible with the LM324 and offers greater bandwidth and input resistance over the LM324. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC6034 is smaller than that of the LM324.

Low-Leakage Sample-and-Hold


+5V
Input
S/H
1/4 CD4066
1/4 LMC6034
Output
0.1 µF polypropylene
or polystyrene

TL/H/11134-13

Instrumentation Amplifier


−
+
1/4 LMC6034
R3
10k
R4
100k
R1, 44.2k
9.1k
R2
2k
pot
V_IN
R5, 44.2k
1/4 LMC6034
V_OUT
1/4 LMC6034
R6
10k
R7
91k
20k pot

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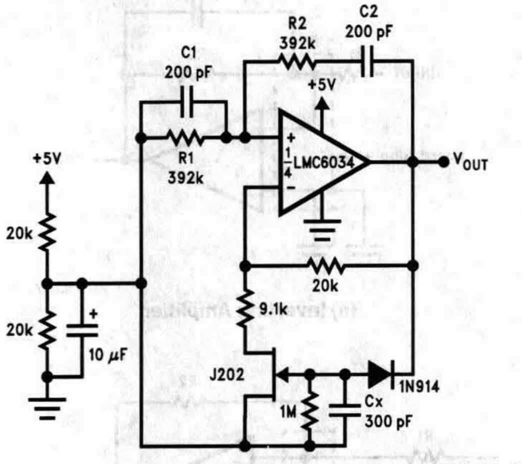
$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3} \quad \text{if } R1 = R5, \; R3 = R6, \text{ and } R4 = R7.$$

= 100 for circuit as shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affect CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator


R2
392k
C2
200 pF
C1
200 pF
+5V
R1
392k
1/4 LMC6034
V_OUT
+5V
20k
20k
9.1k
20k
10 µF
J202
1N914
1M
Cx
300 pF

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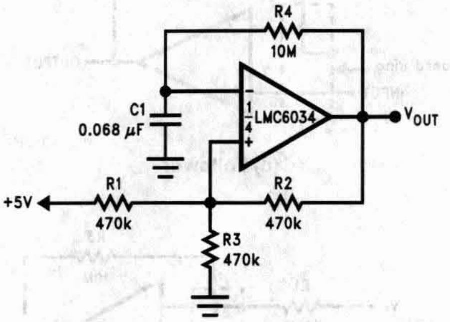
Oscillator frequency is determined by R1, R2, C1, and C2:

$f_{osc} = 1/2\pi RC$, where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.0V.

1 Hz Square-Wave Oscillator


R4
10M
C1
0.068 µF
1/4 LMC6034
V_OUT
+5V
R1
470k
R2
470k
R3
470k

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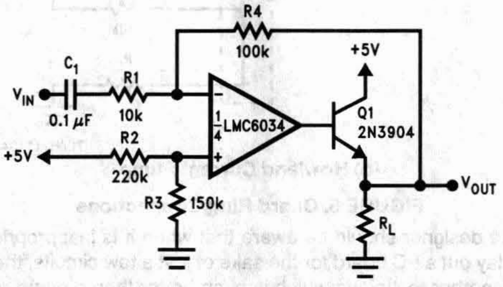
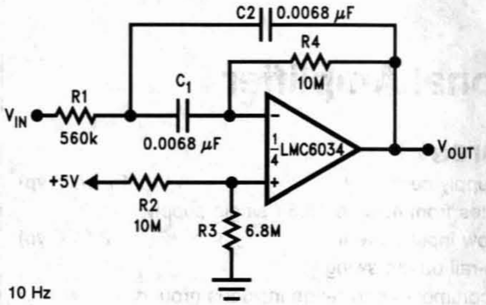
Power Amplifier


R4
100k
+5V
C1
V_IN
R1
10k
0.1 µF
1/4 LMC6034
Q1
2N3904
+5V
R2
220k
R3
150k
V_OUT
R_L

TL/H/11134-17

Typical Single-Supply Applications (V+ = 5.0 VDC) (Continued)

10 Hz Bandpass Filter


C2 0.0068 μF
R4 10M
C1
R1 560k
VIN
0.0068 μF
¼ LMC6034
VOUT
+5V
R2 10M
R3 6.8M

f_O = 10 Hz
Q = 2.1
Gain = −8.8

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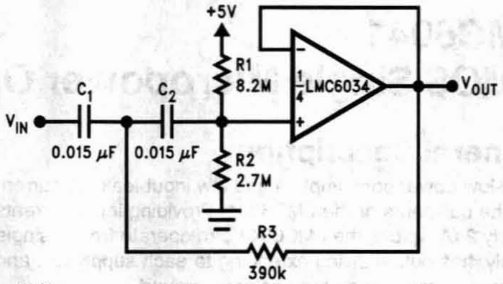
10 Hz High-Pass Filter


+5V
R1 8.2M
C1
C2
VIN
0.015 μF
0.015 μF
R2 2.7M
¼ LMC6034
VOUT
R3 390k

f_c = 10 Hz
d = 0.895
Gain = 1
2 dB passband ripple

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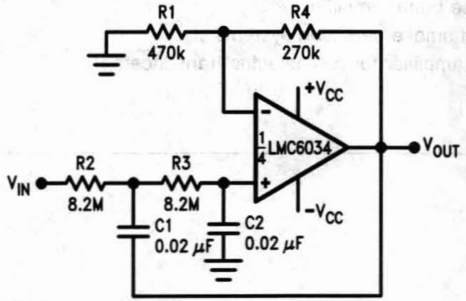
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)


R1 470k
R4 270k
+VCC
¼ LMC6034
VOUT
VIN
R2 8.2M
R3 8.2M
C1 0.02 μF
C2 0.02 μF
−VCC

f_c = 1 Hz
d = 1.414
Gain = 1.57

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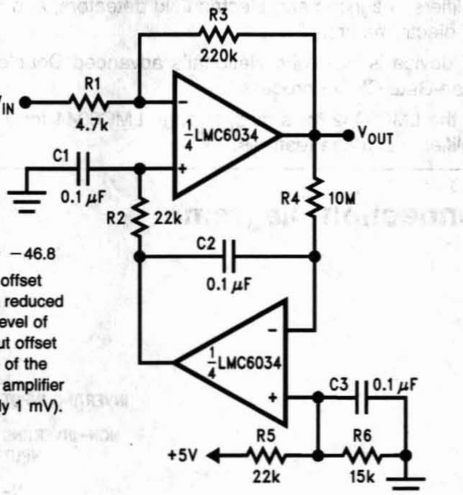
High Gain Amplifier with Offset Voltage Reduction


R3 220k
VIN
R1 4.7k
¼ LMC6034
VOUT
C1 0.1 μF
R4 10M
R2 22k
C2 0.1 μF
¼ LMC6034
C3 0.1 μF
+5V
R5 22k
R6 15k

Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

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National Semiconductor

LMC6041
CMOS Single Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6041. Providing input currents of only 2 fA typical, the LMC6041 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6041 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6041 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6042 for a dual, and the LMC6044 for a quad amplifier with these features.

Features

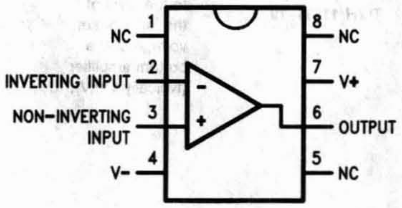
- Low supply current 14 μA (Typ)
- Operates from 4.5V to 15.5V single supply
- Ultra low input current 2 fA (Typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



TL/H/11136-1

Ordering Information

Package	Temperature Range	NSC Drawing	Transport Media
	Industrial −40°C to +85°C		
8-Pin Small Outline	LMC6041AIM LMC6041IM	M08A	Rail Tape and Reel
8-Pin Molded DIP	LMC6041AIN LM6041IN	N08E	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^-	(Note 2)
Output Short Circuit to V^+	(Note 11)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	110°C
ESD Tolerance (Note 4)	500V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Power Dissipation	(Note 3)

Operating Ratings

Temperature Range	
LMC6041AI, LMC6041I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Power Dissipation	(Note 9)
Thermal Resistance (θ_{JA}) (Note 10)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typical (Note 5)	LMC6041AI Limit (Note 6)	LMC6041I Limit (Note 6)	Units (Limit)
V_{OS}	Input Offset Voltage			1	3 **3.3**	6 **6.3**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.3			μV/°C
I_B	Input Bias Current			0.002	**4**	**4**	pA max
I_{OS}	Input Offset Current			0.001	**2**	**2**	pA max
R_{IN}	Input Resistance			>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		75	68 **66**	62 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		75	68 **66**	62 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$ $V_O = 2.5V$		94	84 **83**	74 **73**	dB min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 50 dB		−0.4	−0.1 **0**	−0.1 **0**	V max
				$V^+ - 1.9V$	$V^+ - 2.3V$ **$V^+ - 2.5V$**	$V^+ - 2.3V$ **$V^+ - 2.4V$**	V min
A_V	Large Signal Voltage Gain	$R_L = 100\ k\Omega$ (Note 7)	Sourcing	1000	400 **300**	300 **200**	V/mV min
			Sinking	500	180 **120**	90 **70**	V/mV min
		$R_L = 25\ k\Omega$ (Note 7)	Sourcing	1000	200 **160**	100 **80**	V/mV min
			Sinking	250	100 **60**	50 **40**	V/mV min

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6041AI Limit (Note 6)	LMC6041I Limit (Note 6)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to $V^+/2$	4.987	4.970 **4.950**	4.940 **4.910**	V min
			0.004	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to $V^+/2$	4.980	4.920 **4.870**	4.870 **4.820**	V min
			0.010	0.080 **0.130**	0.130 **0.180**	V max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to $V^+/2$	14.970	14.920 **14.880**	14.880 **14.820**	V min
			0.007	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to $V^+/2$	14.950	14.900 **14.850**	14.850 **14.800**	V min
			0.022	0.100 **0.150**	0.150 **0.200**	V max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **10**	13 **8**	mA min
		Sinking, $V_O = 5V$	21	16 **8**	13 **8**	mA min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15 **10**	15 **10**	mA min
		Sinking, $V_O = 13V$ (Note 11)	39	24 **8**	21 **8**	mA min
I_S	Supply Current	$V_O = 1.5V$	14	20 **24**	26 **30**	μA max
		$V^+ = 15V$	18	26 **31**	34 **39**	μA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6041AI	LMC6041I	Units (Limit)
				Limit (Note 6)	Limit (Note 6)	
SR	Slew Rate	(Note 8)	0.02	0.015 **0.010**	0.010 **0.007**	V/μs min
GBW	Gain-Bandwidth Product		75			kHz
ϕ_m	Phase Margin		60			Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	83			nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002			pA/$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{pp}$ ±5V Supply	0.01			%

Note 1: Absolute Maxium Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

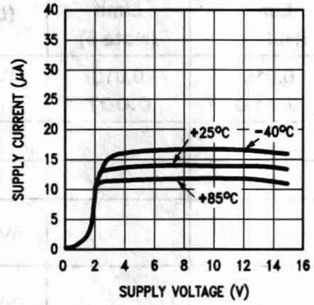
Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

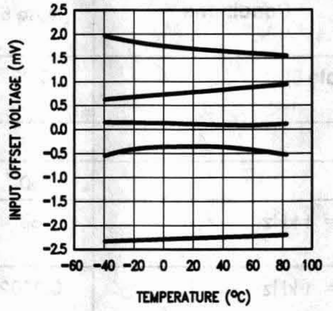
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

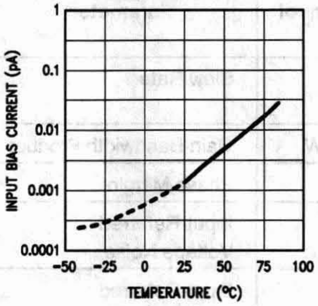
Supply Current vs Supply Voltage



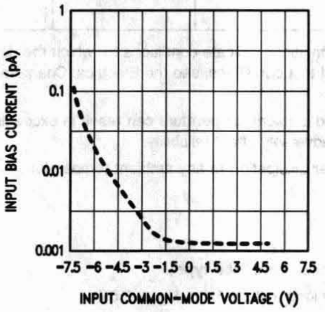
Offset Voltage vs Temperature of Five Representative Units



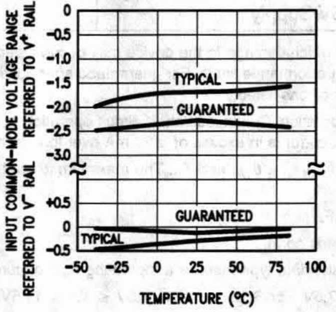
Input Bias Current vs Temperature



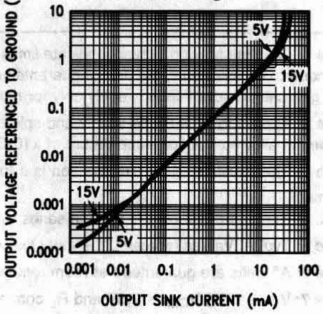
Input Bias Current vs Input Common-Mode Voltage



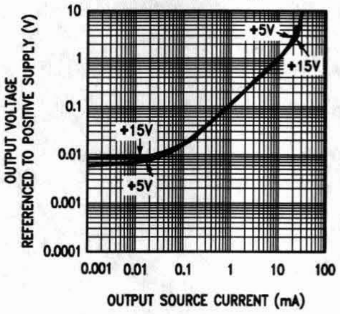
Input Common-Mode Voltage Range vs Temperature



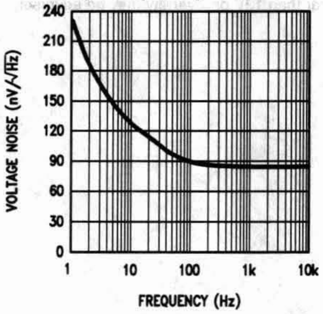
Output Characteristics Current Sinking



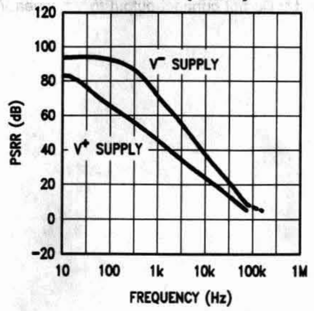
Output Characteristics Current Sourcing



Input Voltage Noise vs Frequency

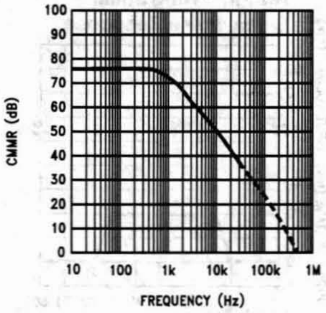


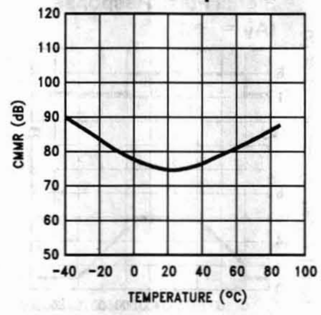
Power Supply Rejection Ratio vs Frequency

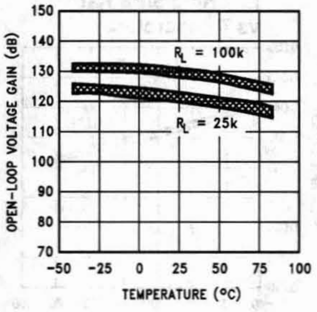


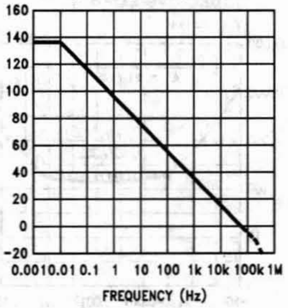
TL/H/11136–2

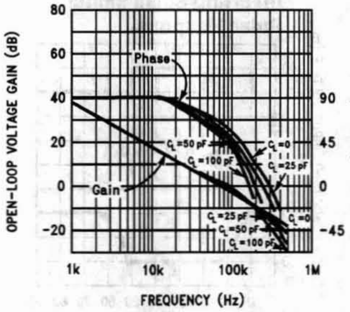
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

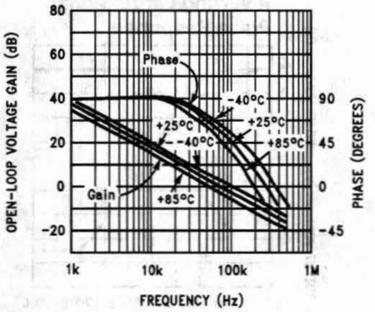

CMRR vs Frequency

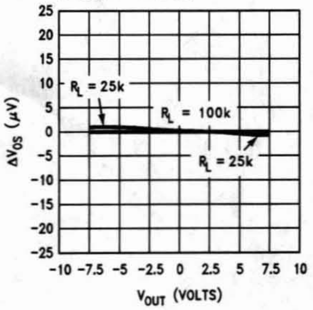

CMRR vs Temperature

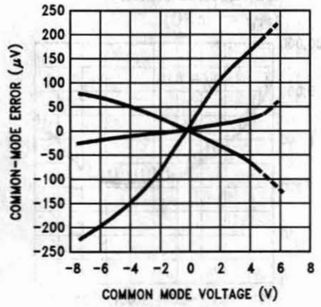

Open-Loop Voltage Gain vs Temperature

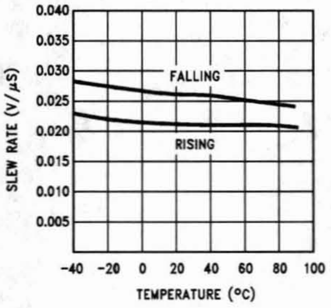

Open-Loop Frequency Response


Gain and Phase Responses vs Load Capacitance


Gain and Phase Responses vs Temperature


Gain Error (V_{OS} vs V_{OUT})

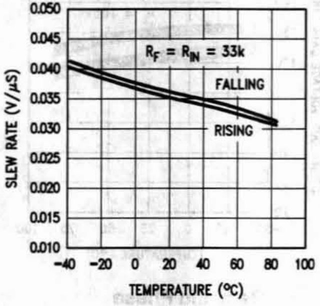

Common-Mode Error vs Common-Mode Voltage of Three Representative Units


Non-Inverting Slew Rate vs Temperature

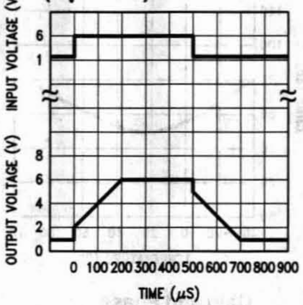
TL/H/11136-3

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

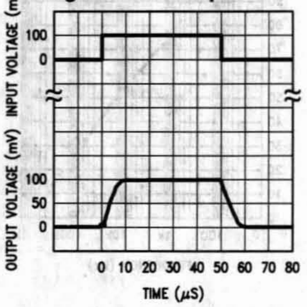
Inverting Slew Rate vs Temperature



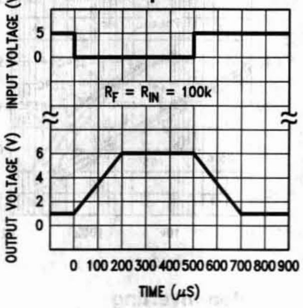
Non-Inverting Large Signal Pulse Response ($A_V = +1$)



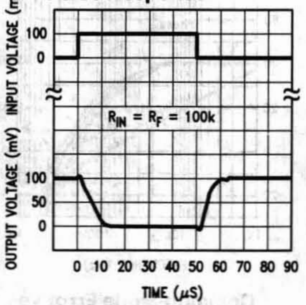
Non-Inverting Small Signal Pulse Response



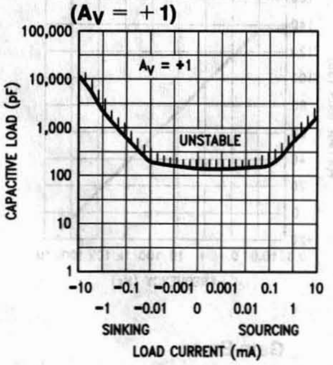
Inverting Large-Signal Pulse Response



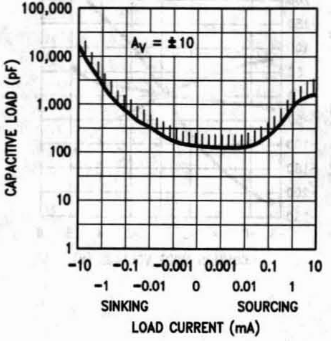
Inverting Small Signal Pulse Response



Stability vs Capacitive Load ($A_V = +1$)



Stability vs Capacitive Load ($A_V = \pm 10$)



TL/H/11136–4

Applications Hints

AMPLIFIER TOPOLOGY

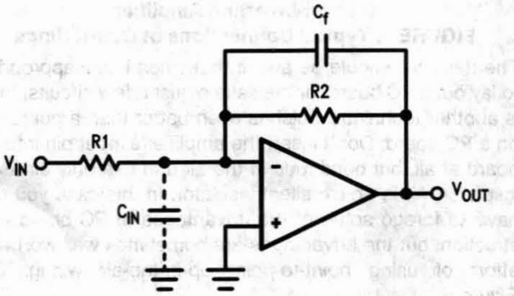
The LMC6041 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6041 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input current, like the LMC6041.

Although the LMC6041 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuits board parasitics, reduce phase margins.

When high input impedance are demanded, guarding of the LMC6041 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work.**)



TL/H/11136–5

FIGURE 1. Cancelling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Adding a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

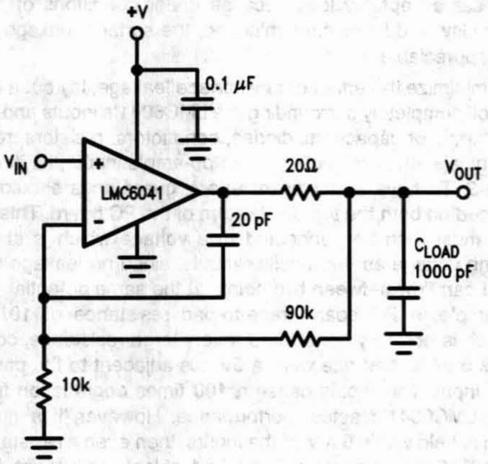
or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.



TL/H/11136–6

FIGURE 2a. LMC6041 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V+ (*Figure 2b*). Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

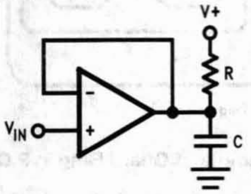


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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

Application Hints (Continued)

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6041, typically less than 2fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6041's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifer inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6041's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.

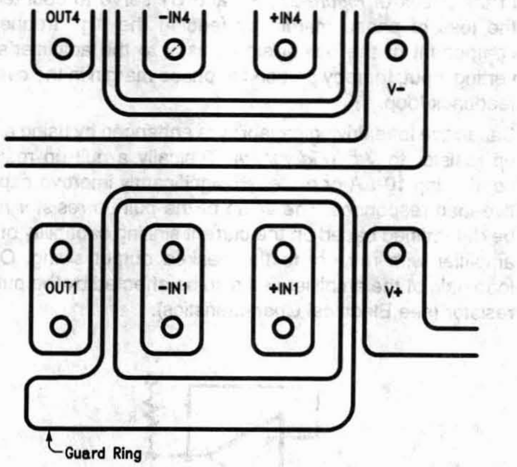

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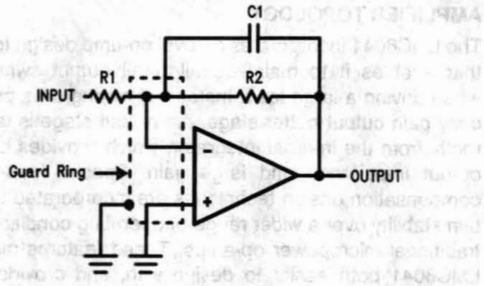
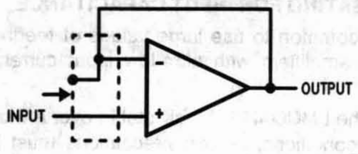
FIGURE 3. Example of Guard Ring in P.C. Board Layout



TL/H/11136-8

(a) Inverting Amplifier



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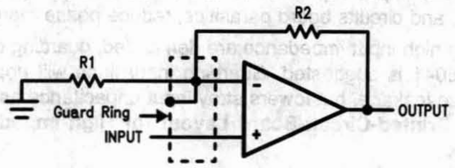
(b) Follower

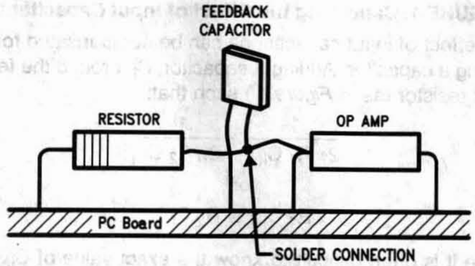


TL/H/11136-10

(c) Non-Inverting Amplifier

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



TL/H/11136-11

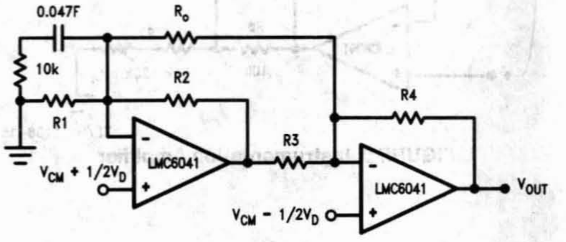
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6041 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these type of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.



TL/H/11136–12

FIGURE 6. Two Op-Amp Instrumentation Amplifier

The circuit in *Figure 6* is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 28 μA. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to *Figure 6*, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D.

Rejection of the common-mode component of the input is accomplished by making the ratio of R1/R2 equal to R3/R4. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R_O}\right) V_D$$

A suggested design guideline is to minimize the difference of value between R1 through R4. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If RN = R1 = R2 = R3 = R4 then the gain equation can be simplified:

$$V_{OUT} = 2\left(1 + \frac{RN}{R_O}\right) V_D$$

Due to the "zero-in, zero-out" performance of the LMC6041, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to V_S– 2.3V, worst case at room temperature. This feature of the LMC6041 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in *Figure 7*. Provisions have been made for low sensitivity trimming of CMRR and gain.

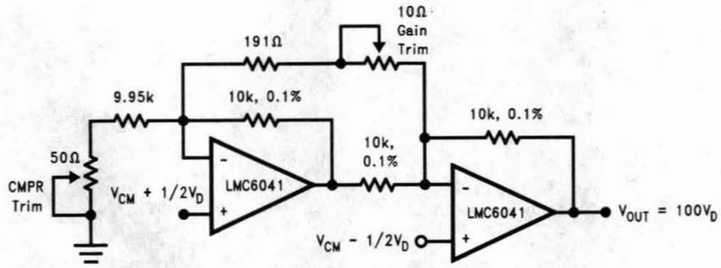


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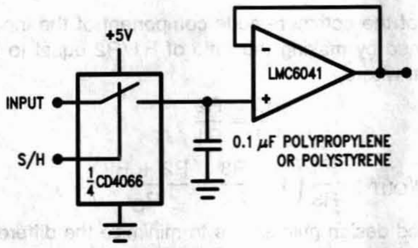
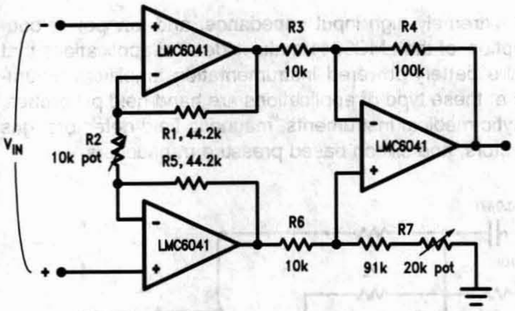
FIGURE 7. Low-Power Two-Op-Amp Instrumentation Amplifier

Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)


+5V
INPUT
S/H
$\frac{1}{4}$ CD4066
LMC6041
OUTPUT
0.1 μF POLYPROPYLENE
OR POLYSTYRENE

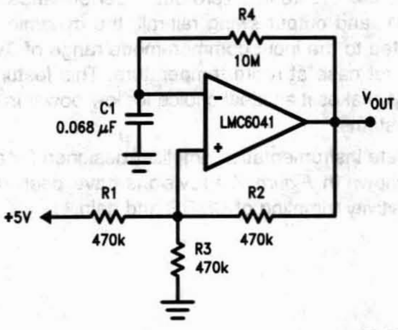
TL/H/11136–14

FIGURE 8. Low-Leakage Sample and Hold


−
+
V_{IN}
LMC6041
R3
10k
R4
100k
R1, 44.2k
R2
10k pot
R5, 44.2k
LMC6041
V_{OUT}
LMC6041
R6
10k
R7
91k
20k pot

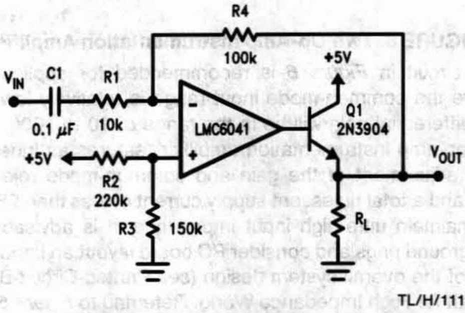
TL/H/11136–15

FIGURE 9. Instrumentation Amplifier


R4
10M
C1
0.068 μF
LMC6041
V_{OUT}
+5V
R1
470k
R2
470k
R3
470k

TL/H/11136–16

FIGURE 10. 1 Hz Square-Wave Oscillator


R4
100k
+5V
V_{IN}
C1
0.1 μF
R1
10k
LMC6041
Q1
2N3904
V_{OUT}
+5V
R2
220k
R3
150k
R_L

TL/H/11136–17

FIGURE 11. AC Coupled Power Amplifier

National Semiconductor

LMC6042
CMOS Dual Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6042. Providing input currents of only 2 fA typical, the LMC6042 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6042 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6042 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6041 for a single, and the LMC6044 for a quad amplifier with these features.

Features

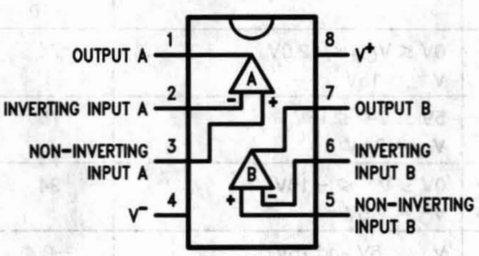
- Low supply current 10 μA/Amp (typ)
- Operates from 4.5V to 15V single supply
- Ultra low input current 2 fA (typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



TL/H/11137-1

Ordering Information

Package	Temperature Range	NSC Drawing	Transport Media
	Industrial −40°C to +85°C		
8-Pin Small Outline	LMC6042AIM LMC6042IM	M08A	Rail Tape and Reel
8-Pin Molded DIP	LMC6042AIN LMC6042IN	N08E	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 seconds)	260°C
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	110°C
ESD Tolerance (Note 4)	500V
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$

Operating Ratings

Temperature Range	
LMC6042AI, LMC6042I	$-40°C \leq T_J \leq +85°C$
Supply Voltage	$4.5V \leq V^+ \leq 15.5V$
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typical (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
V_{OS}	Input Offset Voltage			1	3 **3.3**	6 **6.3**	mV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.3			μV/°C
I_B	Input Bias Current			0.002	**4**	**4**	pA (Max)
I_{OS}	Input Offset Current			0.001	**2**	**2**	pA (Max)
R_{IN}	Input Resistance			>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 12.0V$ $V^+ = 15V$		75	68 **66**	62 **60**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V^+ \leq 15V$ $V_O = 2.5V$		75	68 **66**	62 **60**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \leq V^- \leq -10V$ $V_O = 2.5V$		94	84 **83**	74 **73**	dB Min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB		−0.4	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9V$	$V^+ - 2.3V$ **$V^+ - 2.5V$**	$V^+ - 2.3V$ **$V^+ - 2.4V$**	V Min
A_V	Large Signal Voltage Gain	$R_L = 100\ k\Omega$ (Note 7)	Sourcing	1000	400 **300**	300 **200**	V/mV Min
			Sinking	500	180 **120**	90 **70**	V/mV Min
		$R_L = 25\ k\Omega$ (Note 7)	Sourcing	1000	200 **160**	100 **80**	V/mV Min
			Sinking	250	100 **60**	50 **40**	V/mV Min

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6042AI	LMC6042I	Units (Limit)
				Limit (Note 6)	Limit (Note 6)	
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to $V^+/2$	4.987	4.970 **4.950**	4.940 **4.910**	V Min
			0.004	0.030 **0.050**	0.060 **0.090**	V Max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to $V^+/2$	4.980	4.920 **4.870**	4.870 **4.820**	V Min
			0.010	0.080 **0.130**	0.130 **0.180**	V Max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to $V^+/2$	14.970	14.920 **14.880**	14.880 **14.820**	V Min
			0.007	0.030 **0.050**	0.060 **0.090**	V Max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to $V^+/2$	14.950	14.900 **14.850**	14.850 **14.800**	V Min
			0.022	0.100 **0.150**	0.150 **0.200**	V Max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **10**	13 **8**	mA Min
		Sinking, $V_O = 5V$	21	16 **8**	13 **8**	mA Min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15 **10**	15 **10**	mA Min
		Sinking, $V_O = 13V$ (Note 12)	39	24 **8**	21 **8**	mA Min
I_S	Supply Current	Both Amplifiers $V_O = 1.5V$	20	34 **39**	45 **50**	μA Max
		Both Amplifiers $V^+ = 15V$	26	44 **51**	56 **65**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6042AI	LMC6042I	Units (Limit)
				Limit (Note 6)	Limit (Note 6)	
SR	Slew Rate	(Note 8)	0.02	0.015 **0.010**	0.010 **0.007**	V/μs Min
GBW	Gain-Bandwidth Product		100			kHz
ϕ_m	Phase Margin		60			Deg
	Amp-to-Amp Isolation	(Note 9)	115			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	83			$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.0002			$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	f = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{PP}$ ±5V Supply	0.01			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12\ V_{PP}$.

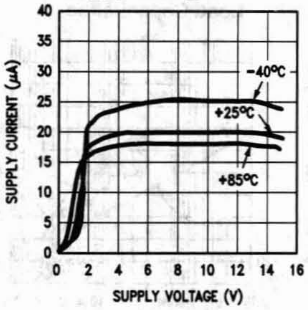
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

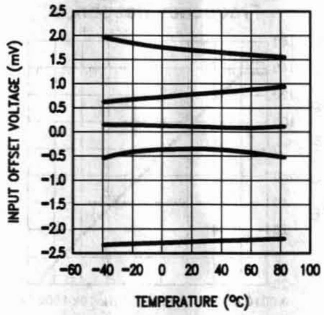
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

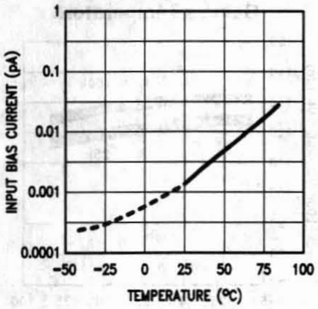
Supply Current vs Supply Voltage



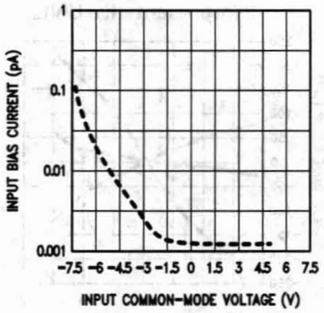
Offset Voltage vs Temperature of Five Representative Units



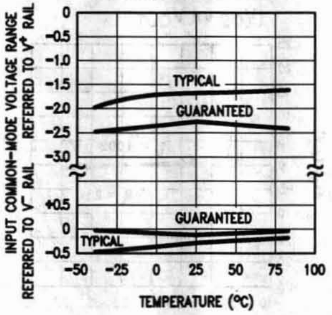
Input Bias Current vs Temperature



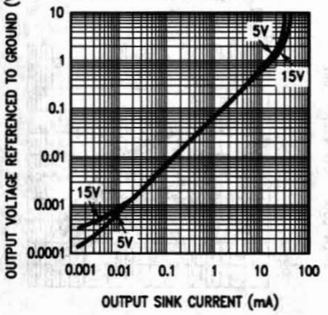
Input Bias Current vs Input Common-Mode Voltage



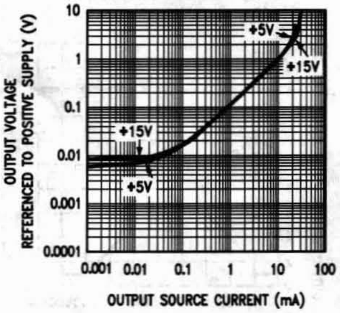
Input Common-Mode Voltage Range vs Temperature



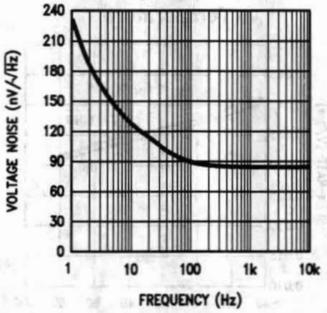
Output Characteristics Current Sinking



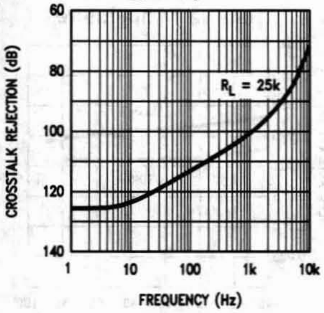
Output Characteristics Current Sourcing



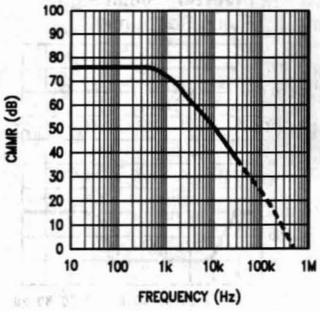
Input Voltage Noise vs Frequency



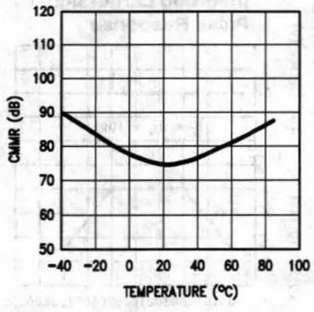
Crosstalk Rejection vs Frequency



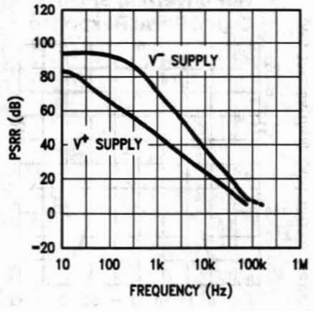
CMRR vs Frequency



CMRR vs Temperature



Power Supply Rejection Ratio vs Frequency

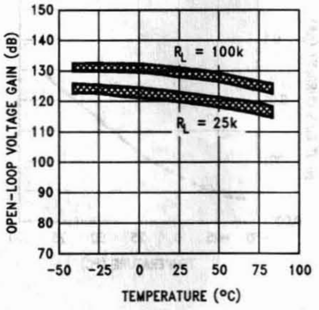


TL/H/11137–2

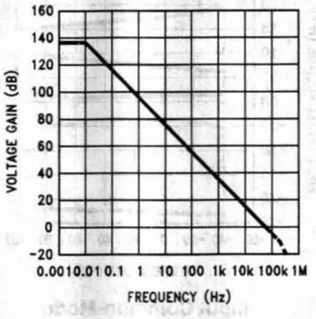
Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

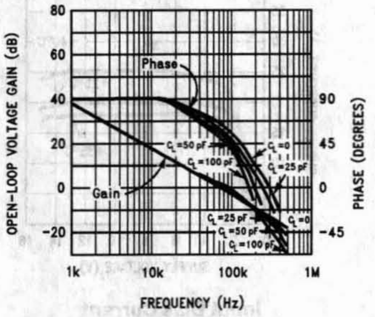
Open-Loop Voltage Gain vs Temperature



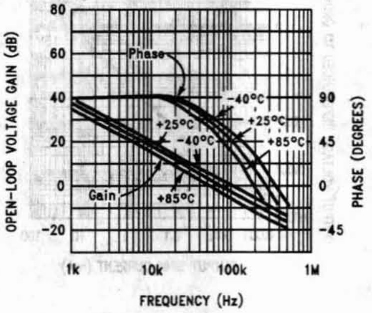
Open-Loop Frequency Response



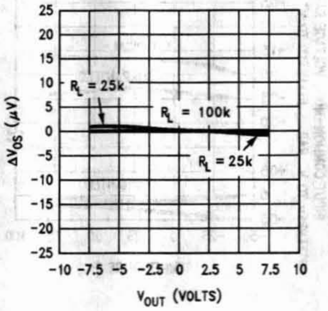
Gain and Phase Responses vs Load Capacitance



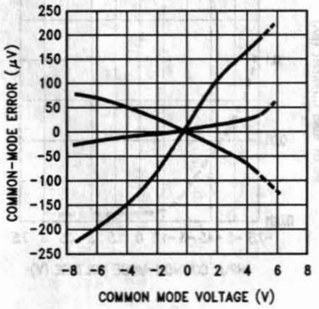
Gain and Phase Response vs Temperature



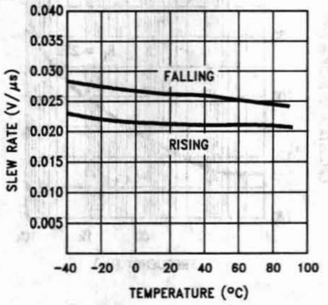
Gain Error (V_{OS} vs V_{OUT})



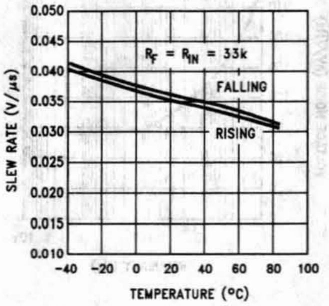
Common-Mode Error vs Common-Mode Voltage of 3 Representative Units



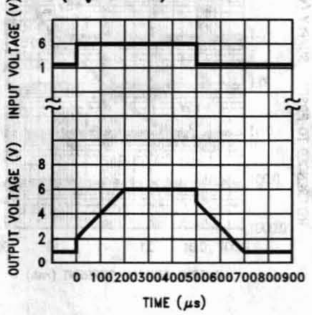
Non-Inverting Slew Rate vs Temperature



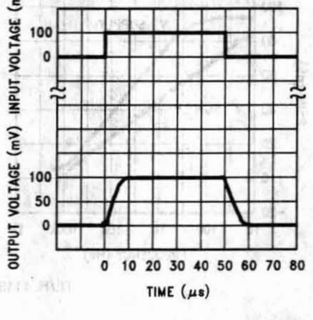
Inverting Slew Rate vs Temperature



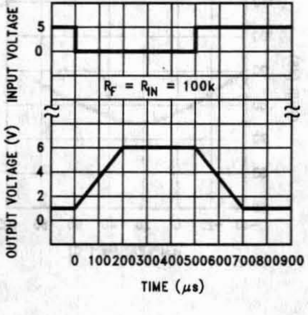
Non-Inverting Large Signal Pulse Response ($A_V = +1$)



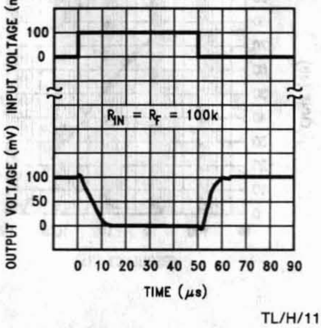
Non-Inverting Small Signal Pulse Response



Inverting Large-Signal Pulse Response



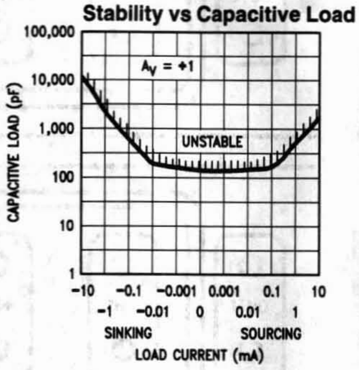
Inverting Small Signal Pulse Response

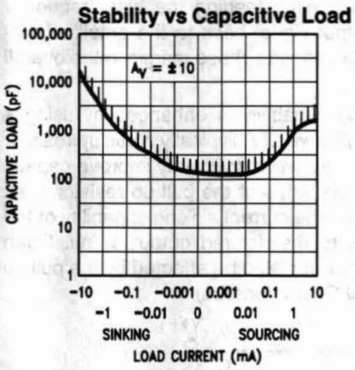


TL/H/11137-3

Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)





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Applications Hints

AMPLIFIER TOPOLOGY

The LMC6042 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6042 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input curent, like the LMC6042.

Although the LMC6042 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6042 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work**).

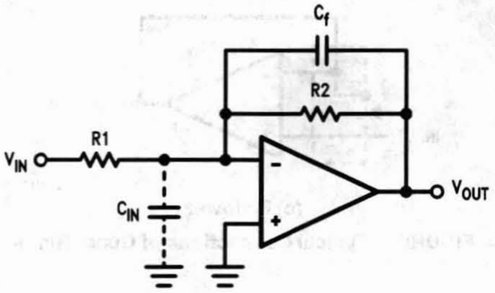

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FIGURE 1. Cancelling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R1\, C_{IN}} \geq \frac{1}{2\pi R2\, C_f}$$

or

$$R1\, C_{IN} \leq R2\, C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

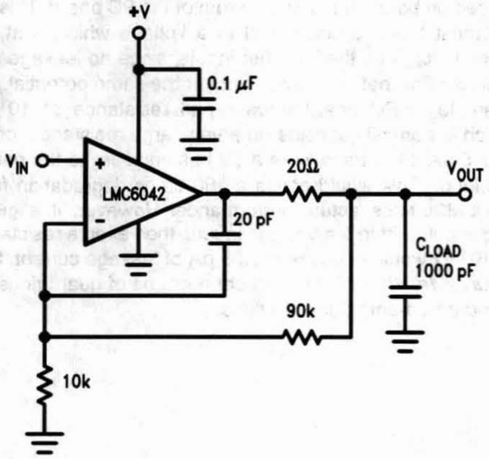

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FIGURE 2a. LMC6042 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

Applications Hints (Continued)

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 2b)*. Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

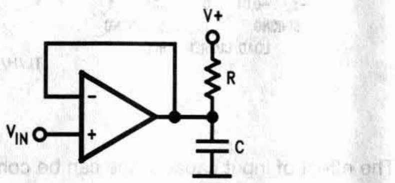

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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6042, typically less than 2 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6042's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6042's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations.

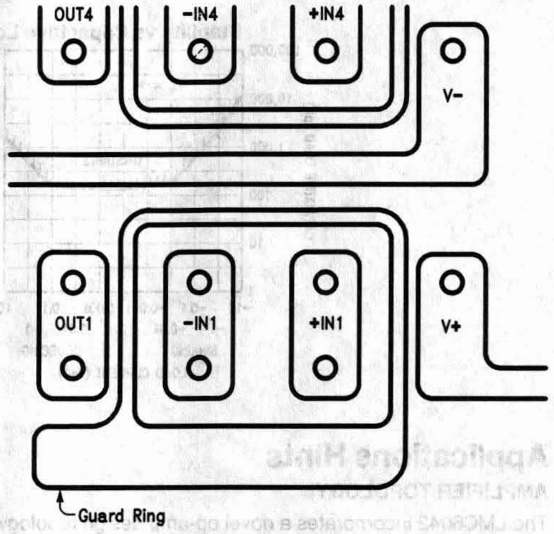

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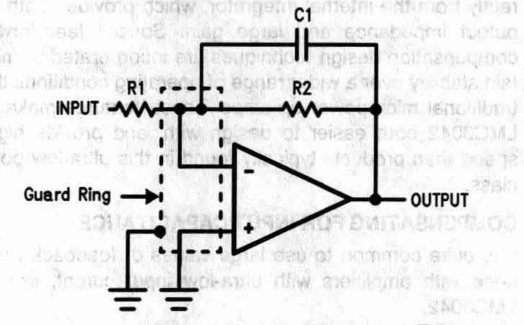
FIGURE 3. Example of Guard Ring in P.C. Board Layout



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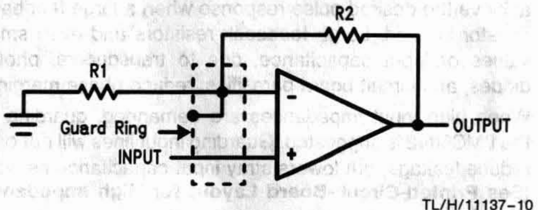
(a) Inverting Amplifier



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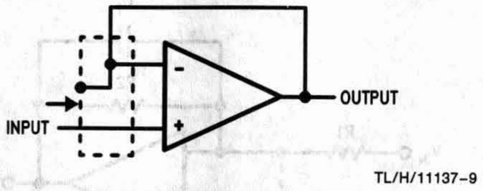
(b) Non-Inverting Amplifier



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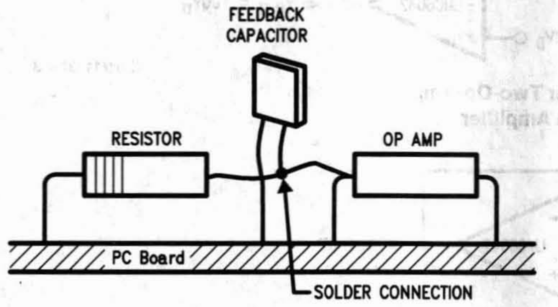
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

Application Hints (Continued)

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6042 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

The circuit in *Figure 6* is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 20 μA. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to *Figure 6*, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D.

Rejection of the common-mode component of the input is accomplished by making the ratio of R1/R2 equal to R3/R4. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R0}\right) V_D$$

A suggested design guideline is to minimize the difference of value between R1 through R4. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If RN = R1 = R2 = R3 = R4 then the gain equation can be simplified:

$$V_{OUT} = 2\left(1 + \frac{RN}{R0}\right) V_D$$

Due to the "zero-in, zero-out" performance of the LMC6042, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to $V_S - 2.3V$, worst case at room temperature. This feature of the LMC6042 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in *Figure 7*. Provisions have been made for low sensitivity trimming of CMRR and gain.

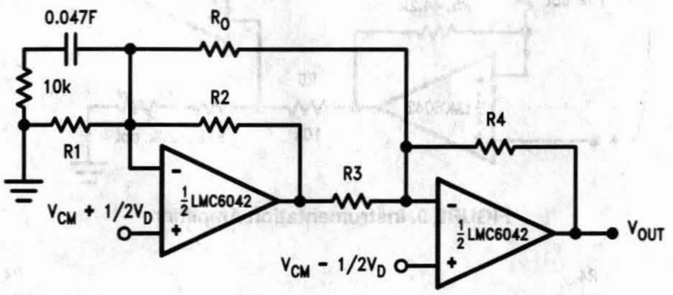

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FIGURE 6. Two Op-Amp Instrumentation Amplifier

Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)

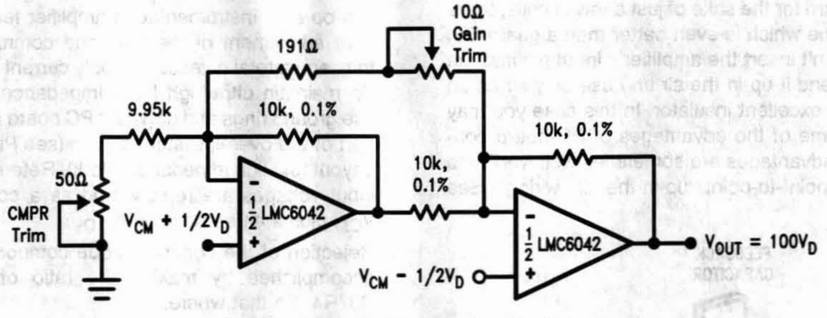
10Ω Gain Trim
191Ω
9.95k
10k, 0.1%
10k, 0.1%
50Ω
CMPR Trim
V_{CM} + 1/2V_D
$\frac{1}{2}$ LMC6042
10k, 0.1%
$\frac{1}{2}$ LMC6042
V_{CM} − 1/2V_D
V_{OUT} = 100V_D

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FIGURE 7. Low-Power Two-Op-Amp Instrumentation Amplifier

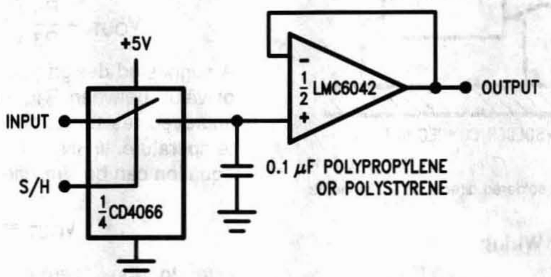
+5V
INPUT
S/H
$\frac{1}{4}$ CD4066
$\frac{1}{2}$ LMC6042
OUTPUT
0.1 μF POLYPROPYLENE OR POLYSTYRENE

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FIGURE 8. Low-Leakage Sample and Hold

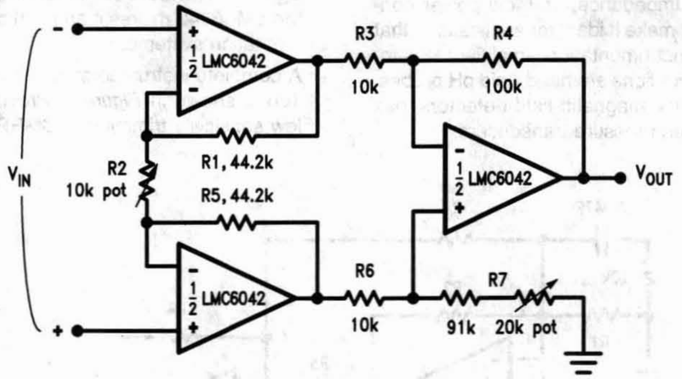
−
+
V_{IN}
$\frac{1}{2}$ LMC6042
$\frac{1}{2}$ LMC6042
$\frac{1}{2}$ LMC6042
R3 10k
R4 100k
R1, 44.2k
R2 10k pot
R5, 44.2k
R6 10k
R7 91k 20k pot
V_{OUT}

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FIGURE 9. Instrumentation Amplifier

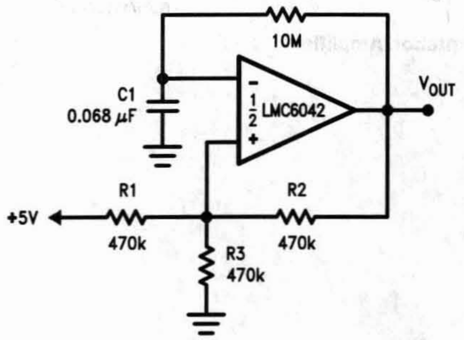
R4 10M
C1 0.068 μF
$\frac{1}{2}$ LMC6042
V_{OUT}
R1 470k
R2 470k
R3 470k
+5V

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FIGURE 10. 1 Hz Square Wave Oscillator

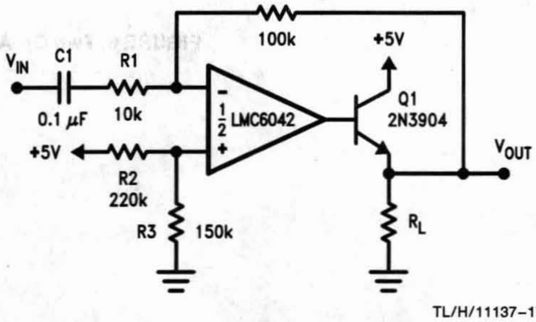
R4 100k
+5V
V_{IN}
C1 0.1 μF
R1 10k
$\frac{1}{2}$ LMC6042
Q1 2N3904
+5V
R2 220k
R3 150k
R_L
V_{OUT}

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FIGURE 11. AC Coupled Power Amplifier

National Semiconductor

LMC6044 CMOS Quad Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6044. Providing input currents of only 2 fA typical, the LMC6044 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6044 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6044 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6041 for a single, and the LMC6042 for a dual amplifier with these features.

Features

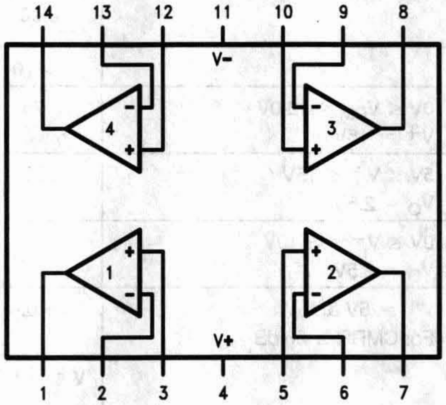
- Low supply current 10 μA/Amp (Typ)
- Operates from 4.5V to 15.5V single supply
- Ultra low input current 2 fA (Typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram

14-Pin DIP/SO



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Ordering Information

Package	Temperature Range Industrial −40°C to +85°C	NSC Drawing	Transport Media
14-Pin Small Outline	LMC6044AIM LMC6044IM	M14A	Rail Tape and Reel
14-Pin Molded DIP	LMC6044AIN LMC6044IN	N14A	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	110°C
ESD Tolerance (Note 4)	500V
Voltage at I/O Pin (V^+)	+0.3V, (V^-) −0.3V

Operating Ratings

Temperature Range	
LMC6044AI, LMC6044I	$-40°C \leq T_J \leq +85°C$
Supply Voltage	$4.5V \leq V^+ \leq 15.5V$
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
14-Pin DIP	85°C/W
14-Pin SO	115°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI Limit (Note 6)	LMC6044I Limit (Note 6)	Units (Limit)
V_{OS}	Input Offset Voltage		1	3 **3.3**	6 **6.3**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.3			μV/°C
I_B	Input Bias Current		0.002	**4**	**4**	pA max
I_{OS}	Input Offset Current		0.001	**2**	**2**	pA max
R_{IN}	Input Resistance		>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 12.0V$ $V^+ = 15V$	75	68 **66**	62 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V^+ \leq 15V$ $V_O = 2.5V$	75	68 **66**	62 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \leq V^- \leq -10V$ $V_O = 2.5V$	94	84 **83**	74 **73**	dB min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	V max
			$V^+ - 1.9V$	$V^+ - 2.3V$ **$V^+ - 2.5V$**	$V^+ - 2.3V$ **$V^+ - 2.4V$**	V min
A_V	Large Signal Voltage Gain	$R_L = 100\ k\Omega$ (Note 7) Sourcing	1000	400 **300**	300 **200**	V/mV min
		Sinking	500	180 **120**	90 **70**	V/mV min
		$R_L = 25\ k\Omega$ (Note 7) Sourcing	1000	200 **160**	100 **80**	V/mV min
		Sinking	250	100 **60**	50 **40**	V/mV min

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI Limit (Note 6)	LMC6044I Limit (Note 6)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.970 **4.950**	4.940 **4.910**	V min
			0.004	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to 2.5V	4.980	4.920 **4.870**	4.870 **4.820**	V min
			0.010	0.080 **0.130**	0.130 **0.180**	V max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to $V^+/2$	14.970	14.920 **14.880**	14.880 **14.820**	V min
			0.007	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to $V^+/2$	14.950	14.900 **14.850**	14.850 **14.800**	V min
			0.022	0.100 **0.150**	0.150 **0.200**	V max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **10**	13 **8**	mA min
		Sinking, $V_O = 5V$	21	16 **8**	13 **8**	mA min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15 **10**	15 **10**	mA min
		Sinking, $V_O = 13V$ (Note 12)	39	24 **8**	21 **8**	mA min
I_S	Supply Current	Four Amplifiers $V_O = 1.5V$	40	65 **72**	75 **82**	μA max
		Four Amplifiers $V^+ = 15V$	52	85 **94**	98 **107**	μA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI Limit (Note 6)	LMC6044I Limit (Note 6)	Units (Limit)
SR	Slew Rate	(Note 8)	0.02	0.015 **0.010**	0.010 **0.007**	V/μs min
GBW	Gain-Bandwidth Product		0.10			MHz
ϕ_m	Phase Margin		60			Deg
	Amp-to-Amp Isolation	(Note 9)	115			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83			$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002			$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{pp}$ ±5V Supply	0.01			%

Note 1: Absolute Maximum Ratings indicate limts beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

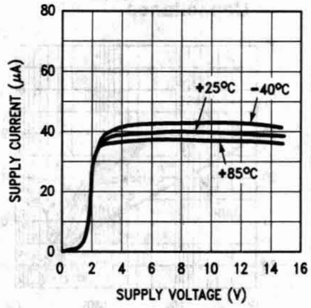
Note 9: Input referred $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12\ V_{PP}$.

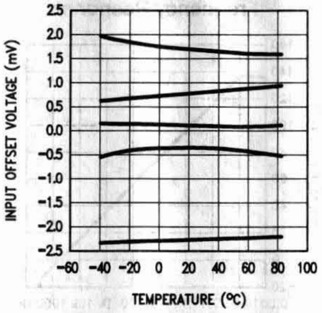
Note 10: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

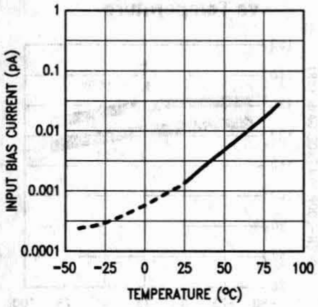
Note 11: All numbers apply for packages soldered directly into a PC poard.

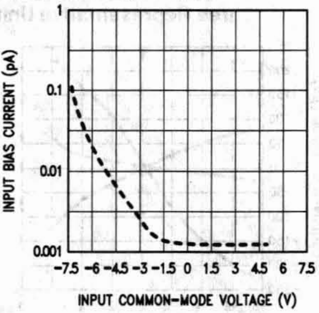
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

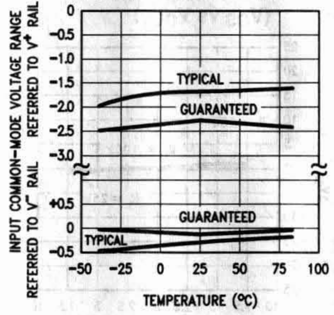
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

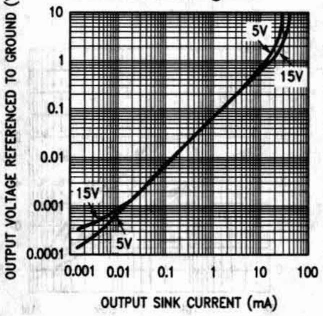

Supply Current vs Supply Voltage

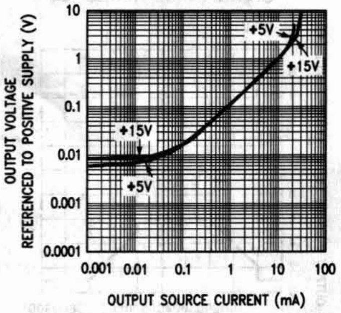

Offset Voltage vs Temperature of Five Representative Units

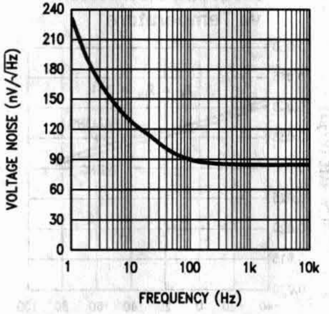

Input Bias Current vs Temperature

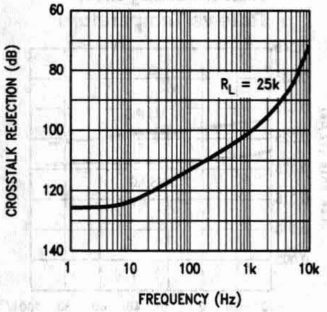

Input Bias Current vs Input Common-Mode Voltage

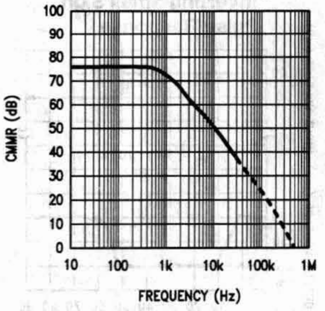

Input Common-Mode Voltage Range vs Temperature

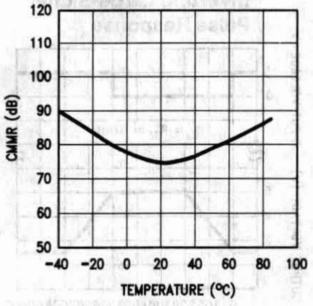

Output Characteristics Current Sinking

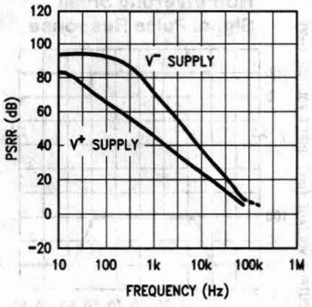

Output Characteristics Current Sourcing


Input Voltage Noise vs Frequency


Crosstalk Rejection vs Frequency


CMRR vs Frequency


CMRR vs Temperature


Power Supply Rejection Ratio vs Frequency

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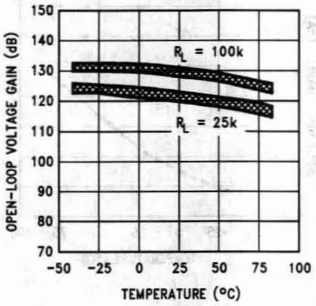
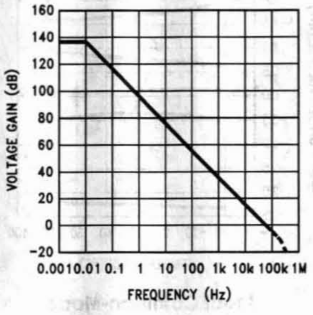
Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

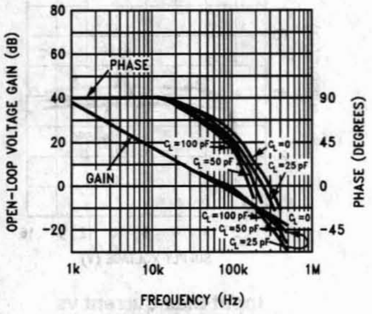
Open-Loop Voltage Gain vs Temperature



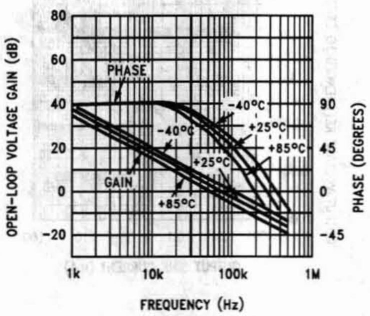
Open-Loop Frequency Response



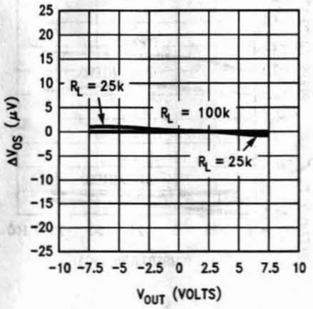
Gain and Phase Responses vs Load Capacitance



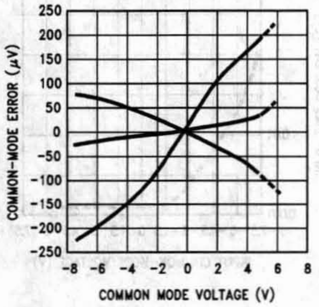
Gain and Phase Responses vs Temperature



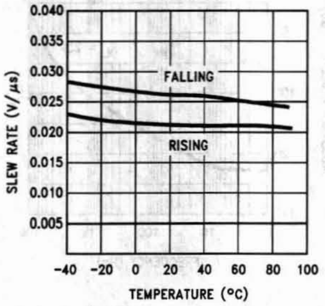
Gain Error (V_{OS} vs V_{OUT})



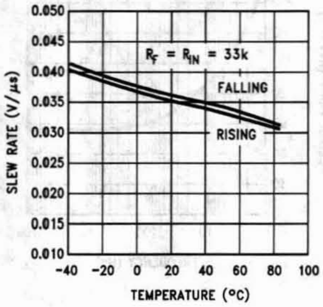
Common-Mode Error vs Common-Mode Voltage of Three Representative Units



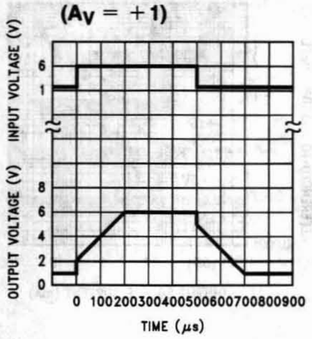
Non-Inverting Slew Rate vs Temperature



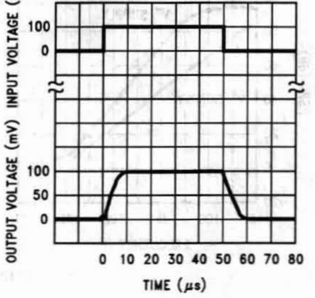
Inverting Slew Rate vs Temperature



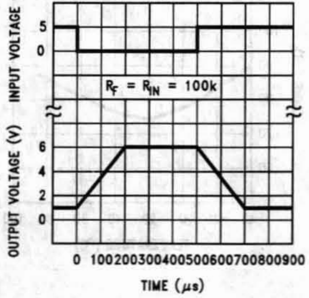
Non-Inverting Large Signal Pulse Response ($A_V = +1$)



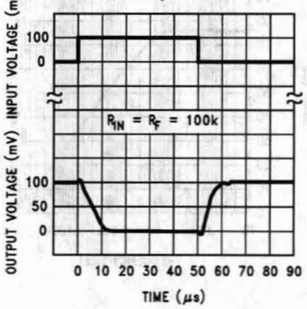
Non-Inverting Small Signal Pulse Response



Inverting Large-Signal Pulse Response



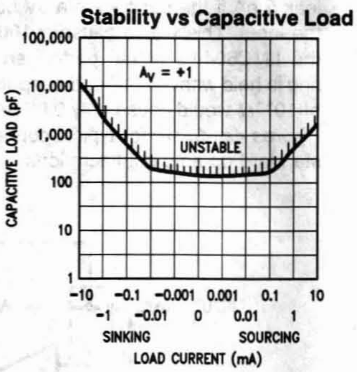
Inverting Small Signal Pulse Response

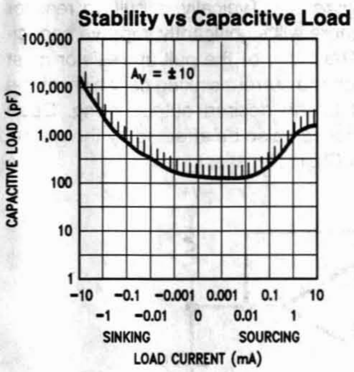


TL/H/11138–3

Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)





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Application Hints

AMPLIFIER TOPOLOGY

The LMC6044 incorporates a novel op-amp design topology that enables it to maintain rail to rail output swing even when driving a large load. Instead of relying on a push-pull unity gain outupt buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6044 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input current, like the LMC6044.

Although the LMC6044 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuits board parasitics, reduce phase margins.

When high input impedance are demanded, guarding of the LMC6044 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work.**)

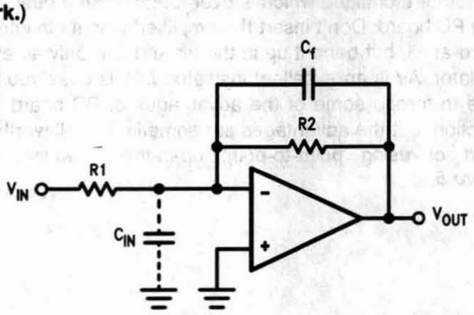

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FIGURE 1. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Adding a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

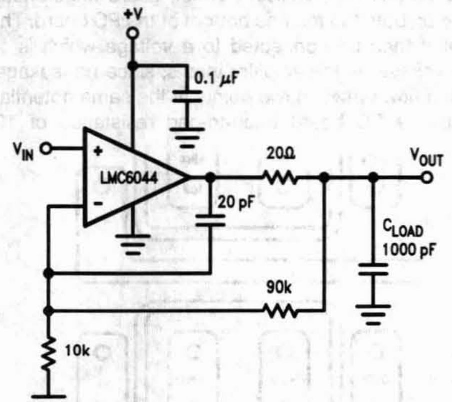
or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a.*



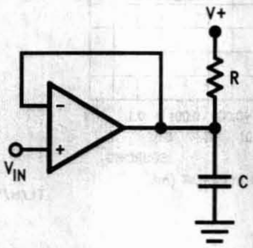
TL/H/11138–6

FIGURE 2a. LMC6044 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Application Hints (Continued)

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 2b)*. Typically, a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



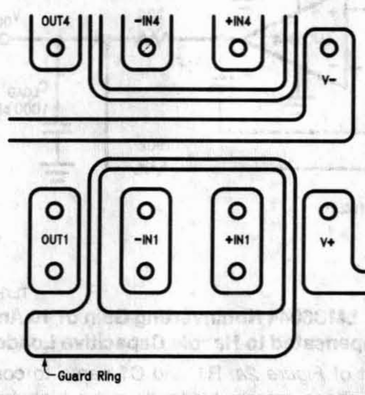
TL/H/11138–18

FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

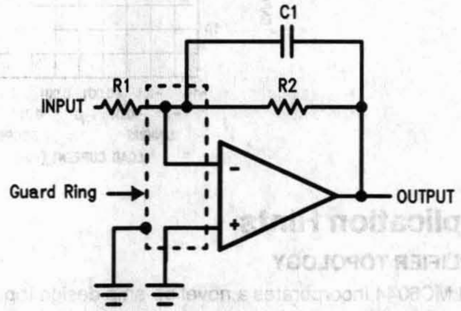
It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6044, typically less than 2 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6044's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifer inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6044's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.



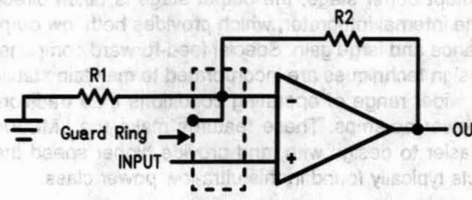
TL/H/11138–7

FIGURE 3. Example of Guard Ring in P.C. Board Layout



TL/H/11138–8

(a) Inverting Amplifier



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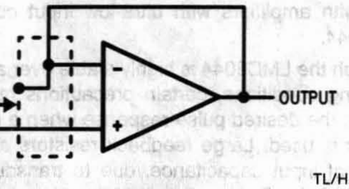
(b) Non-Inverting Amplifier



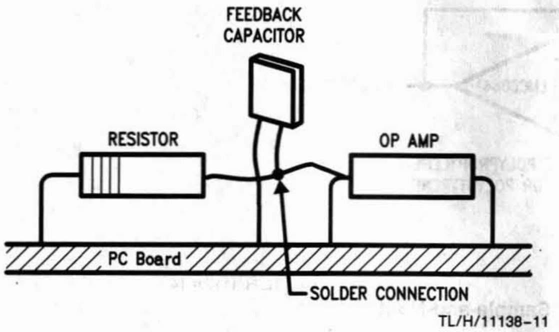
TL/H/11138–9

(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.

Typical Single-Supply Applications $(V^+ = 5.0\ V_{DC})$


FEEDBACK CAPACITOR
RESISTOR
OP AMP
PC Board
SOLDER CONNECTION
TL/H/11138-11

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

The extremely high input impedance, and low power consumption, of the LMC6044 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these type of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

The circuit in *Figure 6* is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 40 μA. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to *Figure 6*, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D. Rejection of the common-mode component of the input is accomplished by making the ratio of R1/R2 equal to R3/R4. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{RO}\right) V_D$$

A suggested design guideline is to minimize the difference of value between R1 through R4. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If RN = R1 = R2 = R3 = R4 then the gain equation can be simplified:

$$V_{OUT} = 2\left(1 + \frac{RN}{RO}\right) V_D$$

Due to the "zero-in, zero-out" performance of the LMC6044, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to V_S− 2.3V, worst case at room temperature. This feature of the LMC6044 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in *Figure 7*. Provisions have been made for low sensitivity trimming of CMRR and gain.

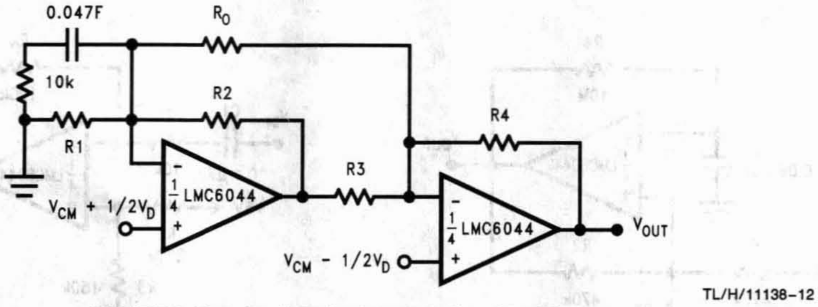

0.047F
R_O
10k
R2
R1
R4
R3
V_{CM} + 1/2V_D
$\frac{1}{4}$ LMC6044
$\frac{1}{4}$ LMC6044
V_{CM} − 1/2V_D
V_{OUT}
TL/H/11138-12

FIGURE 6. Two Op-Amp Instrumentation Amplifier

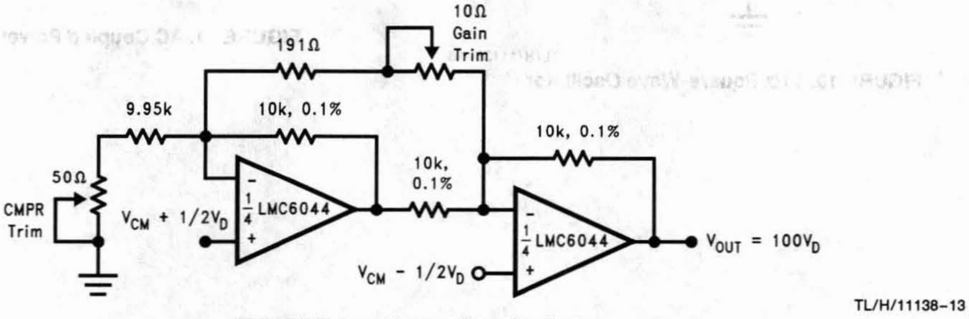
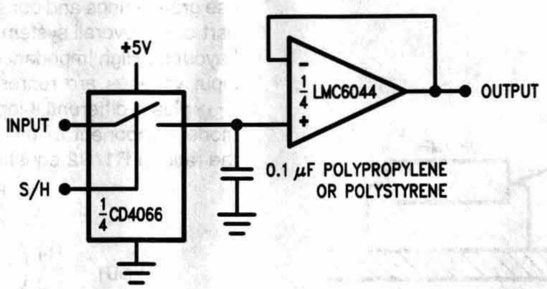

10Ω Gain Trim
191Ω
9.95k
10k, 0.1%
10k, 0.1%
10k, 0.1%
50Ω
CMPR Trim
V_{CM} + 1/2V_D
$\frac{1}{4}$ LMC6044
$\frac{1}{4}$ LMC6044
V_{CM} − 1/2V_D
V_{OUT} = 100V_D
TL/H/11138-13

FIGURE 7. Low-Power Two-Op-Amp Instrumentation Amplifier

Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)


+5V
INPUT
S/H
$\frac{1}{4}$ CD4066
$\frac{1}{4}$ LMC6044
OUTPUT
0.1 μF POLYPROPYLENE
OR POLYSTYRENE

TL/H/11138–14

FIGURE 8. Low-Leakage Sample-and-Hold

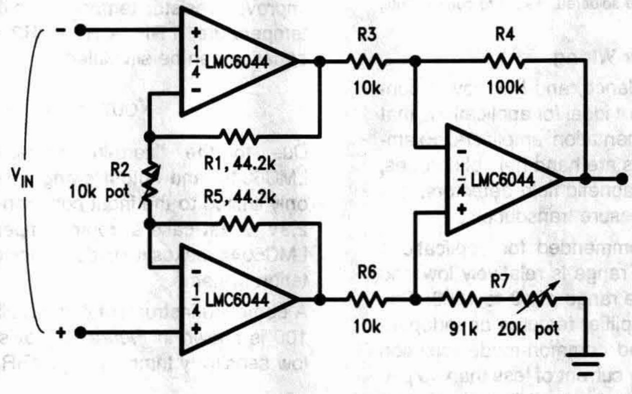

−
+
V_{IN}
$\frac{1}{4}$ LMC6044
R2
10k pot
R1, 44.2k
R5, 44.2k
R3
10k
R4
100k
R6
10k
R7
91k
20k pot
V_{OUT}

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FIGURE 9. Instrumentation Amplifier

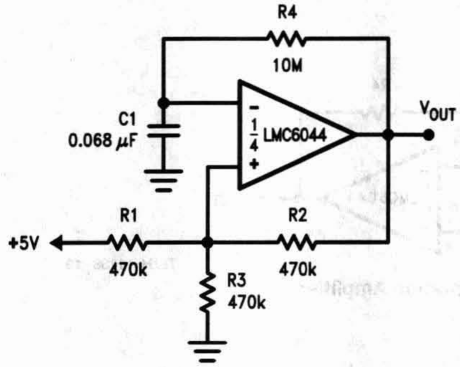
R4
10M
C1
0.068 μF
$\frac{1}{4}$ LMC6044
V_{OUT}
+5V
R1
470k
R2
470k
R3
470k

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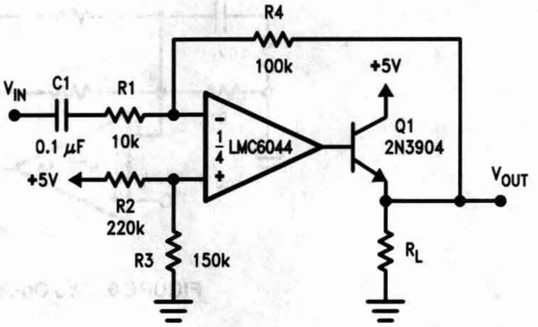
FIGURE 10. 1 Hz Square-Wave Oscillator


V_{IN}
C1
0.1 μF
R1
10k
R4
100k
+5V
R2
220k
R3
150k
$\frac{1}{4}$ LMC6044
Q1
2N3904
R_L
V_{OUT}

TL/H/11138–17

FIGURE 11. AC Coupled Power Amplifier

National Semiconductor

LMC6061 Precision CMOS Single Micropower Operational Amplifier

General Description

The LMC6061 is a precision single low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6061 ideally suited for battery powered applications.

Other applications using the LMC6061 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6081 precision single operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6062 or LMC6064 respectively.

PATENT PENDING

Features (Typical Unless Otherwise Noted)

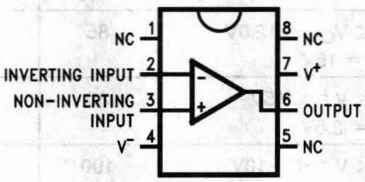
Feature	Value
Low offset voltage	100 μV
Ultra low supply current	20 μA
Operates from 4.5V to 15V single supply	
Ultra low input bias current	10 fA
Output swing within 10 mV of supply rail, 100k load	
Input common-mode range includes V^-	
High voltage gain	140 dB
Improved latchup immunity	

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



TL/H/11422–1

Top View

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
8-Pin Molded DIP	LMC6061AMN	LMC6061AIN LMC6061IN	N08E	Rail
8-Pin Small Outline		LMC6061AIM LMC6061IM	M08A	Rail Tape and Reel
8-Pin Ceramic DIP	LMC6061AMJ/883		J08A	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6061AM	$-55°C \le T_J \le +125°C$
LMC6061AI, LMC6082I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 11)	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
Power Dissipation	(Note 9)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		100	350 **1200**	350 **900**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift		1.0				μV/°C
I_B	Input Bias Current		0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current		0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance		>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	85	75 **70**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	85	75 **70**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	100	84 **70**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
			$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V Min
A_V	Large Signal Voltage Gain	$R_L = 100\ k\Omega$ (Note 7) Sourcing	4000	400 **200**	400 **300**	300 **200**	V/mV Min
		Sinking	3000	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 25\ k\Omega$ (Note 7) Sourcing	3000	400 **150**	400 **150**	200 **80**	V/mV Min
		Sinking	2000	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.995	4.990 **4.970**	4.990 **4.980**	4.950 **4.925**	V Min
			0.005	0.010 **0.030**	0.010 **0.020**	0.050 **0.075**	V Max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to 2.5V	4.990	4.975 **4.955**	4.975 **4.965**	4.950 **4.850**	V Min
			0.010	0.020 **0.045**	0.020 **0.035**	0.050 **0.150**	V Max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.990	14.975 **14.955**	14.975 **14.965**	14.950 **14.925**	V Min
			0.010	0.025 **0.050**	0.025 **0.035**	0.050 **0.075**	V Max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to 7.5V	14.965	14.900 **14.800**	14.900 **14.850**	14.850 **14.800**	V Min
			0.025	0.050 **0.200**	0.050 **0.150**	0.100 **0.200**	V Max
I_O	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, $V_O = 5V$	21	16 **7**	16 **8**	16 **8**	mA Min
I_O	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	25	15 **9**	15 **10**	15 **10**	mA Min
		Sinking, $V_O = 13V$ (Note 10)	35	24 **7**	24 **8**	24 **8**	mA Min
I_S	Supply Current	$V^+ = +5V$, $V_O = 1.5V$	20	24 **35**	24 **32**	32 **40**	μA Max
		$V^+ = +15V$, $V_O = 7.5V$	24	30 **40**	30 **38**	40 **48**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	35	20 **8**	20 **10**	15 **7**	V/ms Min
GBW	Gain-Bandwidth Product		100				kHz
θ_m	Phase Margin		50				Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	83				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{PP}$ ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

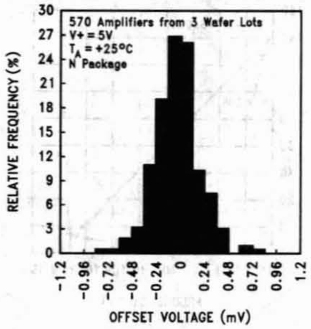
Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.

Note 11: All numbers apply for packages soldered directly into a PC board.

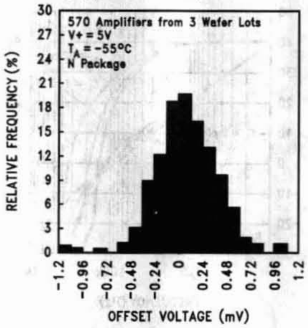
Note 12: For guaranteed Military Temperature Range parameters see RETSMC6061X.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

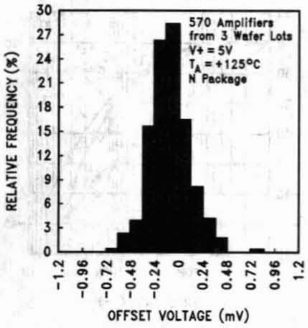
Distribution of LMC6061 Input Offset Voltage ($T_A = +25°C$)



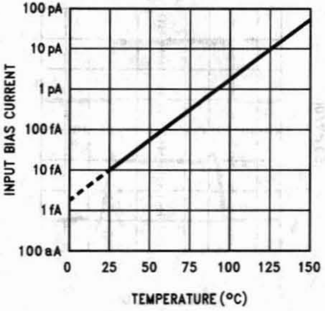
Distribution of LMC6061 Input Offset Voltage ($T_A = -55°C$)



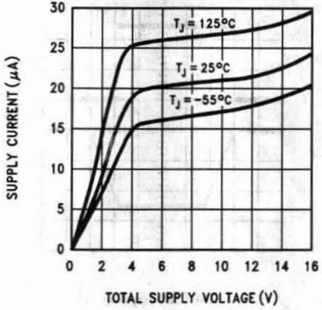
Distribution of LMC6061 Input Offset Voltage ($T_A = +125°C$)



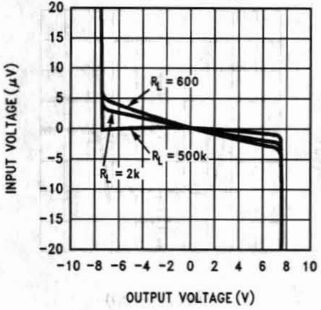
Input Bias Current vs Temperature



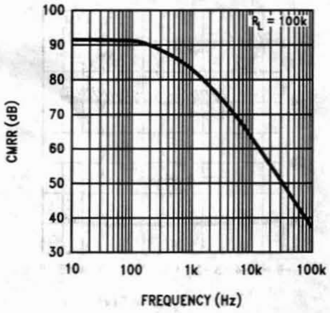
Supply Current vs Supply Voltage



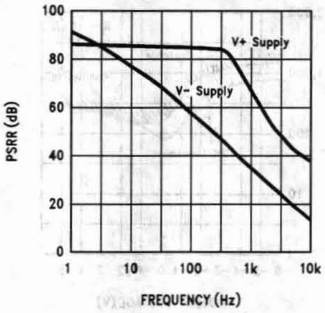
Input Voltage vs Output Voltage



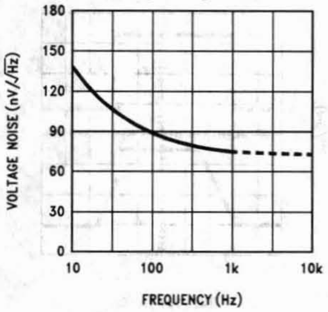
Common Mode Rejection Ratio vs Frequency



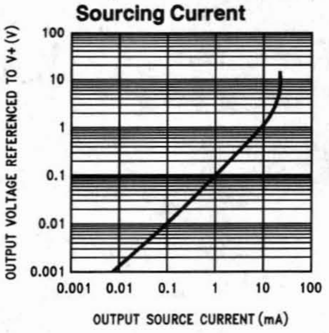
Power Supply Rejection Ratio vs Frequency



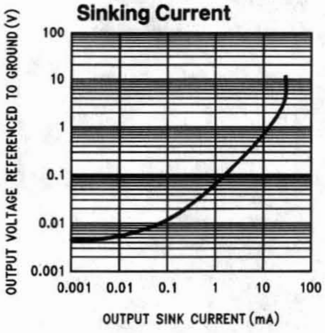
Input Voltage Noise vs Frequency



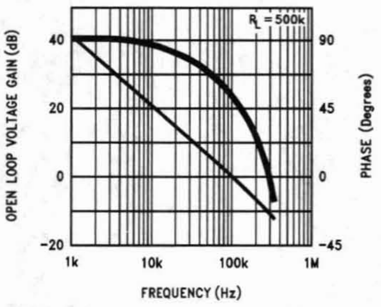
Output Characteristics Sourcing Current



Output Characteristics Sinking Current

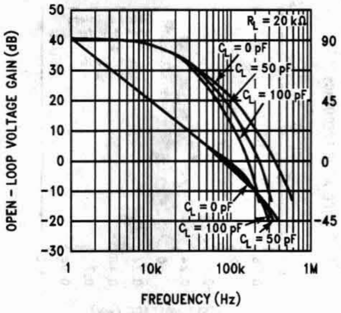


Gain and Phase Response vs Temperature (−55°C to +125°C)

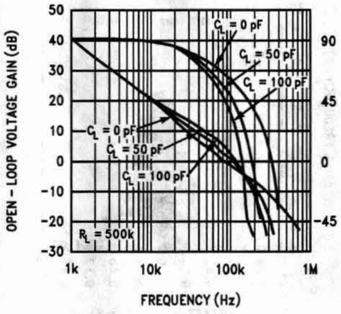


TL/H/11422–2

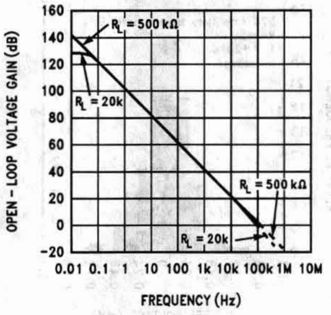
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified



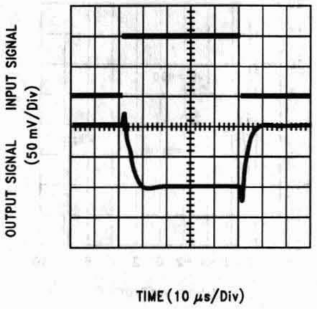
Gain and Phase Response vs Capacitive Load with $R_L = 20\ k\Omega$



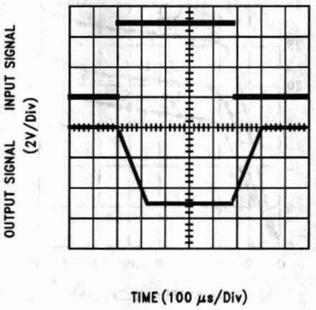
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$



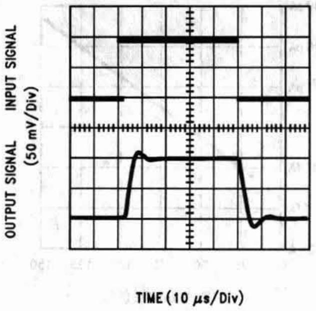
Open Loop Frequency Response



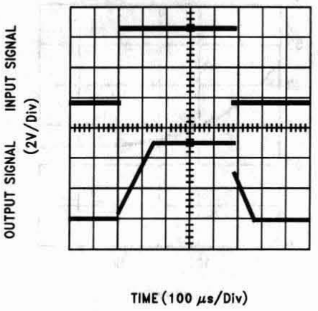
Inverting Small Signal Pulse Response



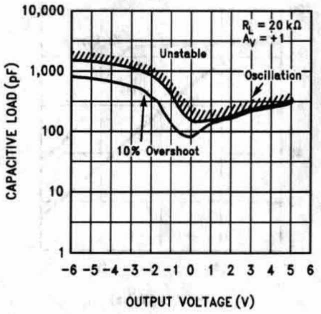
Inverting Large Signal Pulse Response



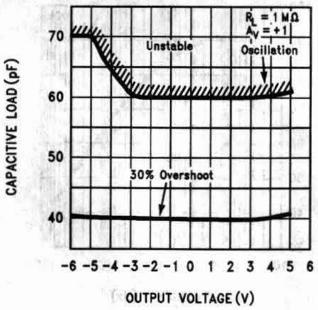
Non-Inverting Small Signal Pulse Response



Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load, $R_L = 20\ k\Omega$



Stability vs Capacitive Load $R_L = 1\ M\Omega$

TL/H/11422–3

Applications Hints

AMPLIFIER TOPOLOGY

The LMC6061 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6061 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6061.

Although the LMC6061 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6061 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See ***Printed-Circuit-Board Layout for High Impedance Work***).

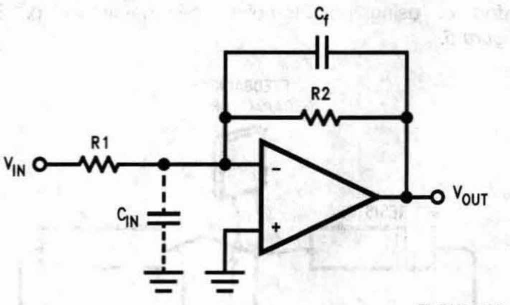
The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \ge \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \le R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.



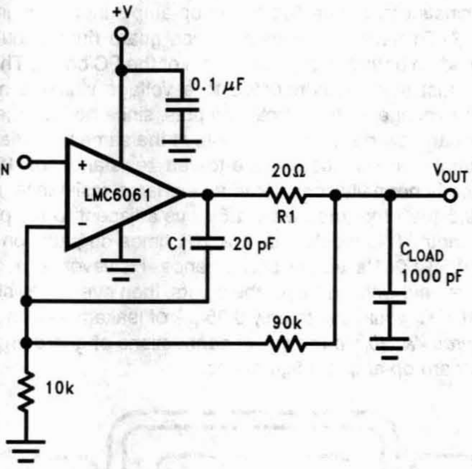
TL/H/11422–5

FIGURE 1. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

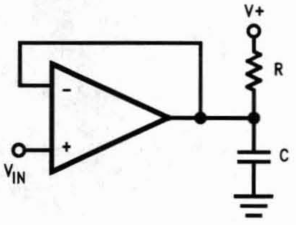


TL/H/11422–4

FIGURE 2a. LMC6061 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b)*. Typically a pull up resistor conducting 10 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see electrical characteristics).



TL/H/11422–14

FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6061, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are

Applications Hints (Continued)

quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6061's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 3.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6061's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.

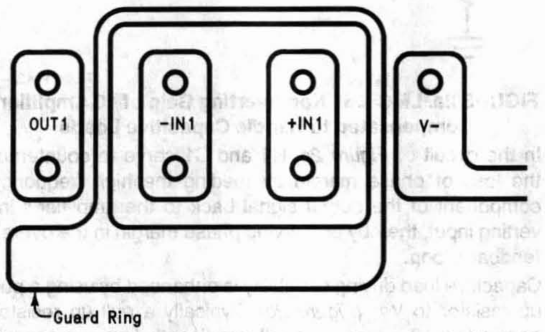


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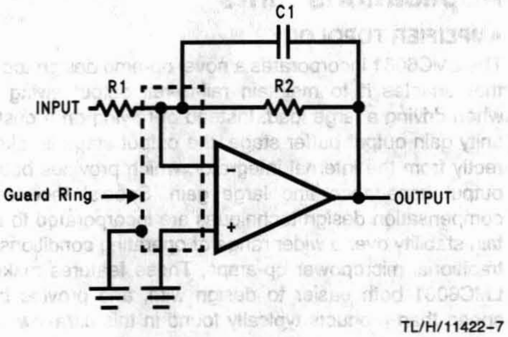
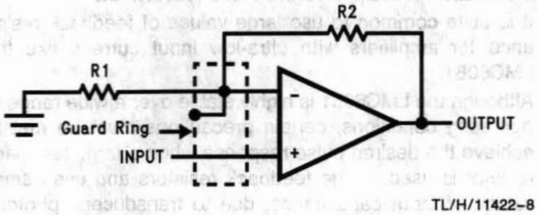
FIGURE 3. Example of Guard Ring in P.C. Board Layout



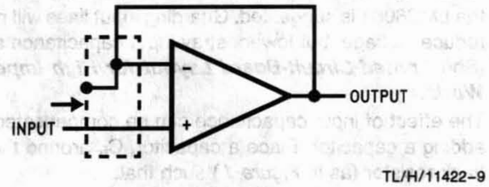
TL/H/11422-7

(a) Inverting Amplifier



TL/H/11422-8

(b) Non-Inverting Amplifier

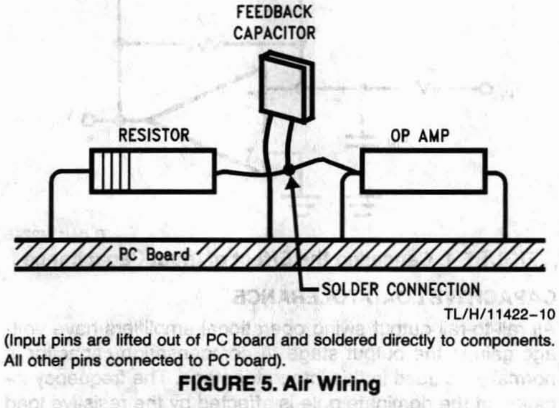


TL/H/11422-9

(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5.*



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring

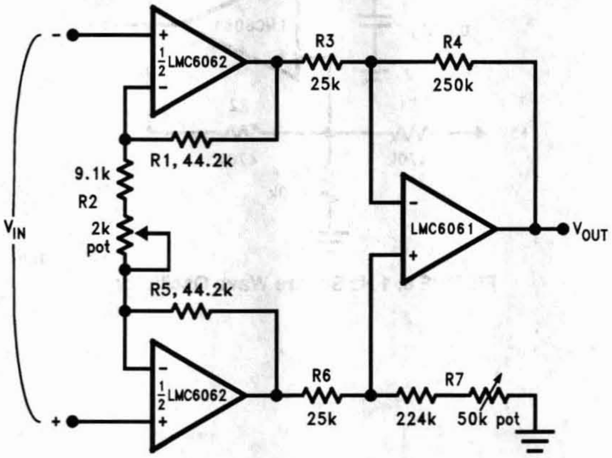
Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6061 and LMC6081 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6061 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 100$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



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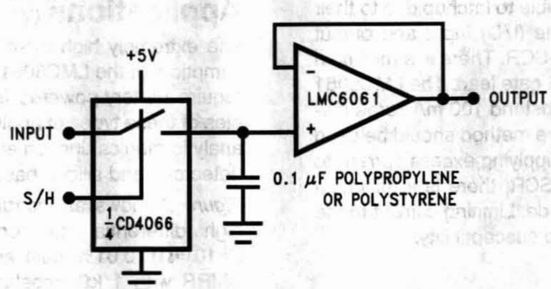
If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications ($V^{+} = 5.0\ V_{DC}$) (Continued)


+5V
INPUT
S/H
$\frac{1}{4}$CD4066
0.1 μF POLYPROPYLENE
OR POLYSTYRENE
LMC6061
OUTPUT

TL/H/11422–12

FIGURE 7. Low-Leakage Sample and Hold

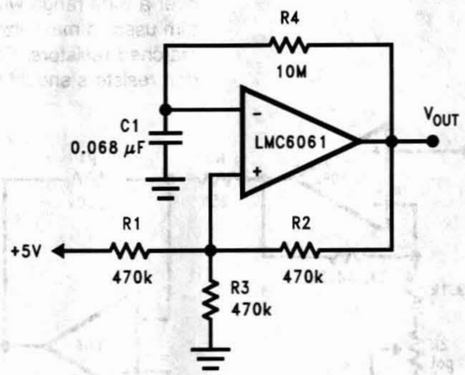

R4
10M
C1
0.068 μF
LMC6061
V_{OUT}
R1
470k
+5V
R2
470k
R3
470k

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FIGURE 8. 1 Hz Square Wave Oscillator

National Semiconductor

LMC6062 Precision CMOS Dual Micropower Operational Amplifier

General Description

The LMC6062 is a precision dual low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6062 ideally suited for battery powered applications.

Other applications using the LMC6062 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6082 precision dual operational amplifier.

PATENT PENDING

Features (Typical Unless Otherwise Noted)

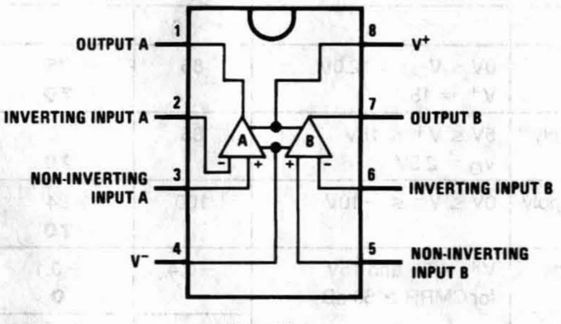
Low offset voltage	100 μV
Ultra low supply current	16 μA/Amplifier
Operates from 4.5V to 15V single supply	
Ultra low input bias current	10 fA
Output swing within 10 mV of supply rail, 100k load	
Input common-mode range includes V^-	
High voltage gain	140 dB
Improved latchup immunity	

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



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Top View

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
8-Pin Molded DIP	LMC6062AMN	LMC6062AIN LMC6062IN	N08E	Rail
8-Pin Small Outline		LMC6062AIM LMC6062IM	M08A	Rail Tape and Reel
8-Pin Ceramic DIP	LMC6062AMJ/883		J08A	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6062AM	$-55°C \le T_J \le +125°C$
LMC6062AI, LMC6082I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 12)	
8-Pin Molded DIP	115°C/W
8-Pin SO	193°C/W
Power Dissipation	(Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6062AM Limit (Note 6)	LMC6062AI Limit (Note 6)	LMC6062I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			100	350 **1200**	350 **900**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75 **70**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75 **70**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		100	84 **70**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V Min
A_V	Large Signal Voltage Gain	$R_L = 100\ k\Omega$ (Note 7)	Sourcing	4000	400 **200**	400 **300**	300 **200**	V/mV Min
			Sinking	3000	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 25\ k\Omega$ (Note 7)	Sourcing	3000	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	2000	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6062AM Limit (Note 6)	LMC6062AI Limit (Note 6)	LMC6062I Limit (Note 6)	Units
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.995	4.990 **4.970**	4.990 **4.980**	4.950 **4.925**	V Min
			0.005	0.010 **0.030**	0.010 **0.020**	0.050 **0.075**	V Max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to 2.5V	4.990	4.975 **4.955**	4.975 **4.965**	4.950 **4.850**	V Min
			0.010	0.020 **0.045**	0.020 **0.035**	0.050 **0.150**	V Max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.990	14.975 **14.955**	14.975 **14.965**	14.950 **14.925**	V Min
			0.010	0.025 **0.050**	0.025 **0.035**	0.050 **0.075**	V Max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to 7.5V	14.965	14.900 **14.800**	14.900 **14.850**	14.850 **14.800**	V Min
			0.025	0.050 **0.200**	0.050 **0.150**	0.100 **0.200**	V Max
I_O	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, $V_O = 5V$	21	16 **7**	16 **8**	16 **8**	mA Min
I_O	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	25	15 **9**	15 **10**	15 **10**	mA Min
		Sinking, $V_O = 13V$ (Note 11)	35	24 **7**	24 **8**	24 **8**	mA Min
I_S	Supply Current	Both Amplifiers $V^+ = +5V$, $V_O = 1.5V$	32	38 **60**	38 **46**	46 **56**	μA Max
		Both Amplifiers $V^+ = +15V$, $V_O = 7.5V$	40	47 **70**	47 **55**	57 **66**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6062AM Limit (Note 6)	LMC6062AI Limit (Note 6)	LMC6062I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	35	20 **8**	20 **10**	15 **7**	V/ms Min
GBW	Gain-Bandwidth Product		100				kHz
θ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	(Note 9)	155				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	$F = 1\ kHz, A_V = -5$ $R_L = 100\ k\Omega, V_O = 2\ V_{PP}$ ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 100 Hz to produce $V_O = 12\ V_{PP}$.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

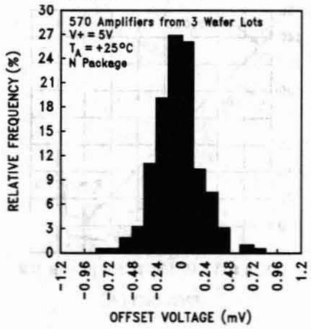
Note 11: Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.

Note 12: All numbers apply for packages soldered directly into a PC board.

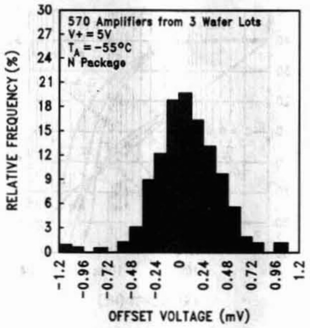
Note 13: For guaranteed Military Temperature Range parameters, see RETSMC6062X.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

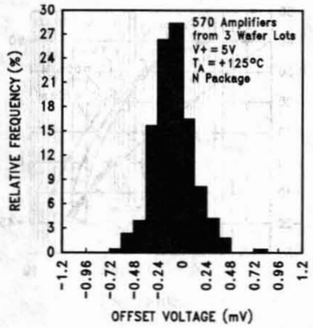
Distribution of LMC6062 Input Offset Voltage ($T_A = +25°C$)



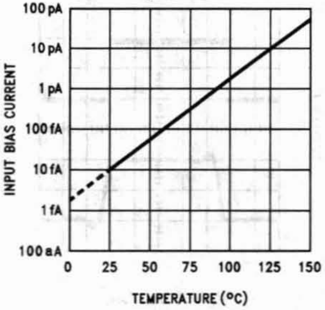
Distribution of LMC6062 Input Offset Voltage ($T_A = -55°C$)



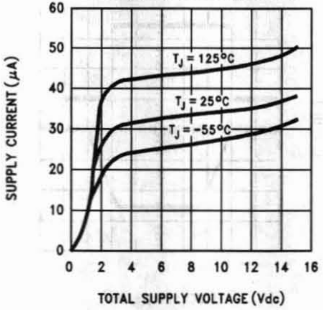
Distribution of LMC6062 Input Offset Voltage ($T_A = +125°C$)



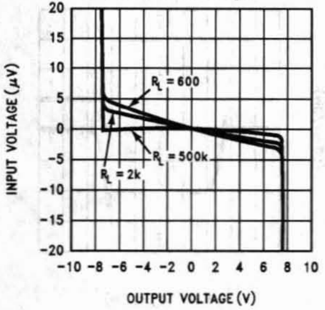
Input Bias Current vs Temperature



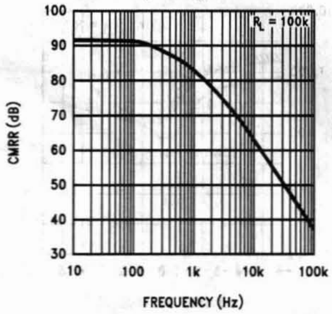
Supply Current vs Supply Voltage



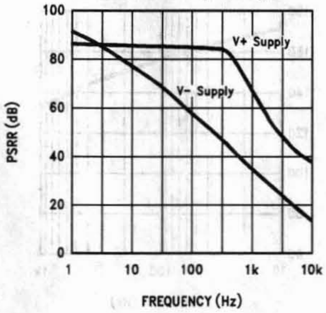
Input Voltage vs Output Voltage



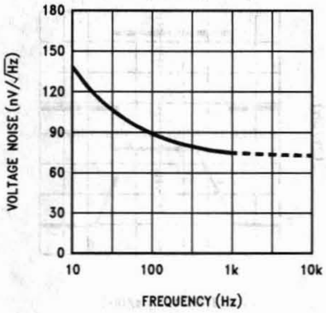
Common Mode Rejection Ratio vs Frequency



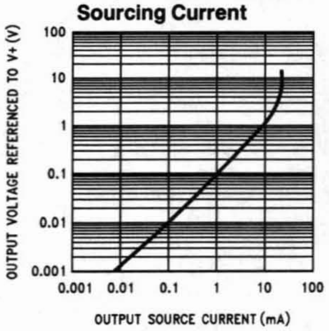
Power Supply Rejection Ratio vs Frequency



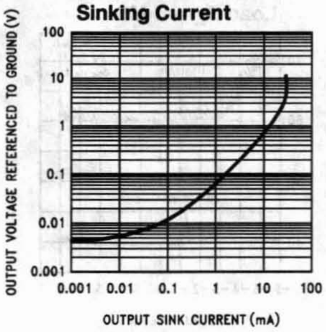
Input Voltage Noise vs Frequency



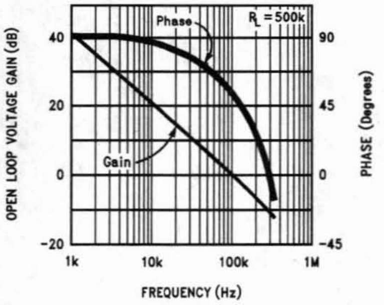
Output Characteristics Sourcing Current



Output Characteristics Sinking Current

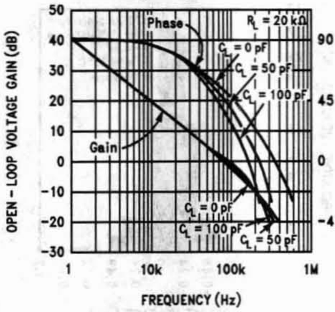


Gain and Phase Response vs Temperature ($-55°C$ to $+125°C$)

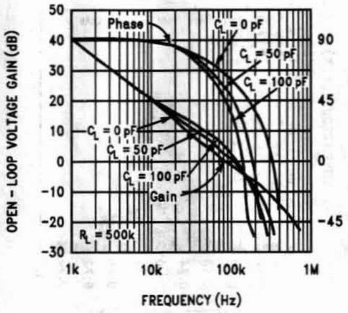


TL/H/11298–2

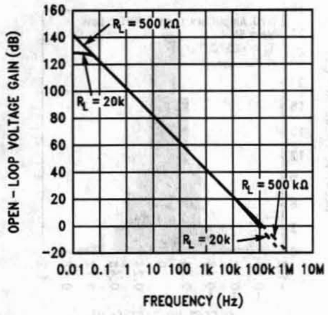
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified



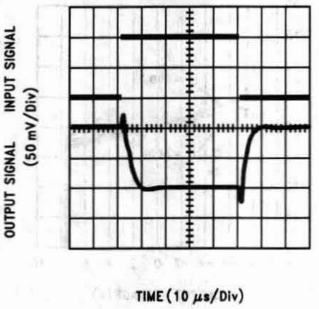
Gain and Phase Response vs Capacitive Load with $R_L = 20\ k\Omega$



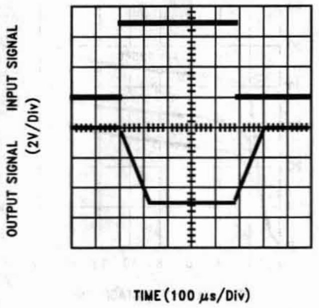
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$



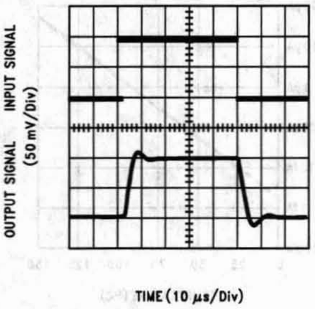
Open Loop Frequency Response



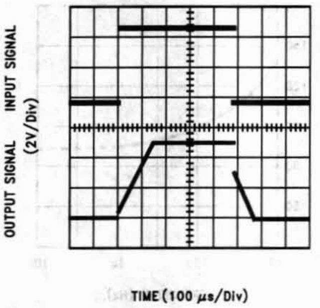
Inverting Small Signal Pulse Response



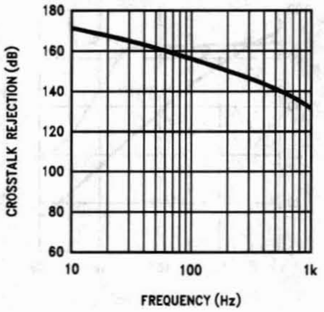
Inverting Large Signal Pulse Response



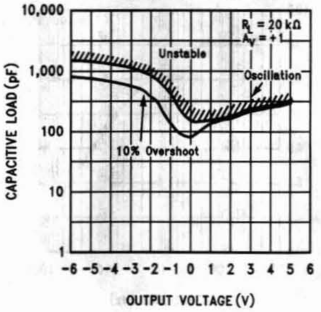
Non-Inverting Small Signal Pulse Response



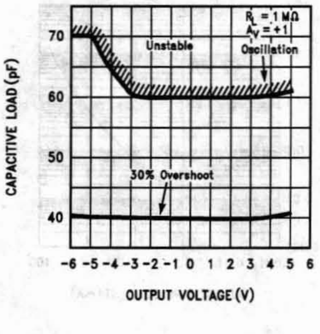
Non-Inverting Large Signal Pulse Response



Crosstalk Rejection vs Frequency



Stability vs Capacitive Load, $R_L = 20\ k\Omega$



Stability vs Capacitive Load $R_L = 1\ M\Omega$

TL/H/11298–3

Applications Hints

AMPLIFIER TOPOLOGY

The LMC6062 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6062 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6062.

Although the LMC6062 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6062 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See ***Printed-Circuit-Board Layout for High Impedance Work***).

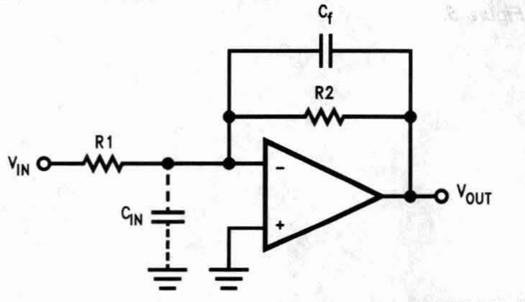
The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1\, C_{IN} \leq R_2\, C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.



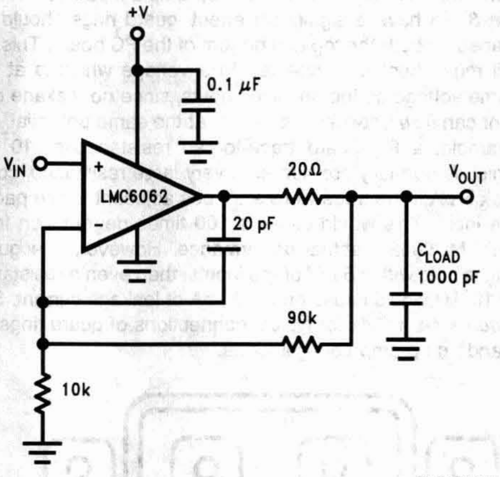
TL/H/11298-4

FIGURE 1. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a.*



TL/H/11298-5

FIGURE 2a. LMC6062 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b)*. Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

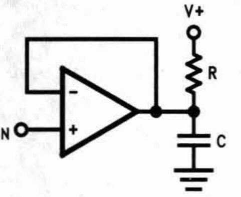


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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6062, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are

Applications Hints (Continued)

quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6062's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 3.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6062's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.

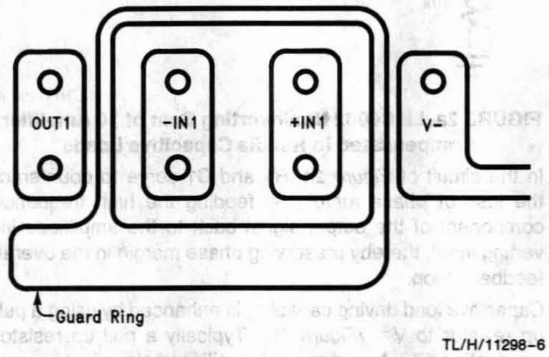
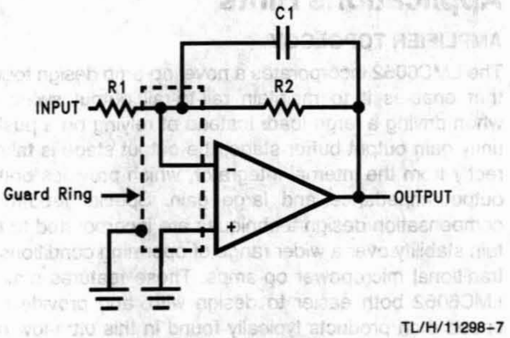
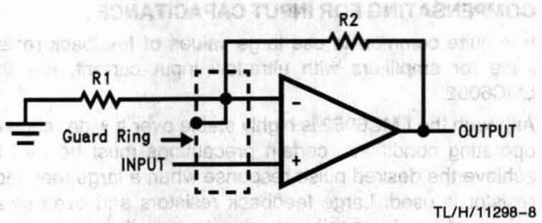


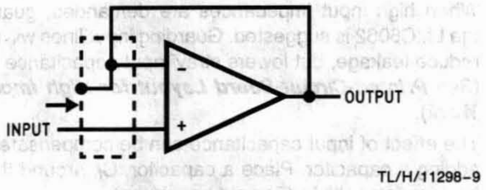
FIGURE 3. Example of Guard Ring in P.C. Board Layout



(a) Inverting Amplifier



(b) Non-Inverting Amplifier



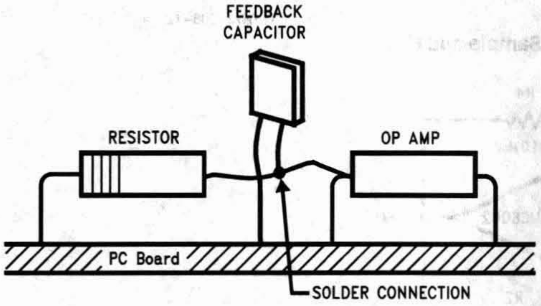
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5.*

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6062 and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



TL/H/11298–10

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

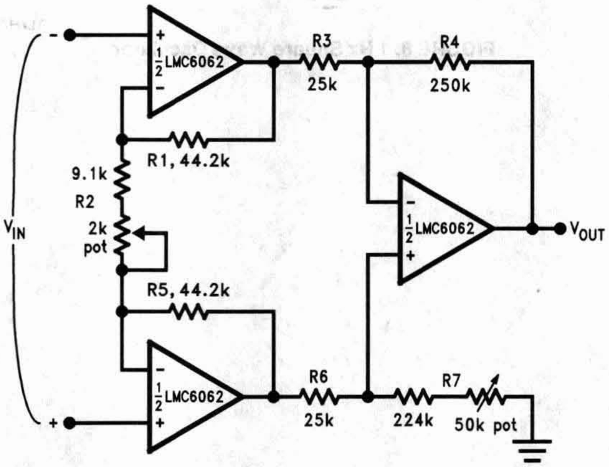
FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6062 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 100$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



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If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

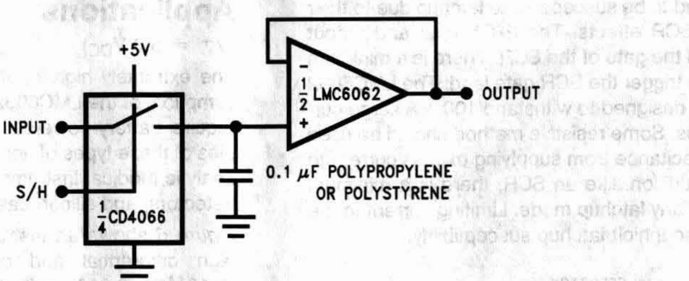

+5V
INPUT
S/H
$\frac{1}{4}$ CD4066
$\frac{1}{2}$ LMC6062
OUTPUT
0.1 µF POLYPROPYLENE
OR POLYSTYRENE
TL/H/11298-12

FIGURE 7. Low-Leakage Sample and Hold

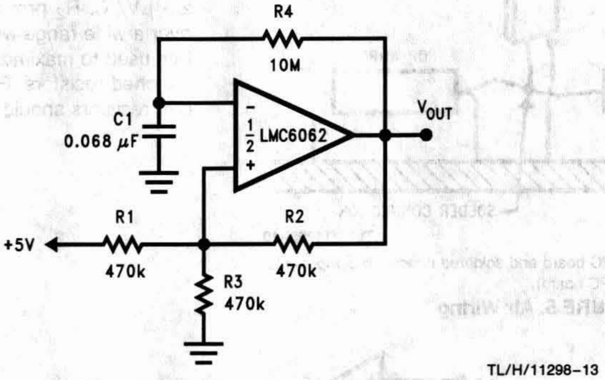

R4
10M
C1
0.068 µF
$\frac{1}{2}$ LMC6062
V_{OUT}
R1
470k
+5V
R2
470k
R3
470k
TL/H/11298-13

FIGURE 8. 1 Hz Square Wave Oscillator

National Semiconductor

LMC6064 Precision CMOS Quad Micropower Operational Amplifier

General Description

The LMC6064 is a precision quad low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption make the LMC6064 ideally suited for battery powered applications.

Other applications using the LMC6064 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6084 precision quad operational amplifier.

For single or dual operational amplifier with similar features, see the LMC6061 or LMC6062 respectively.

PATENT PENDING

Features (Typical Unless Otherwise Noted)

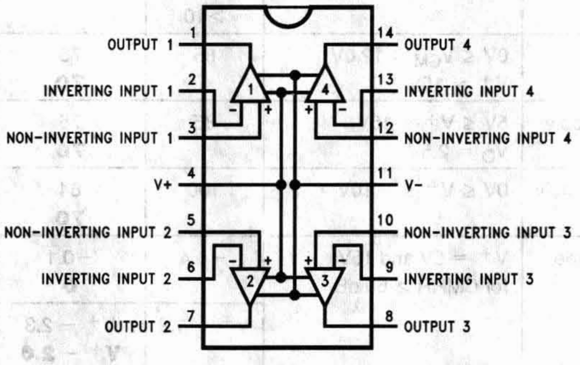
■ Low offset voltage	100 μV
■ Ultra low supply current	16 μA/Amplifier
■ Operates from 4.5V to 15V single supply	
■ Ultra low input bias current	10 fA
■ Output swing within 10 mV of supply rail, 100k load	
■ Input common-mode range includes V$^-$	
■ High voltage gain	140 dB
■ Improved latchup immunity	

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

14-Pin DIP/SO



OUTPUT 1
INVERTING INPUT 1
NON-INVERTING INPUT 1
V+
NON-INVERTING INPUT 2
INVERTING INPUT 2
OUTPUT 2
1
2
3
4
5
6
7
14
13
12
11
10
9
8
OUTPUT 4
INVERTING INPUT 4
NON-INVERTING INPUT 4
V-
NON-INVERTING INPUT 3
INVERTING INPUT 3
OUTPUT 3

TL/H/11466-1

Top View

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
14-Pin Molded DIP	LMC6064AMN	LMC6064AIN LMC6064IN	N14A	Rail
14-Pin Small Outline		LMC6064AIM LMC6064IM	M14A	Rail Tape and Reel
14-Pin Ceramic DIP	LMC6064AMJ		J14A	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage $(V^+ - V^-)$	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6064AM	$-55°C \le T_J \le +125°C$
LMC6064AI, LMC6064I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 12)	
14-Pin Molded DIP	81°C/W
14-Pin SO	126°C/W
Power Dissipation	(Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6064AM Limit (Note 6)	LMC6064AI Limit (Note 6)	LMC6064I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			100	350 **1200**	350 **900**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75 **70**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75 **70**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		100	84 **70**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V Min
A_V	Large Signal Voltage Gain	$R_L = 100\ k\Omega$ (Note 7)	Sourcing	4000	400 **200**	400 **300**	300 **200**	V/mV Min
			Sinking	3000	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 25\ k\Omega$ (Note 7)	Sourcing	3000	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	2000	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6064AM Limit (Note 6)	LMC6064AI Limit (Note 6)	LMC6064I Limit (Note 6)	Units
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.995	4.990 **4.970**	4.990 **4.980**	4.950 **4.925**	V Min
			0.005	0.010 **0.030**	0.010 **0.020**	0.050 **0.075**	V Max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to 2.5V	4.990	4.975 **4.955**	4.975 **4.965**	4.950 **4.850**	V Min
			0.010	0.020 **0.045**	0.020 **0.035**	0.050 **0.150**	V Max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.990	14.975 **14.955**	14.975 **14.965**	14.950 **14.925**	V Min
			0.010	0.025 **0.050**	0.025 **0.035**	0.050 **0.075**	V Max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to 7.5V	14.965	14.900 **14.800**	14.900 **14.850**	14.850 **14.800**	V Min
			0.025	0.050 **0.200**	0.050 **0.150**	0.100 **0.200**	V Max
I_O	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, $V_O = 5V$	21	16 **7**	16 **8**	16 **8**	mA Min
I_O	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	25	15 **9**	15 **10**	15 **10**	mA Min
		Sinking, $V_O = 13V$ (Note 11)	35	24 **7**	24 **8**	24 **8**	mA Min
I_S	Supply Current	All Four Amplifiers $V^+ = +5V$, $V_O = 1.5V$	64	76 **120**	76 **92**	92 **112**	μA Max
		All Four Amplifiers $V^+ = +15V$, $V_O = 7.5V$	80	94 **140**	94 **110**	114 **132**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6064AM Limit (Note 6)	LMC6064AI Limit (Note 6)	LMC6064I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	35	20 **8**	20 **10**	15 **7**	V/ms Min
GBW	Gain-Bandwidth Product		100				kHz
θ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	(Note 9)	155				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{PP}$ ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 100 Hz to produce $V_O = 12\ V_{PP}$.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

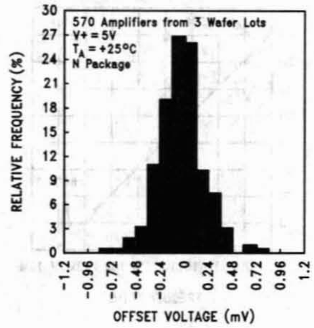
Note 11: Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.

Note 12: All numbers apply for packages soldered directly into a PC board.

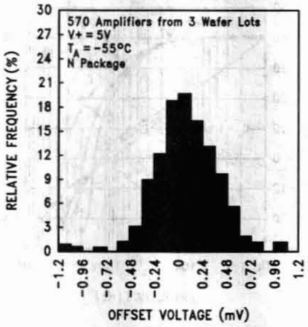
Note 13: For guaranteed Military Temperature Range parameters see RETSMC6064X.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

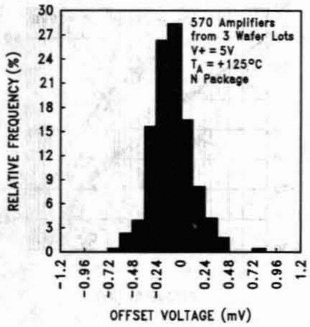
Distribution of LMC6064 Input Offset Voltage ($T_A = +25°C$)



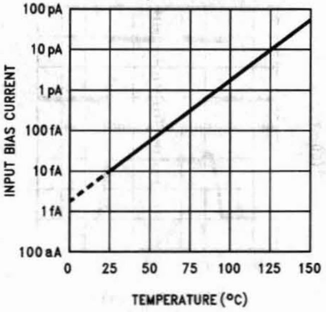
Distribution of LMC6064 Input Offset Voltage ($T_A = -55°C$)



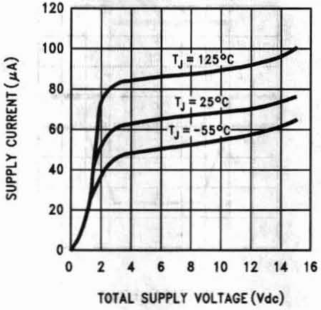
Distribution of LMC6064 Input Offset Voltage ($T_A = +125°C$)



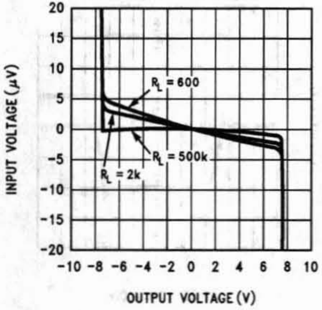
Input Bias Current vs Temperature



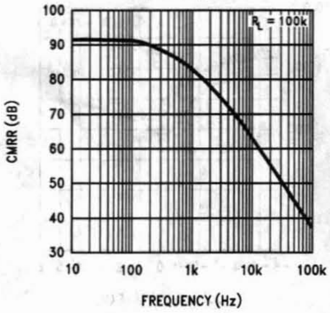
Supply Current vs Supply Voltage



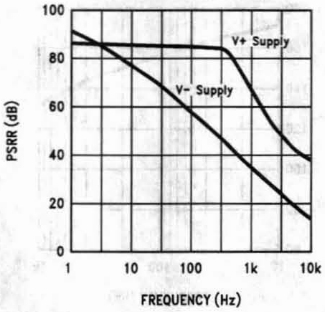
Input Voltage vs Output Voltage



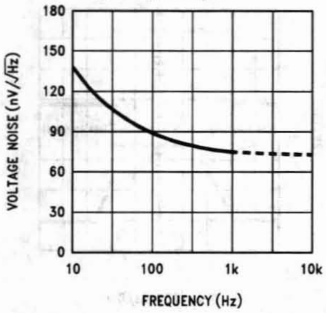
Common Mode Rejection Ratio vs Frequency



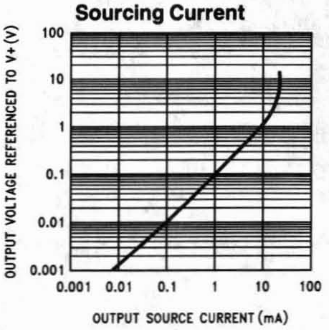
Power Supply Rejection Ratio vs Frequency



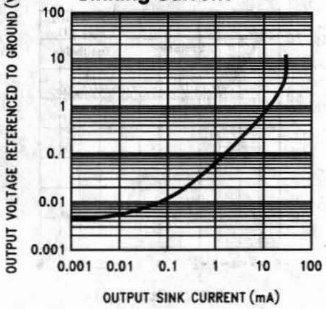
Input Voltage Noise vs Frequency



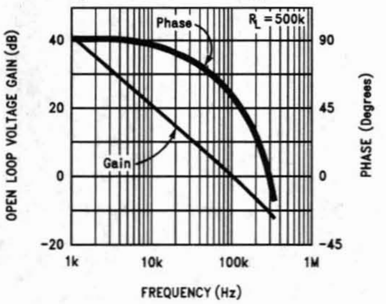
Output Characteristics Sourcing Current



Output Characteristics Sinking Current



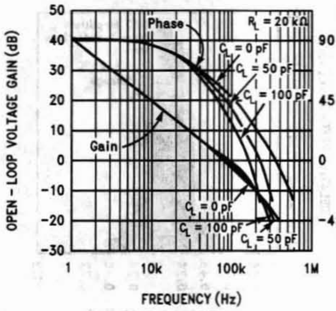
Gain and Phase Response vs Temperature (−55°C to +125°C)



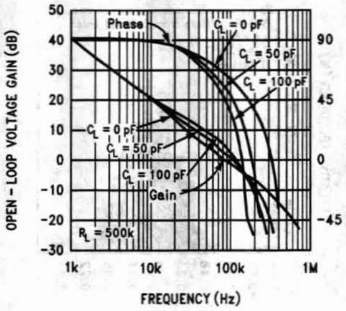
TL/H/11466–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

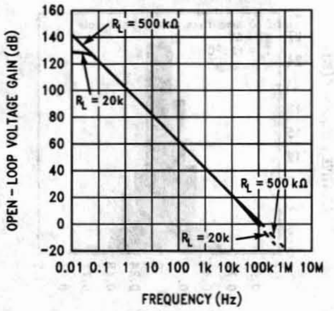
Gain and Phase Response vs Capacitive Load with $R_L = 20\ k\Omega$



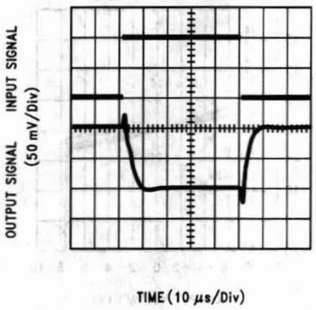
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$



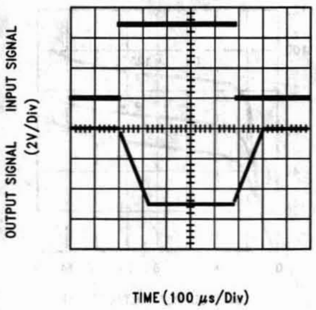
Open Loop Frequency Response



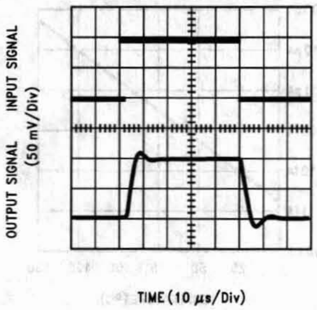
Inverting Small Signal Pulse Response



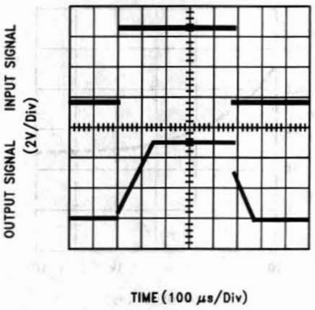
Inverting Large Signal Pulse Response



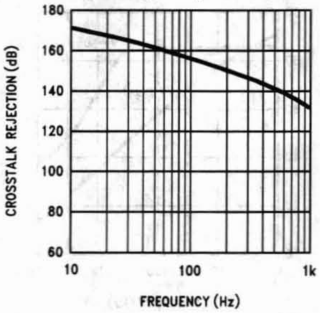
Non-Inverting Small Signal Pulse Response



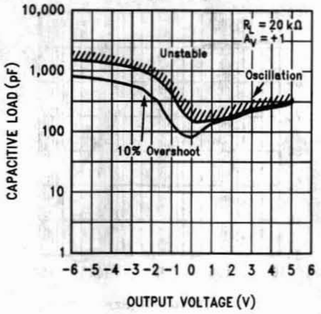
Non-Inverting Large Signal Pulse Response



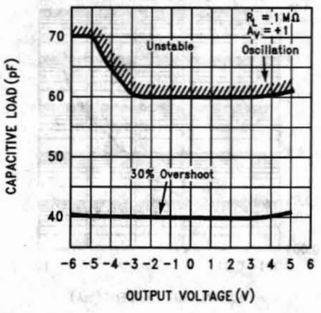
Crosstalk Rejection vs Frequency



Stability vs Capacitive Load, $R_L = 20\ k\Omega$



Stability vs Capacitive Load $R_L = 1\ M\Omega$



TL/H/11466–3

Applications Hints

AMPLIFIER TOPOLOGY

The LMC6064 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6064 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6064.

Although the LMC6064 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6064 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See ***Printed-Circuit-Board Layout for High Impedance Work***).

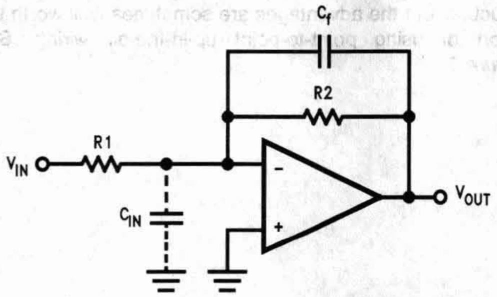
The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.



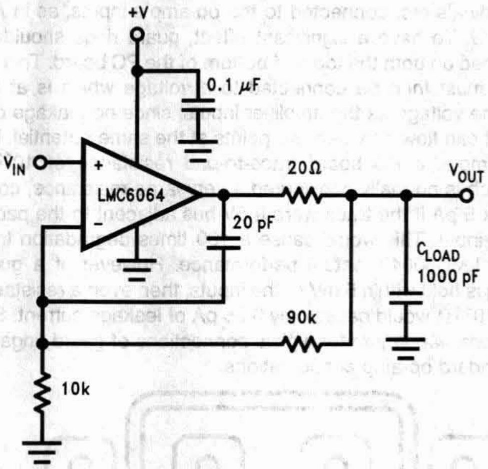
TL/H/11466-4

FIGURE 1. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a.*

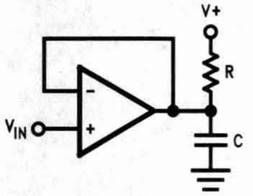


TL/H/11466-5

FIGURE 2a. LMC6064 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 2b)*. Typically a pull up resistor conducting 10 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



TL/H/11466-6

FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

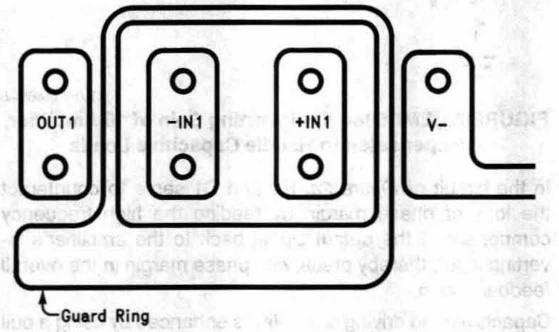
PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6064, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are

Applications Hints (Continued)

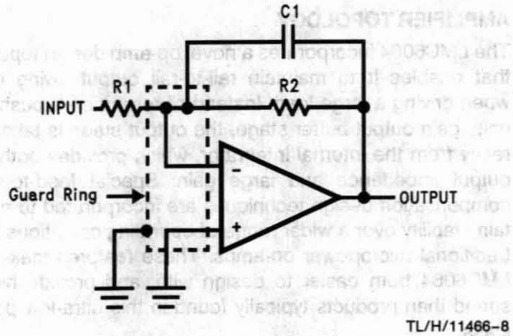
quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6064's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 3.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6064's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.



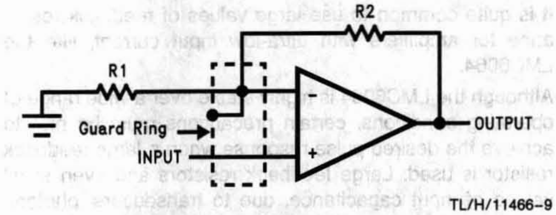
TL/H/11466–7

FIGURE 3. Example of Guard Ring in P.C. Board Layout



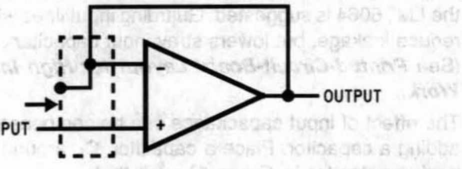
TL/H/11466–8

(a) Inverting Amplifier



TL/H/11466–9

(b) Non-Inverting Amplifier



TL/H/11466–10

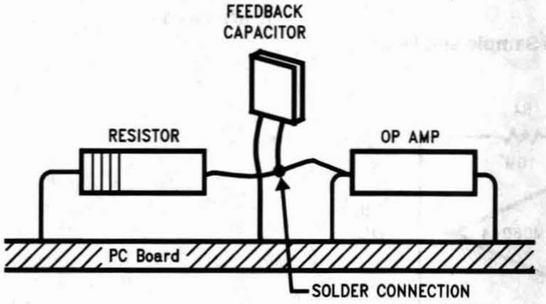
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5.*

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6064 and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



TL/H/11466–11

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

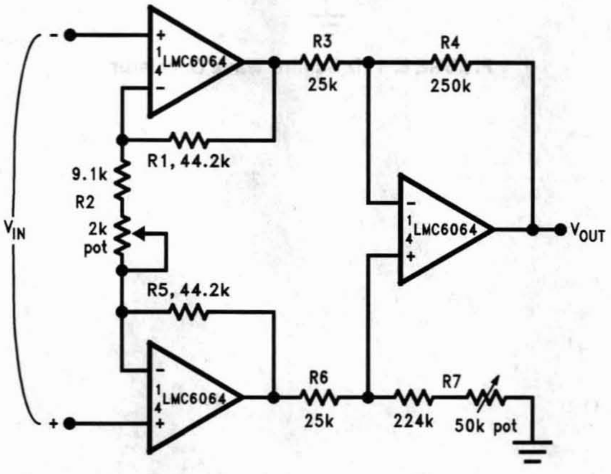
FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6064 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 100$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



TL/H/11466–12

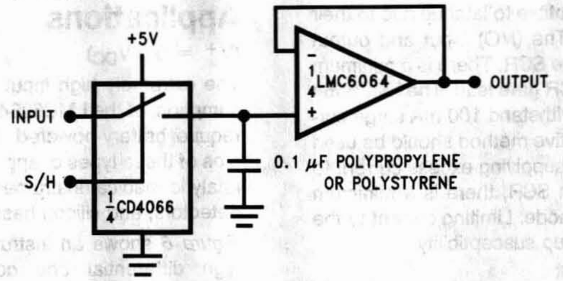
If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

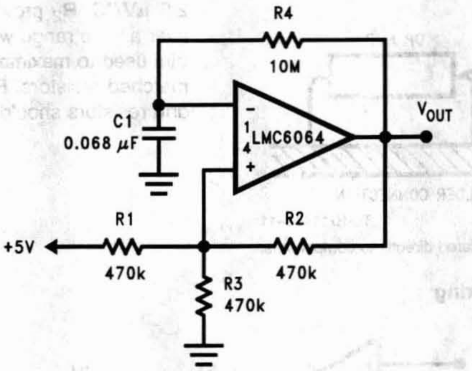
FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)


+5V
INPUT
S/H
$\frac{1}{4}$ CD4066
−
+
$\frac{1}{4}$ LMC6064
OUTPUT
0.1 μF POLYPROPYLENE
OR POLYSTYRENE

TL/H/11466–13

FIGURE 7. Low-Leakage Sample and Hold


R4
10M
C1
0.068 μF
−
+
$\frac{1}{4}$ LMC6064
V_{OUT}
R1
470k
+5V
R2
470k
R3
470k

TL/H/11466–14

FIGURE 8. 1 Hz Square Wave Oscillator

National Semiconductor

LMC6081 Precision CMOS Single Operational Amplifier

General Description

The LMC6081 is a precision low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6081 ideally suited for precision circuit applications.

Other applications using the LMC6081 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6061 precision micropower operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6082 or LMC6084 respectively.

PATENT PENDING

Features (Typical unless otherwise stated)

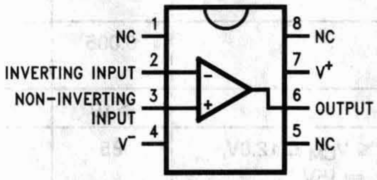
- Low offset voltage 150 μV
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



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Top View

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
8-Pin Molded DIP	LMC6081AMN	LMC6081AIN LMC6081IN	N08E	Rail
8-Pin Small Outline		LMC6081AIM LMC6081IM	M08A	Rail Tape and Reel

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	(V+) +0.3V, (V−) −0.3V
Supply Voltage (V+ − V−)	16V
Output Short Circuit to V+	(Note 10)
Output Short Circuit to V−	(Note 2)
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6081AM	$-55°C \le T_J \le +125°C$
LMC6081AI, LMC6081I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}), (Note 11)	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
Power Dissipation (Note 9)	

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6081AM Limit (Note 6)	LMC6081AI Limit (Note 6)	LMC6081I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			150	350 **1000**	350 **800**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	**100**	**4**	**4**	pA Max
I_{OS}	Input Offset Current			0.005	**100**	**2**	**2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75 **72**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75 **72**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		94	84 **81**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V Min
A_V	Large Signal Voltage Gain	$R_L = 2\ k\Omega$ (Note 7)	Sourcing	1400	400 **300**	400 **300**	300 **200**	V/mV Min
			Sinking	350	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 600\Omega$ (Note 7)	Sourcing	1200	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	150	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6081AM Limit (Note 6)	LMC6081AI Limit (Note 6)	LMC6081I Limit (Note 6)	Units
V_O	Output Swing	$V^+ = 5V$ $R_L = 2\ k\Omega$ to 2.5V	4.87	4.80 **4.70**	4.80 **4.73**	4.75 **4.67**	V Min
			0.10	0.13 **0.19**	0.13 **0.17**	0.20 **0.24**	V Max
		$V^+ = 5V$ $R_L = 600\Omega$ to 2.5V	4.61	4.50 **4.24**	4.50 **4.31**	4.40 **4.21**	V Min
			0.30	0.40 **0.63**	0.40 **0.50**	0.50 **0.63**	V Max
		$V^+ = 15V$ $R_L = 2\ k\Omega$ to 7.5V	14.63	14.50 **14.30**	14.50 **14.34**	14.37 **14.25**	V Min
			0.26	0.35 **0.48**	0.35 **0.45**	0.44 **0.56**	V Max
		$V^+ = 15V$ $R_L = 600\Omega$ to 7.5V	13.90	13.35 **12.80**	13.35 **12.86**	12.92 **12.44**	V Min
			0.79	1.16 **1.42**	1.16 **1.32**	1.33 **1.58**	V Max
I_O	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, $V_O = 5V$	21	16 **11**	16 **13**	13 **10**	mA Min
I_O	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	30	28 **18**	28 **22**	23 **18**	mA Min
		Sinking, $V_O = 13V$ (Note 10)	34	28 **19**	28 **22**	23 **18**	mA Min
I_S	Supply Current	$V^+ = +5V$, $V_O = 1.5V$	450	750 **900**	750 **900**	750 **900**	μA Max
		$V^+ = +15V$, $V_O = 7.5V$	550	850 **950**	850 **950**	850 **950**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6081AM Limit (Note 6)	LMC6081AI Limit (Note 6)	LMC6081 Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.5	0.8 **0.5**	0.8 **0.6**	0.8 **0.6**	V/μs Min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕ_m	Phase Margin		50				Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 10 kHz, $A_V = -10$ $R_L = 2\ k\Omega$, $V_O = 8\ V_{PP}$ ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

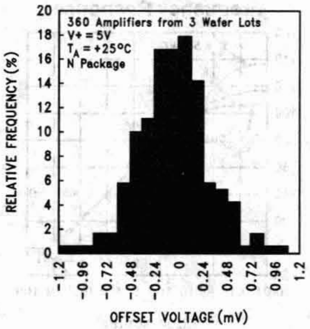
Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

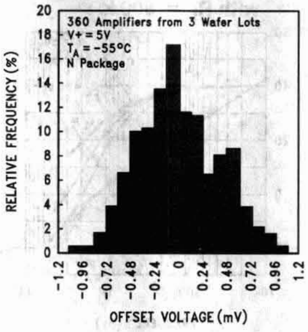
Note 11: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

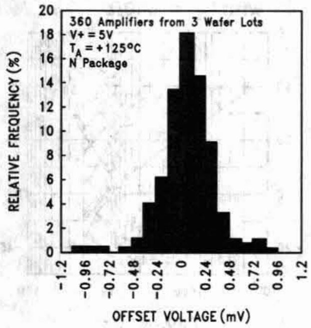
Distribution of LMC6081 Input Offset Voltage ($T_A = +25°C$)



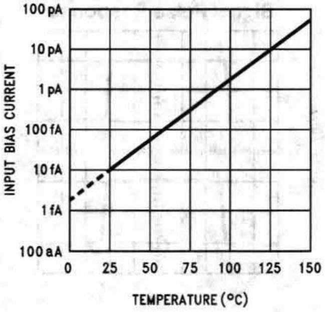
Distribution of LMC6081 Input Offset Voltage ($T_A = -55°C$)



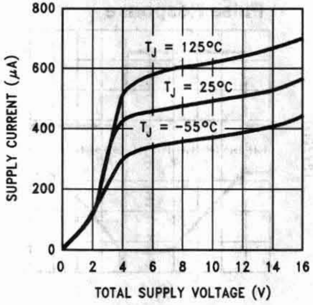
Distribution of LMC6081 Input Offset Voltage ($T_A = +125°C$)



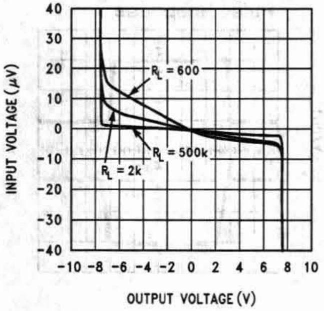
Input Bias Current vs Temperature



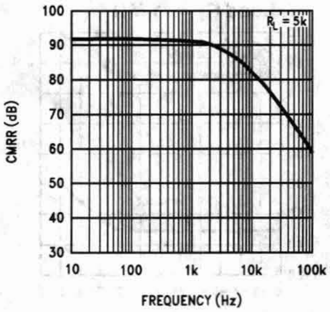
Supply Current vs Supply Voltage



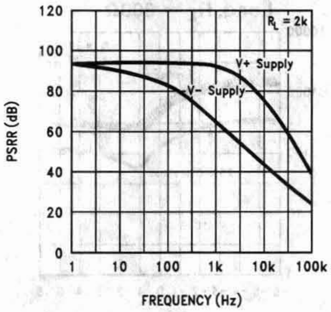
Input Voltage vs Output Voltage



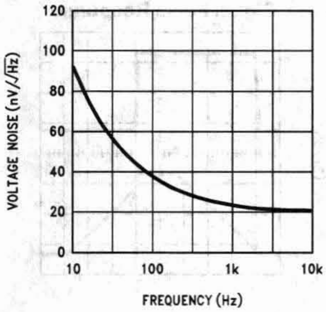
Common Mode Rejection Ratio vs Frequency



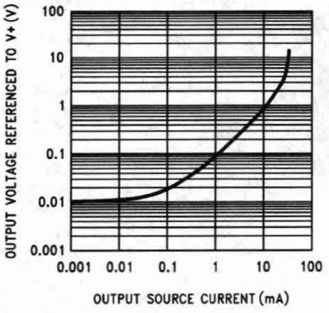
Power Supply Rejection Ratio vs Frequency



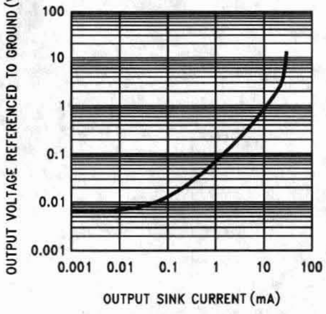
Input Voltage Noise vs Frequency



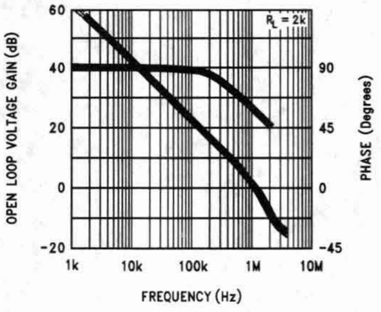
Output Characteristics Sourcing Current



Output Characteristics Sinking Current



Gain and Phase Response vs Temperature (−55°C to +125°C)



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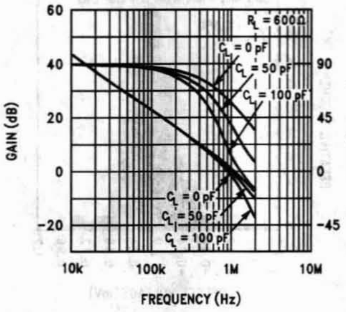
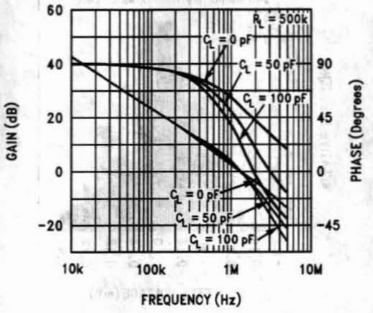
Typical Performance Characteristics (Continued)

$V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

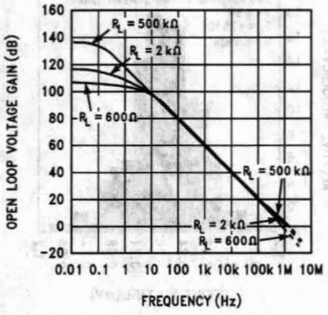
Gain and Phase Response vs Capacitive Load with $R_L = 600\Omega$



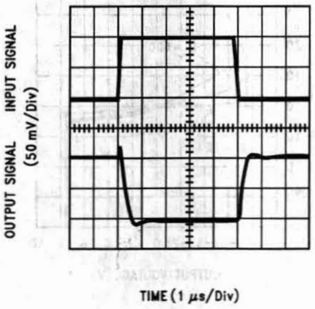
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$



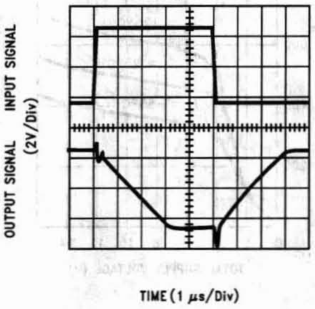
Open Loop Frequency Response



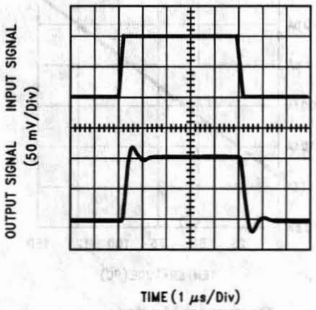
Inverting Small Signal Pulse Response



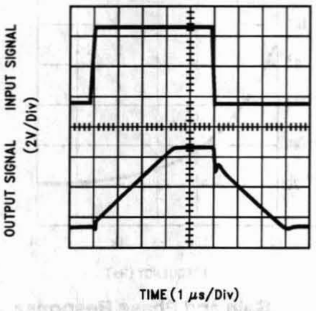
Inverting Large Signal Pulse Response



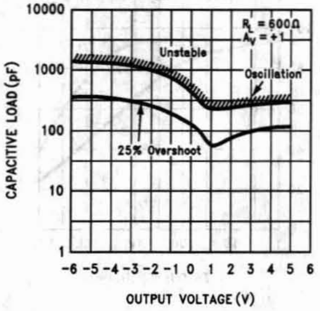
Non-Inverting Small Signal Pulse Response



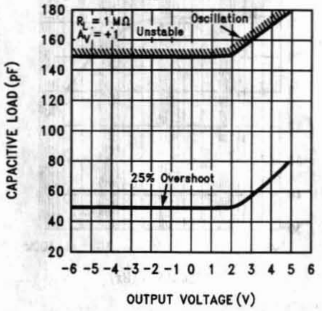
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load, $R_L = 600\Omega$



Stability vs Capacitive Load $R_L = 1\ M\Omega$



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Applications Hints

AMPLIFIER TOPOLOGY

The LMC6081 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6081 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6081.

Although the LMC6081 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6081 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work).*

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1\, C_{IN} \leq R_2\, C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

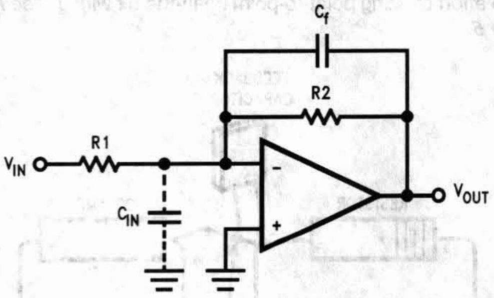

FIGURE 1. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a.*

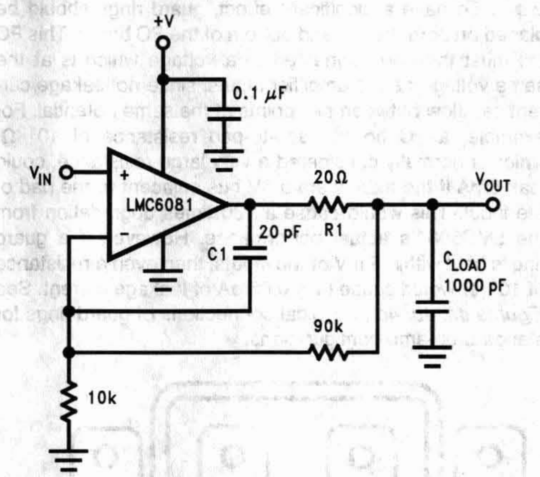

FIGURE 2a. LMC6081 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a,* R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 2b).* Typically a pull up resistor conducting 500 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see electrical characteristics).

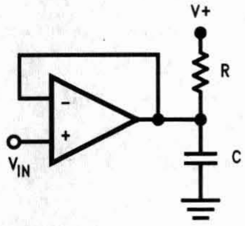

FIGURE 2b: Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6081, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface

Applications Hints (Continued)

leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6081's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6081's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations.

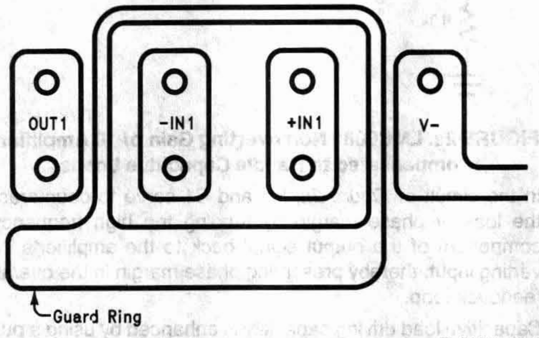

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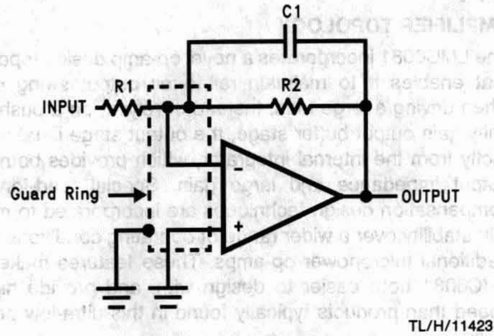
FIGURE 3. Example of Guard Ring in P.C. Board Layout



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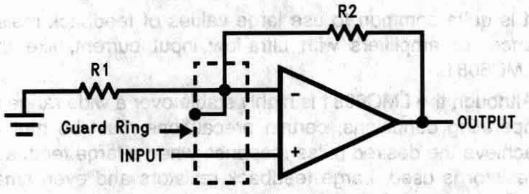
(a) Inverting Amplifier



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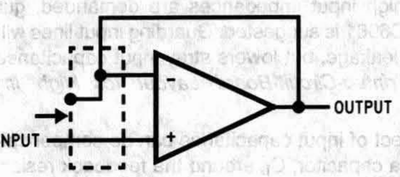
(b) Non-Inverting Amplifier



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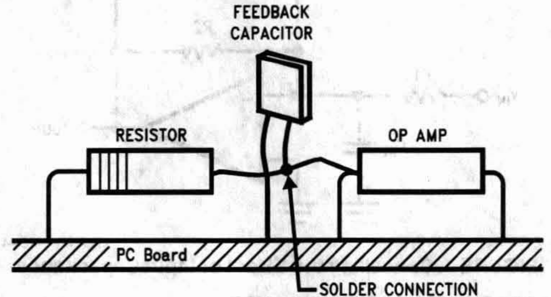
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring

Latchup

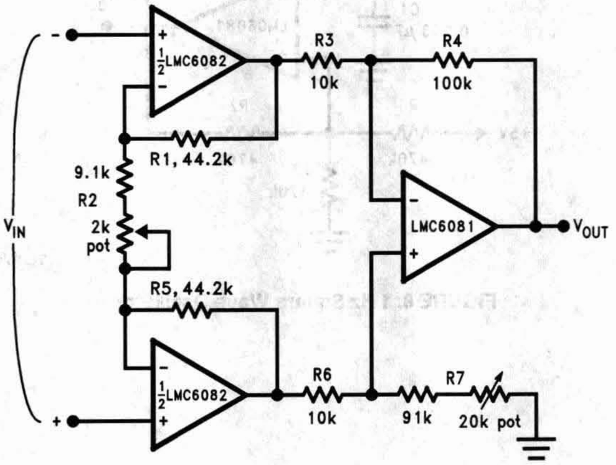
CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6061 and LMC6081 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6081 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



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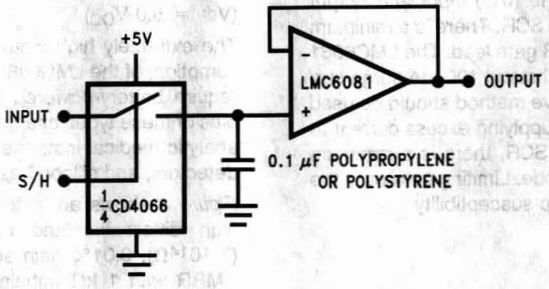
If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)


+5V
INPUT
S/H
1/4 CD4066
-
+
LMC6081
OUTPUT
0.1 μF POLYPROPYLENE
OR POLYSTYRENE

TL/H/11423-12

FIGURE 7. Low-Leakage Sample and Hold

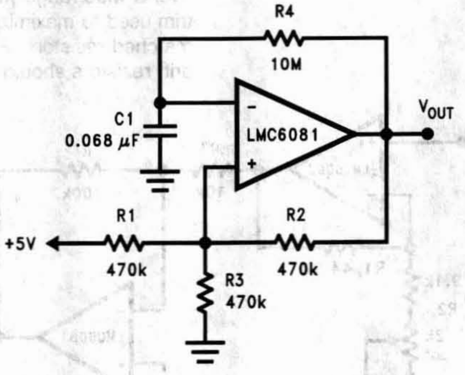

R4
10M
C1
0.068 μF
-
+
LMC6081
V_OUT
R1
+5V
470k
R2
470k
R3
470k

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FIGURE 8. 1 Hz Square Wave Oscillator

National Semiconductor

LMC6082 Precision CMOS Dual Operational Amplifier

General Description

The LMC6082 is a precision dual low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6082 ideally suited for precision circuit applications.

Other applications using the LMC6082 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6062 precision dual micropower operational amplifier.

PATENT PENDING

Features (Typical unless otherwise stated)

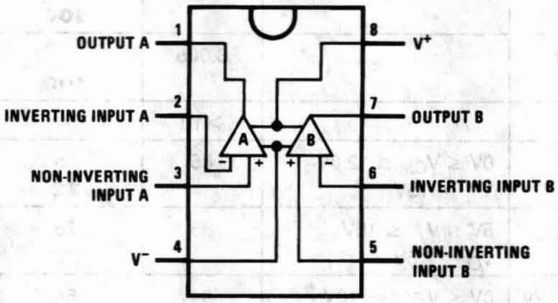
- Low offset voltage 150 μV
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V−
- High voltage gain 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



Top View

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Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
8-Pin Molded DIP	LMC6082AMN	LMC6082AIN LMC6082IN	N08E	Rail
8-Pin Small Outline		LMC6082AIM LMC6082IM	M08A	Rail Tape and Reel

For MIL-STD-883C qualified products, please contact your local National Semiconductor Sales Office or Distributor for availability and specification information.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	(V+) +0.3V, (V−) −0.3V
Supply Voltage (V+ − V−)	16V
Output Short Circuit to V+	(Note 11)
Output Short Circuit to V−	(Note 2)
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6082AM	$-55°C \leq T_J \leq +125°C$
LMC6082AI, LMC6082I	$-40°C \leq T_J \leq +85°C$
Supply Voltage	$4.5V \leq V^+ \leq 15.5V$
Thermal Resistance (θ_{JA}) (Note 12)	
8-Pin Molded DIP	115°C/W
8-Pin SO	193°C/W
Power Dissipation	(Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6082AM Limit (Note 6)	LMC6082AI Limit (Note 6)	LMC6082I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			150	350 **1000**	350 **800**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	**100**	**4**	**4**	pA Max
I_{OS}	Input Offset Current			0.005	**100**	**2**	**2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 12.0V$ $V^+ = 15V$		85	75 **72**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V^+ \leq 15V$ $V_O = 2.5V$		85	75 **72**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \leq V^- \leq -10V$		94	84 **81**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V Min
A_V	Large Signal Voltage Gain	$R_L = 2\ k\Omega$ (Note 7)	Sourcing	1400	400 **300**	400 **300**	300 **200**	V/mV Min
			Sinking	350	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 600\Omega$ (Note 7)	Sourcing	1200	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	150	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6082AM Limit (Note 6)	LMC6082AI Limit (Note 6)	LMC6082I Limit (Note 6)	Units
V_O	Output Swing	$V^+ = 5V$ $R_L = 2\ k\Omega$ to 2.5V	4.87	4.80 **4.70**	4.80 **4.73**	4.75 **4.67**	V Min
			0.10	0.13 **0.19**	0.13 **0.17**	0.20 **0.24**	V Max
		$V^+ = 5V$ $R_L = 600\Omega$ to 2.5V	4.61	4.50 **4.24**	4.50 **4.31**	4.40 **4.21**	V Min
			0.30	0.40 **0.63**	0.40 **0.50**	0.50 **0.63**	V Max
		$V^+ = 15V$ $R_L = 2\ k\Omega$ to 7.5V	14.63	14.50 **14.30**	14.50 **14.34**	14.37 **14.25**	V Min
			0.26	0.35 **0.48**	0.35 **0.45**	0.44 **0.56**	V Max
		$V^+ = 15V$ $R_L = 600\Omega$ to 7.5V	13.90	13.35 **12.80**	13.35 **12.86**	12.92 **12.44**	V Min
			0.79	1.16 **1.42**	1.16 **1.32**	1.33 **1.58**	V Max
I_O	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, $V_O = 5V$	21	16 **11**	16 **13**	13 **10**	mA Min
I_O	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	30	28 **18**	28 **22**	23 **18**	mA Min
		Sinking, $V_O = 13V$ (Note 11)	34	28 **19**	28 **22**	23 **18**	mA Min
I_S	Supply Current	Both Amplifiers $V^+ = +5V$, $V_O = 1.5V$	0.9	1.5 **1.8**	1.5 **1.8**	1.5 **1.8**	mA Max
		Both Amplifiers $V^+ = +15V$, $V_O = 7.5V$	1.1	1.7 **2**	1.7 **2**	1.7 **2**	mA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6082AM Limit (Note 6)	LMC6082AI Limit (Note 6)	LMC6082I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.5	0.8 **0.5**	0.8 **0.6**	0.8 **0.6**	V/μs Min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	(Note 9)	140				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 10 kHz, $A_V = -10$ $R_L = 2\ k\Omega$, $V_O = 8\ V_{PP}$ ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A) / \theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\ V_{PP}$.

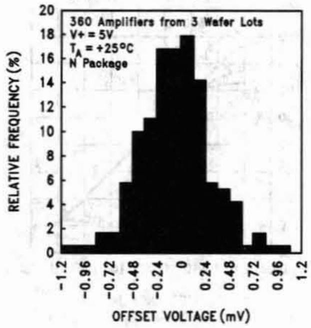
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 11: Do not connect output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

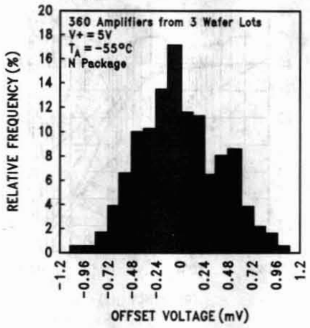
Note 12: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

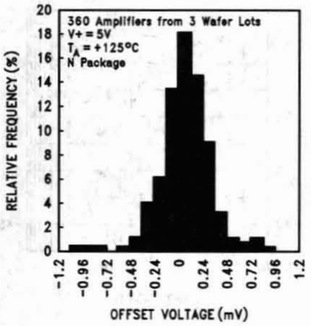
Distribution of LMC6082 Input Offset Voltage ($T_A = +25°C$)



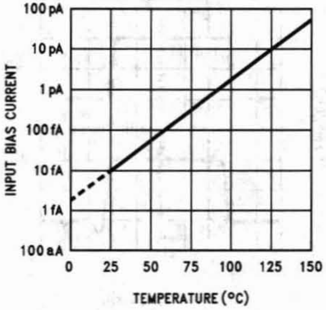
Distribution of LMC6082 Input Offset Voltage ($T_A = -55°C$)



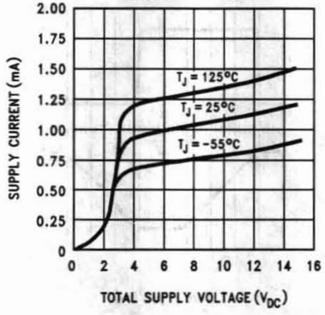
Distribution of LMC6082 Input Offset Voltage ($T_A = +125°C$)



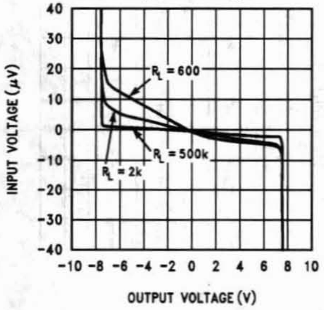
Input Bias Current vs Temperature



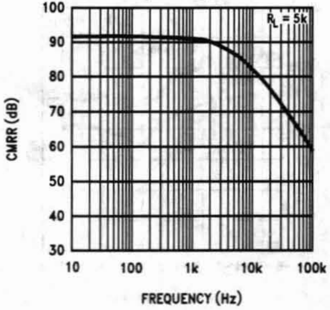
Supply Current vs Supply Voltage



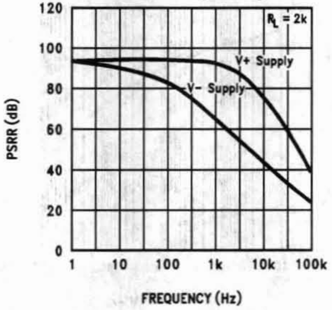
Input Voltage vs Output Voltage



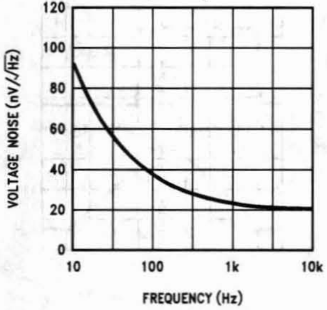
Common Mode Rejection Ratio vs Frequency



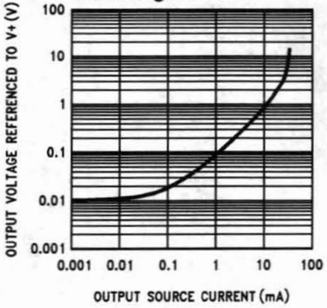
Power Supply Rejection Ratio vs Frequency



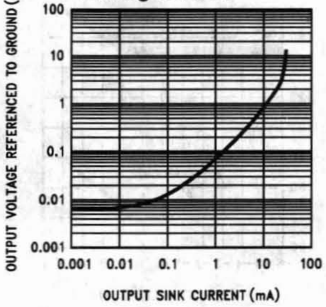
Input Voltage Noise vs Frequency



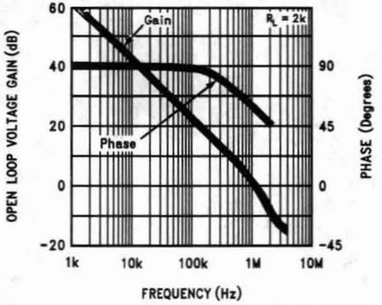
Output Characteristics Sourcing Current



Output Characteristics Sinking Current



Gain and Phase Response vs Temperature (−55°C to +125°C)



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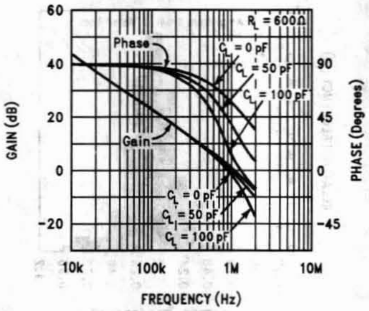
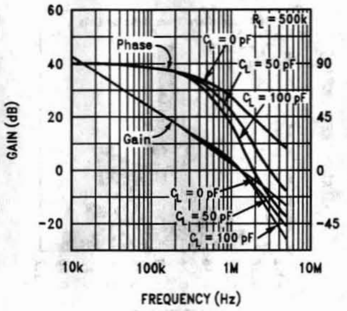
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

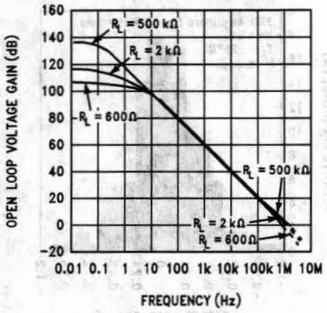
Gain and Phase Response vs Capacitive Load with $R_L = 600\Omega$



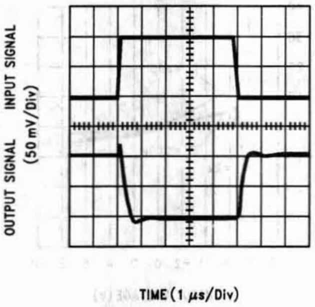
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$



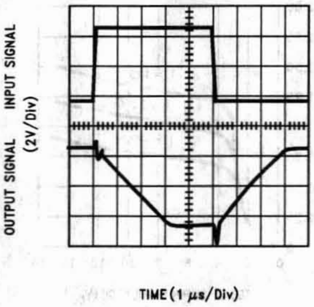
Open Loop Frequency Response



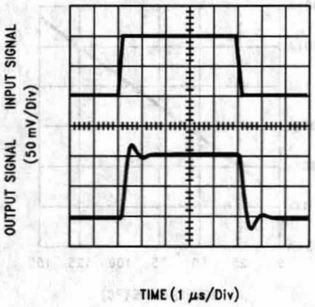
Inverting Small Signal Pulse Response



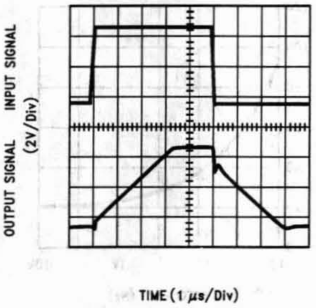
Inverting Large Signal Pulse Response



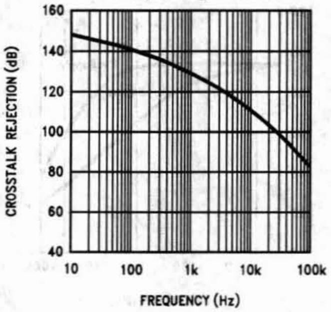
Non-Inverting Small Signal Pulse Response



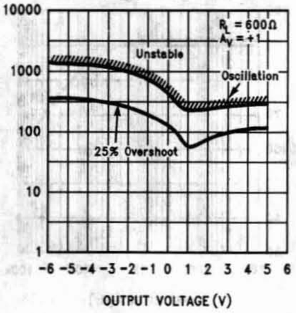
Non-Inverting Large Signal Pulse Response



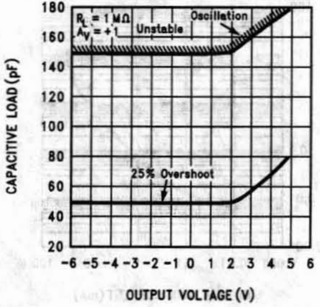
Crosstalk Rejection vs Frequency



Stability vs Capacitive Load, $R_L = 600\Omega$



Stability vs Capacitive Load $R_L = 1\ M\Omega$



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Applications Hints

AMPLIFIER TOPOLOGY

The LMC6082 incorporates a novel op-amp design topology that enables it to maintain rail to rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6082 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6082.

Although the LMC6082 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6082 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work).*

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 \, C_{IN} \leq R_2 \, C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

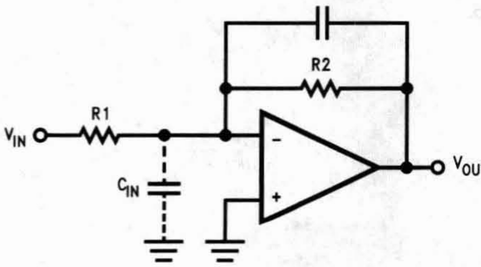


FIGURE 1. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a.*

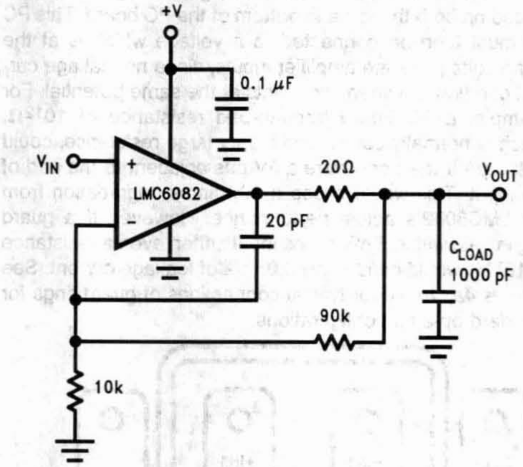


FIGURE 2a. LMC6082 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a,* R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 2b).* Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

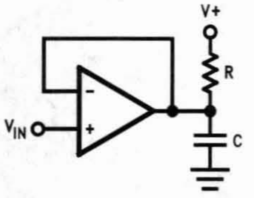


FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

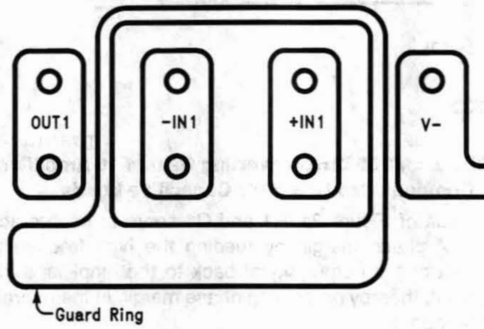
PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6082, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface

Applications Hints

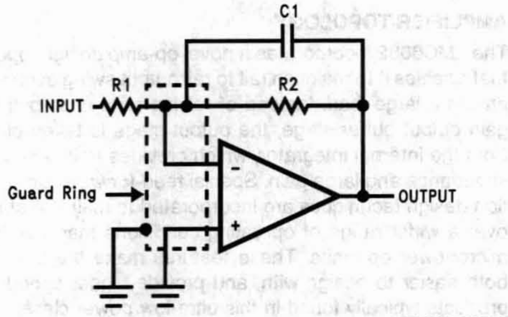
leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6082's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6082's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.



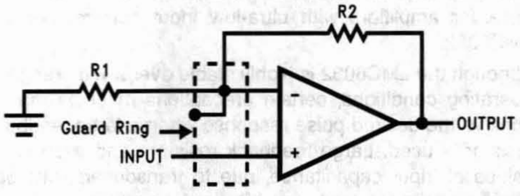
TL/H/11297-6

FIGURE 3. Example of Guard Ring in P.C. Board Layout



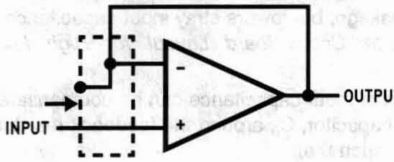
TL/H/11297-7

(a) Inverting Amplifier



TL/H/11297-8

(b) Non-Inverting Amplifier



TL/H/11297-9

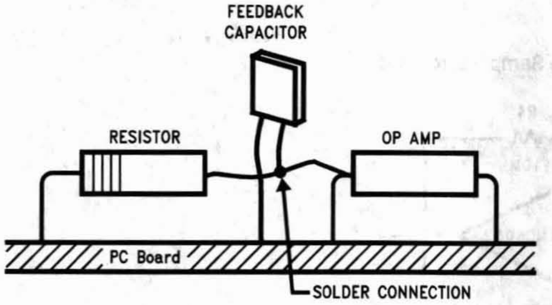
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6062 and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



TL/H/11297-10

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

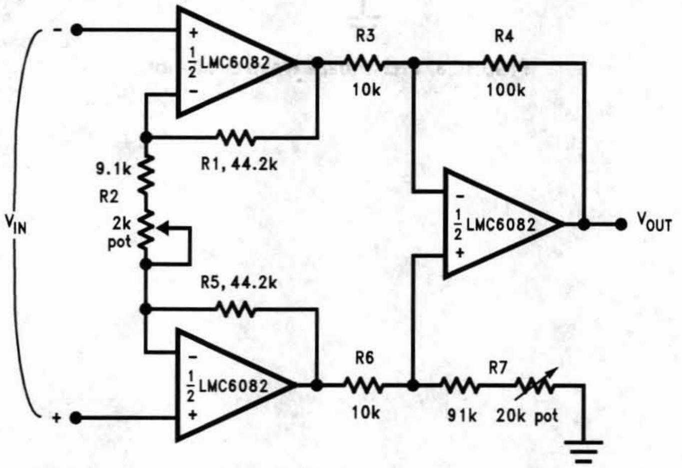
FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6082 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



TL/H/11297-11

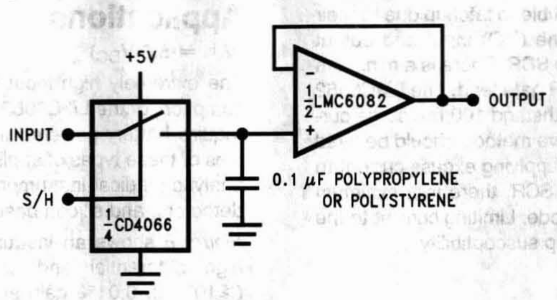
If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

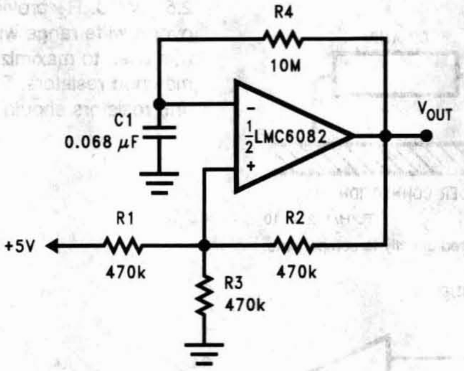
FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications (V+ = 5.0 V_{DC})


+5V
INPUT
S/H
$\frac{1}{4}$CD4066
$\frac{1}{2}$LMC6082
−
+
OUTPUT
0.1 µF POLYPROPYLENE
OR POLYSTYRENE

TL/H/11297-12

FIGURE 7. Low-Leakage Sample and Hold


R4
10M
C1
0.068 µF
$\frac{1}{2}$LMC6082
−
+
V_{OUT}
R1
470k
R2
470k
R3
470k
+5V

TL/H/11297-13

FIGURE 8. 1 Hz Square Wave Oscillator

National Semiconductor

LMC6084
Precision CMOS Quad Operational Amplifier

General Description

The LMC6084 is a precision quad low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6084 ideally suited for precision circuit applications.

Other applications using the LMC6084 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6064 precision quad micropower operational amplifier.

For a single or dual operational amplifier with similar features, see the LMC6081 or LMC6082 respectively.

PATENT PENDING

Features (Typical unless otherwise stated)

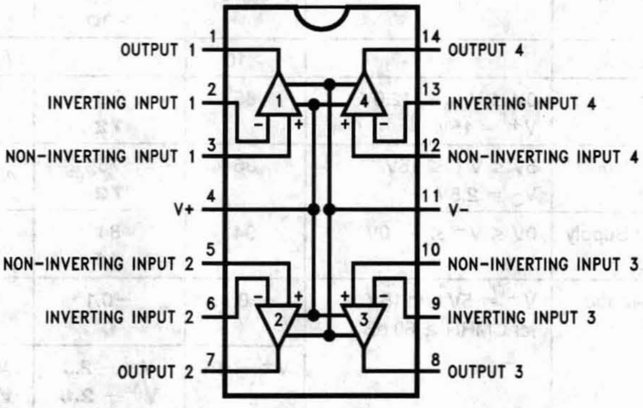
- Low offset voltage 150 μV
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V−
- High voltage gain 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

14-Pin DIP/SO


1
OUTPUT 1
2
INVERTING INPUT 1
3
NON-INVERTING INPUT 1
4
V+
5
NON-INVERTING INPUT 2
6
INVERTING INPUT 2
7
OUTPUT 2
14
OUTPUT 4
13
INVERTING INPUT 4
12
NON-INVERTING INPUT 4
11
V−
10
NON-INVERTING INPUT 3
9
INVERTING INPUT 3
8
OUTPUT 3
1
2
3
4
−
+

TL/H/11467–1

Top View

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
14-Pin Molded DIP	LMC6084AMN	LMC6084AIN LMC6084IN	N14A	Rail
14-Pin Small Outline		LMC6084AIM LMC6084IM	M14A	Rail Tape and Reel

For MIL-STD-883C qualified products, please contact your local National Semiconductor Sales Office or Distributor for availability and specification information.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	(V+) +0.3V, (V−) −0.3V
Supply Voltage (V+ − V−)	16V
Output Short Circuit to V+	(Note 11)
Output Short Circuit to V−	(Note 2)
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6084AM	$-55°C \leq T_J \leq +125°C$
LMC6084AI, LMC6084I	$-40°C \leq T_J \leq +85°C$
Supply Voltage	$4.5V \leq V^+ \leq 15.5V$
Thermal Resistance (θ_{JA}) (Note 12)	
14-Pin Molded DIP	81°C/W
14-Pin SO	126°C/W
Power Dissipation	(Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6084AM Limit (Note 6)	LMC6084AI Limit (Note 6)	LMC6084I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			150	350 **1000**	350 **800**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	**100**	**4**	**4**	pA Max
I_{OS}	Input Offset Current			0.005	**100**	**2**	**2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 12.0V$ $V^+ = 15V$		85	75 **72**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V^+ \leq 15V$ $V_O = 2.5V$		85	75 **72**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \leq V^- \leq -10V$		94	84 **81**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V Min
A_V	Large Signal Voltage Gain	$R_L = 2\ k\Omega$ (Note 7)	Sourcing	1400	400 **300**	400 **300**	300 **200**	V/mV Min
			Sinking	350	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 600\Omega$ (Note 7)	Sourcing	1200	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	150	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6084AM Limit (Note 6)	LMC6084AI Limit (Note 6)	LMC6084I Limit (Note 6)	Units
V_O	Output Swing	$V^+ = 5V$ $R_L = 2\ k\Omega$ to 2.5V	4.87	4.80 **4.70**	4.80 **4.73**	4.75 **4.67**	V Min
			0.10	0.13 **0.19**	0.13 **0.17**	0.20 **0.24**	V Max
		$V^+ = 5V$ $R_L = 600\Omega$ to 2.5V	4.61	4.50 **4.24**	4.50 **4.31**	4.40 **4.21**	V Min
			0.30	0.40 **0.63**	0.40 **0.50**	0.50 **0.63**	V Max
		$V^+ = 15V$ $R_L = 2\ k\Omega$ to 7.5V	14.63	14.50 **14.30**	14.50 **14.34**	14.37 **14.25**	V Min
			0.26	0.35 **0.48**	0.35 **0.45**	0.44 **0.56**	V Max
		$V^+ = 15V$ $R_L = 600\Omega$ to 7.5V	13.90	13.35 **12.80**	13.35 **12.86**	12.92 **12.44**	V Min
			0.79	1.16 **1.42**	1.16 **1.32**	1.33 **1.58**	V Max
I_O	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, $V_O = 5V$	21	16 **11**	16 **13**	13 **10**	mA Min
I_O	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	30	28 **18**	28 **22**	23 **18**	mA Min
		Sinking, $V_O = 13V$ (Note 11)	34	28 **19**	28 **22**	23 **18**	mA Min
I_S	Supply Current	All Four Amplifiers $V^+ = +5V$, $V_O = 1.5V$	1.8	3.0 **3.6**	3.0 **3.6**	3.0 **3.6**	mA Max
		All Four Amplifiers $V^+ = +15V$, $V_O = 7.5V$	2.2	3.4 **4.0**	3.4 **4.0**	3.4 **4.0**	mA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6084AM Limit (Note 6)	LMC6084AI Limit (Note 6)	LMC6084I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.5	0.8 **0.5**	0.8 **0.6**	0.8 **0.6**	V/μs Min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	(Note 9)	140				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	$F = 10\ kHz, A_V = -10$ $R_L = 2\ k\Omega, V_O = 8\ V_{PP}$ ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A) / \theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\ V_{PP}$.

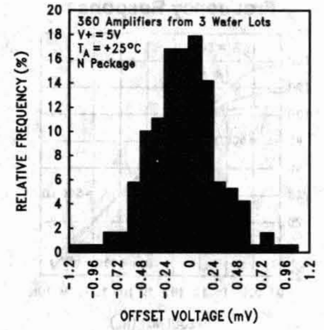
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 11: Do not connect output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

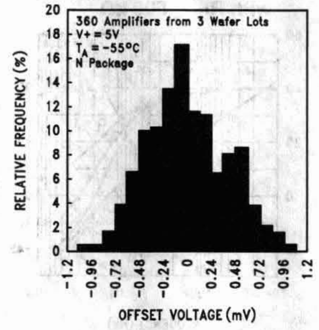
Note 12: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

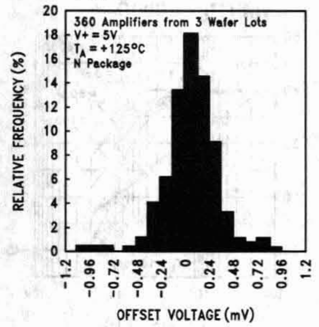
Distribution of LMC6084 Input Offset Voltage ($T_A = +25°C$)



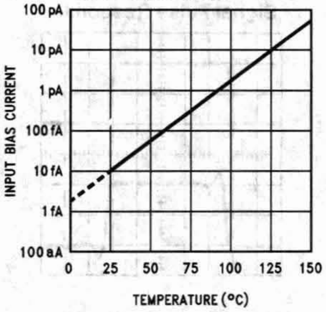
Distribution of LMC6084 Input Offset Voltage ($T_A = -55°C$)



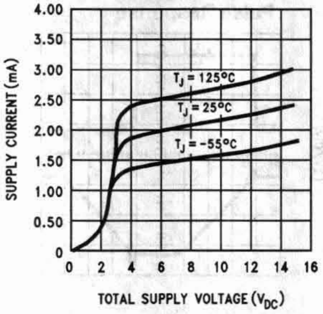
Distribution of LMC6084 Input Offset Voltage ($T_A = +125°C$)



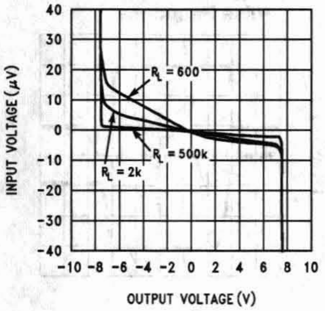
Input Bias Current vs Temperature



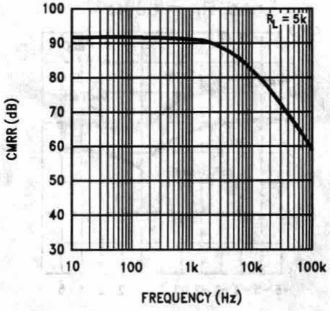
Supply Current vs Supply Voltage



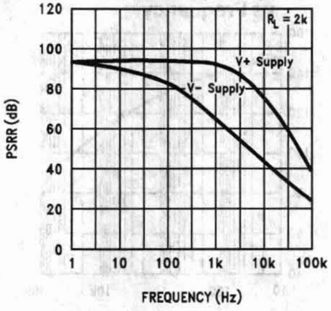
Input Voltage vs Output Voltage



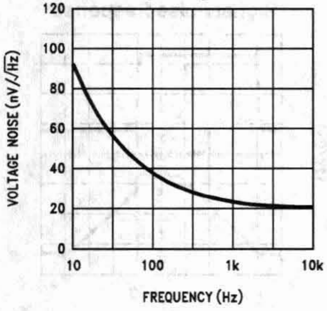
Common Mode Rejection Ratio vs Frequency



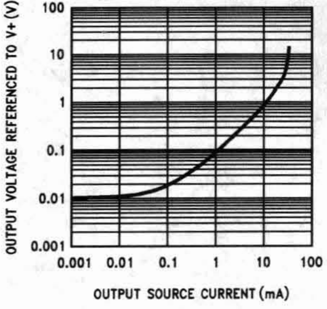
Power Supply Rejection Ratio vs Frequency



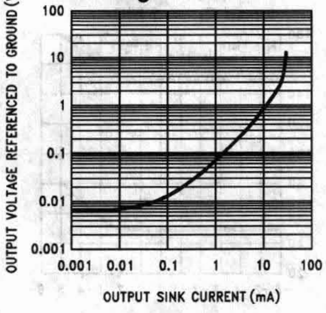
Input Voltage Noise vs Frequency



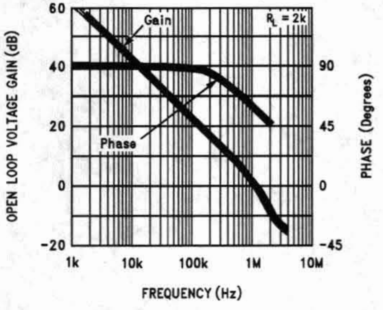
Output Characteristics Sourcing Current



Output Characteristics Sinking Current



Gain and Phase Response vs Temperature (−55°C to +125°C)

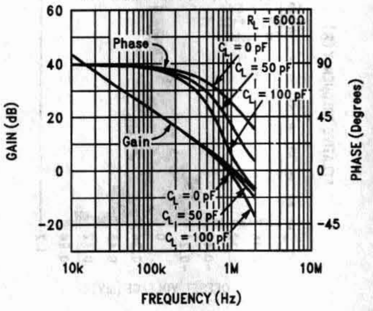


TL/H/11467–2

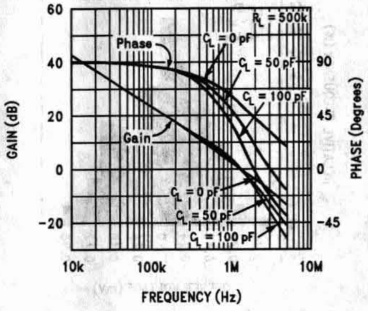
Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified (Continued)

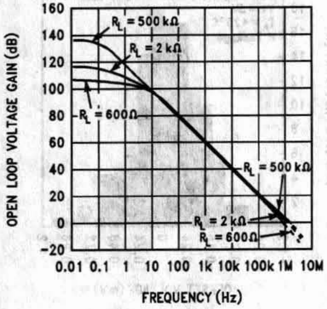
Gain and Phase Response vs Capacitive Load with $R_L = 600\Omega$



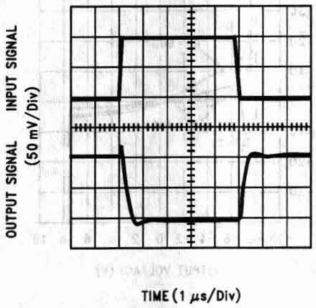
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$



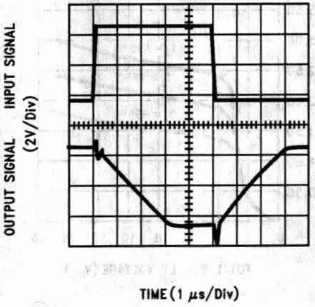
Open Loop Frequency Response



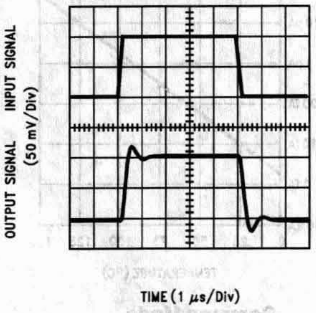
Inverting Small Signal Pulse Response



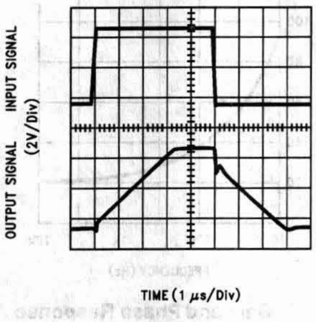
Inverting Large Signal Pulse Response



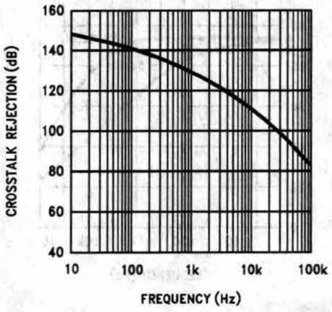
Non-Inverting Small Signal Pulse Response



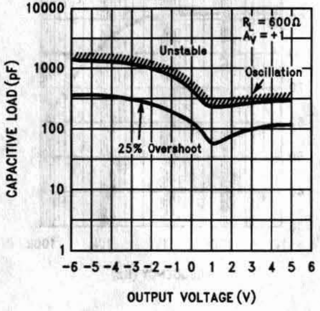
Non-Inverting Large Signal Pulse Response



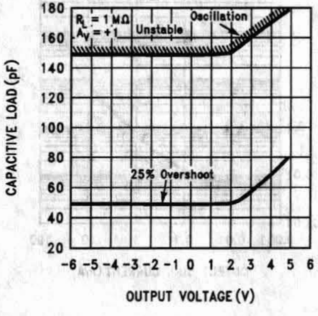
Crosstalk Rejection vs Frequency



Stability vs Capacitive Load, $R_L = 600\Omega$



Stability vs Capacitive Load $R_L = 1\ M\Omega$



TL/H/11467-3

Applications Hints

AMPLIFIER TOPOLOGY

The LMC6084 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6084 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6084.

Although the LMC6084 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6084 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work).*

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1\,C_{IN} \leq R_2\,C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

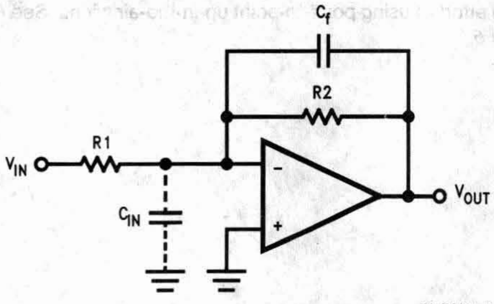


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FIGURE 1. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a.*

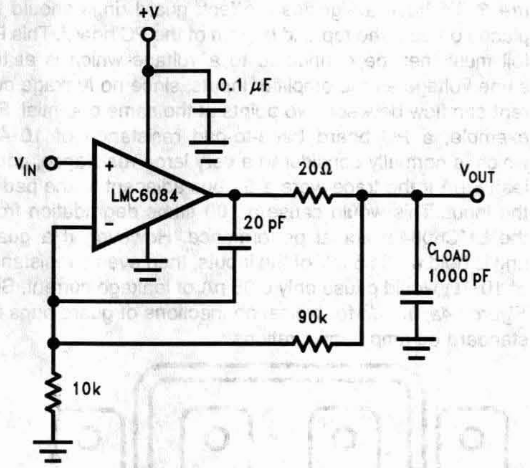

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FIGURE 2a. LMC6084 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 2b).* Typically a pull up resistor conducting 500 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

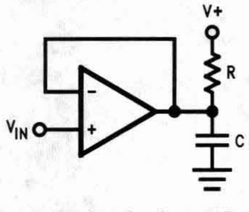

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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6084, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface

Applications Hints (Continued)

leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6084's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6084's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations.

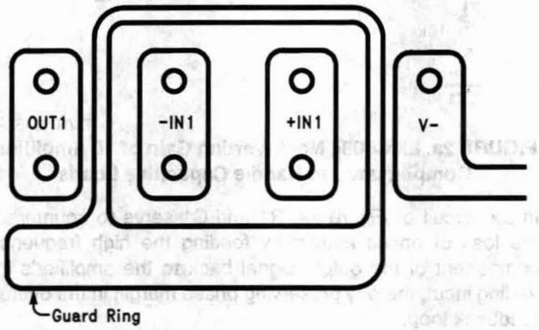

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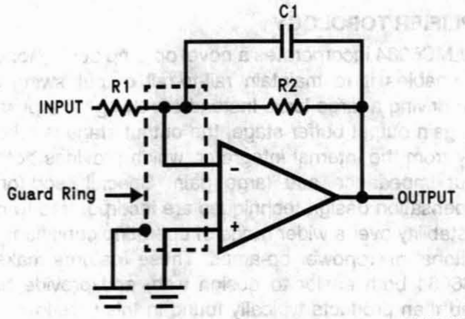
FIGURE 3. Example of Guard Ring in P.C. Board Layout



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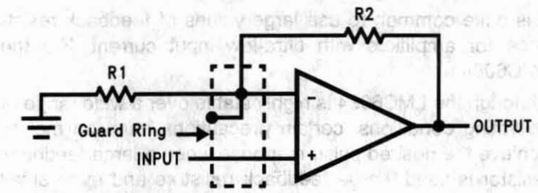
(a) Inverting Amplifier



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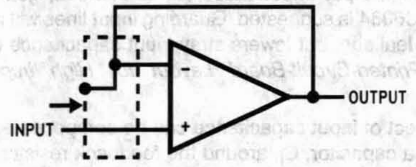
(b) Non-Inverting Amplifier



TL/H/11467-10

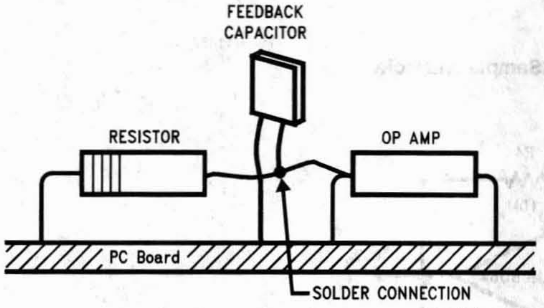
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6084 is designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

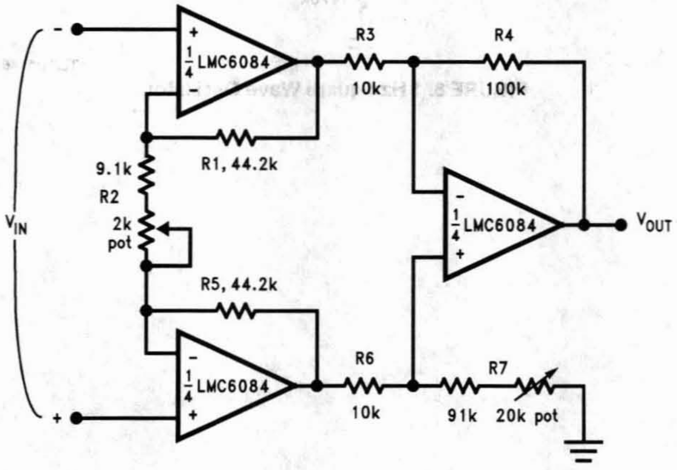
FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6084 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



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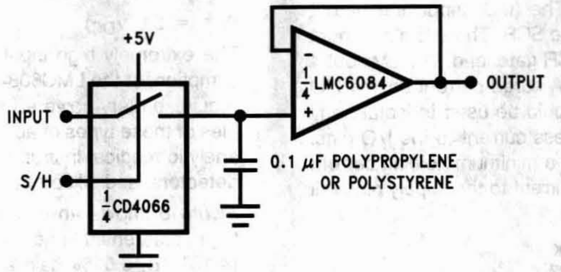
If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)



+5V
INPUT
S/H
$\frac{1}{4}$CD4066
$\frac{1}{4}$LMC6084
OUTPUT
0.1 μF POLYPROPYLENE
OR POLYSTYRENE

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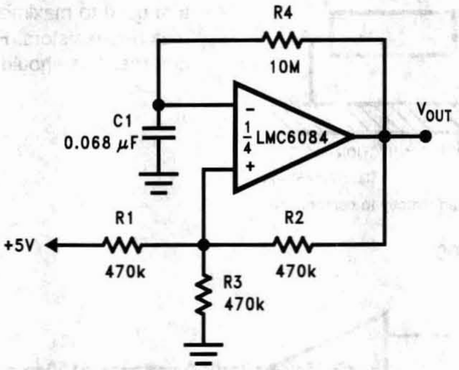
FIGURE 7. Low-Leakage Sample and Hold



R4
10M
C1
0.068 μF
$\frac{1}{4}$LMC6084
V_{OUT}
R1
470k
+5V
R2
470k
R3
470k

TL/H/11467–14

FIGURE 8. 1 Hz Square Wave Oscillator

National Semiconductor

LMC6462 Dual/LMC6464 Quad Micropower, Rail-to-Rail Input and Output CMOS Operational Amplifier

General Description

The LMC6462/4 is a micropower version of the popular LMC6482/4, combining Rail-to-Rail Input and Output Range with very low power consumption.

The LMC6462/4 provides an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifier, guaranteed for loads down to 25 kΩ, assures maximum dynamic sigal range. This rail-to-rail performance of the amplifier, combined with its high voltage gain makes it unique among rail-to-rail amplifiers. The LMC6462/4 is an excellent upgrade for circuits using limited common-mode range amplifiers.

The LMC6462/4, with guaranteed specifications at 3V and 5V, is especially well-suited for low voltage applications. A quiescent power consumption of 60 μW per amplifier (at $V_S = 3V$) can extend the useful life of battery operated systems. The amplifier's 150 fA input current, low offset voltage of 0.25 mV, and 85 dB CMRR maintain accuracy in battery-powered systems.

Features (Typical unless otherwise noted)

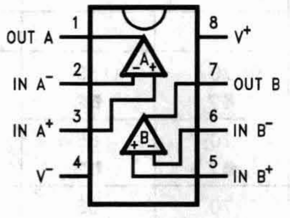
- Ultra Low Supply Current 20 μA/Amplifier
- Guaranteed Characteristics at 3V and 5V
- Rail-to-Rail Input Common-Mode Voltage Range
- Rail-to-Rail Output Swing (within 10 mV of rail, $V_S = 5V$ and $R_L = 25\ k\Omega$)
- Low Input Current 150 fA
- Low Input Offset Voltage 0.25 mV

Applications

- Battery Operated Circuits
- Transducer Interface Circuits
- Portable Communication Devices
- Medical Applications
- Battery Monitoring

Connection Diagrams

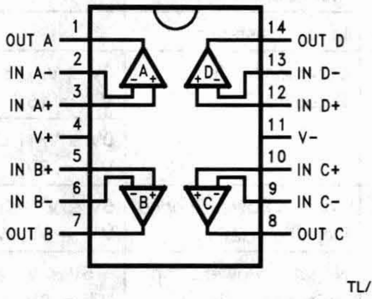
8-Pin DIP/SO



Top View

TL/H/12051-1

14-Pin DIP/SO



Top View

TL/H/12051-2

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
8-Pin Molded DIP	LMC6462AMN	LMC6462AIN, LMC6462BIN	N08E	Rails
8-Pin SO-8		LMC6462AIM, LMC6462BIM LMC6462AIMX, LMC6462BIMX	M08A M08A	Rails Tape and Reel
14-Pin Molded DIP	LMC6464AMN	LMC6464AIN, LMC6464BIN	N14A	Rails
14-Pin SO-14		LMC6464AIM, LMC6464BIM LMC6464AIMX, LMC6464BIMX	M14A M14A	Rails Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2.0 kV
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage $(V^+ - V^-)$	16V
Current at Input Pin (Note 12)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$3.0V \le V^+ \le 15.5V$
Junction Temperature Range	
LMC6462AM, LMC6464AM	$-55°C \le T_J \le +125°C$
LMC6462AI, LMC6464AI	$-40°C \le T_J \le +85°C$
LMC6462BI, LMC6464BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
N Package, 14-Pin Molded DIP	81°C/W
M Package, 14-Pin Surface Mount	126°C/W

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6462AI LMC6464AI Limit (Note 6)	LMC6462BI LMC6464BI Limit (Note 6)	LMC6462AM LMC6464AM Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.25	0.5 **1.2**	3.0 **3.7**	0.5 **1.5**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.5				μV/°C
I_B	Input Current	(Note 13)	0.15	**10**	**10**	**200**	pA max
I_{OS}	Input Offset Current	(Note 13)	0.075	**5**	**5**	**100**	pA max
C_{IN}	Common-Mode Input Capacitance		3				pF
R_{IN}	Input Resistance		>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 15.0V$, $V^+ = 15V$	85	70 **67**	65 **62**	70 **65**	dB min
		$0V \le V_{CM} \le 5.0V$ $V^+ = 5V$	85	70 **67**	65 **62**	70 **65**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V^- = 0V, V_O = 2.5V$	85	70 **67**	65 **62**	70 **65**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-5V \le V^- \le -15V$, $V^+ = 0V, V_O = -2.5V$	85	70 **67**	65 **62**	70 **65**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ For CMRR ≥ 50 dB	−0.2	−0.10 **0.00**	−0.10 **0.00**	−0.10 **0.00**	V max
			5.30	5.25 **5.00**	5.25 **5.00**	5.25 **5.00**	V min
		$V^+ = 15V$ For CMRR ≥ 50 dB	−0.2	−0.15 **0.00**	−0.15 **0.00**	−0.15 **0.00**	V max
			15.30	15.25 **15.00**	15.25 **15.00**	15.25 **15.00**	V min

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6462AI LMC6464AI Limit (Note 6)	LMC6462BI LMC6464BI Limit (Note 6)	LMC6462AM LMC6464AM Limit (Note 6)	Units
A_V	Large Signal Voltage Gain	R_L = 100 kΩ (Note 7)	Sourcing	3000				V/mV min
			Sinking	400				V/mV min
		R_L = 25 kΩ (Note 7)	Sourcing	2500				V/mV min
			Sinking	200				V/mV min
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ to $V^+/2$		4.995	4.990 **4.980**	4.950 **4.925**	4.990 **4.970**	V min
				0.005	0.010 **0.020**	0.050 **0.075**	0.010 **0.030**	V max
		V^+ = 5V R_L = 25 kΩ to $V^+/2$		4.990	4.975 **4.965**	4.950 **4.850**	4.975 **4.955**	V min
				0.010	0.020 **0.035**	0.050 **0.150**	0.020 **0.045**	V max
		V^+ = 15V R_L = 100 kΩ to $V^+/2$		14.990	14.975 **14.965**	14.950 **14.925**	14.975 **14.955**	V min
				0.010	0.025 **0.035**	0.050 **0.075**	0.025 **0.050**	V max
		V^+ = 15V R_L = 25 kΩ to $V^+/2$		14.965	14.900 **14.850**	14.850 **14.800**	14.900 **14.800**	V min
				0.025	0.050 **0.150**	0.100 **0.200**	0.050 **0.200**	V max
I_{SC}	Output Short Circuit Current V^+ = 5V	Sourcing, V_O = 0V		27	19 **15**	19 **15**	19 **15**	mA min
		Sinking, V_O = 5V		27	22 **17**	22 **17**	22 **17**	mA min
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V		38	24 **17**	24 **17**	24 **17**	mA min
		Sinking, V_O = 12V (Note 8)		75	55 **45**	55 **45**	55 **45**	mA min
I_S	Supply Current	Dual, LMC6462 V^+ = +5V, V_O = $V^+/2$		40	55 **70**	55 **70**	55 **75**	μA max
		Quad, LMC6464 V^+ = +5V, V_O = $V^+/2$		80	110 **140**	110 **140**	110 **150**	μA max
		Dual, LMC6462 V^+ = +15V, V_O = $V^+/2$		50	60 **70**	60 **70**	60 **75**	μA max
		Quad, LMC6464 V^+ = +15V, V_O = $V^+/2$		90	120 **140**	120 **140**	120 **150**	μA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6462AI LMC6464AI Limit (Note 6)	LMC6462BI LMC6464BI Limit (Note 6)	LMC6462AM LMC6464AM Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	28	15 **8**	15 **8**	15 **8**	V/ms min
GBW	Gain-Bandwidth Product	$V^+ = 15V$	50				kHz
ϕ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	(Note 10)	130				dB
e_n	Input-Referred Voltage Noise	f = 1 kHz $V_{CM} = 1V$	80				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.03				$pA/\sqrt{Hz}$

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6462AI LMC6464AI Limit (Note 6)	LMC6462BI LMC6464BI Limit (Note 6)	LMC6462AM LMC6464AM Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.9	2.0 **2.7**	3.0 **3.7**	2.0 **3.0**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				μV/°C
I_B	Input Current	(Note 13)	0.15	**10**	**10**	**200**	pA
I_{OS}	Input Offset Current	(Note 13)	0.075	**5**	**5**	**100**	pA
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 3V$	74	60	60	60	dB min
PSRR	Power Supply Rejection Ratio	$3V \le V^+ \le 15V$, $V^- = 0V$	80	60	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	−0.10	0.0	0.0	0.0	V max
			3.0	3.0	3.0	3.0	V min
V_O	Output Swing	$R_L = 25\ k\Omega$ to $V^+/2$	2.95	2.9	2.9	2.9	V min
			0.15	0.1	0.1	0.1	V max
I_S	Supply Current	Dual, LMC6462 $V_O = V^+/2$	40	55 **70**	55 **70**	55 **70**	μA
		Quad, LMC6464 $V_O = V^+/2$	80	110 **140**	110 **140**	110 **140**	μA max

3V AC Electrical Characteristics

Unless otherwise specified, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6462AI LMC6464AI Limit (Note 6)	LMC6462BI LMC6464BI Limit (Note 6)	LMC6462AM LMC6464AM Limit (Note 6)	Units
SR	Slew Rate	(Note 11)	23				V/ms
GBW	Gain-Bandwidth Product		50				kHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.

Note 3: Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $3.5V \le V_O \le 7.5V$.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\ V_{PP}$.

Note 11: Connected as Voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

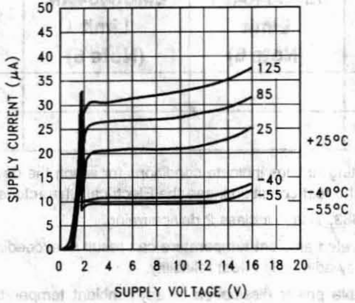
Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature Range parameters see RETSMC6462/4X.

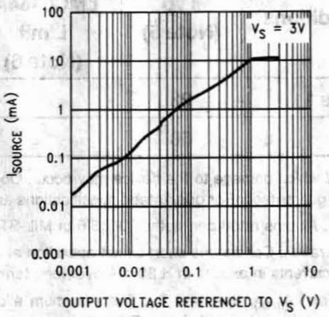
Typical Performance Characteristics

$V_S = +5V$, Single Supply, $T_A = 25°C$ unless otherwise specified

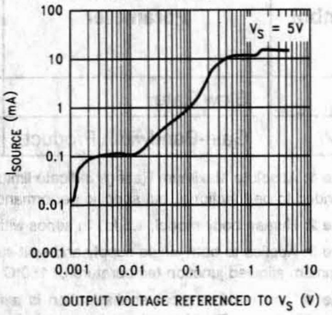
Supply Current vs Supply Voltage



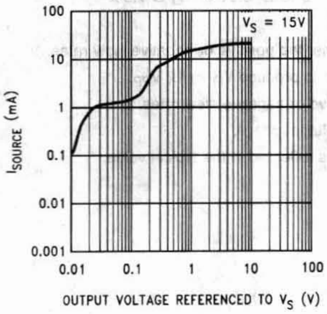
Sourcing Current vs Output Voltage



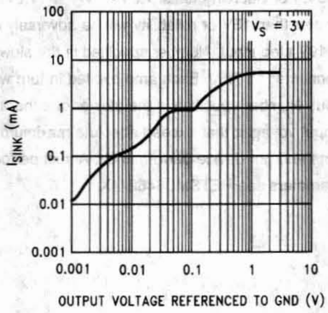
Sourcing Current vs Output Voltage



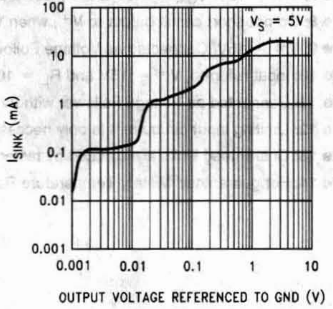
Sourcing Current vs Output Voltage



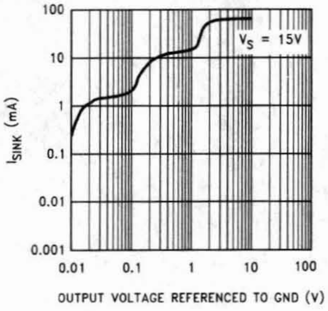
Sinking Current vs Output Voltage



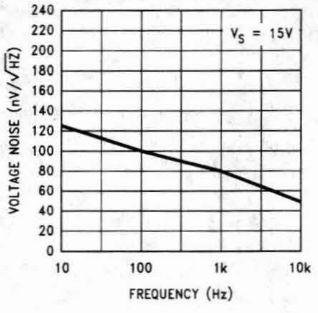
Sinking Current vs Output Voltage



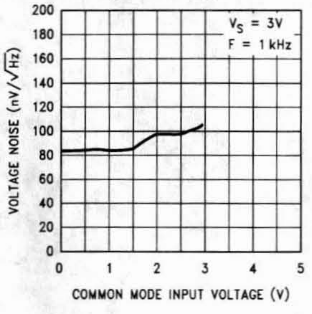
Sinking Current vs Output Voltage



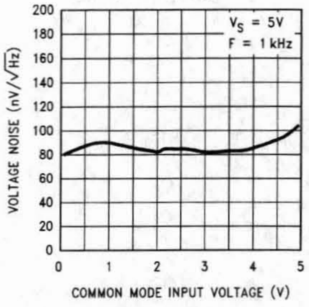
Input Voltage Noise vs Frequency



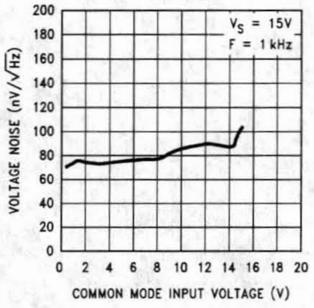
Input Voltage Noise vs Input Voltage



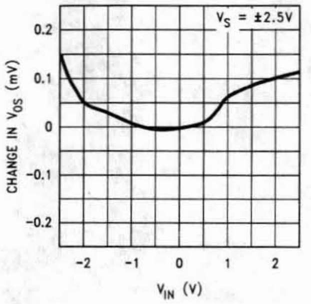
Input Voltage Noise vs Input Voltage



Input Voltage Noise vs Input Voltage



ΔV_{OS} vs CMR

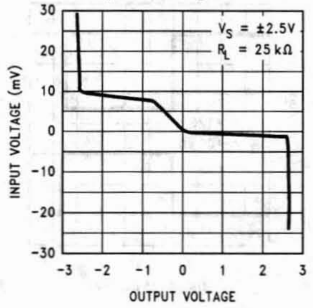


TL/H/12051-3

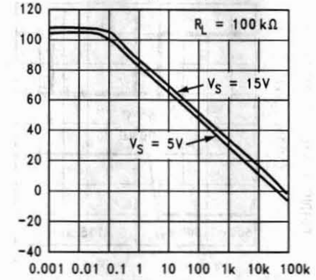
Typical Performance Characteristics (Continued)

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

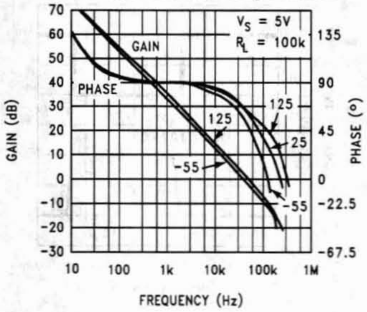
Input Voltage vs Output Voltage



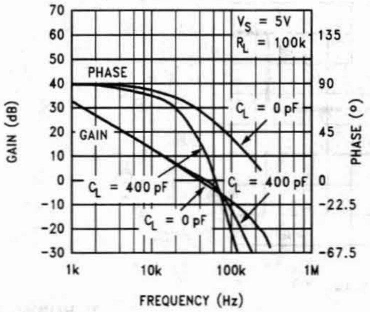
Open Loop Frequency Response



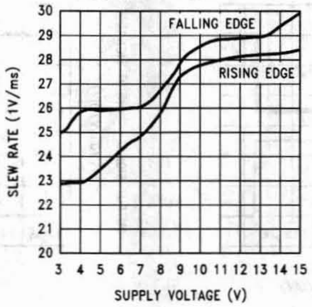
Open Loop Frequency Response vs Temperature



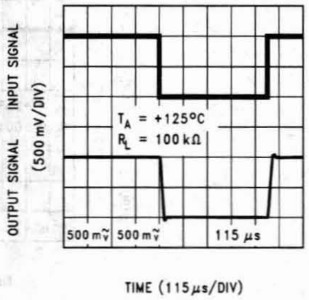
Gain and Phase vs Capacitive Load



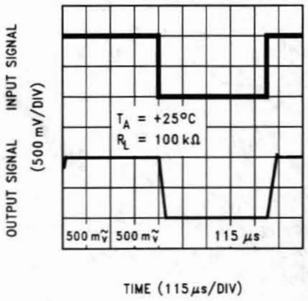
Slew Rate vs Supply Voltage



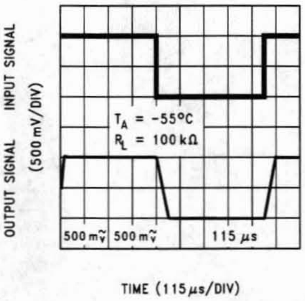
Non-Inverting Large Signal Pulse Response



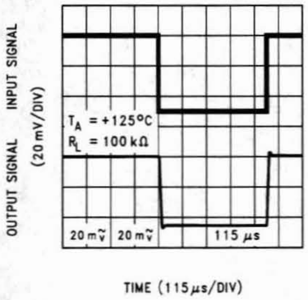
Non-Inverting Large Signal Pulse Response



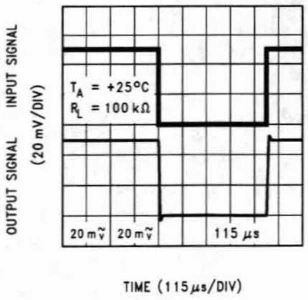
Non-Inverting Large Signal Pulse Response



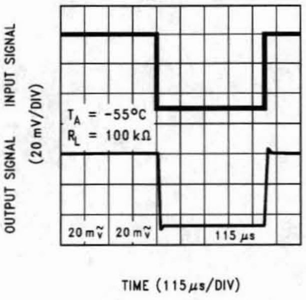
Non-Inverting Small Signal Pulse Response



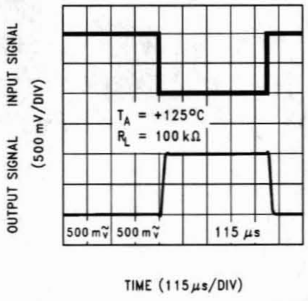
Non-Inverting Small Signal Pulse Response



Non-Inverting Small Signal Pulse Response



Inverting Large Signal Pulse Response

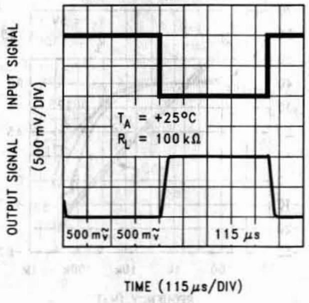


TL/H/12051–4

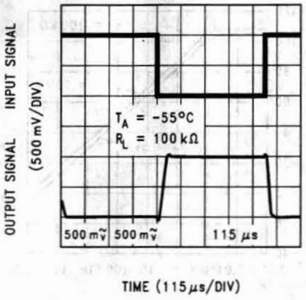
Typical Performance Characteristics (Continued)

$V_S = +5V$, Single Supply, $T_A = 25°C$ unless otherwise specified

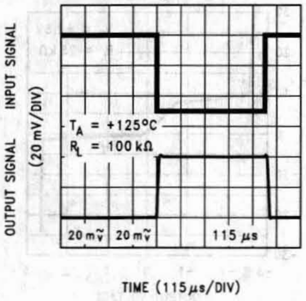
Inverting Large Signal Pulse Response



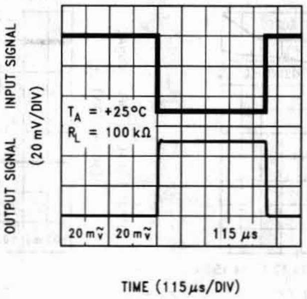
Inverting Large Signal Pulse Response



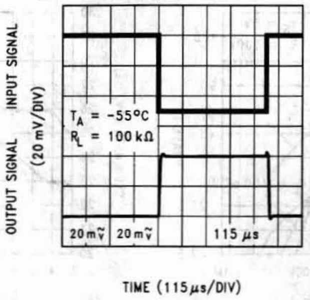
Inverting Small Signal Pulse Response



Inverting Small Signal Pulse Response



Inverting Small Signal Pulse Response



TL/H/12051–29

Application Information

1.0 Input Common-Mode Voltage Range

The LMC6462/4 has a rail-to-rail input common-mode voltage range. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

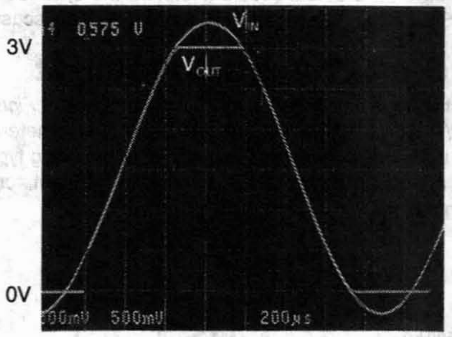


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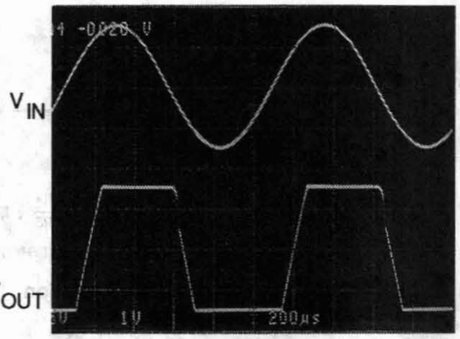
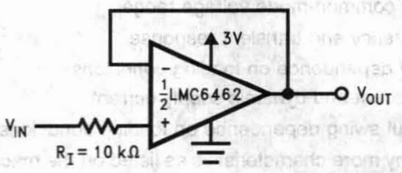
FIGURE 1. An Input Voltage Signal Exceeds the LMC6462/4 Power Supply Voltage with No Output Phase Inversion

The absolute maximum input voltage at $V^+ = 3V$ is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins, possibly affecting reliability. The input current can be externally limited to ±5 mA, with an input resistor, as shown in *Figure 3*.



TL/H/12051-6

FIGURE 2. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in *Figure 3* Causing No Phase Inversion Due to R_I



TL/H/12051-7

FIGURE 3. Input Current Protection for Voltages Exceeding the Supply Voltage

2.0 Rail-to-Rail Output

The approximated output resistance of the LMC6462/4 is 180Ω sourcing, and 130Ω sinking at $V_S = 3V$, and 110Ω sourcing and 83Ω sinking at $V_S = 5V$. The maximum output swing can be estimated as a function of load using the calculated output resistance.

3.0 Capacitive Load Tolerance

The LMC6462/4 can typically drive a 200 pF load with $V_S = 5V$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. If there is a resistive component of the load in parallel to the capacitive component, the isolation resistor and the resistive load create a voltage divider at the output. This introduces a DC error at the output.

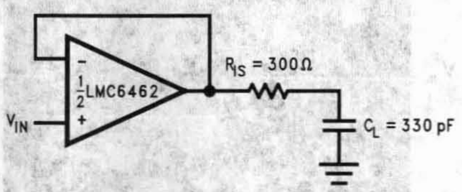


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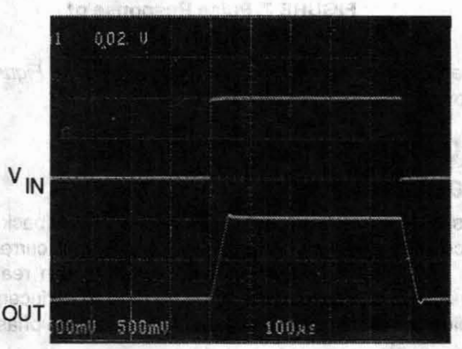
FIGURE 4. Resistive Isolation of a 300 pF Capacitive Load



TL/H/12051-9

FIGURE 5. Pulse Response of the LMC6462 Circuit Shown in *Figure 4*

Figure 5 displays the pulse response of the LMC6462/4 circuit in *Figure 4*.

Another circuit, shown in *Figure 6*, is also used to indirectly drive capacitive loads. This circuit is an improvement to the circuit shown in *Figure 4* because it provides DC accuracy as well as AC stability. R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 should be experimentally determined by the system designer for the desired pulse response. Increased capacitive drive is possible by increasing the value of the capacitor in the feedback loop.

Application Information (Continued)

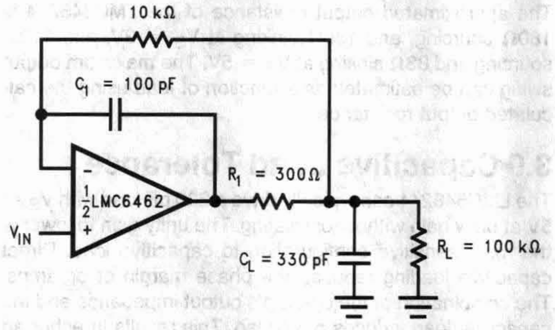

10 kΩ
C_1 = 100 pF
R_1 = 300Ω
-
$\frac{1}{2}$LMC6462
+
V_{IN}
C_L = 330 pF
R_L = 100 kΩ

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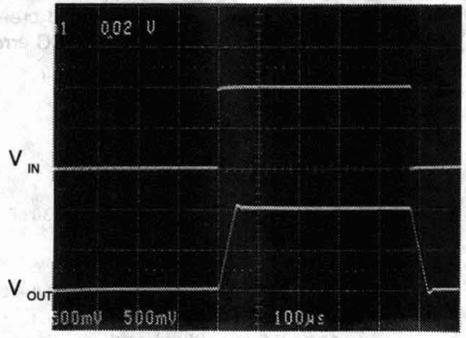
FIGURE 6. LMC6462 Non-Inverting Amplifier, Compensated to Handle a 300 pF Capacitive and 100 kΩ Resistive Load



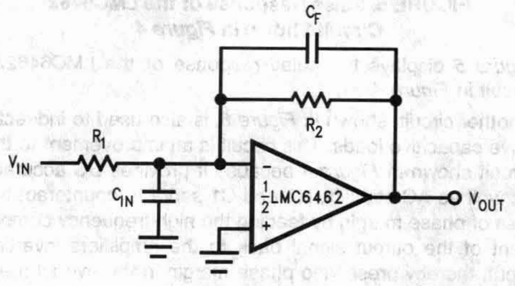
TL/H/12051-11

FIGURE 7. Pulse Response of LMC6462 Circuit in *Figure 6*

The pulse response of the circuit shown in *Figure 6* is shown in *Figure 7*.

4.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6462/4. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.


C_F
R_2
R_1
V_{IN}
C_{IN}
-
$\frac{1}{2}$LMC6462
+
V_{OUT}

TL/H/12051-12

FIGURE 8. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 8*), C_F, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \ge \frac{1}{2\pi R_2 C_F}$$

or

$$R_1 C_{IN} \le R_2 C_F$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

5.0 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in *Figures 9* and *10*. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with $V_S = \pm 5V$.

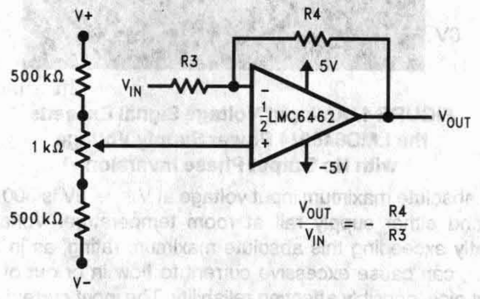

V+
R4
R3
5V
500 kΩ
V_{IN}
-
$\frac{1}{2}$LMC6462
+
V_{OUT}
1 kΩ
-5V
500 kΩ
$\frac{V_{OUT}}{V_{IN}} = -\frac{R4}{R3}$
V-

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FIGURE 9. Inverting Configuration Offset Voltage Adjustment

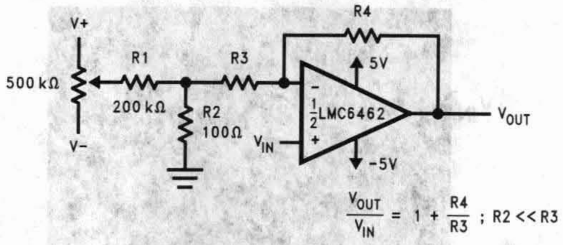
V+
R4
R1
R3
5V
500 kΩ
200 kΩ
R2
100Ω
V_{IN}
V-
-
$\frac{1}{2}$LMC6462
+
V_{OUT}
-5V
$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R4}{R3}$; R2 << R3

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FIGURE 10. Non-Inverting Configuration Offset Voltage Adjustment

6.0 Spice Macromodel

A Spice macromodel is available for the LMC6462/4. This model includes a simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact the National Semiconductor Customer Response Center to obtain an operational amplifier Spice model library disk.

Application Information (Continued)

7.0 Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6462/4, typically 150 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6462's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 11*. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 30 times degradation from the LMC6462/4's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 12a*, *12b* and *12c* for typical connections of guard rings for standard op-amp configurations.

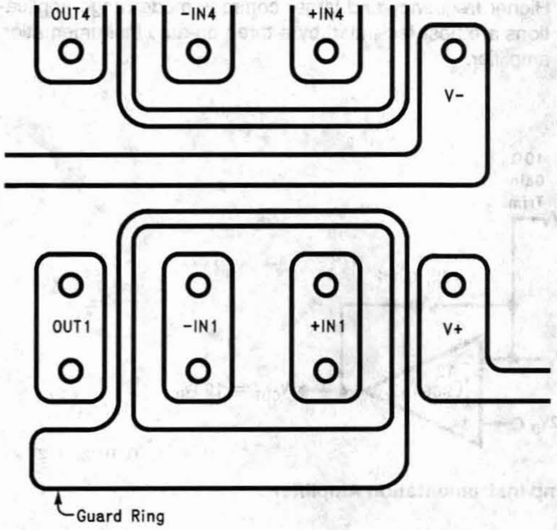

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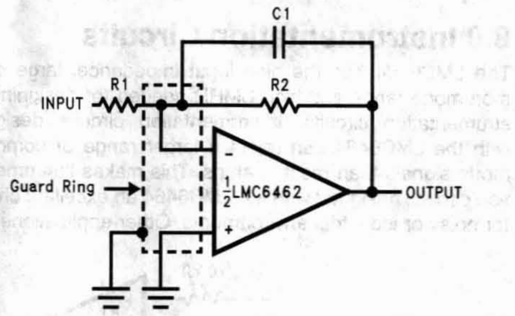
FIGURE 11. Example of Guard Ring in P.C. Board Layout



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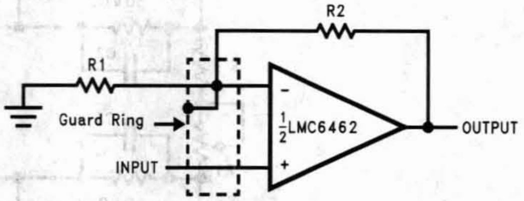
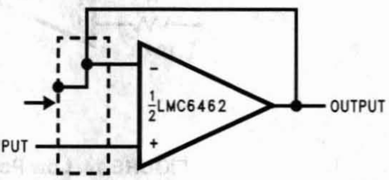
(a) Inverting Amplifier



TL/H/12051-17

(b) Non-Inverting Amplifier

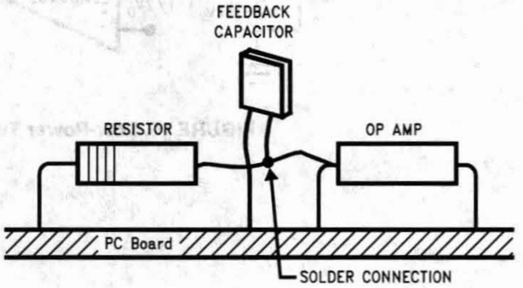


TL/H/12051-18

(c) Follower

FIGURE 12. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 13*.



TL/H/12051-19

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

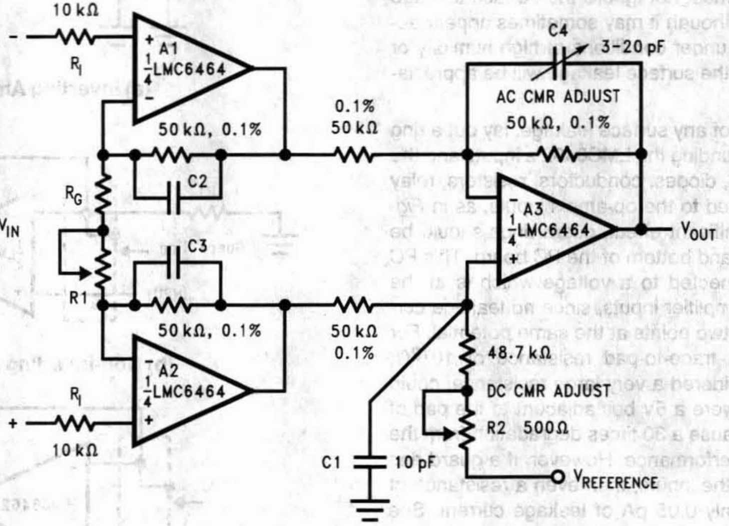
FIGURE 13. Air Wiring

Application Information (Continued)

8.0 Instrumentation Circuits

The LMC6464 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6464 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6464 an excellent choice for noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with Rg to set the differential gain of the three op-amp instrumentation circuit in *Figure 14*. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.



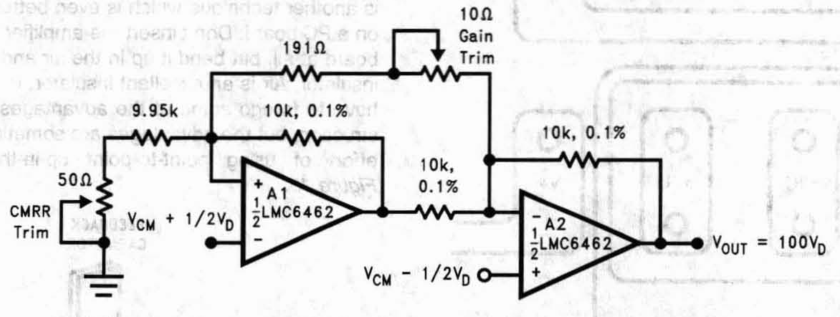
10 kΩ
−
R_I
A1
$\frac{1}{4}$LMC6464
50 kΩ, 0.1%
R_G
C2
V_{IN}
C3
R1
50 kΩ, 0.1%
A2
$\frac{1}{4}$LMC6464
R_I
+
10 kΩ
0.1%
50 kΩ
50 kΩ
0.1%
C4
3-20 pF
AC CMR ADJUST
50 kΩ, 0.1%
A3
$\frac{1}{4}$LMC6464
V_{OUT}
48.7 kΩ
DC CMR ADJUST
R2 500Ω
C1
10 pF
$V_{REFERENCE}$

TL/H/12051-20

FIGURE 14. Low Power Three Op-Amp Instrumentation Amplifier

A two op-amp instrumentation amplifier designed for a gain of 100 is shown in *Figure 15*. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.



10Ω
Gain
Trim
191Ω
9.95k
10k, 0.1%
50Ω
CMRR
Trim
V_{CM} + 1/2V_D
A1
$\frac{1}{2}$LMC6462
10k,
0.1%
10k, 0.1%
A2
$\frac{1}{2}$LMC6462
V_{CM} − 1/2V_D
V_{OUT} = 100V_D

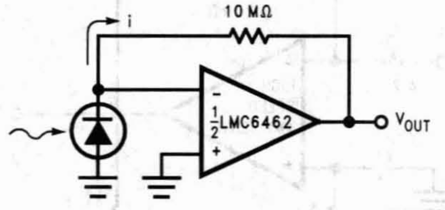
TL/H/12051-21

FIGURE 15. Low-Power Two-Op-Amp Instrumentation Amplifier

Application Information (Continued)

Typical Single-Supply Applications

TRANSDUCER INTERFACE CIRCUITS

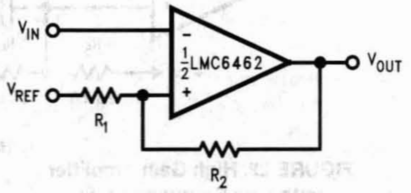

i
10 MΩ
$\frac{1}{2}$LMC6462
V_{OUT}

TL/H/12051–22

FIGURE 16. Photo Detector Circuit

Photocells can be used in portable light measuring instruments. The LMC6462, which can be operated off a battery, is an excellent choice for this circuit because of its very low input current and offset voltage.

LMC6462 AS A COMPARATOR

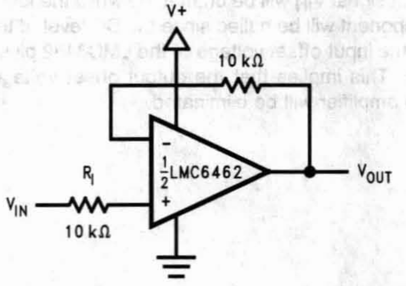

V_{IN}
$\frac{1}{2}$LMC6462
V_{OUT}
V_{REF}
R_1
R_2

TL/H/12051–23

FIGURE 17. Comparator with Hysteresis

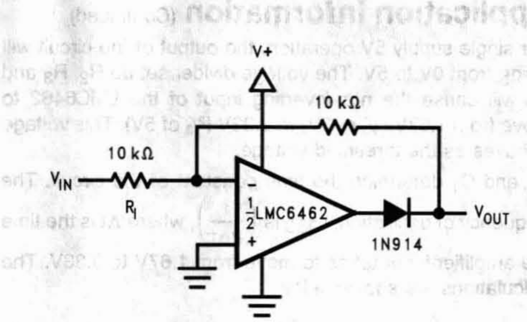
Figure 17 shows the application of the LMC6462 as a comparator. The hysteresis is determined by the ratio of the two resistors. The LMC6462 can thus be used as a micropower comparator, in applications where the quiescent current is an important parameter.

HALF-WAVE AND FULL-WAVE RECTIFIERS


V+
10 kΩ
R_I
$\frac{1}{2}$LMC6462
V_{OUT}
V_{IN}
10 kΩ

TL/H/12051–24

FIGURE 18. Half-Wave Rectifier with Input Current Protection (R_I)

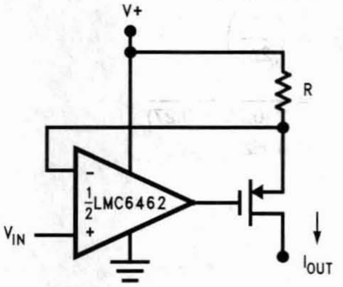

V+
10 kΩ
10 kΩ
V_{IN}
R_I
$\frac{1}{2}$LMC6462
1N914
V_{OUT}

TL/H/12051–25

FIGURE 19. Full-Wave Rectifier with Input Current Protection (R_I)

In *Figures 18* and *19*, R_I limits current into the amplifier since excess current can be caused by the input voltage exceeding the supply voltage.

PRECISION CURRENT SOURCE


V+
R
$\frac{1}{2}$LMC6462
V_{IN}
I_{OUT}

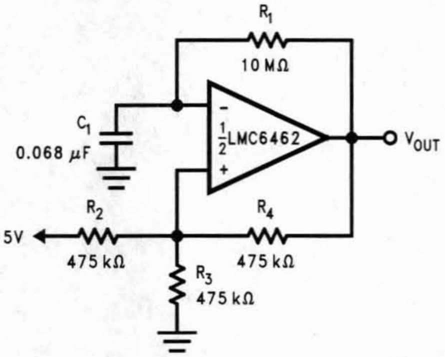
TL/H/12051–26

FIGURE 20. Precision Current Source

The output current I_{OUT} is given by:

$$I_{OUT} = \left(\frac{V+ - V_{IN}}{R}\right)$$

OSCILLATORS


R_1
10 MΩ
C_1
0.068 μF
$\frac{1}{2}$LMC6462
V_{OUT}
R_2
R_4
5V
475 kΩ
475 kΩ
R_3
475 kΩ

TL/H/12051–27

FIGURE 21. 1 Hz Square-Wave Oscillator

Application Information (Continued)

For single supply 5V operation, the output of the circuit will swing from 0V to 5V. The voltage divider set up R_2, R_3 and R_4 will cause the non-inverting input of the LMC6462 to move from 1.67V (⅓ of 5V) to 3.33V (⅔ of 5V). This voltage behaves as the threshold voltage.

R_1 and C_1 determine the time constant of the circuit. The frequency of oscillation, f_{OSC} is $\left(\frac{1}{2\Delta t}\right)$, where Δt is the time the amplifier input takes to move from 1.67V to 3.33V. The calculations are shown below.

$$1.67 = 5\left(1 - e^{-\frac{t_1}{\tau}}\right)$$

where $\tau = RC = 0.68$ seconds

$$\rightarrow t_1 = 0.27 \text{ seconds.}$$

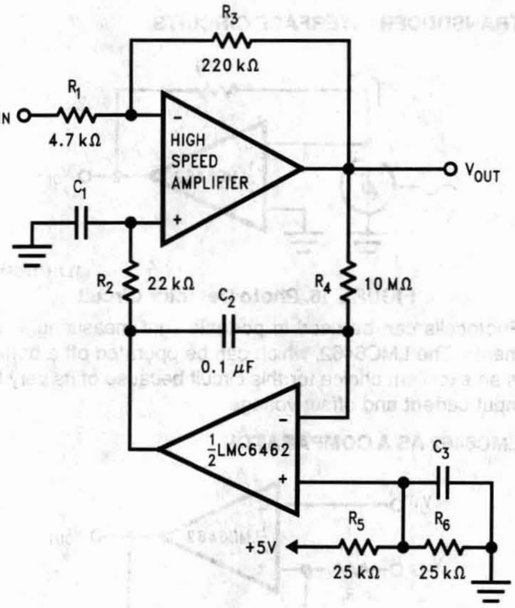
and

$$3.33 = 5\left(1 - e^{-\frac{t_2}{\tau}}\right)$$

$$\rightarrow t_2 = 0.75 \text{ seconds}$$

$$\text{Then, } f_{OSC} = \left(\frac{1}{2\Delta t}\right) = \frac{1}{2\,(0.75 - 0.27)} = 1 \text{ Hz}$$

LOW FREQUENCY NULL



TL/H/12051-28

FIGURE 22. High Gain Amplifier with Low Frequency Null

Output offset voltage is the error introduced in the output voltage due to the inherent input offset voltage V_{OS}, of an amplifier.

Output Offset Voltage = (Input Offset Voltage) (Gain)

In the above configuration, the resistors R_5 and R_6 determine the nominal voltage around which the input signal, V_{IN} should be symmetrical. The high frequency component of the input signal V_{IN} will be unaffected while the low frequency component will be nulled since the DC level of the output will be the input offset voltage of the LMC6462 plus the bias voltage. This implies that the output offset voltage due to the top amplifier will be eliminated.

National Semiconductor

LMC6482 CMOS Dual Rail-To-Rail Input and Output Operational Amplifier

General Description

The LMC6482 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6482 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC272 and TLC277.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6482's rail-to-rail output swing. The LMC6482's rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6482 especially well-suited for battery-operated systems.

See the LMC6484 data sheet for a Quad CMOS operational amplifier with these same features.

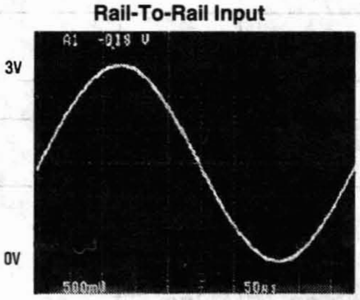
Features (Typical unless otherwise noted)

■ Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)	
■ Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)	
■ Guaranteed 3V, 5V and 15V Performance	
■ Excellent CMRR and PSRR	82 dB
■ Ultra Low Input Current	20 fA
■ High Voltage Gain ($R_L = 500\ k\Omega$)	130 dB
■ Specified for 2 kΩ and 600Ω loads	

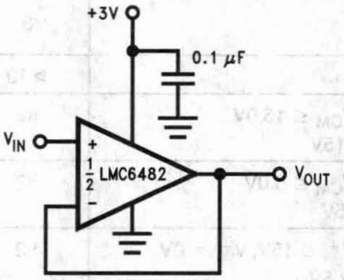
Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC272, TLC277

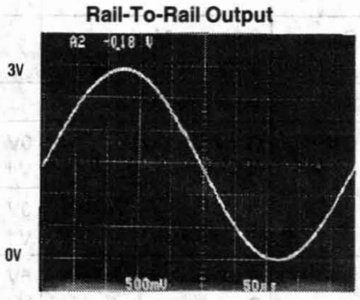
3V Single Supply Buffer Circuit



TL/H/11713-1

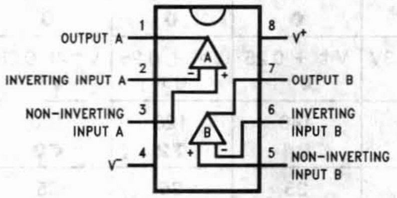


TL/H/11713-2



TL/H/11713-3

Connection Diagram



TL/H/11713-4

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
8-Pin Molded DIP	LMC6482MN	LMC6482AIN LMC6482IN	N08E	Rail
8-pin Small Outline		LMC6482AIM LMC6482IM	M08A	Rail Tape and Reel
8-pin Ceramic DIP	LMC6482AMJ/883		J08A	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	1.5 kV
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage $(V^+ - V^-)$	16V
Current at Input Pin (Note 12)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$3.0V \leq V^+ \leq 15.5V$
Junction Temperature Range	
LMC6482AM	$-55°C \leq T_J \leq +125°C$
LMC6482AI, LMC6482I	$-40°C \leq T_J \leq +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	90°C/W
M Package, 8-Pin Surface Mount	155°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			0.11	0.750 **1.35**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Current	(Note 13)		0.02	**4.0**	**4.0**	**10.0**	pA max
I_{OS}	Input Offset Current	(Note 13)		0.01	**2.0**	**2.0**	**5.0**	pA max
C_{IN}	Common-Mode Input Capacitance			3				pF
R_{IN}	Input Resistance			>10				TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 15.0V$ $V^+ = 15V$		82	70 **67**	65 **62**	65 **60**	dB min
		$0V \leq V_{CM} \leq 5.0V$ $V^+ = 5V$		82	70 **67**	65 **62**	65 **60**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V^+ \leq 15V$, $V^- = 0V$ $V_O = 2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-5V \leq V^- \leq -15V$, $V^+ = 0V$ $V_O = -2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and $15V$ For CMRR ≥ 50 dB		$V^- - 0.3$	−0.25 **0**	−0.25 **0**	−0.25 **0**	V max
				$V^+ + 0.3V$	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	V min
A_V	Large Signal Voltage Gain	$R_L = 2\ k\Omega$ (Notes 7, 13)	Sourcing	666	140 **84**	120 **72**	120 **60**	V/mV min
			Sinking	75	35 **20**	35 **20**	35 **18**	V/mV min
		$R_L = 600\Omega$ (Notes 7, 13)	Sourcing	300	80 **48**	50 **30**	50 **25**	V/mV min
			Sinking	35	20 **13**	15 **10**	15 **8**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_O	Output Swing	$V^+ = 5V$ $R_L = 2\ k\Omega$ to $V^+/2$	4.9	4.8 **4.7**	4.8 **4.7**	4.8 **4.7**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	0.18 **0.24**	V max
		$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$	4.7	4.5 **4.24**	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	0.5 **0.65**	V max
		$V^+ = 15V$ $R_L = 2\ k\Omega$ to $V^+/2$	14.7	14.4 **14.2**	14.4 **14.2**	14.4 **14.2**	V min
			0.16	0.32 **0.45**	0.32 **0.45**	0.32 **0.45**	V max
		$V^+ = 15V$ $R_L = 600\Omega$ to $V^+/2$	14.1	13.4 **13.0**	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.3**	1.0 **1.3**	1.0 **1.3**	V max
I_{SC}	Output Short Circuit Current $V^+ = 5V$	Sourcing, $V_O = 0V$	20	16 **12**	16 **12**	16 **10**	mA min
		Sinking, $V_O = 5V$	15	11 **9.5**	11 **9.5**	11 **8.0**	mA min
I_{SC}	Output Short Circuit Current $V^+ = 15V$	Sourcing, $V_O = 0V$	30	28 **22**	28 **22**	28 **20**	mA min
		Sinking, $V_O = 12V$ (Note 8)	30	30 **24**	30 **24**	30 **22**	mA min
I_S	Supply Current	Both Amplifiers $V^+ = +5V$, $V_O = V^+/2$	1.0	1.4 **1.8**	1.4 **1.8**	1.4 **1.9**	mA max
		Both Amplifiers $V^+ = 15V$, $V_O = V^+/2$	1.3	1.6 **1.9**	1.6 **1.9**	1.6 **2.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	1.3	1.0 **0.7**	0.9 **0.63**	0.9 **0.54**	V/μs min
GBW	Gain-Bandwidth Product	$V^+ = 15V$	1.5				MHz
ϕ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	(Note 10)	150				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz $V_{cm} = 1V$	37				nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.03				pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 10 kHz, $A_V = -2$ $R_L = 10\ k\Omega$, $V_O = 4.1\ V_{PP}$	0.01				%
		F = 10 kHz, $A_V = -2$ $R_L = 10\ k\Omega$, $V_O = 8.5\ V_{PP}$ $V^+ = 10V$	0.01				%

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.9	2.0 **2.7**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				μV/°C
I_B	Input Bias Current		0.02				pA
I_{OS}	Input Offset Current		0.01				pA
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 3V$	74	64	60	60	dB min
PSRR	Power Supply Rejection Ratio	$3V \leq V^+ \leq 15V, V^- = 0V$	80	68	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	$V^- - 0.25$	0	0	0	V max
			$V^+ + 0.25$	V^+	V^+	V^+	V min
V_O	Output Swing	$R_L = 2\ k\Omega$ to $V^+/2$	2.8				V
			0.2				V
		$R_L = 600\Omega$ to $V^+/2$	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
I_S	Supply Current	Both Amplifiers	0.825	1.2 **1.5**	1.2 **1.5**	1.2 **1.6**	mA max

AC Electrical Characteristics

Unless otherwise specified, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, and $R_L > 1M$.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
SR	Slew Rate	(Note 11)	0.9				V/μs
GBW	Gain-Bandwidth Product		1.0				MHz
T.H.D.	Total Harmonic Distortion	$F = 10\ kHz, A_V = -2$ $R_L = 10\ k\Omega, V_O = 2\ V_{PP}$	0.01				%

Note 1: Absolute Maximum Ratings indicate limts beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a Class 1 device rating.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $3.5V \leq V_O \leq 7.5V$.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\ V_{PP}$.

Note 11: Connected as voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

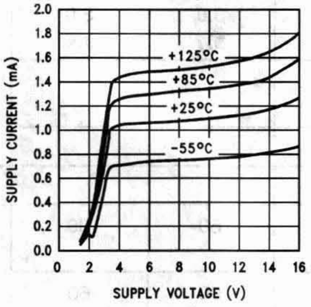
Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature parameters see RETS6482X.

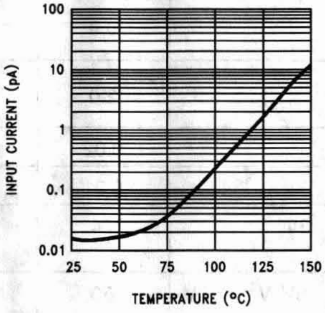
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25°C$ unless otherwise specified

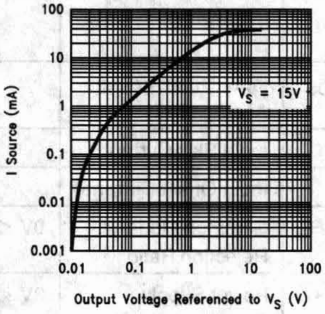
Supply Current vs Supply Voltage



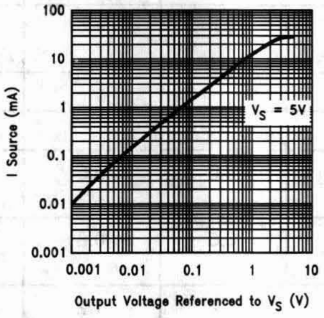
Input Current vs Temperature



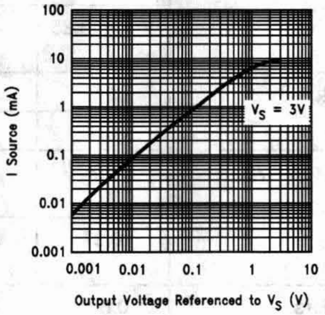
Sourcing Current vs Output Voltage



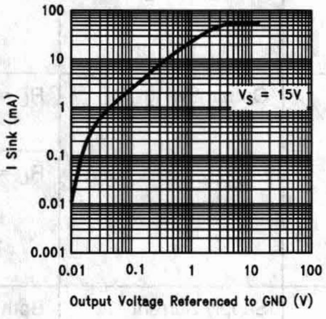
Sourcing Current vs Output Voltage



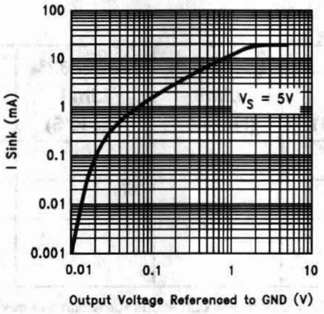
Sourcing Current vs Output Voltage



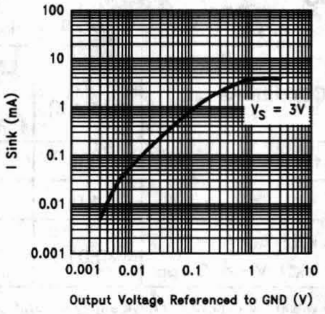
Sinking Current vs Output Voltage



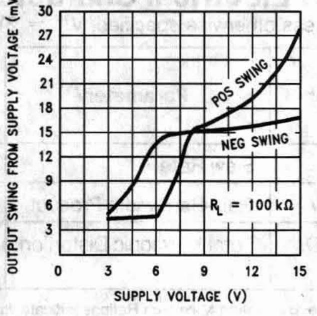
Sinking Current vs Output Voltage



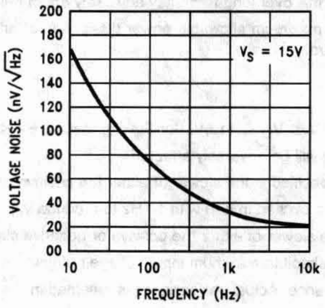
Sinking Current vs Output Voltage



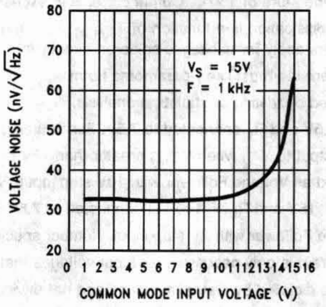
Output Voltage Swing vs Supply Voltage



Input Voltage Noise vs Frequency



Input Voltage Noise vs Input Voltage

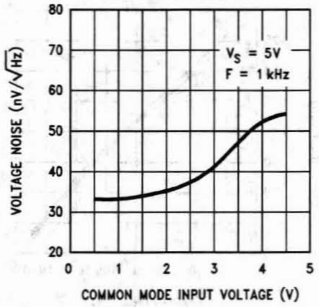


TL/H/11713–5

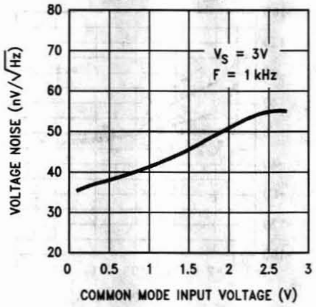
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

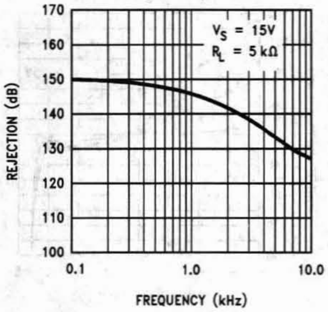
Input Voltage Noise vs Input Voltage



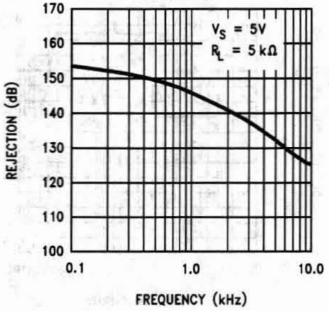
Input Voltage Noise vs Input Voltage



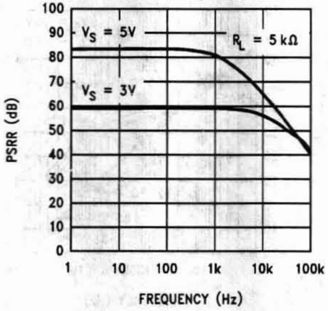
Crosstalk Rejection vs Frequency



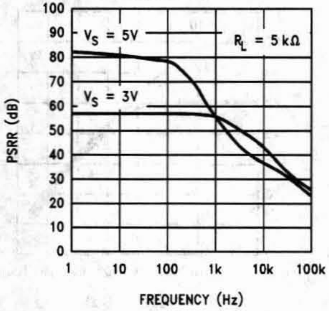
Crosstalk Rejection vs Frequency



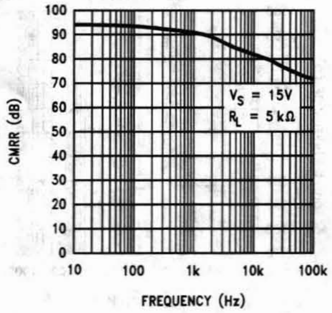
Positive PSRR vs Frequency



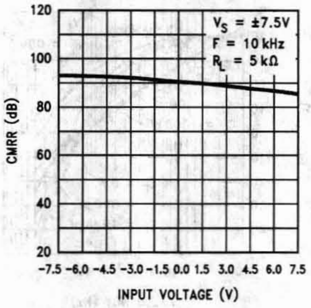
Negative PSRR vs Frequency



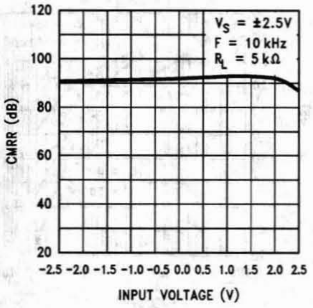
CMRR vs Frequency



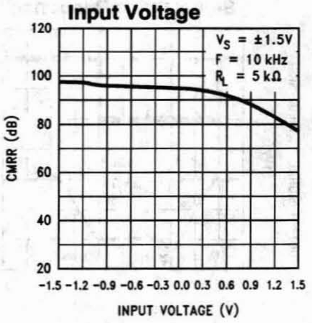
CMRR vs Input Voltage



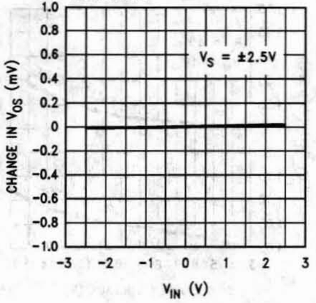
CMRR vs Input Voltage



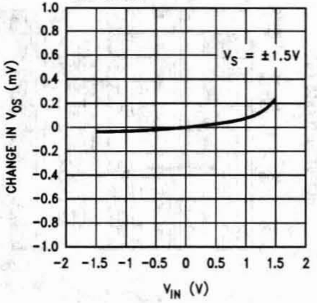
CMRR vs Input Voltage



ΔV_{OS} vs CMR



ΔV_{OS} vs CMR

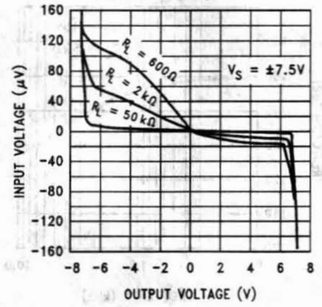


TL/H/11713–6

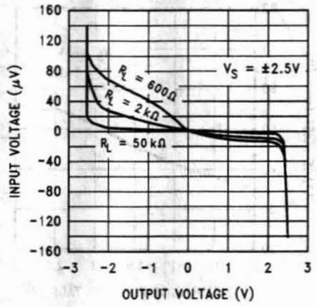
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

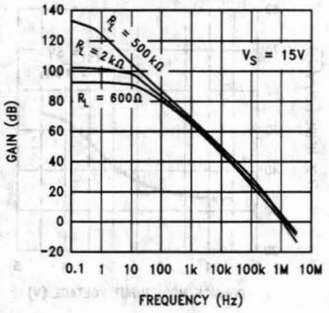
Input Voltage vs Output Voltage



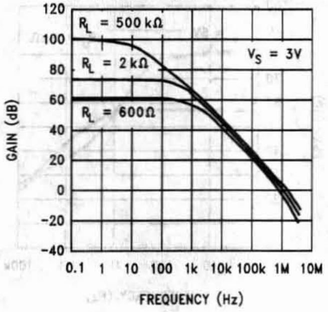
Input Voltage vs Output Voltage



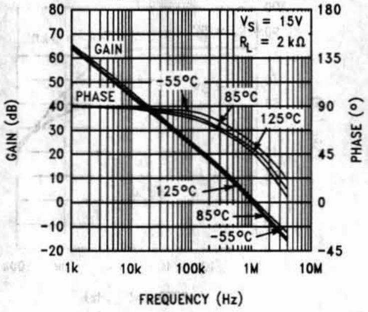
Open Loop Frequency Response



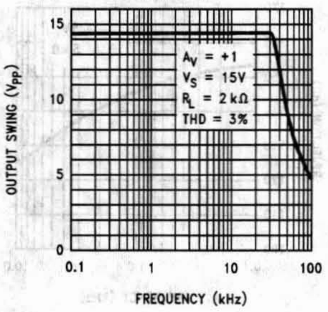
Open Loop Frequency Responce



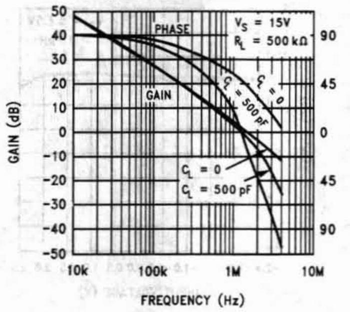
Open Loop Frequency Response vs Temperature



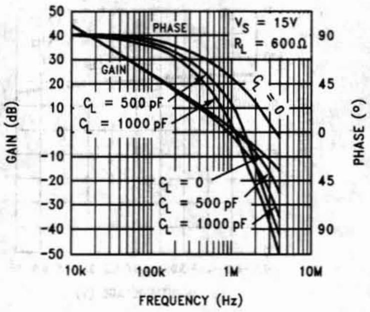
Maximum Output Swing vs Frequency



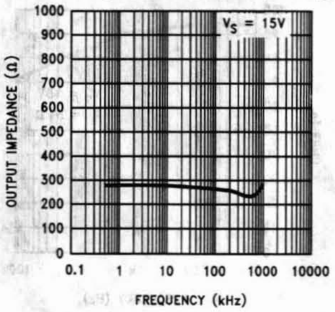
Gain and Phase vs Capacitive Load



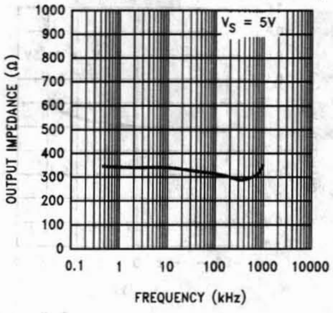
Gain and Phase vs Capacitive Load



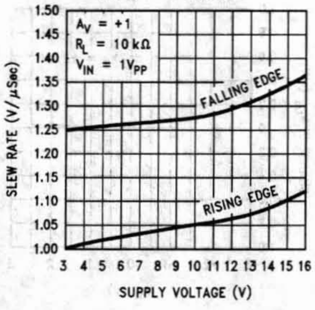
Open Loop Output Impedance vs Frequency



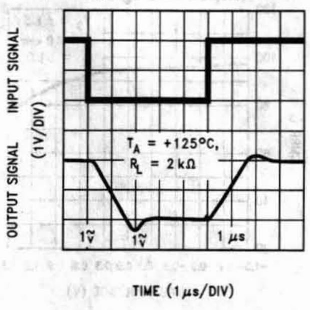
Open Loop Output Impedance vs Frequency



Slew Rate vs Supply Voltage



Non-Inverting Large Signal Pulse Response

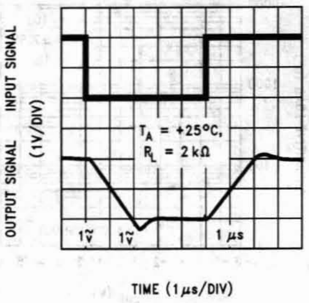


TL/H/11713-7

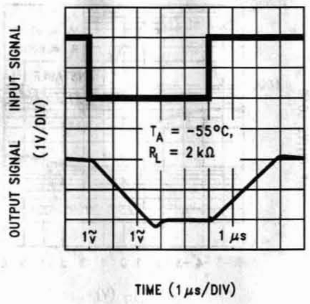
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

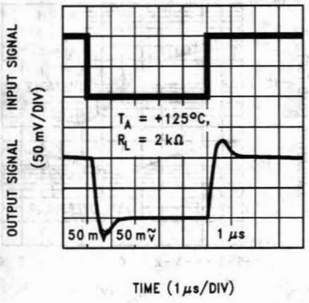
Non-Inverting Large Signal Pulse Response



Non-Inverting Large Signal Pulse Response



Non-Inverting Small Signal Pulse Response



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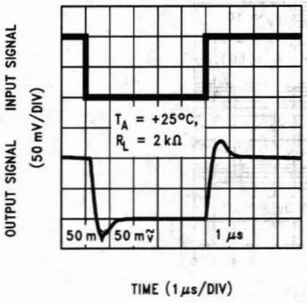
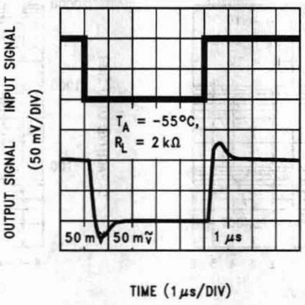
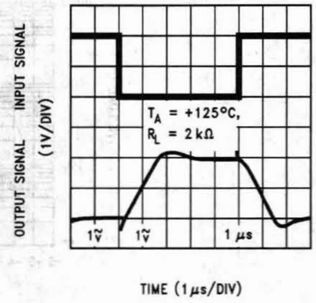


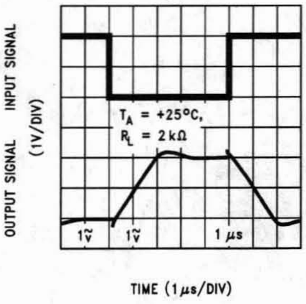
Non-Inverting Small Signal Pulse Response



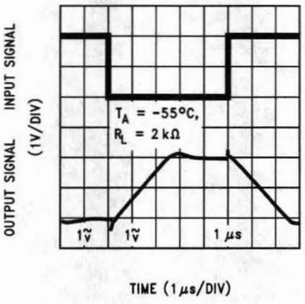
Inverting Large Signal Pulse Response



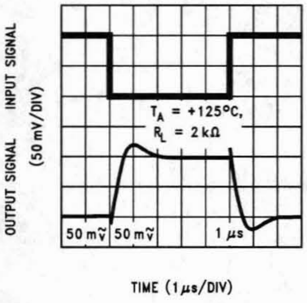
Inverting Large Signal Pulse Response



Inverting Large Signal Pulse Response



Inverting Small Signal Pulse Response



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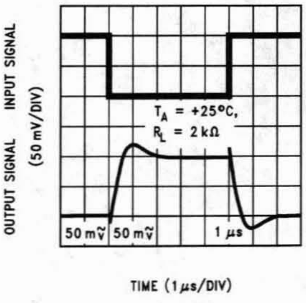
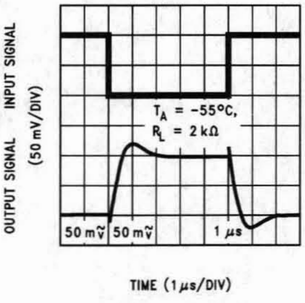
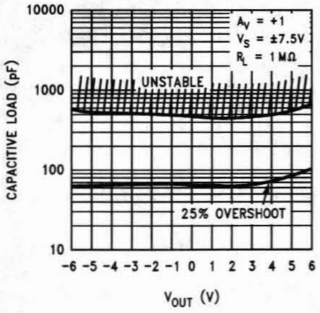
Inverting Small Signal Pulse Response



Inverting Small Signal Pulse Response



Stability vs Capacitive Load

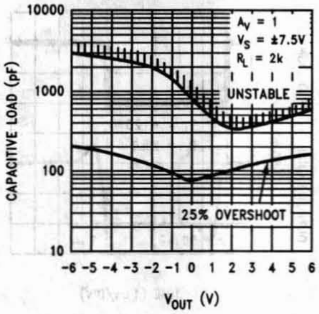


TL/H/11713–8

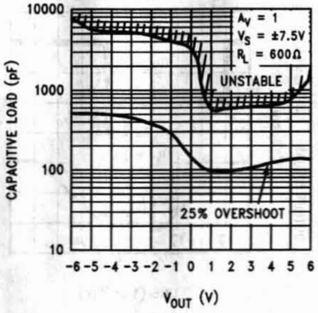
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

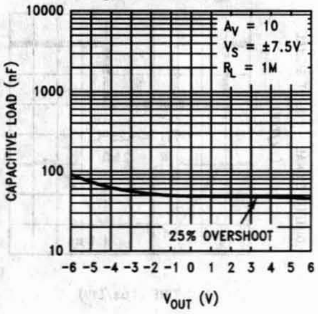
Stability vs Capacitive Load



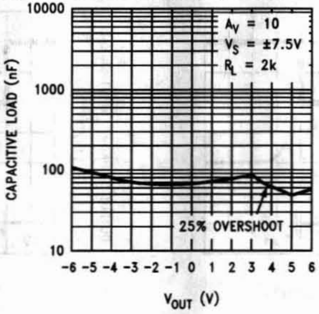
Stability vs Capacitive Load



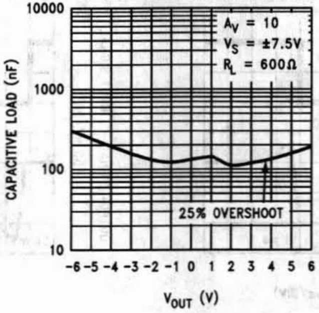
Stability vs Capacitive Load



Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/11713–9

Application Information

1.0 Amplifier Topology

The LMC6482 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6482's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

2.0 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6482 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

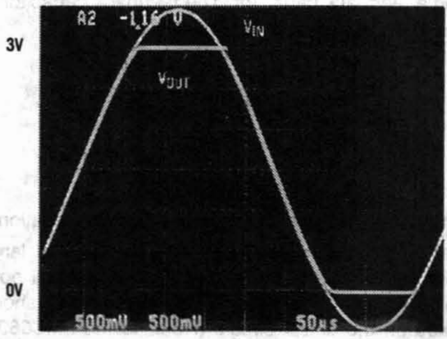


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FIGURE 1. An Input Voltage Signal Exceeds the LMC6482 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

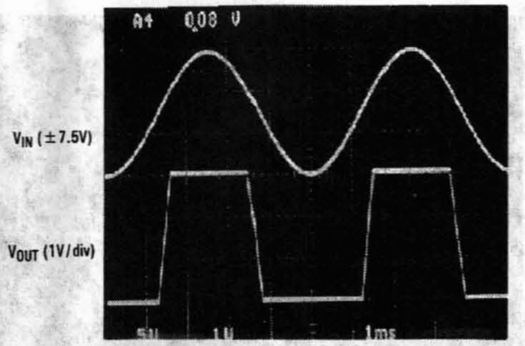

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FIGURE 2. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in *Figure 3* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor (R_I) as shown in *Figure 3*.

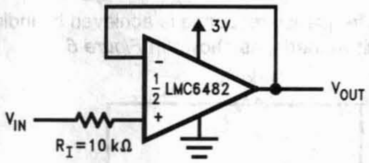

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FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

3.0 Rail-To-Rail Output

The approximated output resistance of the LMC6482 is 180Ω sourcing and 130Ω sinking at Vs = 3V and 110Ω sourcing and 80Ω sinking at Vs = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC6482 can typically directly drive a 100 pF load with V_S = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. This simple technique is useful for isolating the capacitive inputs of multiplexers and A/D converters.

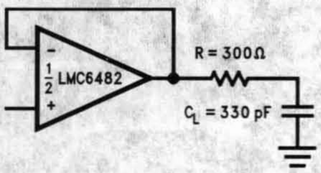

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FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

Application Information (Continued)

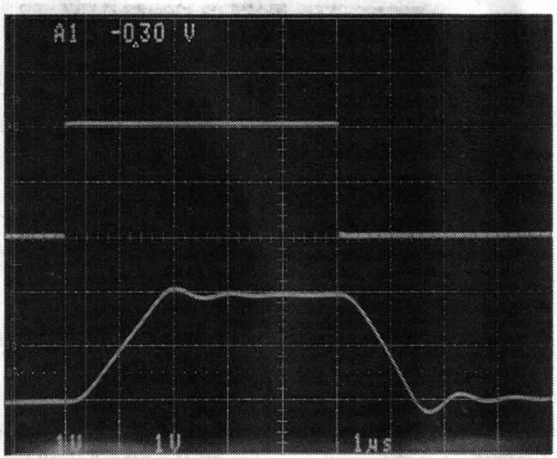

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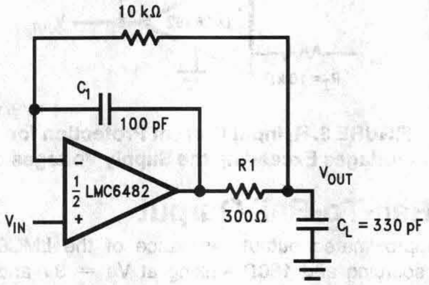
FIGURE 5. Pulse Response of the LMC6482 Circuit in *Figure 4*

Improved frequency response is achieved by indirectly driving capacitive loads, as shown in *Figure 6*.



TL/H/11713-15

FIGURE 6. LMC6482 Noninverting Amplifier, Compensated to Handle a 330 pF Capacitive Load

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in *Figure 7*.

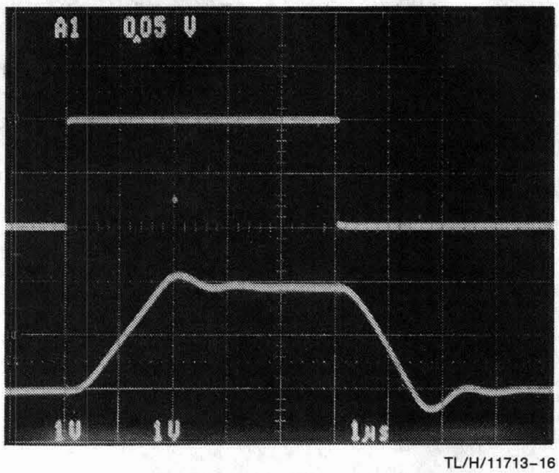


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FIGURE 7. Pulse Response of LMC6482 Circuit in *Figure 6*

5.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6482. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.

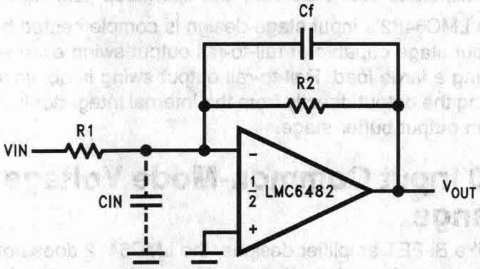

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FIGURE 8. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 8*), C_f, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

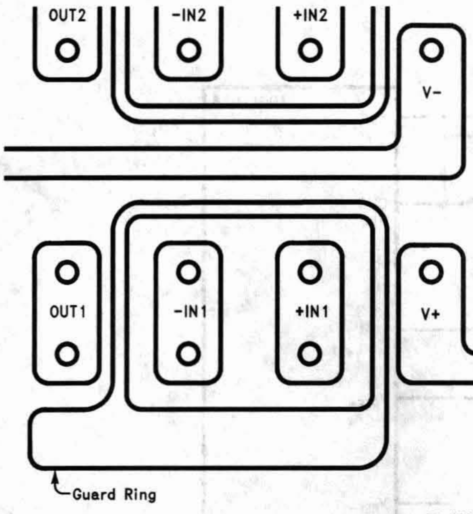
Printed circuit board stray capacitance may be larger or smaller than that of a bread-board, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

Application Information (Continued)

6.0 Printed-Circuit-Board Layout for High-Impedance Work

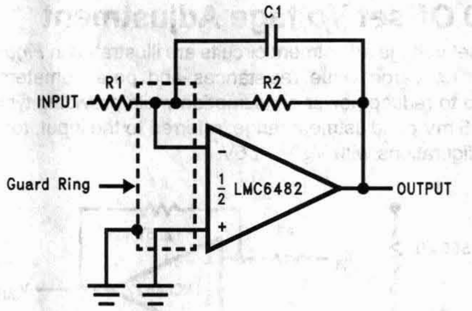
It is generally recognized that any circuit which must operrate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6482, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even through it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LM6482's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 9.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6482's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 10a, 10b, 10c* for typical connections of guard rings for standard op-amp configurations.



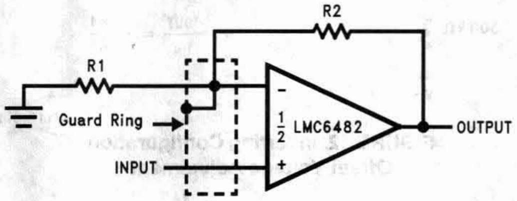
TL/H/11713-20

FIGURE 9. Example of Guard Ring in P.C. Board Layout



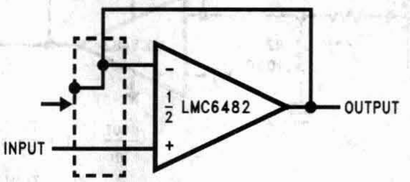
TL/H/11713-21

(a) Inverting Amplifier



TL/H/11713-22

(b) Non-Inverting Amplifier

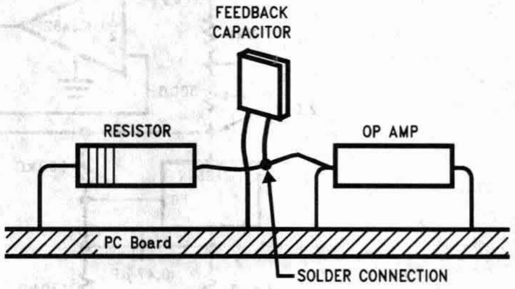


TL/H/11713-23

(c) Follower

FIGURE 10. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 11.*



TL/H/11713-24

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 11. Air Wiring

Application Information (Continued)

7.0 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in *Figure 12* and *13*. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with $V_S = \pm 5V$.

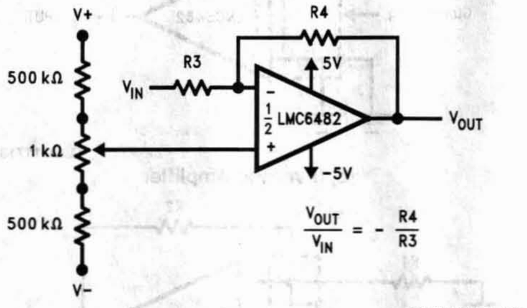

V+
R4
R3
5V
500 kΩ
V_{IN}
$\frac{1}{2}$ LMC6482
V_{OUT}
1 kΩ
-5V
500 kΩ
$\frac{V_{OUT}}{V_{IN}} = -\frac{R4}{R3}$
V-
TL/H/11713–25

FIGURE 12. Inverting Configuration Offset Voltage Adjustment

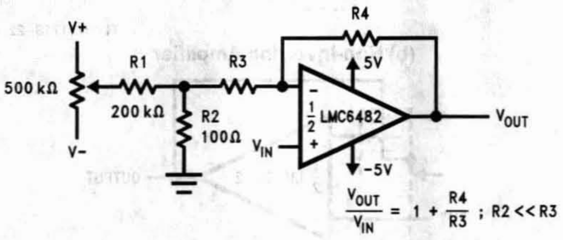

R4
V+
R1
R3
5V
500 kΩ
200 kΩ
R2
100Ω
$\frac{1}{2}$ LMC6482
V_{OUT}
V-
V_{IN}
-5V
$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R4}{R3}$; R2 << R3
TL/H/11713–26

FIGURE 13. Non-Inverting Configuration Offset Voltage Adjustment

8.0 Upgrading Applications

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6482's features. The key benefit of designing in the LMC6482 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inverison or severe distortion.

9.0 Data Acquisition Systems

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6482 *(Figure 14)*. Capable of using the full supply range, the LMC6482 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC4282 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.

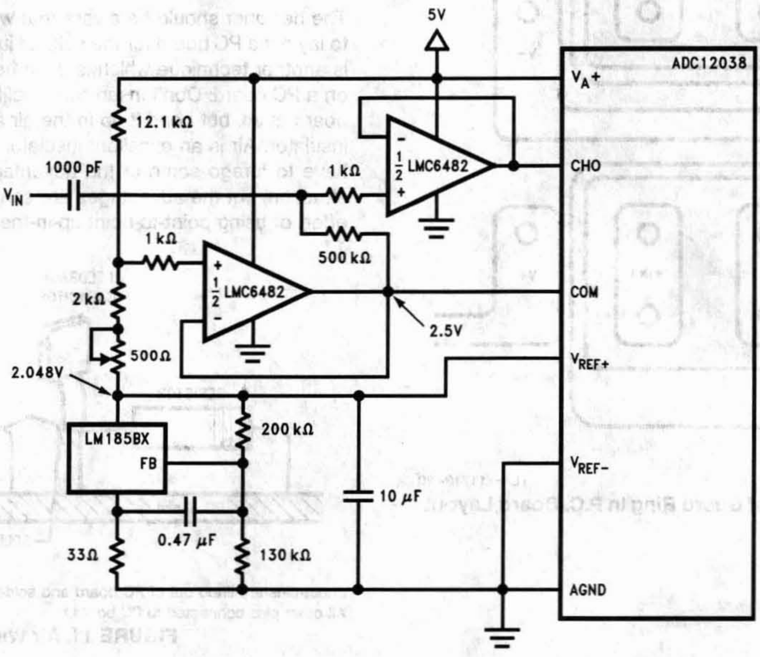

5V
ADC12038
V_A+
12.1 kΩ
1000 pF
V_{IN}
1 kΩ
$\frac{1}{2}$ LMC6482
CHO
1 kΩ
500 kΩ
$\frac{1}{2}$ LMC6482
COM
2 kΩ
2.5V
500Ω
V_{REF+}
2.048V
LM185BX
200 kΩ
FB
V_{REF-}
10 μF
0.47 μF
33Ω
130 kΩ
AGND
TL/H/11713–28

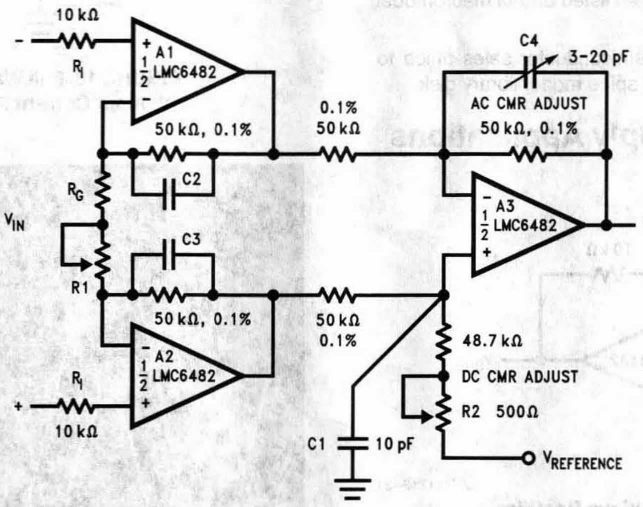
FIGURE 14. Operating from the same Supply Voltage, the LMC6482 buffers the ADC12038 maintaining excellent accuracy

Application Information (Continued)

10.0 Instrumentation Circuits

The LMC6482 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6482 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6482 an excellent choice of noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based tranducers.

A small valued potentiometer is used in series with R_g to set the differential gain of the 3 op-amp instrumentation circuit in *Figure 15*. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

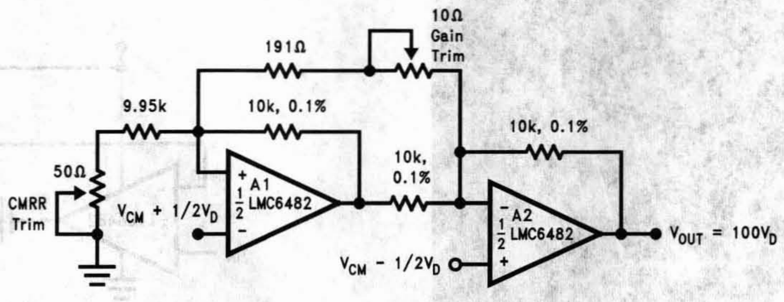

10 kΩ
R1
A1
1/2 LMC6482
50 kΩ, 0.1%
C2
RG
VIN
C3
R1
50 kΩ, 0.1%
A2
1/2 LMC6482
R1
10 kΩ
0.1%
50 kΩ
50 kΩ
0.1%
C4
3–20 pF
AC CMR ADJUST
50 kΩ, 0.1%
A3
1/2 LMC6482
VOUT
48.7 kΩ
DC CMR ADJUST
R2 500Ω
VREFERENCE
C1
10 pF

TL/H/11713–29

FIGURE 15. Low Power 3 Op-Amp Instrumentation Amplifier

A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in *Figure 16*. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.


10Ω
Gain
Trim
191Ω
9.95k
10k, 0.1%
50Ω
CMRR
Trim
VCM + 1/2VD
A1
1/2 LMC6482
10k,
0.1%
10k, 0.1%
A2
1/2 LMC6482
VCM − 1/2VD
VOUT = 100VD

TL/H/11713–30

FIGURE 16. Low-Power Two-Op-Amp Instrumentation Amplifier

Application Information (Continued)

11.0 Spice Macromodel

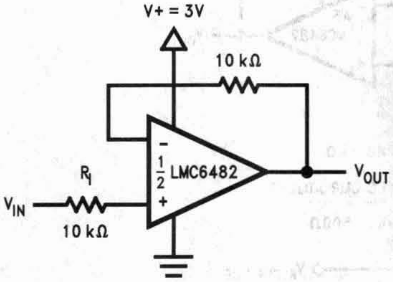
A spice macromodel is available for the LMC6482. This model includes accurate simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

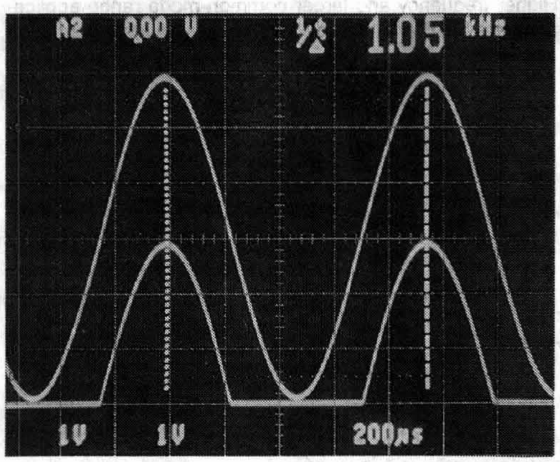
Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications



TL/H/11713–31

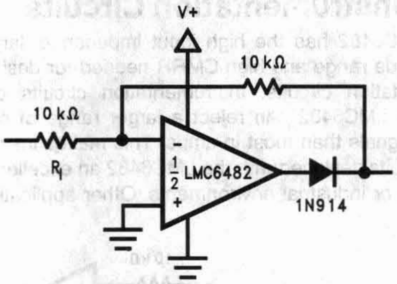
FIGURE 17. Half-Wave Rectifier with Input Current Protection (RI)



TL/H/11713–32

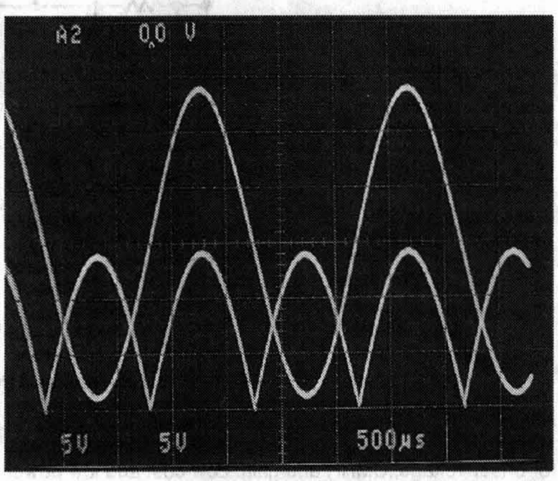
FIGURE 17A. Half-Wave Rectifier Waveform

The circuit in *Figure 17* uses a single supply to half wave rectify a sinusoid centered about ground. R$_I$ limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in *Figure 18*.



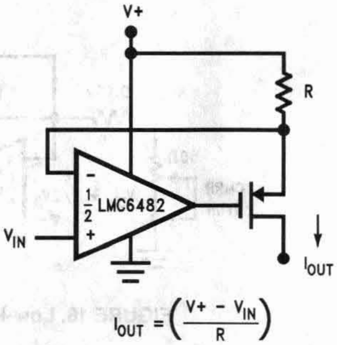
TL/H/11713–33

FIGURE 18. Full Wave Rectifier with Input Current Protection (R$_I$)



TL/H/11713–34

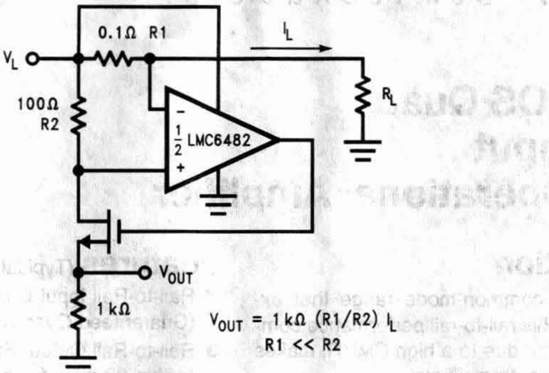
FIGURE 18A. Full Wave Rectifier Waveform



TL/H/11713–35

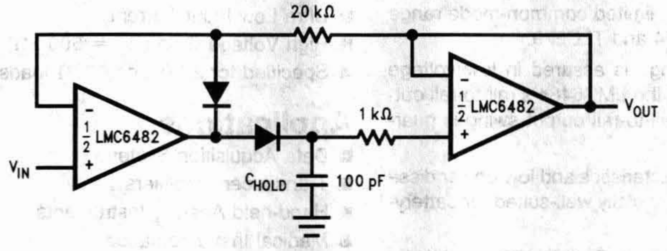
FIGURE 19. Large Compliance Range Current Source

Typical Single-Supply Applications


0.1Ω R1
I_L
V_L
100Ω
R2
R_L
$\frac{1}{2}$ LMC6482
V_{OUT}
1 kΩ
V_{OUT} = 1 kΩ (R1/R2) I_L
R1 << R2

TL/H/11713–36

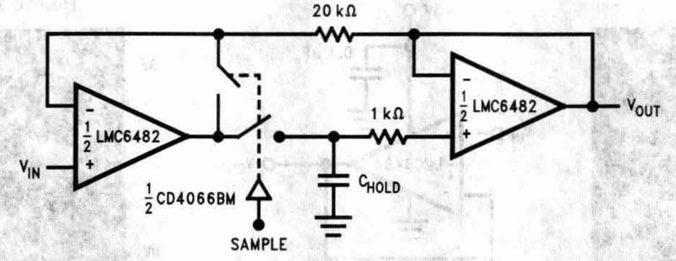
FIGURE 20. Positive Supply Current Sense


20 kΩ
$\frac{1}{2}$ LMC6482
$\frac{1}{2}$ LMC6482
1 kΩ
V_{OUT}
V_{IN}
C_{HOLD}
100 pF

TL/H/11713–37

FIGURE 21. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

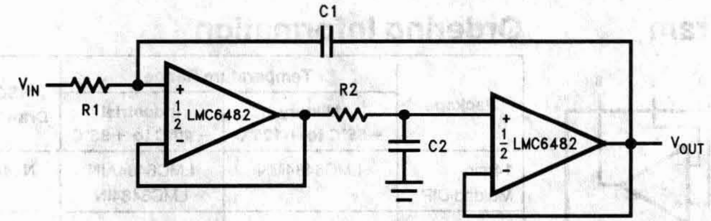
In *Figure 21* dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6482 has a negligible effect on droop.


20 kΩ
$\frac{1}{2}$ LMC6482
$\frac{1}{2}$ LMC6482
1 kΩ
V_{OUT}
V_{IN}
$\frac{1}{2}$ CD4066BM
C_{HOLD}
SAMPLE

TL/H/11713–38

FIGURE 22. Rail-to-Rail Sample and Hold

The LMC6482's high CMRR (82 dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.


C1
V_{IN}
R1
$\frac{1}{2}$ LMC6482
R2
C2
$\frac{1}{2}$ LMC6482
V_{OUT}

TL/H/11713–27

$$R1 = R2, C1 = C2; f = \frac{1}{2\pi R1\ C1}; DF = ½ \sqrt{\frac{C_2}{C_1}} \sqrt{\frac{R_2}{R_1}}$$

FIGURE 23. Rail-to-Rail Single Supply Low Pass Filter

The low pass filter circuit in *Figure 23* can be used as an anti-aliasing filter with the same voltage supply as the A/D converter.

Filter designs can also take advantage of the LMC6482 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

National Semiconductor

LMC6484 CMOS Quad Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6484 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6484 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC274 and TLC279.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6484's rail-to-rail output swing. The LMC6484's rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6484 especially well-suited for battery-operated systems.

See the LMC6482 data sheet for a Dual CMOS operational amplifier with these same features.

Features (Typical unless otherwise noted)

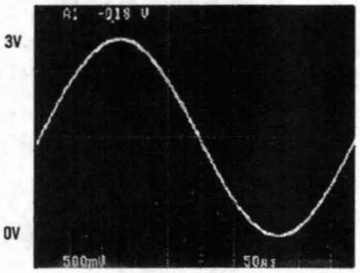
■ Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)	
■ Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)	
■ Guaranteed 3V, 5V and 15V Performance	
■ Excellent CMRR and PSRR	82 dB
■ Ultra Low Input Current	20 fA
■ High Voltage Gain (R_L = 500 kΩ)	130 dB
■ Specified for 2 kΩ and 600Ω loads	

Applications

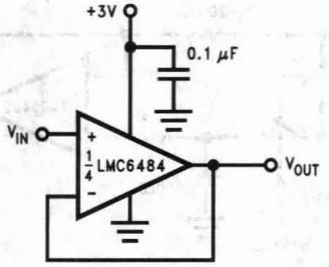
- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC274, TLC279

3V Single Supply Buffer Circuit

Rail-to-Rail Input

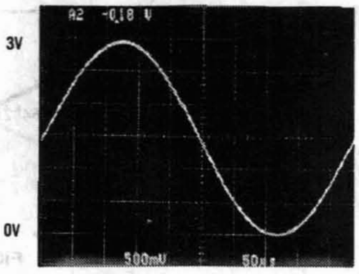


TL/H/11714–1



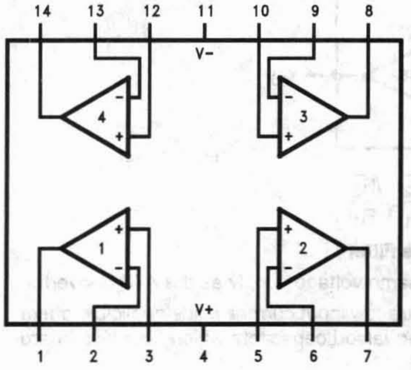
TL/H/11714–2

Rail-to-Rail Output



TL/H/11714–3

Connection Diagram



TL/H/11714–4

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
14-pin Molded DIP	LMC6484MN	LMC6484AIN LMC6484IN	N14A	Rail
14-pin Small Outline		LMC6484AIM LMC6484IM	M14A	Rail Tape and Reel
14-pin Ceramic DIP	LMC6484AMJ/883		J14A	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2.0 kV
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage $(V^+ - V^-)$	16V
Current at Input Pin (Note 12)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$3.0V \le V^+ \le 15.5V$
Junction Temperature Range	
LMC6484AM	$-55°C \le T_J \le +125°C$
LMC6484AI, LMC6484I	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 14-Pin Molded DIP	70°C/W
M Package, 14-Pin Surface Mount	110°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			0.110	0.750 **1.35**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Current	(Note 13)		0.02	**4.0**	**4.0**	**100**	pA max
I_{OS}	Input Offset Current	(Note 13)		0.01	**2.0**	**2.0**	**50**	pA max
C_{IN}	Common-Mode Input Capacitance			3				pF
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 15.0V$, $V^+ = 15V$		82	70 **67**	65 **62**	65 **60**	dB min
		$0V \le V_{CM} \le 5.0V$ $V^+ = 5V$		82	70 **67**	65 **62**	65 **60**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V^- = 0V, V_O = 2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-5V \le V^- \le -15V$, $V^+ = 0V, V_O = -2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB		$V^- - 0.3$	−0.25 **0**	−0.25 **0**	−0.25 **0**	V max
				$V^+ + 0.3$	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	V min
A_V	Large Signal Voltage Gain	$R_L = 2k\Omega$ (Notes 7, 13)	Sourcing	666	140 **84**	120 **72**	120 **60**	V/mV min
			Sinking	75	35 **20**	35 **20**	35 **18**	V/mV min
		$R_L = 600\Omega$ (Notes 7, 13)	Sourcing	300	80 **48**	50 **30**	50 **25**	V/mV min
			Sinking	35	20 **13**	15 **10**	15 **8**	V/mV min

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_O	Output Swing	$V^+ = 5V$ $R_L = 2\ k\Omega$ to $V^+/2$	4.9	4.8 **4.7**	4.8 **4.7**	4.8 **4.7**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	0.18 **0.24**	V max
		$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$	4.7	4.5 **4.24**	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	0.5 **0.65**	V max
		$V^+ = 15V$ $R_L = 2\ k\Omega$ to $V^+/2$	14.7	14.4 **14.2**	14.4 **14.2**	14.4 **14.2**	V min
			0.16	0.32 **0.45**	0.32 **0.45**	0.32 **0.45**	V max
		$V^+ = 15V$ $R_L = 600\Omega$ to $V^+/2$	14.1	13.4 **13.0**	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.3**	1.0 **1.3**	1.0 **1.3**	V max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0V$	20	16 **12**	16 **12**	16 **10**	mA min
	$V+ = 5V$	Sinking, $V_O = 5V$	15	11 **9.5**	11 **9.5**	11 **8.0**	mA min
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0V$	30	28 **22**	28 **22**	28 **20**	mA min
	$V^+ = 15V$	Sinking, $V_O = 12V$ (Note 8)	30	30 **24**	30 **24**	30 **22**	mA min
I_S	Supply Current	All Four Amplifiers $V^+ = +5V$, $V_O = V^+/2$	2.0	2.8 **3.6**	2.8 **3.6**	2.8 **3.8**	mA max
		All Four Amplifiers $V^+ = +15V$, $V_O = V^+/2$	2.6	3.0 **3.8**	3.0 **3.8**	3.0 **4.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484A Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	1.3	1.0 **0.7**	0.9 **0.63**	0.9 **0.54**	V/μs min
GBW	Gain-Bandwidth Product	$V^+ = 15V$	1.5				MHz
ϕ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	(Note 10)	150				dB
e_n	Input-Referred Voltage Noise	f = 1 kHz $V_{CM} = 1V$	37				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.03				$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	f = 1 kHz, $A_V = -2$ $R_L = 10\ k\Omega$, $V_O = 4.1\ V_{PP}$	0.01				%
		f = 10 kHz, $A_V = -2$ $R_L = 10\ k\Omega$, $V_O = 8.5\ V_{PP}$ $V^+ = 10V$	0.01				%

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.9	2.0 **2.7**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				μV/°C
I_B	Input Bias Current		0.02				pA
I_{OS}	Input Offset Current		0.01				pA
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 3V$	74	64	60	60	dB min
PSRR	Power Supply Rejection Ratio	$3V \le V^+ \le 15V$, $V^- = 0V$	80	68	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	$V^- - 0.25$	0	0	0	V max
			$V^+ + 0.25$	V^+	V^+	V^+	V min
V_O	Output Swing	$R_L = 2\ k\Omega$ to $V^+/2$	2.8				V
			0.2				V
		$R_L = 600\Omega$ to $V^+/2$	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
I_S	Supply Current	All Four Amplifiers	1.65	2.5 **3.0**	2.5 **3.0**	2.5 **3.2**	mA max

AC Electrical Characteristics

Unless otherwise specified, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
SR	Slew Rate	(Note 11)	0.9				V/μs
GBW	Gain-Bandwidth Product		1.0				MHz
T.H.D.	Total Harmonic Distortion	f = 10 kHz, $A_V = -2$ $R_L = 10\ k\Omega$, $V_O = 2\ V_{PP}$	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.

Note 3: Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $3.5V \le V_O \le 7.5V$.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\ V_{PP}$.

Note 11: Connected as Voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

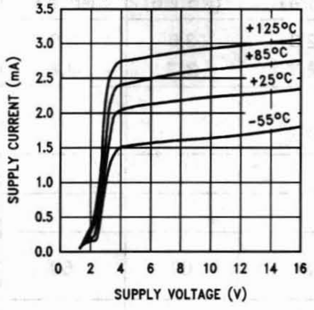
Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

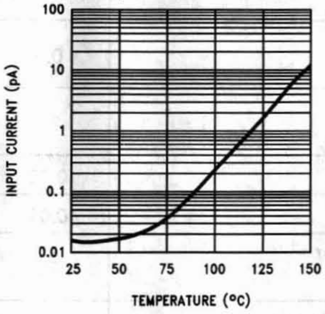
Note 14: For guaranteed Military Temperature Range parameters see RETSMC6484X.

Typical Performance Characteristics

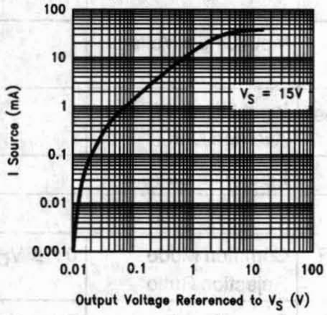
$V_S = +15V$, Single Supply, $T_A = 25°C$ unless otherwise specified



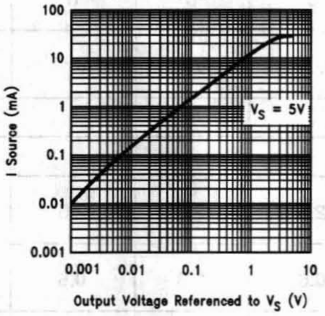
Supply Current vs Supply Voltage



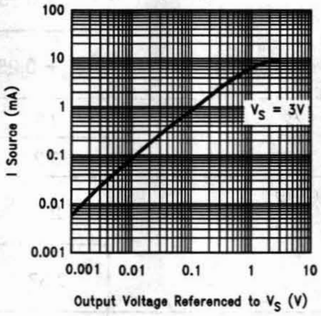
Input Current vs Temperature



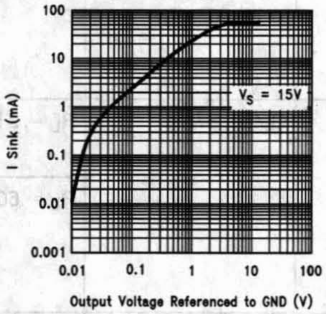
Sourcing Current vs Output Voltage



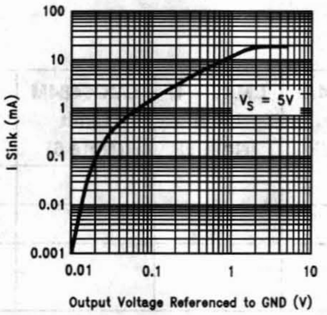
Sourcing Current vs Output Voltage



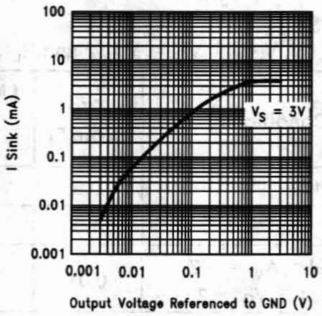
Sourcing Current vs Output Voltage



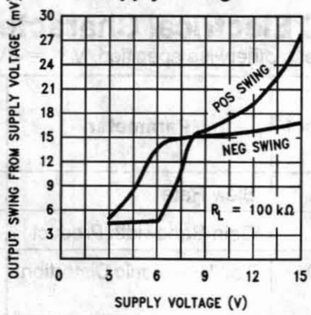
Sinking Current vs Output Voltage



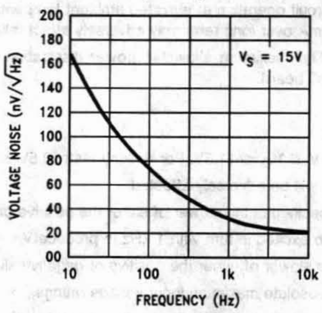
Sinking Current vs Output Voltage



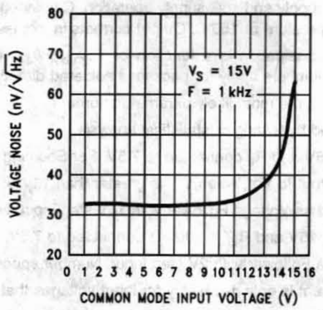
Sinking Current vs Output Voltage



Output Voltage Swing vs Supply Voltage



Input Voltage Noise vs Frequency



Input Voltage Noise vs Input Voltage

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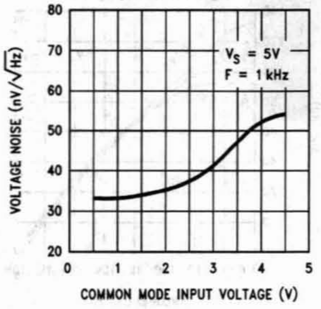
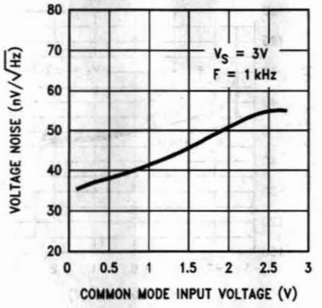
Typical Performance Characteristics

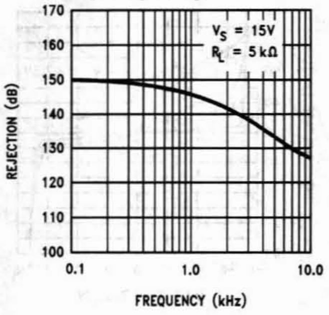
V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)



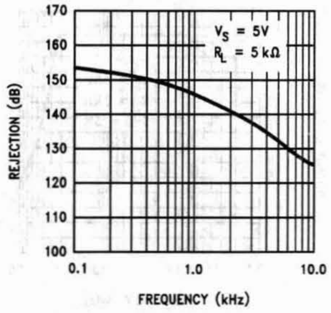
Input Voltage Noise vs Input Voltage



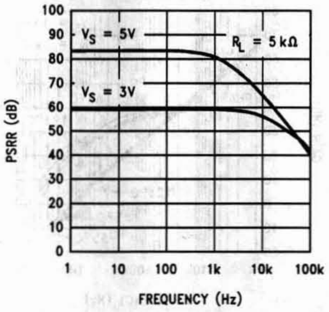
Input Voltage Noise vs Input Voltage



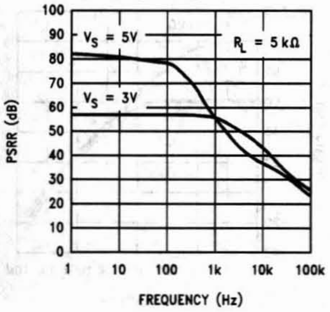
Crosstalk Rejection vs Frequency



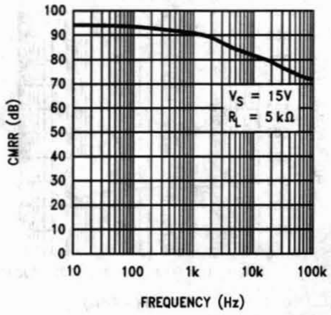
Crosstalk Rejection vs Frequency



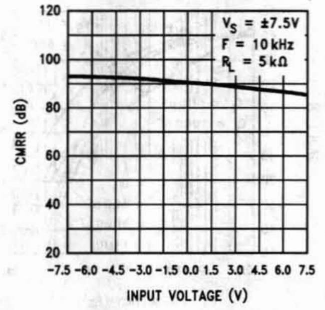
Positive PSRR vs Frequency



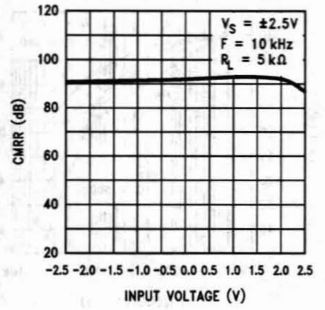
Negative PSRR vs Frequency



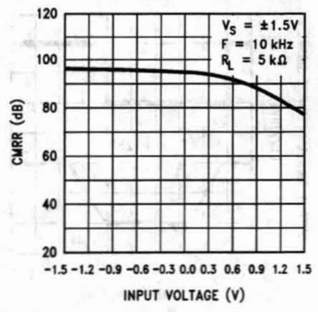
CMRR vs Frequency



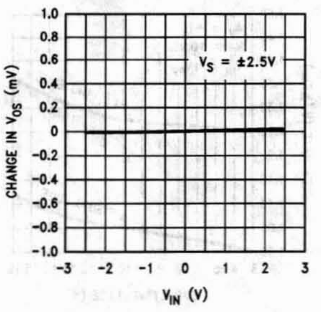
CMRR vs Input Voltage



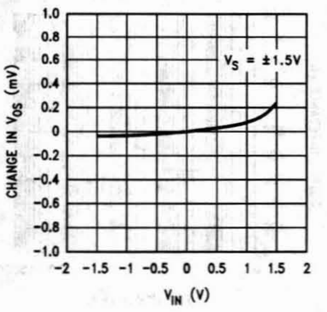
CMRR vs Input Voltage



CMRR vs Input Voltage



ΔV_{OS} vs CMR



ΔV_{OS} vs CMR

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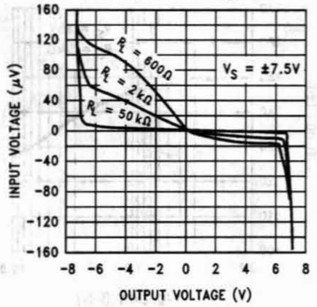
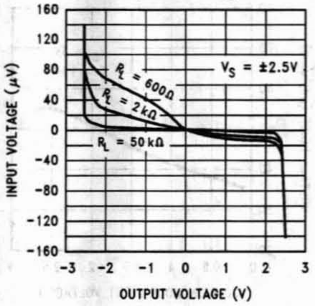
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25°C$ unless otherwise specified (Continued)

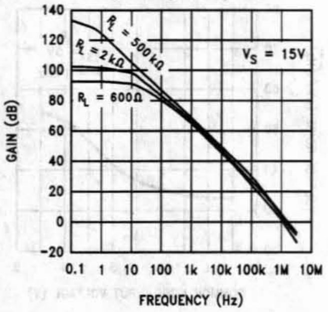
Input Voltage vs Output Voltage



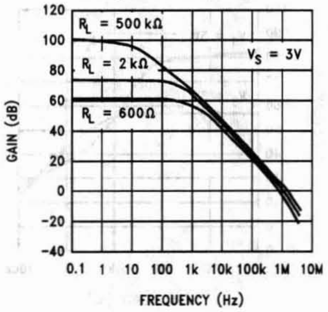
Input Voltage vs Output Voltage



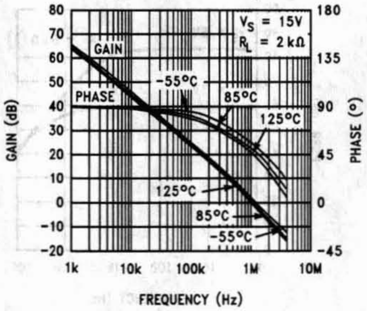
Open Loop Frequency Response



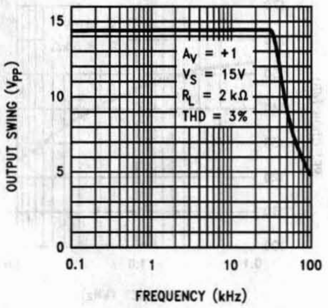
Open Loop Frequency Response



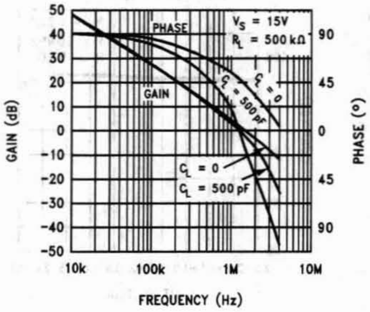
Open Loop Frequency Response vs Temperature



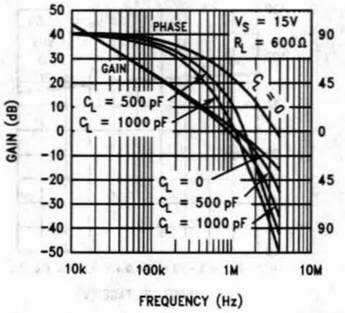
Maximum Output Swing vs Frequency



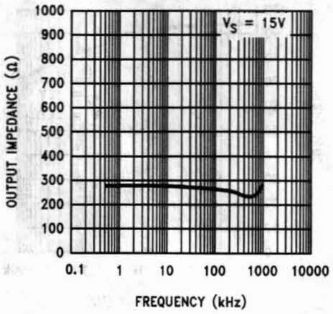
Gain and Phase vs Capacitive Load



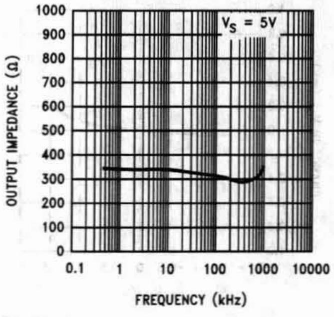
Gain and Phase vs Capacitive Load



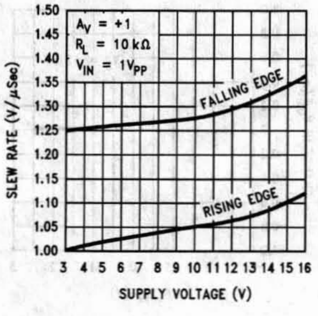
Open Loop Output Impedance vs Frequency



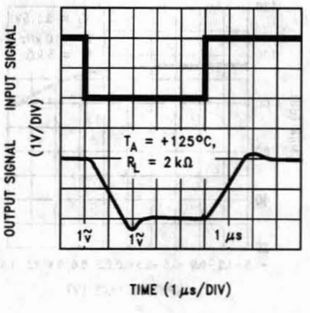
Open Loop Output Impedance vs Frequency



Slew Rate vs Supply Voltage



Non-Inverting Large Signal Pulse Response



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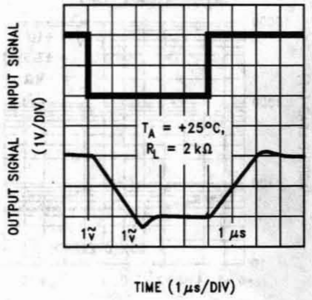
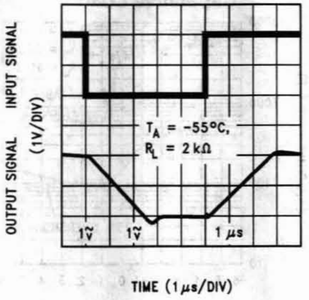
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

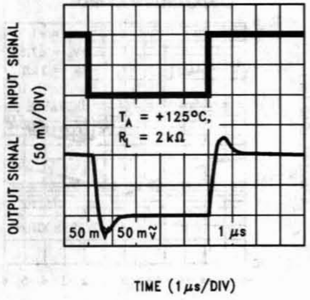
Non-Inverting Large Signal Pulse Response



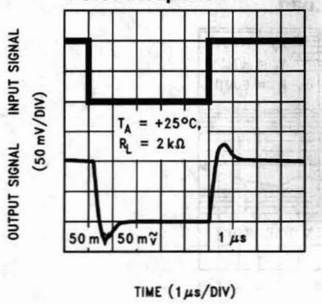
Non-Inverting Large Signal Pulse Response



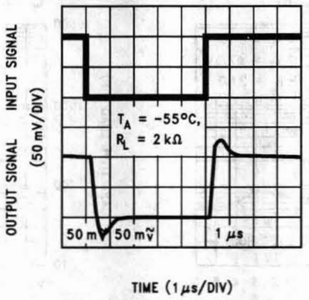
Non-Inverting Small Signal Pulse Response



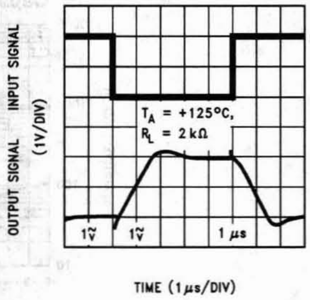
Non-Inverting Small Signal Pulse Response



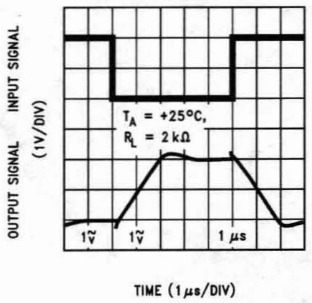
Non-Inverting Small Signal Pulse Response



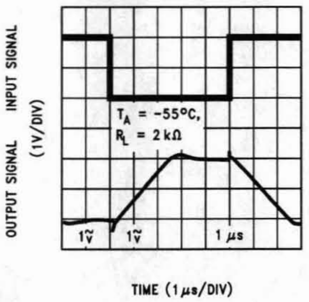
Inverting Large Signal Pulse Response



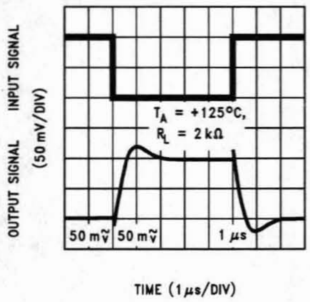
Inverting Large Signal Pulse Response



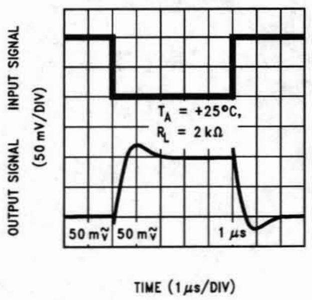
Inverting Large Signal Pulse Response



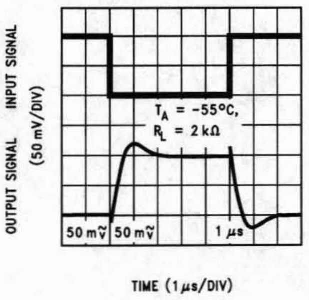
Inverting Small Signal Pulse Response



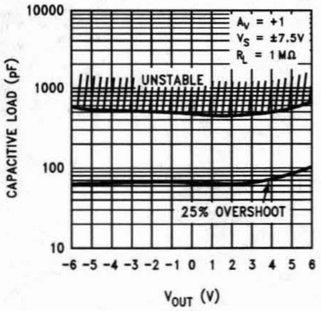
Inverting Small Signal Pulse Response



Inverting Small Signal Pulse Response



Stability vs Capacitive Load

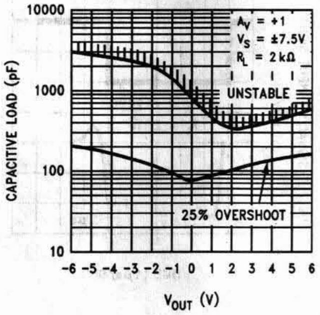


TL/H/11714–8

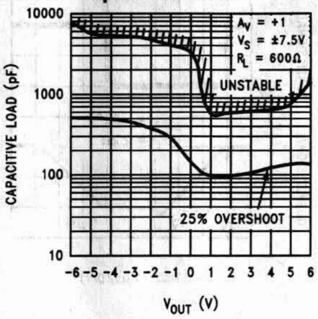
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

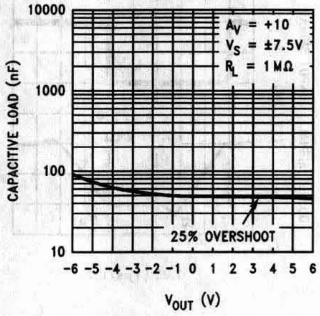
Stability vs Capacitive Load



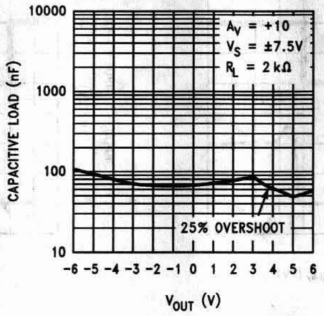
Stability vs Capacitive Load



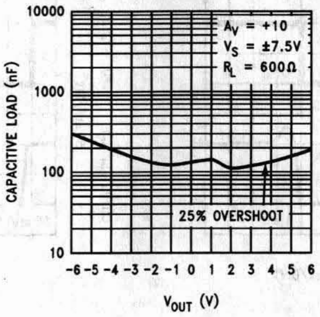
Stability vs Capacitive Load



Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/11714–9

Application Information (Continued)

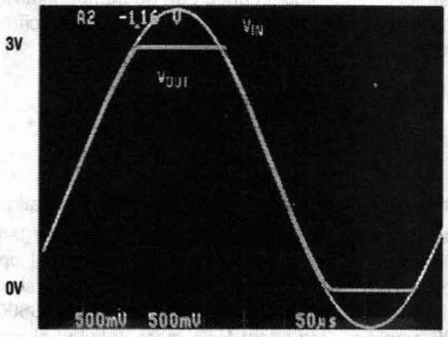
1.0 Amplifier Topology

The LMC6484 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6484's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

2.0 Input Common-Mode Voltage Range

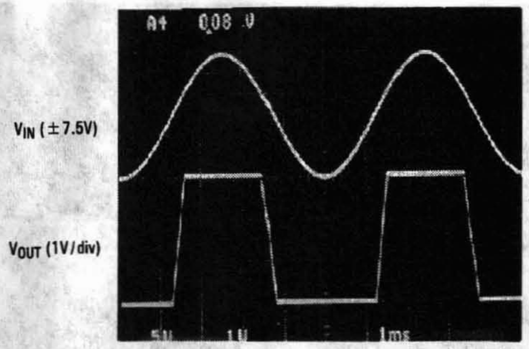
Unlike Bi-FET amplifier designs, the LMC6484 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion on the output.



TL/H/11714–10

FIGURE 1. An Input Voltage Signal Exceeds the LMC6484 Power Supply Voltages with No Output Phase Inversion

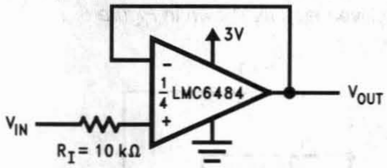
The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins possibly affecting reliability.



TL/H/11714–12

FIGURE 2. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in *Figure 3* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in *Figure 3*.



TL/H/11714–11

FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

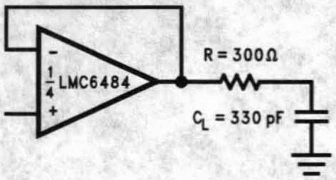
3.0 Rail-To-Rail Output

The approximated output resistance of the LMC6484 is 180Ω sourcing and 130Ω sinking at $V_S = 3V$ and 110Ω sourcing and 83Ω sinking at $V_S = 5V$. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC6484 can typically directly drive a 100 pF load with $V_S = 15V$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

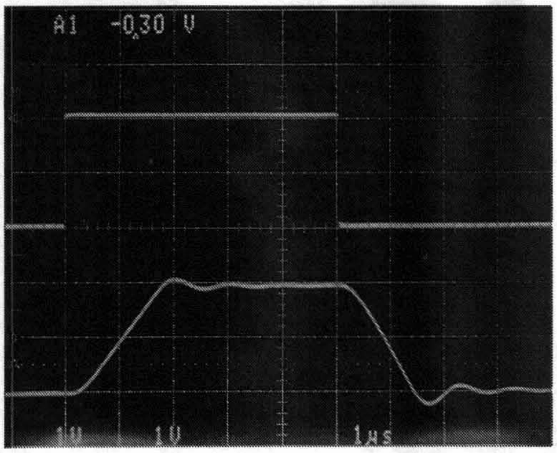
Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.



TL/H/11714–17

FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

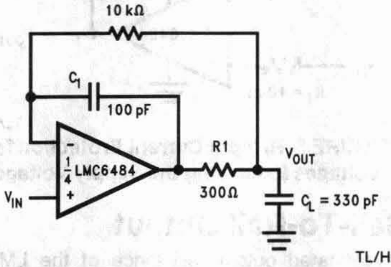
Application Information (Continued)



TL/H/11714–18

FIGURE 5. Pulse Response of the LMC6484 Circuit in *Figure 4*

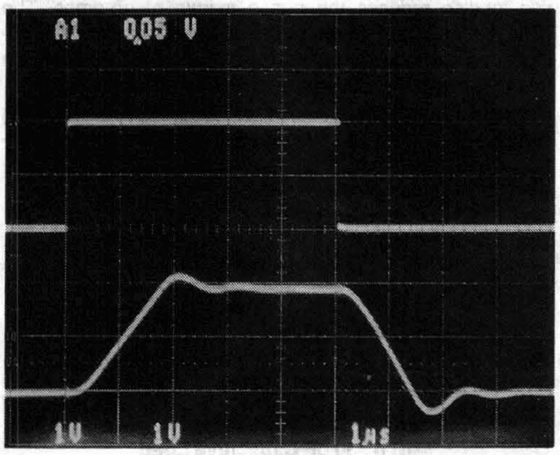
Improved frequency response is achieved by indirectly driving capacitive loads as shown in *Figure 6*.



TL/H/11714–15

FIGURE 6. LMC6484 Non-Inverting Amplifier, Compensated to Handle a 330 pF Capacitive Load

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in *Figure 7*.

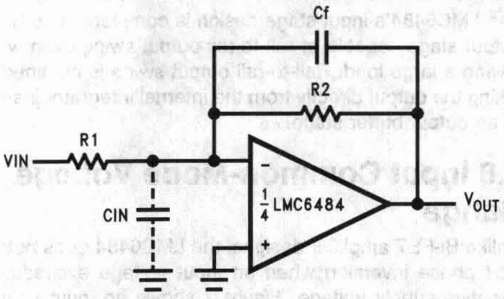


TL/H/11714–16

FIGURE 7. Pulse Response of LMC6484 Circuit in *Figure 6*

5.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6484. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.



TL/H/11714–19

FIGURE 8. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 8*), C_f, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

Application Information (Continued)

6.0 Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. when one wishes to take advantage of the ultra-low input current of the LMC6484, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6484's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 9*. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6484's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 10a*, *10b* and *10c* for typical connections of guard rings for standard op-amp configurations.

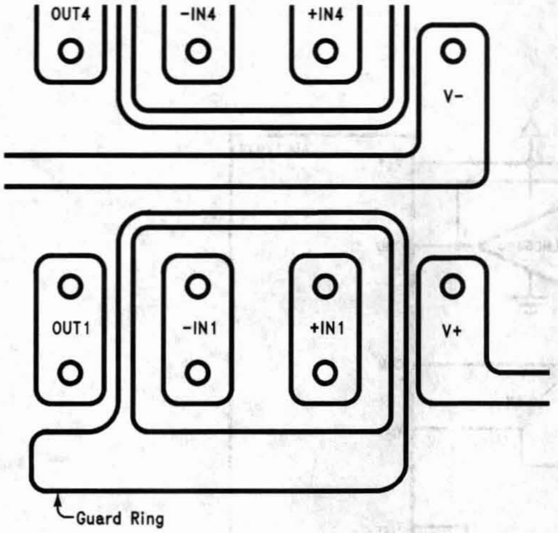


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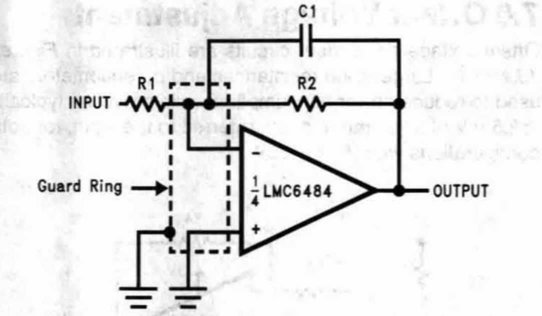
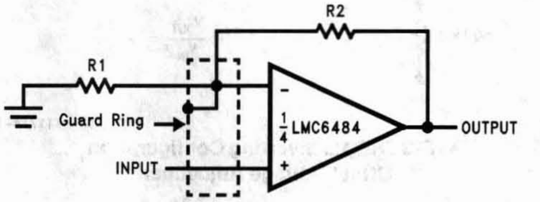
FIGURE 9. Example of Guard Ring in P.C. Board Layout



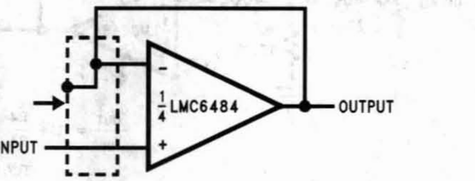
TL/H/11714–21

(a) Inverting Amplifier



TL/H/11714–22

(b) Non-Inverting Amplifier

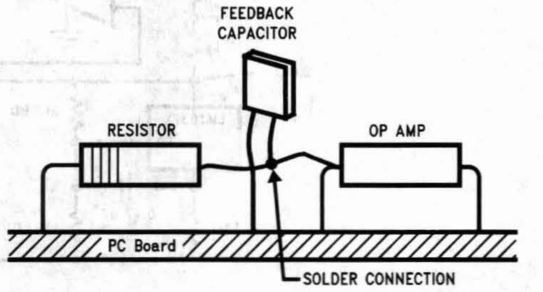


TL/H/11714–23

(c) Follower

FIGURE 10. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 11*.



TL/H/11714–24

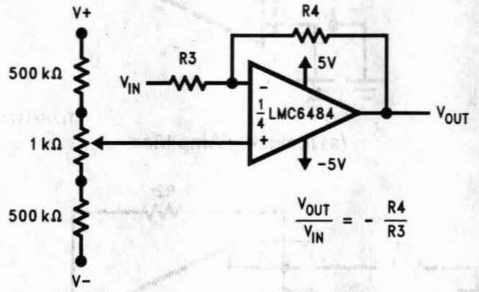
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 11. Air Wiring

Application Information (Continued)

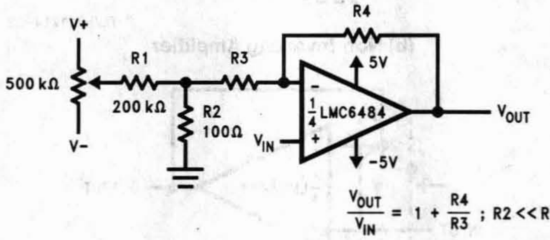
7.0 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in *Figures 13* and *14.* Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with $V_S = \pm 5V$.


V+
R4
R3
5V
500 kΩ
V_{IN}
$\frac{1}{4}$ LMC6484
V_{OUT}
1 kΩ
-5V
500 kΩ
V-
$\frac{V_{OUT}}{V_{IN}} = -\frac{R4}{R3}$

TL/H/11714–25

FIGURE 12. Inverting Configuration Offset Voltage Adjustment


R4
V+
R1
R3
5V
500 kΩ
200 kΩ
R2
100Ω
$\frac{1}{4}$ LMC6484
V_{OUT}
V-
V_{IN}
-5V
$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R4}{R3}$; R2 << R3

TL/H/11714–26

FIGURE 13. Non-Inverting Configuration Offset Voltage Adjustment

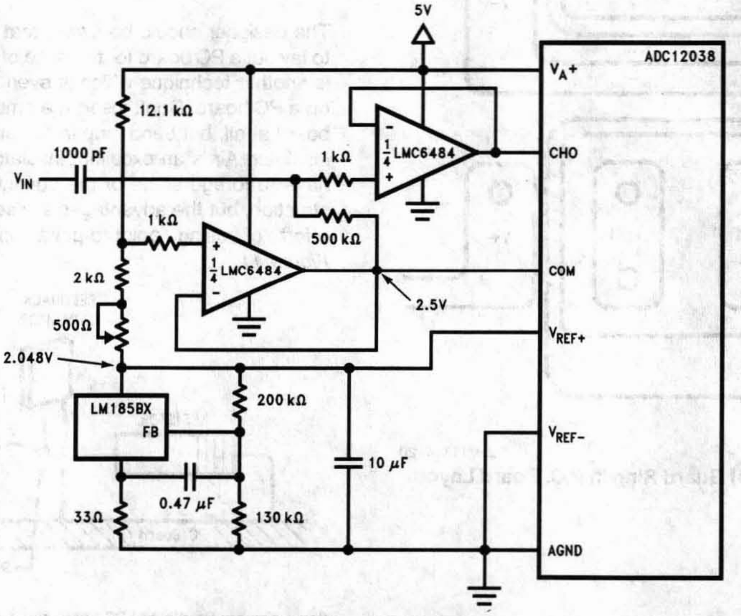
8.0 Upgrading Applications

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6484's features. The key benefit of designing in the LMC6484 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inversion or severe distortion.

9.0 Data Acquisition Systems

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6484 *(Figure 14).* Capable of using the full supply range, the LMC6484 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC6484 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.


5V
ADC12038
V_A+
12.1 kΩ
$\frac{1}{4}$ LMC6484
1000 pF
1 kΩ
CH0
V_{IN}
1 kΩ
500 kΩ
$\frac{1}{4}$ LMC6484
2 kΩ
COM
2.5V
500Ω
V_{REF+}
2.048V
LM185BX
FB
200 kΩ
V_{REF-}
10 µF
0.47 µF
33Ω
130 kΩ
AGND

TL/H/11714–28

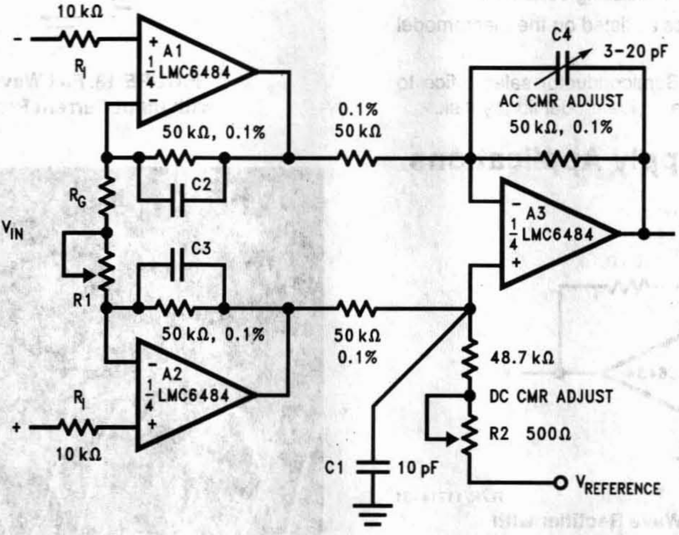
FIGURE 14. Operating from the same Supply Voltage, the LMC6484 buffers the ADC12038 maintaining excellent accuracy

Application Information (Continued)

10.0 Instrumentation Circuits

The LMC6484 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6484 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6484 an excellent choice for noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with Rg to set the differential gain of the 3 op-amp instrumentation circuit in *Figure 15*. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

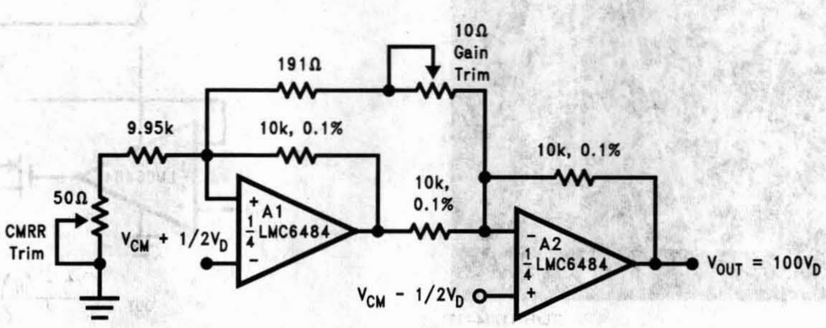

10 kΩ
R_I
A1
1/4 LMC6484
50 kΩ, 0.1%
C2
R_G
V_{IN}
C3
R1
50 kΩ, 0.1%
A2
1/4 LMC6484
R_I
10 kΩ
0.1%
50 kΩ
50 kΩ
0.1%
C4
3-20 pF
AC CMR ADJUST
50 kΩ, 0.1%
A3
1/4 LMC6484
V_{OUT}
48.7 kΩ
DC CMR ADJUST
R2 500Ω
C1
10 pF
$V_{REFERENCE}$

TL/H/11714-29

FIGURE 15. Low Power 3 Op-Amp Instrumentation Amplifier

A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in *Figure 16*. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.


191Ω
10Ω
Gain
Trim
9.95k
10k, 0.1%
50Ω
CMRR
Trim
V_{CM} + 1/2V_D
A1
1/4 LMC6484
10k,
0.1%
10k, 0.1%
A2
1/4 LMC6484
V_{OUT} = 100V_D
V_{CM} - 1/2V_D

TL/H/11714-30

FIGURE 16. Low-Power Two-Op-Amp Instrumentation Amplifier

Application Information (Continued)

11.0 Spice Macromodel

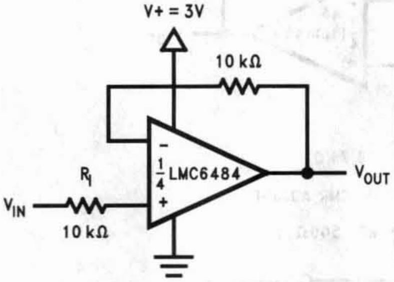
A spice macromodel is available for the LMC6484. This model includes accurate simulation of:

- input common-mode voltage range
- frequency and transient response
- GBW dependence on loading conditions
- quiescent and dynamic supply current
- output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

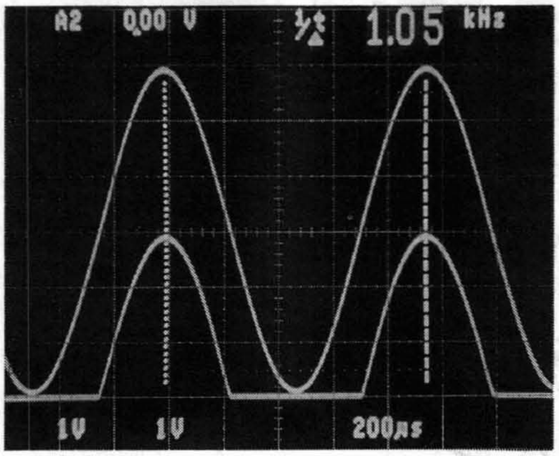
Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications



TL/H/11714–31

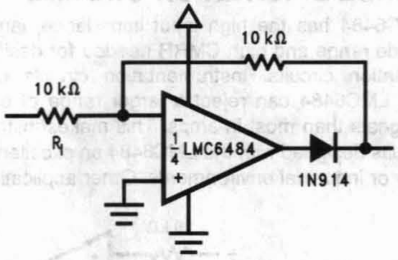
FIGURE 17. Half-Wave Rectifier with Input Current Protection (RI)



TL/H/11714–32

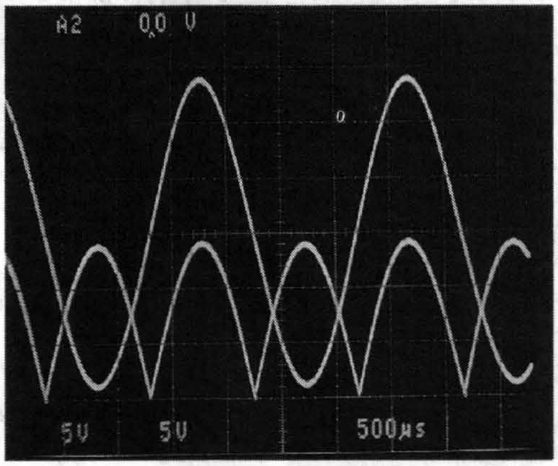
FIGURE 17a. Half-Wave Rectifier Waveform

The circuit in *Figure 17* uses a single supply to half wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in *Figure 18*.



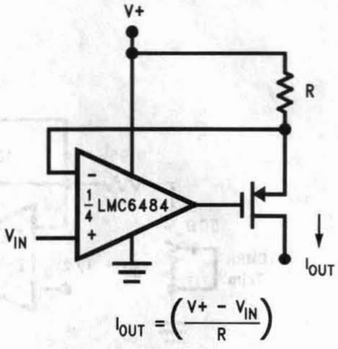
TL/H/11714–33

FIGURE 18. Full Wave Rectifier with Input Current Protection (R_I)



TL/H/11714–34

FIGURE 18a. Full Wave Rectifier Waveform



TL/H/11714–35

FIGURE 19. Large Compliance Range Current Source

Typical Single-Supply Applications (Continued)

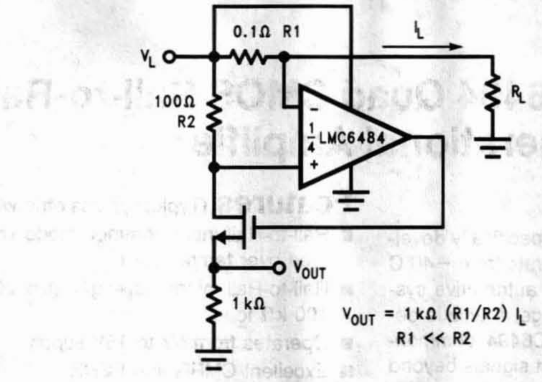

0.1Ω R1
I_L
V_L
100Ω
R2
R_L
$\frac{1}{4}$ LMC6484
V_{OUT}
1 kΩ
V_{OUT} = 1 kΩ (R1/R2) I_L
R1 << R2
TL/H/11714-36

FIGURE 20. Positive Supply Current Sense

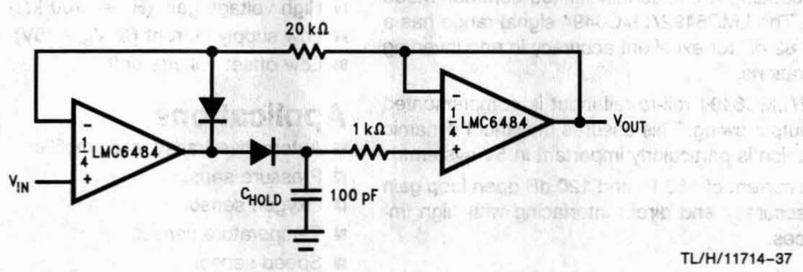

20 kΩ
$\frac{1}{4}$ LMC6484
$\frac{1}{4}$ LMC6484
1 kΩ
V_{OUT}
V_{IN}
C_{HOLD}
100 pF
TL/H/11714-37

FIGURE 21. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

In *Figure 21* dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6484 has a negligible effect on droop.

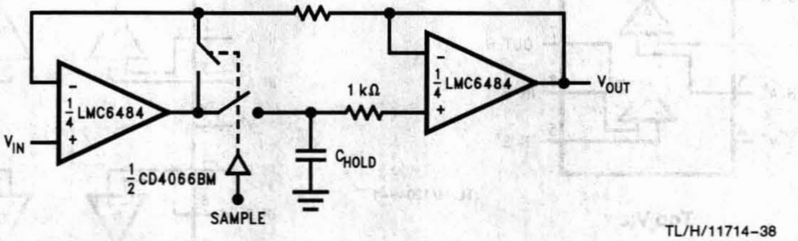
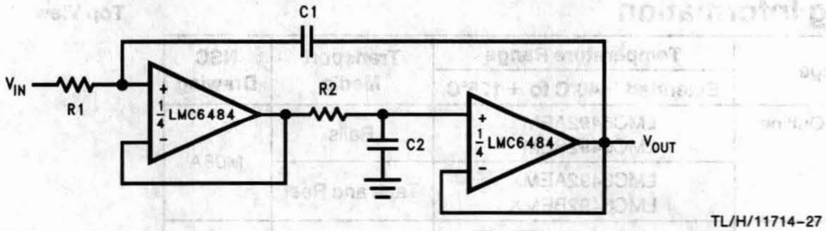

20 kΩ
$\frac{1}{4}$ LMC6484
$\frac{1}{4}$ LMC6484
1 kΩ
V_{OUT}
V_{IN}
$\frac{1}{2}$ CD4066BM
C_{HOLD}
SAMPLE
TL/H/11714-38

FIGURE 22. Rail-to-Rail Sample and Hold

The LMC6484's high CMRR (85 dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.


C1
V_{IN}
R1
$\frac{1}{4}$ LMC6484
R2
C2
$\frac{1}{4}$ LMC6484
V_{OUT}
TL/H/11714-27

$$R1 = R2, C1 = C2; f = \frac{1}{2\pi R1C1}; DF = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\sqrt{\frac{R_2}{R_1}}$$

FIGURE 23. Rail-to-Rail Single Supply Low Pass Filter

The low pass filter circuit in *Figure 23* can be used as an anti-aliasing filter with the same voltage supply as the A/D converter.

Filter designs can also take advantage of the LMC6484 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

National Semiconductor

LMC6492 Dual/LMC6494 Quad CMOS Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6492/LMC6494 amplifiers were specifically developed for single supply applications that operate from −40°C to +125°C. This feature is well-suited for automotive systems because of the wide temperature range. A unique design topology enables the LMC6492/LMC6494 common-mode voltage range to accommodate input signals beyond the rails. This eliminates non-linear output errors due to input signals exceeding a traditionally limited common-mode voltage range. The LMC6492/LMC6494 signal range has a high CMRR of 82 dB for excellent accuracy in non-inverting circuit configurations.

The LMC6492/LMC6494 rail-to-rail input is complemented by rail-to-rail output swing. This assures maximum dynamic signal range which is particularly important in 5V systems.

Ultra-low input current of 150 fA and 120 dB open loop gain provide high accuracy and direct interfacing with high impedance sources.

Features (Typical unless otherwise noted)

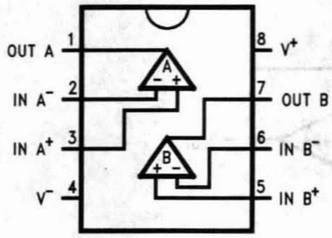
- Rail-to-Rail input common-mode voltage range, guaranteed over temperature
- Rail-to-Rail output swing within 20 mV of supply rail, 100 kΩ load
- Operates from 5V to 15V supply
- Excellent CMRR and PSRR 82 dB
- Ultra low input current 150 fA
- High voltage gain (R_L = 100 kΩ) 120 dB
- Low supply current (@ V_S = 5V) 500 μA/Amplifier
- Low offset voltage drift 1.0 μV/°C

Applications

- Automotive transducer amplifier
- Pressure sensor
- Oxygen sensor
- Temperature sensor
- Speed sensor

Connection Diagrams

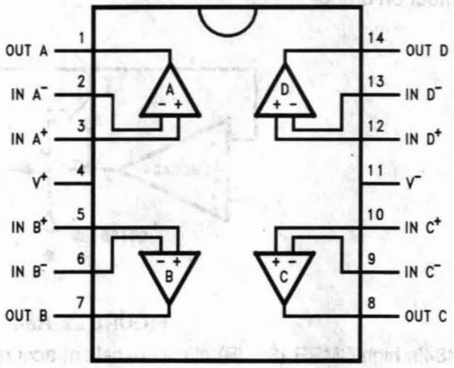
8-Pin DIP/SO



TL/H/12049–1

Top View

14-Pin DIP/SO



TL/H/12049–2

Top View

Ordering Information

Package	Temperature Range	Transport Media	NSC Drawing
	Extended −40°C to +125°C		
8-Pin Small Outline	LMC6492AEM LMC6492BEM	Rails	M08A
	LMC6492AEMX LMC6492BEMX	Tape and Reel	
8-Pin Molded DIP	LMC6492AEN LMC6492BEN	Rails	N08A
14-Pin Small Outline	LMC6494AEM LMC6494BEM	Rails	M14A
	LMC6494AEMX LMC6494BEMX	Tape and Reel	
14-Pin Molded DIP	LMC6494AEN LMC6494BEN	Rails	N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Conditions (Note 1)

Supply Voltage	$2.5V \le V^+ \le 15.5V$
Junction Temperature Range	
LMC6492AE, LMC6492BE	$-40°C \le T_J \le +125°C$
LMC6494AE, LMC6494BE	$-40°C \le T_J \le +125°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	108°C/W
M Package, 8-Pin Surface Mount	171°C/W
N Package, 14-Pin Molded DIP	78°C/W
M Package, 14-Pin Surface Mount	118°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6492AE LMC6494AE Limit (Note 6)	LMC6492BE LMC6494BE Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.11	3.0 **3.8**	6.0 **6.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0			μV/°C
I_B	Input Bias Current	(Note 11)	0.15	**200**	**200**	pA max
I_{OS}	Input Offset Current	(Note 11)	0.075	**100**	**100**	pA max
R_{IN}	Input Resistance		>10			Tera Ω
C_{IN}	Common-Mode Input Capacitance		3			pF
CMRR	Common-Mode Rejection Ratio	$0V \le V_{CM} \le 15V$ $V^+ = 15V$	82	65 **60**	63 **58**	dB min
		$0V \le V_{CM} \le 5V$	82	65 **60**	63 **58**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V_O = 2.5V$	82	65 **60**	63 **58**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$, $V_O = 2.5V$	82	65 **60**	63 **58**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB	$V^- - 0.3$	−0.25 **0**	−0.25 **0**	V max
			$V^+ + 0.3$	$V^+ + 0.25$ $\mathbf{V^+}$	$V^+ + 0.25$ $\mathbf{V^+}$	V min
A_V	Large Signal Voltage Gain	$R_L = 2\ k\Omega$ Sourcing (Note 7)	300			V/mV min
		Sinking	40			

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6492AE LMC6494AE Limit (Note 6)	LMC6492BE LMC6494BE Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.9	4.8 **4.7**	4.8 **4.7**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	V max
		V^+ = 5V R_L = 600Ω to $V^+/2$	4.7	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	V max
		V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.7	14.4 **14.0**	14.4 **14.0**	V min
			0.16	0.35 **0.5**	0.35 **0.5**	V max
		V^+ = 15V R_L = 600Ω to $V^+/2$	14.1	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.5**	1.0 **1.5**	V max
I_{SC}	Output Short Circuit Current V^+ = 5V	Sourcing, V_O = 0V	25	16 **10**	16 **10**	mA min
		Sinking, V_O = 5V	22	11 **8**	11 **8**	
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **20**	28 **20**	
		Sinking, V_O = 5V (Note 8)	30	30 **22**	30 **22**	
I_S	Supply Current	LMC6492 V^+ = +5V, V_O = $V^+/2$	1.0	1.75 **2.1**	1.75 **2.1**	mA max
		LMC6492 V^+ = +15V, V_O = $V^+/2$	1.3	1.95 **2.3**	1.95 **2.3**	mA max
		LMC6494 V^+ = +5V, V_O = $V^+/2$	2.0	3.5 **4.2**	3.5 **4.2**	mA max
		LMC6494 V^+ = +15V, V_O = $V^+/2$	2.6	3.9 **4.6**	3.9 **4.6**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6492AE LMC6494AE Limit (Note 6)	LMC6492BE LMC6494BE Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	1.3	0.7 **0.5**	0.7 **0.5**	V/μs min
GBW	Gain-Bandwidth Product	$V^+ = 15V$	1.5			MHz
ϕ_m	Phase Margin		50			Deg
G_m	Gain Margin		15			dB
	Amp-to-Amp Isolation	(Note 10)	150			dB
e_n	Input-Referred Voltage Noise	$F = 1\ kHz$ $V_{CM} = 1V$	37			$\frac{nV}{\sqrt{HZ}}$
i_n	Input-Referred Current Noise	$F = 1\ kHz$	0.06			$\frac{pA}{\sqrt{HZ}}$
T.H.D.	Total Harmonic Distortion	$F = 1\ kHz, A_V = -2$ $R_L = 10\ k\Omega, V_O = -4.1\ V_{PP}$	0.01			%
		$F = 10\ kHz, A_V = -2$ $R_L = 10\ k\Omega, V_O = 8.5\ V_{PP}$ $V^+ = 10V$	0.01			

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $3.5V \leq V_O \leq 7.5V$.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15V$. Connected as voltage follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

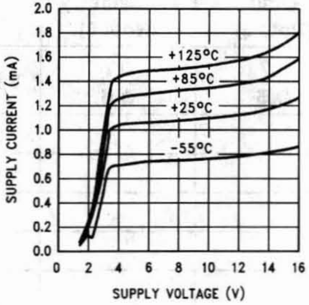
Note 10: Input referred, $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\ V_{PP}$.

Note 11: Guaranteed limits are dictated by tester limits and not device performance. Actual performance is reflected in the typical value.

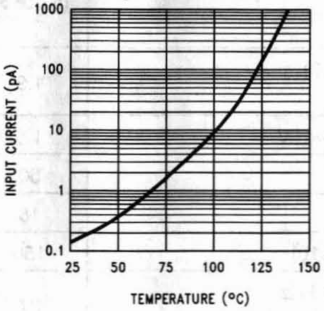
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25°C$ unless otherwise specified

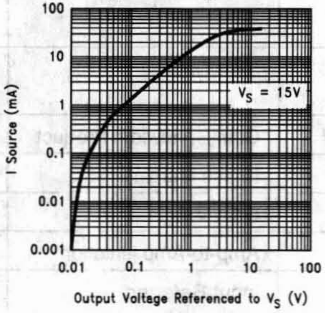
Supply Current vs Supply Voltage



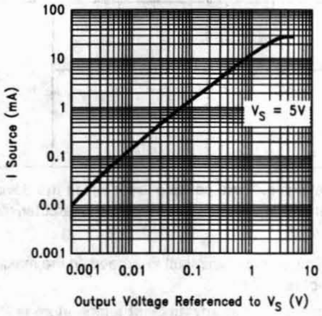
Input Current vs Temperature



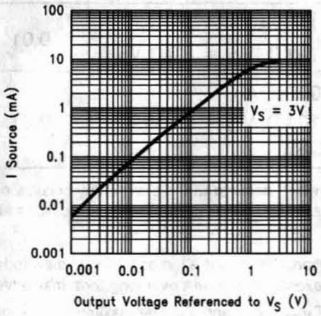
Sourcing Current vs Output Voltage



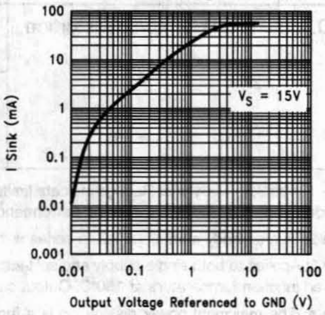
Sourcing Current vs Output Voltage



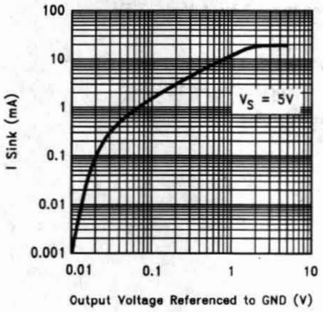
Sourcing Current vs Output Voltage



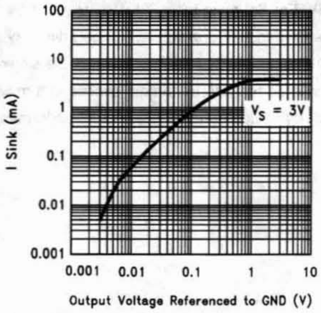
Sinking Current vs Output Voltage



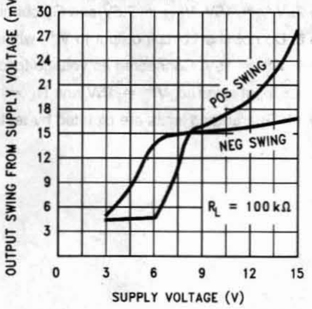
Sinking Current vs Output Voltage



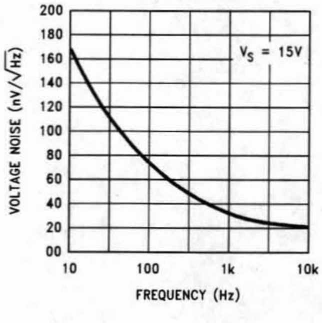
Sinking Current vs Output Voltage



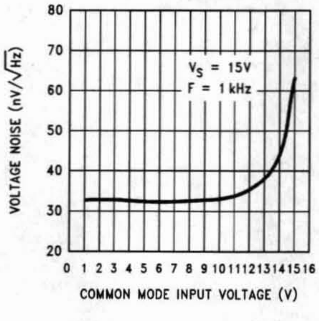
Output Voltage Swing vs Supply Voltage



Input Voltage Noise vs Frequency



Input Voltage Noise vs Input Voltage



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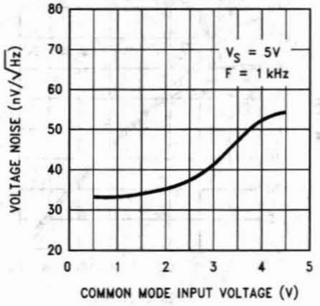
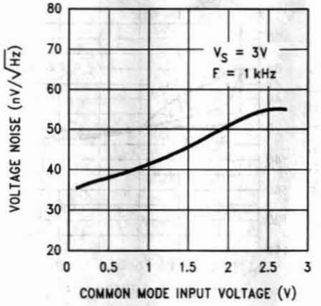
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25°C$ unless otherwise specified (Continued)

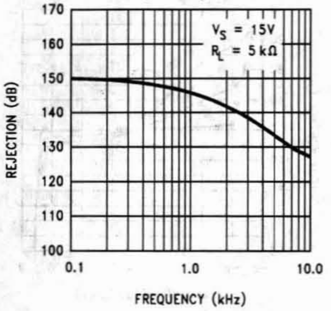
Input Voltage Noise vs Input Voltage



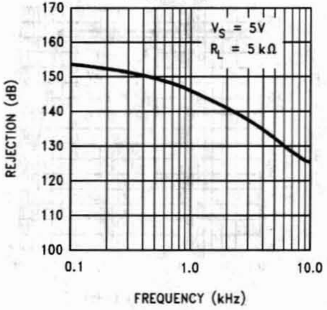
Input Voltage Noise vs Input Voltage



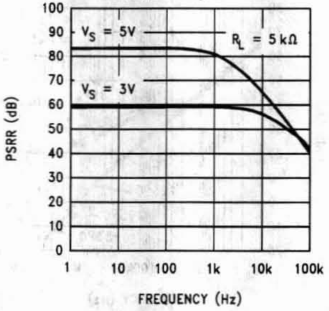
Crosstalk Rejection vs Frequency



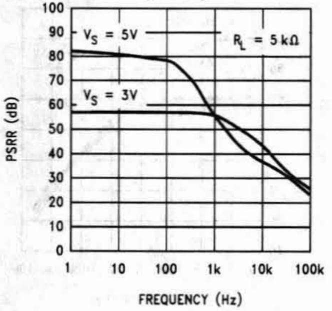
Crosstalk Rejection vs Frequency



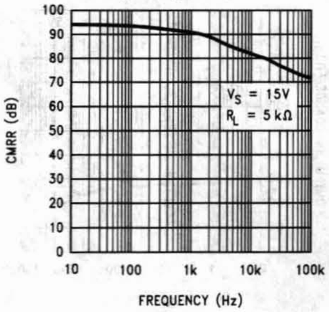
Positive PSRR vs Frequency



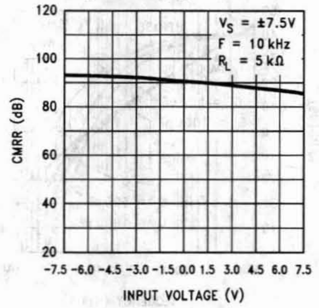
Negative PSRR vs Frequency



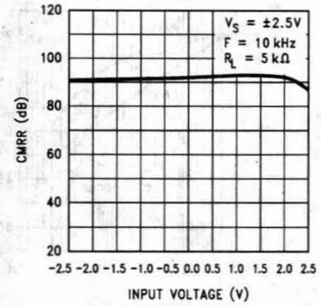
CMRR vs Frequency



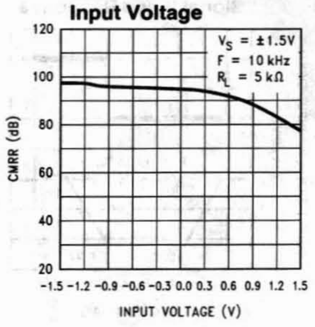
CMRR vs Input Voltage



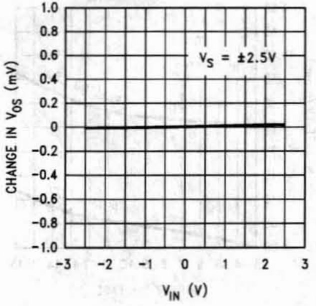
CMRR vs Input Voltage



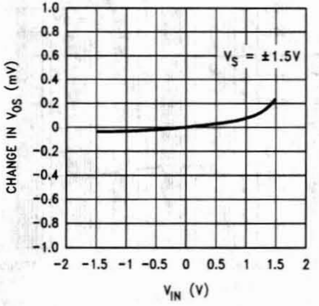
CMRR vs Input Voltage



ΔV_{OS} vs CMR



ΔV_{OS} vs CMR

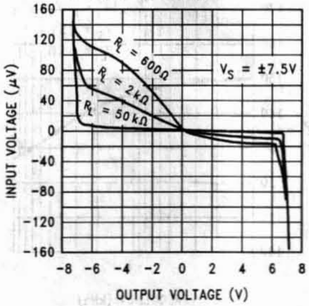


TL/H/12049-4

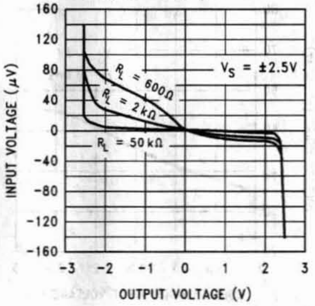
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

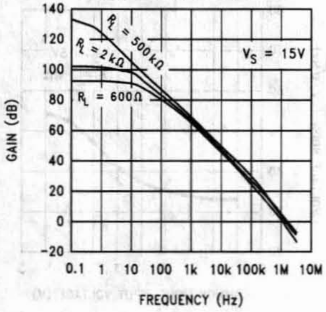
Input Voltage vs Output Voltage



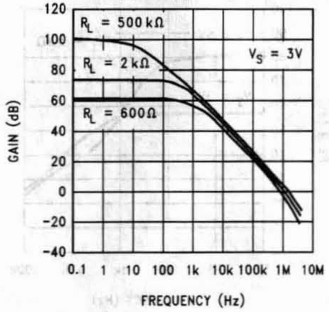
Input Voltage vs Output Voltage



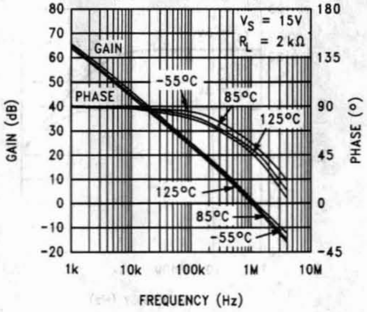
Open Loop Frequency Response



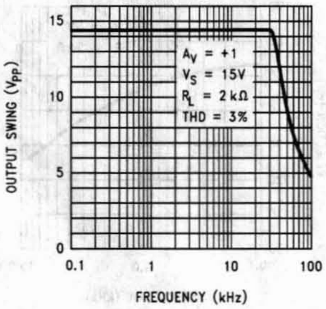
Open Loop Frequency Response



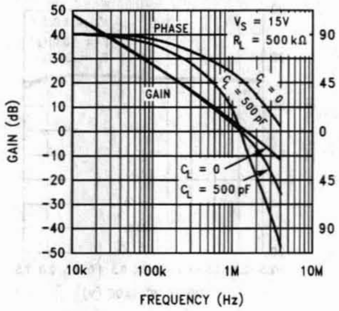
Open Loop Frequency Response vs Temperature



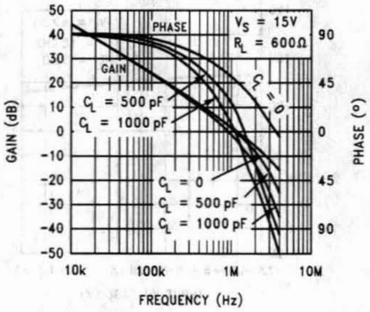
Maximum Output Swing vs Frequency



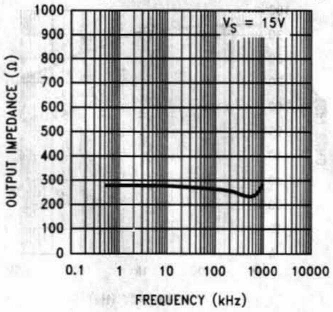
Gain and Phase vs Capacitive Load



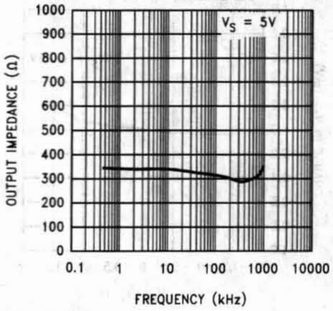
Gain and Phase vs Capacitive Load



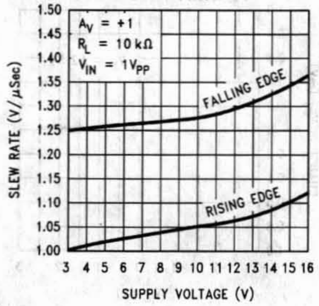
Open Loop Output Impedance vs Frequency



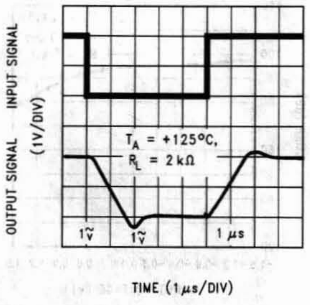
Open Loop Output Impedance vs Frequency



Slew Rate vs Supply Voltage



Non-Inverting Large Signal Pulse Response

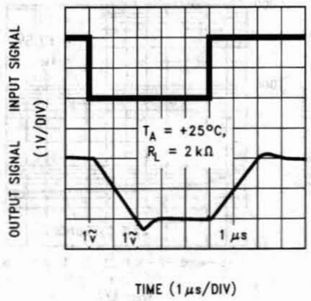


TL/H/12049–5

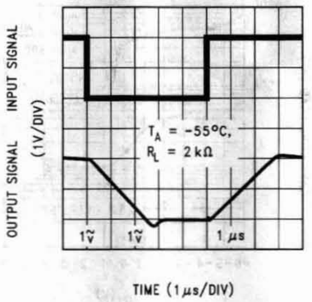
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

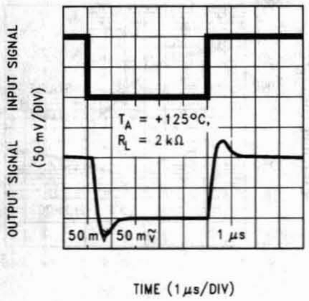
Non-Inverting Large Signal Pulse Response



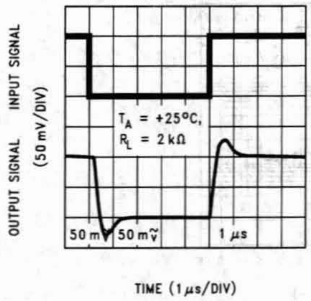
Non-Inverting Large Signal Pulse Response



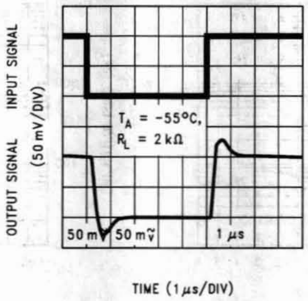
Non-Inverting Small Signal Pulse Response



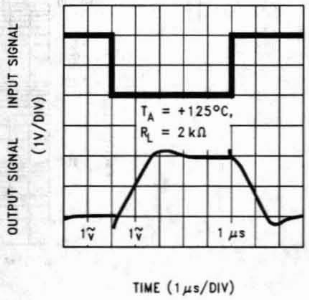
Non-Inverting Small Signal Pulse Response



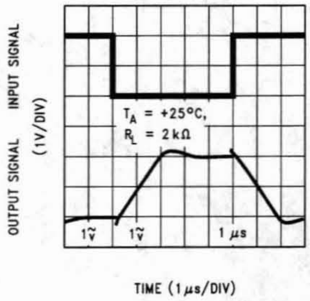
Non-Inverting Small Signal Pulse Response



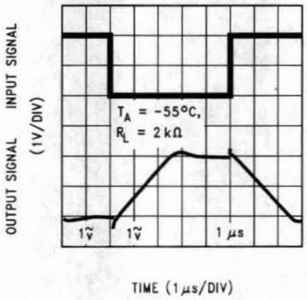
Inverting Large Signal Pulse Response



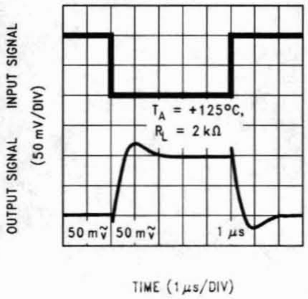
Inverting Large Signal Pulse Response



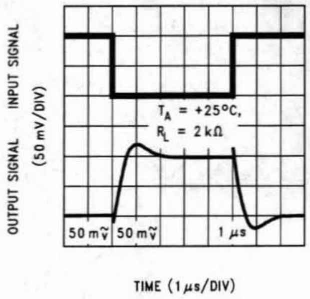
Inverting Large Signal Pulse Response



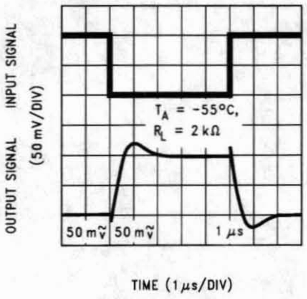
Inverting Small Signal Pulse Response



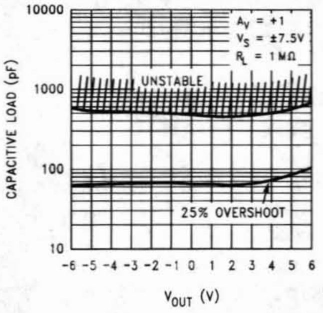
Inverting Small Signal Pulse Response



Inverting Small Signal Pulse Response



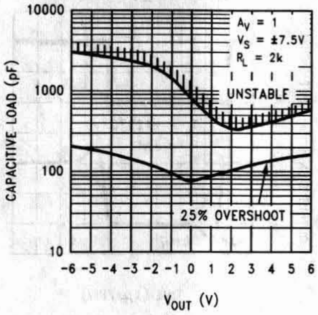
Stability vs Capacitive Load



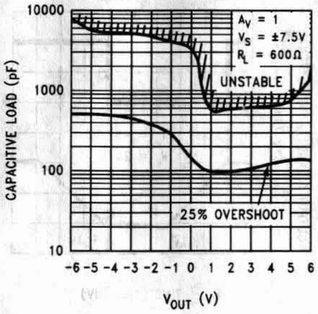
TL/H/12049-6

Typical Performance Characteristics

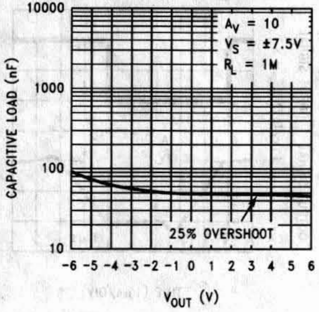
V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)



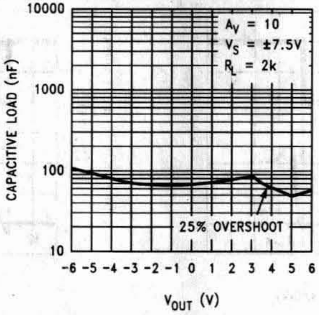
Stability vs Capacitive Load



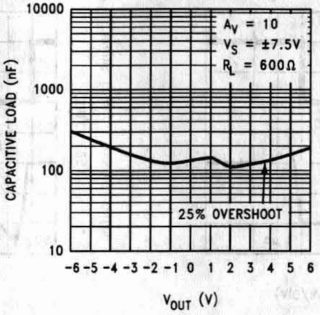
Stability vs Capacitive Load



Stability vs Capacitive Load



Stability vs Capacitive Load



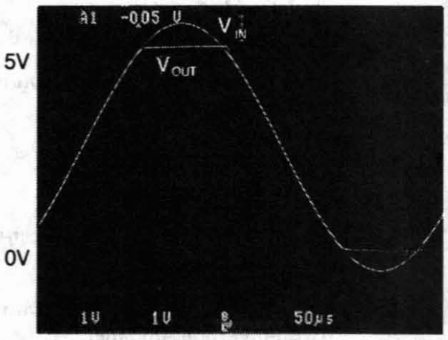
Stability vs Capacitive Load

TL/H/12049-7

Application Notes

Input Common-Mode Voltage Range

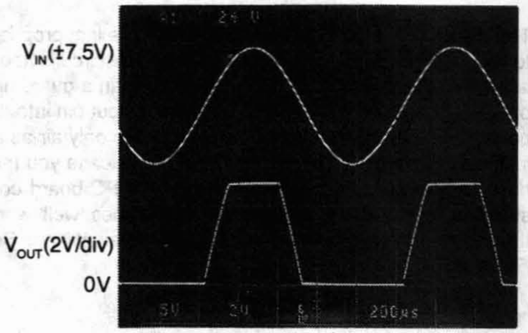
Unlike Bi-FET amplifier designs, the LMC6492/4 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion on the output.



TL/H/12049–8

FIGURE 1. An Input Voltage Signal Exceeds the LMC6492/4 Power Supply Voltages with No Output Phase Inversion

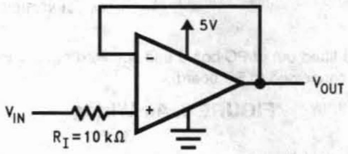
The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins possibly affecting reliability.



TL/H/12049–9

FIGURE 2. A ±7.5V Input Signal Greatly Exceeds the 5V Supply in *Figure 3* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor (R_I) as shown in *Figure 3*.



TL/H/12049–10

FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

Rail-To-Rail Output

The approximate output resistance of the LMC6492/4 is 110Ω sourcing and 80Ω sinking at $V_S = 5V$. Using the calculated output resistance, maximum output voltage swing can be esitmated as a function of load.

Compensating for Input Capacitance

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6492/4.

Although the LMC6492/4 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors with even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6492/4 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

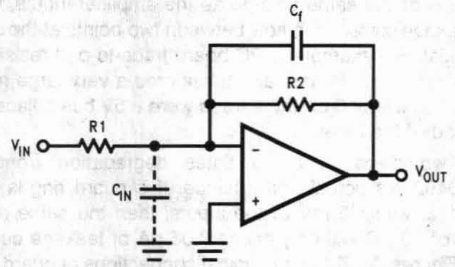
The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.



TL/H/12049–11

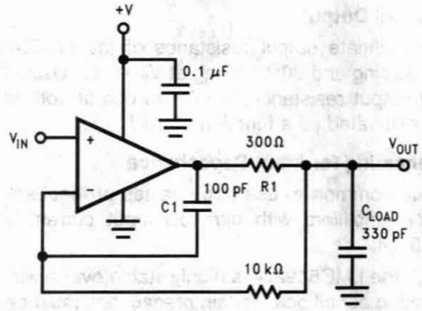
FIGURE 4. Cancelling the Effect of Input Capacitance

Capacitive Load Tolerance

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see Typical Curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 5*.

Application Notes (Continued)



TL/H/12049–12

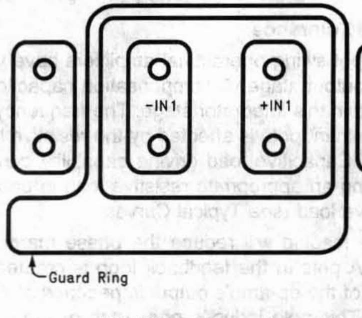
FIGURE 5. LMC6492/4 Noninverting Amplifier, Compensated to Handle Capacitive Loads

Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6492/4, typically 150 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

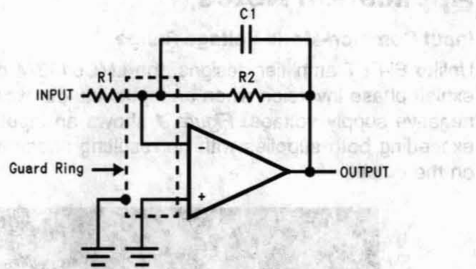
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6492/4's inputs and the terminals of components connected to the op-amp's inputs, as in *Figure 6*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input.

This would cause a 33 times degradation from the LMC6492/4's actual performance. If a guard ring is used and held within 5 mV of the inputs, then the same resistance of $10^{11}\Omega$ will only cause 0.05 pA of leakage current. See *Figures 7a, 7b, 7c* for typical connections of guard rings for standard op-amp configurations.



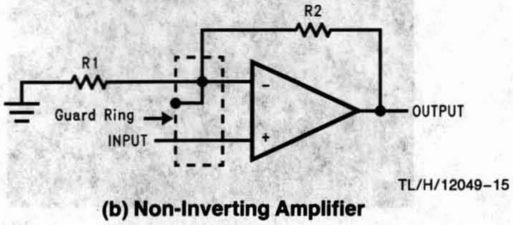
TL/H/12049–13

FIGURE 6. Examples of Guard Ring in PC Board Layout



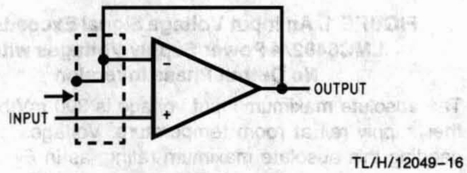
TL/H/12049–14

(a) Inverting Amplifier



TL/H/12049–15

(b) Non-Inverting Amplifier

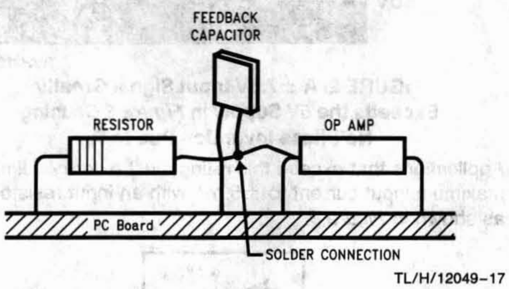


TL/H/12049–16

(c) Follower

FIGURE 7.Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 8*.



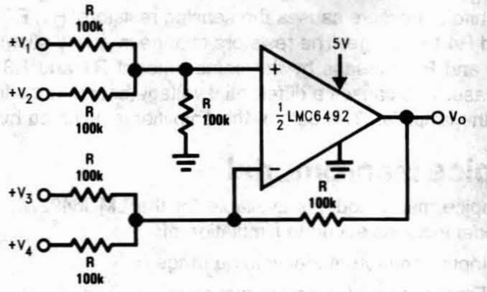
TL/H/12049–17

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 8. Air Wiring

Application Circuits

DC Summing Amplifier
($V_{IN} \geq 0V_{DC}$ and $V_O \geq V_{DC}$)


R 100k
+V1
+V2
R 100k
R 100k
5V
+
1/2 LMC6492
Vo
+V3
R 100k
R 100k
+V4
R 100k

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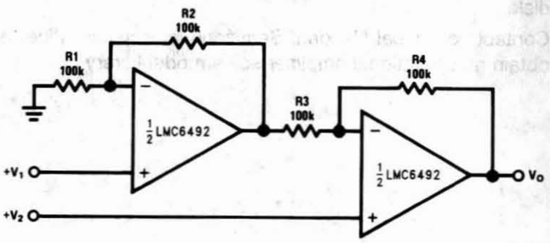
Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2 \geq (V_3 + V_4)$ to keep $V_O > 0V_{DC}$

High Input Z, DC Differential Amplifier


R2 100k
R1 100k
R4 100k
R3 100k
1/2 LMC6492
1/2 LMC6492
+V1
+V2
Vo

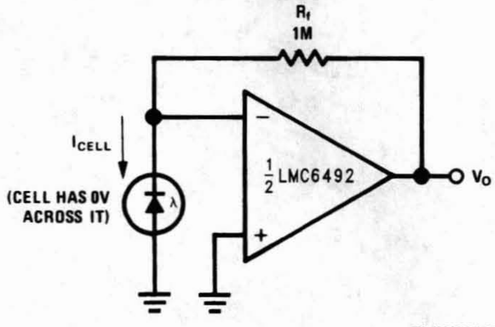
TL/H/12049-19

For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

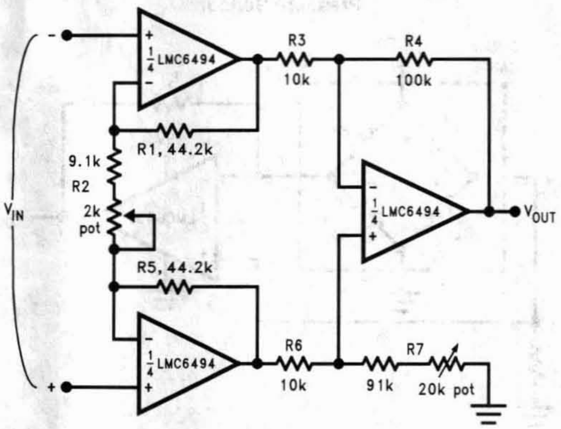
As shown: $V_O = 2(V_2 - V_1)$

Photo Voltaic-Cell Amplifier


Rf
1M
ICELL
(CELL HAS 0V ACROSS IT)
λ
1/2 LMC6492
Vo

TL/H/12049-20

Instrumentation Amplifier


1/4 LMC6494
R3 10k
R4 100k
R1, 44.2k
9.1k
R2
2k pot
VIN
1/4 LMC6494
VOUT
R5, 44.2k
R6 10k
R7
91k
20k pot
1/4 LMC6494

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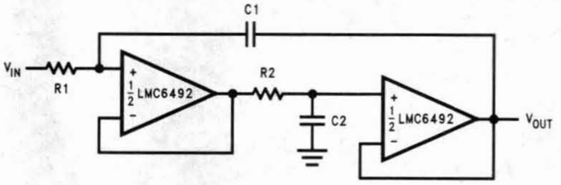
If R1 = R5, R3 = R6, and R4 = R7; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.3k$).

Rail-to-Rail Single Supply Low Pass Filter

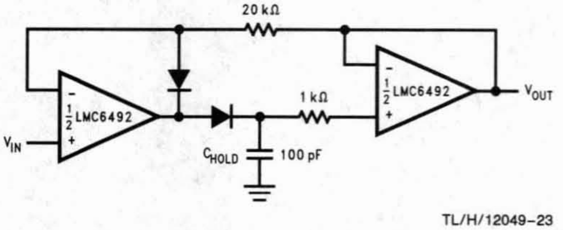

C1
VIN
R1
R2
1/2 LMC6492
C2
1/2 LMC6492
VOUT

TL/H/12049-22

R1 = R2, C1 = C2; $f = \frac{1}{2\pi R1C1}$; Damping Factor $= \frac{1}{2}\sqrt{\frac{C2}{C1}}\sqrt{\frac{R2}{R1}}$

This low-pass filter circuit can be used as an anti-aliasing filter with the same supply as the A/D converter. Filter designs can also take advantage of the LMC6492/4 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

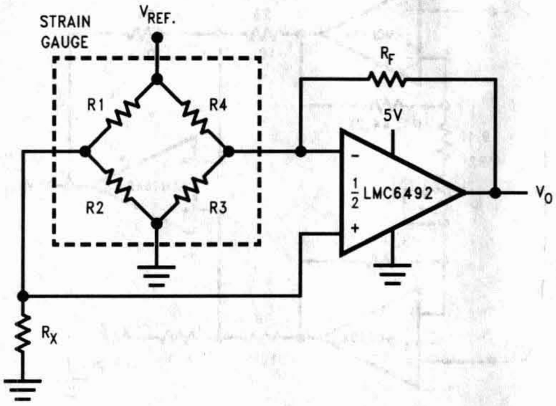

20 kΩ
1 kΩ
1/2 LMC6492
VOUT
1/2 LMC6492
VIN
CHOLD
100 pF

TL/H/12049-23

Dielectric absorption and leakage is minimized by using a polystyrene or polypropylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. Select low-leakage current diodes to minimize drooping.

Application Circuits (Continued)

Pressure Sensor



TL/H/12049-24

$R_f = R_X$

$R_f >> R1, R2, R3, \text{and } R4$

$$V_O = \left(\frac{R2}{R1 + R2} - \frac{R3}{R4 + R3}\right)\frac{R_f\,(R3 + R4)}{R3\,R4}V_{REF}$$

In a manifold absolute pressure sensor application, a strain gauge is mounted on the intake manifold in the engine unit. Manifold pressure causes the sensing resistors, R1, R2, R3 and R4 to change. The resistors change in a way such that R2 and R4 increase by the same amount R1 and R3 decrease. This causes a differential voltage between the input of the amplifier. The gain of the amplifier is adjusted by R_f.

Spice Macromodel

A spice macromodel is available for the LMC6492/4. This model includes accurate simulation of:

- Input common-model voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many other characteristics as listed on the macromodel disk.

Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

National Semiconductor

LMC6574 Quad/LMC6572 Dual Low Voltage (2.7V and 3V) Operational Amplifier

General Description

Low voltage operation and low power dissipation make the LMC6574/2 ideal for battery-powered systems.

3V amplifier performance is backed by 2.7V guarantees to ensure operation throughout battery lifetime. These guarantees also enable analog circuits to operate from the same 3.3V supply used for digital logic.

Battery life is maximized because each amplifier dissipates only micro-watts of power.

The LMC6574/2 does not sacrifice functionality for low voltage operation. The LMC6574/2 generates 120 dB of open-loop gain just like a conventional amplifier, but the LMC6574/2 can do this from a 2.7V supply.

These amplifiers are designed with features that optimize low voltage operation. The output voltage swings rail-to-rail to maximize signal-to-noise ratio and dynamic signal range. The common-mode input voltage range extends from 800 mV below the positive supply to 100 mV below ground.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

Features (Typical unless otherwise noted)

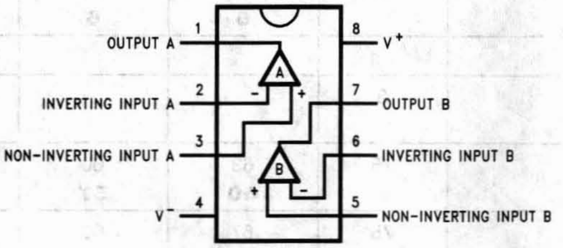
- Guaranteed 2.7V and 3V Performance
- Rail-to-Rail Output Swing (within 5 mV of supply rail, 100 kΩ load)
- Ultra-Low Supply Current 40 μA/Amplifier
- Low Cost
- Ultra-Low Input Current 20 fA
- High Voltage Gain @ $V_S = 2.7V$, $R_L = 100$ kΩ 120 dB
- Specified for 100 kΩ and 5 kΩ loads

Applications

- Transducer Amplifier
- Portable or Remote Equipment
- Battery-Operated Instruments
- Data Acquisition Systems
- Medical Instrumentation
- Improved Replacement for TLV2322 and TLV2324

Connection Diagrams

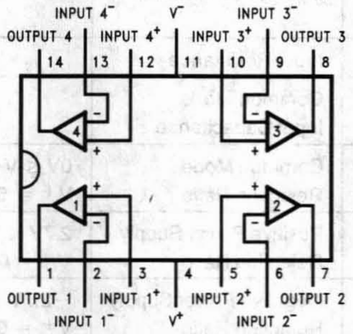
8-Pin DIP/SO



TL/H/11934-1

Order Number LMC6572AIN, LMC6572BIN, LMC6572AIM or LMC6572BIM
See NS Package Number N08E or M08A

14-Pin DIP/SO



TL/H/11934-2

Order Number LMC6574AIN, LMC6574BIN, LMC6574AIM or LMC6574BIM
See NS Package Number N14A or M14A

Ordering Information

Package	Temperature Range Industrial, −40°C to +85°C	NSC Drawing	Transport Media
8-Pin Molded DIP	LMC6572AIN, LMC6572BIN	N08E	Rail
8-Pin Small Outline	LMC6572AIM, LMC6572BIM	M08A	Rail
	LMC6572AIMX, LMC6572BIMX		Tape and Reel
14-Pin Molded DIP	LMC6574AIN, LMC6574BIN	N14A	Rail
14-Pin Small Outline	LMC6574AIM, LMC6574BIM	M14A	Rail
	LMC6574AIMX, LMC6574BIMX		Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	12V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±10 mA
Current at Power Supply Pin	35 mA
Lead Temperature (Soldering, 10 Seconds)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.7V \leq V^+ \leq 11V$
Junction Temperature Range	
LMC6572AI, LMC6572BI	$-40°C \leq T_J \leq +85°C$
LMC6574AI, LMC6574BI	$-40°C \leq T_J \leq +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
N Package, 14-Pin Molded DIP	81°C/W
M Package, 14-Pin Surface Mount	126°C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 2.7V$ and 3V	0.5	3 **3.5**	7 **7.5**	mV Max
TCV_{OS}	Input Offset Voltage Average Drift		1.5			μV/°C
I_B	Input Current		0.02	 **10**	 **10**	pA Max
I_{OS}	Input Offset Current		0.01	 **6**	 **6**	pA Max
R_{IN}	Input Resistance		>1			Tera Ω
C_{IN}	Common-Mode Input Capacitance		3			pF
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 3.5V$ $V^+ = 5V$	75	63 **60**	60 **57**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$2.7V \leq V^+ \leq 5V$, $V^- = 0V$	75	67 **65**	60 **58**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$-2.7V \leq V^- \leq -5V$, $V^+ = 0V$	83	75 **73**	67 **65**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 2.7V$ and 3V for CMRR ≥ 50 dB	−0.1	−0.05 **0**	−0.05 **0**	V Max
			$V^+ - 0.8$	$V^+ - 1.0$ **$V^+ - 1.3$**	$V^+ - 1.0$ **$V^+ - 1.3$**	V Min
A_V	Large Signal Voltage Gain	$R_L = 100\ k\Omega$ (Note 7) Sourcing	1000			V/mV
		Sinking	500			V/mV

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
V_O	Output Swing	$V^+ = 2.7V$ $R_L = 100\ k\Omega$ to $V^+/2$	2.695	2.68 **2.66**	2.65 **2.62**	V Min
			0.005	0.03 **0.05**	0.06 **0.09**	V Max
		$V^+ = 2.7V$ $R_L = 5\ k\Omega$ to $V^+/2$	2.66	2.55 **2.45**	2.45 **2.35**	V Min
			0.04	0.15 **0.25**	0.25 **0.35**	V Max
		$V^+ = 3V$ $R_L = 100\ k\Omega$ to $V^+/2$	2.995	2.98 **2.96**	2.95 **2.93**	V Min
			0.005	0.03 **0.05**	0.06 **0.09**	V Max
		$V^+ = 3V$ $R_L = 5\ k\Omega$ to $V^+/2$	2.96	2.85 **2.75**	2.75 **2.65**	V Min
			0.04	0.15 **0.25**	0.25 **0.35**	V Max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0V$	6.0	4.0 **3.0**	3.0 **2.0**	mA Min
		Sinking, $V_O = 2.7V$	4.0	3.0 **2.0**	2.5 **1.5**	mA Min
I_S	Supply Current	Quad Package $V^+ = +2.7V$, $V_O = V^+/2$	160	240 **280**	240 **280**	μA Max
		Quad Package $V^+ = +3V$, $V_O = V^+/2$	160	240 **280**	240 **280**	μA Max
		Dual Package $V^+ = +2.7V$, $V_O = V^+/2$	80	120 **140**	120 **140**	μA Max
		Dual Package $V^+ = +3V$, $V_O = V^+/2$	80	120 **140**	120 **140**	μA Max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
SR	Slew Rate	$V^+ = 2.7V$ and 3V (Note 8)	90	30 **10**	30 **10**	V/ms Min
GBW	Gain-Bandwidth Product	$V^+ = 3V$	0.22			MHz
ϕ_m	Phase Margin		60			Deg
G_m	Gain Margin		12			dB
	Amp-to-Amp Isolation	(Note 9)	120			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz $V_{CM} = 1V$	45			$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.002			$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 10 kHz, $A_V = -2$ $R_L = 10\ k\Omega$, $V_O = 1.0\ V_{PP}$	0.05			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

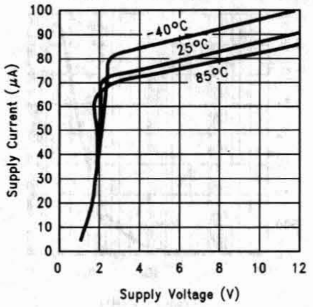
Note 7: $V^+ = 3V$, $V_{CM} = 1.5V$ and R_L connected to 1.5V. For Sourcing tests, $1.5V \le V_O \le 2.5V$. For Sinking tests, $0.5V \le V_O \le 1.5V$.

Note 8: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates.

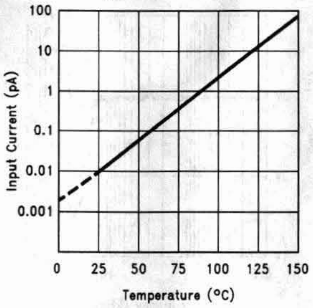
Note 9: Input referred, $V^+ = 3V$ and $R_L = 100\ k\Omega$ connected to 1.5V. Each amp excited in turn with 1 KHz to produce $V_O = 2\ V_{PP}$.

Typical Performance Characteristics $V_S = +3V$, $T_A = 25°C$, Unless otherwise specified

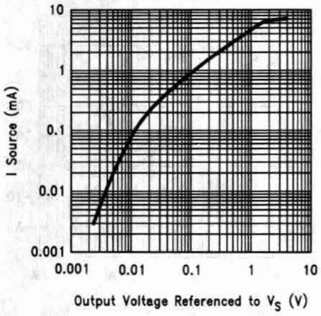
Supply Current vs Supply Voltage (Dual Package)



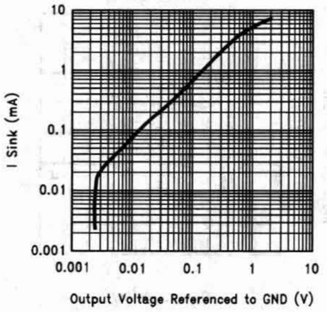
Input Current vs Temperature



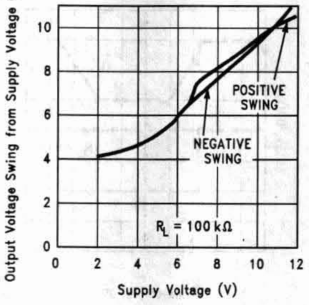
Sourcing Current vs Output Voltage



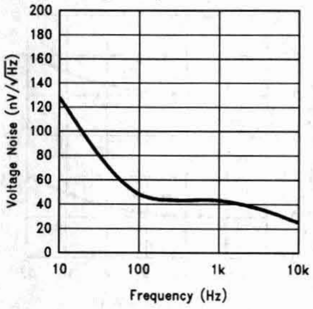
Sinking Current vs Output Voltage



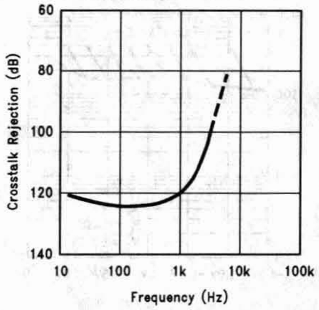
Output Voltage Swing vs Supply Voltage



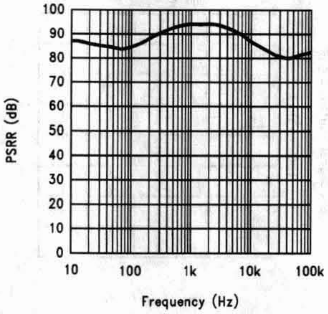
Input Voltage Noise vs Frequency



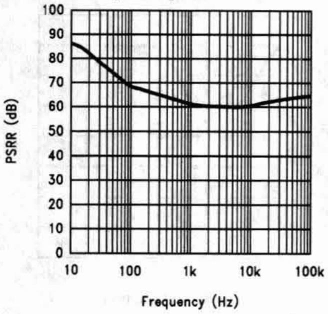
Crosstalk Rejection vs Frequency



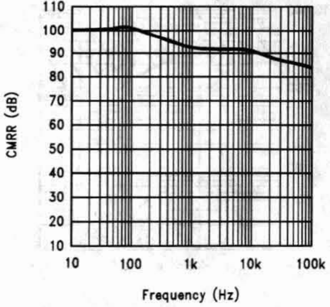
Positive PSRR vs Frequency



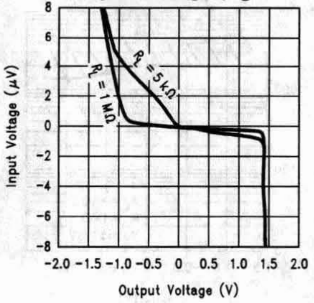
Negative PSRR vs Frequency



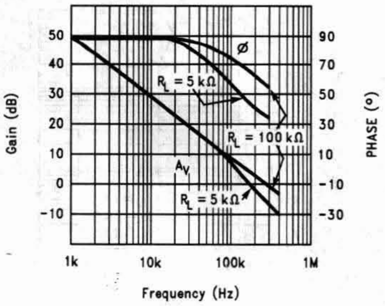
CMRR vs Frequency



Input Voltage vs Output Voltage ($V_S = \pm1.5$)



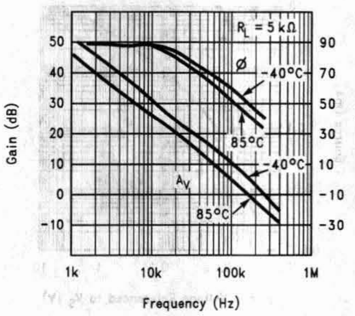
Open Loop Frequency Response



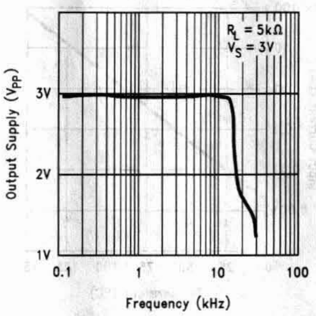
TL/H/11934-3

Typical Performance Characteristics (Continued) $V_S = +3V$, $T_A = 25°C$, Unless otherwise specified

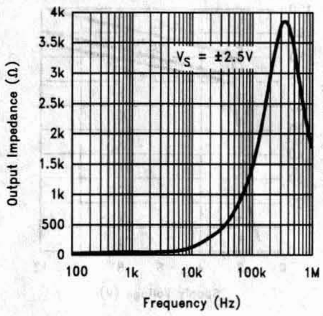
Open Loop Frequency Response vs Temperature



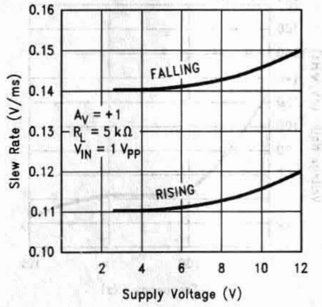
Maximum Output Swing vs Frequency



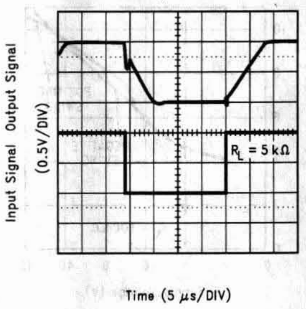
Z_{OUT} vs Frequency



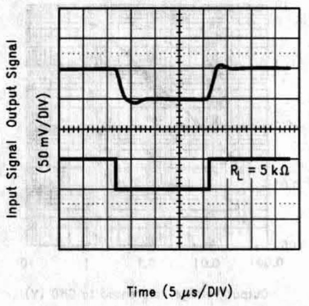
Slew Rate vs Supply Voltage



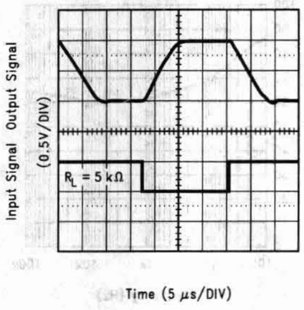
Non-Inverting Large Signal Pulse Response



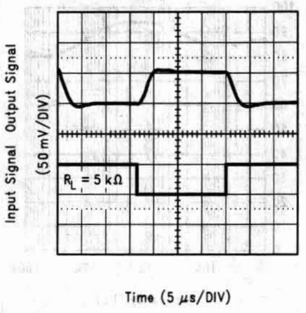
Non-Inverting Small Signal Pulse Response



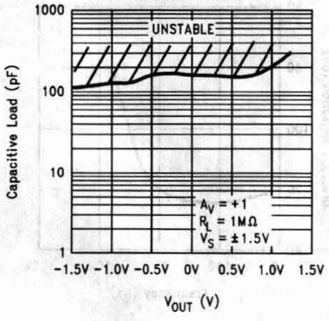
Inverting Large Signal Pulse Response



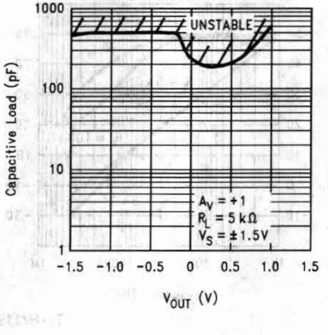
Inverting Small Signal Pulse Response



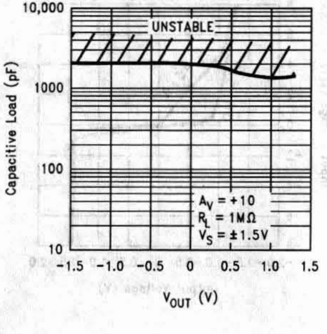
Stability vs Capacitive Load



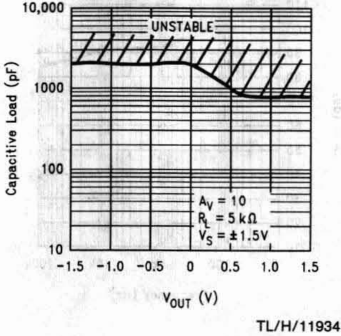
Stability vs Capacitive Load



Stability vs Capacitive Load



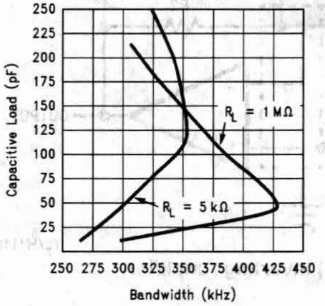
Stability vs Capacitive Load



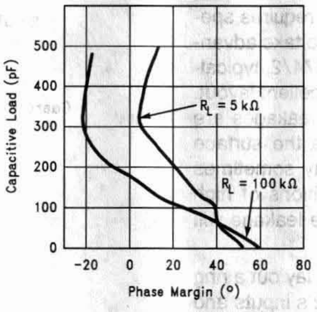
TL/H/11934–4

Typical Performance Characteristics (Continued) $V_S = +3V$, $T_A = 25°C$, Unless otherwise specified

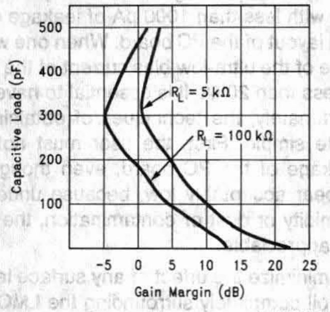
Bandwidth vs Capacitive Load



Capacitive Load vs Phase Margin



Capacitive Load vs Gain Margin



TL/H/11934-5

Applications Hints

1.0 LOW VOLTAGE AMPLIFIER TOPOLOGY

The LMC6574/2 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6574/2 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

2.0 COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6574/2.

Although the LMC6574/2 is highly stable over a wide range of operating conditions, a large feedback resistor will react even with small values of capacitance at the input of the op-amp to reduce phase margin. The capacitance at the input of the op-amp comes from transducers, photodiodes and circuit board parasitics.

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in *Figure 1*) such that:

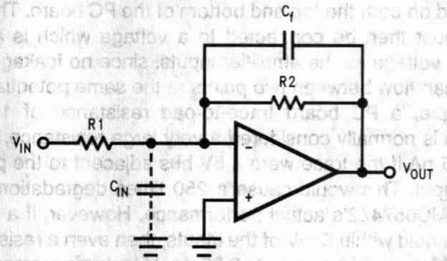
$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1\, C_{IN} \leq R_2\, C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

When high input impedances are demanded, guarding of the LMC6574/2 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work).*

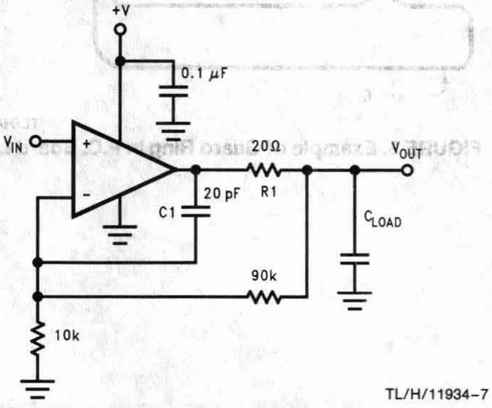


TL/H/11934-6

FIGURE 1. Cancelling the Effect of Input Capacitance

3.0 CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2*.



TL/H/11934-7

FIGURE 2. LMC6574/2 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

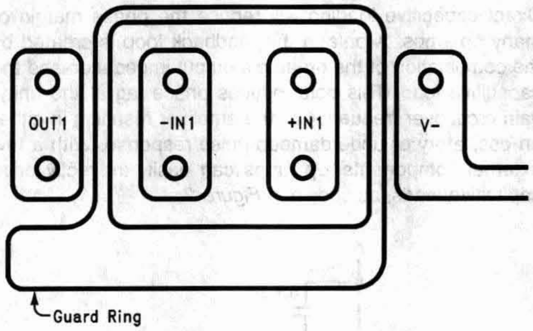
In the circuit of *Figure 2*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Applications Hints (Continued)

4.0 PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

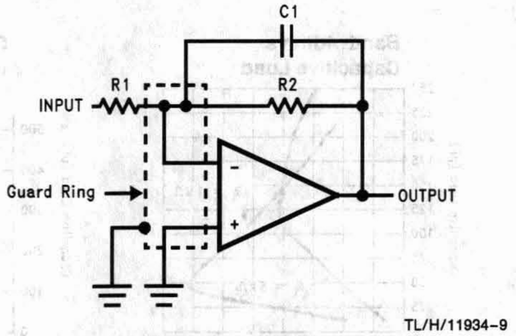
It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6574/2, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6574/2's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6574/2's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.



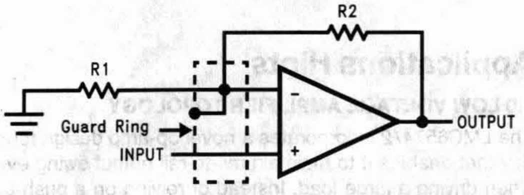
TL/H/11934-8

FIGURE 3. Example of Guard Ring in P.C. Board Layout



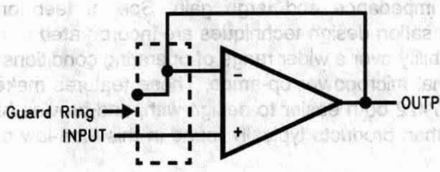
TL/H/11934-9

(a) Inverting Amplifier



TL/H/11934-10

(b) Non-Inverting Amplifier

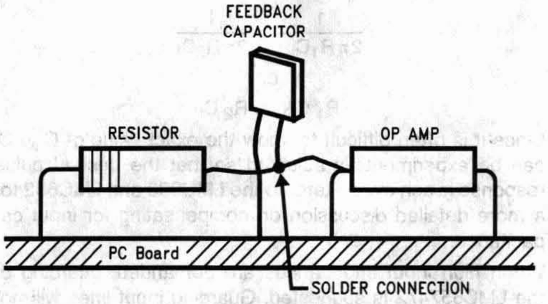


TL/H/11934-11

(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



TL/H/11934-12

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring

Applications Hints (Continued)

5.0 SPICE MACROMODEL

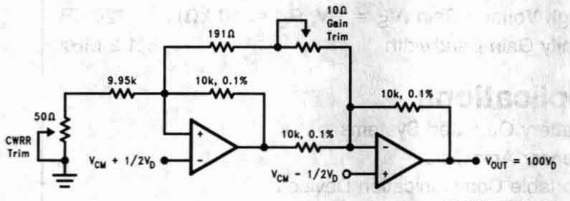
A spice macromodel is available for the LMC6574/2. This model includes accurate simulation of:

- input common-mode voltage range
- frequency and transient response
- GBW dependence on loading conditions
- quiescent and dynamic supply current
- output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

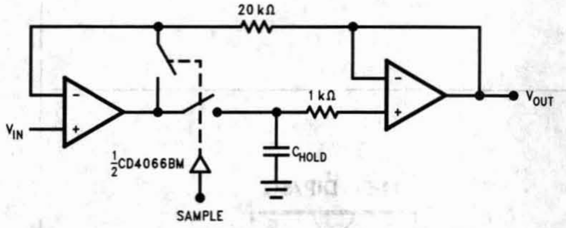
Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications


10Ω
Gain
Trim
191Ω
9.95k
10k, 0.1%
10k, 0.1%
10k, 0.1%
50Ω
CWRR
Trim
$V_{CM} + 1/2V_D$
$V_{CM} - 1/2V_D$
$V_{OUT} = 100V_D$

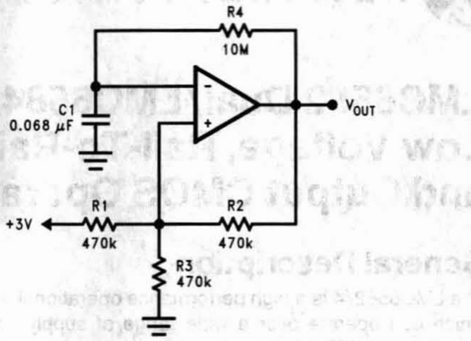
TL/H/11934–13

FIGURE 6. Low-Power Two-Op-Amp Instrumentation Amplifier


20 kΩ
1 kΩ
V_{IN}
V_{OUT}
$\frac{1}{2}$CD4066BM
C_{HOLD}
SAMPLE

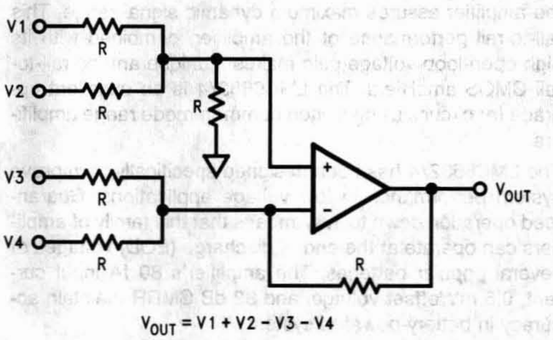
TL/H/11934–14

FIGURE 7. Sample and Hold


R4
10M
C1
0.068 µF
V_{OUT}
+3V
R1
470k
R2
470k
R3
470k

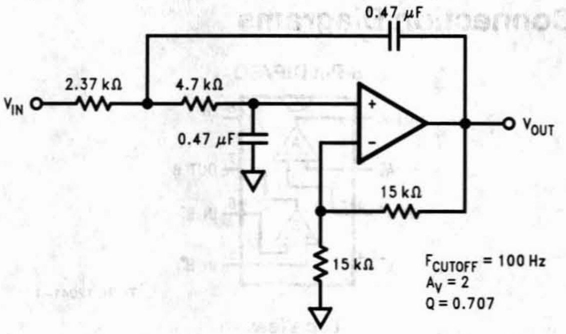
TL/H/11934–15

FIGURE 8. 1 Hz Square Wave Oscillator


V1
V2
V3
V4
R
R
R
R
R
R
V_{OUT}
$V_{OUT} = V1 + V2 - V3 - V4$

TL/H/11934–16

FIGURE 9. Adder/Subtractor Circuit


0.47 µF
2.37 kΩ
4.7 kΩ
V_{IN}
V_{OUT}
0.47 µF
15 kΩ
15 kΩ
$F_{CUTOFF} = 100$ Hz
$A_V = 2$
Q = 0.707

TL/H/11934–17

FIGURE 10. Low Pass Filter

National Semiconductor

PRELIMINARY

LMC6582 Dual/LMC6584 Quad Low Voltage, Rail-To-Rail Input and Output CMOS Operational Amplifier

General Description

The LMC6582/4 is a high performance operational amplifier which can operate over a wide range of supply voltages, from 1.8V to 10V. It has guaranteed specs at 1.8V, 2.2V, 3V, 5V, and 10V.

The LMC6582/4 provides an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifier assures maximum dynamic signal range. This rail-to-rail performance of the amplifier, combined with its high open-loop voltage gain makes it unique among rail-to-rail CMOS amplifiers. The LMC6582/4 is an excellent upgrade for circuits using limited common-mode range amplifiers.

The LMC6582/4 has been designed specifically to improve system performance in low voltage applications. Guaranteed operation down to 1.8V means that this family of amplifiers can operate at the end of discharge (EOD) voltages of several popular batteries. The amplifier's 80 fA input current, 0.5 mV offset voltage, and 82 dB CMRR maintain accuracy in battery-powered systems.

For a single, dual or quad CMOS amplifier with similar specs and a powerdown mode, refer to the LMC6681/2/4 datasheet.

Features (Typical unless otherwise noted)

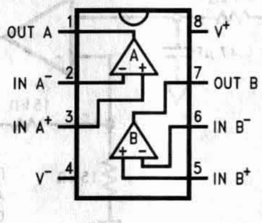
- Guaranteed Specs at 1.8V, 2.2V, 3V, 5V, 10V
- Rail-to-Rail Input Common-Mode Voltage Range
- Rail-to-Rail Output Swing (within 10 mV of supply rail, @ $V_S = 3V$ and $R_L = 10\ k\Omega$)
- CMRR and PSRR 82 dB
- Ultra Low Input Current 80 fA
- High Voltage Gain ($V_S = 3V$, $R_L = 10\ k\Omega$) 120 dB
- Unity Gain Bandwidth 1.2 MHz

Applications

- Battery Operated Systems
- Sensor Amplifiers
- Portable Communication Devices
- Medical Instrumentation
- Level Detectors, Sample-and-Hold Circuits
- Battery Monitoring

Connection Diagrams

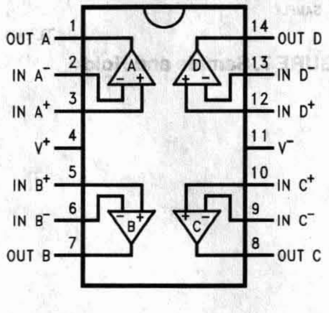
8-Pin DIP/SO



TL/H/12041-1

Top View

14-Pin DIP/SO



TL/H/12041-2

Top View

Ordering Information

Package	Temperature Range Industrial, −40°C to +85°C	NSC Drawing	Transport Media
8-pin Molded DIP	LMC6582AIN, LMC6582BIN	N08E	Rails
8-pin Small Outline	LMC6582AIM, LMC6582BIM LMC6582AIMX, LMC6582BIMX	M08A M08A	Rails Tape and Reel
14-pin Molded DIP	LMC6584AIN, LMC6584BIN	N14A	Rails
14-pin Small Outline	LMC6584AIM, LMC6584BIM LMC6584AIMX, LMC6584BIMX	M14A M14A	Rails Tape and Reel

National Semiconductor

PRELIMINARY

LMC6681 Single/LMC6682 Dual/LMC6684 Quad Low Voltage, Rail-To-Rail Input and Output CMOS Amplifier with Powerdown

General Description

The LMC6681/2/4 is a high performance operational amplifier which can operate over a wide range of supply voltages, from 1.8V to 10V. It has guaranteed specs at 1.8V, 2.2V, 3V, 5V, and 10V.

The LMC6681/2/4 provides an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifier assures maximum dynamic signal range. This rail-to-rail performance of the amplifier, combined with its high open-loop voltage gain makes it unique among CMOS rail-to-rail amplifiers. The LMC6681/2/4 is an excellent upgrade for circuits using limited common-mode range amplifiers.

The LMC6681/2/4 has a powerdown mode which can be triggered externally. In this powerdown mode, the supply current decreases from 1.4 mA (for two amplfiers) to 1.5 μA (for two amplifiers). The LMC6684 has two powerdown options. Each of the powerdown pins disables two amplifiers.

The LMC6681/2/4 has been designed specifically to improve system performance in low voltage applications. The amplifier's 80 fA input current, 0.5 mV offset voltage, and 82 dB CMRR maintain accuracy in battery-powered systems.

Features (Typical unless otherwise noted)

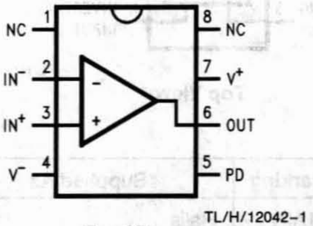
- Guaranteed Specs at 1.8V, 2.2V, 3V, 5V, 10V
- Rail-to-Rail Input Common-Mode Voltage Range
- Rail-to-Rail Output Swing (within 10 mV of supply rail, @ $V_S = 3V$ and $R_L = 10\ k\Omega$)
- Powerdown Mode $I_{S\ OFF} \leq 1.5\ \mu A$/Amplifier (Guaranteed at V_S = 1.8V, 2.2V, 3V, and 5V)
- Ultra Low Input Current 80 fA
- High Voltage Gain (V_S = 3V, R_L = 10 kΩ) 120 dB
- Unity Gain Bandwidth 1.2 MHz

Applications

- Battery Operated Circuits
- Sensor Amplifiers
- Portable Communication Devices
- Medical Instrumentation
- Battery Monitoring Circuits
- Level Detectors, Sample-and-Hold Circuits

Connection Diagrams

8-Pin DIP/SO



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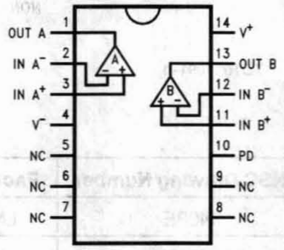
Top View

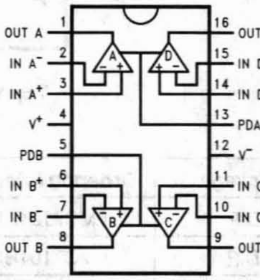
14-Pin DIP/SO



TL/H/12042-2

Top View

16-Pin DIP/SO



TL/H/12042-3

Top View

Ordering Information

Package	Temperature Range Industrial, −40°C to +85°C	NSC Drawing	Transport Media
8-Pin Molded DIP	LMC6681AIN, LMC6681BIN	N08E	Rails
8-Pin Small Outline	LMC6681AIM, LMC6681BIM LMC6681AIMX, LMC6681B1MX	M08A M08A	Rails Tape and Reel
14-Pin Molded DIP	LMC6682AIN, LMC6682BIN	N14A	Rails
14-Pin Small Outline	LMC6682AIM, LMC6682BIM LMC6682AIMX, LMC6682BIMX	M14A M14A	Rails Tape and Reel
16-Pin Molded DIP	LMC6684AIN, LMC6684BIN	N16A	Rails
16-Pin Small Outline	LMC6684AIM, LMC6684BIM LMC6684AIMX, LMC6684BIMX	M16A M16A	Rails Tape and Reel

National Semiconductor

LMC7101 Tiny Low Power Operational Amplifier with Rail-To-Rail Input and Output

General Description

The LMC7101 is a high performance CMOS operational amplifier available in the space saving SOT 23-5 Tiny package. This makes the LMC7101 ideal for space and weight critical designs. The performance is similar to a single amplifier of the LMC6482/4 type, with rail-to-rail input and output, high open loop gain, low distortion, and low supply currents.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

Features

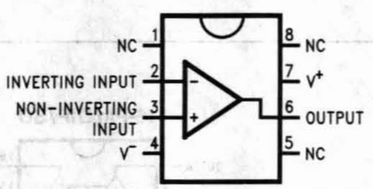
- Tiny SOT23-5 package saves space—typical circuit layouts take half the space of SO-8 designs
- Guaranteed specs at 2.7V, 3V, 5V, 15V supplies
- Typical supply current 0.5 mA at 5V
- Typical total harmonic distortion of 0.01% at 5V
- 1.0 MHz gain-bandwidth
- Similar to popular LMC6482/4
- Input common-mode range includes V^- and V^+
- Tiny package outside dimensions—120 x 118 x 56 mils, 3.05 x 3.00 x 1.43 mm

Applications

- Mobile communications
- Notebooks and PDAs
- Battery powered products
- Sensor interface

Connection Diagrams

8-Pin DIP



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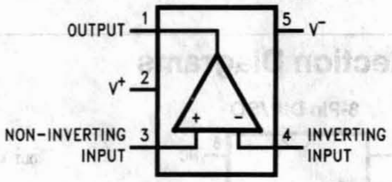
Top View

5-Pin SOT23-5



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Top View

Package	Ordering Information	NSC Drawing Number	Package Marking	Supplied As
8-Pin DIP	LMC7101AIN	N08E	LMC7101AIN	Rails
8-Pin DIP	LMC7101BIN	N08E	LMC7101BIN	Rails
5-Pin SOT 23-5	LMC7101AIM5	MA05A	A00A	250 Units on Tape and Reel
5-Pin SOT 23-5	LMC7101BIM5	MA05A	A00B	250 Units on Tape and Reel
5-Pin SOT 23-5	LMC7101AIM5X	MA05A	A00A	3k Units Tape and Reel
5-Pin SOT 23-5	LMC7101BIM5X	MA05A	A00B	3k Units Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Difference Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage $(V^+ - V^-)$	16V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±35 mA
Current at Power Supply Pin	35 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Recommended Operating Conditions (Note 1)

Supply Voltage	$2.7V \leq V^+ \leq 15.5V$
Junction Temperature Range	
LMC7101AI, LMC7101BI	$-40°C \leq T_J \leq +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M05A Package, 5-Pin Surface Mt.	325°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 2.7V$	0.11	6	9	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1			μV/°C
I_B	Input Bias Current		1.0	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	$0V \leq V_{CM} \leq 2.7V$ $V^+ = 2.7V$	70	55	50	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = V$ For CMRR ≥ 50 dB	0.0	0.0	0.0	V min
			3.0	2.7	2.7	V max
PSRR	Power Supply Rejection Ratio	$V^+ = 1.35V$ to $1.65V$ $V^- = -1.35V$ to $-1.65V$ $V_{CM} = 0$	60	50	45	dB min
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$R_L = 2\ k\Omega$	2.45	2.15	2.15	V min
			0.25	0.5	0.5	V max
		$R_L = 10\ k\Omega$	2.68	2.64	2.64	V min
			0.025	0.06	0.06	V max
I_S	Supply Current		0.5	0.81 **0.95**	0.81 **0.95**	mA max
SR	Slew Rate	(Note 8)	0.7			V/μs
GBW	Gain-Bandwidth Product		0.6			MHz

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L = 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.11	4 **6**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1			μV/°C
I_B	Input Current		1.0	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	$0V \le V_{CM} \le 3V$ $V^+ = 3V$	74	64	60	db min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	0.0	0.0	0.0	V min
			3.3	3.0	3.0	V max
PSRR	Power Supply Rejection Ratio	$V^+ = 1.5V$ to $7.5V$ $V^- = -1.5V$ to $-7.5V$ $V_O = V_{CM} = 0$	80	68	60	dB min
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$R_L = 2\ k\Omega$	2.8	2.6	2.6	V min
			0.2	0.4	0.4	V max
		$R_L = 600\Omega$	2.7	2.5	2.5	V min
			0.37	0.6	0.6	V max
I_S	Supply Current		0.5	0.81 **0.95**	0.81 **0.95**	mA max

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L = 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 5V$	0.11	3 **5**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0			μV/°C
I_B	Input Current		1	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	$0V \le V_{CM} \le 5V$	82	65 **60**	60 **55**	db min
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 5V$ to $15V$ $V^- = 0V$, $V_O = 1.5V$	82	70 **65**	65 **62**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$V^- = -5V$ to $-15V$ $V^+ = 0V$, $V_O = -1.5V$	82	70 **65**	65 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	−0.3	−0.20 **0.00**	−0.20 **0.00**	V min
			5.3	5.20 **5.00**	5.20 **5.00**	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$R_L = 2\ k\Omega$	4.9	4.7 **4.6**	4.7 **4.6**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	V max
		$R_L = 600\Omega$	4.7	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	V max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0V$	24	16 **11**	16 **11**	mA min
		Sinking, $V_O = 5V$	19	11 **7.5**	11 **7.5**	mA min
I_S	Supply Current		0.5	0.85 **1.0**	0.85 **1.0**	mA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L = 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	F = 10 kHz, $A_V = -2$ $R_L = 10\ k\Omega$, $V_O = 4.0\ V_{PP}$	0.01			%
SR	Slew Rate		1.0			V/μs
GBW	Gain_Bandwidth Product		1.0			MHz

15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 15V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L = 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.11			mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0			μV/°C
I_B	Input Current		1.0	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	$0V \le V_{CM} \le 15V$	82	70 **65**	65 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 5V$ to 15V $V^- = 0V$, $V_O = 1.5V$	82	70 **65**	65 **62**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$V^- = -5V$ to $-15V$ $V^+ = 0V$, $V_O = -1.5V$	82	70 **65**	65 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ For CMRR ≥ 50 dB	−0.3	−0.20 **0.00**	−0.20 **0.00**	V min
			15.3	15.20 **15.00**	15.20 **15.00**	V max
A_V	Large Signal Voltage Gain	$R_L = 2\ k\Omega$ (Note 7) Sourcing	340	80 **40**	80 **40**	V/mV
		Sinking	24	15 **10**	15 **10**	
		$R_L = 600\Omega$ (Note 7) Sourcing Sinking	300 15	34 6	34 6	V/mV
C_{IN}	Input Capacitance		3			pF
V_O	Output Swing	$V^+ = 15V$ $R_L = 2\ k\Omega$	14.7	14.4 **14.2**	14.4 **14.2**	V min
			0.16	0.32 **0.45**	0.32 **0.45**	V max
		$V^+ = 15V$ $R_L = 600\Omega$	14.1	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.3**	1.0 **1.3**	V max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0V$ (Note 9)	50	30 **20**	30 **20**	mA min
		Sinking, $V_O = 12V$ (Note 9)	50	30 **20**	30 **20**	mA min
I_S	Supply Current		0.8	1.50 **1.71**	1.50 **1.71**	mA max

15V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 15V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L = 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
SR	Slew Rate	$V^+ = 15V$ (Note 8)	1.1	0.5 **0.4**	0.5 **0.4**	V/µs min
GBW	Gain-Bandwidth Product	$V^+ = 15V$	1.1			MHz
ϕ_m	Phase Margin		45			Deg
G_m	Gain Margin		10			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz $V_{CM} = 1V$	37			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	F = 1 kHz	1.5			$\frac{fA}{\sqrt{Hz}}$
T.H.D.	Total Harmonic Distortion	F = 10 kHz, $A_V = -2$ $R_L = 10\ k\Omega$, $V_O = 8.5\ V_{PP}$	0.01			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $PD = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 1.5V$ and R_L connect to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 12.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

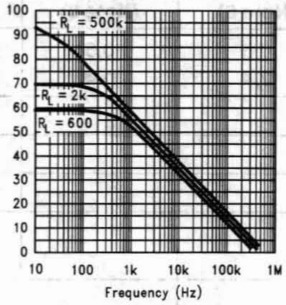
Note 8: $V^+ = 15V$. Connected as a Voltage Follower with a 10V step input. Number specified is the slower of the positive and negative slew rates. $R_L = 100\ k\Omega$ connected to 7.5V. Amp excited with 1 kHz to produce $V_O = 10\ V_{PP}$.

Note 9: Do not short circuit output to V^+ when V^+ is greater than 12V or reliability will be adversely affected.

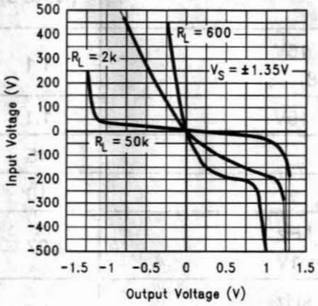
Typical Performance Characteristics $V_S = +2.7V$, Single Supply, $T_A = 25°C$ unless specified

2.7V PERFORMANCE

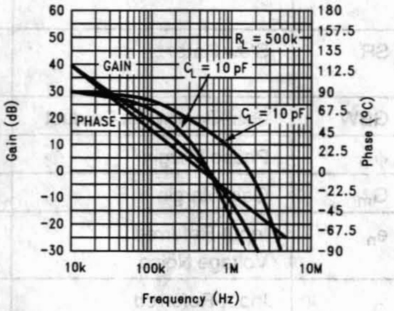
Open Loop Frequency Response (2.7V)



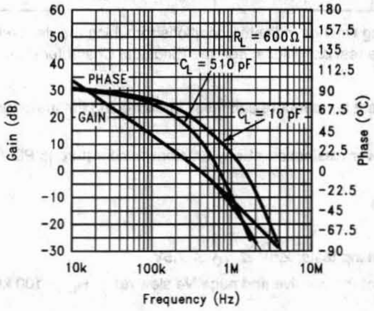
Input Voltage vs Output Voltage (2.7V)



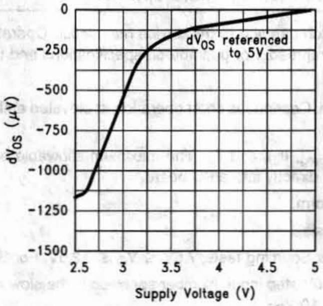
Gain and Phase vs Capacitance Load (2.7V)



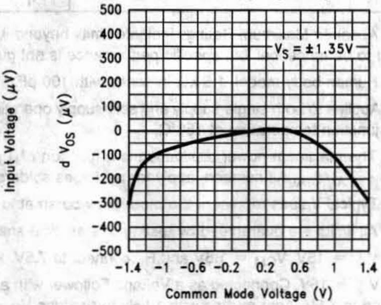
Gain and Phase vs Capacitance Load (2.7V)



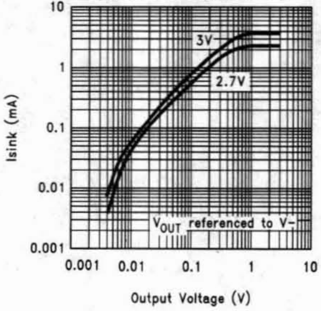
dV_{OS} vs Supply Voltage



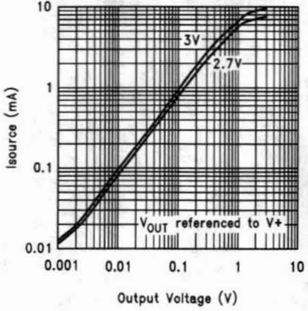
dV_{OS} vs Common Mode Voltage (2.7V)



Sinking Current vs Output Voltage (2.7V)



Sourcing Current vs Output Voltage (2.7V)



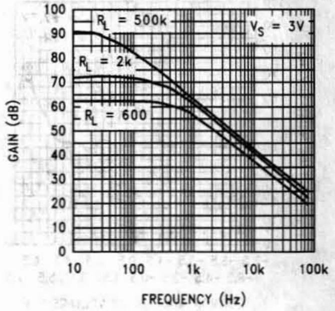
TL/H/11991–15

Typical Performance Characteristics

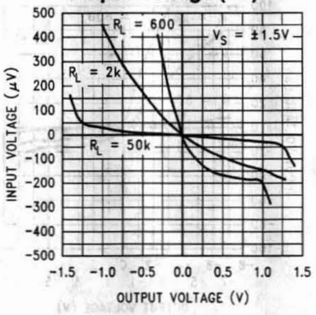
Single Supply, $T_A = 25^\circ C$ unless specified (Continued)

3V PERFORMANCE

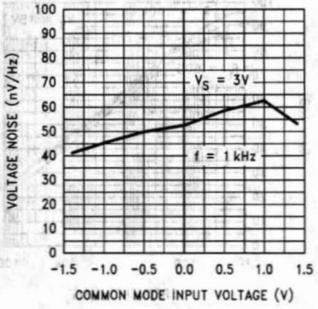
Open Loop Frequency Response (3V)



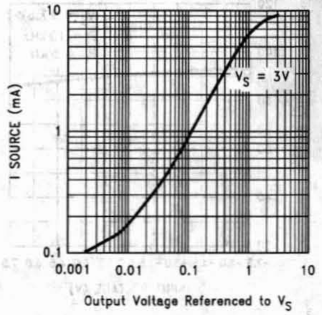
Input Voltage vs Output Voltage (3V)



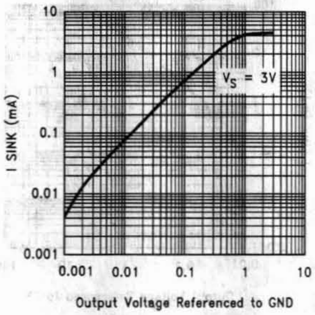
Input Voltage Noise vs Input Voltage (3V)



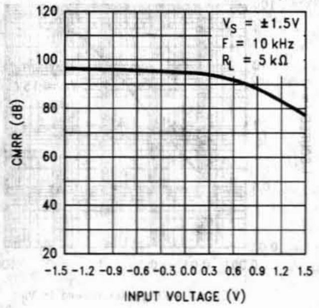
Sourcing Current vs Output Voltage (3V)



Sinking Current vs Output Voltage (3V)

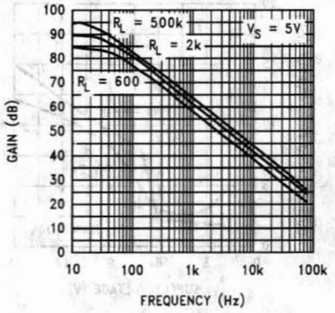


CMRR vs Input Voltage (3V)

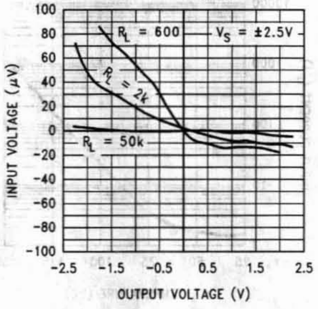


5V PERFORMANCE

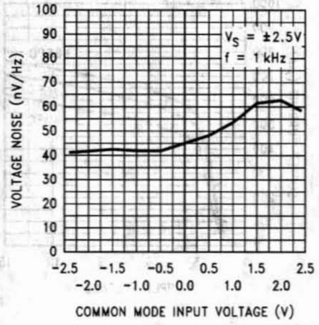
Open Loop Frequency Response (5V)



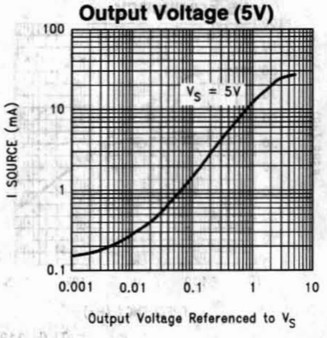
Input Voltage vs Output Voltage (5V)



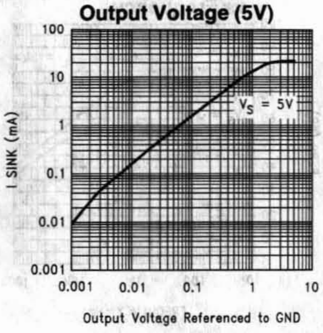
Input Voltage Noise vs Input Voltage (5V)



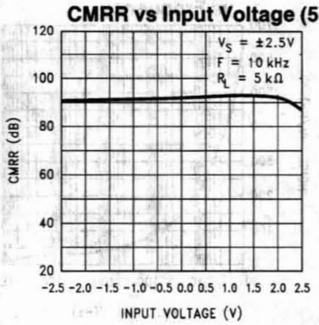
Sourcing Current vs Output Voltage (5V)



Sinking Current vs Output Voltage (5V)



CMRR vs Input Voltage (5V)

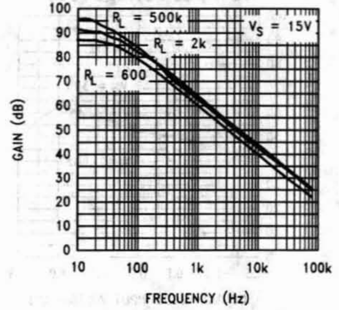


TL/H/11991–3

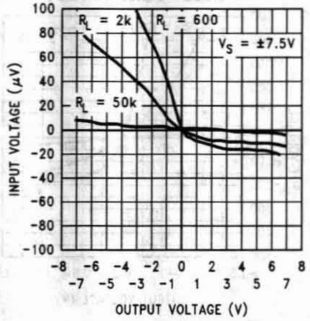
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25°C$ unless specified (Continued)

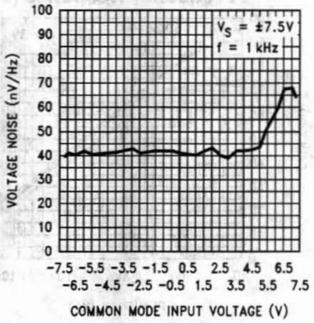
Open Loop Frequency Response (15V)



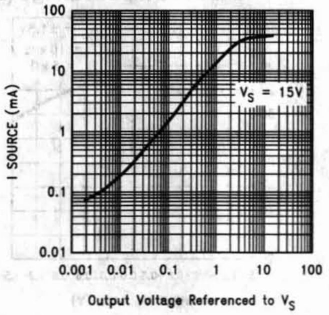
Input Voltage vs Output Voltage (15V)



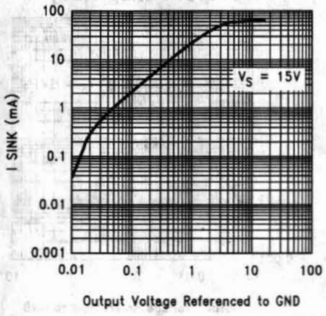
Input Voltage Noise vs Input Voltage (15V)



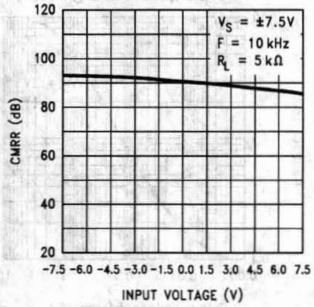
Sourcing Current vs Output Voltage (15V)



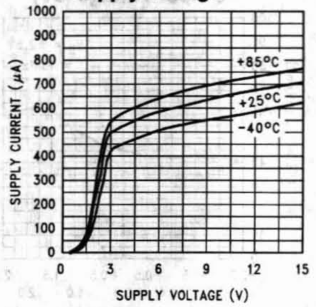
Sinking Current vs Output Voltage (15V)



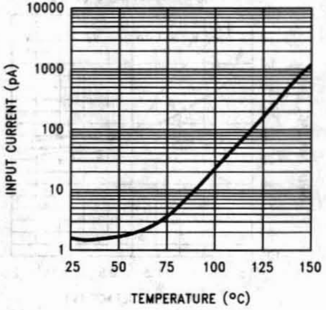
CMRR vs Input Voltage (15V)



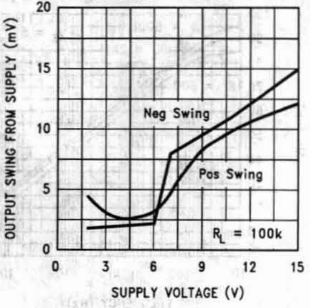
Supply Current vs Supply Voltage



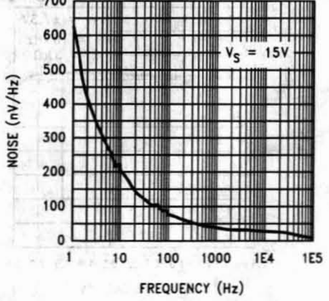
Input Current vs Temperature



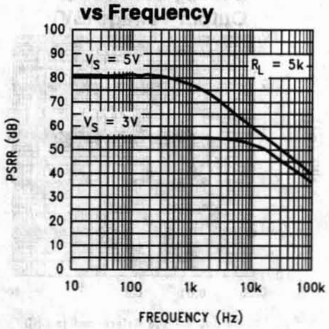
Output Voltage Swing vs Supply Voltage



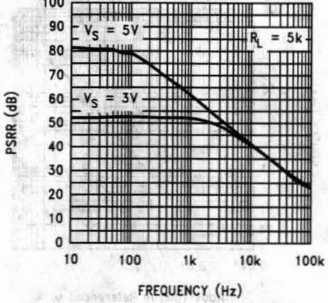
Input Voltage Noise vs Frequency



Positive PSRR vs Frequency



Negative PSRR vs Frequency

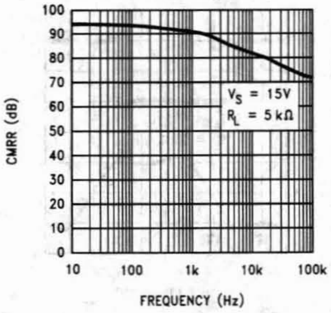


TL/H/11991–4

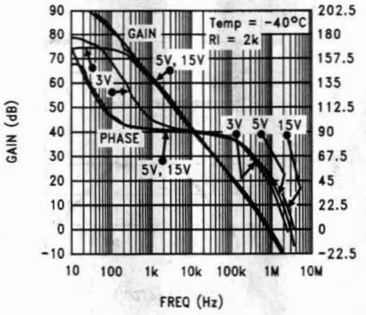
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25°C$ unless specified (Continued)

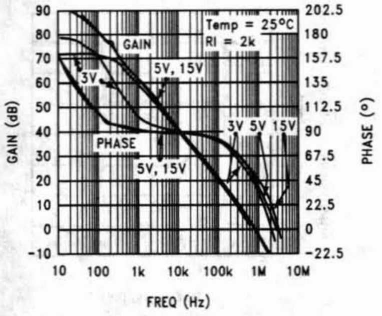
CMRR vs Frequency



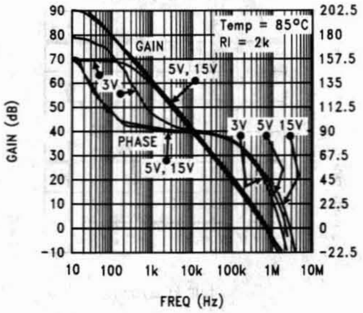
Open Loop Frequency Response @ −40°C



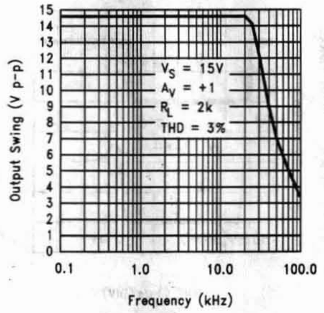
Open Loop Frequency Response @ 25°C



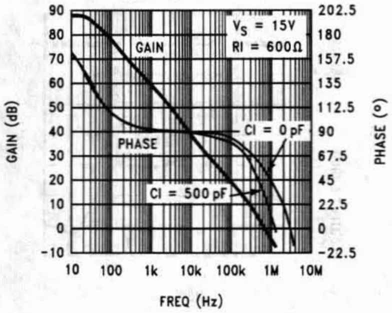
Open Loop Frequency Response @ 85°C



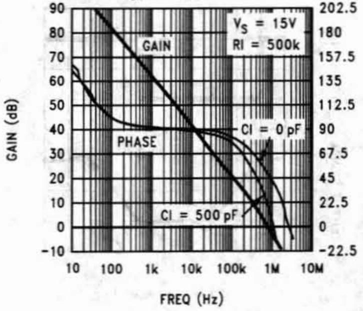
Maximum Output Swing vs Frequency



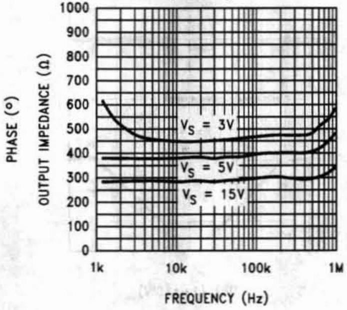
Gain and Phase vs Capacitive Load



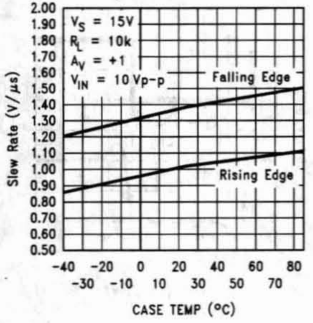
Gain and Phase vs Capacitive Load



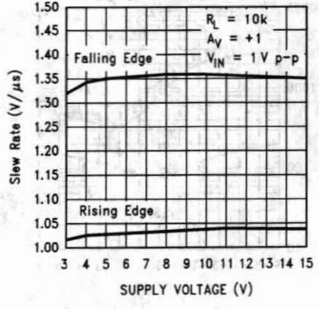
Output Impedance vs Frequency



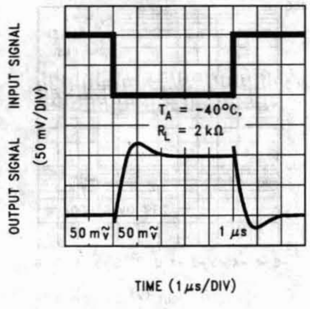
Slew Rate vs Temperature



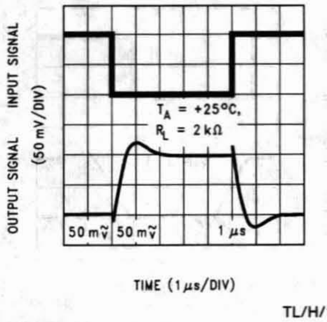
Slew Rate vs Supply Voltage



Inverting Small Signal Pulse Response



Inverting Small Signal Pulse Response

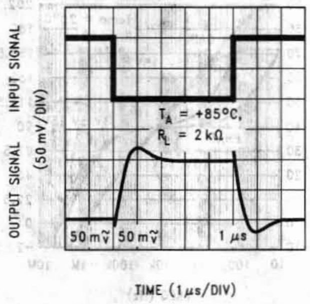


TL/H/11991–5

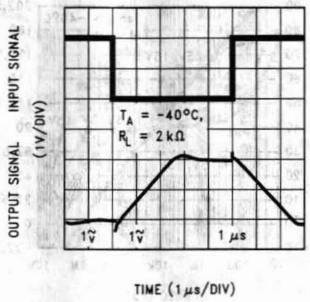
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25°C$ unless specified (Continued)

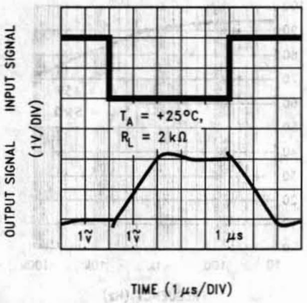
Inverting Small Signal Pulse Response



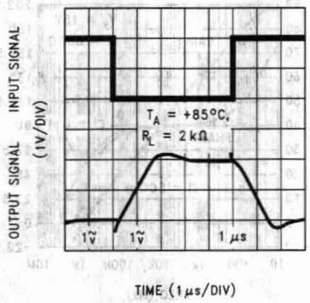
Inverting Large Signal Pulse Response



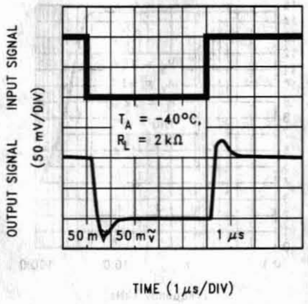
Inverting Large Signal Pulse Response



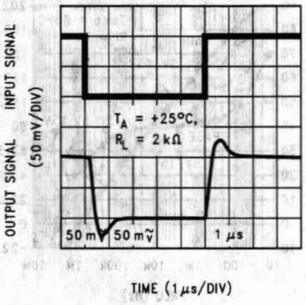
Inverting Large Signal Pulse Response



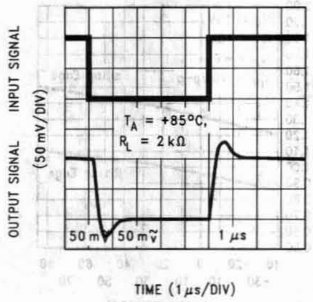
Non-Inverting Small Signal Pulse Response



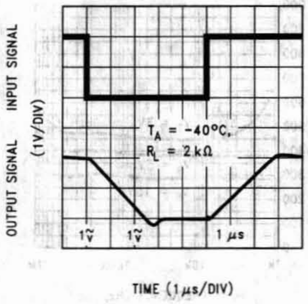
Non-Inverting Small Signal Pulse Response



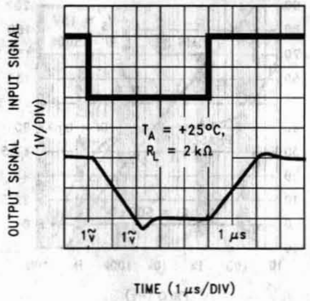
Non-Inverting Small Signal Pulse Response



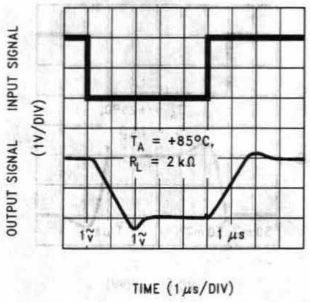
Non-Inverting Large Signal Pulse Response



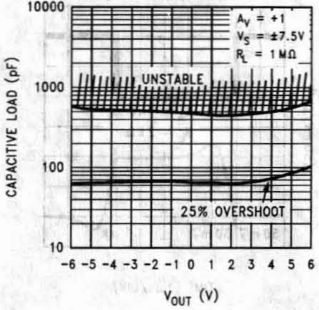
Non-Inverting Large Signal Pulse Response



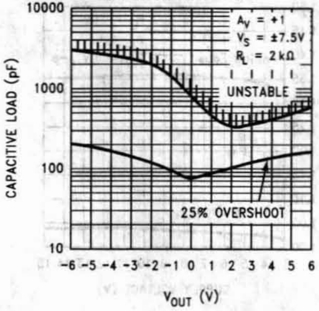
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load

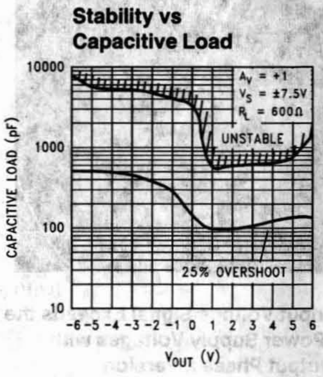


TL/H/11991–6

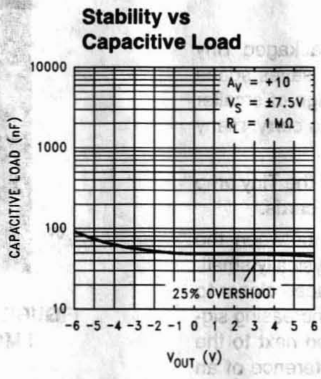
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless specified (Continued)

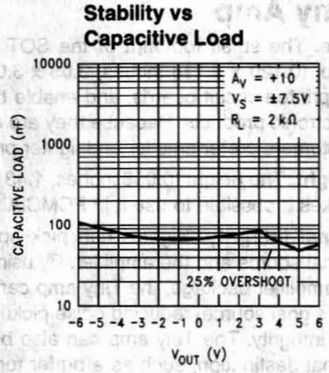
Stability vs Capacitive Load



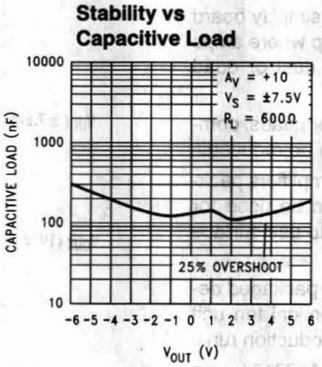
Stability vs Capacitive Load



Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/11991-7

Application Information

1.0 Benefits of the LMC7101 Tiny Amp

Size. The small footprint of the SOT 23-5 packaged Tiny amp, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

Height. The height (0.056 inches, 1.43 mm) of the Tiny amp makes it possible to use it in PCMCIA type III cards.

Signal Integrity. Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

Simplified Board Layout. The Tiny amp can simplify board layout in several ways. First, by placing an amp where amps are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny amps instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

DIPs available for prototyping. LMC7101 amplifiers packaged in conventional 8-pin dip packages can be used for prototyping and evaluation without the need to use surface mounting in early project stages.

Tapes of ten for prototyping. The SOT23-5 packaged devices are available in convenient and economical ten unit tapes for prototypes, evaluation, and small production runs.

Low THD. The high open loop gain of the LMC7101 amp allows it to achieve very low audio distortion—typically 0.01% at 10 kHz with a 10 kΩ load at 5V supplies. This makes the Tiny an excellent for audio, modems, and low frequency signal processing.

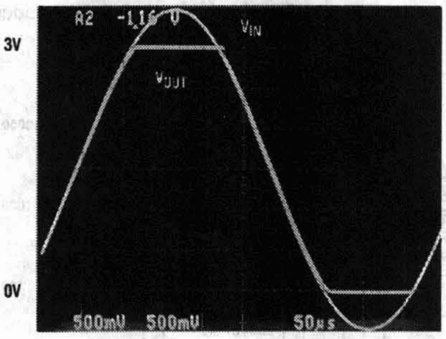
Low Supply Current. The typical 0.5 mA supply current of the LMC7101 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Wide Voltage Range. The LMC7101 is characterized at 15V, 5V and 3V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7101 a good choice for devices where the voltage may vary over the life of the batteries.

2.0 Input Common Mode Voltage Range

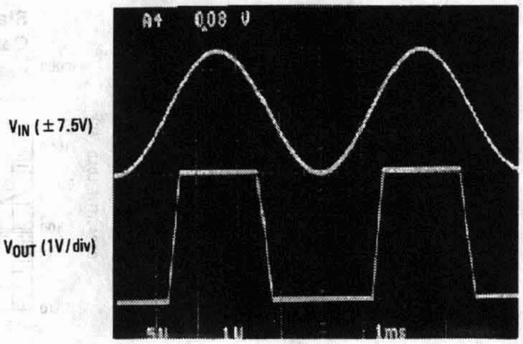
The LMC7101 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion of the output.

The absolute maximum input voltage is 300 mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins, adversely affecting reliability.



TL/H/11991-8

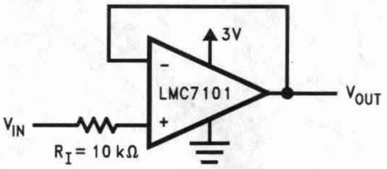
FIGURE 1. An Input Voltage Signal Exceeds the LMC7101 Power Supply Voltages with No Output Phase Inversion



TL/H/11991-9

FIGURE 2. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in *Figure 3* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in *Figure 3*.



TL/H/11991-10

FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

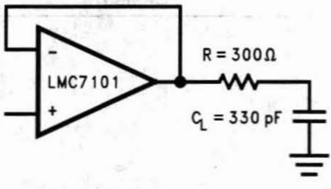
3.0 Rail-To-Rail Output

The approximate output resistance of the LMC7101 is 180Ω sourcing and 130Ω sinking at $V_S = 3V$ and 110Ω sourcing and 80Ω sinking at $V_S = 5V$. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC7101 can typically directly drive a 100 pF load with $V_S = 15V$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.



TL/H/11991–11

FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

5.0 Compensating for Input Capacitance when Using Large Value Feedback Resistors

When using very large value feedback resistors, (usually > 500 kΩ) the large feed back resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 5*), C_f is first estimated by:

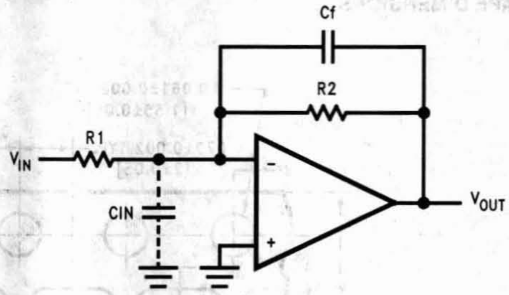
$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)



TL/H/11991–12

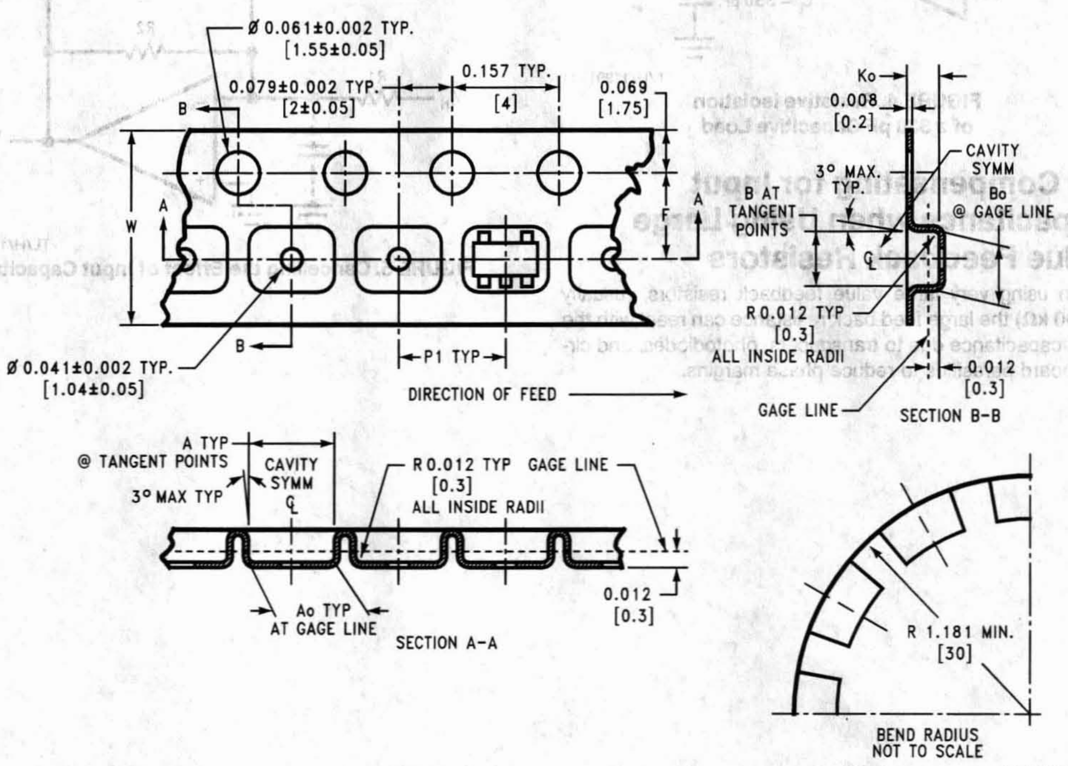
FIGURE 5. Cancelling the Effect of Input Capacitance

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

TAPE DIMENSIONS



Ø 0.061±0.002 TYP.
[1.55±0.05]
0.079±0.002 TYP.
[2±0.05]
0.157 TYP.
[4]
0.069
[1.75]
B
A
W
F
A
B
Ø 0.041±0.002 TYP.
[1.04±0.05]
P1 TYP
DIRECTION OF FEED
Ko
0.008
[0.2]
CAVITY SYMM
3° MAX. TYP.
B AT TANGENT POINTS
Bo @ GAGE LINE
℄
R 0.012 TYP
[0.3]
ALL INSIDE RADII
0.012
[0.3]
GAGE LINE
SECTION B-B
A TYP @ TANGENT POINTS
3° MAX TYP
CAVITY SYMM
℄
R 0.012 TYP
[0.3]
ALL INSIDE RADII
GAGE LINE
0.012
[0.3]
Ao TYP AT GAGE LINE
SECTION A-A
R 1.181 MIN.
[30]
BEND RADIUS NOT TO SCALE

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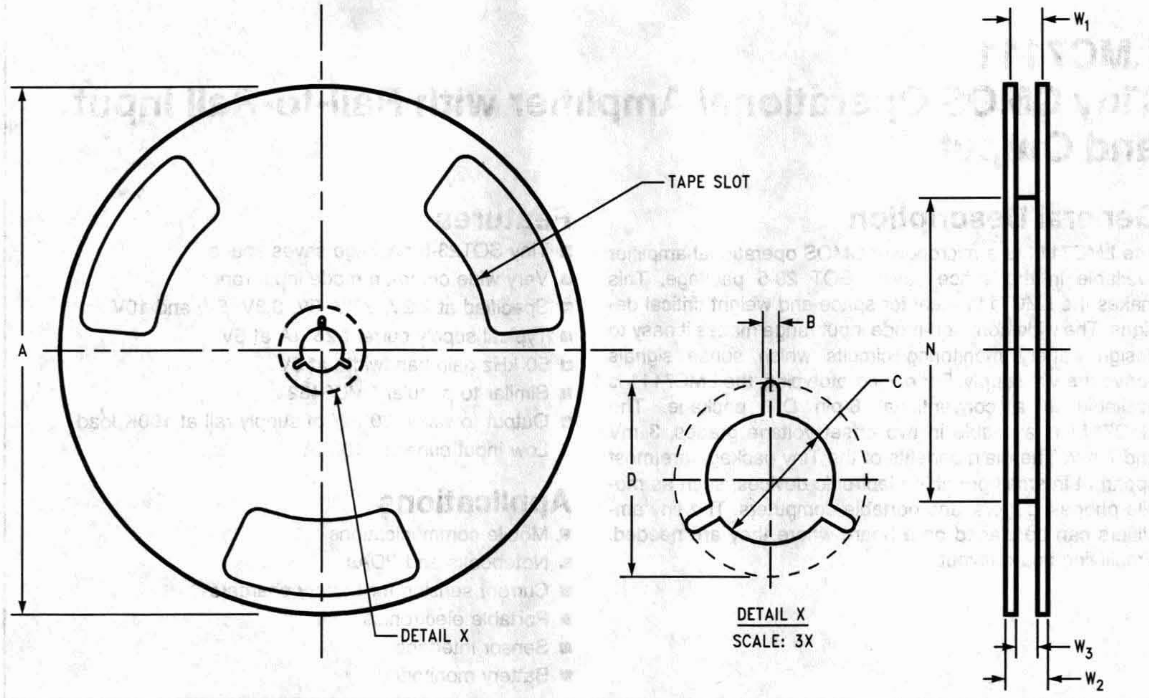
8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

SOT-23-5 Tape and Reel Specification (Continued)

REEL DIMENSIONS



TL/H/11991–14

8 mm	7.00	0.059	0.512	0.795	2.165	0.331 + 0.059/−0.000	0.567	W1 + 0.078/−0.039
	330.00	1.50	13.00	20.20	55.00	8.40 + 1.50/−0.00	14.40	W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

6.0 SPICE Macromodel

A SPICE macromodel is available for the LMC7101. This model includes simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions and many more characteristics as listed on the macro model disk. Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

National Semiconductor

PRELIMINARY

LMC7111
Tiny CMOS Operational Amplifier with Rail-to-Rail Input and Output

General Description

The LMC7111 is a micropower CMOS operational amplifier available in the space saving SOT 23-5 package. This makes the LMC7111 ideal for space and weight critical designs. The wide common-mode input range makes it easy to design battery monitoring circuits which sense signals above the V+ supply. For easy prototyping, the LMC7111 is available in a conventional 8-pin DIP package. The LMC7111 is available in two offset voltage grades, 3 mV and 7 mV. The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, and portable computers. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

Features

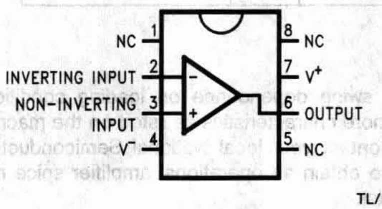
- Tiny SOT23-5 package saves space
- Very wide common mode input range
- Specified at 2.2V, 2.7V, 3V, 3.3V, 5V, and 10V
- Typical supply current 25 µA at 5V
- 50 kHz gain-bandwidth at 5V
- Similar to popular LMC6462
- Output to within 20 mV of supply rail at 100K load
- Low input current 100 fA

Applications

- Mobile communications
- Notebooks and PDAs
- Current sensing for battery chargers
- Portable electronics
- Sensor interface
- Battery monitoring

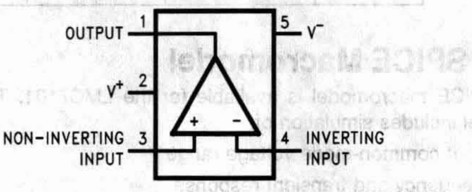
Connection Diagrams

8-Pin DIP



Top View

5-Pin SOT23-5



Top View

Ordering Information

Package	Ordering Information	NSC Drawing Number	Package Marking	Transport Media
8-Pin DIP	LMC7111AIN	N08E	LMC7111AIN	Rails
8-Pin DIP	LMC7111BIN	N08E	LMC7111BIN	Rails
5-Pin SOT23-5	LMC7111AIM5	MA05A	A01A	250 Units on Tape and Reel
5-Pin SOT23-5	LMC7111BIM5	MA05A	A01B	250 Units on Tape and Reel
5-Pin SOT23-5	LMC7111AIM5X	MA05A	A01A	3K Units on Tape and Reel
5-Pin SOT23-5	LMC7111BIM5X	MA05A	A01B	3K Units on Tape and Reel

National Semiconductor

LPC660
Low Power CMOS Quad Operational Amplifier

General Description

The LPC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltage from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is typically less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC662 datasheet for a Dual CMOS operational amplifier and LPC661 datasheet for a single CMOS operational amplifier with these same features.

Applications

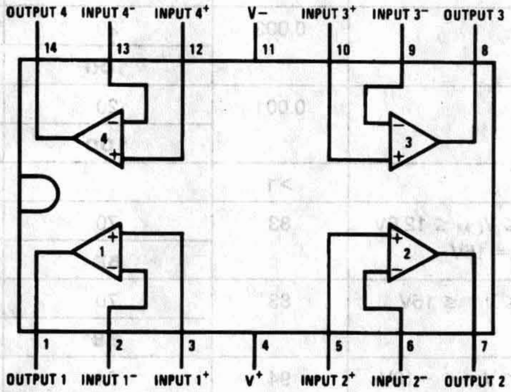
- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Features

- Rail-to-rail output swing
- Micropower operation (1 mW)
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 2 fA
- Input common-mode includes V⁻
- Operation range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/μs
- Full military temp. range available

Connection Diagram

14-Pin DIP/SO



TL/H/10547–1

Top View

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military	Industrial		
14-Pin Side Brazed Ceramic DIP	LPC660AMD		D14E	Rail
14-Pin Small Outline		LPC660AIM or LPC660IM	M14A	Rail Tape and Reel
14-Pin Molded DIP		LPC660AIN or LPC660IN	N14A	Rail
14-Pin Ceramic DIP	LPC660AMJ/883		J14A	Rail

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 1)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 2)	150°C
ESD Rating (C = 100 pF, R = 1.5 kΩ)	1000V
Power Dissipation	(Note 2)
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Current at Power Supply Pin	35 mA

Operating Ratings (Note 3)

Temperature Range	
LPC660AM	$-55°C \le T_J \le +125°C$
LPC660AI	$-40°C \le T_J \le +85°C$
LPC660I	$-40°C \le T_J \le +85°C$
Supply Range	4.75V to 15.5V
Power Dissipation	(Note 9)
Thermal Resistance (θ_{JA}), (Note 10)	
14-Pin Ceramic DIP	90°C/W
14-Pin Molded DIP	85°C/W
14-Pin SO	115°C/W
14-Pin Side Brazed Ceramic DIP	90°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883 Limit (Notes 4, 8)	LPC660AI Limit (Note 4)	LPC660I Limit (Note 4)	Units
Input Offset Voltage		1	3	3	6	mV
			3.5	**3.3**	**6.3**	max
Input Offset Voltage Average Drift		1.3				μV/°C
Input Bias Current		0.002	20			pA
			100	**4**	**4**	max
Input Offset Current		0.001	20			pA
			100	**2**	**2**	max
Input Resistance		>1				Tera Ω
Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 12.0V V^+ = 15V	83	70	70	63	dB
			68	**68**	**61**	min
Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V	83	70	70	63	dB
			68	**68**	**61**	min
Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V	94	84	84	74	dB
			82	**83**	**73**	min
Input Common Mode Voltage Range	V^+ = 5V & 15V For CMRR > 50 dB	−0.4	−0.1	−0.1	−0.1	V
			0	**0**	**0**	max
		V^+ − 1.9	V^+ − 2.3	V^+ − 2.3	V^+ − 2.3	V
			V^+ − 2.6	**V^+ − 2.5**	**V^+ − 2.5**	min

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L > 1M$ unless otherwise specified. (Continued)

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883 Limit (Notes 4, 8)	LPC660AI Limit (Note 4)	LPC660I Limit (Note 4)	Units
Large Signal Voltage Gain	$R_L = 100\ k\Omega$ (Note 5) Sourcing	1000	400	400	300	V/mV min
			250	**300**	**200**	
	Sinking	500	180	180	90	V/mV min
			70	**120**	**70**	
	$R_L = 5\ k\Omega$ (Note 5) Sourcing	1000	200	200	100	V/mV min
			150	**160**	**80**	
	Sinking	250	100	100	50	V/mV min
			35	**60**	**40**	
Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to $V^+/2$	4.987	4.970	4.970	4.940	V min
			4.950	**4.950**	**4.910**	
		0.004	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	$V^+ = 5V$ $R_L = 5\ k\Omega$ to $V^+/2$	4.940	4.850	4.850	4.750	V min
			4.750	**4.750**	**4.650**	
		0.040	0.150	0.150	0.250	V max
			0.250	**0.250**	**0.350**	
	$V^+ = 15V$ $R_L = 100\ k\Omega$ to $V^+/2$	14.970	14.920	14.920	14.880	V min
			14.880	**14.880**	**14.820**	
		0.007	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	$V^+ = 15V$ $R_L = 5\ k\Omega$ to $V^+/2$	14.840	14.680	14.680	14.580	V min
			14.600	**14.600**	**14.480**	
		0.110	0.220	0.220	0.320	V max
			0.300	**0.300**	**0.400**	
Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16	16	13	mA min
			12	**14**	**11**	
	Sinking, $V_O = 5V$	21	16	16	13	mA min
			12	**14**	**11**	
Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19	28	23	mA min
			19	**25**	**20**	
	Sinking, $V_O = 13V$ (Note 11)	39	19	28	23	mA min
			19	**24**	**19**	
Supply Current	All Four Amplifiers $V_O = 1.5V$	160	200	200	240	μA max
			250	**230**	**270**	

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5$, and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883 Limit (Notes 4, 8)	LPC660AI Limit (Note 4)	LPC660I Limit (Note 4)	Units
Slew Rate	(Note 6)	0.11	0.07	0.07	0.05	V/μs
			0.04	**0.05**	**0.03**	min
Gain-Bandwidth Product		0.35				MHz
Phase Margin		50				Deg
Gain Margin		17				dB
Amp-to-Amp Isolation	(Note 7)	130				dB
Input Referred Voltage Noise	F = 1 kHz	42				$nV/\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002				$pA/\sqrt{Hz}$
Total Harmonic Distortion	F = 1 kHz, $A_V = -10$ $R_L = 100\ k\Omega$, $V_O = 8\ V_{PP}$	0.01				%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 6: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

Note 8: A military RETS electrical test specification is available on request. At the time of printing, the LPC660AMJ/883 RETS specification complied fully with the boldface limits in this column. The LPC660AMJ/883 may also be procured to a Standard Military Drawing specification.

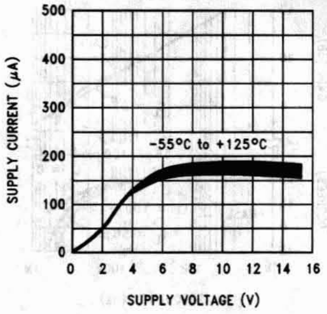
Note 9: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

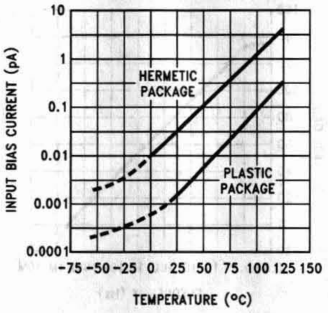
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

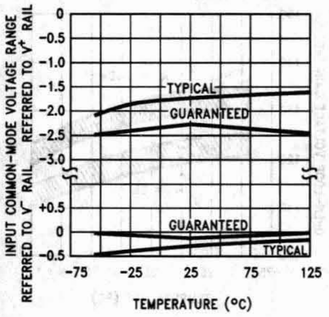
Supply Current vs Supply Voltage



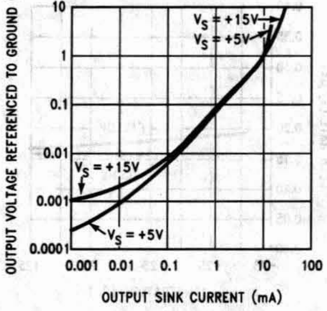
Input Bias Current vs Temperature



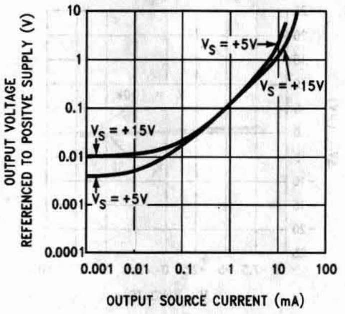
Common-Mode Voltage Range vs Temperature



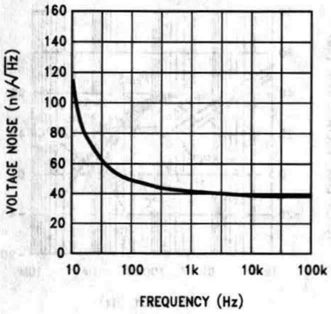
Output Characteristics Current Sinking



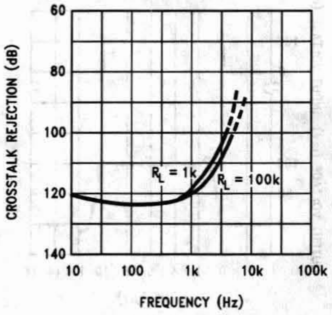
Output Characteristics Current Sourcing



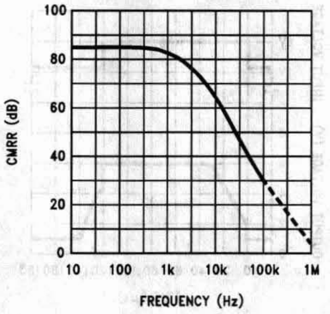
Input Voltage Noise vs Frequency



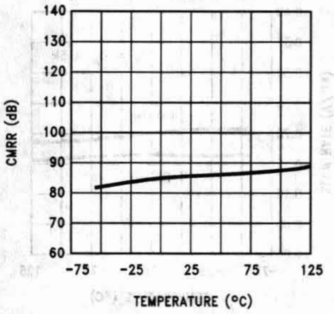
Crosstalk Rejection vs Frequency



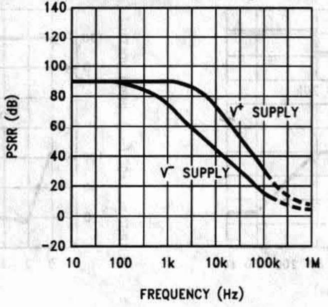
CMRR vs Frequency



CMRR vs Temperature



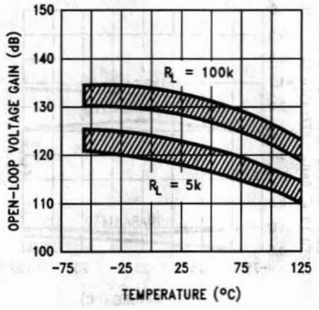
Power Supply Rejection Ratio vs Frequency



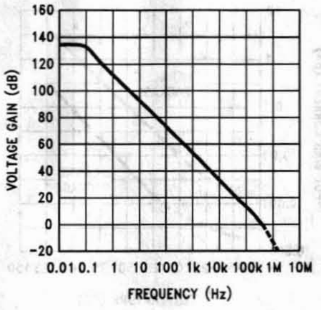
TL/H/10547–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

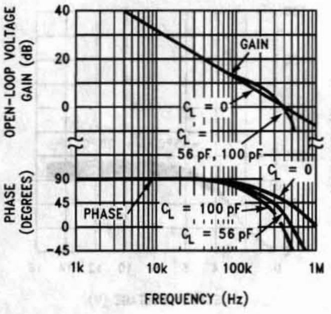
Open-Loop Voltage Gain vs Temperature



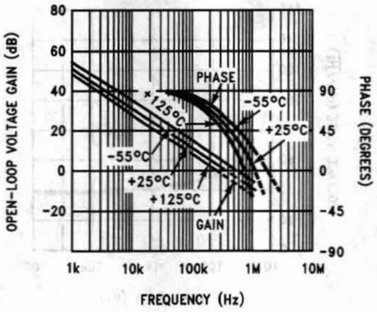
Open-Loop Frequency Response



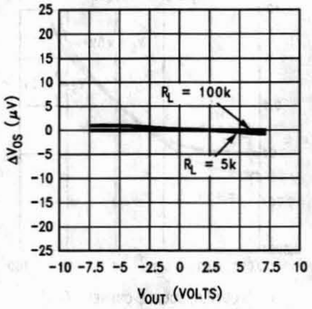
Gain and Phase Responses vs Load Capacitance



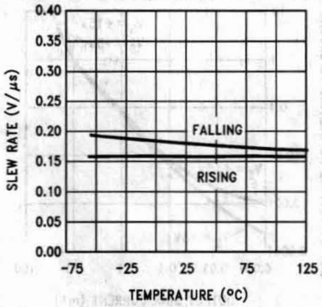
Gain and Phase Responses vs Temperature



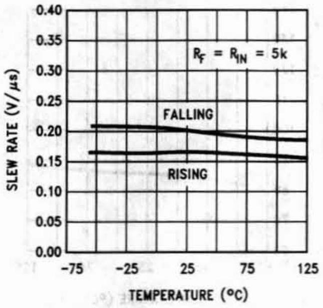
Gain Error (V_{OS} vs V_{OUT})



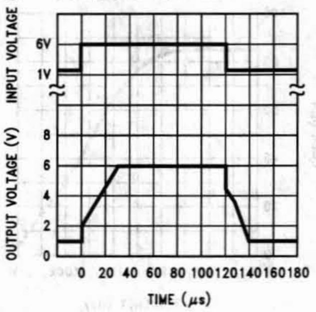
Non-Inverting Slew Rate vs Temperature



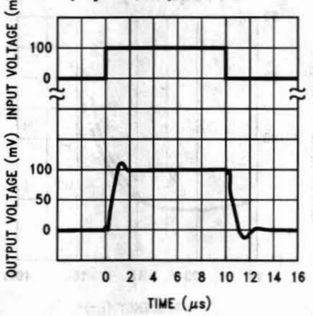
Inverting Slew Rate vs Temperature



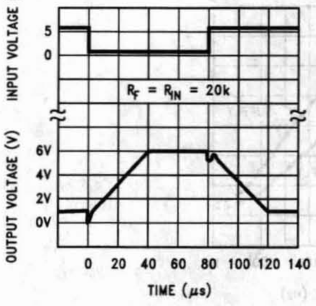
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



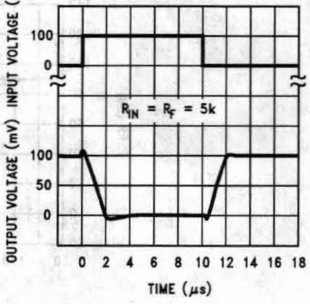
Non-Inverting Small Signal Pulse Response ($A_V = +1$)



Inverting Large-Signal Pulse Response



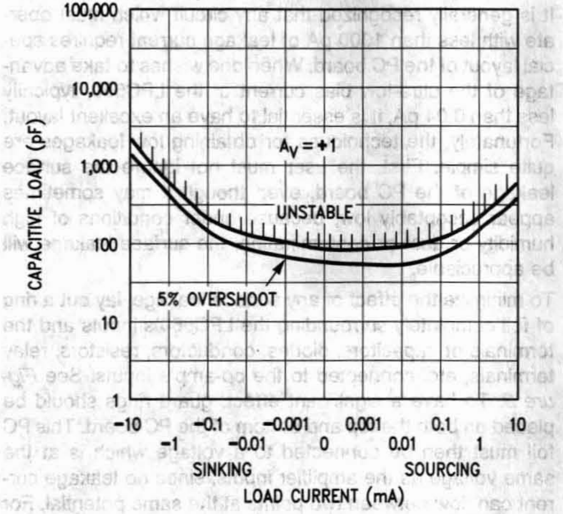
Inverting Small-Signal Pulse Response



TL/H/10547-3

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ (Continued)

Stability vs Capacitive Load



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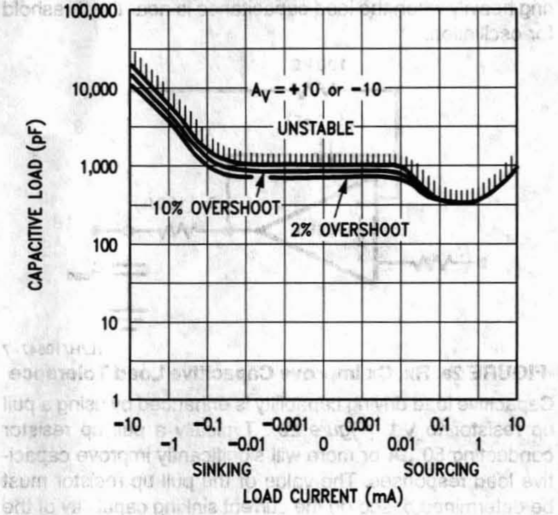
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Stability vs Capacitive Load



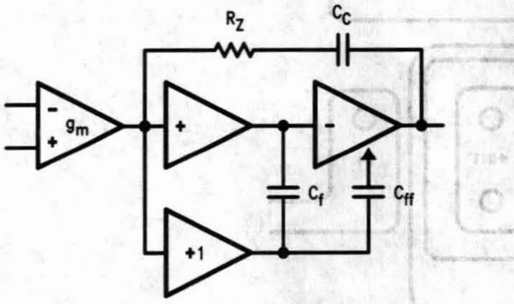
TL/H/10547–5

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC660 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/10547–6

FIGURE 1. LPC660 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

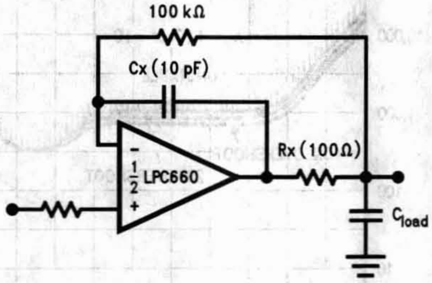
CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

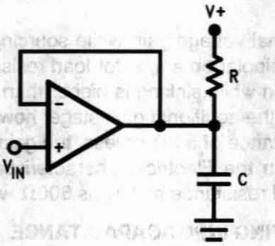
operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/10547-7

FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 2b)*. Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



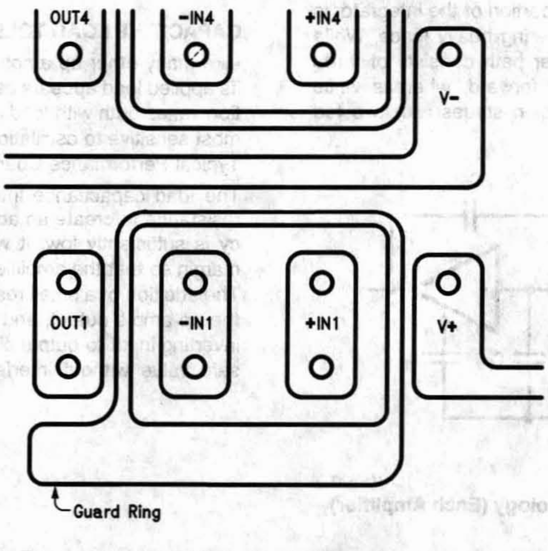
TL/H/10547-26

FIGURE 2b. Compensating for Large Capacitive Loads with A Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC660, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

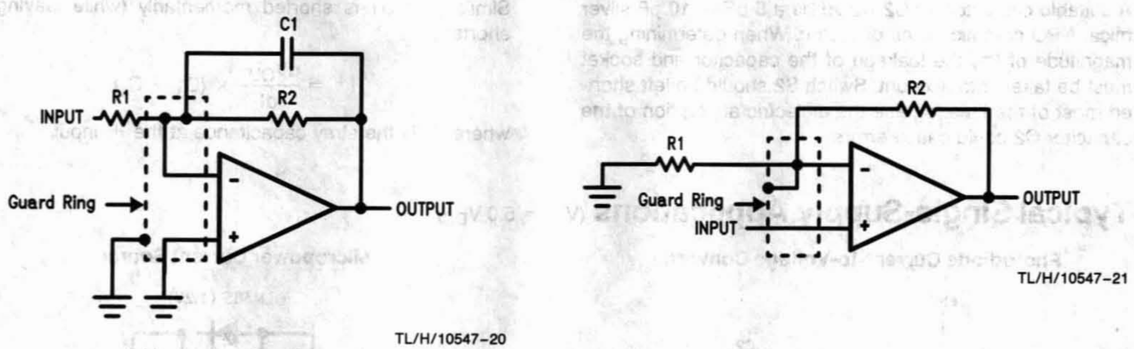
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 4d*.



TL/H/10547-19

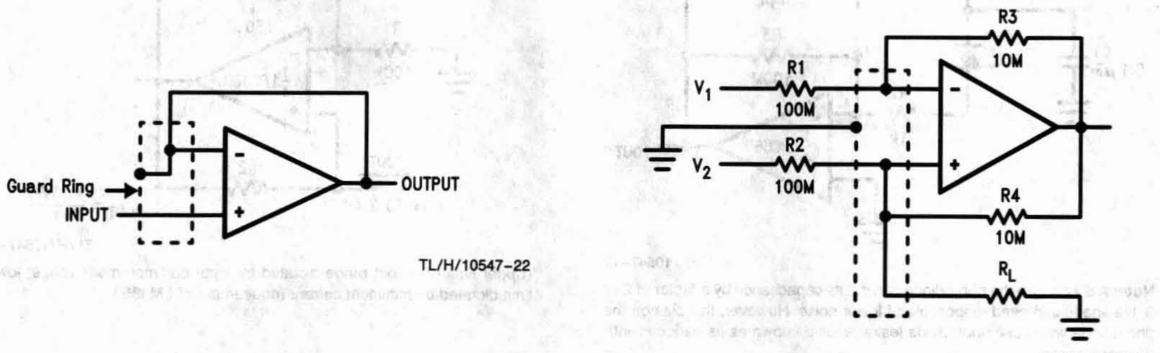
FIGURE 3. Example of Guard Ring in P.C. Board Layout using the LPC660

Application Hints (Continued)


C1
R1
R2
INPUT
Guard Ring
OUTPUT
TL/H/10547-20
R2
R1
Guard Ring
INPUT
OUTPUT
TL/H/10547-21

(a) Inverting Amplifier

(b) Non-Inverting Amplifier

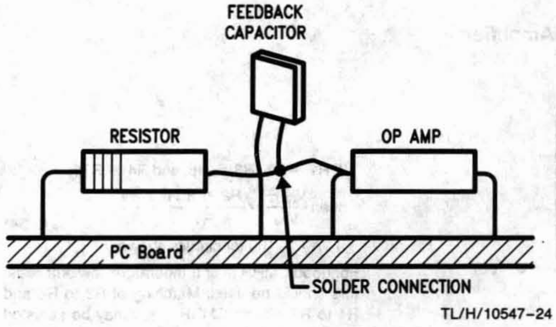

Guard Ring
INPUT
OUTPUT
TL/H/10547-22
R3
10M
R1
V₁
100M
R2
V₂
100M
R4
10M
R_L
TL/H/10547-23

(c) Follower

(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.


FEEDBACK
CAPACITOR
RESISTOR
OP AMP
PC Board
SOLDER CONNECTION
TL/H/10547-24

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 6* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then $I^- = \frac{dV_{OUT}}{dt} \times C2$.

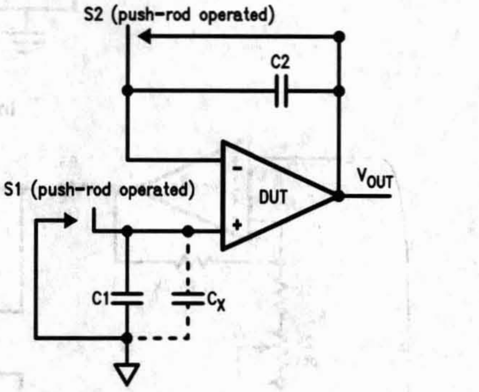

S2 (push-rod operated)
C2
S1 (push-rod operated)
DUT
V_{OUT}
C1
C_X
TL/H/10547-25

FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

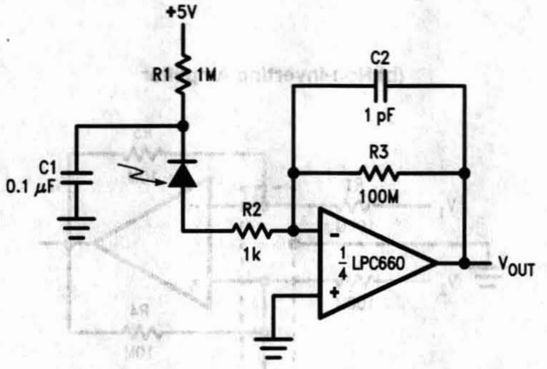
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Photodiode Current-to-Voltage Converter

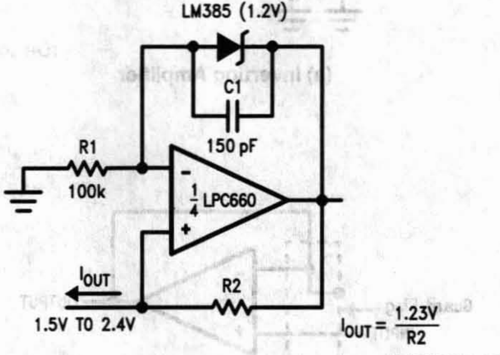


+5V
R1
1M
C2
1 pF
R3
100M
C1
0.1 μF
R2
1k
1/4 LPC660
V_OUT

TL/H/10547-17

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Micropower Current Source

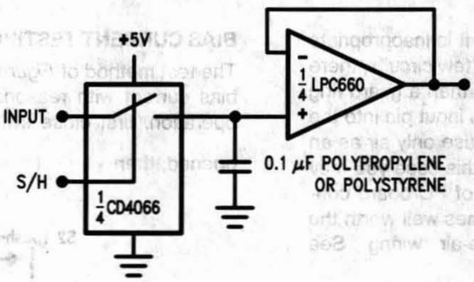


LM385 (1.2V)
C1
150 pF
R1
100k
1/4 LPC660
I_OUT
R2
1.5V TO 2.4V
I_OUT = 1.23V / R2

TL/H/10547-18

(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

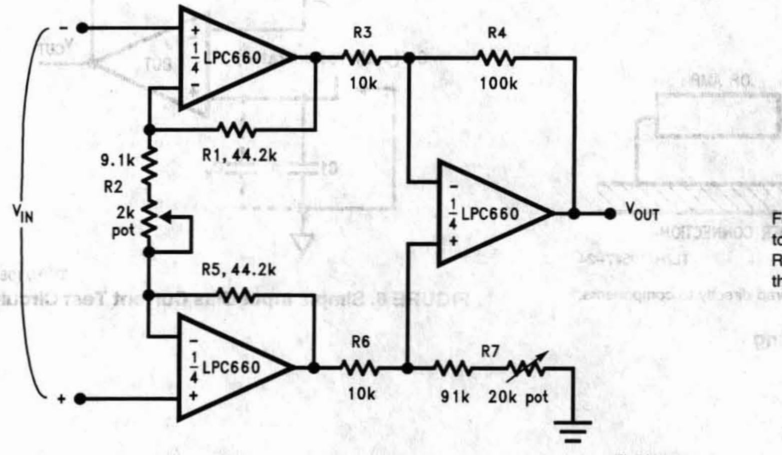
Low-Leakage Sample-and-Hold



+5V
1/4 LPC660
OUTPUT
INPUT
S/H
1/4 CD4066
0.1 μF POLYPROPYLENE OR POLYSTYRENE

TL/H/10547-8

Instrumentation Amplifier



−
+
1/4 LPC660
R3
10k
R4
100k
R1, 44.2k
9.1k
R2
2k pot
V_IN
1/4 LPC660
V_OUT
R5, 44.2k
1/4 LPC660
R6
10k
R7
91k
20k pot

If R1 = R5, R3 = R6, and R4 = R7;

then $\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R1} \times \frac{R4}{R3}$

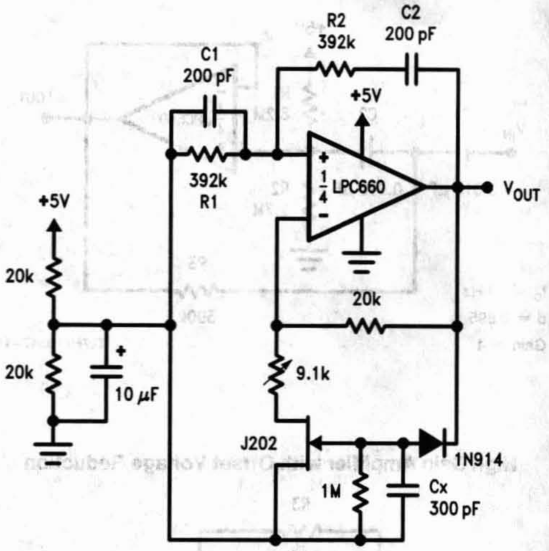
$\therefore A_V \approx 100$ for circuits shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

TL/H/10547-9

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Sine-Wave Oscillator


R2
392k
C2
200 pF
C1
200 pF
+5V
392k
R1
$\frac{1}{4}$ LPC660
V_OUT
+5V
20k
20k
20k
10 µF
9.1k
J202
1N914
1M
Cx
300 pF

TL/H/10547–10

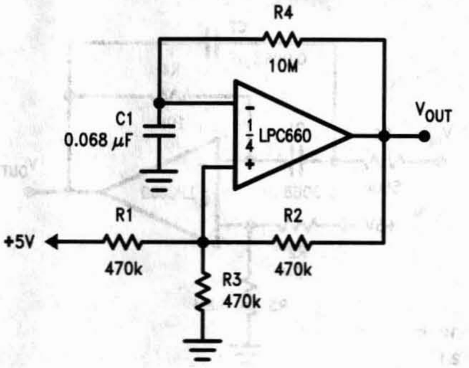
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

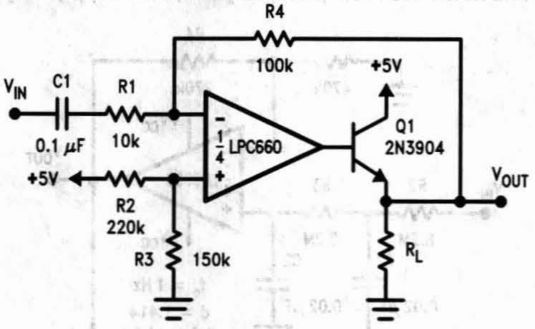
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator


R4
10M
C1
0.068 µF
$\frac{1}{4}$ LPC660
V_OUT
R1
470k
+5V
R2
470k
R3
470k

TL/H/10547–11

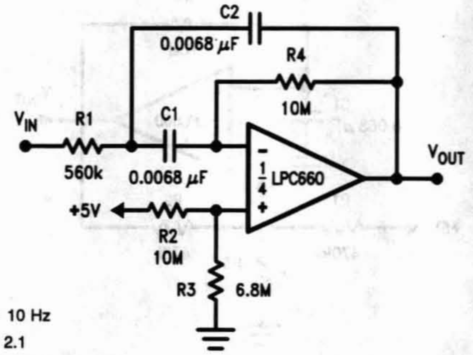
Power Amplifier


R4
100k
+5V
V_IN
C1
0.1 µF
R1
10k
$\frac{1}{4}$ LPC660
Q1
2N3904
+5V
R2
220k
V_OUT
R3
150k
R_L

TL/H/10547–12

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

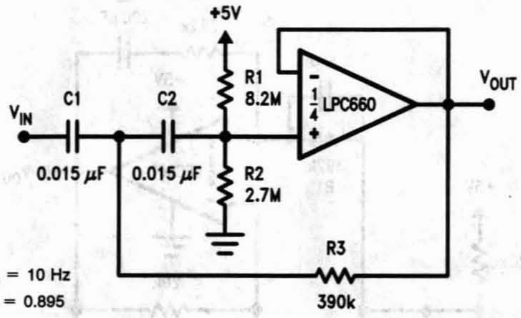
10 Hz Bandpass Filter


C2
0.0068 μF
R4
10M
V_IN
R1
560k
C1
0.0068 μF
−
1/4 LPC660
+
V_OUT
+5V
R2
10M
R3
6.8M

$f_O = 10$ Hz
$Q = 2.1$
Gain = −8.8

TL/H/10547-13

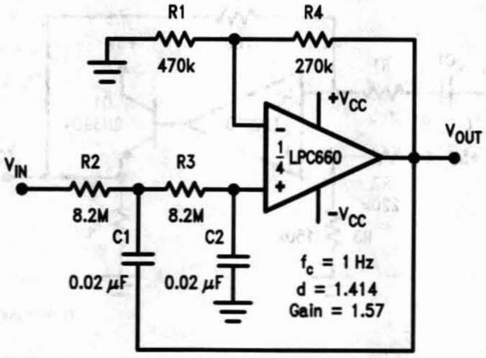
10 Hz High-Pass Filter (2 dB Dip)


+5V
R1
8.2M
V_IN
C1
C2
0.015 μF
0.015 μF
R2
2.7M
−
1/4 LPC660
+
V_OUT
R3
390k

$f_c = 10$ Hz
$d = 0.895$
Gain = 1

TL/H/10547-14

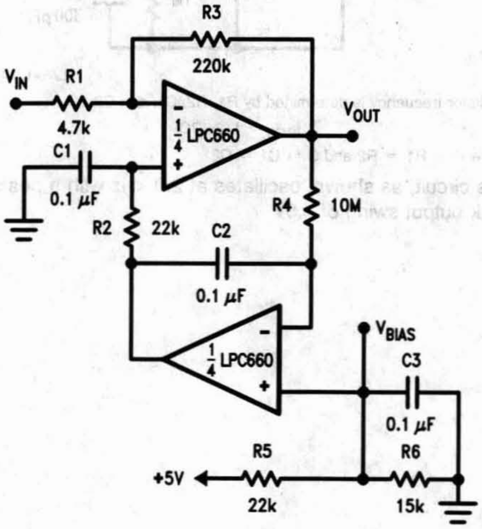
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)


R1
470k
R4
270k
+V_CC
−
1/4 LPC660
+
−V_CC
V_OUT
V_IN
R2
8.2M
R3
8.2M
C1
0.02 μF
C2
0.02 μF

$f_c = 1$ Hz
$d = 1.414$
Gain = 1.57

TL/H/10547-15

High Gain Amplifier with Offset Voltage Reduction


R3
220k
V_IN
R1
4.7k
−
1/4 LPC660
+
V_OUT
C1
0.1 μF
R2
22k
R4
10M
C2
0.1 μF
−
1/4 LPC660
+
V_BIAS
C3
0.1 μF
R5
22k
R6
15k
+5V

Gain = −46.8

TL/H/10547-16

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

National Semiconductor

LPC661
Low Power CMOS Operational Amplifier

General Description

The LPC661 CMOS operational amplifier is ideal for operation from a single supply. It features a wide range of operating supply voltage from +5V to +15V, rail-to-rail output swing and an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the supply current requirement is typically 55 μA.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC660 datasheet for a Quad CMOS operational amplifier or the LPC662 data sheet for a Dual CMOS operational amplifier with these same features.

Features (Typical unless otherwise noted)

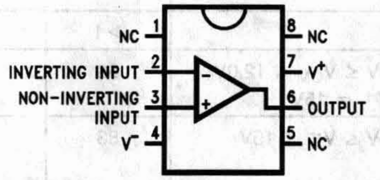
- Rail-to-rail output swing
- Low supply current 55 μA
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 2 fA
- Input common-mode range includes GND
- Operating range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/μs

Applications

- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Connection Diagram

8-Pin DIP/SO



TL/H/11227-1

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
8-Pin Small Outline		LPC661AIM LPC661IM	M08A	Tape and Reel Rail
8-Pin Molded DIP	LPC661AMN	LPC661AIN LPC661IN	N08E	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	16V
Differential Input Voltage	± Supply Voltage
Output Short Circuit to V^+	(Note 9)
Output Short Circuit to V^-	(Note 2)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Junction Temperature (Note 3)	150°C
Power Dissipation	(Note 3)
ESD Rating (C = 100 pF, R = 1.5 kΩ)	1000V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Voltage Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Current at Power Supply Pin	35 mA

Operating Ratings (Note 1)

Supply Voltage	$4.75V \le V^+ \le 15.5V$
Junction Temperature Range	
LPC661AM	$-55°C \le T_J \le +125°C$
LPC661AI	$-40°C \le T_J \le +85°C$
LPC661I	$-40°C \le T_J \le +85°C$
Power Dissipation	(Note 7)
Thermal Resistance (θ_{JA}) (Note 8)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
V_{OS}	Input Offset Voltage		1	3 **3.5**	3 **3.3**	6 **6.3**	mV
TCV_{OS}	Input Offset Voltage Average Drift		1.3				μV/°C
I_B	Input Bias Current		0.002	20 **100**	**4**	**4**	pA max
I_{OS}	Input Offset Current		0.001	20 **100**	**2**	**2**	pA max
R_{IN}	Input Resistance		>1				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70 **68**	70 **68**	63 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	70 **68**	70 **68**	63 **61**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84 **82**	84 **83**	74 **73**	dB min
V_{CM}	Input Common Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V min
A_V	Large Signal Voltage Gain	Sourcing $R_L = 100\ k\Omega$ (Note 5)	1000	400 **250**	400 **300**	300 **200**	V/mV min
		Sinking $R_L = 100\ k\Omega$ (Note 5)	500	180 **70**	180 **120**	90 **70**	V/mV min
		Sourcing $R_L = 5\ k\Omega$ (Note 5)	1000	200 **150**	200 **160**	100 **80**	V/mV min
		Sinking $R_L = 5\ k\Omega$ (Note 5)	250	100 **35**	100 **60**	50 **40**	V/mV min

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.970 **4.950**	4.970 **4.950**	4.940 **4.910**	V min
			0.004	0.030 **0.050**	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 5V$ $R_L = 5\ k\Omega$ to 2.5V	4.940	4.850 **4.750**	4.850 **4.750**	4.750 **4.650**	V min
			0.040	0.150 **0.250**	0.150 **0.250**	0.250 **0.350**	V max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.970	14.920 **14.880**	14.920 **14.880**	14.880 **14.820**	V min
			0.007	0.030 **0.050**	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 15V$ $R_L = 5\ k\Omega$ to 7.5V	14.840	14.680 **14.600**	14.680 **14.600**	14.580 **14.480**	V min
			0.110	0.220 **0.300**	0.220 **0.300**	0.320 **0.400**	V max
I_O	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **12**	16 **14**	13 **11**	mA min
		Sinking, $V_O = 5V$	21	16 **12**	16 **14**	13 **11**	mA min
I_O	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19 **19**	28 **25**	23 **20**	mA min
		Sinking, $V_O = 13V$ (Note 9)	39	19 **19**	28 **24**	23 **19**	mA min
I_S	Supply Current	$V^+ = 5V$, $V_O = 1.5V$	55	60 **70**	60 **70**	70 **85**	μA max
		$V^+ = 15V$, $V_O = 1.5V$	58	75 **85**	75 **85**	90 **105**	μA max

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
SR	Slew Rate	(Note 6)	0.11	0.07 **0.04**	0.07 **0.05**	0.05 **0.03**	V/μs min
GBW	Gain-Bandwidth Product		350				kHz
ϕm	Phase Margin		50				Deg
G_M	Gain Margin		17				dB
e_n	Input Referred Voltage Noise	F = 1 kHz	42				$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise	F = 1 kHz	0.0002				$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -10$ $R_L = 100\ k\Omega$, $V_O = 8\ V_{PP}$ $V^+ = 15V$	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For sourcing tests, $7.5V \le V_O \le 11.5V$. For sinking tests, $2.5V \le V_O \le 7.5V$.

Note 6: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

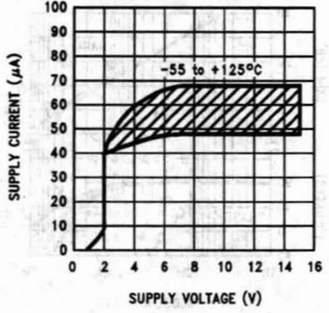
Note 7: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 8: All numbers apply for packages soldered directly into a PC board.

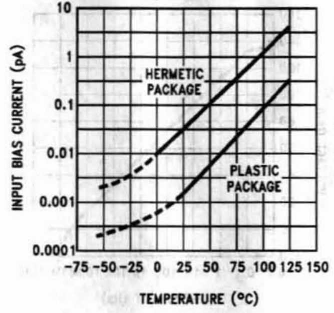
Note 9: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

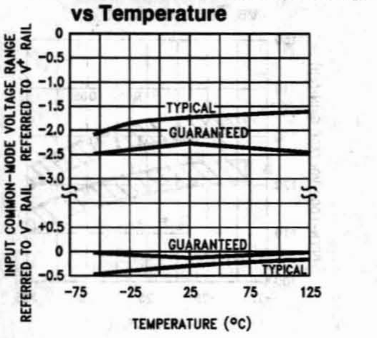
Supply Current vs Supply Voltage



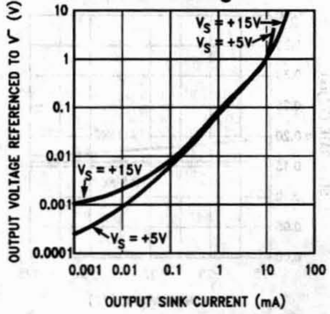
Input Bias Current vs Temperature



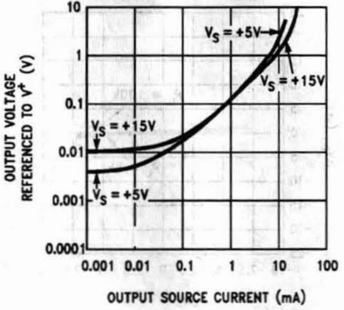
Common-Mode Voltage Range vs Temperature



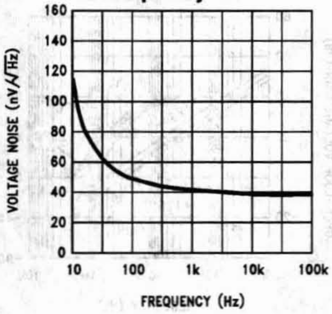
Output Characteristics Current Sinking



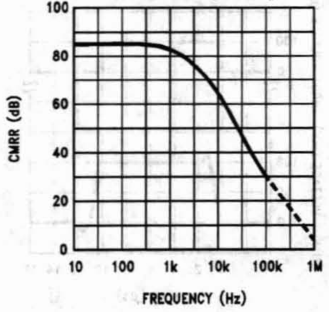
Output Characteristics Current Sourcing



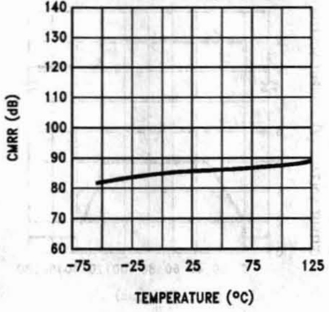
Input Voltage Noise vs Frequency



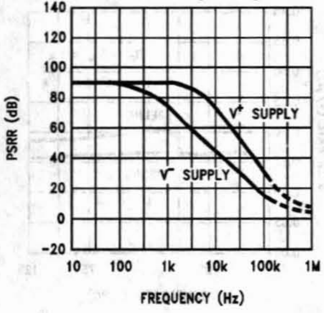
CMRR vs Frequency



CMRR vs Temperature



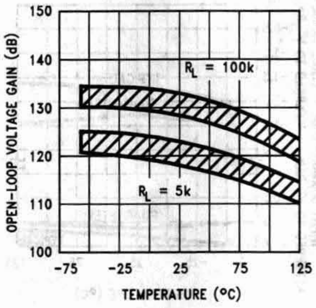
Power Supply Rejection Ratio vs Frequency



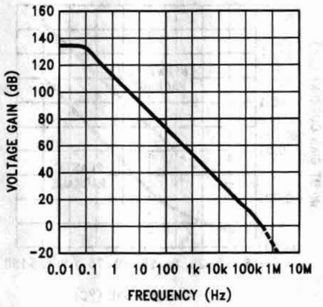
TL/H/11227–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

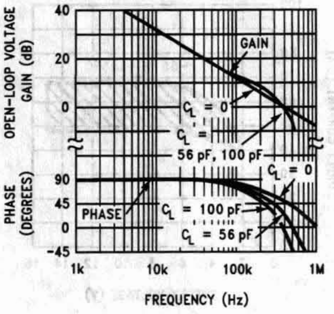
Open-Loop Voltage Gain vs Temperature



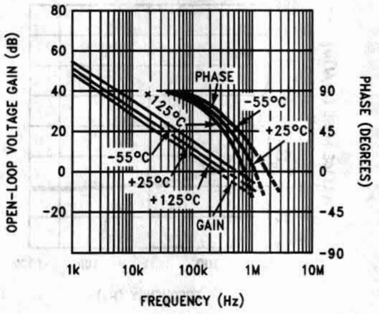
Open-Loop Frequency Response



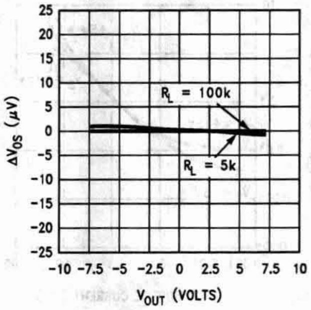
Gain and Phase Responses vs Load Capacitance



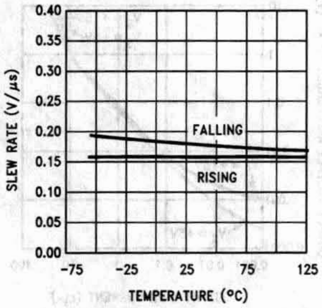
Gain and Phase Responses vs Temperature



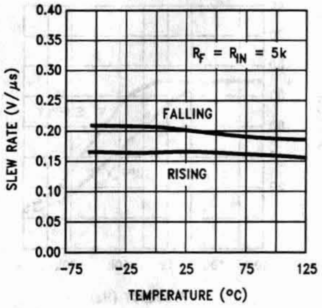
Gain Error (V_{OS} vs V_{OUT})



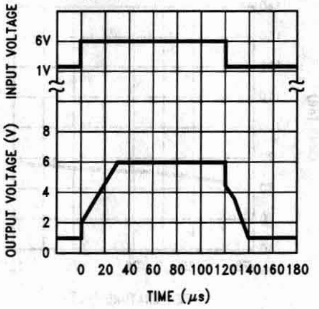
Non-Inverting Slew Rate vs Temperature



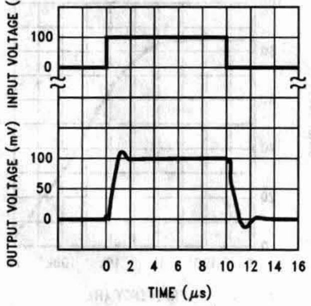
Inverting Slew Rate vs Temperature



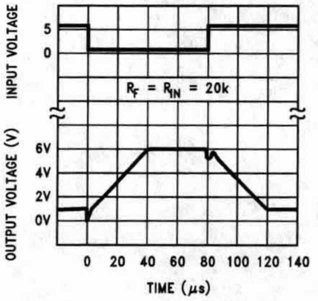
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



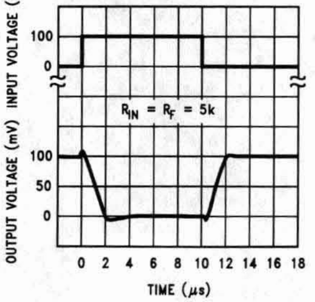
Non-Inverting Small Signal Pulse Response ($A_V = +1$)



Inverting Large-Signal Pulse Response



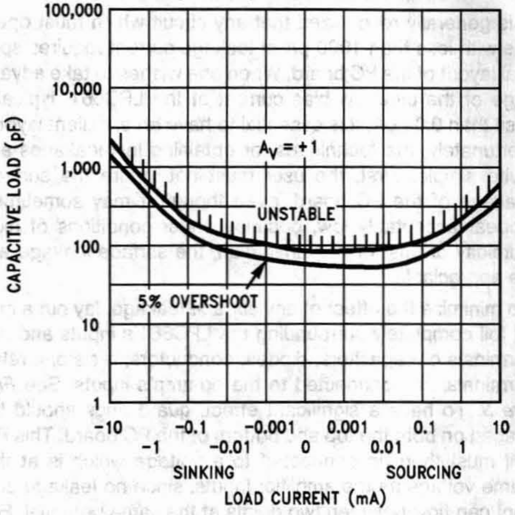
Inverting Small-Signal Pulse Response



TL/H/11227–3

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ (Continued)

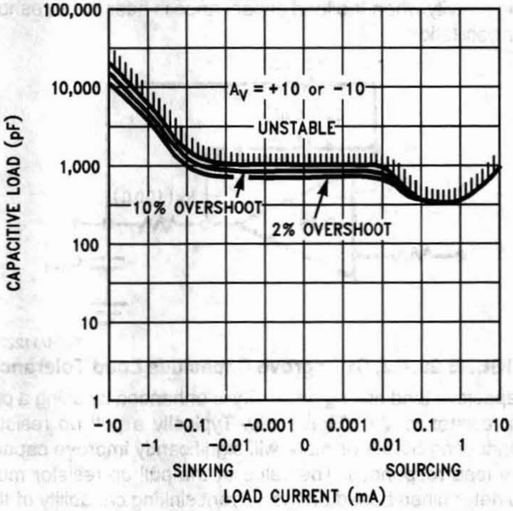
Stability vs Capacitive Load



TL/H/11227-4

Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Stability vs Capacitive Load



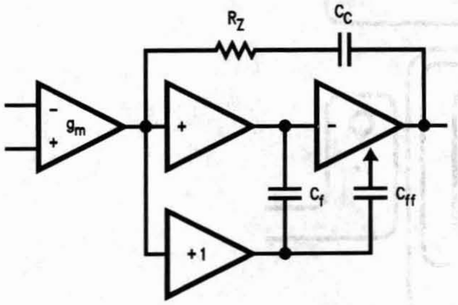
TL/H/11227-5

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC661 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/11227-6

FIGURE 1. LPC661 Circuit Topology

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

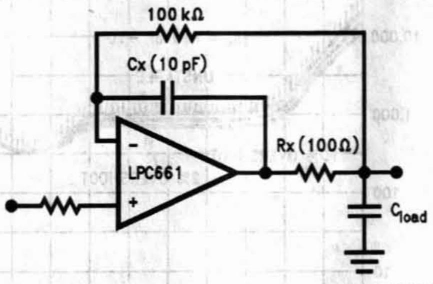
CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC661 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

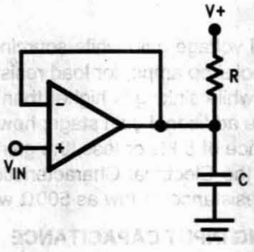
operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/11227-7

FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 2b)*. Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



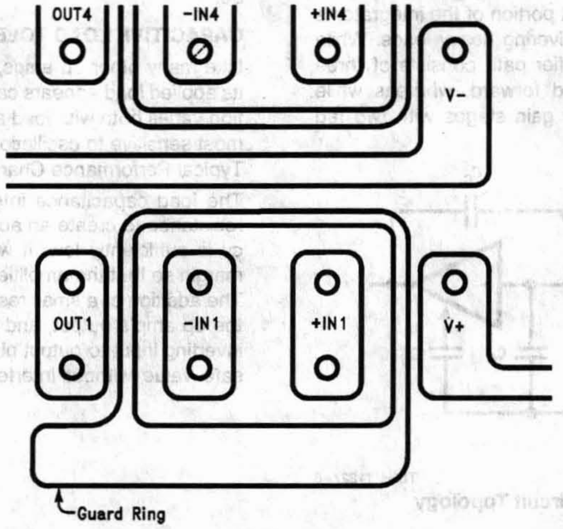
TL/H/11227-24

FIGURE 2b. Compensating for Large Capacitive Loads with A Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC661, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

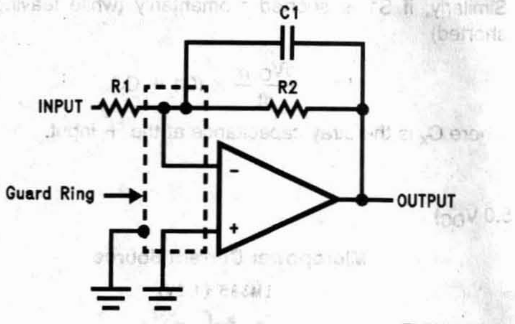
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC661's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 4d*.



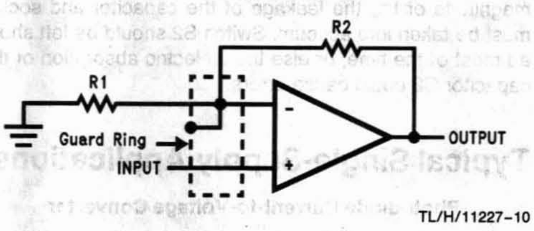
TL/H/11227-8

FIGURE 3. Example of Guard Ring in P.C. Board Layout, Using the LPC660

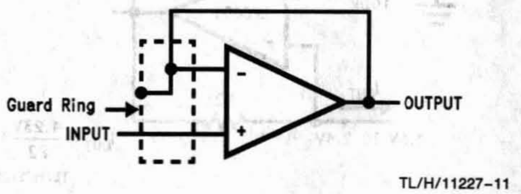
Application Hints (Continued)


C1
R1
R2
INPUT
Guard Ring
OUTPUT
TL/H/11227-9

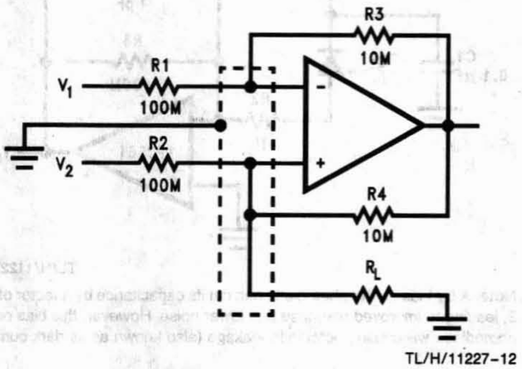
(a) Inverting Amplifier


R2
R1
Guard Ring
INPUT
OUTPUT
TL/H/11227-10

(b) Non-Inverting Amplifier


Guard Ring
INPUT
OUTPUT
TL/H/11227-11

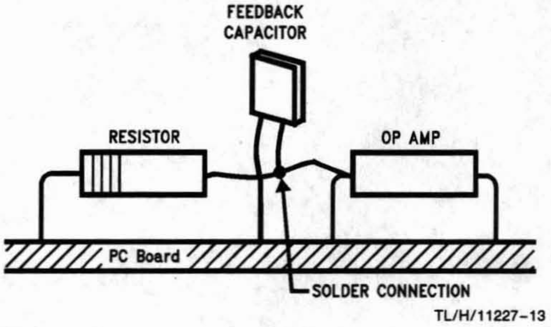
(c) Follower


R3
10M
R1
V_1
100M
R2
V_2
100M
R4
10M
R_L
TL/H/11227-12

(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.


FEEDBACK CAPACITOR
RESISTOR
OP AMP
PC Board
SOLDER CONNECTION
TL/H/11227-13

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 6* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

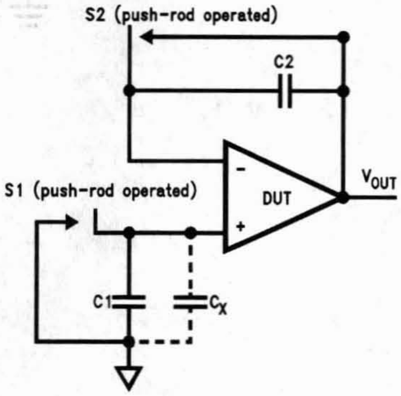

S2 (push-rod operated)
C2
S1 (push-rod operated)
DUT
V_{OUT}
C1
C_X
TL/H/11227-14

FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

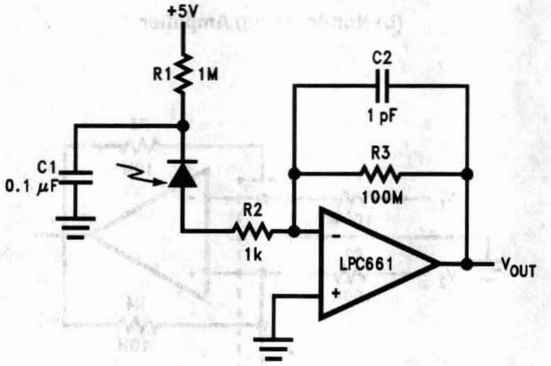
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Photodiode Current-to-Voltage Converter

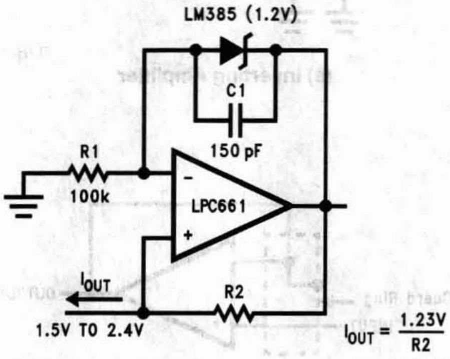


+5V
R1
1M
C2
1 pF
R3
100M
C1
0.1 µF
R2
1k
LPC661
V_OUT

TL/H/11227–15

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Micropower Current Source

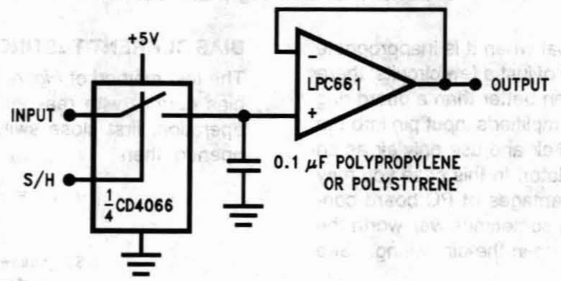


LM385 (1.2V)
C1
150 pF
R1
100k
LPC661
I_OUT
R2
1.5V TO 2.4V
I_OUT = 1.23V / R2

TL/H/11227–16

(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold

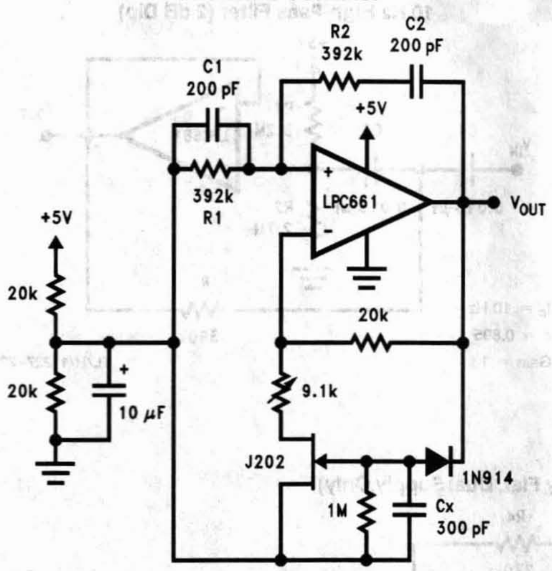


+5V
INPUT
S/H
1/4 CD4066
LPC661
OUTPUT
0.1 µF POLYPROPYLENE OR POLYSTYRENE

TL/H/11227–17

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Sine-Wave Oscillator


R2
392k
C2
200 pF
C1
200 pF
+5V
392k
R1
LPC661
V_{OUT}
+5V
20k
20k
10 µF
20k
9.1k
J202
1N914
1M
Cx
300 pF

TL/H/11227-18

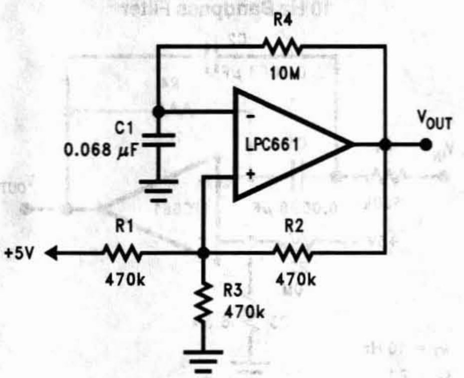
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

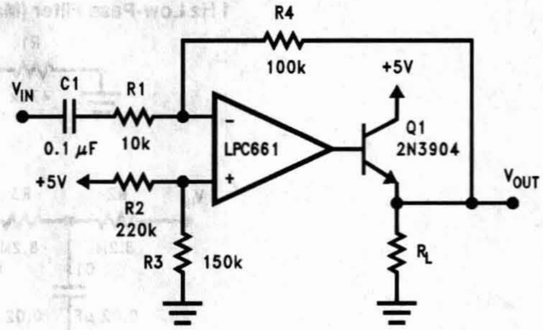
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator


R4
10M
C1
0.068 µF
LPC661
V_{OUT}
R1
R2
+5V
470k
470k
R3
470k

TL/H/11227-19

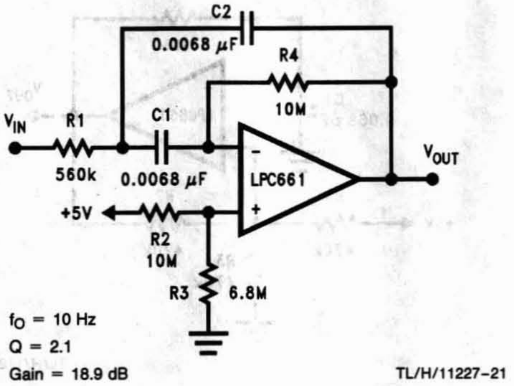
Power Amplifier


R4
100k
+5V
V_{IN}
C1
R1
0.1 µF
10k
LPC661
Q1
2N3904
+5V
R2
220k
R3
150k
V_{OUT}
R_L

TL/H/11227-20

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

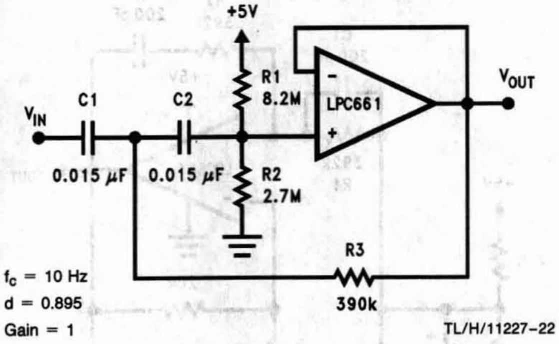
10 Hz Bandpass Filter


C2
0.0068 μF
R4
10M
V_{IN}
R1
560k
C1
0.0068 μF
LPC661
V_{OUT}
+5V
R2
10M
R3
6.8M

$f_O = 10$ Hz
Q = 2.1
Gain = 18.9 dB

TL/H/11227-21

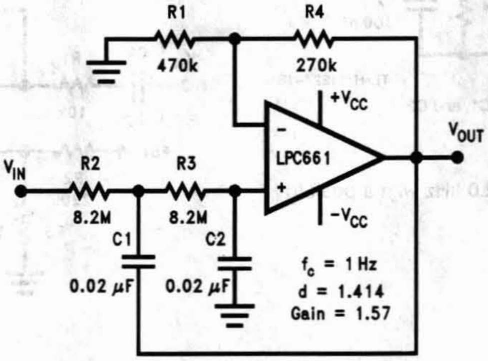
10 Hz High-Pass Filter (2 dB Dip)


+5V
V_{IN}
C1
0.015 μF
C2
0.015 μF
R1
8.2M
R2
2.7M
LPC661
V_{OUT}
R3
390k

$f_c = 10$ Hz
d = 0.895
Gain = 1

TL/H/11227-22

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)


R1
470k
R4
270k
+V_{CC}
V_{OUT}
LPC661
V_{IN}
R2
8.2M
R3
8.2M
-V_{CC}
C1
0.02 μF
C2
0.02 μF

$f_c = 1$ Hz
d = 1.414
Gain = 1.57

TL/H/11227-23

National Semiconductor

LPC662
Low Power CMOS Dual Operational Amplifier

General Description

The LPC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltage from +5V to +15V, rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is typically less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC660 datasheet for a Quad CMOS operational amplifier and LPC661 for a single CMOS operational amplifier with these same features.

Applications

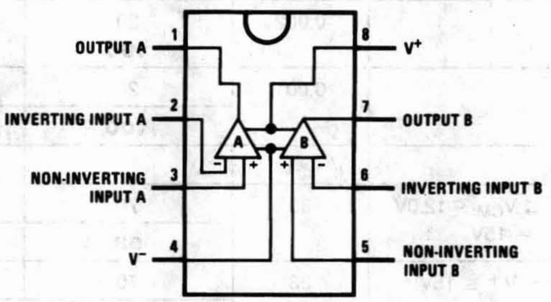
- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Features

■ Rail-to-rail output swing	
■ Micropower operation (<0.5 mW)	
■ Specified for 100 kΩ and 5 kΩ loads	
■ High voltage gain	120 dB
■ Low input offset voltage	3 mV
■ Low offset voltage drift	1.3 μV/°C
■ Ultra low input bias current	2 fA
■ Input common-mode includes GND	
■ Operating range from +5V to +15V	
■ Low distortion	0.01% at 1 kHz
■ Slew rate	0.11 V/μs
■ Full military temperature range available	

Connection Diagram

8-Pin DIP/SO



TL/H/10548–1

Top View

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military	Industrial		
8-Pin Side Brazed Ceramic DIP	LPC662AMD		D08C	Rail
8-Pin Small Outline		LPC662AIM or LPC662IM	M08A	Rail Tape and Reel
8-Pin Molded DIP		LPC662AIN or LPC662IN	N08E	Rail
8-Pin Ceramic DIP	LPC662AMJ/883		J08A	Rail

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 1)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Rating (C = 100 pF, R = 1.5 kΩ)	1000V
Power Dissipation	(Note 2)
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$

Operating Ratings (Note 3)

Temperature Range	
LPC662AMJ/883	$-55°C \le T_J \le +125°C$
LPC662AM	$-55°C \le T_J \le +125°C$
LPC662AI	$-40°C \le T_J \le +85°C$
LPC662I	$-40°C \le T_J \le +85°C$
Supply Range	4.75V to 15.5V
Power Dissipation	(Note 9)
Thermal Resistance (θ_{JA}) (Note 10)	
8-Pin Ceramic DIP	100°C/W
8-Pin Molded DIP	101°C/W
8-Pin SO	165°C/W
8-Pin Side Brazed Ceramic DIP	100°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LPC662AM LPC662AMJ/883 Limit (Notes 4, 8)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Input Offset Voltage		1	3	3	6	mV
			3.5	**3.3**	**6.3**	max
Input Offset Voltage Average Drift		1.3				μV/°C
Input Bias Current		0.002	20			pA
			100	**4**	**4**	max
Input Offset Current		0.001	20			pA
			100	**2**	**2**	max
Input Resistance		>1				Tera Ω
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70	70	63	dB
			68	**68**	**61**	min
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70	70	63	dB
			68	**68**	**61**	min
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84	84	74	dB
			82	**83**	**73**	min
Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB	−0.4	−0.1	−0.1	−0.1	V
			0	**0**	**0**	max
		$V^+ - 1.9$	$V^+ - 2.3$	$V^+ - 2.3$	$V^+ - 2.3$	V
			$V^+ - 2.6$	**$V^+ - 2.5$**	**$V^+ - 2.5$**	min

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified. (Continued)

Parameter	Conditions	Typ	LPC662AM LPC662AMJ/883 Limit (Notes 4, 8)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Large Signal Voltage Gain	R_L = 100 kΩ (Note 5) Sourcing	1000	400	400	300	V/mV min
			250	**300**	**200**	
	Sinking	500	180	180	90	V/mV min
			70	**120**	**70**	
	R_L = 5 kΩ (Note 5) Sourcing	1000	200	200	100	V/mV min
			150	**160**	**80**	
	Sinking	250	100	100	50	V/mV min
			35	**60**	**40**	
Output Swing	V^+ = 5V R_L = 100 kΩ to $V^+/2$	4.987	4.970	4.970	4.940	V min
			4.950	**4.950**	**4.910**	
		0.004	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	V^+ = 5V R_L = 5 kΩ to $V^+/2$	4.940	4.850	4.850	4.750	V min
			4.750	**4.750**	**4.650**	
		0.040	0.150	0.150	0.250	V max
			0.250	**0.250**	**0.350**	
	V^+ = 15V R_L = 100 kΩ to $V^+/2$	14.970	14.920	14.920	14.880	V min
			14.880	**14.880**	**14.820**	
		0.007	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	V^+ = 15V R_L = 5 kΩ to $V^+/2$	14.840	14.680	14.680	14.580	V min
			14.600	**14.600**	**14.480**	
		0.110	0.220	0.220	0.320	V max
			0.300	**0.300**	**0.400**	
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16	16	13	mA min
			12	**14**	**11**	
	Sinking, V_O = 5V	21	16	16	13	mA min
			12	**14**	**11**	
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	19	28	23	mA min
			19	**25**	**20**	
	Sinking, V_O = 13V (Note 11)	39	19	28	23	mA min
			19	**24**	**19**	
Supply Current	Both Amplifiers V_O = 1.5V	86	120	120	140	μA max
			145	**140**	**160**	

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LPC662AM LPC662AMJ/883 Limit (Notes 4, 8)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Slew Rate	(Note 6)	0.11	0.07	0.07	0.05	V/µs
			0.04	**0.05**	**0.03**	min
Gain-Bandwidth Product		0.35				MHz
Phase Margin		50				Deg
Gain Margin		17				dB
Amp-to-Amp Isolation	(Note 7)	130				dB
Input Referred Voltage Noise	F = 1 kHz	42				nV/$\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{Hz}$
Total Harmonic Distortion	F = 1 kHz, $A_V = -10$, $V^+ = 15V$ $R_L = 100\ k\Omega$, $V_O = 8\ V_{PP}$	0.01				%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation of any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 6: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

Note 8: A military RETS electrical test specification is available on request. At the time of printing, the LPC662AMJ/883 RETS specification complied fully with the **boldface** limits in this column. The LPC662AMJ/883 may also be procured to a Standard Military Drawing specification.

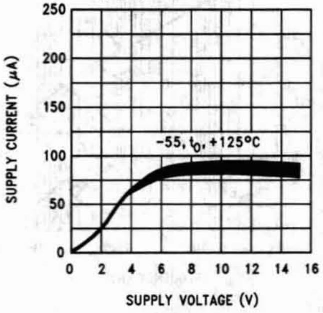
Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

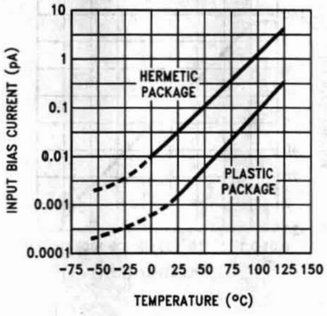
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

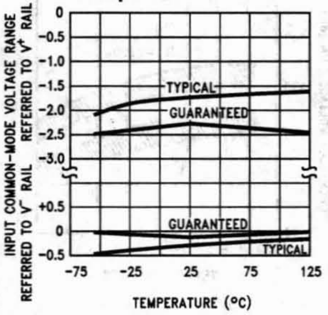
Supply Current vs Supply Voltage



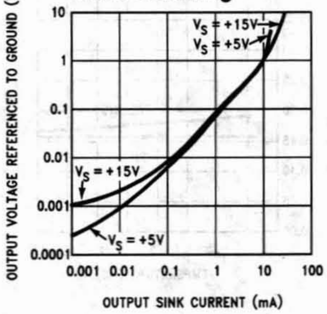
Input Bias Current vs Temperature



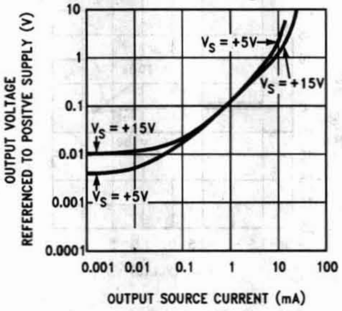
Input Common-Mode Voltage Range vs Temperature



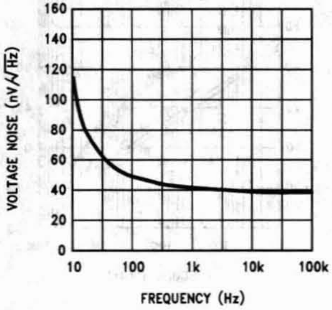
Output Characteristics Current Sinking



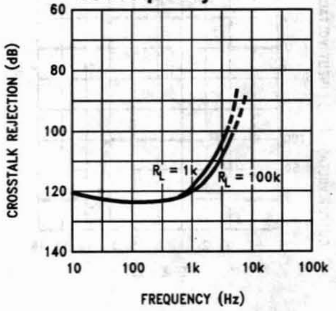
Output Characteristics Current Sourcing



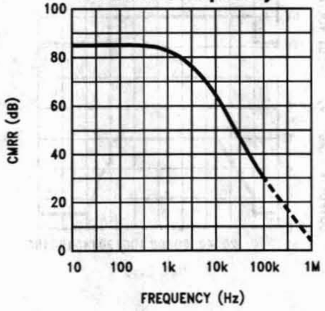
Input Voltage Noise vs Frequency



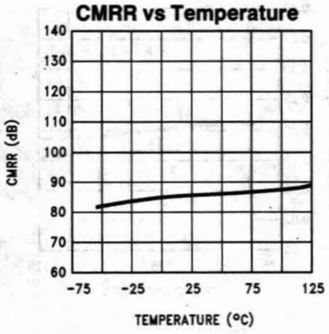
Crosstalk Rejection vs Frequency



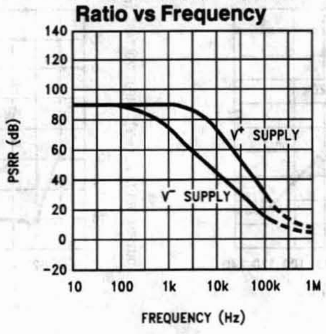
CMRR vs Frequency



CMRR vs Temperature



Power Supply Rejection Ratio vs Frequency



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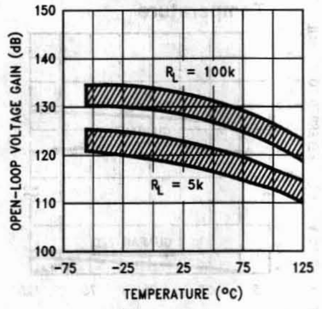
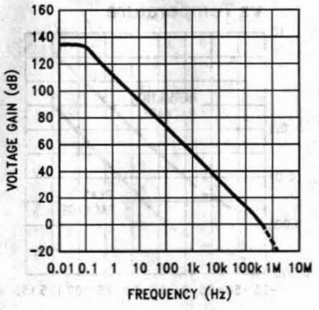
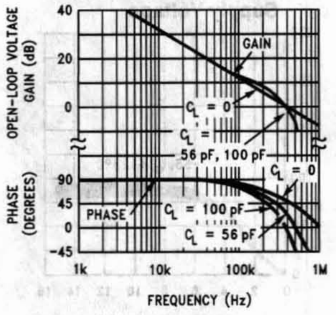
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)



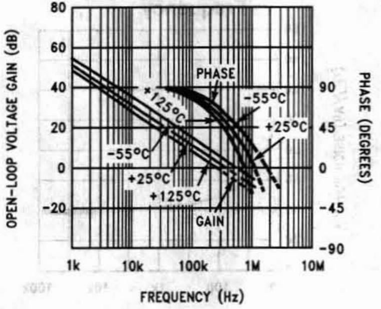
Open-Loop Voltage Gain vs Temperature



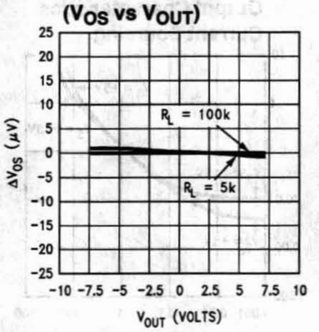
Open-Loop Frequency Response



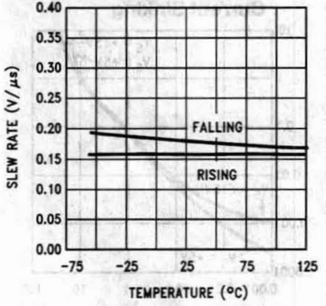
Gain and Phase Responses vs Load Capacitance



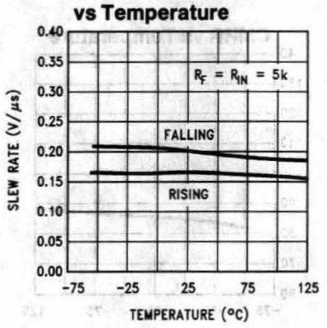
Gain and Phase Responses vs Temperature



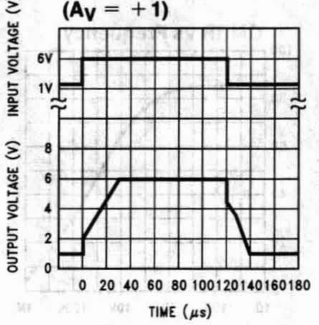
Gain Error (V_{OS} vs V_{OUT})



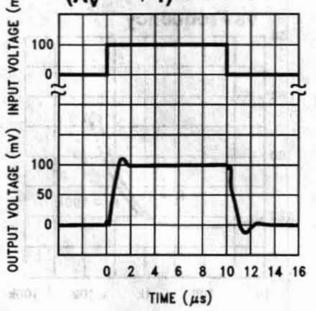
Non-Inverting Slew Rate vs Temperature



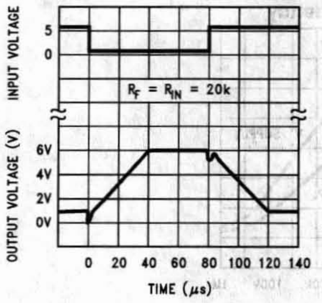
Inverting Slew Rate vs Temperature



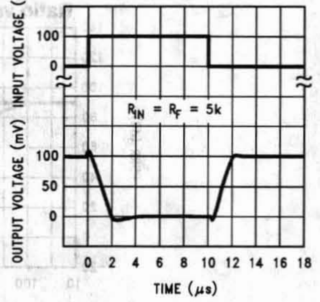
Large-Signal Pulse Non-Inverting Response (A_V = +1)



Non-Inverting Small Signal Pulse Response (A_V = +1)



Inverting Large-Signal Pulse Response



Inverting Small-Signal Pulse Response

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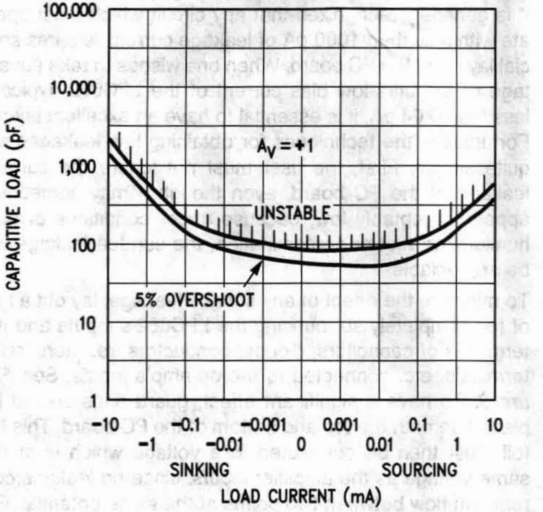
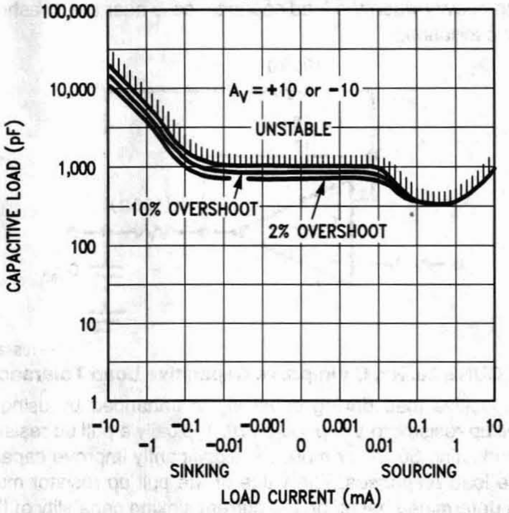
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ (Continued)

Stability vs Capacitive Load



TL/H/10548–4

Stability vs Capacitive Load



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Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC662 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

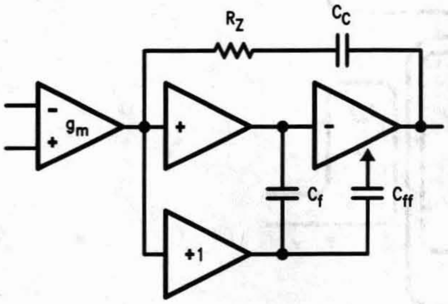

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FIGURE 1. LPC662 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC662 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

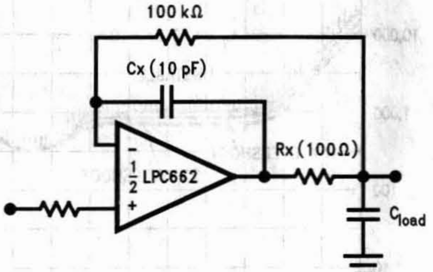

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FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V+ *(Figure 2b)*. Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

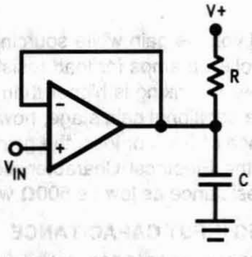

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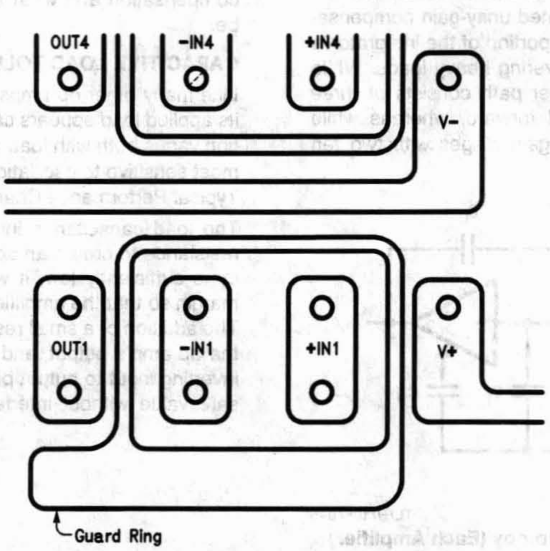
FIGURE 2b. Compensating for Large Capacitive Loads with A Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

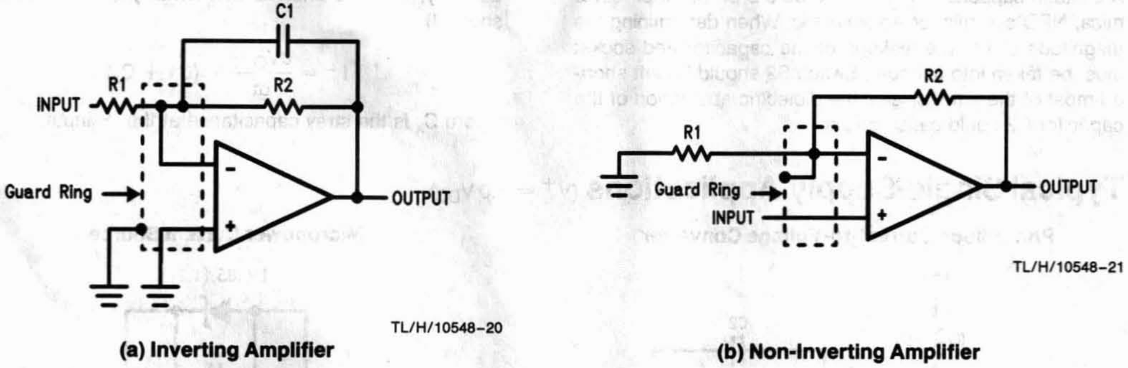
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC662's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 3.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC662's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 4d.*



TL/H/10548–19

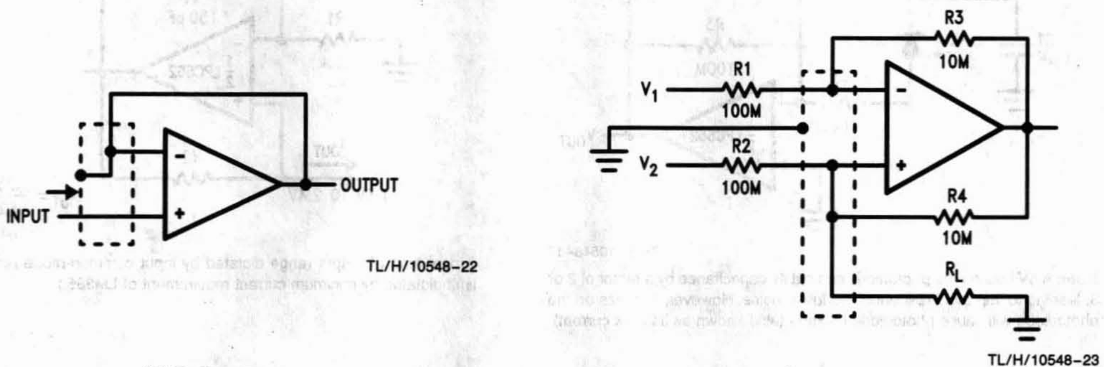
FIGURE 3. Example of Guard Ring in P.C. Board Layout, using the LPC660

Application Hints (Continued)


C1
R1
R2
INPUT
Guard Ring
OUTPUT
TL/H/10548-20
R2
R1
Guard Ring
INPUT
OUTPUT
TL/H/10548-21

(a) Inverting Amplifier

(b) Non-Inverting Amplifier

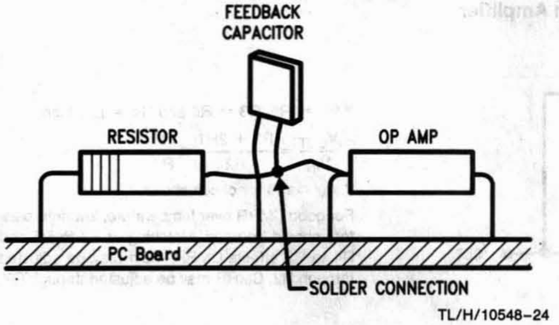

INPUT
OUTPUT
TL/H/10548-22
R3
10M
V1
R1
100M
R2
V2
100M
R4
10M
RL
TL/H/10548-23

(c) Follower

(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.


FEEDBACK CAPACITOR
RESISTOR
OP AMP
PC Board
SOLDER CONNECTION
TL/H/10548-24

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 6* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

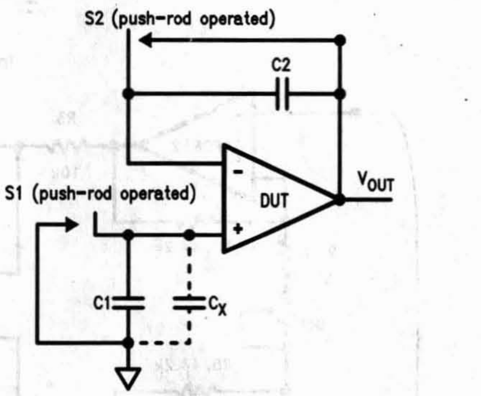

S2 (push-rod operated)
C2
S1 (push-rod operated)
DUT
VOUT
C1
CX
TL/H/10548-25

FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

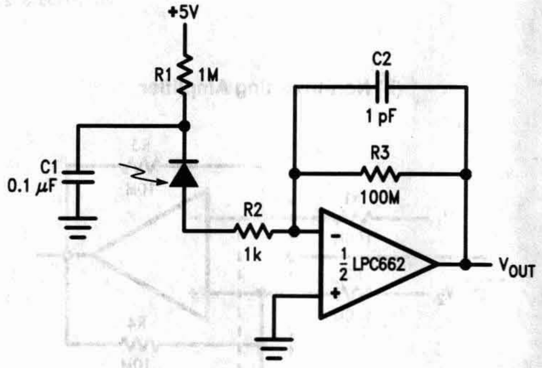
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Photodiode Current-to-Voltage Converter

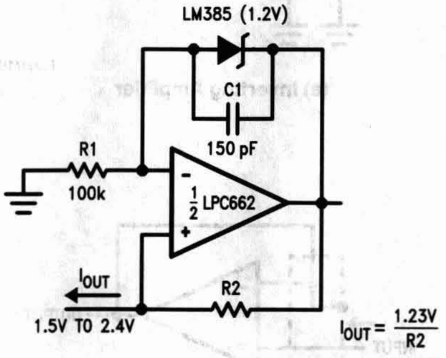


+5V
R1
1M
C2
1 pF
R3
100M
C1
0.1 µF
R2
1k
-
+
½ LPC662
VOUT

TL/H/10548-17

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Micropower Current Source



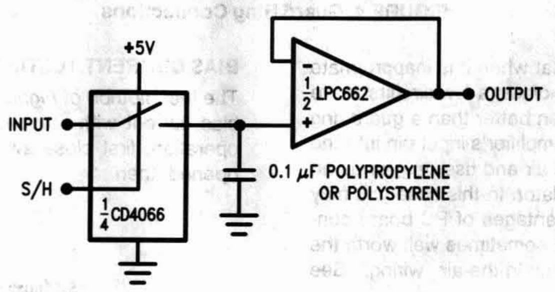
LM385 (1.2V)
C1
150 pF
R1
100k
-
+
½ LPC662
IOUT
R2
1.5V TO 2.4V

$$I_{OUT} = \frac{1.23V}{R2}$$

TL/H/10548-18

(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

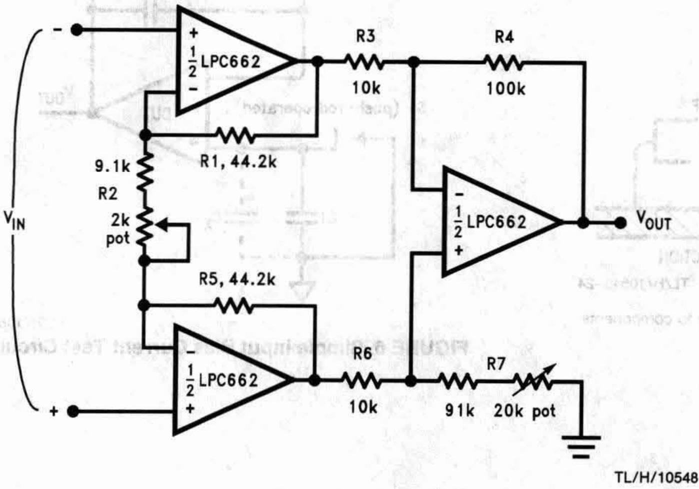
Low-Leakage Sample-and-Hold



+5V
INPUT
S/H
¼ CD4066
-
+
½ LPC662
OUTPUT
0.1 µF POLYPROPYLENE
OR POLYSTYRENE

TL/H/10548-8

Instrumentation Amplifier



-
+
½ LPC662
R3
10k
R4
100k
R1, 44.2k
9.1k
R2
2k pot
VIN
VOUT
R5, 44.2k
R6
10k
R7
91k
20k pot

If R1 = R5, R3 = R6 and R4 = R7; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

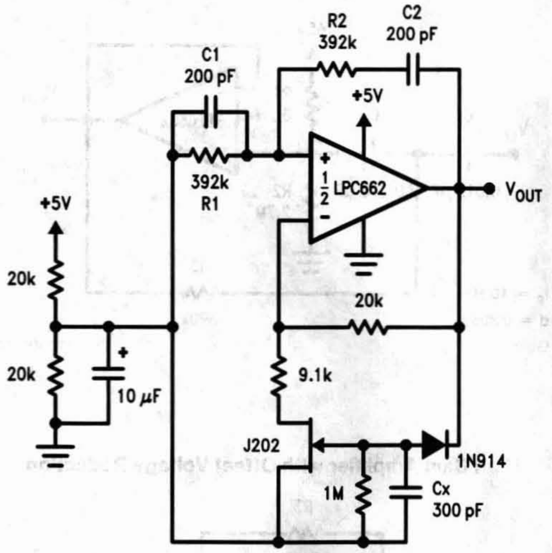
$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

TL/H/10548-9

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Sine-Wave Oscillator



R2
392k
C2
200 pF
C1
200 pF
+5V
392k
R1
1/2 LPC662
V_{OUT}
+5V
20k
20k
10 µF
20k
9.1k
J202
1N914
1M
Cx
300 pF

TL/H/10548–10

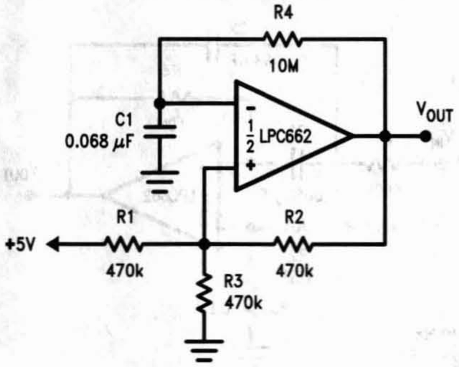
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

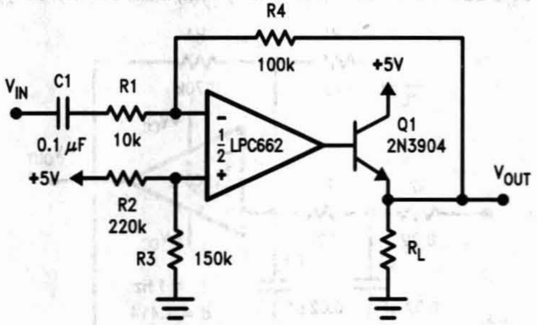
1 Hz Square-Wave Oscillator



R4
10M
C1
0.068 µF
1/2 LPC662
V_OUT
R1
R2
+5V
470k
470k
R3
470k

TL/H/10548–11

Power Amplifier

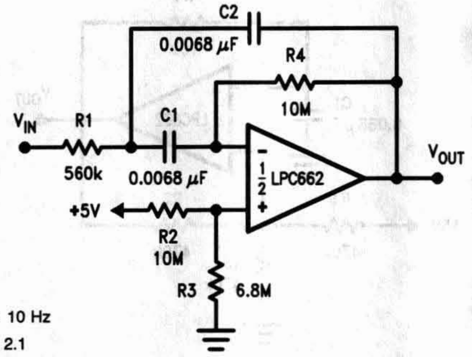


R4
100k
+5V
V_IN
C1
R1
0.1 µF
10k
1/2 LPC662
Q1
2N3904
+5V
V_OUT
R2
220k
R3
150k
R_L

TL/H/10548–12

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

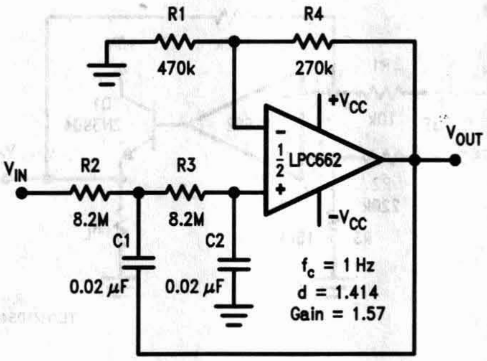
10 Hz Bandpass Filter


C2
0.0068 µF
R4
10M
V_IN
R1
560k
C1
0.0068 µF
−
1/2 LPC662
+
V_OUT
+5V
R2
10M
R3
6.8M

$f_O = 10$ Hz
Q = 2.1
Gain = −8.8

TL/H/10548–13

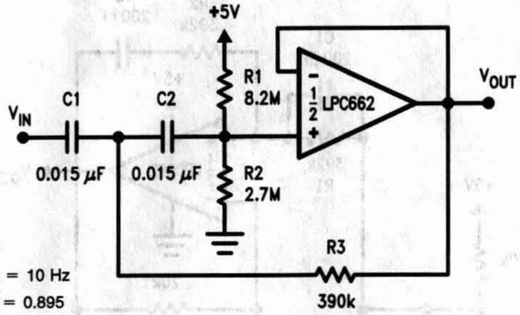
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)


R1
470k
R4
270k
+V_CC
−
1/2 LPC662
+
−V_CC
V_OUT
V_IN
R2
8.2M
R3
8.2M
C1
0.02 µF
C2
0.02 µF

$f_c = 1$ Hz
d = 1.414
Gain = 1.57

TL/H/10548–15

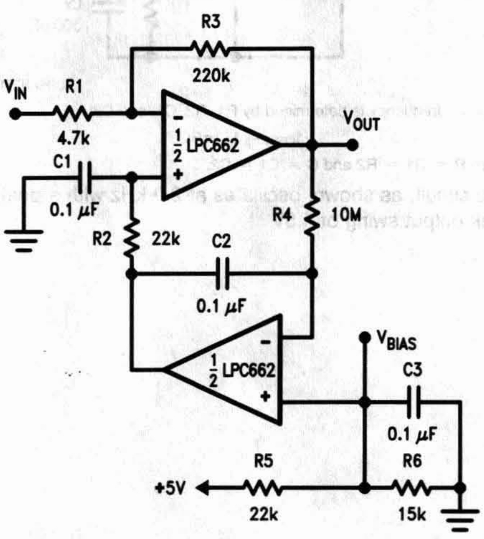
10 Hz High-Pass Filter (2 dB Dip)


+5V
R1
8.2M
−
1/2 LPC662
+
V_OUT
V_IN
C1
0.015 µF
C2
0.015 µF
R2
2.7M
R3
390k

$f_c = 10$ Hz
d = 0.895
Gain = 1

TL/H/10548–14

High Gain Amplifier with Offset Voltage Reduction


R3
220k
V_IN
R1
4.7k
−
1/2 LPC662
+
V_OUT
C1
0.1 µF
R2
22k
R4
10M
C2
0.1 µF
−
1/2 LPC662
+
V_BIAS
C3
0.1 µF
R5
22k
R6
15k
+5V

Gain = −46.8

TL/H/10548–16

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

National Semiconductor

OP-07 Low Offset, Low Drift Operational Amplifier

General Description

The OP-07 has very low input offset voltage which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current and high open-loop gain. The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain applications.

The wide input voltage range of ±13V minimum combined with high CMRR of 110 dB and high input impedance provide high accuracy in the non-inverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variation in temperature is excellent.

The OP-07 is available in TO-99 metal can, ceramic or molded DIP.

For improved specifications, see the LM607.

Features

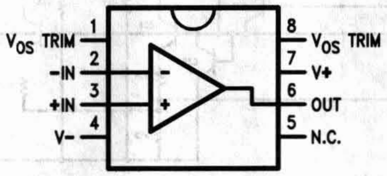
■ Low V_{OS}	75 μV Max
■ Low V_{OS} Drift	0.6 μV/°C Max
■ Ultra-Stable vs Time	1.0 μV/Month Max
■ Low Noise	0.6 μVp-p Max
■ Wide Input Voltage Range	±14V
■ Wide Supply Voltage Range	±3V to ±18V
■ Fits 725/108A/308A, 741, AD510 Sockets	
■ Replaces the μA714	

Applications

- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Precision Reference Buffer
- Analog Computing Functions

Connection Diagram

Dual-In-Line Package



TL/H/10550–1

See NS Package Number N08E

Ordering Information

$T_A = 25°C$ V_{OS}Max (μV)	N08E Plastic	Operating Temperature Range
75	OP07EP	COM
150	OP07CP	COM
150	OP07DP	COM

*Also available per SMD #8203602

Absolute Maximum Ratings

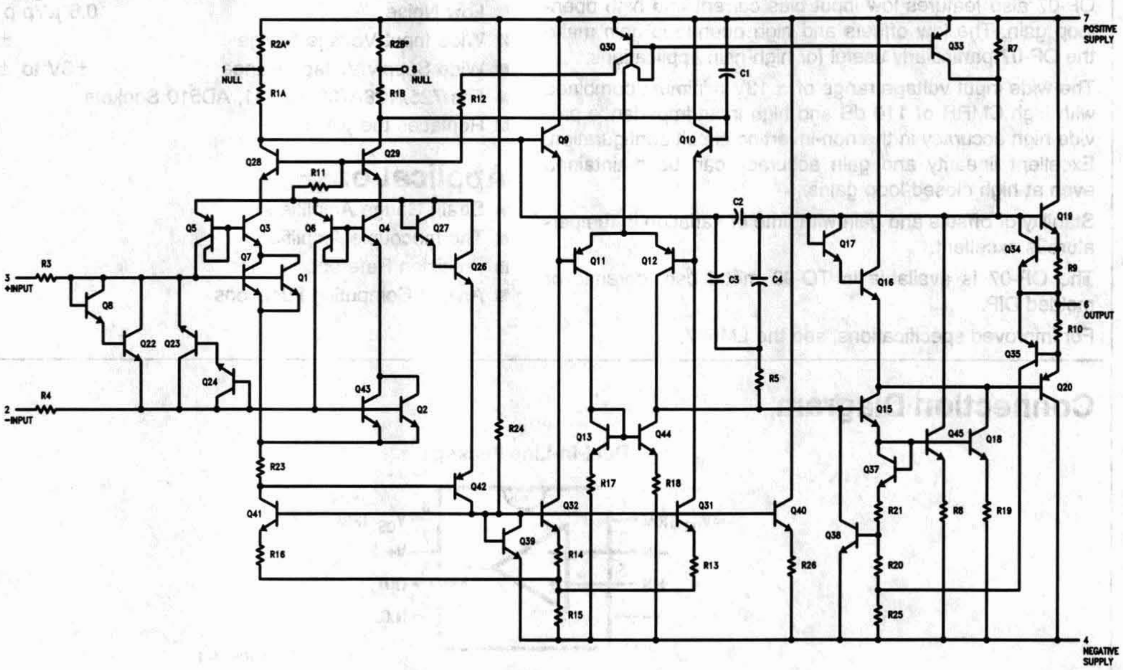
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Internal Power Dissipation (Note 5)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 6)	±22V
Output Short-Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	260°C
Junction Temperature	−65°C to +150°C

Operating Temperature Range

OP-07E, OP-07C, OP-07D	0°C to +70°C

Simplified Schematic


R2A*
R2B*
1 NULL
8 NULL
R1A
R1B
R12
Q30
C1
Q33
R7
7 POSITIVE SUPPLY
Q9
Q10
Q28
Q29
R11
C2
Q5
Q3
Q6
Q4
Q27
Q7
Q1
Q26
Q11
Q12
C3
C4
Q17
Q19
Q34
R9
Q16
6 OUTPUT
R10
Q35
Q20
R3
3 +INPUT
Q8
Q22
Q23
Q24
R5
Q15
R4
2 −INPUT
Q43
Q2
R24
Q13
Q44
Q45
Q18
R23
Q37
Q42
R17
R18
Q41
Q32
Q31
Q40
R21
R8
R19
Q38
Q39
R16
R14
R13
R26
R20
R15
R25
4 NEGATIVE SUPPLY

TL/H/10550-3

*R2A and R2B are electronically trimmed on chip at the factory for minimum offset voltage.

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $0°C \le T_A \le 70°C$

Symbol	Parameter	Conditions	OP-07E			OP-07C			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1)		30 **45**	75 **130**		60 **85**	150 **250**	µV
$V_{OS/t}$	Long-Term V_{OS} Stability	(Note 2)		0.3	1.5		0.4	2.0	µV/Mo
I_{OS}	Input Offset Current			0.5 **0.9**	3.8 **5.3**		0.8 **1.6**	6.0 **8.0**	nA
I_B	Input Bias Current			±1.2 **±1.5**	±4.0 **±5.5**		±1.8 **±2.2**	±7.0 **±9.0**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6		0.38	0.65	µV$_{p-p}$
e_n	Input Noise Voltage Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	nV/√Hz
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30		15	35	pA$_{p-p}$
i_n	Input Noise Current Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
R_{IN}	Input Resistance Differential-Mode	(Note 4)	15	50		8	33		MΩ
R_{INCM}	Input Resistance Common-Mode			160			120		GΩ
IVR	Input Voltage Range		±13.0	±14.0		±13	±14		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	106 **103**	123 **123**		100 **97**	120 **120**		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$ $V_S = \pm 3V$ to $\pm 18V$		5 **7**	20 **32**		7 **10**	32 **51**	µV/V
A_{VO}	Large Signal Voltage Gain	$R_L \ge 2 k\Omega$, $V_O = \pm 10V$ $R_L \ge 2 k\Omega$ $R_L \ge 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 4)	200 **180** 150	500 **450** 400		120 **100** 100	400 **400** 400		V/mV
V_O	Output Voltage Swing	$R_L \ge 10 k\Omega$ $R_L \ge 2 k\Omega$ $R_L \ge 2 k\Omega$ $R_L \ge 1 k\Omega$	±12.5 ±12.0 **±12.0** ±10.5	±13.0 ±12.8 **±12.6** ±12.0		±12.0 ±11.5 **±11.0**	±13.0 ±12.8 **±12.6** ±12.0		V
SR	Slew Rate	$R_L \ge 2 k\Omega$ (Note 3)	0.1	0.3		0.1	0.3		V/µs
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		0.4	0.6		MHz
R_O	Output Resistance	$V_O = 0$, $I_O = 0$		60			60		Ω
P_d	Power Consumption	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load		75 4	120 6		80 4	150 8	mW
	Offset Adj. Range	$R_P = 20 k\Omega$		±4			±4		mV
TCV_{OS}	Average Input Offset Voltage Drift Without External Trim	(Note 4)		**0.3**	**1.3**		**0.5**	**1.8**	µV/°C
TCV_{OSn}	With External Trim	$R_P = 20 k\Omega$ (Note 4)		**0.3**	**1.3**		**0.4**	**1.6**	
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**8**	**35**		**12**	**50**	pA/°C
TCI_B	Average Input Bias Current Drift	(Note 3)		**13**	**35**		**18**	**50**	pA/°C

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Conditions	OP-07D			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1)		60 **85**	150 **250**	μV
$V_{OS/t}$	Long-Term V_{OS} Stability	(Note 2)		0.5	3.0	μV/Mo
I_{OS}	Input Offset Current			0.8 **1.6**	6.0 **8.0**	nA
I_B	Input Bias Current			±2.0 **±3.0**	±12.0 **±14.0**	nA
$e_{np\text{-}p}$	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.38	0.65	μVp-p
e_n	Input Noise Voltage Density	$f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz		10.5 10.3 9.8	20.0 13.5 11.5	nV/√Hz
$i_{np\text{-}p}$	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		15	35	pAp-p
i_n	Input Noise Current Density	$f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz		0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
R_{IN}	Input Resistance Differential-Mode	(Note 4)	7	31		MΩ
R_{INCM}	Input Resistance Common-Mode			120		GΩ
IVR	Input Voltage Range		±13	±14		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	94 **94**	110 **106**		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		7 **10**	32 **51**	μV/V
A_{VO}	Large Signal Voltage Gain	$R_L \leq 2 k\Omega$, $V_O = \pm 10V$ $R_L = 2 k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$, V_S ±3V (Note 4)	120 **100**	400 **400** 400		V/mV
V_O	Output Voltage Swing	$R_L \geq 10 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 1 k\Omega$	±12.0 ±11.5 **±11.0**	±13.0 ±12.8 **±12.6** ±12.0		V
SR	Slew Rate	$R_L \geq 2 k\Omega$ (Note 3)	0.1	0.3		V/μs
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		MHz
RO	Output Resistance	$V_O = 0$, $I_O = 0$		60		Ω
P_d	Power Consumption	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load		80 4	150 8	mW
	Offset Adj. Range	$R_P = 20 k\Omega$		±4		mV
TCV_{OS}	Average Input Offset Voltage Drift Without External Trim	(Note 4)		**0.7**	**2.5**	μV/°C
$TCV_{OS}n$	With External Trim	$R_P = 20 k\Omega$ (Note 4)		**0.7**	**2.5**	μV/°C
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**12**	**50**	pA/°C
TCI_B	Average Input Bias Current Drift	(Note 3)		**18**	**50**	pA/°C

Note 1: V_{OS} is measured approximately 0.5 second after application of power.

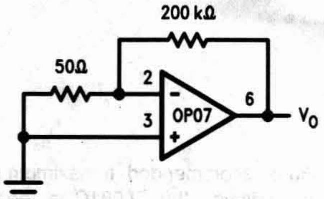
Note 2: Long-Term Offset Voltage Stability refers to the averaged trend line of V_{OS} vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Parameter is sample tested.

Note 3: Sample Tested.

Note 4: Guaranteed by design.

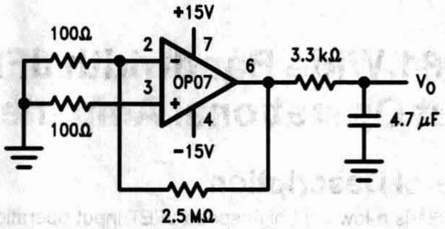
Test Circuits

Offset Voltage Test Circuit


200 kΩ
50Ω
2
3
6
OP07
V_O

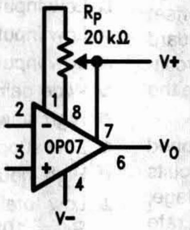
TL/H/10550-4

Low Frequency Noise Test Circuit


+15V
100Ω
100Ω
2
3
7
4
6
OP07
−15V
3.3 kΩ
4.7 μF
V_O
2.5 MΩ

TL/H/10550-5

Optional Offset Nulling Circuit


R_P
20 kΩ
V+
1
8
2
3
7
6
4
OP07
V_O
V−

TL/H/10550-6

National Semiconductor

TL081 Wide Bandwidth JFET Input Operational Amplifier

General Description

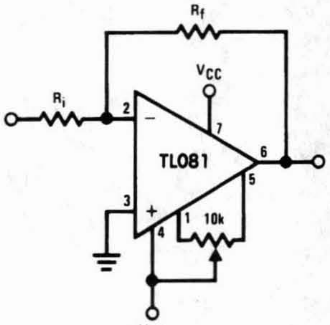
The TL081 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL081 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The TL081 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the TL081C is the better choice.

Features

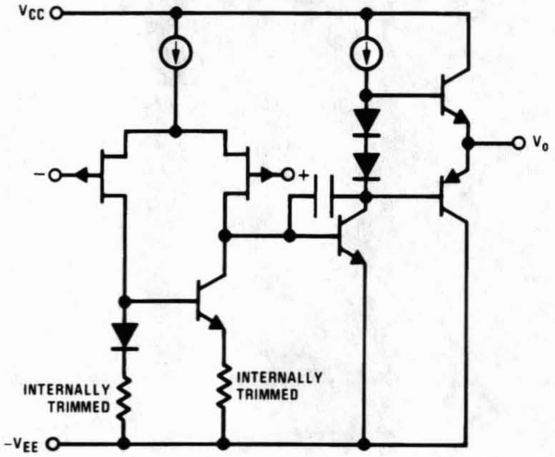
■ Internally trimmed offset voltage	15 mV
■ Low input bias current	50 pA
■ Low input noise voltage	25 nV/$\sqrt{\text{Hz}}$
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



TL/H/8358-1

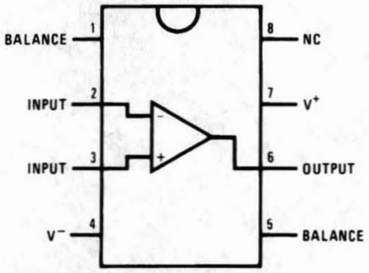
Simplified Schematic



TL/H/8358-2

Connection Diagram

Dual-In-Line Package



TL/H/8358-4

Order Number TL081CP
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C
θ_{jA}	120°C/W

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	TL081C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C Over Temperature		5	15 20	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		25	100 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		50	200 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	2.8	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	TL081C			Units
			Min	Typ	Max	
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13		V/μs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 120°C/W junction to ambient for N package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

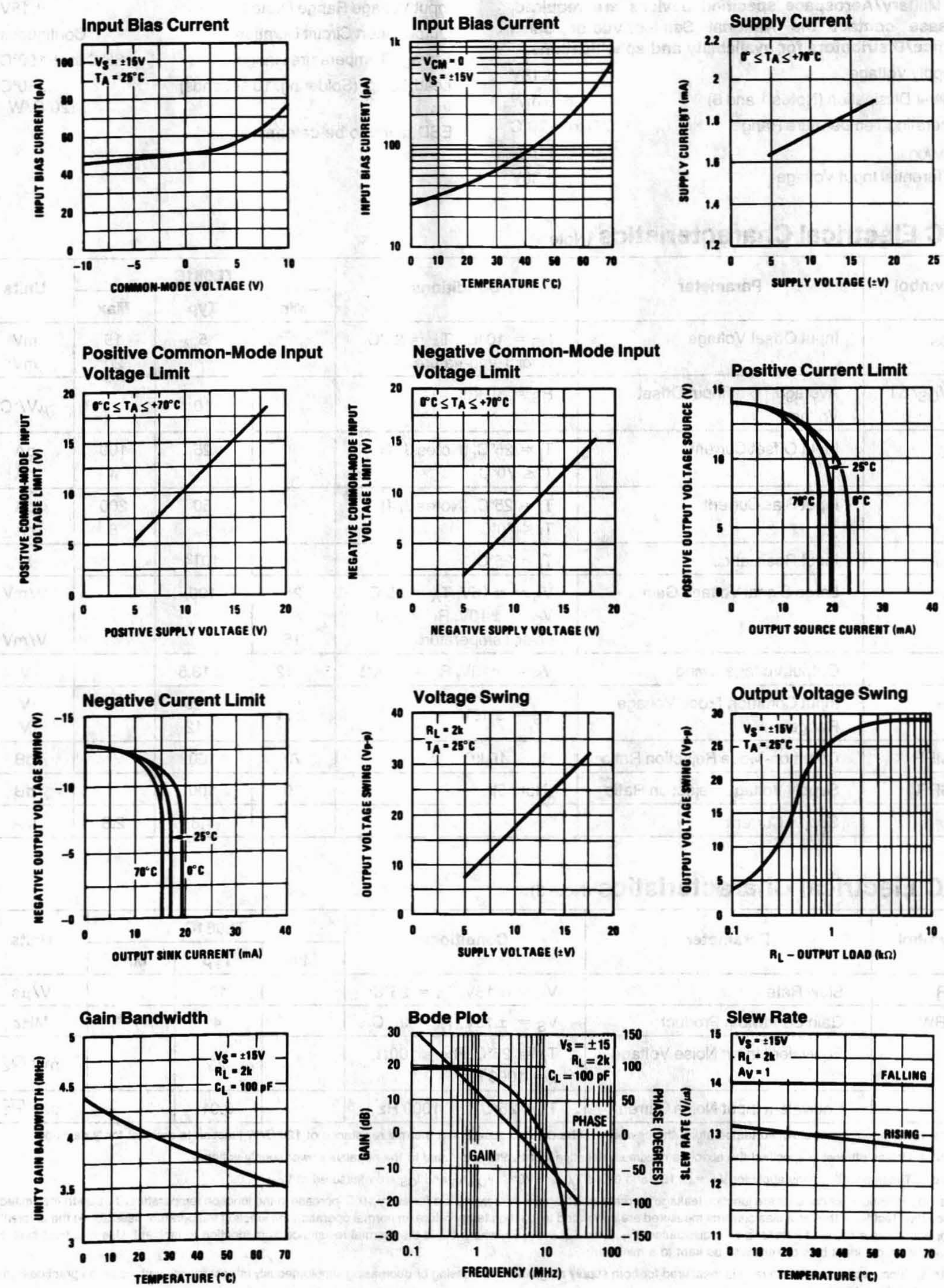
Note 3: These specifications apply for V_S = ±15V and 0°C $\leq T_A \leq$ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from V_S = ±5V to ±15V.

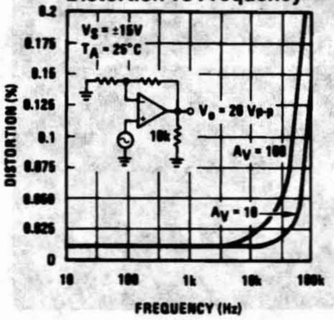
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

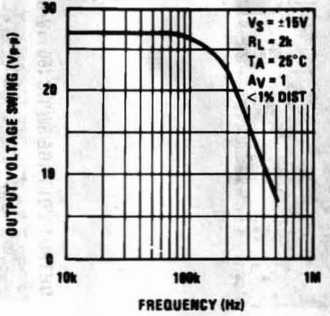
Typical Performance Characteristics

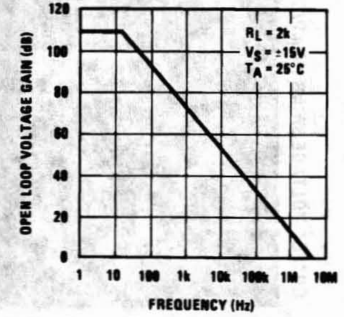


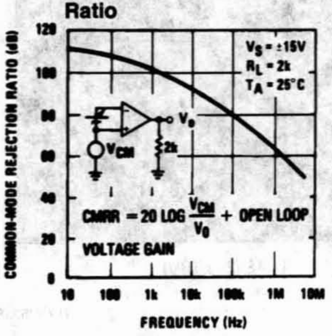
TL/H/8358–5

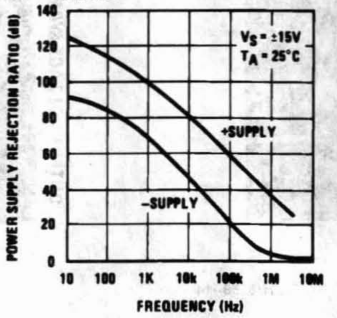
Typical Performance Characteristics (Continued)

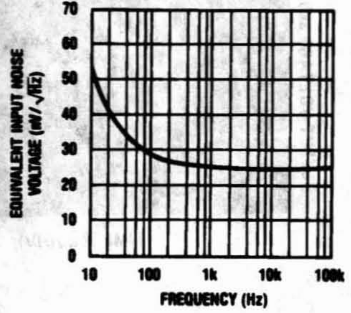

Distortion vs Frequency

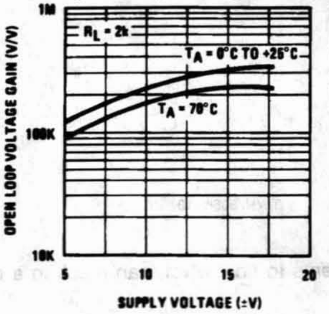

Undistorted Output Voltage Swing

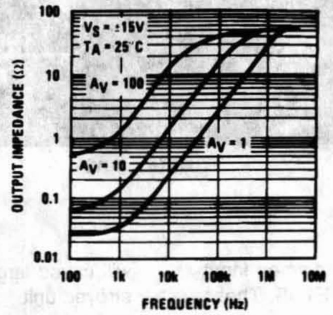

Open Loop Frequency Response

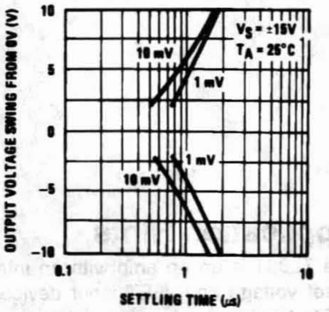

Common-Mode Rejection Ratio


Power Supply Rejection Ratio


Equivalent Input Noise Voltage


Open Loop Voltage Gain (V/V)

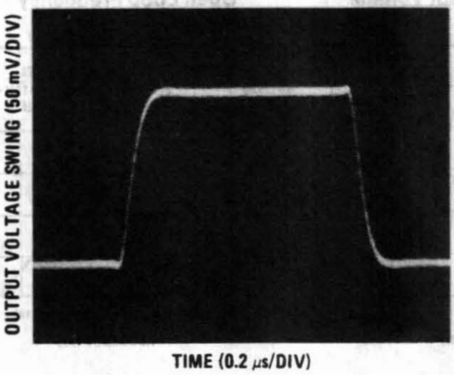

Output Impedance


Inverter Settling Time

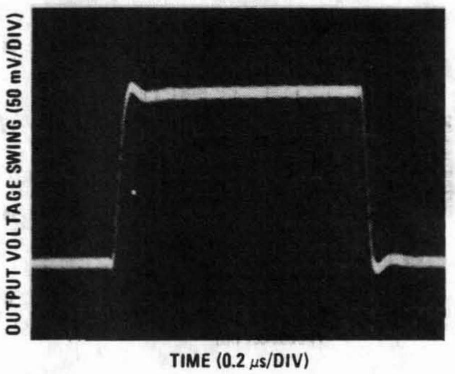
TL/H/8358–6

Pulse Response

Small Signal Inverting



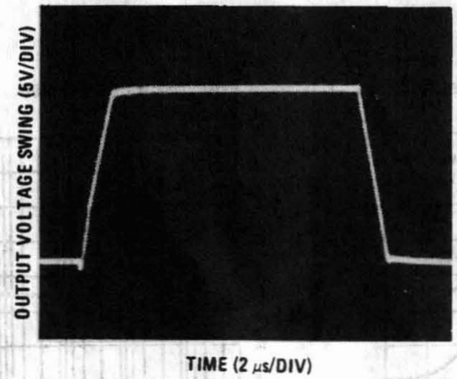
Small Signal Non-Inverting



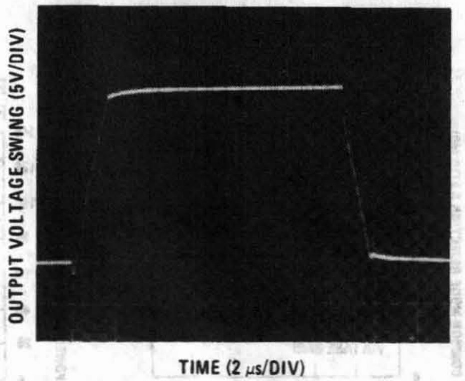
TL/H/8358-7

TL/H/8358-13

Large Signal Inverting



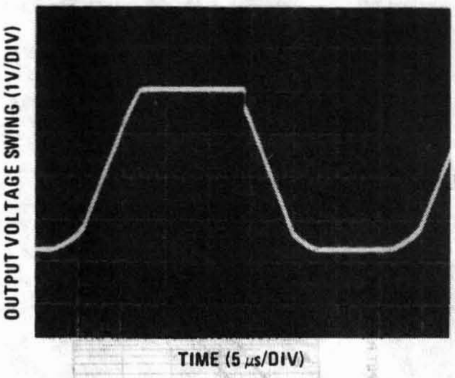
Large Signal Non-Inverting



TL/H/8358-14

TL/H/8358-15

Current Limit (R_L = 100Ω)



TL/H/8358-16

Application Hints

The TL081 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The TL081 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The TL081 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

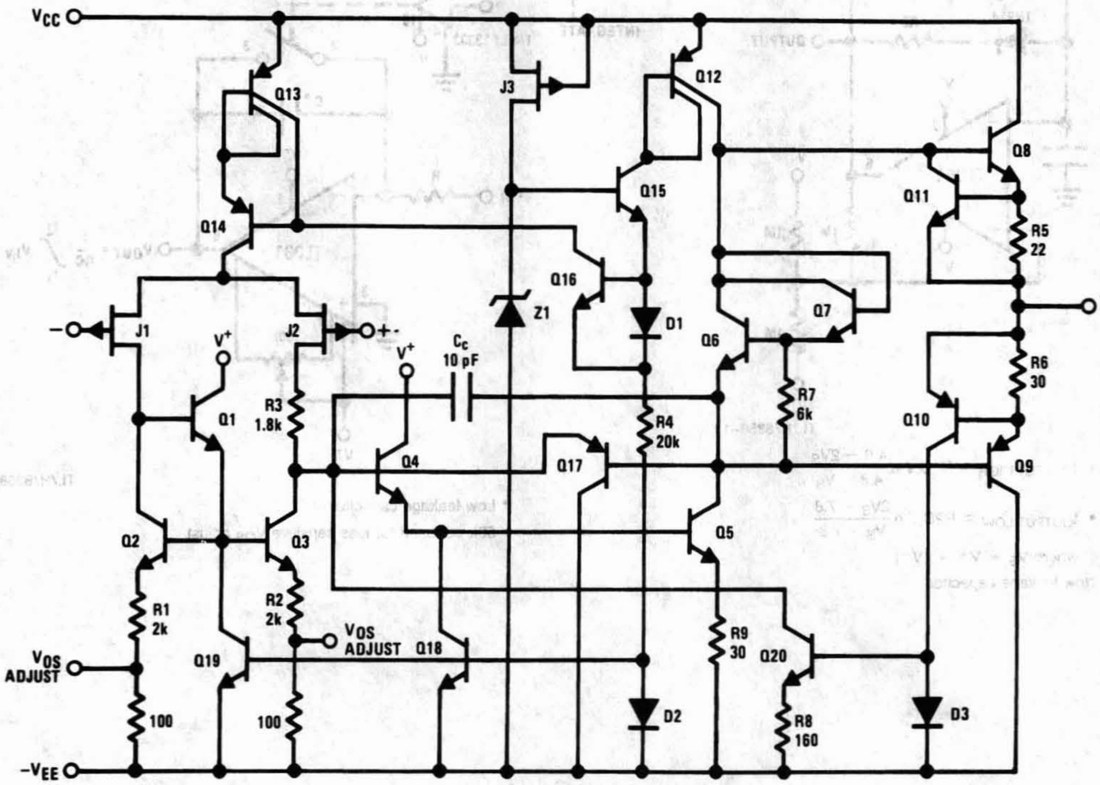
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

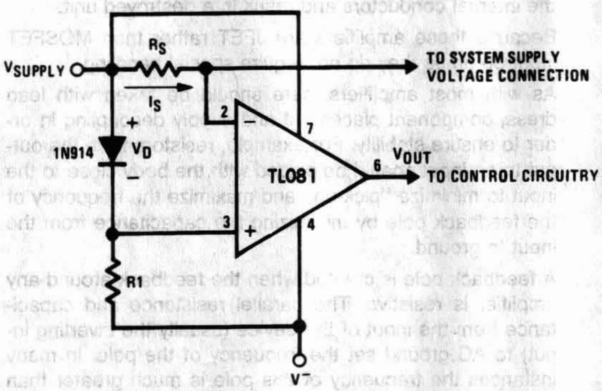
Detailed Schematic



TL/H/8358-8

Typical Applications

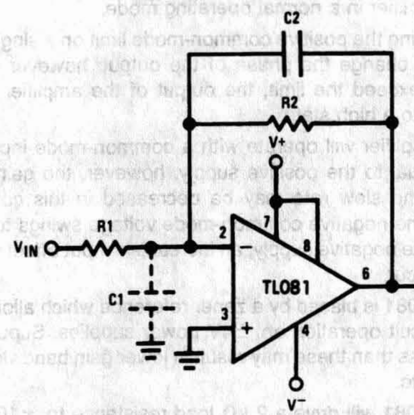
Supply Current Indicator/Limiter


R_S
V_SUPPLY
TO SYSTEM SUPPLY VOLTAGE CONNECTION
I_S
2
7
+
1N914
V_D
−
V_OUT
6
TL081
TO CONTROL CIRCUITRY
3
4
R1
V−

TL/H/8358-9

- V_{OUT} switches high when $R_S I_S > V_D$

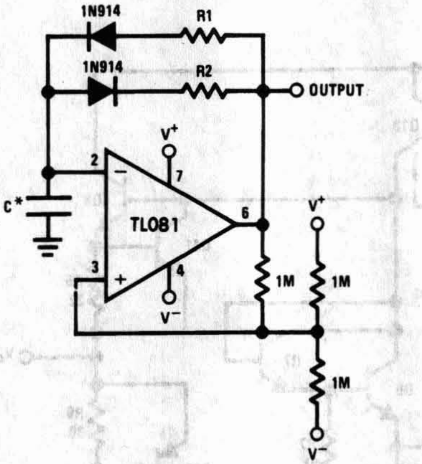
Hi-Z$_{IN}$ Inverting Amplifier


C2
R2
V+
7
R1
2
8
V_IN
6
C1
TL081
3
4
V−

TL/H/8358-10

Parasitic input capacitance C1 ≅ (3 pF for TL081 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator


1N914
R1
1N914
R2
OUTPUT
V+
2
7
C*
TL081
6
V+
3
4
1M
1M
V−
1M
V−

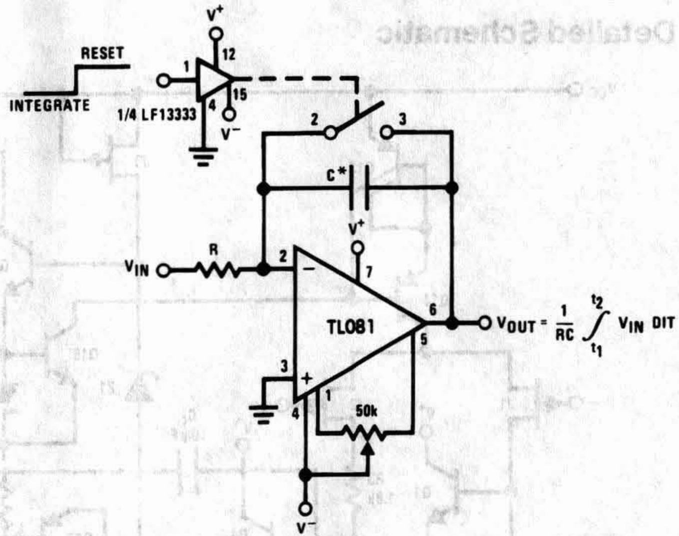
TL/H/8358-11

- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \dfrac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \dfrac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator


V+
RESET
12
INTEGRATE
1
15
1/4 LF13333
4
V−
2
3
C*
V+
R
2
V_IN
7
6
TL081
5
V_OUT = 1/RC ∫ V_IN DIT (t1 to t2)
3
1
4
50k
V−

TL/H/8358-12

- Low leakage capacitor
- 50k pot used for less sensitive V_{OS} adjust

National Semiconductor

TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

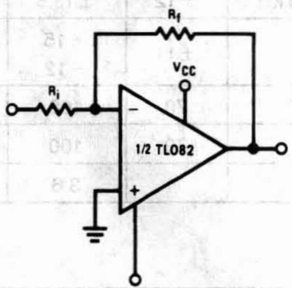
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage	15 mV
■ Low input bias current	50 pA
■ Low input noise voltage	16nV/$\sqrt{\text{Hz}}$
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	3.6 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20\ Vp-p$, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection

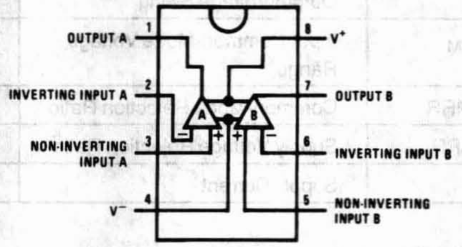


R_f
V_{CC}
R_i
1/2 TL082
$-V_{EE}$

TL/H/8357–1

Connection Diagram

DIP/SO Package (Top View)

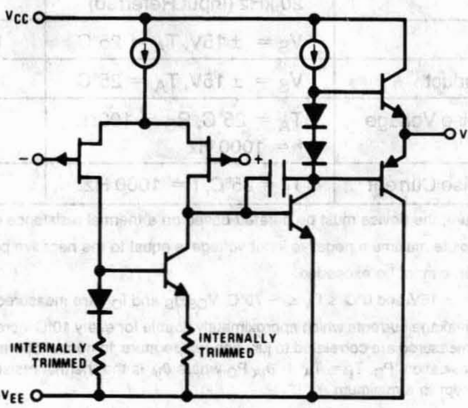


OUTPUT A 1
INVERTING INPUT A 2
NON-INVERTING INPUT A 3
V⁻ 4
8 V⁺
7 OUTPUT B
6 INVERTING INPUT B
5 NON-INVERTING INPUT B
A
B

TL/H/8357–3

Order Number TL082CM or TL082CP
See NS Package Number M08A or N08E

Simplified Schematic



V_{CC}
−
+
V_O
INTERNALLY TRIMMED
INTERNALLY TRIMMED
$-V_{EE}$

TL/H/8357–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 1)
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$ Over Temperature		5	15 20	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10		μV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 4, 5) $T_j \leq 70°C$		25	200 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 4, 5) $T_j \leq 70°C$		50	400 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\ k\Omega$ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	70	100		dB
I_S	Supply Current			3.6	5.6	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1Hz-20 kHz (Input Referred)		−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	8	13		V/μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 115°C/W junction to ambient for the N package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

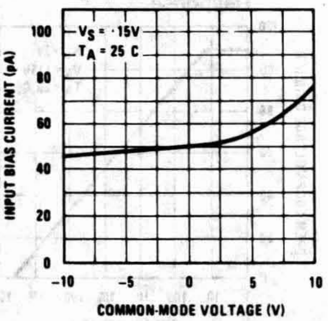
Note 4: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

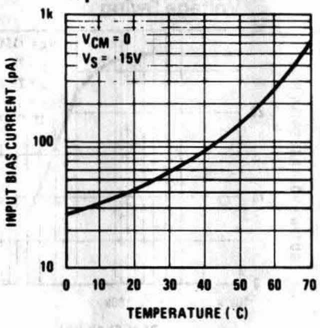
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm 6V$ to $\pm 15V$.

Typical Performance Characteristics

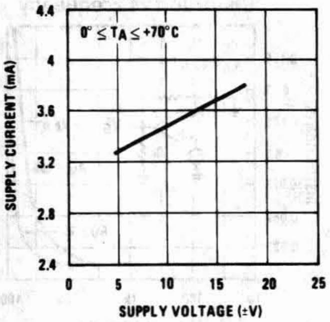
Input Bias Current



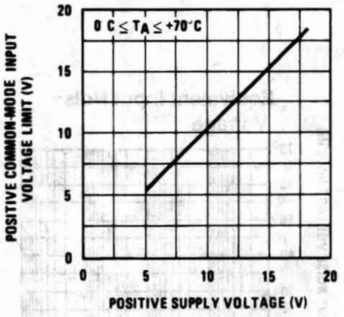
Input Bias Current



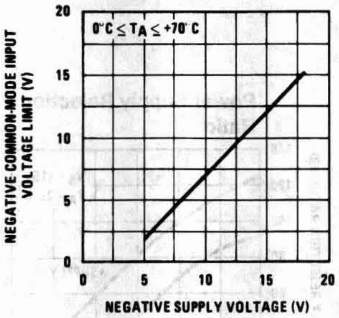
Supply Current



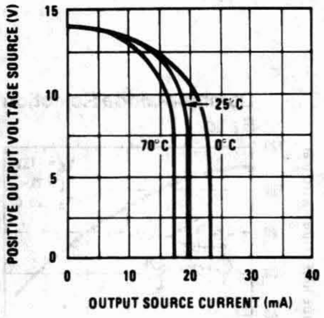
Positive Common-Mode Input Voltage Limit



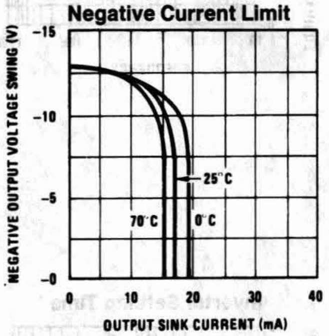
Negative Common-Mode Input Voltage Limit



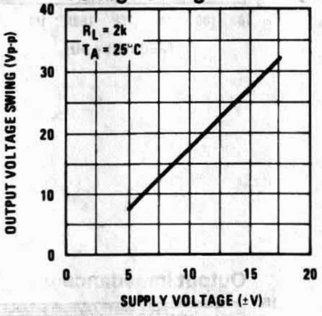
Positive Current Limit



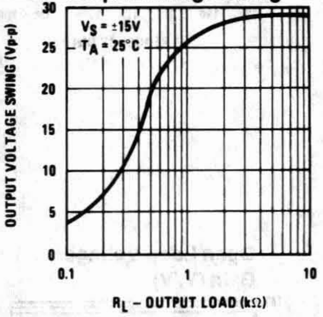
Negative Current Limit



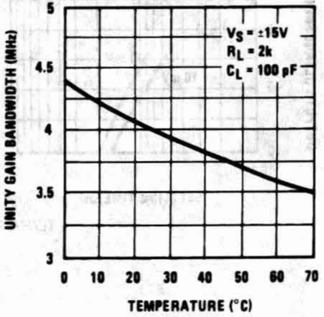
Voltage Swing



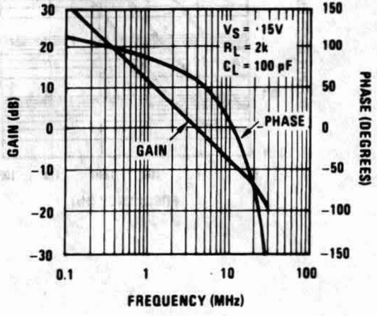
Output Voltage Swing



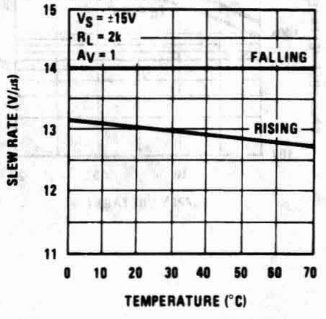
Gain Bandwidth



Bode Plot



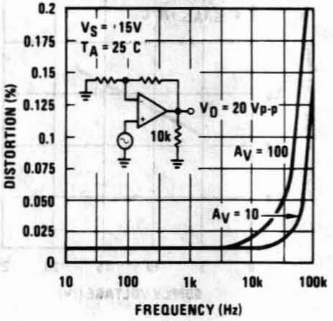
Slew Rate



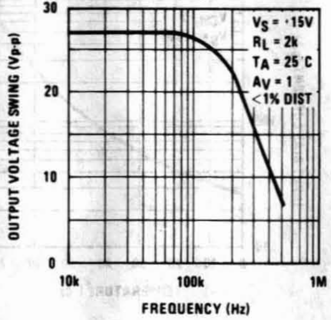
TL/H/8357-4

Typical Performance Characteristics (Continued)

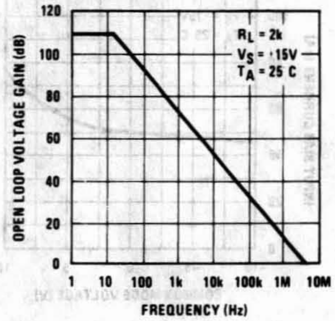
Distortion vs Frequency



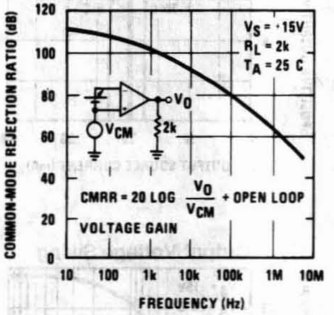
Undistorted Output Voltage Swing



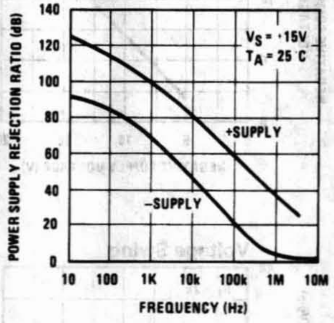
Open Loop Frequency Response



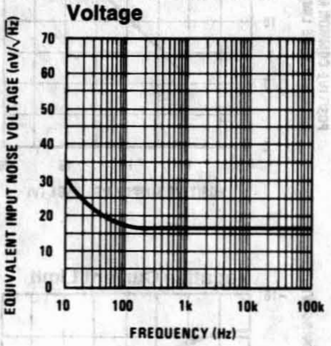
Common-Mode Rejection Ratio



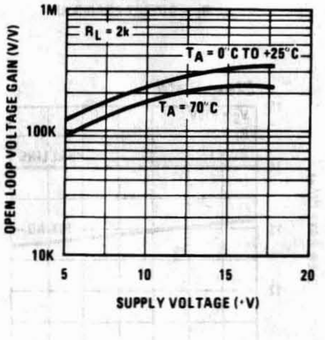
Power Supply Rejection Ratio



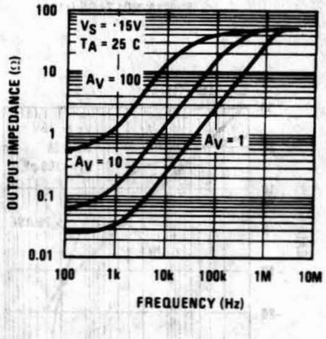
Equivalent Input Noise Voltage



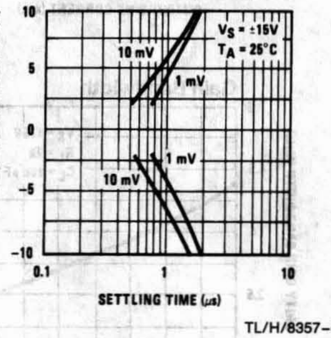
Open Loop Voltage Gain (V/V)



Output Impedance



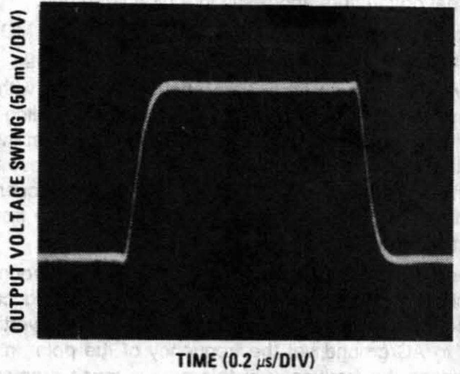
Inverter Settling Time



TL/H/8357–5

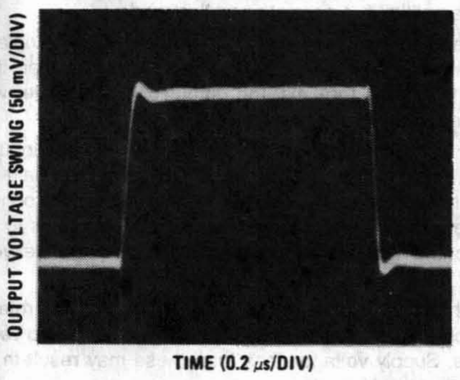
Pulse Response

Small Signal Inverting



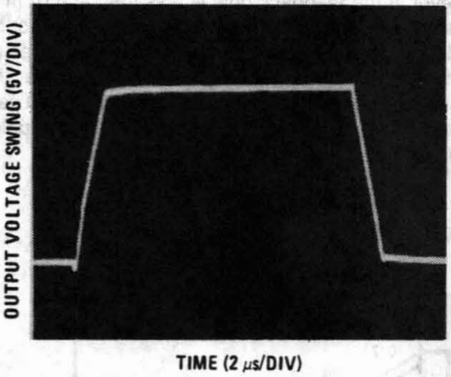
TL/H/8357-6

Small Signal Non-Inverting



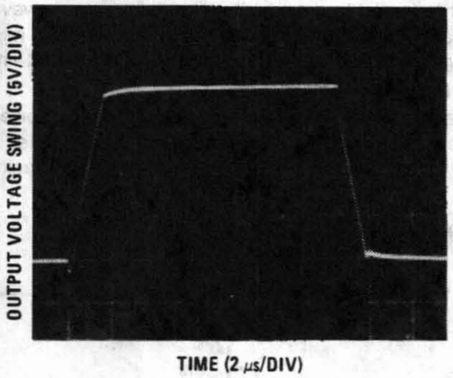
TL/H/8357-7

Large Signal Inverting



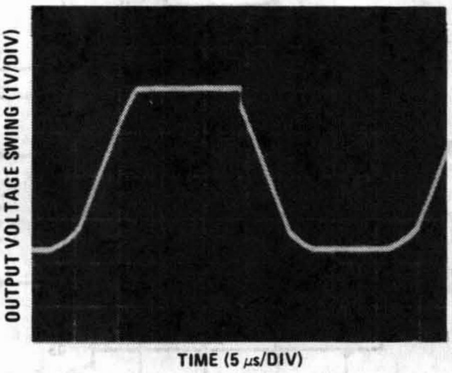
TL/H/8357-8

Large Signal Non-Inverting



TL/H/8357-9

Current Limit (R_L = 100Ω)



TL/H/8357-10

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case

Application Hints (Continued)

does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

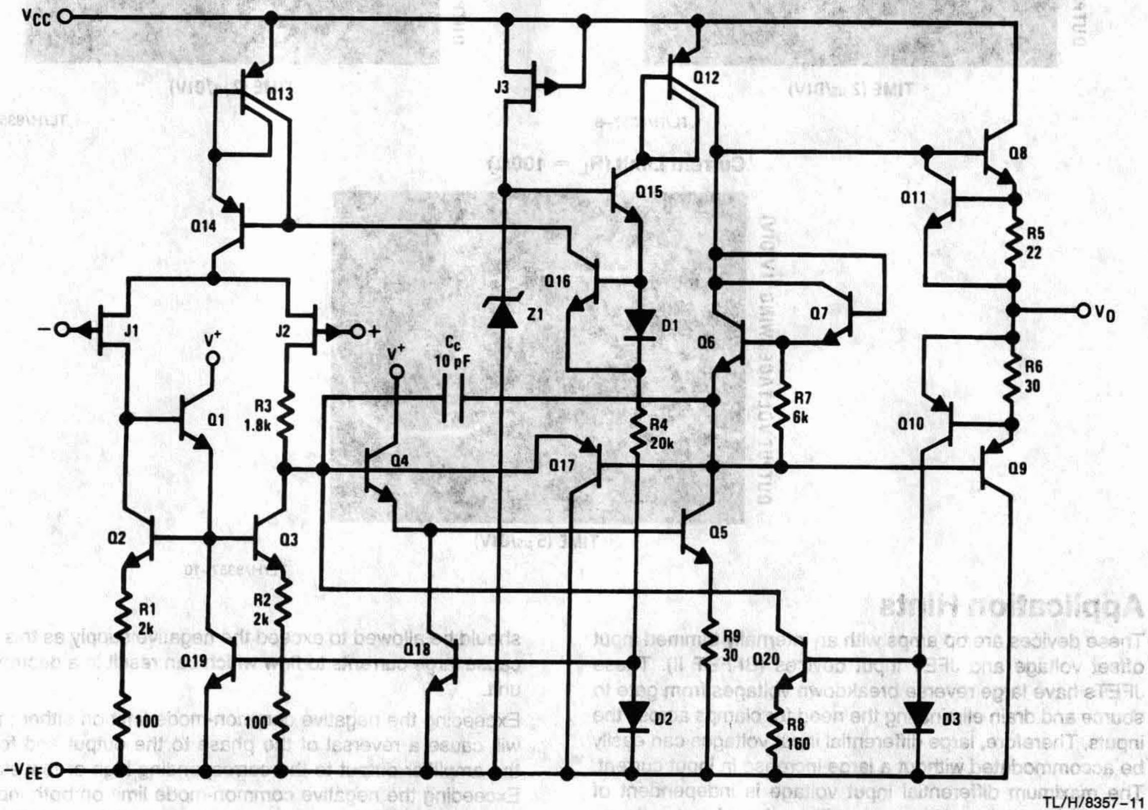
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

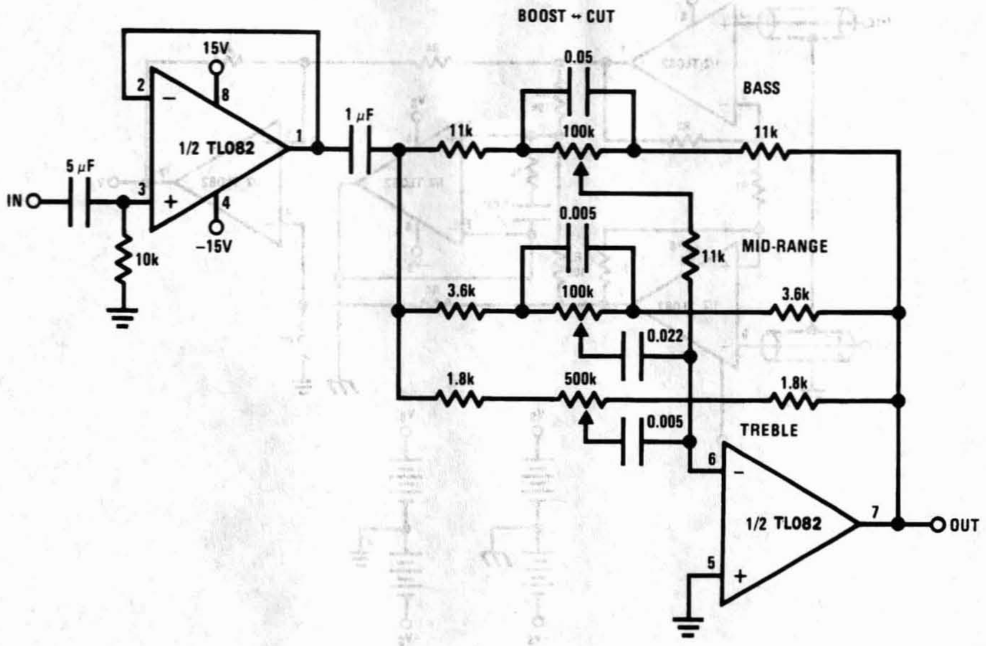
Detailed Schematic



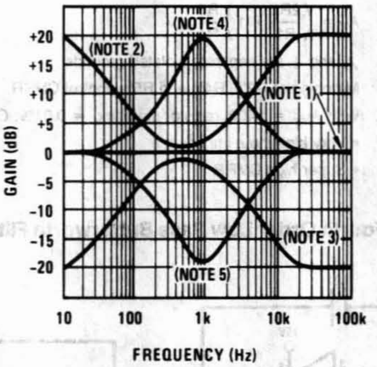
TL/H/8357–11

Typical Applications

Three-Band Active Tone Control


BOOST ↔ CUT
15V
2
8
−
1/2 TL082
1
+
3
4
−15V
IN
5 μF
10k
1 μF
11k
0.05
100k
11k
BASS
0.005
11k
MID-RANGE
3.6k
100k
3.6k
0.022
1.8k
500k
1.8k
0.005
TREBLE
6
1/2 TL082
7
OUT
5

TL/H/8357–12



TL/H/8357–13

Note 1: All controls flat.

Note 2: Bass and treble boost, mid flat.

Note 3: Bass and treble cut, mid flat.

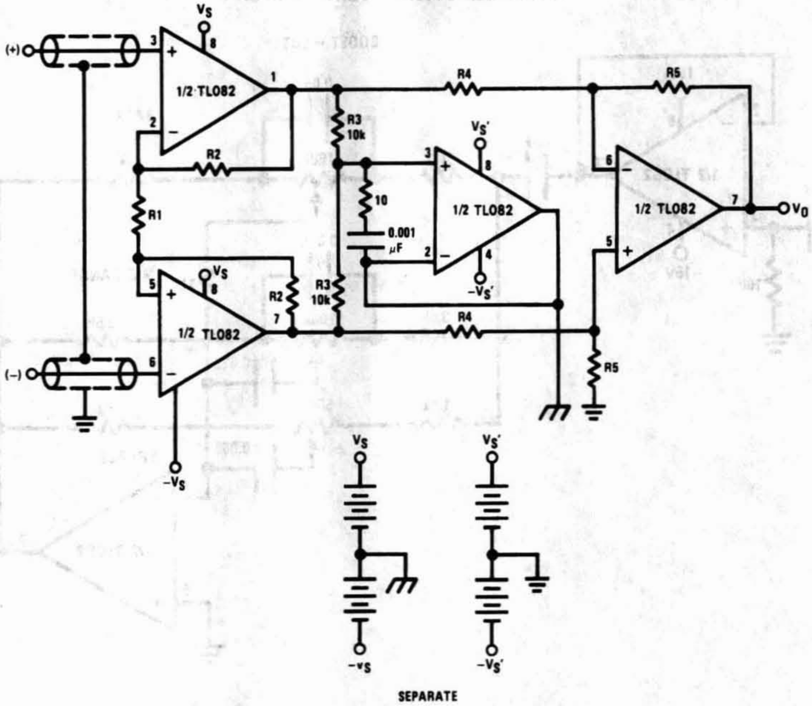
Note 4: Mid boost, bass and treble flat.

Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier


(+)
(−)
VS
−VS
1/2 TL082
1/2 TL082
1/2 TL082
1/2 TL082
R1
R2
R2
R3 10k
R3 10k
10
0.001 μF
R4
R4
R5
R5
VS′
−VS′
VO
VS
−VS
VS′
−VS′
SEPARATE

TL/H/8357-14

$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

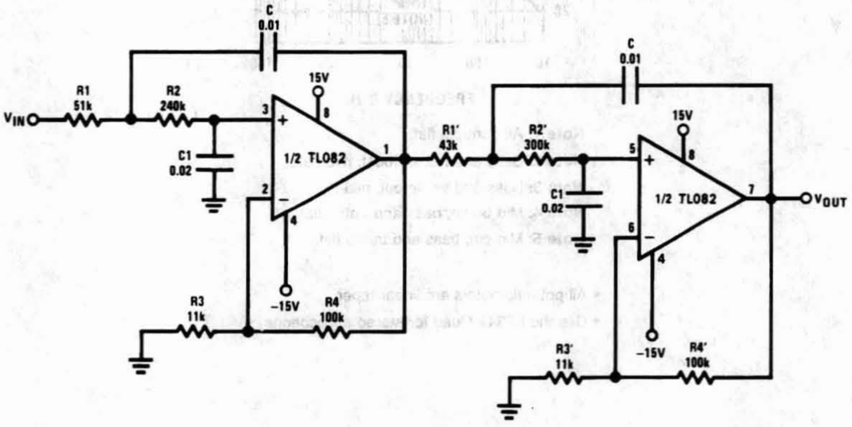
⏚ and ⏚ are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

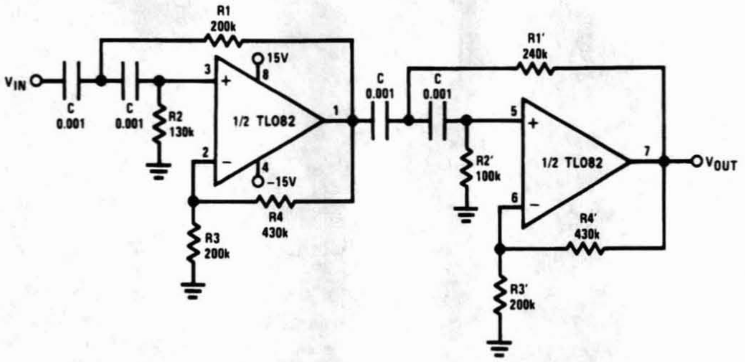

C 0.01
R1 51k
R2 240k
VIN
C1 0.02
15V
−15V
1/2 TL082
R3 11k
R4 100k
C 0.01
R1′ 43k
R2′ 300k
C1′ 0.02
15V
−15V
1/2 TL082
VOUT
R3′ 11k
R4′ 100k

TL/H/8357-15

- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4′/R3′)
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

Typical Applications (Continued)

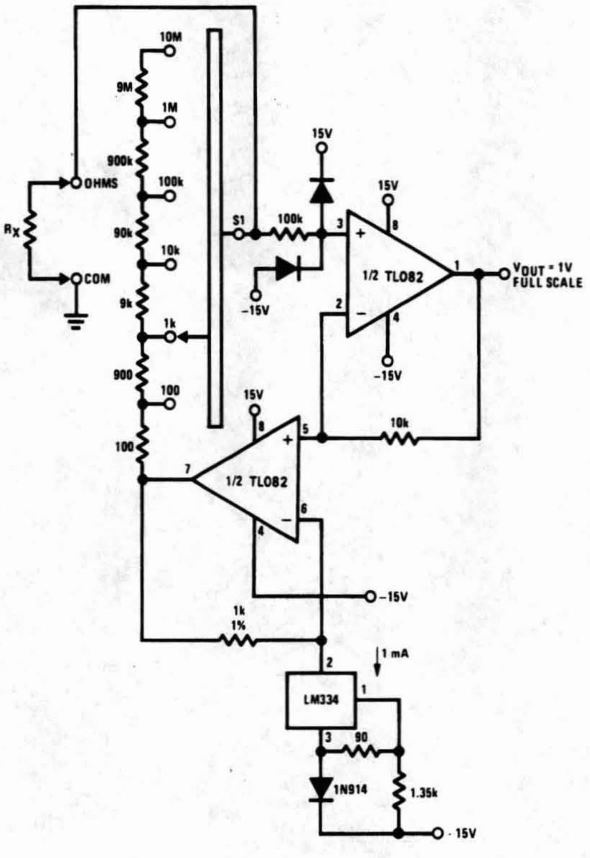
Fourth Order High Pass Butterworth Filter


R1
200k
V_IN
C
0.001
C
0.001
R2
130k
3
15V
8
1/2 TL082
1
2
4
-15V
R4
430k
R3
200k
C
0.001
C
0.001
R1'
240k
5
R2'
100k
1/2 TL082
7
V_OUT
6
R4'
430k
R3'
200k

TL/H/8357–16

- Corner frequency (f_c) $= \sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Ohms to Volts Converter


10M
9M
1M
900k
100k
OHMS
R_X
COM
90k
10k
9k
1k
900
100
100
S1
100k
15V
15V
3
8
1/2 TL082
1
V_OUT = 1V FULL SCALE
-15V
2
4
-15V
15V
8
5
10k
7
1/2 TL082
6
4
-15V
1k
1%
2
1 mA
LM334
1
3
90
1N914
1.35k
· 15V

TL/H/8357–17

$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the TL082CP.

Section 2
Buffers

Section 2 Contents

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Buffers Selection Guide 2-4
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LH0033/LH0063 Fast and Ultra Fast Buffers 2-8
LH4001 Wideband Current Buffer 2-19
LH4002 Wideband Video Buffer 2-23
LM102/LM302 Voltage Followers 2-27
LM110/LM210/LM310 Voltage Followers 2-33
LM6121/LM6221/LM6321 High Speed Buffers 2-46
LM6125/LM6225/LM6325 High Speed Buffers 2-52

Buffers
Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental.

$$\%\ \text{harmonic distortion} = \frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Voltage: That voltage which must be applied to the input terminal to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current.

Input Voltage Range: The range of voltages on the input terminal for which the buffer operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage.

Output Impedance: The ratio of change in output voltage to output current under the stated conditions.

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the buffer with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

National Semiconductor

Buffer Selection Guide (Notes 1 and 2)

Device Type	Key Features	Slew Rate (V/μs)	Bandwidth −3 dB (MHz)	Gain (A_V)	Output (V, mA)	Full Power BW (MHz @ V_{PP}, R_L)	Test Conditions
LH0063	FET Input, Very Fast	2400	200	0.93	±13, ±260	40 @ 20, 50	$R_L = 50, V_S = \pm15V$
LH0033	FET Input, High Speed	1500	100	0.98	±9, ±90	24 @ 20, 1k	$R_L = 1k, V_S = \pm15V$
LH4002	Wideband Video Buffer	1250	200	0.97	±2.2, ±44	100 @ 4, 50	$R_L = 50, V_S = \pm5V$
LH2003/2033	Wideband Video Buffer	1200	100	0.9	±11.3, ±113	2 @ 20, 100	$R_L = 1k, 50, V_S = \pm15$
LM6121/6125	High Speed VIP™ Buffer	800	50	0.90	±12, ±240	10.6 @ 12, 50	$R_L = 50, V_S = \pm15V$
LH0002	Medium Speed	200	30	0.97	±10, ±100	3 @ 20, 1k	$R_L = 1k, V_S = \pm12V$
LH4001	Low Cost LH0002	125	25	0.97	±10, ±100	4 @ 10, 100	$R_L = 100, V_S = \pm12V$
LM110, 210, 310	Voltage Follower	30	20	0.9999	±10, ±10	0.5 @ 20, 10k	$R_L = 10k, V_S = \pm15V$

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: 200°C Temp Range Parts are available. Consult local sales office for information.

National Semiconductor

LH0002 Buffer

General Description

The LH0002 is a general purpose buffer. Its features make it ideal to integrate with operational amplifiers inside a closed loop configuration to increase current output. The symmetrical output portion of the circuit also provides a low output impedance for both the positive and negative slopes of output pulses.

The LH0002 is available in an 8-lead TO-99 can. The LH0002C is available in an 8-lead TO-99, and a 10-pin molded dual-in-line package.

The LH0002 is specified for operation over the −55°C to +125°C military temperature range. The LH0002C is specified for operation over the 0°C to +85°C temperature range.

Features

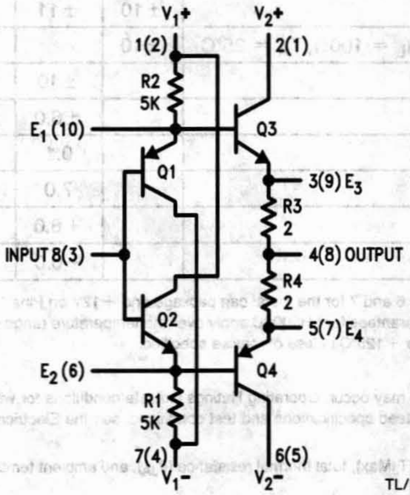
■ High input impedance	400 kΩ
■ Low output impedance	6Ω

- ■ High power efficiency
- ■ Low harmonic distortion
- ■ DC to 30 MHz bandwidth
- ■ Output voltage swing that approaches supply voltage
- ■ 400 mA pulsed output current
- ■ Slew rate is typically 200 V/µs
- ■ Operation from ±5V to ±20V

Applications

- ■ Line driver
- ■ 30 MHz buffer
- ■ High speed D/A conversion

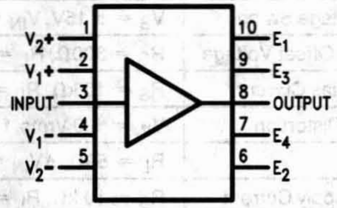
Schematic and Connection Diagrams


V1+
V2+
1(2)
2(1)
R2
5K
E1 (10)
Q3
Q1
3(9) E3
R3
2
INPUT 8(3)
4(8) OUTPUT
R4
2
Q2
5(7) E4
E2 (6)
Q4
R1
5K
7(4)
V1−
6(5)
V2−

TL/H/5560–1

Pin numbers in parentheses denote pin connections for dual-in-line package.

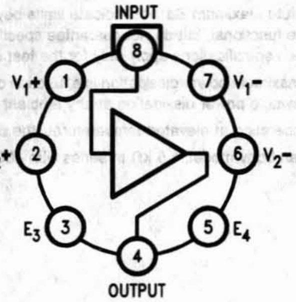
Dual-In-Line Package


V2+ 1
V1+ 2
INPUT 3
V1− 4
V2− 5
10 E1
9 E3
8 OUTPUT
7 E4
6 E2

TL/H/5560–2

Order Number LH0002CN
See NS Package Number N10A

Metal Can Package


INPUT
8
V1+ 1
7 V1−
V2+ 2
6 V2−
E3 3
5 E4
4
OUTPUT

TL/H/5560–3

Order Number LH0002H,
LH0002H-MIL or LH0002CH
LH0002H/883*
See NS Package Number H08D

*Available per SMD #7801301

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Supply Voltage	±22V
Power Dissipation (Note 4)	600 mW
Input Voltage	(Equal to Power Supply Voltage)
Storage Temperature Range	−65°C to +150°C
Junction Temperature	
N Package	+150°C
H Package	+175°C
Steady State Output Current	±100 mA
Pulsed Output Current (50 ms On/1 sec. Off)	±400 mA
Lead Temperature Soldering (10 seconds)	
Metal Can	300°C
Plastic	260°C
ESD Rating (Note 6)	2 kV

Operating Ratings (Note 3)

Temperature Range	
LH0002	−55°C to +125°C
LH0002C	0°C to +85°C
Thermal Resistance (Note 5)	
θ_{JA}, H Package	+125°C/W
θ_{JC}, H Package	+75°C/W
θ_{JA}, N Package	+120°C/W

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Voltage Gain	$R_S = 10\ k\Omega$, $R_L = 1.0\ k\Omega$, $V_{IN} = \pm10V$	0.95	0.97		
Input Impedance	$R_S = 200\ k\Omega$, $V_{IN} = \pm1.0V$, $R_L = 1.0\ k\Omega$	180	400		kΩ
Output Impedance	$V_{IN} = \pm1.0V$, $R_L = 50\Omega$, $R_S = 10\ k\Omega$		6.0	10	Ω
Output Voltage Swing	$R_L = 1.0\ k\Omega$, $V_{IN} = \pm12V$	±10	±11		V
Output Voltage Swing	$V_S = \pm15V$, $V_{IN} = \pm12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $T_A = 25°C$	±10			V
DC Output Offset Voltage	$R_S = 300\Omega$, $R_L = 1.0\ k\Omega$		±10	±30	mV
DC Input Bias Current	$R_S = 10\ k\Omega$, $R_L = 1.0\ k\Omega$		±6.0	±10	μA
Harmonic Distortion	$V_{IN} = 5.0$ Vrms, f = 1.0 kHz		0.1		%
Rise Time	$R_L = 50\Omega$, $\Delta V_{IN} = 100$ mV		7.0	12	ns
Positive Supply Current	$R_S = 10\ k\Omega$, $R_L = 1.0\ k\Omega$		+6.0	+10	mA
Negative Supply Current	$R_S = 10\ k\Omega$, $R_L = 1.0\ k\Omega$		−6.0	−10	mA

Note 1: Specification applies for $T_A = 25°C$ with +12V on Pins 1 and 2; −12V on Pins 6 and 7 for the metal can package and +12V on Pins 1 and 2; −12V on Pins 4 and 5 for the dual-in-line package, unless otherwise specified. The parameter guarantees for LH0002C apply over the temperature range of 0°C to +85°C, while parameters for the LH0002 are guaranteed over the temperature range −55°C to +125°C unless otherwise specified.

Note 2: Refer to RETS0002X for LH0002 military specifications.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

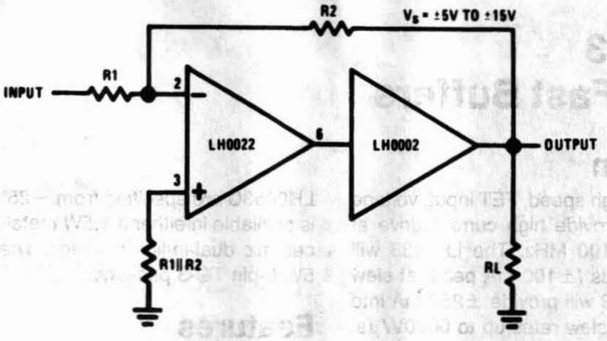
Note 4: The maximum power dissipation is a function of maximum junction temperature (T_JMax), total thermal resistance (θ_{JA}), and ambient temperature (T_A). The maximum allowable power dissipation at any ambient is $P_D = (T_J\text{Max} - T_A)/\theta_{JA}$.

Note 5: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} and T_JMax. $T_J = T_A + P_D\theta_{JA}$.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

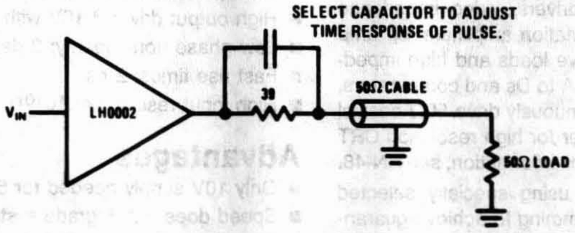
Typical Applications

High Current Operational Amplifier


R2
V_S = ±5V TO ±15V
INPUT
R1
2
−
LH0022
6
LH0002
OUTPUT
3
+
R1 || R2
RL

TL/H/5560–4

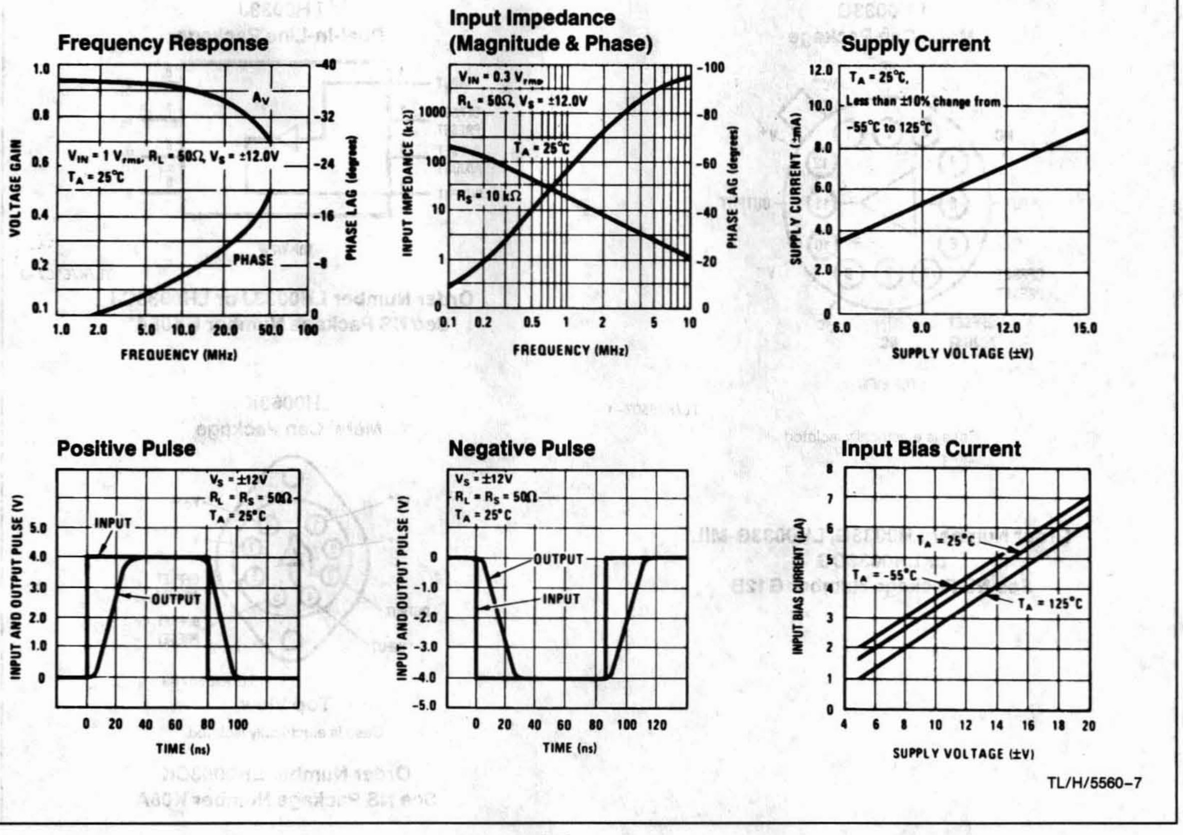
Line Driver


SELECT CAPACITOR TO ADJUST
TIME RESPONSE OF PULSE.
V_IN
LH0002
39
50Ω CABLE
50Ω LOAD

*Previously called NH0002/NH0002C

TL/H/5560–5

Typical Performance Characteristics



TL/H/5560–7

National Semiconductor

LH0033/LH0063
Fast and Ultra Fast Buffers

General Description

The LH0033 and LH0063 are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH0033 will provide ±10 mA into 1 kΩ loads (±100 mA peak) at slew rates of 1500V/μs. The LH0063 will provide ±250 mA into 50Ω loads (±500 mA peak) at slew rates up to 6000V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffers for driving reactive loads and high impedance input buffers for high speed A to Ds and comparators. In addition, the LH0063 can continuously drive 50Ω coaxial cables or be used as a yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH0033 is specified for operation from −55°C to +125°C; the LH0033C and the LH0063C are specified from −25°C to +85°C. The LH0033 is available in either a 1.5W metal TO-8 package or an 8-pin ceramic dual-in-line package. The LH0063 is available in a 5W 8-pin TO-3 package.

Features

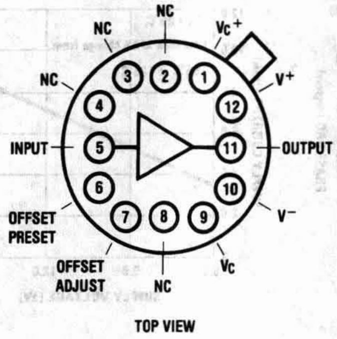
- Ultra fast (LH0063): 6000 V/μs
- Wide range single or dual supply operation
- Wide power bandwidth: DC to 100 MHz
- High output drive: ±10V with 50Ω load
- Low phase non-linearity: 2 degrees
- Fast rise times: 2 ns
- High input resistance: $10^{10}\Omega$

Advantages

- Only 10V supply needed for 5 Vp-p video out
- Speed does not degrade system performance
- Wide data rate range for phase encoded systems

Connection Diagrams

LH0033G
Metal Can Package

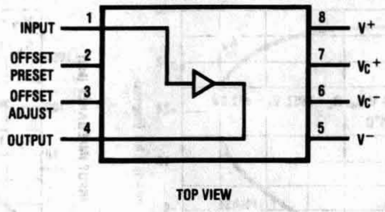


TL/K/5507-1

Case is electrically isolated

Order Number LH0033G, LH0033G-MIL or LH0033CG
See NS Package Number G12B

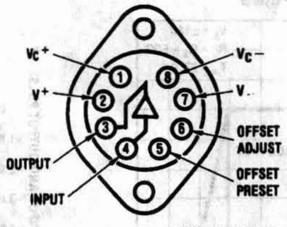
LH0033J
Dual-In-Line Package



TL/K/5507-2

Order Number LH0033J or LH0033CJ
See NS Package Number HY08A

LH0063K
Metal Can Package



TL/K/5507-3

Top View

Case is electrically isolated

Order Number LH0063CK
See NS Package Number K08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	40V
Power Dissipation (See Curves)	
LH0063C	5W
LH0033/LH0033C	2.2W
Junction Temperature	175°C
Input Voltage	$\pm V_S$
Continuous Output Current	
LH0063C	±250 mA
LH0033/LH0033C	±100 mA
Peak Output Current	
LH0063C	±500 mA
LH0033/LH0033C	±250 mA
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Temperature Range

LH0033	−55°C to +125°C
LH0033C and LH0063C	−25°C to +85°C
Storage Temperature Range	−65° to +150°C

ESD rating to be determined.

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified, (Note 1)

Parameter	Conditions	LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage	$R_S = 100\Omega, T_J = 25°C$, $V_{IN} = 0V$ (Note 2) $R_S = 100\Omega$		5.0	10 15		12	20 25	mV mV
Average Temperature Coefficient of Offset Voltage	$R_S = 100\Omega$, $V_{IN} = 0V$ (Note 3)		50	100		50	100	μV/°C
Input Bias Current	$V_{IN} = 0V$ $T_J = 25°C$ (Note 2) $T_A = 25°C$ (Note 4) $T_J = T_A = T_{MAX}$			250 2.5 10			500 5.0 20	pA nA nA
Voltage Gain	$V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0k\Omega$	0.97	0.98	1.00	0.96	0.98	1.00	V/V
Input Impedance	$R_L = 1\ k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 1.0k$		6.0	10		6.0	10	Ω
Output Voltage Swing	$V_I = \pm 14V$, $R_L = 1.0k$ $V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	±12 ±9.0			±12 ±9.0			V V
Supply Current	$V_{IN} = 0V$ (Note 5)		20	22		21	24	mA
Power Consumption	$V_{IN} = 0V$		600	660		630	720	mW

AC Electrical Characteristics $T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1.0\ K\Omega$ (Note 6)

Parameter	Conditions	LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	$V_{IN} = \pm 10V$	1000	1500		1000	1400		V/μs
Bandwidth	$V_{IN} = 1.0$ Vrms		100			100		MHz
Phase Non-Linearity	BW = 1.0Hz to 20 MHz		2.0			2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		2.9			3.2		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.2			1.5		ns
Harmonic Distortion	f > 1 kHz		<0.1			<0.1		%

Note 1: LH0033 is 100% production tested as specified at 25° C, 125°C, and−55°C. LH0033AC/C are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limited are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

Note 3: LH0033 is 100% production tested for this parameter. LH0033C is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 4: Measured in still air 7 minutes after application of power. Guaranteed through correlated automatic pulse testing.

Note 5: Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Note 7: Refer to RETS0033 for the LH0033G military specifications.

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	LH0063C			Units
		Min	Typ	Max	
Output Offset Voltage	$R_S \le 100k\Omega$, $T_J = 25°C$, $R_L = 100\Omega$ (Note 2)		10	50	mV
				100	mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \le 100\ k\Omega$		300		µV/°C
Input Bias Current	$T_J = 25°C$ (Note 2)		10	30	nA
				100	nA
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \le 100\ k\Omega$, $R_L = 1\ k\Omega$	0.94	0.96	1.0	V/V
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \le 100\ k\Omega$, $R_L = 50\Omega$ $T_J = 25°C$	0.91	0.93	0.98	V/V
Input Capacitance	Case Shorted to Output		8.0		pF
Output Impedance	$V_{OUT} = \pm 10V$, $R_S \le 100\ k\Omega$, $R_L = 50\Omega$		1.0	4.0	Ω
Output Current Swing	$V_{IN} = \pm 10V$, $R_S \le 100\ k\Omega$	0.2	0.25		A
Output Voltage Swing	$R_L = 50\Omega$	±10	±13		V
Output Voltage Swing	$V_S = \pm 5.0V$, $R_L = 50\Omega$, $T_J = 25°C$	5.09	7.0		Vp-p
Supply Current	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		50	65	mA
Supply Current	$V_S = \pm 5.0V$		40		mA
Power Consumption	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		1.5	1.95	W
Power Consumption	$V_S = \pm 5.0V$		400		mW

AC Electrical Characteristics $T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$ (Note 3)

Parameter	Conditions	LH0063C			Units
		Min	Typ	Max	
Slew Rate	$R_L = 1.0\ k\Omega$, $V_{IN} = \pm 10V$		6000		V/µs
Slew Rate	$R_L = 50\Omega$, $V_{IN} = \pm 10V$, $T_J = 25°C$	2000	2400		V/µs
Bandwidth	$V_{IN} = 1.0$ Vrms		200		MHz
Phase Non-Linearity	BW = 1.0 Hz to 20 MHz		2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		1.9		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		2.1		ns
Harmonic Distortion			<0.1		%

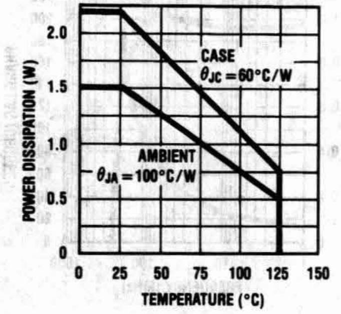
Note 1: LH0063C is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

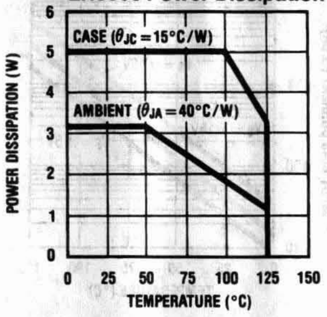
Note 3: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Typical Performance Characteristics

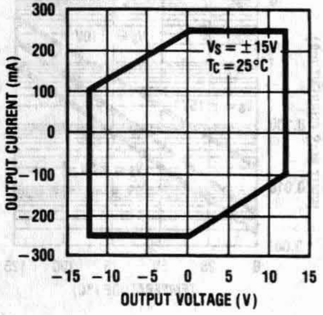
LH0033 Power Dissipation



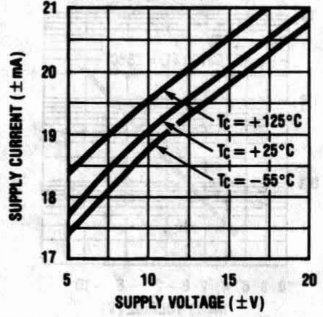
LH0063 Power Dissipation



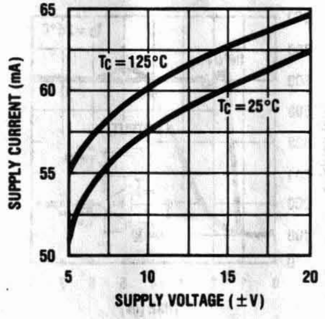
LH0063 DC Safe Operating Area



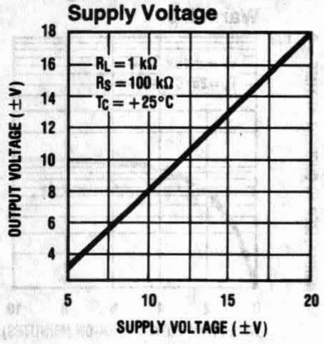
LH0033 Supply Current vs Supply Voltage



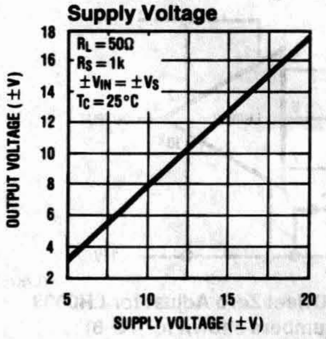
LH0063 Supply Current vs Supply Voltage



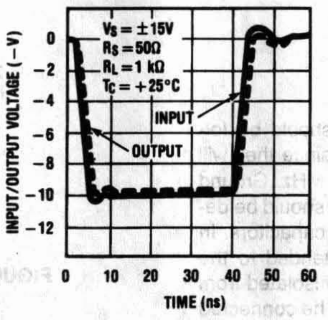
LH0033 Output Voltage vs Supply Voltage



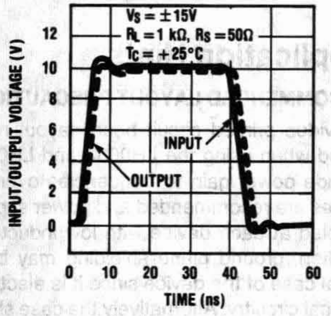
LH0063 Output Voltage vs Supply Voltage



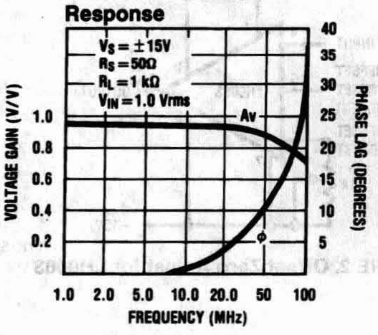
LH0033 Negative Pulse Response



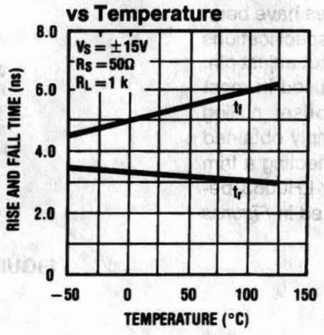
LH0033 Positive Pulse Response



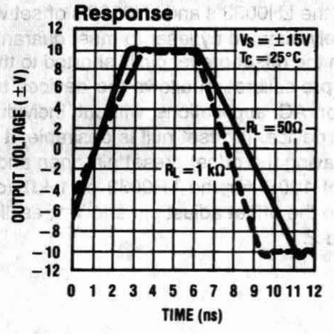
LH0033 Frequency Response



LH0033 Rise and Fall Time vs Temperature



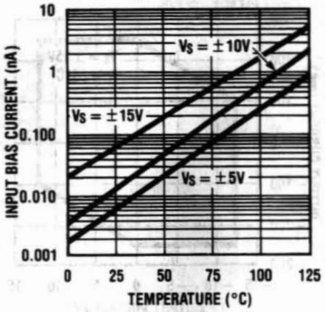
LH0063 Large Signal Pulse Response



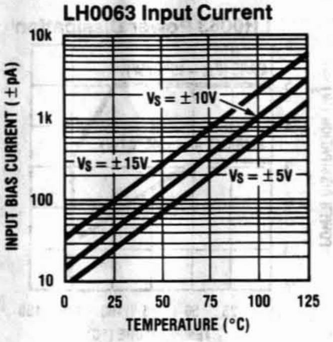
TL/K/5507–4

Typical Performance Characteristics (Continued)

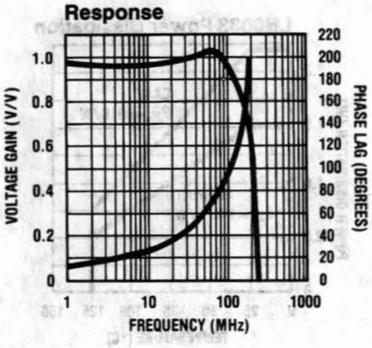
LH0033 Input Bias Current vs Temperature



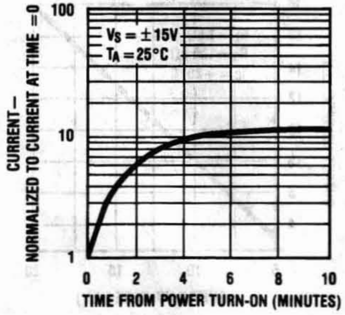
LH0063 Input Current



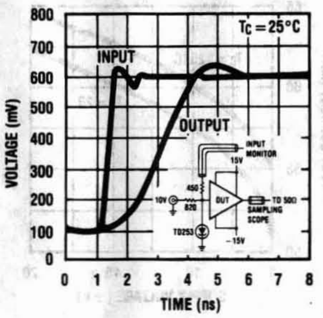
LH0063 Frequency Response



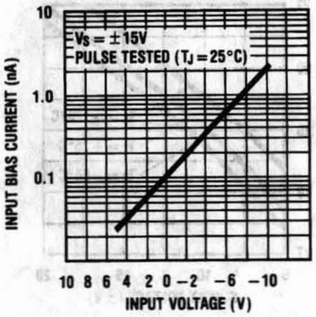
LH0033 Normalized Input Bias Current During Warm-Up



LH0063 Small Signal Rise Time



LH0033 Input Bias Current vs Input Voltage



TL/K/5507–5

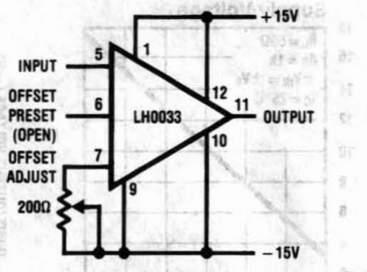
Application Hints

RECOMMENDED LAYOUT PRECAUTIONS

RF/video printed circuit board layout rules should be followed when using the LH0033 and LH0063 since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

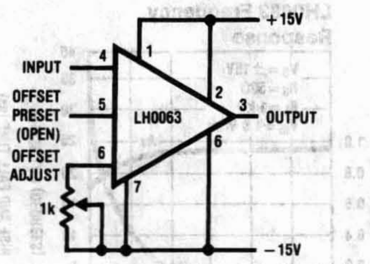
OFFSET VOLTAGE ADJUSTMENT

Both the LH0033's and LH0063's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω for the LH0033 or 1 kΩ for the LH0063 between the offset adjust pin and V⁻, as illustrated in *Figures 1* and *2*.



TL/K/5507–6

FIGURE 1. Offset Zero Adjust for LH0033 (Pin numbers shown for TO-8)



TL/K/5507–7

FIGURE 2. Offset Zero Adjust for LH0063

Application Hints (Continued)

OPERATION FROM SINGLE OR ASYMMETRICAL POWER SUPPLIES

Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.005(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically 0.99

V^+ = Positive supply voltage

V^- = Negative supply voltage

For the above example, ΔV_O would be −35mV. This may be adjusted to zero as described in *Figure 2*. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the Typical Applications section.

SHORT CIRCUIT PROTECTION

In order to optimize transient response and output swing, output current limit has been omitted from the LH0033 and LH0063. Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in *Figures 3 and 4*. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where:

$I_{SC} \leq 100$ mA for LH0033

$I_{SC} \leq 250$ mA for LH0063

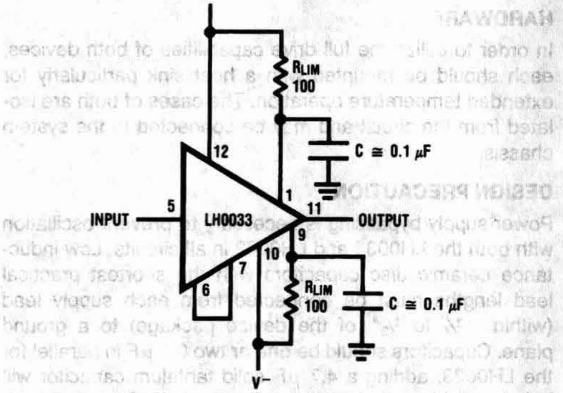


FIGURE 3. LH0033 Using Resistor Current Limiting

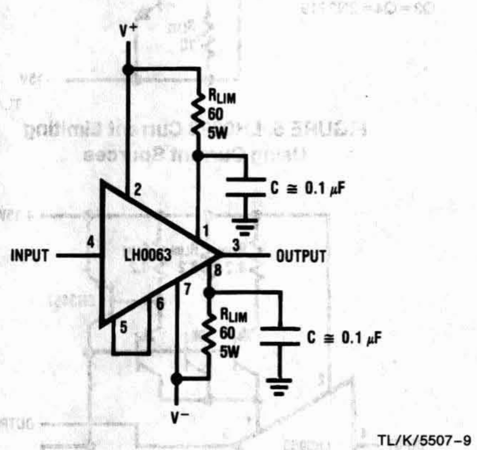


FIGURE 4. LH0063 Using Resistor Current Limiting

Application Hints (Continued)

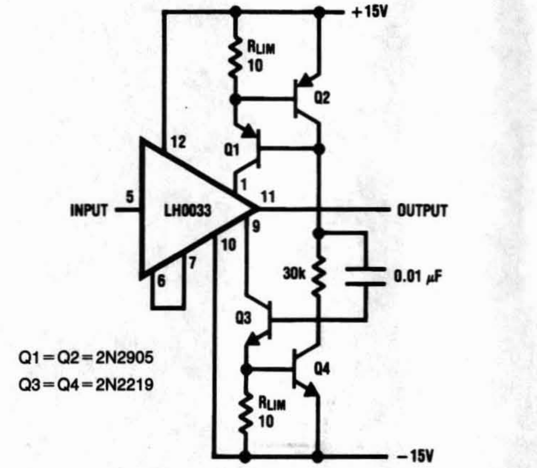
The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling $V_C{}^+$ and $V_C{}^-$ pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in *Figures 5* and *6*. In *Figures 5* and *6*, the current sources are saturated during normal operation, thus apply full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload.

For *Figure 5:*

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\text{ mA}} = 10\Omega$$

In *Figure 6*, quad transistor arrays are used to minimize can count and:

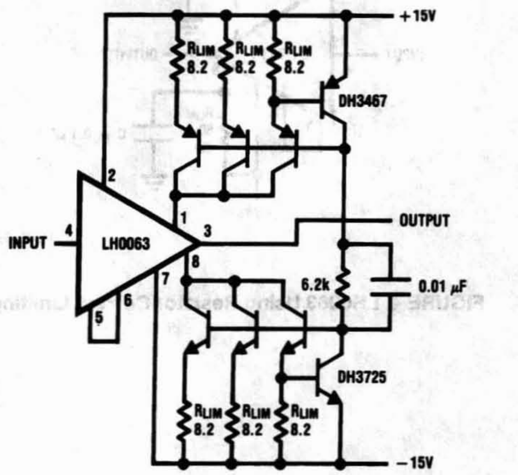
$$R_{LIM} = \frac{V_{BE}}{1/3(I_{SC})} = \frac{0.6V}{1/3(200\text{ mA})} = 8.2\Omega$$



Q1 = Q2 = 2N2905
Q3 = Q4 = 2N2219

TL/K/5507–10

FIGURE 5. LH0033 Current Limiting Using Current Sources



TL/K/5507–11

FIGURE 6. LH0063 Current Limiting Using Current Sources

CAPACITIVE LOADING

Both the LH0033 and LH0063 are designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times d_V/d_t)$ should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH0033:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\text{ mA}$$

and for the LH0063:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\text{ mA}$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below total package power rating:

$$P_D\text{pkg.} \geq P_{DC} + P_{AC}$$
$$P_D\text{pkg.} \geq (V^+ - V^-) \times I_S + P_{AC}$$
$$P_{AC} \cong (V\text{p-p})^2 \times f \times C_L$$

where:

Vp-p = Peak-to-peak output voltage swing
f = Frequency
C_L = Load Capacitance

OPERATION WITHIN AN OP AMP LOOP

Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LM6218, LM6361 or LH0032. An isolation resistor of 47Ω should be used between the op amp output and the input of LH0033. The wide bandwidths and high slew rates of the LH0033 and LH0063 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

HARDWARE

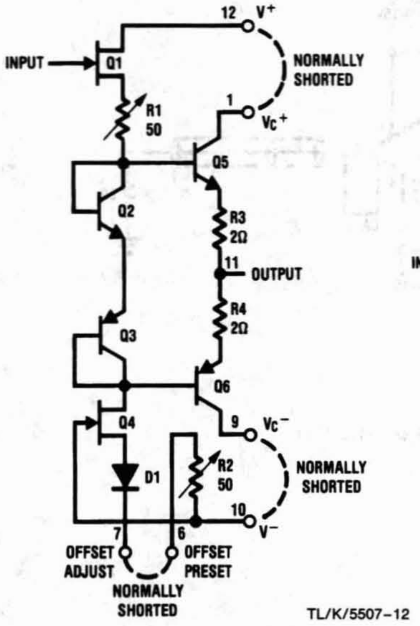
In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to the system chassis.

DESIGN PRECAUTION

Power supply bypassing is necessary to prevent oscillation with both the LH0033 and LH0063 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within <¼ to ½″ of the device package) to a ground plane. Capacitors should be one or two 0.1 µF in parallel for the LH0033; adding a 4.7 µF solid tantalum capacitor will help in troublesome instances. For the LH0063, two 0.1 µF ceramic and one 4.7 µF solid tantalum capacitors in parallel will be necessary on each supply lead.

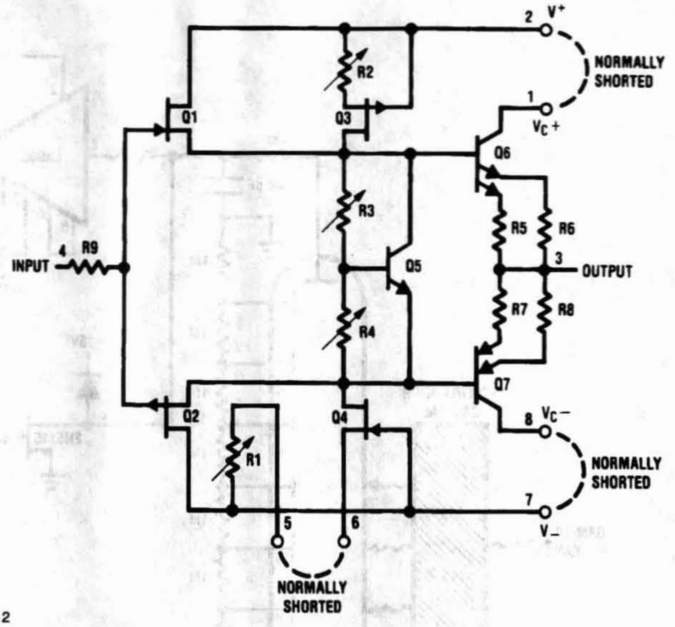
Schematic Diagrams

LH0033/LH0033A


12 V+
INPUT
Q1
NORMALLY SHORTED
R1 50
1 VC+
Q5
Q2
R3 2Ω
11 OUTPUT
R4 2Ω
Q3
Q6
Q4
9 VC−
D1
R2 50
NORMALLY SHORTED
10 V−
7 OFFSET ADJUST
6 OFFSET PRESET
NORMALLY SHORTED

TL/K/5507-12

LH0063

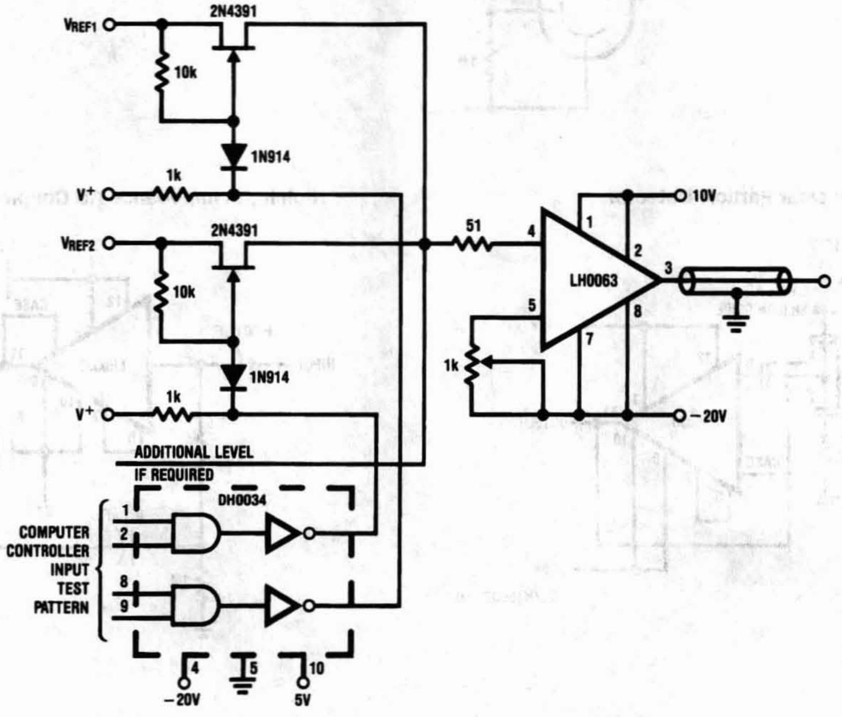

2 V+
NORMALLY SHORTED
R2
Q1
Q3
1 VC+
Q6
R3
R5
R6
4 R9
INPUT
Q5
3 OUTPUT
R4
R7
R8
Q7
Q2
Q4
8 VC−
R1
NORMALLY SHORTED
7 V−
5
6
NORMALLY SHORTED

TL/K/5507-13

Pin numbers shown for TO-8 ("G") package.

Typical Applications

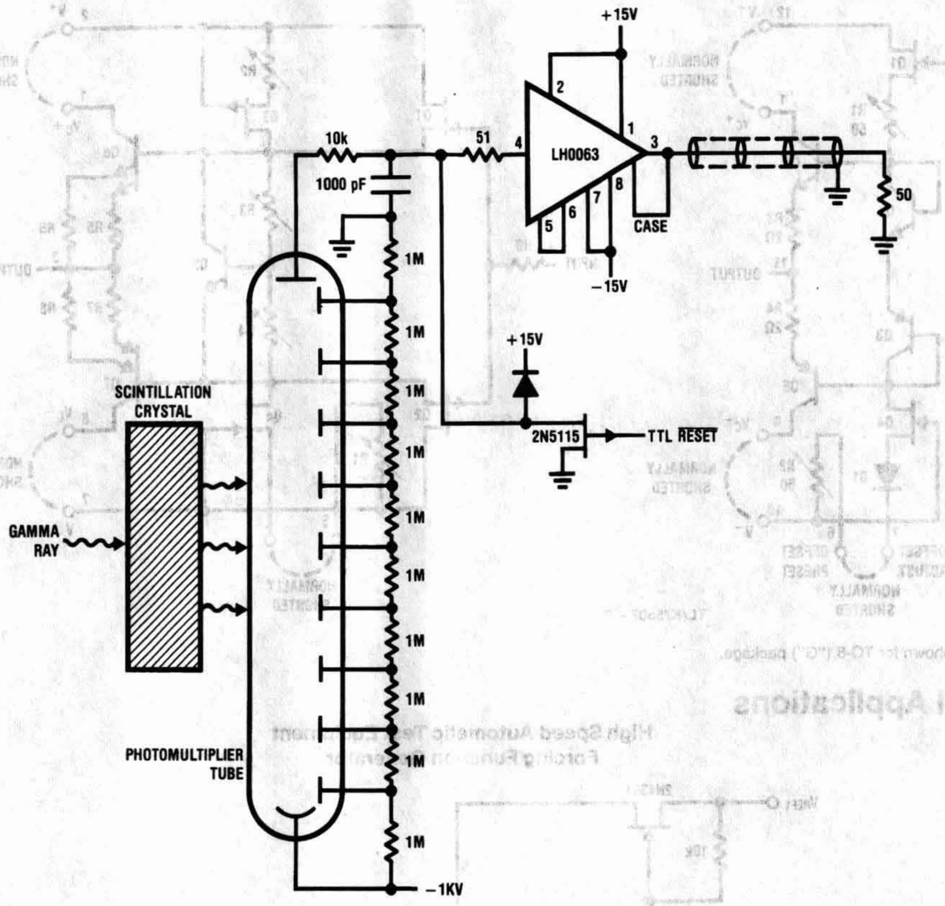
High Speed Automatic Test Equipment Forcing Function Generator


VREF1
2N4391
10k
1N914
1k
V+
VREF2
2N4391
10k
1N914
1k
V+
ADDITIONAL LEVEL IF REQUIRED
DH0034
1
2
8
9
COMPUTER CONTROLLER INPUT TEST PATTERN
4
−20V
5
10
5V
51
4
1
10V
2
LH0063
3
5
8
1k
7
−20V

TL/K/5507-14

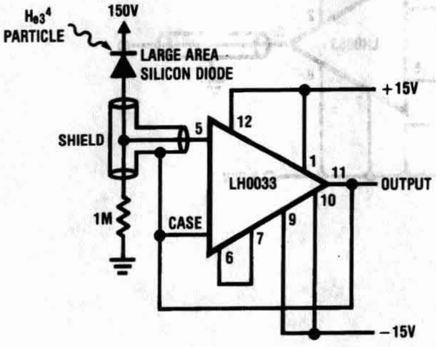
Typical Applications (Continued)

Gamma Ray Pulse Integrator


+15V
10k
1000 pF
51
4
2
1
3
LH0063
5
6
7
8
CASE
−15V
50
1M
+15V
2N5115
TTL $\overline{RESET}$
SCINTILLATION CRYSTAL
GAMMA RAY
PHOTOMULTIPLIER TUBE
−1KV

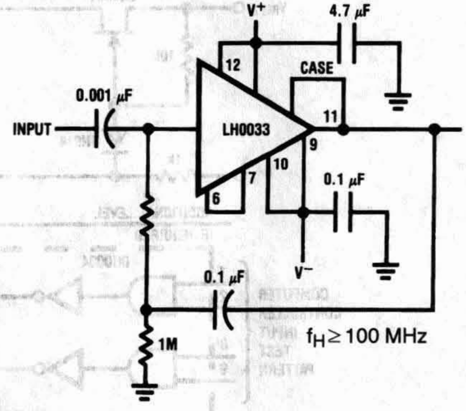
TL/K/5507–15

Nuclear Particle Detector


He_3^4 PARTICLE
150V
LARGE AREA SILICON DIODE
SHIELD
5
12
LH0033
1
11
OUTPUT
10
9
7
6
CASE
1M
+15V
−15V

TL/K/5507–16

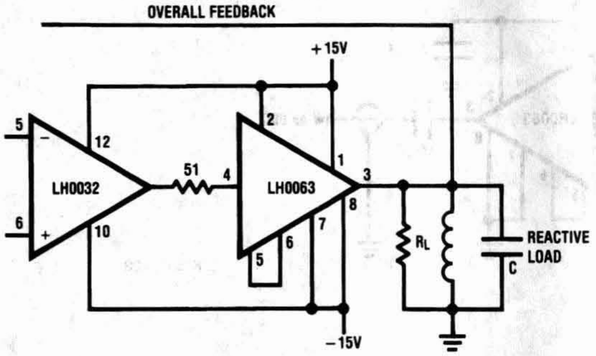
High Input Impedance AC Coupled Amplifier


V+
4.7 μF
12
CASE
0.001 μF
INPUT
LH0033
11
9
10
7
6
0.1 μF
V−
0.1 μF
1M
$f_H \geq 100$ MHz

TL/K/5507–17

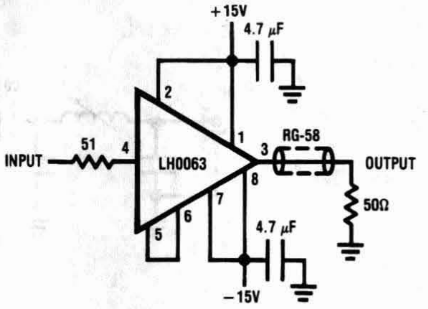
Typical Applications (Continued)

Isolation Buffer


OVERALL FEEDBACK
+15V
5
6
12
10
LH0032
51
4
2
1
LH0063
3
8
5
6
7
RL
REACTIVE LOAD
C
−15V

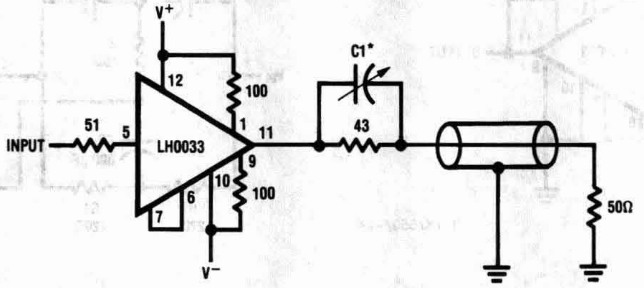
TL/K/5507-18

Coaxial Cable Driver


+15V
4.7 μF
2
INPUT
51
4
LH0063
1
3
8
RG-58
OUTPUT
50Ω
5
6
7
4.7 μF
−15V

TL/K/5507-19

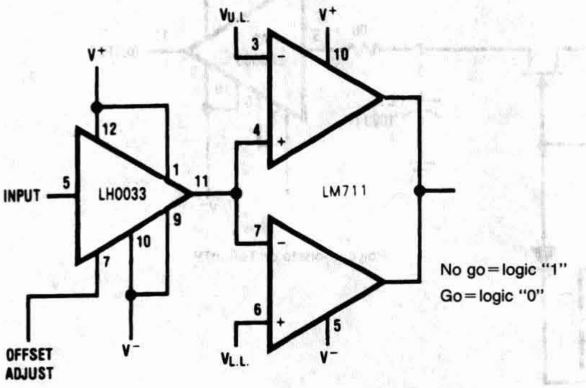
Coaxial Cable Driver


V+
12
100
C1*
INPUT
51
5
LH0033
1
11
43
9
10
100
6
7
V−
50Ω

TL/K/5507-20

*Select C1 for optimum pulse response

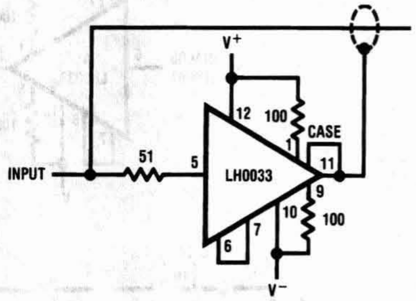
High Input Impedance Comparator with Offset Adjust


VU.L.
V+
3
10
V+
12
4
INPUT
5
LH0033
1
11
LM711
9
10
7
7
6
5
OFFSET ADJUST
V−
VL.L.
V−

No go = logic "1"
Go = logic "0"

TL/K/5507-21

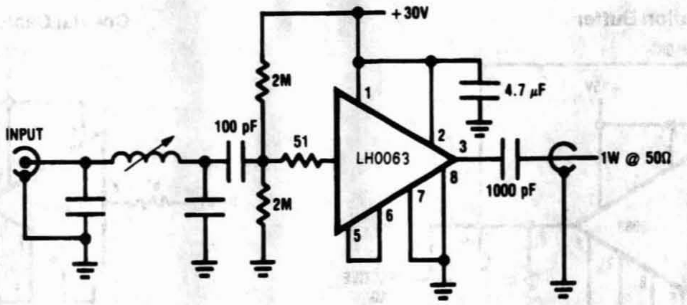
Instrumentation Shield/Line Driver


V+
12
100
CASE
INPUT
51
5
LH0033
1
11
9
10
100
6
7
V−

TL/K/5507-22

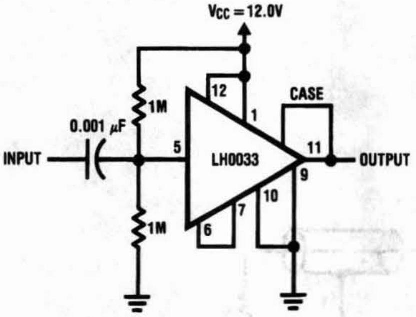
Typical Applications (Continued)

1W CW Final Amplifier


+30V
2M
4.7 μF
INPUT
100 pF
51
1
2
3
LH0063
1W @ 50Ω
8
1000 pF
7
6
5
2M

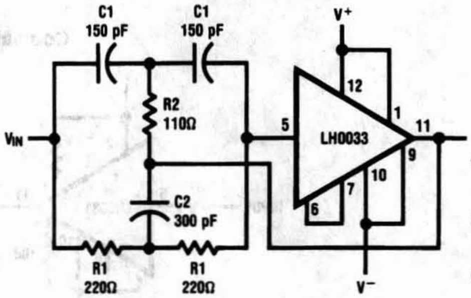
TL/K/5507-23

Single Supply AC Amplifier


V_{CC} = 12.0V
12
CASE
1M
1
0.001 μF
INPUT
5
LH0033
11
OUTPUT
9
10
7
1M
6

TL/K/5507-24

4.5 MHz Notch Filter


C1
150 pF
C1
150 pF
V+
12
R2
110Ω
1
5
11
V_{IN}
LH0033
9
10
7
C2
300 pF
6
R1
220Ω
R1
220Ω
V−

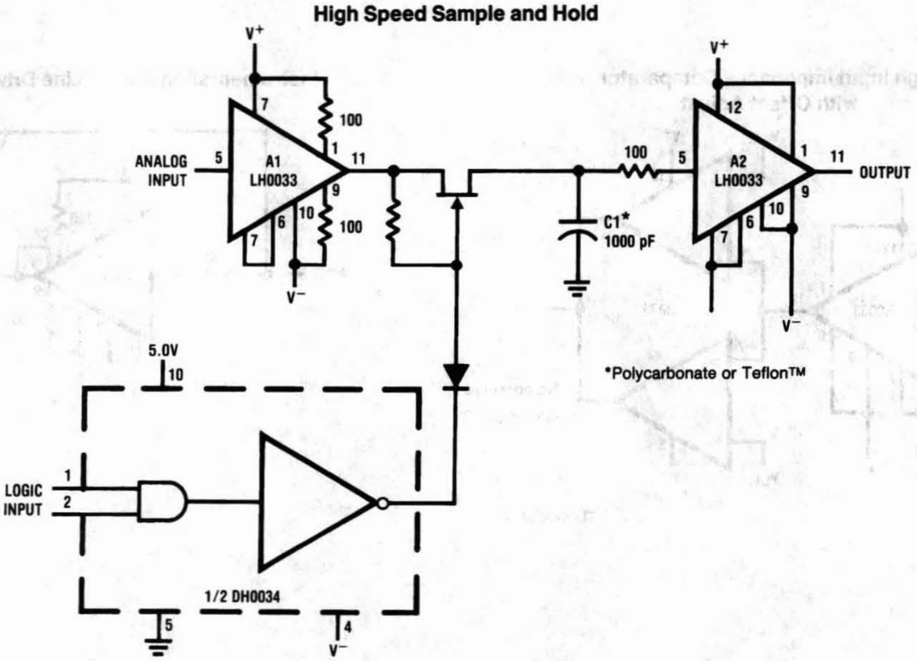
$$f_O = \frac{1}{2\pi R1C1}$$

$$R1 = 2\ R2$$

$$C1 = \frac{C2}{2}$$

TL/K/5507-25

High Speed Sample and Hold


V+
7
100
1
ANALOG INPUT
5
A1
LH0033
11
9
10
6
100
7
V−
100
5
C1*
1000 pF
V+
12
A2
LH0033
1
11
OUTPUT
9
10
6
7
V−
5.0V
10
LOGIC INPUT
1
2
1/2 DH0034
5
4
V−

*Polycarbonate or Teflon™

TL/K/5507-26

National Semiconductor

LH4001 Wideband Current Buffer

General Description

The LH4001 is a high speed unity gain buffer designed to provide high current drive capability at frequencies from DC to over 25 MHz. It is capable of providing a continuous output current of ±100 mA and a peak of ±200 mA.

The LH4001 is designed to fulfill a wide range of applications such as impedance transformation, high impedance input buffers for A/D converters and comparators, as well as high speed line drivers. It is also suitable for use in current booster applications within an op amp loop. This allows the output current capability of existing op amps to be increased to ±100 mA.

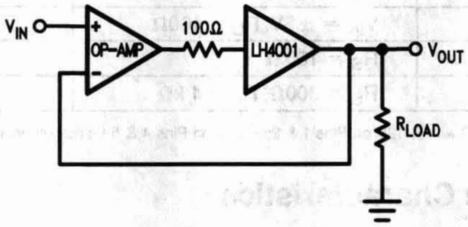
Features

- DC to 25 MHz bandwidth
- 125 V/µs slew rate
- Drives ±10V into 50Ω
- Operates from ±5 to ±20V supplies
- Output swing approaches supply voltage

Applications

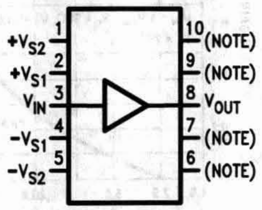
- Boost op amp output
- Buffer amplifiers
- Isolate capacitive loads
- Drive long cables

Typical Applications and Connection Diagram



TL/K/8628-1

Dual-In-Line Package



TL/K/8628-2

Top View

***Note:** Electrically connected internally. No connection should be made to these pins.

Order Number LH4001CN
See NS Package Number N10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	±22V
Continuous Output Current, I_O	±100 mA
Peak Output Current, $I_{O(peak)}$ (50 ms On/1 Sec Off)	±200 mA
Input Voltage Range, V_{IN}	$\pm V_S$
Power Dissipation	500 mW
Storage Temperature Range, T_{STG}	−65°C to +150°C
Junction Temperature, T_J	150°C
Lead Temp. (Soldering, <10 seconds)	260°C

ESD rating is to be determined.

Operating Ratings

Temperature Range, T_A	0°C to +70°C
Thermal Resistance θ_{JA}	120°C/W

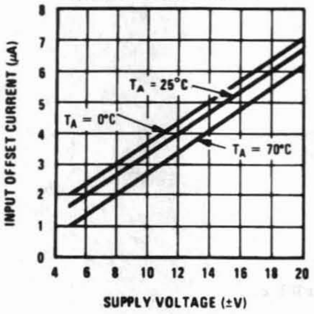
Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A_V	Voltage Gain	$R_S = 10\ k\Omega$, $R_L = 1\ k\Omega$ $V_{IN} = \pm 10V$	0.95	0.97	1	V/V
R_{IN}	Input Impedance	$R_S = 200\ k\Omega$, $R_L = 1\ k\Omega$ $V_{IN} = \pm 1.0V$	180	400		kΩ
R_{OUT}	Output Impedance	$R_S = 10\ k\Omega$, $R_L = 50\Omega$ $V_{IN} = \pm 1.0V$		6	10	Ω
V_O	Output Swing	$V_S = \pm 15V$, $R_S = 50\Omega$ $R_L = 100\Omega$, $V_{IN} = \pm 12V$	±10	±11		V
I_B	Input Bias Current	$R_S = 10\ k\Omega$, $R_L = 1\ k\Omega$		±10	±50	μA
t_r	Rise Time	$R_L = 100\Omega$, $\Delta V_{IN} = 100\ mV$		7		ns
SR	Slew Rate	$V_{IN} = \pm 5V$, $R_L = 100\Omega$		125		V/μs
I_S	Supply Current	$R_S = 10\ k\Omega$		±6	±10	mA
V_{OS}	Offset Voltage	$R_S = 300\Omega$, $R_L = 1\ k\Omega$		±10	±50	mV

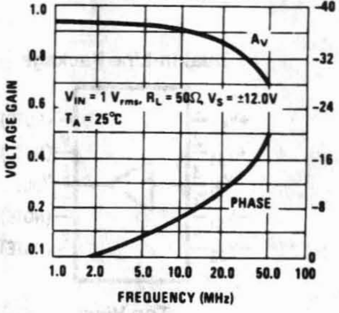
Note 1: Specification applies for $T_A = 25°C$ with +12V on Pins 1 & 2; −12V on Pins 4 & 5 unless otherwise specified.

Typical Performance Characteristics

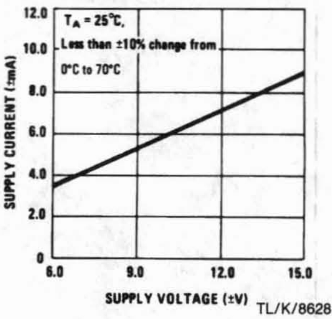
Input Offset Current



Frequency Response

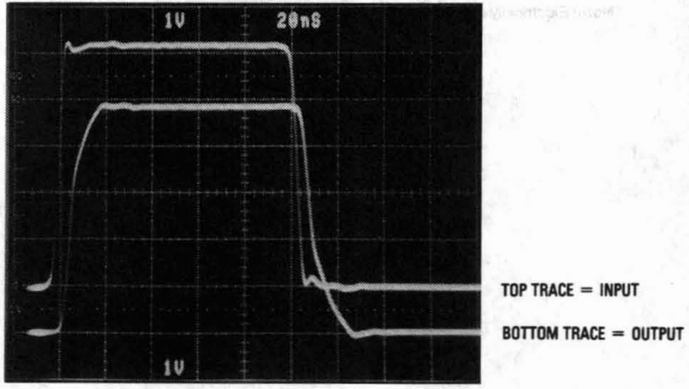


Supply Current



TL/K/8628–3

Pulse Response



TL/K/8628–10

$V_{IN} = \pm 2.5V$, $R_S = R_L = 50\Omega$

Applications Information

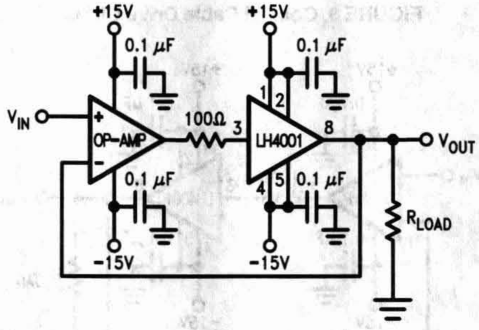
Figure 1 shows a simple implementation of a non-inverting buffer amplifier of unity gain. Popular industry standard operational amplifiers such as LF156, LF351, LF411, LF441, LM11, LM741, etc. can be used in this configuration. Due to the high bandwidth of the LH4001, it is suitable for use with most monolithic op amps.

Figure 2 shows an implementation of an inverting amplifier with output current capability in excess of ±100 mA. The gain of this amplifier is determined by the values of R_F and R_{IN}. The resistor between the non-inverting input and ground is used to minimize the output offset voltage resulting from the input bias current.

Because of its high current drive capability, the LH4001 buffer amplifier is suitable for driving terminated or unterminated co-axial cables, and high current or reactive loads.

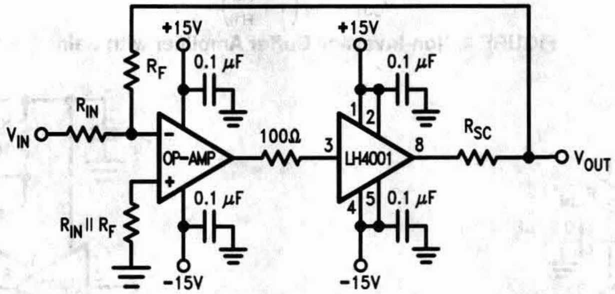
Figure 3 shows a co-axial cable drive circuit. The 43Ω resistor matches the driving source to the cable, however, its inclusion rarely will result in substantial improvement in pulse response into a terminated cable. If the 43Ω resistor is included, the output voltage to the load is about half what it would be without the near end termination.

Figure 4 shows a non-inverting amplifier with gain and output current capability in excess of ±100 mA. It is capable of providing ±10 mA into a 1 kΩ load or ±100 mA into a 100Ω load (±10V swing). *Figures 5* and *6* show two different methods of providing current limit or short circuit protection for the LH4001. In *Figure 6,* the 10Ω resistor limits the output current to approximately 70 mA. This circuit is highly recommended if there is a potential for a short circuit to occur.



TL/K/8628-4

FIGURE 1. Non-Inverting Buffer Amplifier

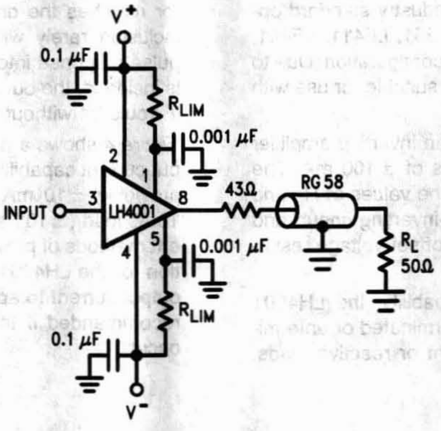


$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_{IN}}$$

TL/K/8628-6

FIGURE 2. Inverting Buffer Amplifier with Current Limit

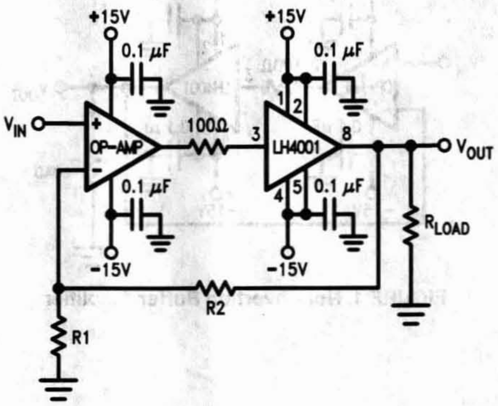
Applications Information (Continued)


V+
0.1 µF
RLIM
0.001 µF
2
1
3
INPUT
LH4001
8
43Ω
RG 58
RL
50Ω
5
4
0.001 µF
RLIM
0.1 µF
V−

$R_{LIM} = 100\Omega$, 1W

TL/K/8628-7

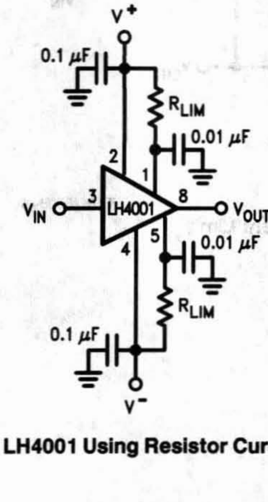
FIGURE 3. Coaxial Cable Drive Circuit


+15V
0.1 µF
+15V
0.1 µF
VIN
+
OP-AMP
−
100Ω
3
1
2
LH4001
8
VOUT
0.1 µF
4
5
0.1 µF
RLOAD
−15V
−15V
R2
R1

TL/K/8628-5

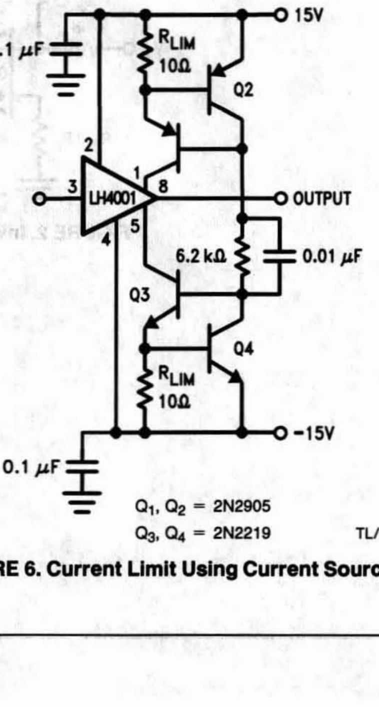
$$V_{OUT} = V_{IN}\left(1 + \frac{R2}{R1}\right)$$

FIGURE 4. Non-Inverting Buffer Amplifier with Gain


V+
0.1 µF
RLIM
0.01 µF
2
1
3
VIN
LH4001
8
VOUT
5
4
0.01 µF
RLIM
0.1 µF
V−

TL/K/8628-8

FIGURE 5. LH4001 Using Resistor Current Limiting


15V
0.1 µF
RLIM
10Ω
Q2
2
1
3
LH4001
8
OUTPUT
5
4
6.2 kΩ
0.01 µF
Q3
Q4
RLIM
10Ω
−15V
0.1 µF

Q_1, Q_2 = 2N2905

Q_3, Q_4 = 2N2219

TL/K/8628-9

FIGURE 6. Current Limit Using Current Sources

National Semiconductor

LH4002 Wideband Video Buffer

General Description

The LH4002 is a high speed voltage follower designed to drive video signals from DC up to 200 MHz. At voltage supplies of ±5V, the LH4002 will provide up to 40 mA into 50Ω at slew rates in excess of 1000 V/μs.

The device is intended to fulfill a wide range of high speed applications including video distribution, impedance transformation, and load isolation. It is also suitable for use in current booster applications within an op amp loop. This allows the output current capability of existing op amps to be increased.

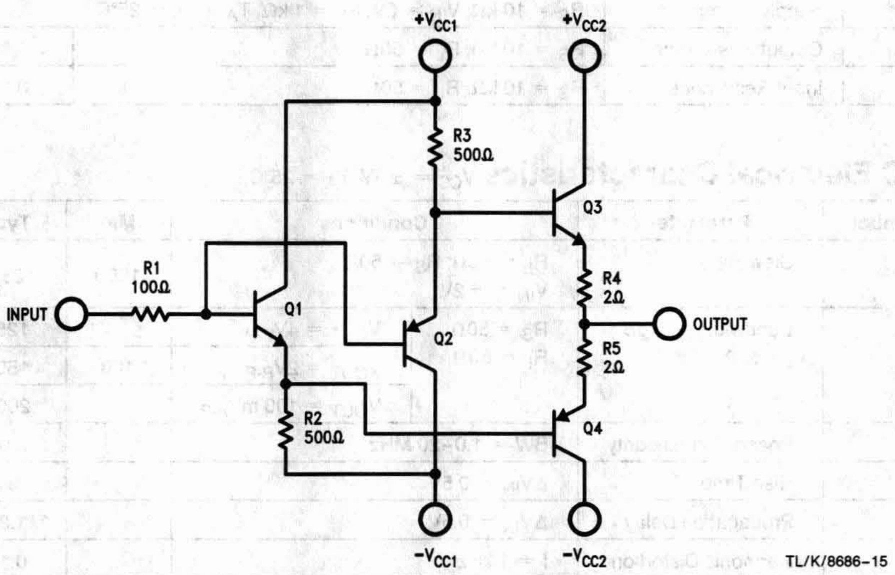
Features

- DC to 200 MHz Bandwidth with $V_S = \pm 5V$
- 1250 V/μs Slew Rate into 50Ω
- 150 MHz Bandwidth with $V_S = \pm 5V$, $R_L = 50\Omega$ and Voltage Swing = 2 V_{P-P}

Applications

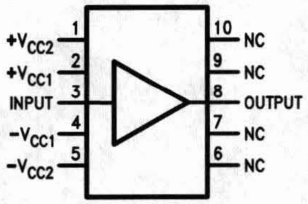
- Wideband Amplifier Buffer
- Wideband Line Driver

Schematic and Connection Diagrams


+VCC1
+VCC2
R3
500Ω
Q3
R1
100Ω
INPUT
Q1
Q2
R4
2Ω
OUTPUT
R5
2Ω
R2
500Ω
Q4
-VCC1
-VCC2

TL/K/8686-15

Dual-In-Line Package


+VCC2
+VCC1
INPUT
-VCC1
-VCC2
1
2
3
4
5
10
9
8
7
6
NC
NC
OUTPUT
NC
NC

TL/K/8686-2

Top View

Order Number LH4002CN
See NS Package Number N10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	±6V
Input Voltage Range, V_{IN}	$\pm V_S$
Continuous Output Current, I_O	±60 mA
Storage Temperature Range, T_{STG}	−65°C to +150°C
Operating Temperature Range, T_A	
LH4002C	−25°C to +85°C
Junction Temperature, T_J	150°C
Lead Temperature (Soldering, 10 sec)	300°C

ESD rating is to be determined.

DC Electrical Characteristics $V_{CC} = \pm 5V$, $T_{min} \le T_A \le T_{max}$ unless otherwise stated.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$T_A = T_J = 25°C$ $R_S = 150\Omega$, $R_L = 50\Omega$			20	50	mV
I_B	Input Bias Current	$R_S = 1\ k\Omega$, $R_L = 50\Omega$			100	200	μA
A_V	DC Voltage Gain	$R_S = 10\ k\Omega$, $R_L = 1.0\ k\Omega$, $V_{IN} = \pm 2V$		0.95	0.97		V/V
V_O	Output Voltage Swing	$R_S = 150\Omega$, $V_{IN} = \pm 2.5V$	$R_L = 1\ k\Omega$	±2.2	±2.4		V
			$T_A = 25°C$, $R_L = 50\Omega$	±2.0	±2.2		V
I_S	Supply Current	$R_S = 10\ k\Omega$, $V_{IN} = 0V$, $R_L = 1\ k\Omega$, $T_A = T_J = 25°C$			20	35	mA
R_{OUT}	Output Resistance	$R_S = 10\ k\Omega$, $R_L = 50\Omega$			6	10	Ω
R_{IN}	Input Resistance	$R_S = 10\ k\Omega$, $R_L = 50\Omega$		10	18		kΩ

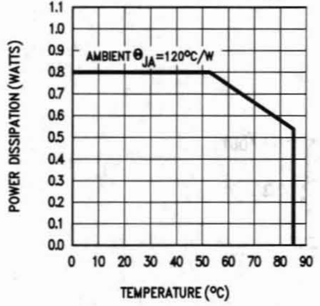
AC Electrical Characteristics $V_{CC} = \pm 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
S_R	Slew Rate	$R_L = 50\Omega$, $R_S = 50\Omega$ $V_{IN} = \pm 2V$		1000	1250		V/μs
f_{3dB}	Bandwidth, −3 dB (Note 2)	$R_S = 50\Omega$ $R_L = 50\Omega$	$V_{OUT} = 4V_{P\text{-}P}$		125		MHz
			$V_{OUT} = 2V_{P\text{-}P}$	100	150		MHz
			$V_{OUT} = 100\ mV_{P\text{-}P}$		200		MHz
	Phase Non-Linearity	BW = 1.0–20 MHz			2.0		degrees
t_r	Rise Time	$\Delta V_{IN} = 0.5V$			3		ns
t_d	Propagation Delay	$\Delta V_{IN} = 0.5V$			1.2		ns
THD	Harmonic Distortion	f = 1 kHz			0.1		%

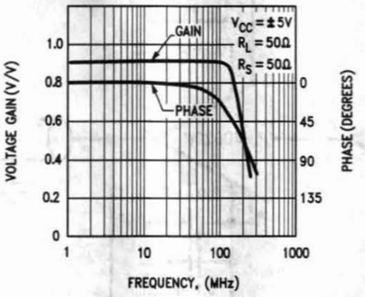
Note 1: Under normal operating conditions $+V_{CC1}$ and $+V_{CC2}$ should be connected together, and $-V_{CC1}$ and $-V_{CC2}$ should be connected together.

Note 2: Guaranteed by design. This parameter is sample tested.

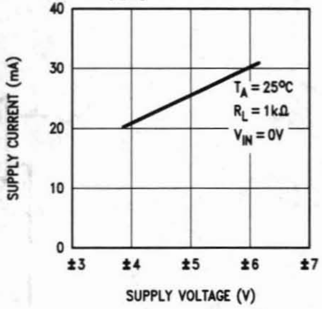
Typical Performance Characteristics


Maximum Power Dissipation Dual-In-Line Package

TL/K/8686–12

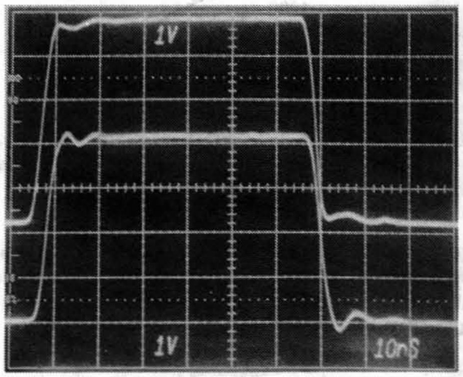

Frequency Response

TL/K/8686–5


Supply Current

TL/K/8686–6

Pulse Response

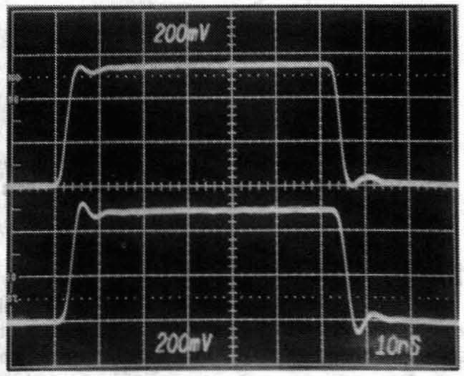


TL/K/8686–7

TOP TRACE = INPUT

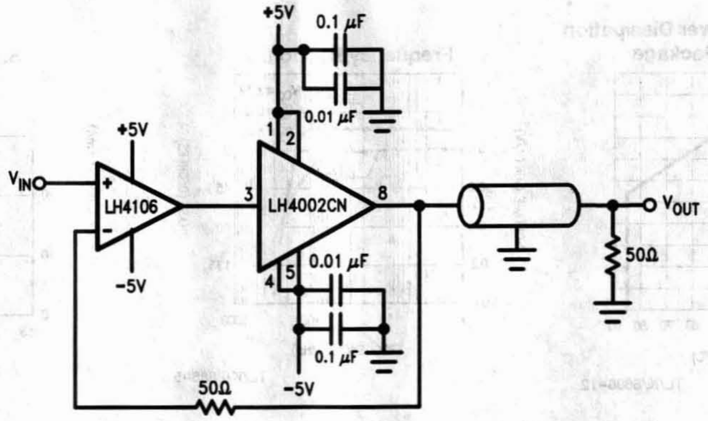
BOTTOM TRACE = OUTPUT

V_S = ±5V
R_L = 50Ω



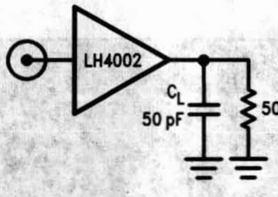
TL/K/8686–8

Typical Applications



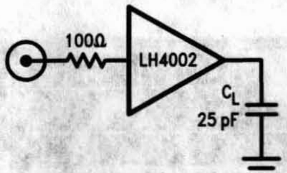
TL/K/8686-11

FIGURE 1. Wideband Unity Gain Amplifier Using LH4002CN



TL/K/8686-9

FIGURE 2. Compensation for Capacitive Loads



TL/K/8686-10

FIGURE 3. Compensation for Capacitive Loads

Applications Information

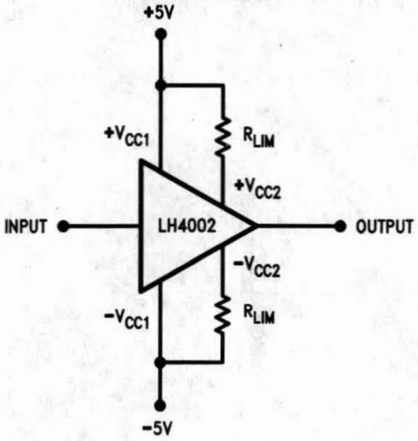
The high speed performance of the LH4002 can only be realized by taking certain precautions in circuit layout and power supply decoupling. Low inductance ceramic chip or disc power supply decoupling capacitors of 0.01 μF in parallel with 0.1 μF should be connected with the shortest practical lead length between device supply leads and a ground plane. Failure to follow these rules can result in oscillations. When driving a capacitive load such as inputs to flash converters, the circuits in *Figure 2* and *3* can be used to minimize the amount of overshoot and ringing at the outputs. *Figure 2* indicates that a 50Ω should be placed in parallel with the load and *Figure 3* recommends that a 100Ω resistor be placed in series with the input to the LH4002.

Short Circuit Protection

In order to optimize transient response and output swing, output current limits have been omitted from the LH4002. Short circuit protection may be added by inserting appropriate value resistors between $+V_{CC1}$ and $+V_{CC2}$ pins and between $-V_{CC1}$ and $-V_{CC2}$ pins as illustrated in *Figure 4*. Resistor values may be predicted by:

$$R_{LIM} = \frac{+V_{CC1}}{I_{SC}} = \frac{-V_{CC1}}{I_{SC}}$$

where $I_{SC} \leq 100$ mA. The inclusion of 50Ω limiting resistors in the collectors of the output transistors limits the short circuit current to approximately 100 mA without reducing the output voltage swing.



TL/K/8686-20

FIGURE 4. LH4002 Using Resistor Current Limiting

National Semiconductor

LM102/LM302 Voltage Followers

General Description

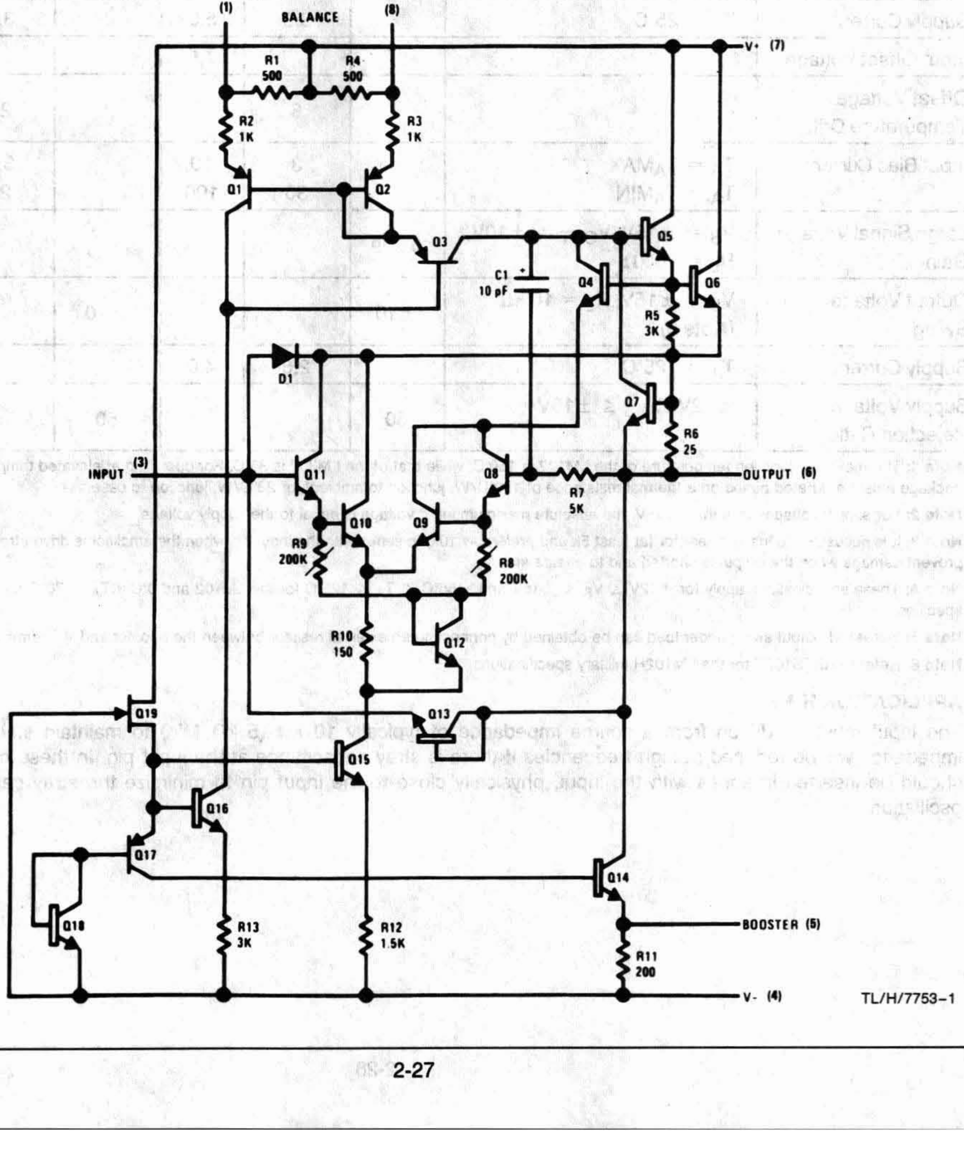
The LM102 series are high-gain operational amplifiers designed specifically for unity-gain voltage follower applications. Built on a single silicon chip, the devices incorporate advanced processing techniques to obtain very low input current and high input impedance. Further, the input transistors are operated at zero collector-base voltage to virtually eliminate high temperature leakage currents. It can therefore be operated in a temperature stabilized component oven to get extremely low input currents and low offset voltage drift.

The LM102, which is designed to operate with supply voltages between ±12V and ±15V, also features low input capacitance as well as excellent small signal and large signal frequency response—all of which minimize high frequency gain error. Because of the low wiring capacitances inherent in monolithic construction, this fast operation can be realized without increasing power consumption.

Features

- Fast slewing — 10V/μs
- Low input current — 10 nA (max)
- High input resistance — 10,000 MΩ
- No external frequency compensation required
- Simple offset balancing with optional 1 kΩ potentiometer
- Plug-in replacement for both the LM101 and LM709 in voltage follower applications

Schematic Diagram


(1)
BALANCE
(8)
V+ (7)
R1 500
R4 500
R2 1K
R3 1K
Q1
Q2
Q3
Q4
Q5
Q6
C1 10 pF
R5 3K
D1
Q7
R6 25
INPUT (3)
Q11
Q8
R7 5K
OUTPUT (6)
Q10
Q9
R9 200K
R8 200K
R10 150
Q12
Q13
Q19
Q15
Q16
Q17
Q14
Q18
R13 3K
R12 1.5K
BOOSTER (5)
R11 200
V- (4)

TL/H/7753-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite
Operating Free Air Temperature Range	
LM102	−55°C to +125°C
LM302	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM102			LM302			Units
		Min	Typ	Max	Min	Type	Max	
Input Offset Voltage	$T_A = 25°C$		2	5		5	15	mV
Input Bias Current	$T_A = 25°C$		3	10		10	30	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		10^9	10^{12}		Ω
Input Capacitance				3.0		3.0		pF
Large Signal Voltage Gain	$T_A = 25°C$, V_S ±15V, $V_{OUT} = \pm 10V$, $R_L = 8\ k\Omega$	0.999	0.9996		0.9985	0.9995	1.0	V/V
Output Resistance	$T_A = 25°C$		0.8	2.5		0.8	2.5	Ω
Supply Current	$T_A = 25°C$		3.5	5.5		3.5	5.5	mA
Input Offset Voltage				7.5			20	mV
Offset Voltage Temperature Drift			6			20		μV/°C
Input Bias Current	$T_A = T_AMAX$ $T_A = T_AMIN$		3 30	10 100		3.0 20	15 50	nA nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 10\ k\Omega$	0.999						
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ (Note 5)	±10			±10			V
Supply Current	$T_A = 125°C$		2.6	4.0				mA
Supply Voltage Rejection Ratio	$\pm 12V \le V_S \le \pm 15V$	60			60			dB

Note 1: The maximum junction temperature of the LM102 is 150°C, while that of the LM302 is 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 20°C/W, junction to case.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: It is necessary to insert a resistor (at least 5k and preferably 10k) in series with the input pin when the amplifier is driven from low impedance sources to prevent damage when the output is shorted and to ensure stability.

Note 4: These specifications apply for $\pm 12V \le V_S \le \pm 15V$ and $-55°C \le T_A \le 125°C$ for the LM102 and $0°C \le T_A \le 70°C$ for the LM302 unless otherwise specified.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

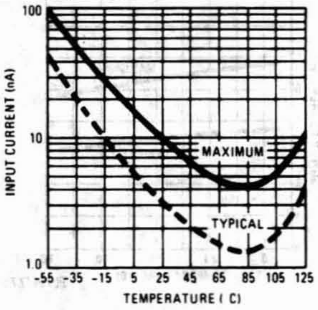
Note 6: Refer to RETS102X for the LM102H military specifications.

APPLICATION HINT

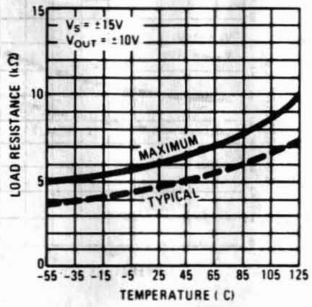
The input must be driven from a source impedance of typically 10 kΩ (5 kΩ Min) to maintain stability. The total source impedance will be reduced at high frequencies if there is stray capacitance at the input pin. In these cases, a 10 kΩ resistor should be inserted in series with the input, physically close to the input pin to minimize the stray capacitance and prevent oscillation.

Guaranteed Performance Characteristics LM102

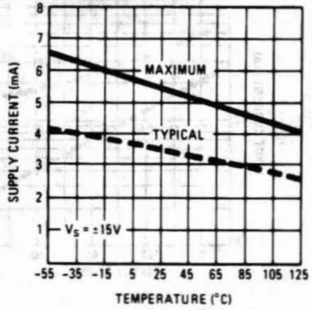
Input Current



Output Swing



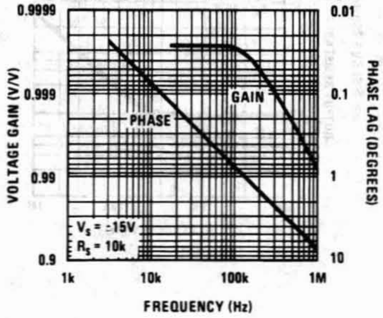
Supply Current



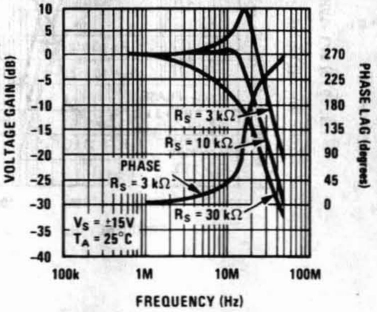
TL/H/7753-7

Typical Performance Characteristics LM102

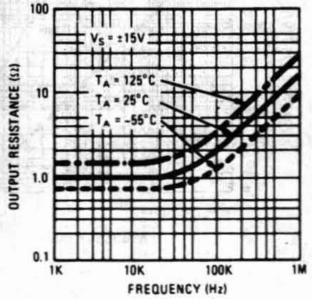
Voltage Gain and Phase Lag



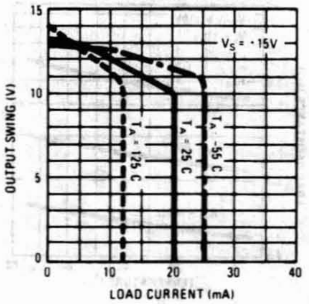
Voltage Gain and Phase Lag



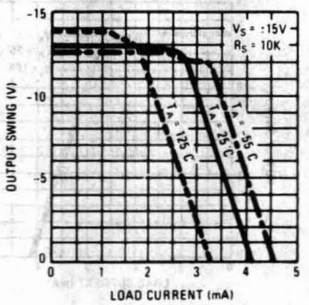
Output Resistance



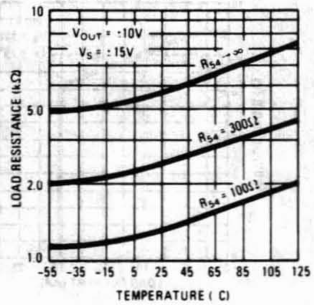
Positive Output Swing



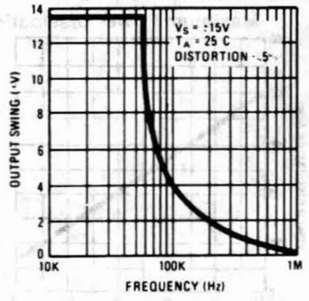
Negative Output Swing



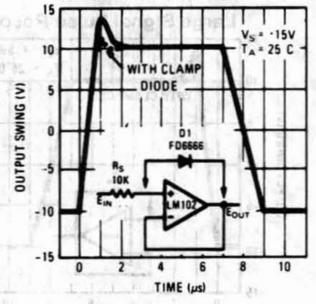
Output Swing



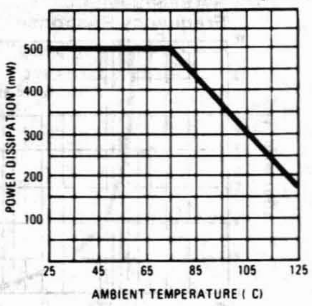
Large Signal Frequency Response



Large Signal Pulse Response



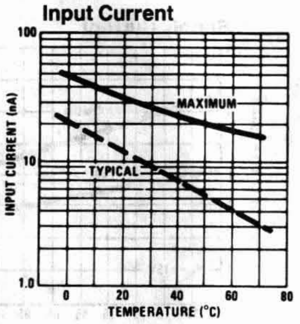
Maximum Power Dissipation



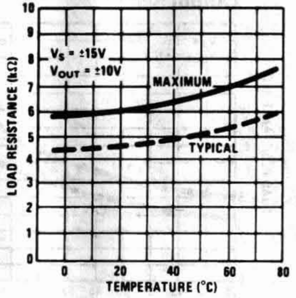
TL/H/7753-8

Guaranteed Performance Characteristics LM302

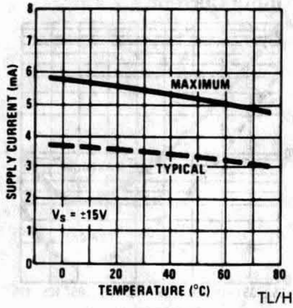
Input Current



Output Swing



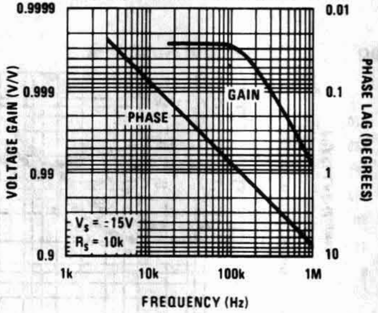
Supply Current



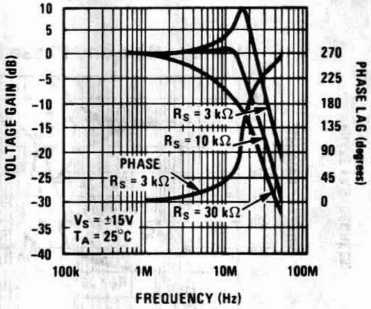
TL/H/7753–9

Typical Performance Characteristics LM302

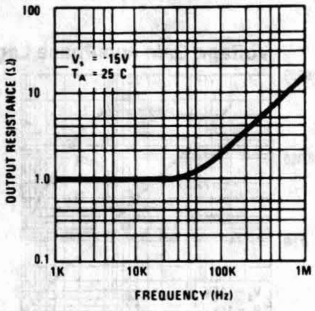
Voltage Gain and Phase Lag



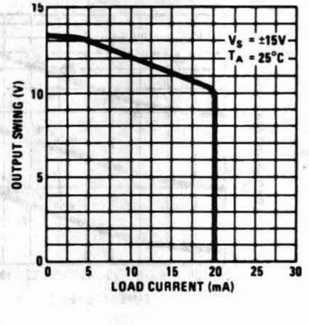
Voltage Gain and Phase Lag



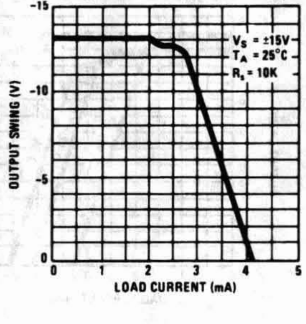
Output Resistance



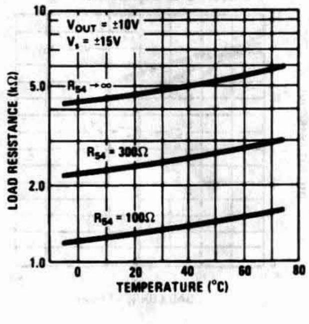
Positive Output Swing



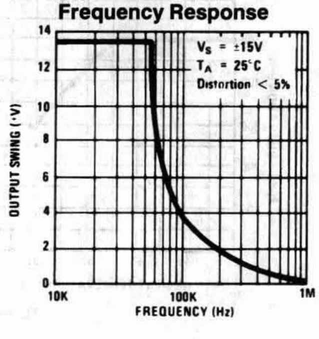
Negative Output Swing



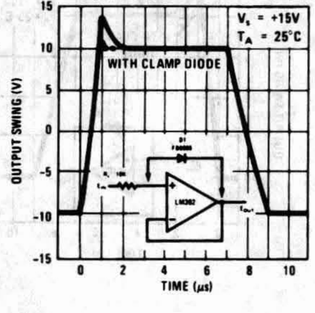
Output Swing



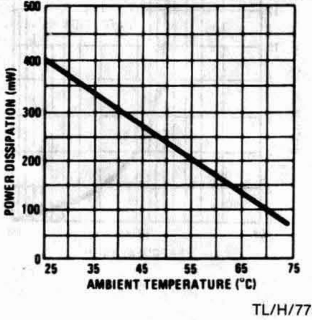
Large Signal Frequency Response



Large Signal Pulse Response



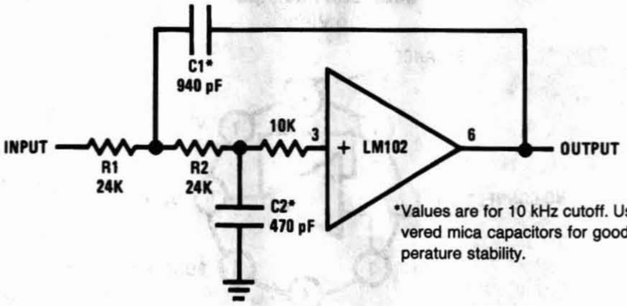
Maximum Power Dissipation



TL/H/7753–10

Typical Applications

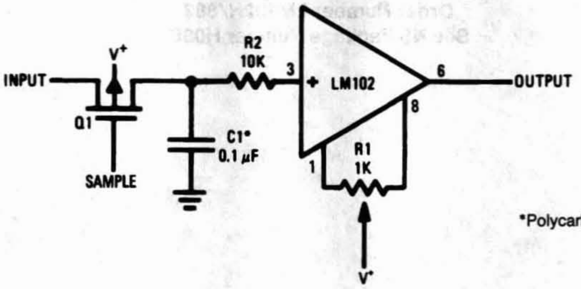
Low Pass Active Filter


C1*
940 pF
INPUT
R1
24K
R2
24K
10K
3
+ LM102
6
OUTPUT
C2*
470 pF

*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

TL/H/7753–3

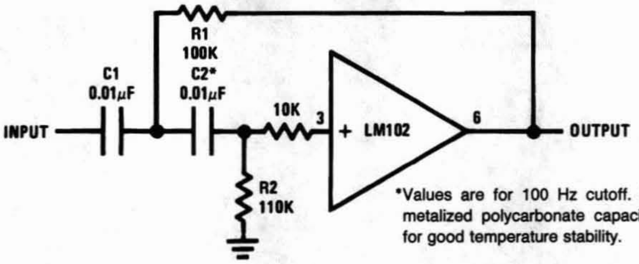
Sample and Hold with Offset Adjustment


INPUT
V+
Q1
SAMPLE
R2
10K
3
+ LM102
6
OUTPUT
8
C1*
0.1 μF
1
R1
1K
V+

*Polycarbonate-dielectric capacitor.

TL/H/7753–4

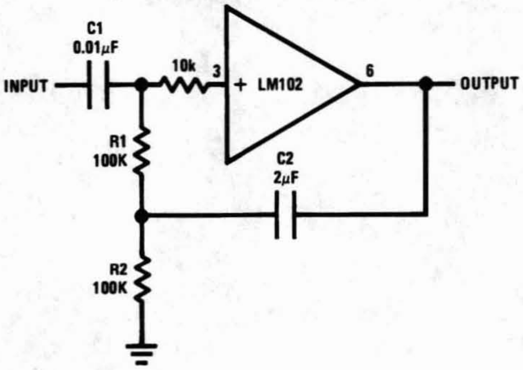
High Pass Active Filter


R1
100K
C1
0.01μF
C2*
0.01μF
INPUT
10K
3
+ LM102
6
OUTPUT
R2
110K

*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

TL/H/7753–5

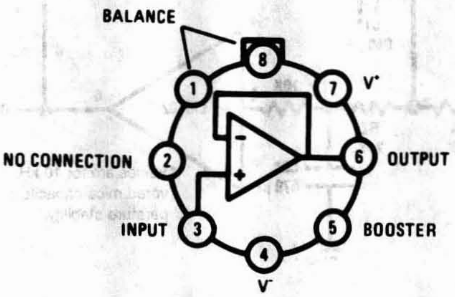
High Input Impedance AC Amplifier


C1
0.01μF
INPUT
10k
3
+ LM102
6
OUTPUT
R1
100K
C2
2μF
R2
100K

TL/H/7753–6

Connection Diagram

Metal Can Package
Top View


BALANCE
8
1
7
V+
NO CONNECTION
2
6
OUTPUT
INPUT
3
5
BOOSTER
4
V-
−
+

TL/H/7753–2

Order Number LM102H/883
See NS Package Number H08C

National Semiconductor

LM110/LM210/LM310 Voltage Follower

General Description

The LM110 series are monolithic operational amplifiers internally connected as unity-gain non-inverting amplifiers. They use super-gain transistors in the input stage to get low bias current without sacrificing speed. Directly interchangeable with 101, 741 and 709 in voltage follower applications, these devices have internal frequency compensation and provision for offset balancing.

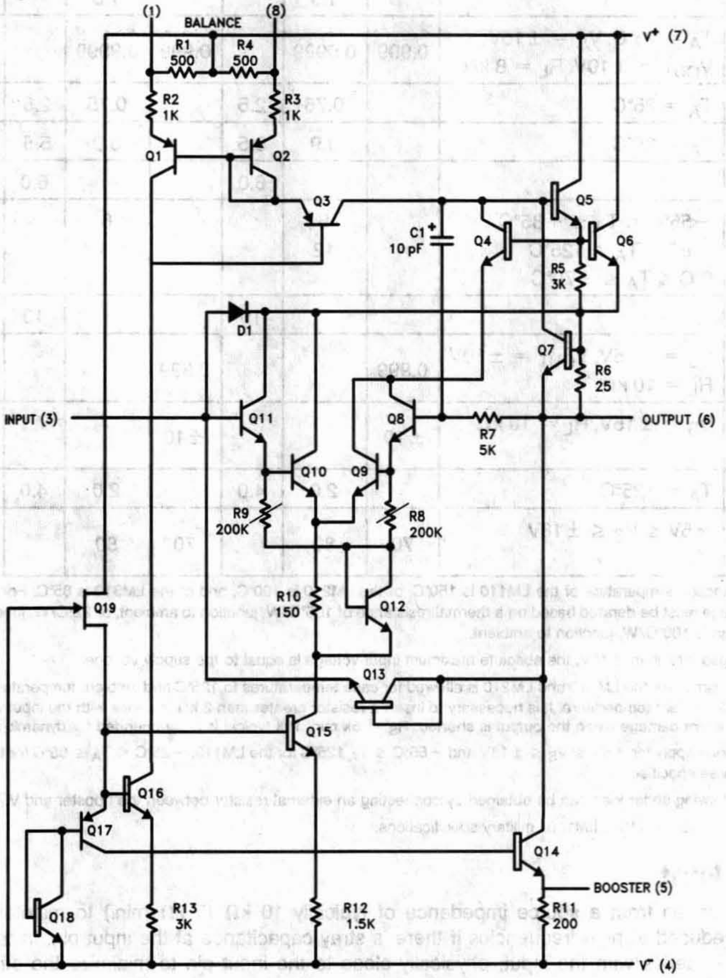
The LM110 series are useful in fast sample and hold circuits, active filters, or as general-purpose buffers. Further, the frequency response is sufficiently better than standard IC amplifiers that the followers can be included in the feedback loop without introducing instability. They are plug-in replacements for the LM102 series voltage followers, offering lower offset voltage, drift, bias current and noise in addition to higher speed and wider operating voltage range.

The LM110 is specified over a temperature range $-55^\circ C \le T_A \le +125^\circ C$, the LM210 from $-25^\circ C \le T_A \le +85^\circ C$ and the LM310 from $0^\circ C \le T_A \le +70^\circ C$.

Features

■ Input current	10 nA max over temperature
■ Small signal bandwidth	20 MHz
■ Slew rate	30 V/µs
■ Supply voltage range	±5V to ±18V

Schematic Diagram


(1)
BALANCE
(8)
R1 500
R4 500
V⁺ (7)
R2 1K
R3 1K
Q1
Q2
Q3
Q5
C1 10 pF
Q4
Q6
R5 3K
D1
Q7
R6 25
INPUT (3)
Q11
Q8
R7 5K
OUTPUT (6)
Q10
Q9
R9 200K
R8 200K
R10 150
Q12
Q19
Q13
Q15
Q16
Q17
Q14
BOOSTER (5)
Q18
R13 3K
R12 1.5K
R11 200
V⁻ (4)

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
LM110	−55°C to +125°C
LM210	−25°C to +85°C
LM310	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM110			LM210			LM310			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		1.5	4.0		1.5	4.0		2.5	7.5	mV
Input Bias Current	$T_A = 25°C$		1.0	3.0		1.0	3.0		2.0	7.0	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Capacitance			1.5			1.5			1.5		pF
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L = 8\ k\Omega$	0.999	0.9999		0.999	0.9999		0.999	0.9999		V/V
Output Resistance	$T_A = 25°C$		0.75	2.5		0.75	2.5		0.75	2.5	Ω
Supply Current	$T_A = 25°C$		3.9	5.5		3.9	5.5		3.9	5.5	mA
Input Offset Voltage				6.0			6.0			10	mV
Offset Voltage Temperature Drift	$-55°C \le T_A \le +85°C$ $+85 \le T_A \le 125°C$ $0°C \le T_A \le +70°C$		6 12 			6 			 10		µV/°C µV/°C µV/°C
Input Bias Current				10			10			10	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L = 10\ k\Omega$	0.999			0.999			0.999			V/V
Output Voltage Swing (Note 5)	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±10			±10			±10			V
Supply Current	$T_A = 125°C$		2.0	4.0		2.0	4.0				mA
Supply Voltage Rejection Ratio	$\pm 5V \le V_S \le \pm 18V$	70	80		70	80		70	80		dB

Note 1: The maximum junction temperature of the LM110 is 150°C, of the LM210 is 100°C, and of the LM310 is 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 22°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit for the LM110 and LM210 is allowed for case temperatures to 125°C and ambient temperatures to 70°C, and for the LM310, 70°C case temperature or 55°C ambient temperature. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted. R_S = 5k min, 10k typical is recommended for dynamic stability in all applications.

Note 4: These specifications apply for $\pm 5V \le V_S \le \pm 18V$ and $-55°C \le T_A$ 125°C for the LM110, $-25°C \le T_A \le 85°C$ for the LM210, and $0°C \le T_A \le 70°C$ for the LM310 unless otherwise specified.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

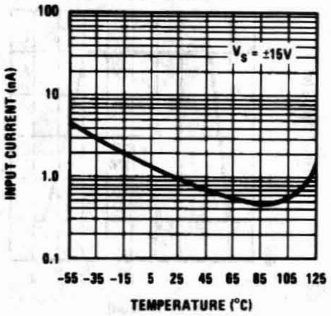
Note 6: Refer to RETS110X for LM110H, LM110J military specifications.

Application Hint

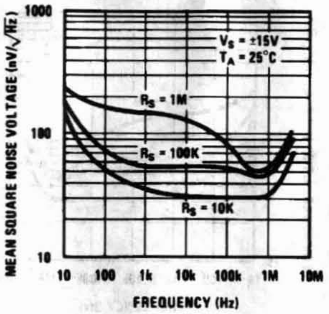
The input must be driven from a source impedance of typically 10 kΩ (5 kΩ min.) to maintain stability. The total source impedance will be reduced at high frequencies if there is stray capacitance at the input pin. In these cases, a 10 kΩ resistor should be inserted in series with the input, physically close to the input pin to minimize the stray capacitance and prevent oscillation.

Typical Performance Characteristics (LM110/LM210)

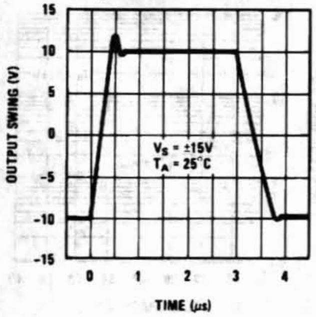
Input Current



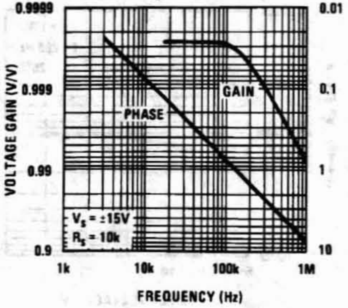
Output Noise Voltage



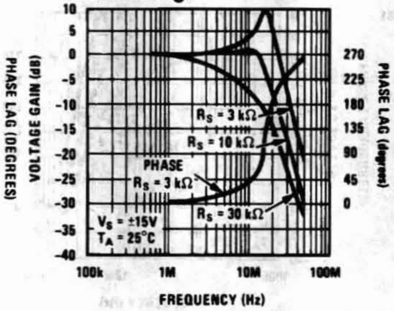
Large Signal Pulse Response



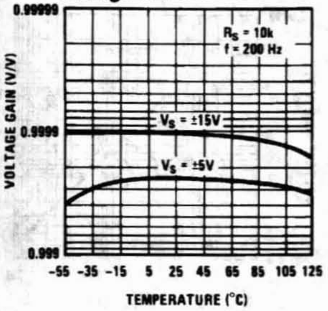
Voltage Gain and Phase Lag



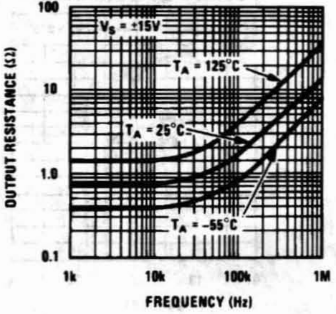
Voltage Gain and Phase Lag



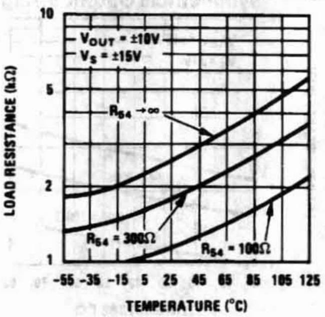
Voltage Gain



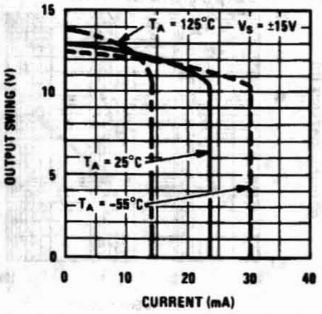
Output Resistance



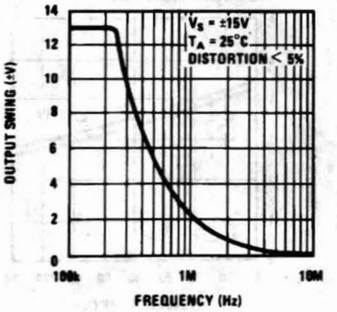
Symmetrical Output Swing



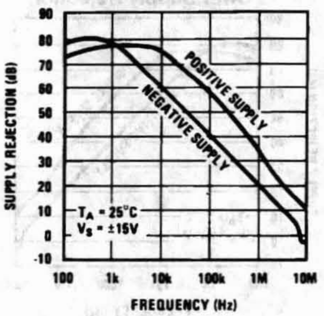
Positive Output Swing



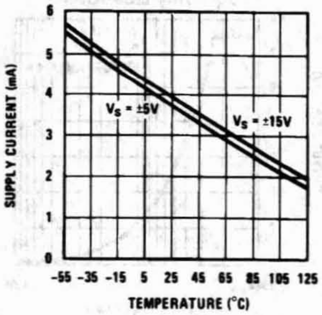
Large Signal Frequency Response



Power Supply Rejection



Supply Current



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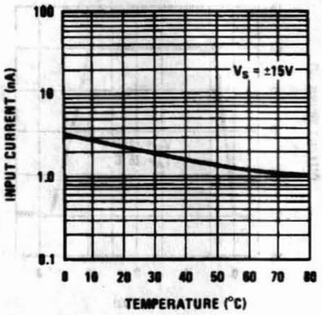
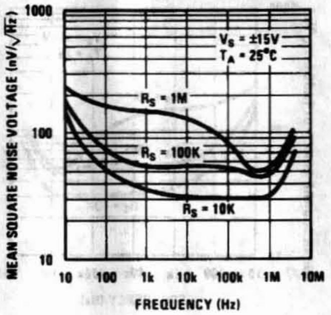
Typical Performance Characteristics (LM310)

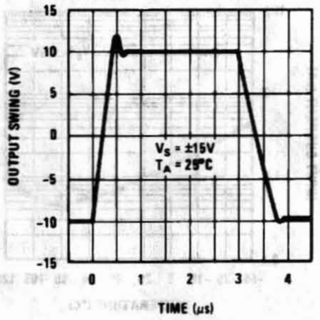
Input Current



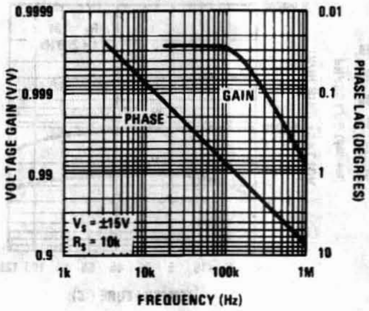
Output Noise Voltage



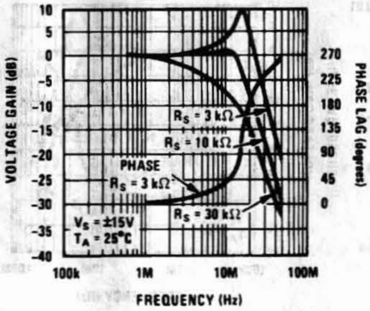
Large Signal Pulse Response



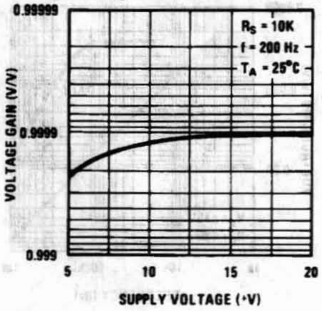
Voltage Gain and Phase Lag



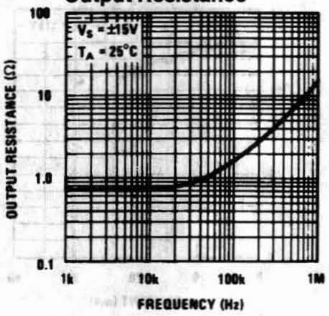
Voltage Gain and Phase Lag



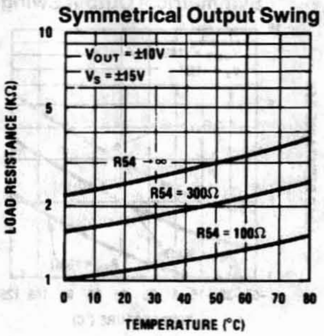
Voltage Gain



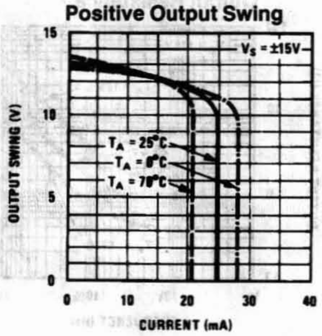
Output Resistance



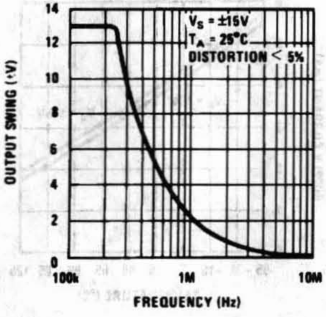
Symmetrical Output Swing



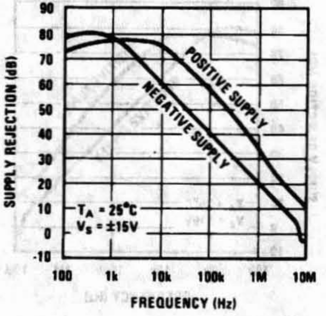
Positive Output Swing



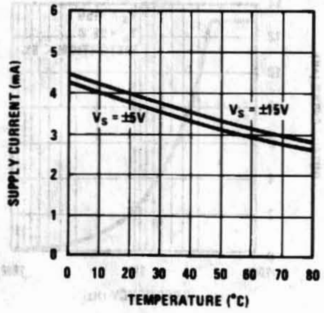
Large Signal Frequency Response



Power Supply Rejection



Supply Current



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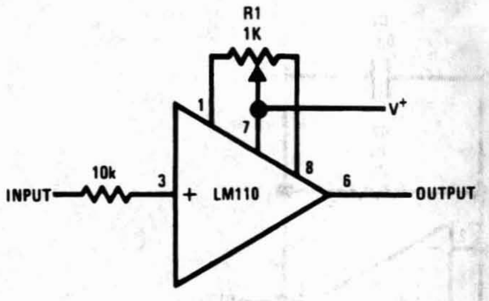
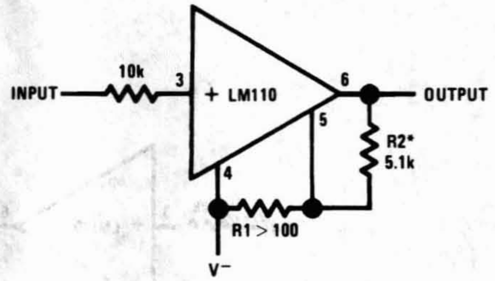
Auxiliary Circuits

Offset Balancing Circuit


R1
1K
1
7
V+
8
6
10k
3
INPUT
+ LM110
OUTPUT

TL/H/7761-2

Increasing Negative Swing Under Load

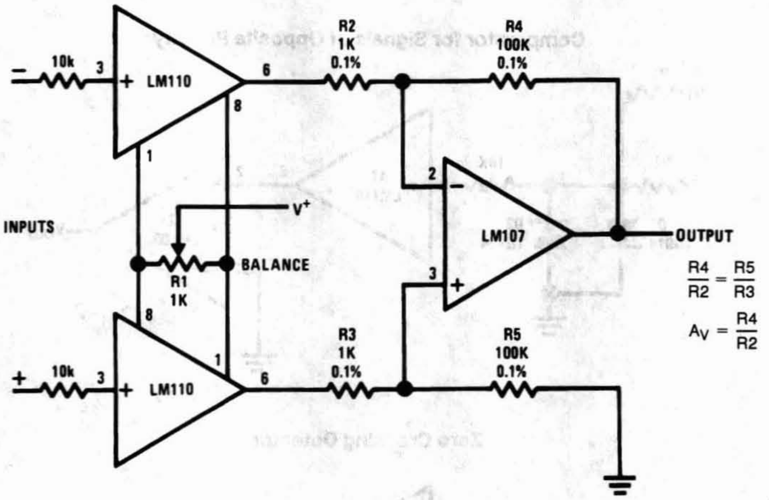

10k
3
INPUT
+ LM110
6
OUTPUT
5
R2*
5.1k
4
R1 > 100
V−

TL/H/7761-3

*May be added to reduce internal dissipation

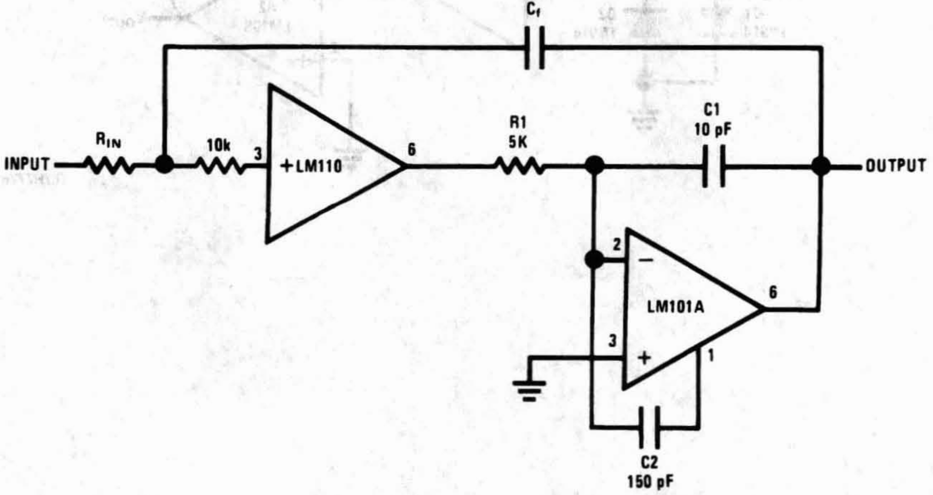
Typical Applications

Differential Input Instrumentation Amplifier


−
10k
3
+ LM110
6
8
1
R2
1K
0.1%
R4
100K
0.1%
2
−
LM107
+
3
OUTPUT
INPUTS
V+
BALANCE
R1
1K
8
+
10k
3
+ LM110
1
6
R3
1K
0.1%
R5
100K
0.1%
R4/R2 = R5/R3
AV = R4/R2

TL/H/7761-4

Fast Integrator with Low Input Current


Cf
INPUT
RIN
10k
3
+LM110
6
R1
5K
C1
10 pF
OUTPUT
2
−
LM101A
6
3
+
1
C2
150 pF

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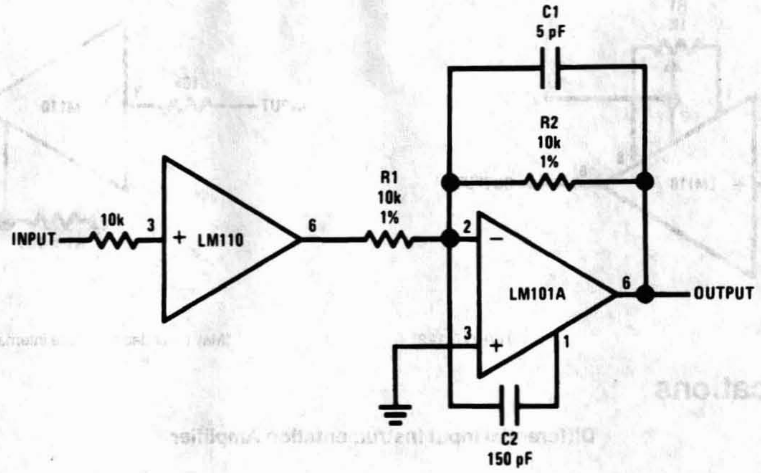
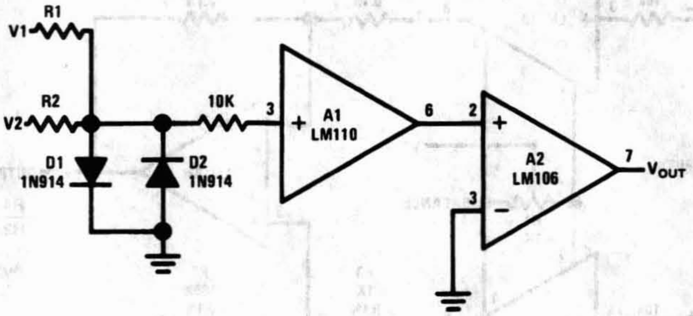
Typical Applications (Continued)

Fast Inverting Amplifier with High Input Impedance


C1
5 pF
R2
10k
1%
R1
10k
1%
INPUT
10k
3
+
LM110
6
2
−
LM101A
6
OUTPUT
3
+
1
C2
150 pF

TL/H/7761-6

Comparator for Signals of Opposite Polarity


V1
R1
V2
R2
10K
3
+
A1
LM110
6
2
+
A2
LM106
7
VOUT
3
−
D1
1N914
D2
1N914

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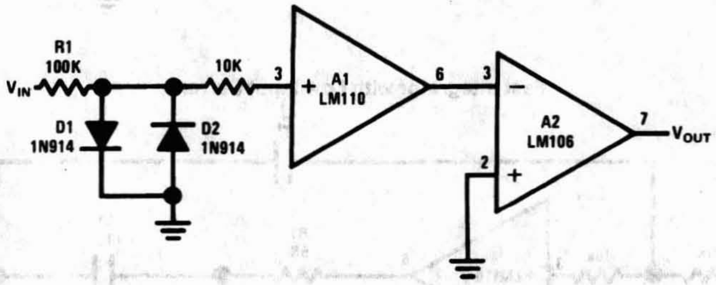
Zero Crossing Detector


R1
100K
VIN
10K
3
+
A1
LM110
6
3
−
A2
LM106
7
VOUT
2
+
D1
1N914
D2
1N914

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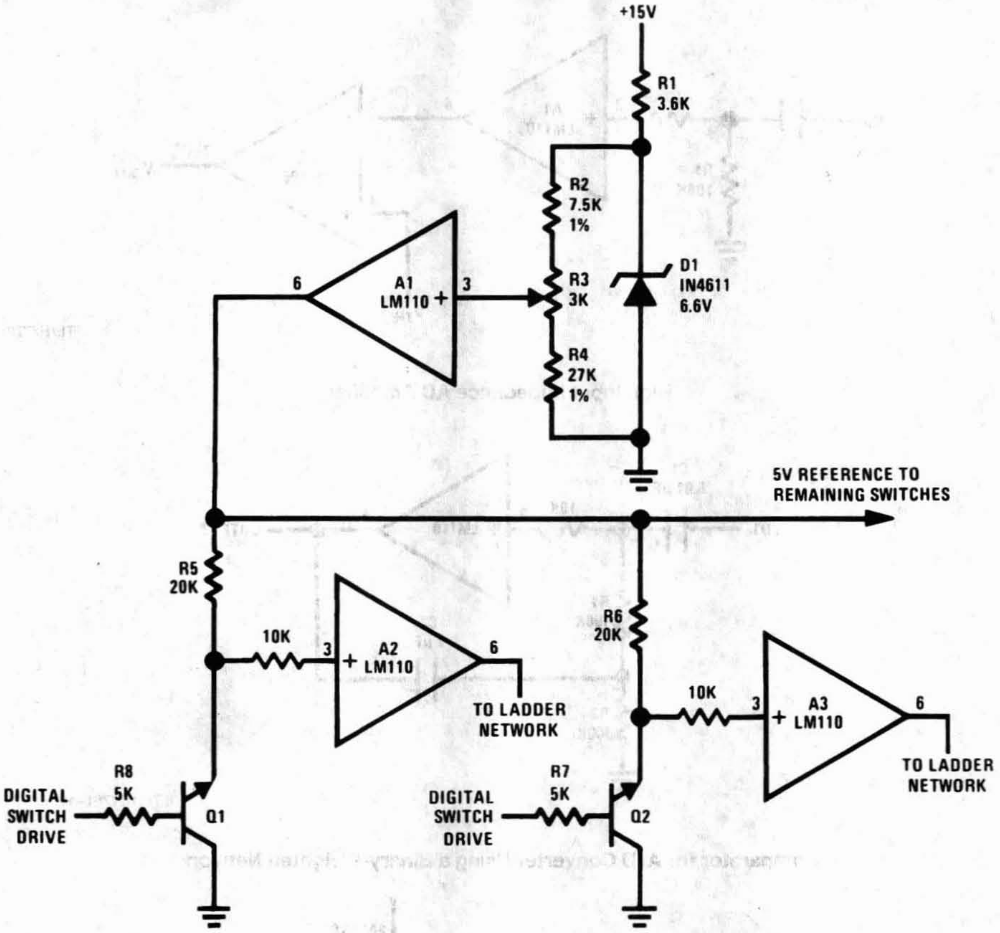
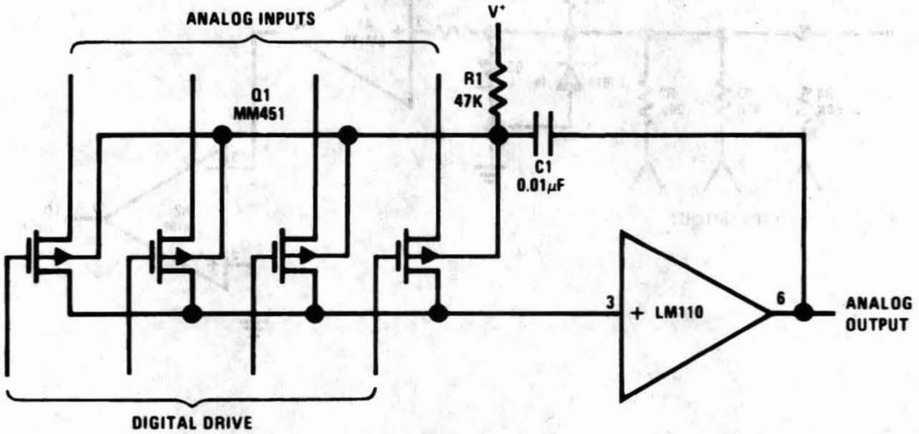
Typical Applications (Continued)

Driver for A/D Ladder Network


+15V
R1
3.6K
R2
7.5K
1%
A1
LM110
6
3
R3
3K
D1
IN4611
6.6V
R4
27K
1%
5V REFERENCE TO
REMAINING SWITCHES
R5
20K
10K
3
A2
LM110
6
TO LADDER
NETWORK
R6
20K
10K
3
A3
LM110
6
TO LADDER
NETWORK
R8
5K
DIGITAL
SWITCH
DRIVE
Q1
R7
5K
DIGITAL
SWITCH
DRIVE
Q2

TL/H/7761-8

Buffer for Analog Switch*

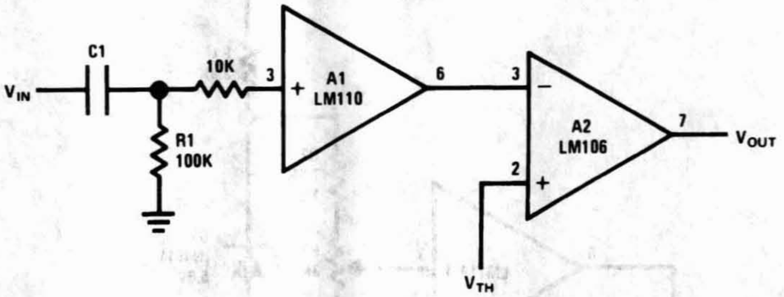

ANALOG INPUTS
V+
Q1
MM451
R1
47K
C1
0.01μF
3
LM110
6
ANALOG
OUTPUT
DIGITAL DRIVE

TL/H/7761-10

*Switch substrates are boot-strapped to reduce output capacitance of switch.

Typical Applications (Continued)

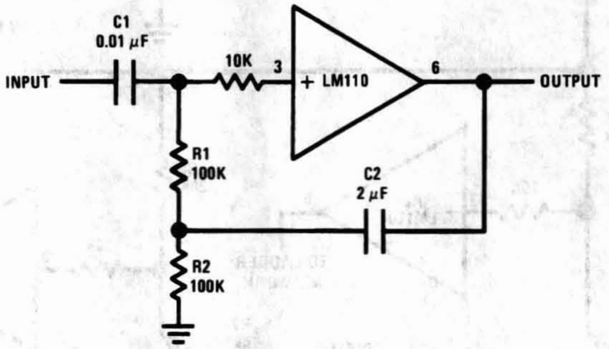
Comparator for AC Coupled Signals



VIN
C1
10K
R1
100K
3
+
A1
LM110
6
3
−
A2
LM106
2
+
7
VOUT
VTH

TL/H/7761–11

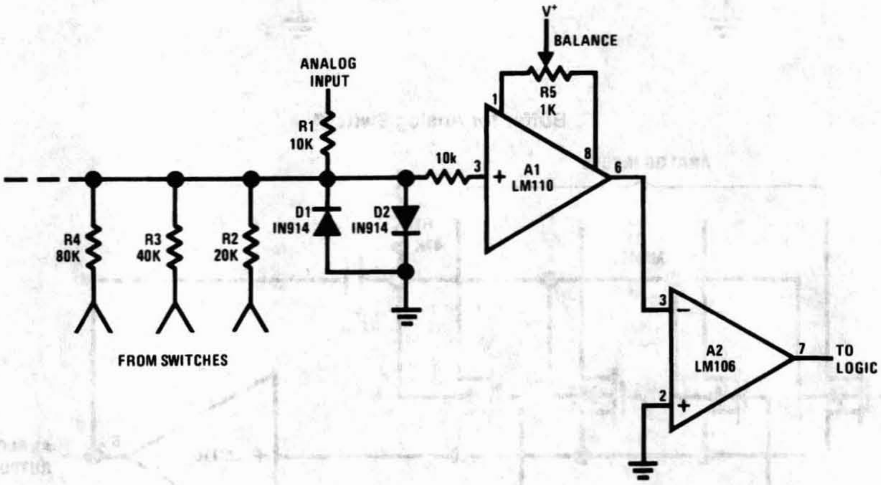
High Input Impedance AC Amplifier



C1
0.01 μF
INPUT
10K
3
+ LM110
6
OUTPUT
R1
100K
C2
2 μF
R2
100K

TL/H/7761–12

Comparator for A/D Converter Using a Binary-Weighted Network

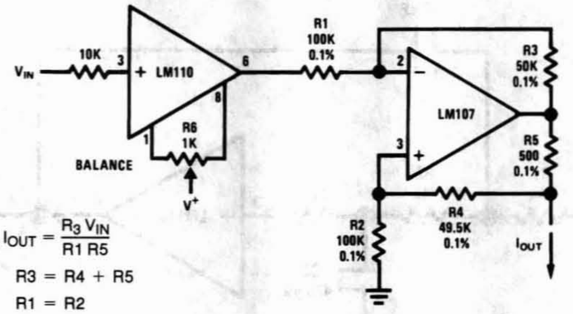


V+
BALANCE
ANALOG
INPUT
R5
1K
R1
10K
1
8
10k
3
+
A1
LM110
6
D1
IN914
D2
IN914
R4
80K
R3
40K
R2
20K
FROM SWITCHES
3
−
A2
LM106
2
+
7
TO
LOGIC

TL/H/7761–13

Typical Applications (Continued)

Bilateral Current Source


V_IN
10K
3
+ LM110
6
8
1
R6
1K
BALANCE
V+
R1
100K
0.1%
2
−
LM107
3
+
R3
50K
0.1%
R5
500
0.1%
R4
49.5K
0.1%
R2
100K
0.1%
I_OUT

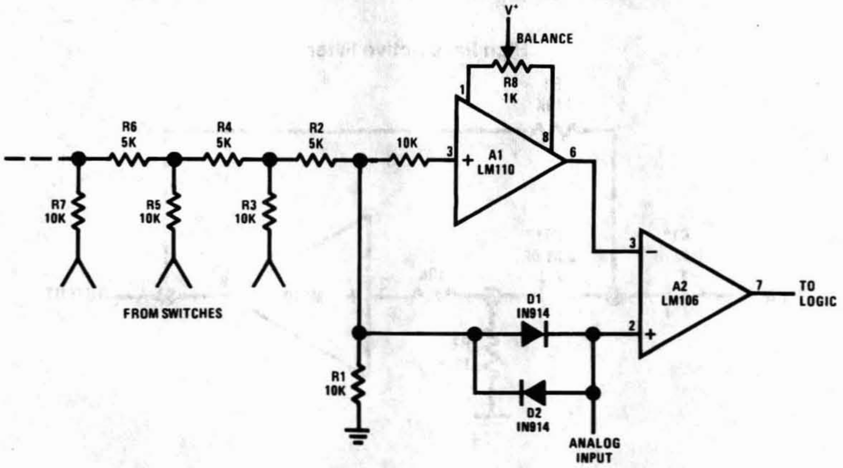
$$I_{OUT} = \frac{R_3 V_{IN}}{R1\ R5}$$

R3 = R4 + R5

R1 = R2

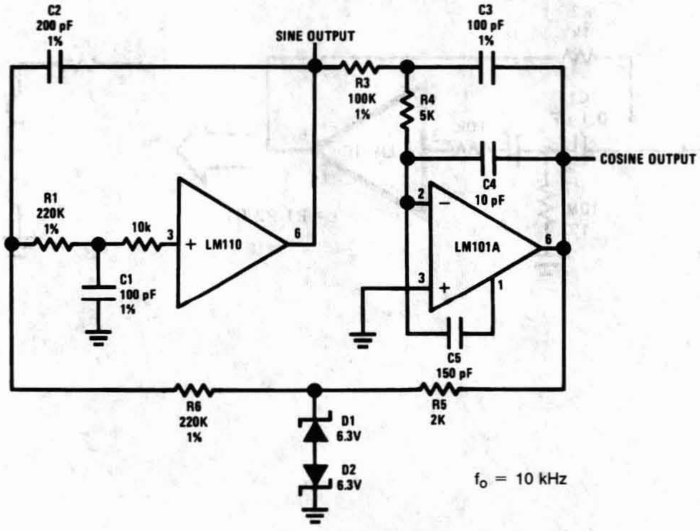
TL/H/7761-14

Comparator for A/D Converter Using a Ladder Network


V+
BALANCE
R8
1K
1
8
R6
5K
R4
5K
R2
5K
10K
3
+ A1
LM110
6
R7
10K
R5
10K
R3
10K
FROM SWITCHES
3
−
A2
LM106
7
TO LOGIC
2
+
D1
IN914
D2
IN914
R1
10K
ANALOG INPUT

TL/H/7761-15

Sine Wave Oscillator

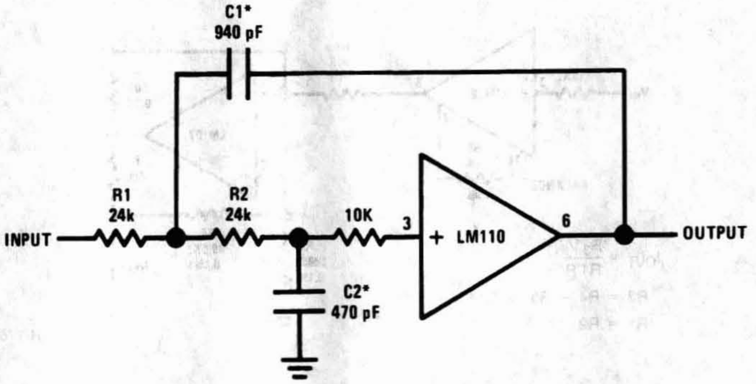

C2
200 pF
1%
SINE OUTPUT
C3
100 pF
1%
R3
100K
1%
R4
5K
C4
10 pF
COSINE OUTPUT
R1
220K
1%
10k
3
+ LM110
6
C1
100 pF
1%
2
−
LM101A
6
3
+
1
C5
150 pF
R6
220K
1%
R5
2K
D1
6.3V
D2
6.3V

$f_o = 10\ kHz$

TL/H/7761-16

Typical Applications (Continued)

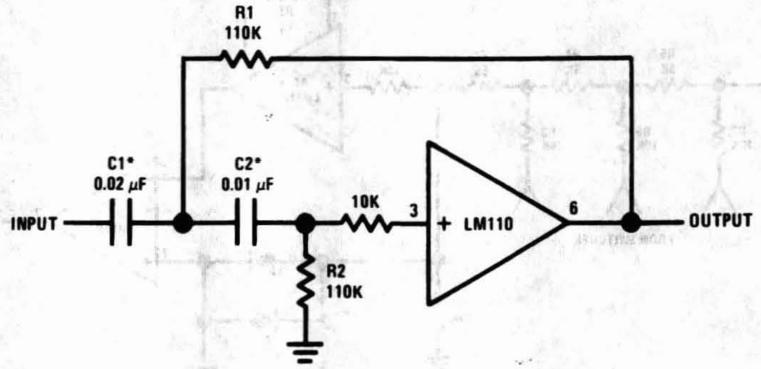
Low Pass Active Filter


C1*
940 pF
R1
24k
R2
24k
10K
3
+ LM110
6
INPUT
OUTPUT
C2*
470 pF

TL/H/7761–18

*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

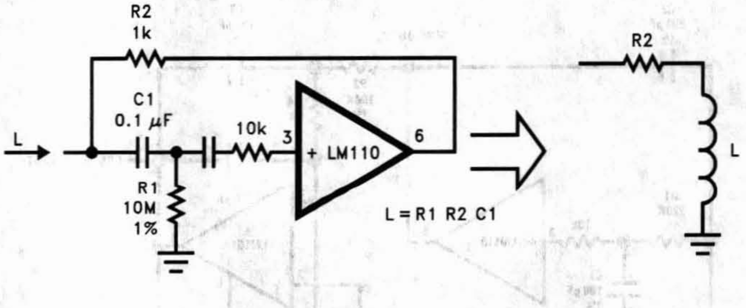
High Pass Active Filter


R1
110K
C1*
0.02 μF
C2*
0.01 μF
10K
3
+ LM110
6
INPUT
OUTPUT
R2
110K

TL/H/7761–19

*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

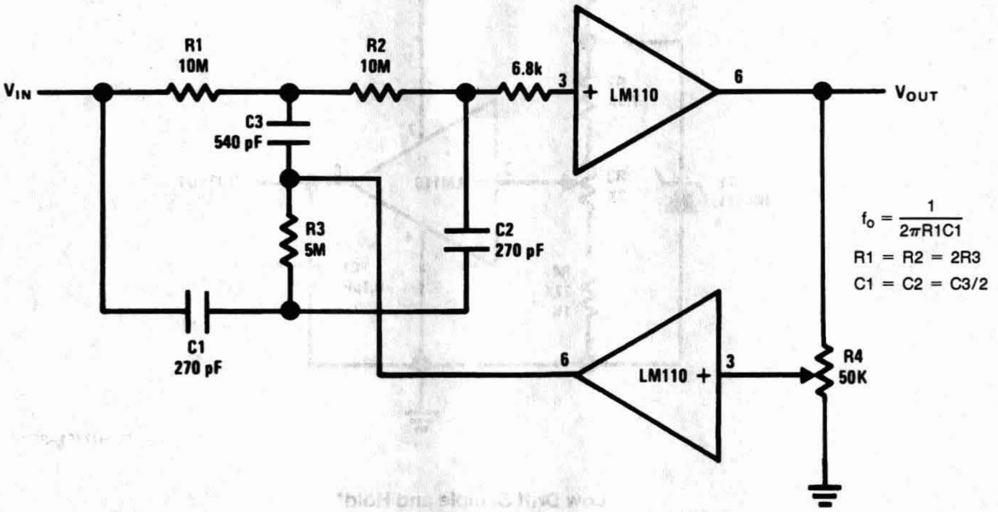
Simulated Inductor


R2
1k
C1
0.1 μF
10k
3
+ LM110
6
L
R1
10M
1%
L = R1 R2 C1
R2
L

TL/H/7761–21

Typical Applications (Continued)

Adjustable Q Notch Filter


V_IN
R1
10M
R2
10M
6.8k
3
+ LM110
6
V_OUT
C3
540 pF
R3
5M
C2
270 pF
C1
270 pF
6
LM110 +
3
R4
50K

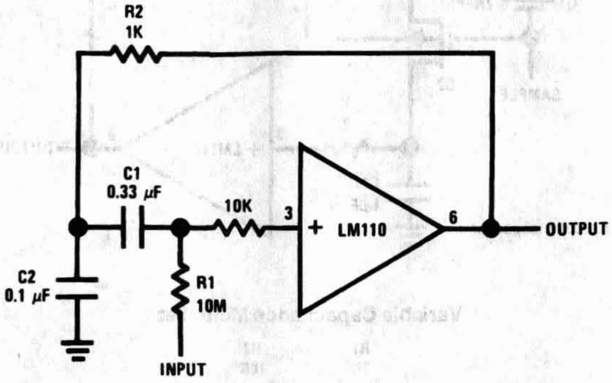
$f_o = \frac{1}{2\pi R1C1}$

R1 = R2 = 2R3

C1 = C2 = C3/2

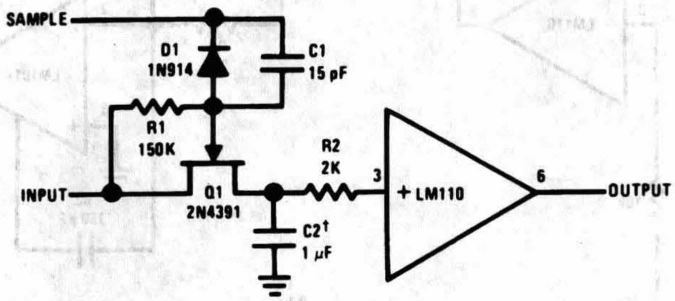
TL/H/7761–22

Bandpass Filter


R2
1K
C1
0.33 μF
10K
3
+ LM110
6
OUTPUT
C2
0.1 μF
R1
10M
INPUT

TL/H/7761–23

Sample and Hold

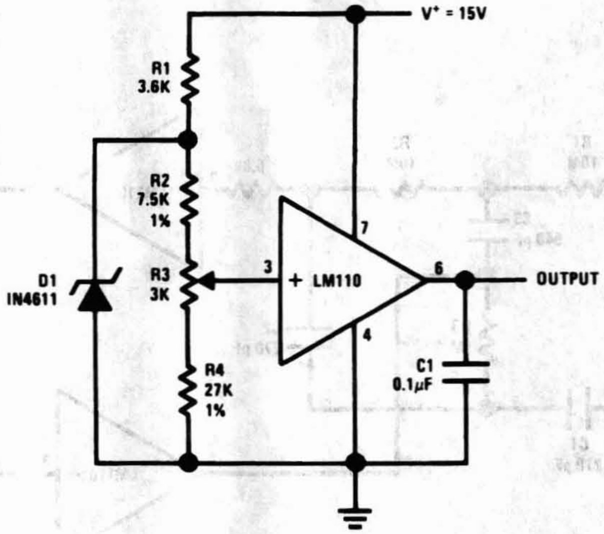

SAMPLE
D1
1N914
C1
15 pF
R1
150K
R2
2K
INPUT
Q1
2N4391
3
+ LM110
6
OUTPUT
C2†
1 μF

TL/H/7761–24

†Use capacitor with polycarbonate teflon or polythylene dietetric

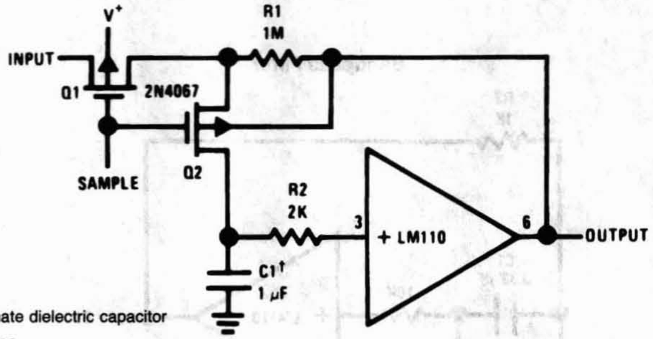
Typical Applications (Continued)

Buffered Reference Source


V⁺ = 15V
R1
3.6K
R2
7.5K
1%
D1
IN4611
R3
3K
3
+ LM110
7
6
4
OUTPUT
R4
27K
1%
C1
0.1μF

TL/H/7761-25

Low Drift Sample and Hold*


V⁺
INPUT
Q1
2N4067
SAMPLE
Q2
R1
1M
R2
2K
3
+ LM110
6
OUTPUT
C1†
1 μF

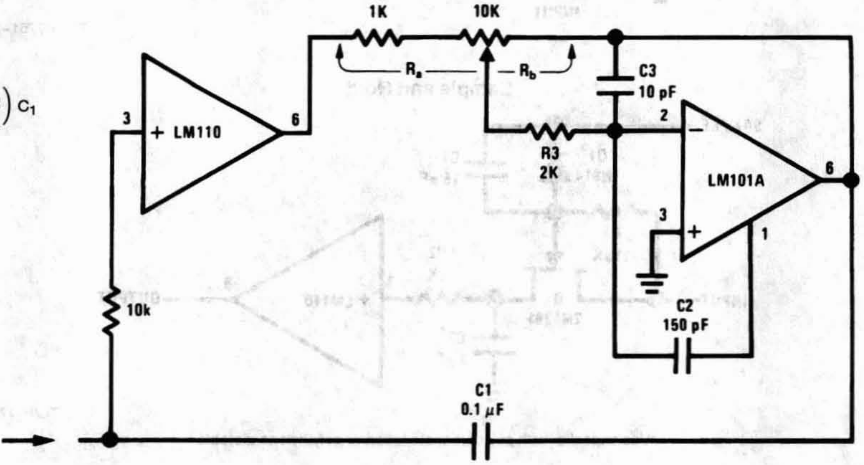
†Teflon polyethylene or polycarbonate dielectric capacitor

*Worst case drift less than 3 mV/sec

TL/H/7761-26

Variable Capacitance Multiplier

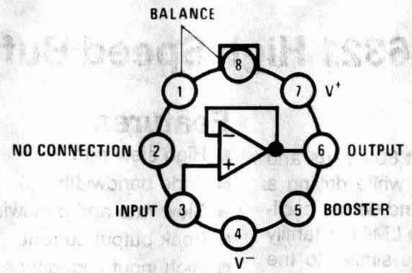
$$C = \left(1 + \frac{R_b}{R_a}\right) C_1$$


R1
1K
R2
10K
R_a
R_b
3
+ LM110
6
C3
10 pF
2
R3
2K
LM101A
6
3
1
C2
150 pF
10k
C1
0.1 μF

TL/H/7761-27

Connection Diagrams

Metal Can Package


BALANCE
8
1
7
V+
NO CONNECTION
2
6
OUTPUT
INPUT
3
5
BOOSTER
4
V−

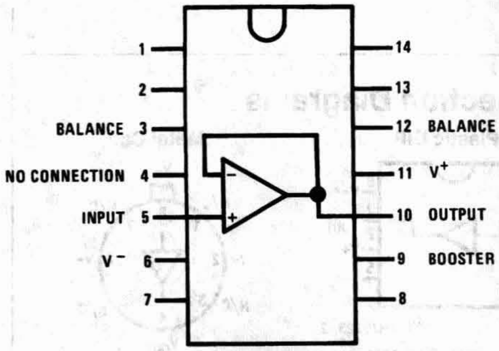
TL/H/7761-30

Package is connected to Pin 4 (V−)

Top View

Order Number LM110H, LM210H or LM310H
LM110H/883*
See NS Package Number H08C

Dual-In-Line Package

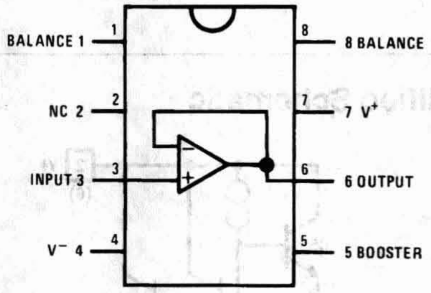

1
2
BALANCE 3
NO CONNECTION 4
INPUT 5
V− 6
7
14
13
12 BALANCE
11 V+
10 OUTPUT
9 BOOSTER
8

TL/H/7761-31

Top View

Order Number LM110J, LM210J,
LM310J or LM110J/883*
See NS Package Number J14A

Dual-In-Line Package


BALANCE 1
1
NC 2
2
INPUT 3
3
V− 4
4
8
8 BALANCE
7
7 V+
6
6 OUTPUT
5
5 BOOSTER

TL/H/7761-32

Top View

Order Number LM310M, LM310N or LM110J-8/883*
See NS Package Number J08A, M08A or N08E

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*Available per SMD# 5962-8760601

National Semiconductor

LM6121/LM6221/LM6321 High Speed Buffer

General Description

These high speed unity gain buffers slew at 800 V/μs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. They can drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6121 family are monolithic ICs which offer performance similar to the LH0002 with the additional features of current limit and thermal shutdown.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

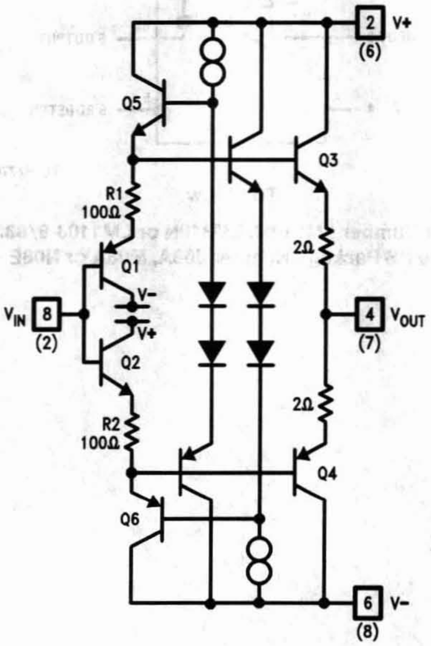
Features

■ High slew rate	800 V/μs
■ Wide bandwidth	50 MHz
■ Slew rate and bandwidth 100% tested	
■ Peak output current	±300 mA
■ High input impedance	5 MΩ
■ LH0002H pin compatible	
■ No oscillations with capacitive loads	
■ 5V to ±15V operation guaranteed	
■ Current and thermal limiting	
■ Fully specified to drive 50Ω lines	

Applications

- Line Driving
- Radar
- Sonar

Simplified Schematic

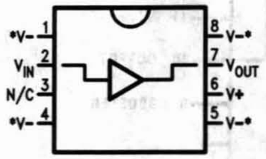


TL/H/9223-1

Numbers in ( ) are for 8-pin N DIP.

Connection Diagrams

Plastic DIP

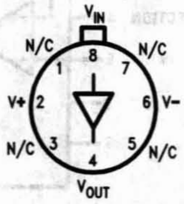


TL/H/9223-2

*Heat-sinking pins. See Application section on heat sinking requirements.

Order Number LM6221N, LM6321N or LM6121J/883
See NS Package Number J08A or N08E

Metal Can



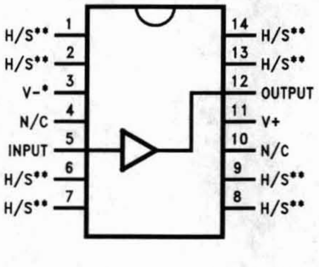
TL/H/9223-3

Top View

Note: Pin 6 connected to case.

Order Number LM6221H or LM6121H/883
See NS Package Number H08C

Plastic SO



TL/H/9223-7

*Pin 3 must be connected to the negative supply.

**Heat-sinking pins. See Application section on heat-sinking requirements. These pins are at V⁻ potential.

Order Number LM6321M
See NS Package Number M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V (±18)
Input to Output Voltage (Note 2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Power Dissipation	(Note 10)
ESD Tolerance (Note 8)	±2000V
Junction Temperature ($T_{J(max)}$)	150°C

Operating Ratings

Operating Temperature Range	
LM6121H/883	−55°C to +125°C
LM6221	−40°C to +85°C
LM6321	0°C to +70°C
Operating Supply Range	4.75 to ±16V
Thermal Resistance (θ_{JA}), (Note 4)	
H Package	150°C/W
N Package	47°C/W
M Package	69°C/W
Thermal Resistance (θ_{JC}), H Package	17°C/W

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq$ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typ	LM6121 Limit (Notes 5, 9)	LM6221 Limit (Note 5)	LM6321 Limit (Note 5)	Units
A_{V1}	Voltage Gain 1	R_L = 1 kΩ, V_{IN} = ±10V	0.990	0.980 **0.970**	0.980 **0.950**	0.970 **0.950**	V/V Min
A_{V2}	Voltage Gain 2	R_L = 50Ω, V_{IN} = ±10V	0.900	0.860 **0.800**	0.860 **0.820**	0.850 **0.820**	
A_{V3}	Voltage Gain 3 (Note 6)	R_L = 50Ω, V^+ = 5V V_{IN} = 2 V_{pp} **(1.5 V_{pp})**	0.840	0.780 **0.750**	0.780 **0.700**	0.750 **0.700**	
V_{OS}	Offset Voltage	R_L = 1 kΩ	15	30 **50**	30 **60**	50 **100**	mV Max
I_B	Input Bias Current	R_L = 1 kΩ, R_S = 10 kΩ	1	4 **7**	4 **7**	5 **7**	μA Max
R_{IN}	Input Resistance	R_L = 50Ω	5				MΩ
C_{IN}	Input Capacitance		3.5				pF
R_O	Output Resistance	I_{OUT} = ±10 mA	3	5 **10**	5 **10**	5 **6**	Ω Max
I_{S1}	Supply Current 1	R_L = ∞	15	18 **20**	18 **20**	20 **22**	mA Max
I_{S2}	Supply Current 2	R_L = ∞, V^+ = 5V	14	16 **18**	16 **18**	18 **20**	
V_{O1}	Output Swing 1	R_L = 1k	13.5	13.3 **13**	13.3 **13**	13.2 **13**	±V Min
V_{O2}	Output Swing 2	R_L = 100Ω	12.7	11.5 **10**	11.5 **10**	11 **10**	
V_{O3}	Output Swing 3	R_L = 50Ω	12	11 **9**	11 **9**	10 **9**	
V_{O4}	Output Swing 4	R_L = 50Ω, V^+ = 5V (Note 6)	1.8	1.6 **1.3**	1.6 **1.4**	1.6 **1.5**	V_{PP} Min
PSSR	Power Supply Rejection Ratio	$V^{\pm}$ = ±5V to ±15V	70	60 **55**	60 **50**	60 **50**	dB Min

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $V_{CM} = 0$, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6121 Limit (Note 5)	LM6221 Limit (Note 5)	LM6321 Limit (Note 5)	Units
SR_1	Slew Rate 1	$V_{IN} = \pm 11V$, $R_L = 1\ k\Omega$	1200	550	550	550	V/µs Min
SR_2	Slew Rate 2	$V_{IN} = \pm 11V$, $R_L = 50\Omega$ (Note 7)	800	550	550	550	
SR_3	Slew Rate 3	$V_{IN} = 2\ V_{PP}$, $R_L = 50\Omega$ $V^+ = 5V$ (Note 6)	50	550	550	550	
BW	−3 dB Bandwidth	$V_{IN} = \pm 100\ mV_{PP}$, $R_L = 50\Omega$ $C_L \leq 10\ pF$	50	30	30	30	MHz Min
t_r, t_f	Rise Time Fall Time	$R_L = 50\Omega$, $C_L \leq 10\ pF$ $V_O = 100\ mV_{PP}$	7.0				ns
t_{pd}	Propagation Delay Time	$R_L = 50\Omega$, $C_L \leq 10\ pF$ $V_O = 100\ mV_{PP}$	4.0				ns
O_S	Overshoot	$R_L = 50\Omega$, $C_L \leq 10\ pF$ $V_O = 100\ mV_{PP}$	10				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit or thermal limit, the input current will increase if the input to output differential voltage exceeds 8V. For input to output differential voltages in excess of 8V the input current should be limited to ±20 mA.

Note 3: The LM6121 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: The thermal resistance θ_{JA} of the device in the N package is measured when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 4, 5 and 8) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal resistance θ_{JA} of the N package is 84°C/W. The thermal resistance θ_{JA} of the device in the M package is measured when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 2, 6, 7, 8, 9, 13, 14) are connected to 1 square inch of 2 oz. copper.

Note 5: Limits are guaranteed by testing or correlation.

Note 6: The input is biased to 2.5V and V_{IN} swings V_{pp} about this value. The input swing is 2 V_{pp} at all temperatures except for the A_V3 test at −55°C where it is reduced to 1.5 V_{pp}.

Note 7: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/µs.

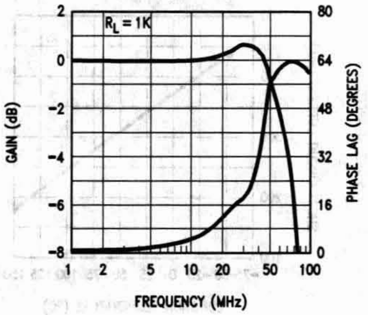
Note 8: The test circuit consists of the human body model of 120 pF in series with 1500Ω.

Note 9: For specification limits over the full Military Temperature Range, see RETS6121X.

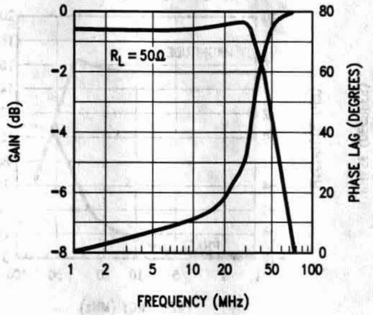
Note 10: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Typical Performance Characteristics $T_J = 25°C$, unless otherwise specified

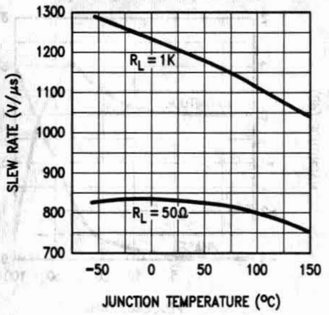
Frequency Response



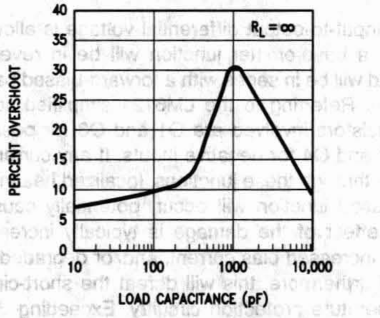
Frequency Response



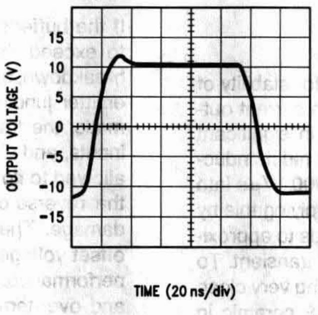
Slew Rate vs Temperature



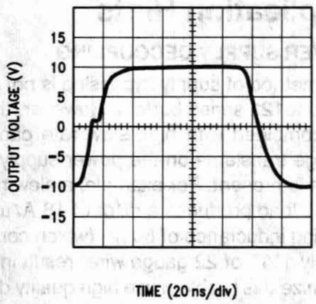
Overshoot vs Capacitive Load



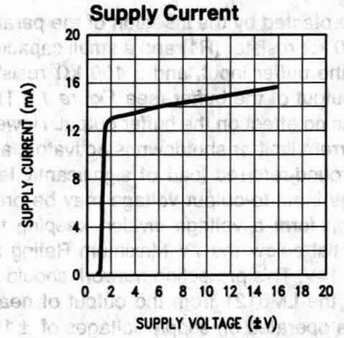
Large Signal Response R_L = 1 kΩ



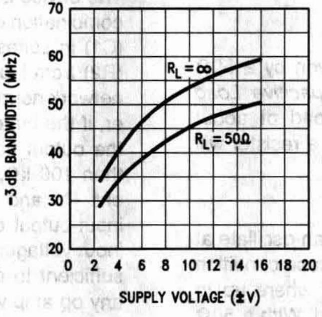
Large Signal Response R_L = 50Ω



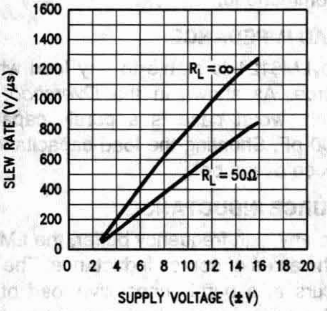
Supply Current



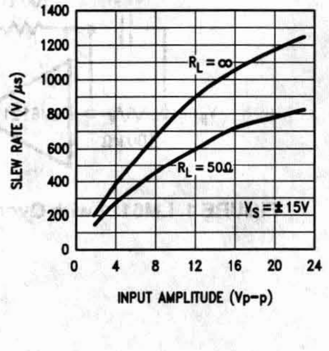
−3 dB Bandwidth



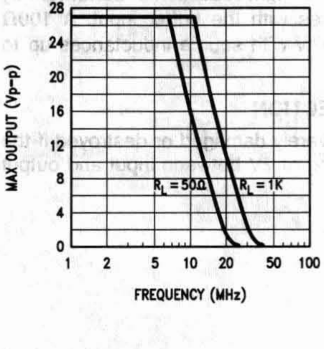
Slew Rate



Slew Rate

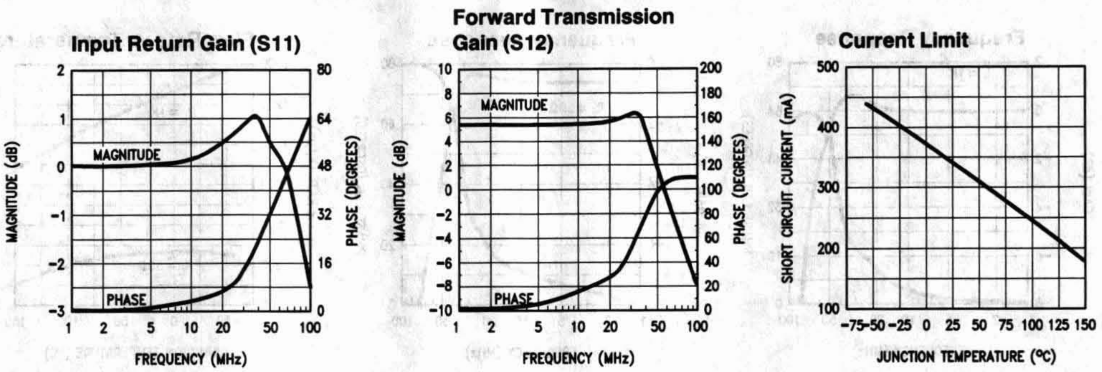


Power Bandwidth



TL/H/9223-4

Typical Performance Characteristics $T_J = 25°C$, unless otherwise specified (Continued)



TL/H/9223-5

Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6121 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/μs into a 50Ω load produces a di/dt of 18 A/μs. Multiplying this by a wiring inductance of 50 nH (which corresponds to approximately 1½″ of 22 gauge wire) result in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 μF ceramic in parallel with one or two 2.2 μF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6121 is stable to any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

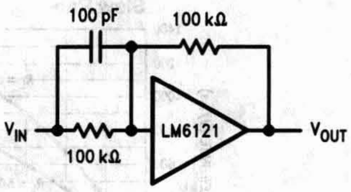
Like any high frequency buffer, the LM6121 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

OVERVOLTAGE PROTECTION

The LM6121 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6121 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. Furthermore, this will defeat the short-circuit and over-temperature protection circuitry. Exceeding ±7V input with a shorted output will destroy the device.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see *Figure 1*). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6121 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.



TL/H/9223-6

FIGURE 1. LM6121 with Overvoltage Protection

Application Hints

HEATSINK REQUIREMENTS

A heatsink may be required with the LM6321 depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the maximum power dissipated by the buffer, P(max), must be calculated. The formula for calculating the maximum allowable power dissipation in any application is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. For the simple case of a buffer driving a resistive load as in *Figure 2*, the maximum DC power dissipation occurs when the output is at half the supply. Assuming equal supplies, the formula is $P_D = I_S\,(2V^+) + V^{+2}/2\,R_L$.

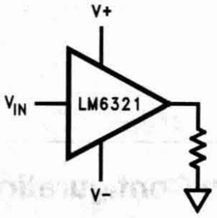


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FIGURE 2

The next parameter which must be calculated is the maximum allowable temperature rise, $T_R(\text{max})$. This is calculated by using the formula:

$$T_R(\text{max}) = T_J(\text{max}) - T_A(\text{max})$$

where: $T_J(\text{max})$ is the maximum allowable junction temperature

$T_A(\text{max})$ is the maximum ambient temperature

Using the calculated values for $T_R(\text{max})$ and P(max), the required value for junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

$$\theta_{(J-A)} = T_R(\text{max})/P(\text{max})$$

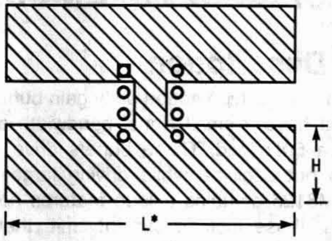
The heatsink for the LM6321 is made using the PC board copper. The heat is conducted from the die, through the lead frame (inside the part), and out the pins which are soldered to the PC board. The pins used for heat conduction are:

TABLE I

Part	Package	Pins
LM6321N	8-Pin DIP	1, 4, 5, 8
LM6321M	14-Pin SO	1, 2, 3, 6, 7, 8, 9, 13, 14

Figure 3 shows copper patterns which may be used to dissipate heat from the LM6321.

8-Pin DIP



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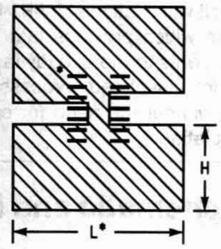
14-Pin SO



TL/H/9223-10

*For best results, use L = 2H

FIGURE 3. Copper Heatsink Patterns

Table II shows some values of junction-to-ambient thermal resistance (θ_{J-A}) for values of L and W for 2 oz. copper:

TABLE II

Package	L (in.)	H (in.)	θ_{J-A} (°C/W)
8-Pin DIP	2	0.5	47
14-Pin SO	1	0.5	69
	2	1	57

National Semiconductor

LM6125/LM6225/LM6325 High Speed Buffer

General Description

The LM6125 family of high speed unity gain buffers slew at 800 V/µs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. These buffers drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6125 contains unique features not found in power buffers; these include current limit, thermal shutdown, electronic shutdown, and an error flag that warns of fault conditions.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

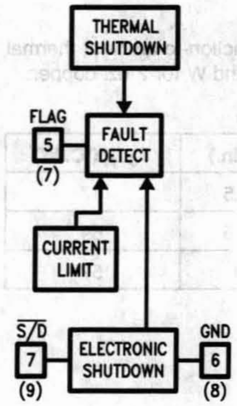
Features

- High slew rate 800 V/µs
- High output current ±300 mA
- Stable with large capacitive loads
- Current and thermal limiting
- Electronic shutdown
- 5V to ±15V operation guaranteed
- Fully specified to drive 50Ω lines

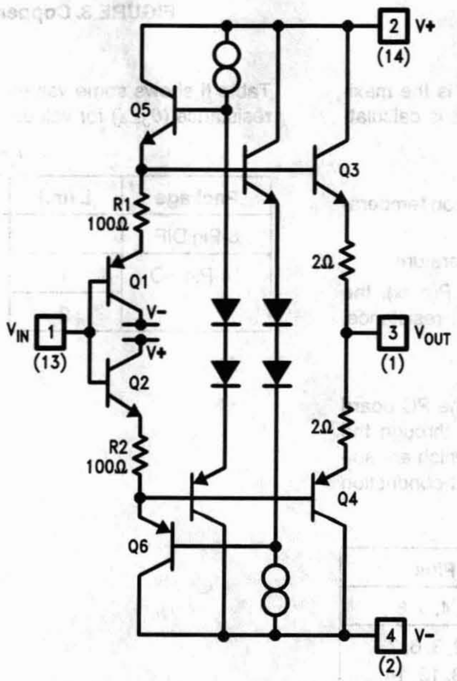
Applications

- Line Driving
- Radar
- Sonar

Simplified Schematic and Block Diagram


THERMAL SHUTDOWN
FLAG
5
(7)
FAULT DETECT
CURRENT LIMIT
S/D
7
(9)
ELECTRONIC SHUTDOWN
GND
6
(8)

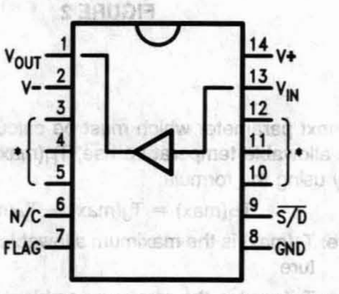
TL/H/9222–1


2 V+
(14)
Q5
Q3
R1 100Ω
2Ω
Q1
V−
V_{IN} 1
(13)
V+
Q2
3 V_{OUT}
(1)
2Ω
R2 100Ω
Q4
Q6
4 V−
(2)

TL/H/9222–2

Numbers in ( ) are for 14-pin N DIP.

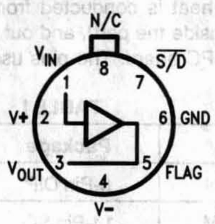
Pin Configurations


V_{OUT} 1
V− 2
3
4
5
N/C 6
FLAG 7
14 V+
13 V_{IN}
12
11
10
9 S/D
8 GND

TL/H/9222–3

*Heat sinking pins.
Internally connected to V−.

Order Number LM6225N
or LM6325N
See NS Package Number N14A


N/C
V_{IN} 8
S/D 7
1
V+ 2
6 GND
V_{OUT} 3
5 FLAG
4
V−

TL/H/9222–4

Top View

Note: Pin 4 connected to case

Order Number LM6125H/883*
or LM6125H
See NS Package Number H08C

*Available per 5962-9081501

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V (±18V)
Input to Output Voltage (Note 2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (Note 3)	Continuous
Flag Output Voltage	GND ≤ Vflag ≤ +Vsupply
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance (Note 9)	±1500V
θ_{JA} (Note 4)	
H Package	150°C/W
N Package	40°C/W
Maximum Junction Temperature (T_J)	150°C
Operating Temperature Range	
LM6125	−55°C to +125°C
LM6225	−40°C to +85°C
LM6325	0°C to +70°C
Operating Supply Voltage Range	4.75V to ±16V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $V_{CM} = 0$, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6125 Limit (Notes 5, 10)	LM6225 Limit (Note 5)	LM6325 Limit (Note 5)	Units
A_{V1}	Voltage Gain 1	$R_L = 1k\Omega$, $V_{IN} = \pm10V$	0.990	0.980 **0.970**	0.980 **0.950**	0.970 **0.950**	V/V Min
A_{V2}	Voltage Gain 2	$R_L = 50\Omega$, $V_{IN} = \pm10V$	0.900	0.860 **0.800**	0.860 **0.820**	0.850 **0.820**	
A_{V3}	Voltage Gain 3 (Note 6)	$R_L = 50\Omega$, $V^+ = 5V$ $V_{IN} = 2\ V_{PP}$ **(1.5 V_{PP})**	0.840	0.780 **0.750**	0.780 **0.700**	0.750 **0.700**	
V_{OS}	Offset Voltage	$R_L = 1\ k\Omega$	15	30 **50**	30 **60**	50 **100**	mV Max
I_B	Input Bias Current	$R_L = 1\ k\Omega$, $R_S = 10\ k\Omega$	1	4 **7**	4 **7**	5 **7**	µA Max
R_{IN}	Input Resistance	$R_L = 50\Omega$	5				MΩ
C_{IN}	Input Capacitance		3.5				pF
R_O	Output Resistance	$I_{OUT} = \pm10\ mA$	3	5 **10**	5 **10**	5 **6**	Ω Max
I_{S1}	Supply Current 1	$R_L = \infty$	15	18 **20**	18 **20**	20 **22**	mA Max
I_{S2}	Supply Current 2	$R_L = \infty$, $V^+ = 5V$	14	16 **18**	16 **18**	18 **20**	
$I_{S/D}$	Supply Current in Shutdown	$R_L = \infty$, $V^{\pm} = \pm15V$	1.1	1.5 **2.0**	1.5 **2.0**	1.5 **2.0**	
V_{O1}	Output Swing 1	$R_L = 1\ k\Omega$	13.5	13.3 **13**	13.3 **13**	13.2 **13**	±V Min
V_{O2}	Output Swing 2	$R_L = 100\Omega$	12.7	11.5 **10**	11.5 **10**	11 **10**	
V_{O3}	Output Swing 3	$R_L = 50\Omega$	12	11 **9**	11 **9**	10 **9**	
V_{O4}	Output Swing 4	$R_L = 50\Omega$	1.8	1.6 **1.3**	1.6 **1.4**	1.6 **1.5**	V_{PP} Min
PSRR	Power Supply Rejection Ratio	$V^+ = 5V$ (Note 6)	70	60 **55**	60 **50**	60 **50**	dB Min
V_{OL}	Flag Pin Output Low Voltage	$V^{\pm} = \pm5V$ to $\pm15V$ $V_{S/D} = 0V$		300 **400**	300 **400**	340 **400**	mV Max
I_{OH}	Flag Pin Output High Current	V_{OH} Flag Pin = 15V (Note 7)	0.01	10 **20**	10 **20**	10 **20**	µA Max

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq$ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typ	LM6125	LM6225	LM6325	Units
				Limit (Notes 5, 10)	Limit (Note 5)	Limit (Note 5)	
V_{TH}	Shutdown Threshold		1.4				V
V_{IH}	Shutdown Pin Trip Point High			2.0 **2.0**	2.0 **2.0**	2.0 **2.0**	V Min
V_{IL}	Shutdown Pin Trip Point Low			0.8 **0.8**	0.8 **0.8**	0.8 **0.8**	V Max
I_{IL}	Shutdown Pin Input Low Current	$V_{S/D}$ = 0V	−0.07	−10 **−20**	−10 **−20**	−10 **−20**	µA Max
I_{IH}	Shutdown Pin Input High Current	$V_{S/D}$ = 5V	−0.05	−10 **−20**	−10 **−20**	−10 **−20**	µA Max
I_O	Bi-State Output Current	Shutdown Pin = 0V V_{OUT} = +5V or −5V	1	50 **2000**	50 **100**	100 **200**	µA

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq$ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typ	LM6125	LM6225	LM6325	Units
				Limit (Note 5)	Limit (Note 5)	Limit (Note 5)	
SR_1	Slew Rate 1	V_{IN} = ±11V, R_L = 1 kΩ	1200				
SR_2	Slew Rate 2	V_{IN} = ±11V, R_L = 50Ω (Note 8)	800	550	550	550	V/µs Min
SR_3	Slew Rate 3	V_{IN} = 2 V_{PP}, R_L = 50Ω V^+ = 5V (Note 6)	50				
BW	−3 dB Bandwidth	V_{IN} = 100 mV_{PP} R_L = 50Ω, $C_L \leq$ 10 pF	50	30	30	30	MHz Min
t_r, t_f	Rise Time Fall Time	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	8.0				ns
t_{PD}	Propagation Delay Time	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	4.0				ns
O_S	Overshoot	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	10				%
V_{FT}	V_{IN}, V_{OUT} Feedthrough in Shutdown	Shutdown Pin = 0V V_{IN} = 4 V_{PP}, 1 MHz R_L = 50Ω	−50				dB
C_{OUT}	Output Capacitance in Shutdown	Shutdown Pin = 0V	30				pF
t_{SD}	Shutdown Response Time		700				ns

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit, thermal limit, or electronic shutdown the input current will increase if the input to output differential voltage exceeds 8V. See Overvoltage Protection in Application Hints.

Note 3: The LM6125 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: For operation at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} and T_J max, $T_J = T_A + \theta_{JA} P_D$. θ_{JC} for the LM6125H and LM6225H is 17°C/W. The thermal impedance θ_{JA} of the device in the N package is 40°C/W when soldered directly to a printed circuit board, and the heat-sinking pins (pins 3, 4, 5, 10, 11, and 12) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal impedance θ_{JA} of the N package is 60°C/W.

Note 5: Limits are guaranteed by testing or correlation.

Note 6: The input is biased to +2.5V, and V_{IN} swings V_{PP} about this value. The input swing is 2 V_{PP} at all temperatures except for the A_V3 test at −55°C where it is reduced to 1.5 V_{PP}.

Note 7: The Error Flag is set (low) during current limit or thermal fault detection in addition to being set by the Shutdown pin. It is an open-collector output which requires an external pullup resistor.

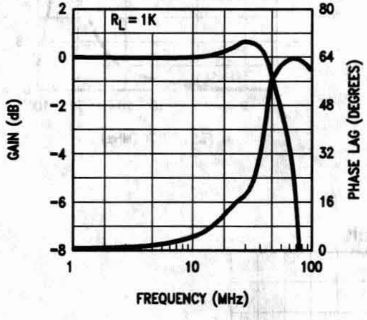
Note 8: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/μs.

Note 9: The test circuit consists of the human body model of 120 pF in series with 1500Ω.

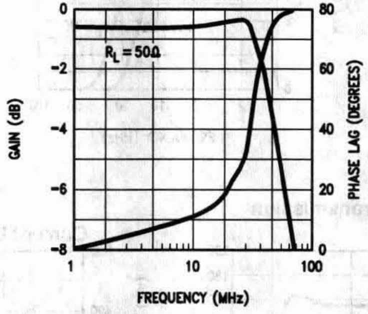
Note 10: A military RETS specification is available on request. At the time of printing, the LM6125H/883 RETS spec complied with the **Boldface** limits in this column. The LM6125H/883 may also be procured as Standard Military Drawing specification #5962-9081501MXX.

Typical Performance Characteristics $T_A = 25°C$, $V_S = \pm15V$, unless otherwise specified

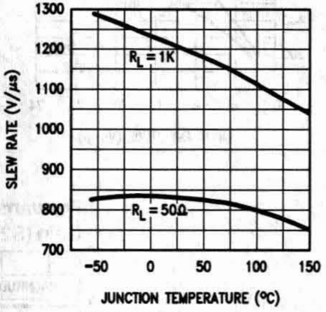
Frequency Response



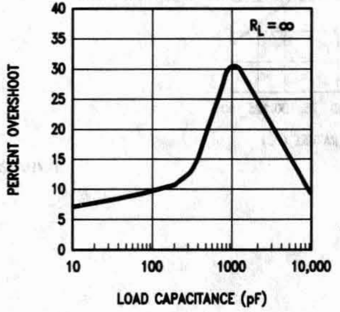
Frequency Response



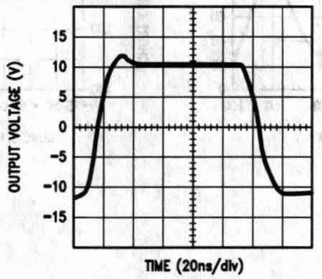
Slew Rate vs Temperature



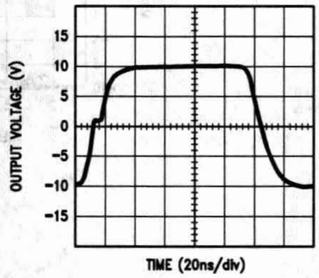
Overshoot vs Capacitive Load



Large Signal Response (R_L = 1 kΩ)



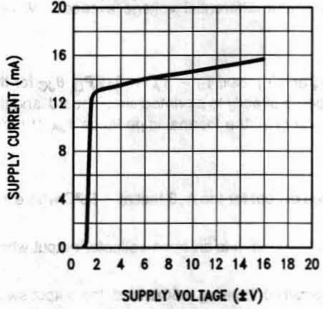
Large Signal Response (R_L = 50Ω)



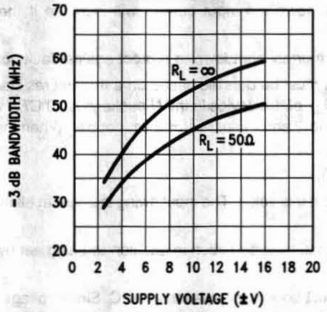
TL/H/9222–5

Typical Performance Characteristics T_A = 25°C, V_S = ±15V, unless otherwise specified (Continued)

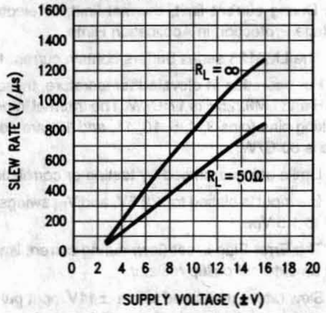
Supply Current



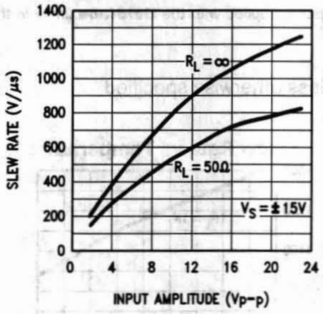
−3 dB Bandwidth



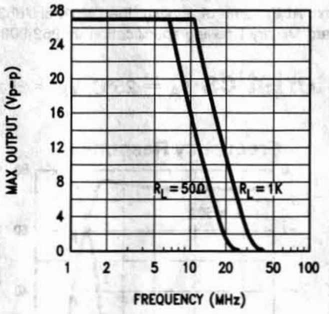
Slew Rate



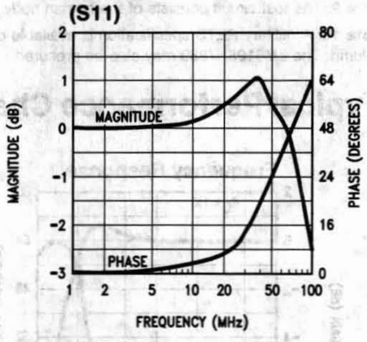
Slew Rate



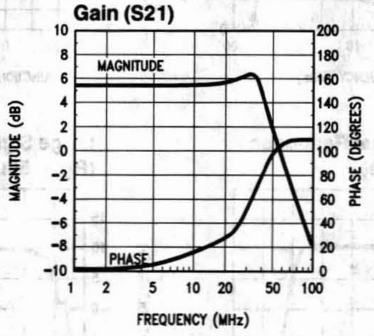
Power Bandwidth



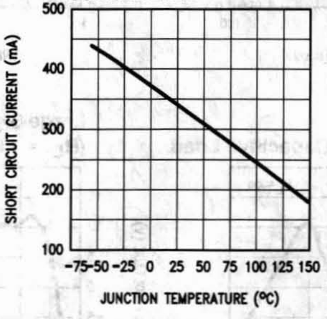
Input Return Gain (S11)



Forward Transmission Gain (S21)

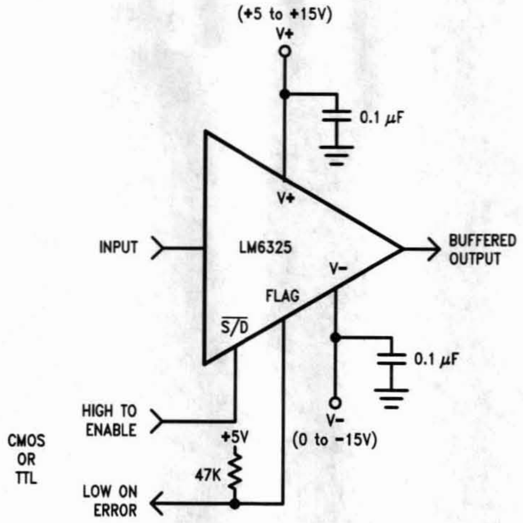


Current Limit



TL/H/9222–7

Typical Connection Diagram



TL/H/9222-6

Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6125 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/µs into a 50Ω load produces a di/dt of 18 A/µs. Multiplying this by a wiring inductance of 50 nH results in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 µF ceramic in parallel with one or two 2.2 µF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6125 is stable into any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

Like any high-frequency buffer, the LM6125 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

ERROR FLAG LOGIC

The Error Flag pin is an open-collector output which requires an external pull-up resistor. Flag voltage is HIGH during operation, and is LOW during a fault condition. A fault condition occurs if either the internal current limit or the thermal shutdown is activated, or the shutdown (S/D) pin is driven low by external logic. Flag voltage returns to its HIGH state when normal operation resumes.

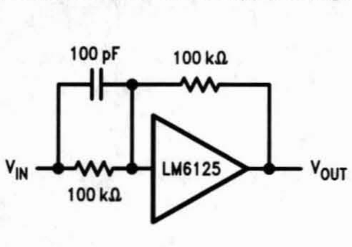
If the S/D pin is not to be used, it should be connected to V+.

OVERVOLTAGE PROTECTION

The LM6125 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6125 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. The damage is cumulative, and may eventually result in complete device failure.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see *Figure 1*). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6125 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.



TL/H/9222-8

FIGURE 1. LM6125 with Overvoltage Protection

Section 3
Voltage Comparators

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Voltage Comparators Definition of Terms

Input Bias Current: The average of the two input currents.

Input Offset Current: The absolute value of the difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

Input Offset Voltage: The absolute value of the voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

Input Voltage Range: The range of voltage on the input terminals (common-mode) over which the offset specifications apply.

Logic Threshold Voltage: The voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

Negative Output Level: The negative DC output voltage with the comparator saturated by a differential input equal to or greater than a specified voltage.

Output Leakage Current: The current into the output terminal with the output voltage within a given range and the input drive equal to or greater than a given value.

Output Resistance: The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

Output Sink Current: The maximum negative current that can be delivered by the comparator.

Positive Output Level: The high output voltage level with a given load and the input drive equal to or greater than a specified value.

Power Consumption: The power required to operate the comparator with no output load. The power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

Response Time: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Saturation Voltage: The low-output voltage level with the input drive equal to or greater than a specified value.

Strobe Current: The current out of the strobe terminal when it is at the zero logic level.

Strobe Output Level: The DC output voltage, independent of input conditions, with the voltage on the strobe terminal equal to or less than the specified low state.

Strobe "ON" Voltage: The maximum voltage on either strobe terminal required to force the output to the specified high state independent of the input voltage.

Strobe "OFF" Voltage: The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator.

Strobe Release Time: The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to the one logic level.

Supply Current: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

Voltage Gain: The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

National Semiconductor

Voltage Comparators Selection Guide

	Response Time (Typ) ns	V_{OS} mV(Max)	I_S mA(Max)	I_B nA(Max)	Special Features
T_A = 25°C (Notes 1 and 2)					
LM6685	2.6	1.9	23	9,000	Single, Very High Speed ECL Output
LM6687	2.6	1.9	38	9,000	Dual, Very High Speed ECL Output
LM360	14	5	32	20,000	High Speed, Complementary Outputs
LM361	14	5	20	30,000	High Speed w/Strobes
LM306	28	5	10	25,000	High Speed, High Drive
LM319	80	8	12.5	1000	High Speed Dual
LM6511	180	5	3.5	130	
LF311	200	10	7.5	0.15	FET Input
LM311	200	7.5	7.5	250	General Purpose Single
LH2311	200	7.5	7.5	250	Dual LM311
LP311	1200	7.5	0.3	100	Low Power Single
LM339	1300	5	2.5	250	General Purpose Quad
LM392	1300	10	1	400	One Comparator Plus One Op Amp
LM393	1300	5	2.5	250	General Purpose Dual
LM2901	1300	7	2.5	250	Automotive Quad
LM612	1500	5	0.250	35	Super-Block™ Dual Comparator + Reference
LM613	1500	5	1	35	Super-Block™ Dual Comparator + Dual Op Amp + Reference
LM615	1500	5	0.600	35	Super-Block™ Quad Comparator + Reference
LM2903	1500	7	2.5	250	Automotive Dual
LP365	4000	6	0.275	75	Programmable Quad
LP339	8000	5	0.1	25	Low Power Quad
LMC676214	4000	5	0.01		MicroPower Rail-to-Rail Input & Output CMOS Comparator
LMC6762	4000	5	20 µA	0.02 pA (typ)	MicroPower Dual
LMC6764	4000	5	40 µA	0.02 pA (typ)	MicroPower Quad
LMC6772	4000	5	20 µA	0.02 pA (typ)	MicroPower Dual, Open Drain Output
LMC6774	4000	5	40 µA	0.02 pA (typ)	MicroPower Quad, Open Drain Output
LMC7211	4000	15	7 µA	0.02 pA (typ)	TinyPak™ SOT23-5 MicroPower Comparator
LMC7221	4000	15	7 µA	0.02 pA (typ)	TinyPak SOT23-5 MicroPower Comparator, Open Drain Output

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: This selection guide should be used to select for Response Time required. Industrial and Military Temperature Range types are available. The DC specs are for the lowest Commercial Grade available.

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LF111/LF211/LF311 Voltage Comparators

General Description

The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to ±15V range the LF111 can be used in the most critical applications.

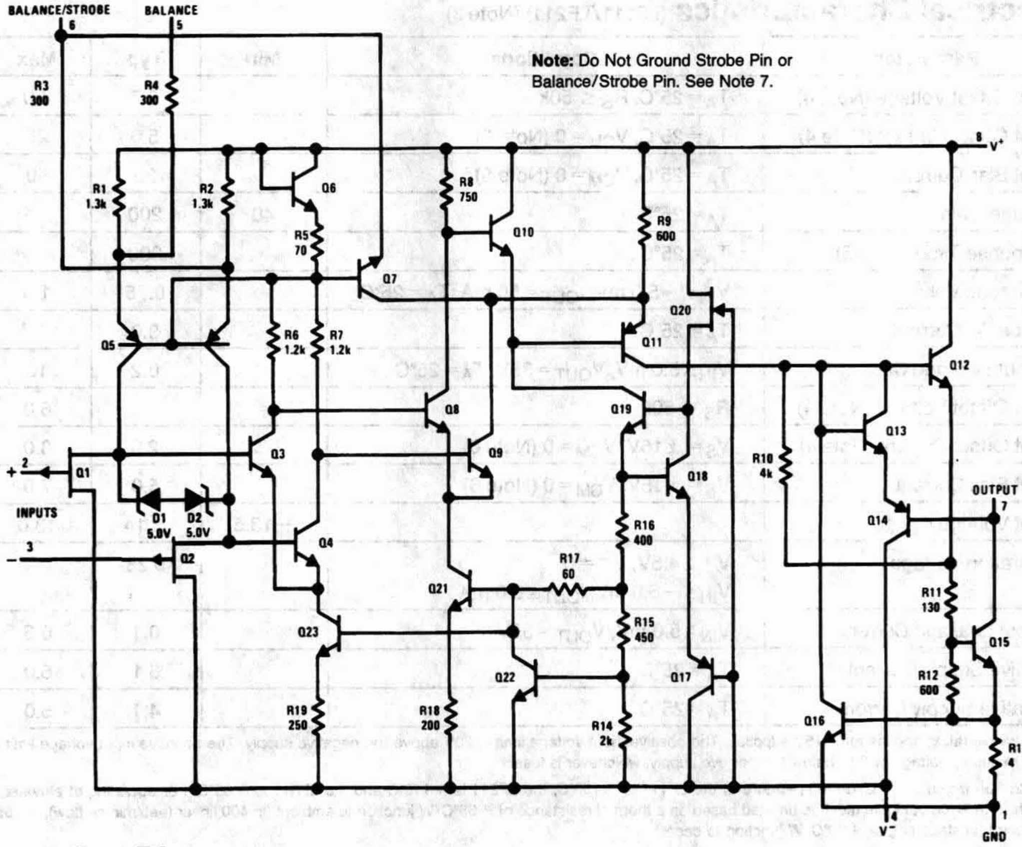
The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done.

Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents. See the "application hints" of the LM311 for application help.

Features

- Eliminates input current errors
- Interchangeable with LM111
- No need for input current buffering

Schematic Diagram

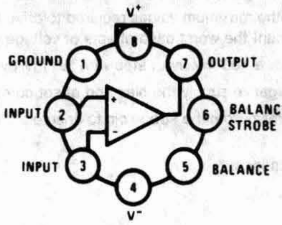

BALANCE/STROBE 6
BALANCE 5
R3 300
R4 300
R1 1.3k
R2 1.3k
Q6
R5 70
Q7
R8 750
Q10
R9 600
8 V+
Q20
Q11
Q12
Q5
R6 1.2k
R7 1.2k
Q8
Q19
Q13
R10 4k
2 +
Q1
Q3
Q9
Q18
OUTPUT 7
INPUTS
D1 5.0V
D2 5.0V
Q4
R16 400
Q14
3 −
Q2
R17 60
Q21
R11 130
Q23
R15 450
Q15
Q22
Q17
R12 600
R19 250
R18 200
R14 2k
Q16
R13 4
4 V−
1 GND

Note: Do Not Ground Strobe Pin or Balance/Strobe Pin. See Note 7.

TL/H/5703–2

Connection Diagram

Metal Can Package


V+
8
GROUND 1
7 OUTPUT
INPUT 2
6 BALANCE/STROBE
INPUT 3
5 BALANCE
4
V−

TL/H/5703–1

Top View

Order Number LF111H, LF111H-MIL or LF311H

See NS Package Number H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 8)

	LF111/LF211	LF311
Total Supply Voltage (V_{84})	36V	36V
Output to Negative Supply Voltage (V_{74})	50V	40V
Ground to Negative Supply Voltage (V_{14})	30V	30V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
Power Dissipation (Note 2)	500 mW	500 mW
Output Short Circuit Duration	10 seconds	10 seconds

	LF111/LF211	LF311
Operating Temp. Range		
LF111	−55°C to +125°C	
LF211	−25°C to +85°C	
LF311		0°C to +70°C
Storage Temp. Range	−65°C to +150°C	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C	260°C

ESD rating to be determined.

Electrical Characteristics (LF111/LF211) (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \le 50k$		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	25	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		20	50	pA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \le -5.0$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \le 5.0$ mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \le 50k$			6.0	mV
Input Offset Current (Note 4)	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		2.0	3.0	nA
Input Bias Current	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		5.0	7.0	nA
Input Voltage Range		−13.5	±14	13.0	V
Saturation Voltage	$V^+ \ge 4.5V$, $V^- = 0$ $V_{IN} \le -6.0$ mV, $I_{OUT} \le 8.0$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \ge 5.0$ mV, $V_{OUT} = 35V$		0.1	0.5	µA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of +65°C/W junction to ambient (in 400 linear feet/min air flow), +165°C/W junction to ambient (in static air), or +20°C/W junction to case.

Note 3: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55°C \le T_A \le +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \le T_A \le \pm 85°C$ and for the LF311 $0°C \le T_A \le +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: This specification gives the current that must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 8: Refer to RETSF111X for LF111H military specifications.

Electrical Characteristics (LF311) (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	10	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	75	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		25	150	pA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$mV, $V_{OUT} = 35$V, $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			15	mV
Input Offset Current (Note 4)	$V_S = \pm 15$V, $V_{CM} = 0$ (Note 6)		1.0		nA
Input Bias Current	$V_S = 15$V, $V_{CM} = 0$ (Note 6)		3.0		nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq 4.5$V, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{OUT} \leq 8.0$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of +165°C/W, junction to ambient, or +20°C/W, junction to case.

Note 3: These specifications apply for $V_S = \pm 15$V and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0 mV supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

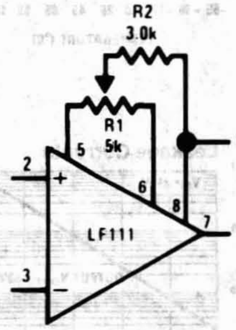
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: This specification gives the current that must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

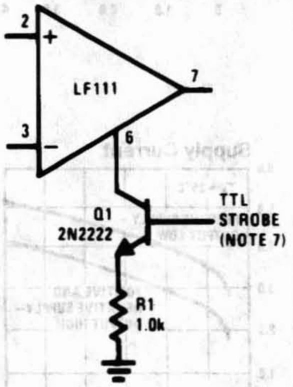
Auxiliary Circuits

Offset Balancing



TL/H/5703-13

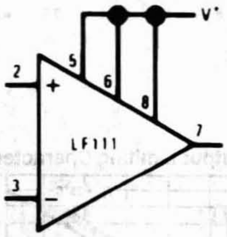
Strobing



TL/H/5703-14

Note: Do Not Ground Strobe Pin.

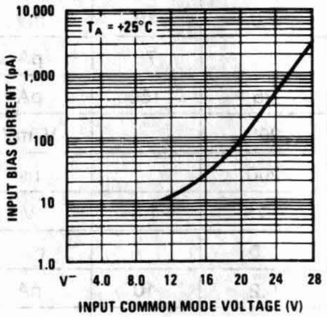
Increasing Input Stage Current*

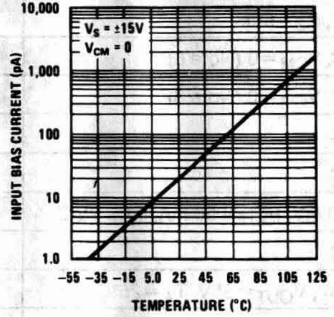


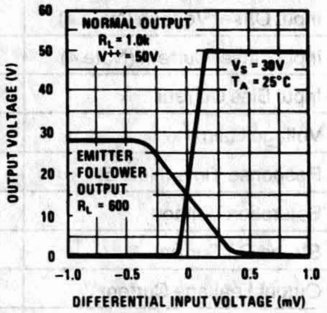
TL/H/5703-15

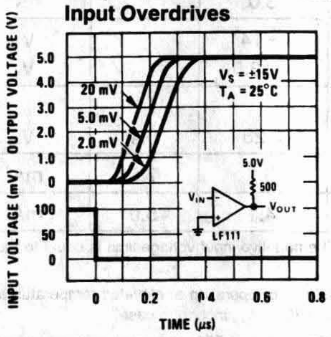
*Increases typical common mode slew from 7.0V/μs to 18V/μs

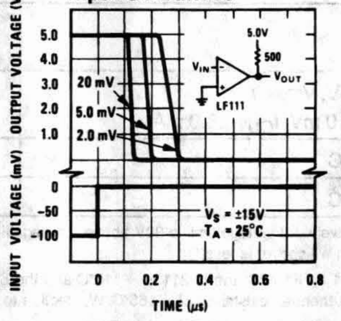
Typical Performance Characteristics

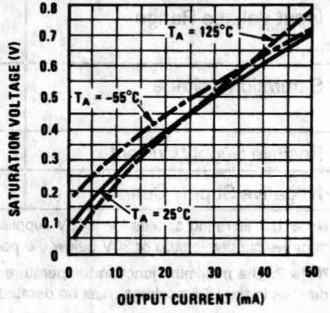

Input Bias Current vs Common Mode

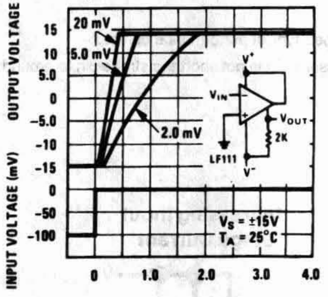

Input Bias Current vs Temperature

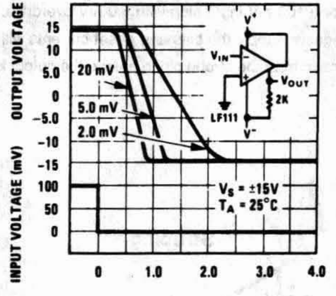

Transfer Function

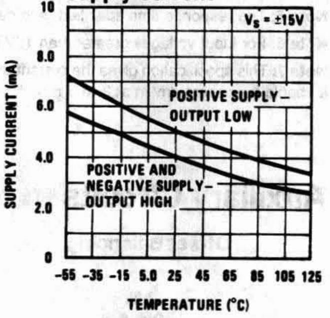

Response Time for Various Input Overdrives

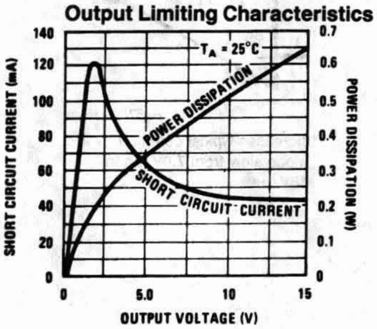

Response Time for Various Input Overdrives

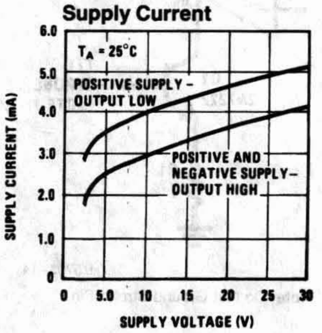

Output Saturation Voltage

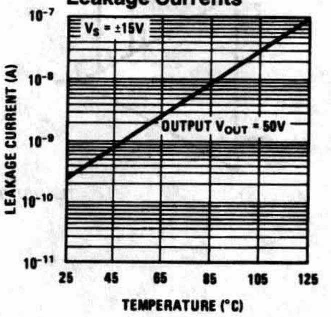

Response Time for Various Input Overdrives


Response Time for Various Input Overdrives


Supply Current


Output Limiting Characteristics

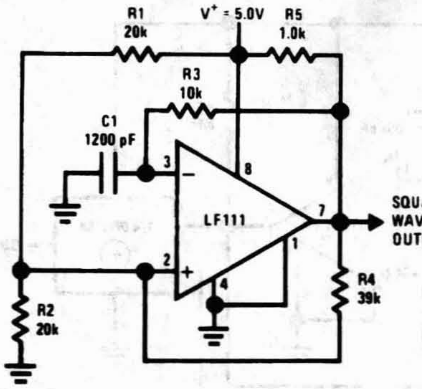

Supply Current


Leakage Currents

TL/H/5703-4

Typical Applications

100 kHz Free Running Multivibrator


R1
20k
V+ = 5.0V
R5
1.0k
R3
10k
C1
1200 pF
3
8
LF111
7
SQUARE
WAVE
OUTPUT*
1
2
4
R4
39k
R2
20k

*TTL or DTL fanout of two.

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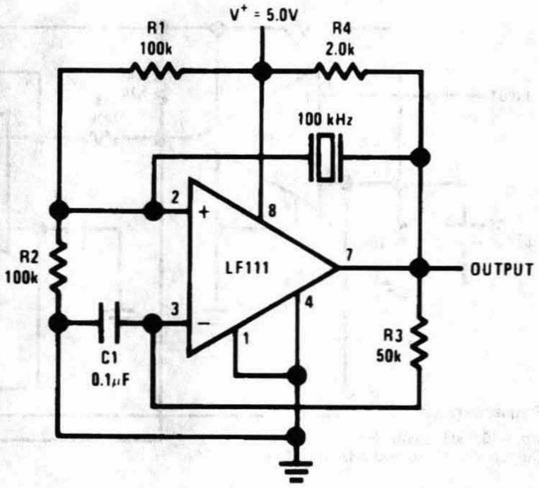
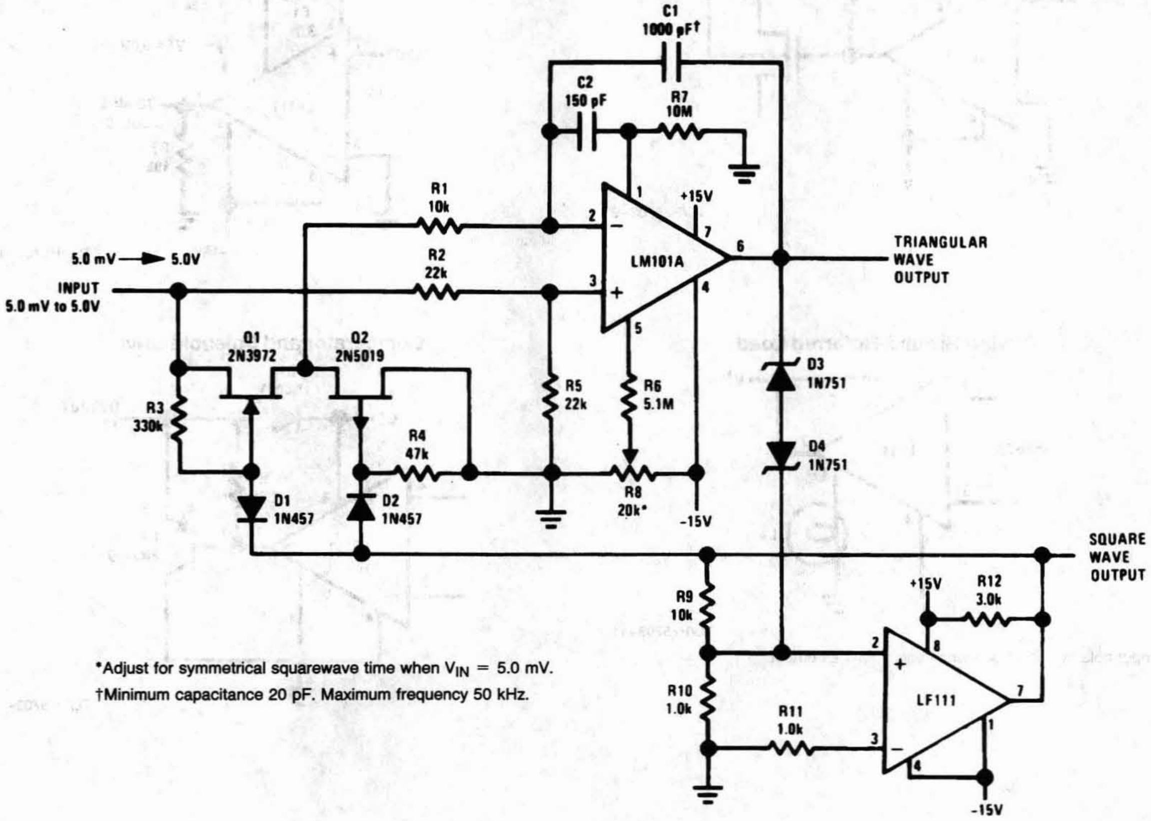
Crystal Oscillator


V+ = 5.0V
R1
100k
R4
2.0k
100 kHz
2
8
R2
100k
LF111
7
OUTPUT
3
4
1
C1
0.1μF
R3
50k

TL/H/5703-3

10 Hz to 10 kHz Voltage Controlled Oscillator


C1
1000 pF†
C2
150 pF
R7
10M
R1
10k
1
+15V
2
7
6
TRIANGULAR
WAVE
OUTPUT
5.0 mV → 5.0V
INPUT
5.0 mV to 5.0V
R2
22k
3
LM101A
4
5
Q1
2N3972
Q2
2N5019
R3
330k
R4
47k
R5
22k
R6
5.1M
D3
1N751
D4
1N751
D1
1N457
D2
1N457
R8
20k*
-15V
SQUARE
WAVE
OUTPUT
R9
10k
+15V
R12
3.0k
2
8
LF111
7
R10
1.0k
R11
1.0k
3
1
4
-15V

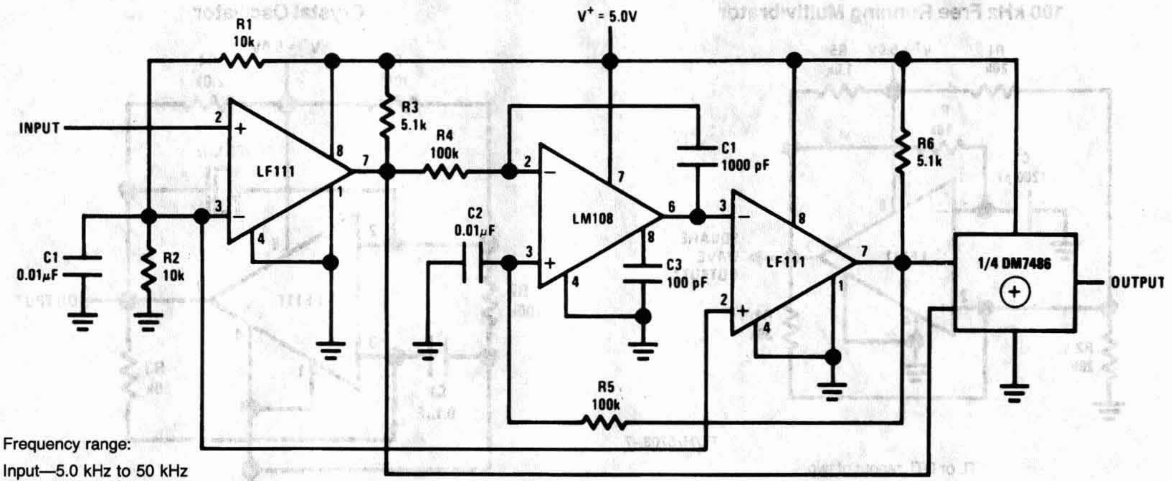
*Adjust for symmetrical squarewave time when V_{IN} = 5.0 mV.

†Minimum capacitance 20 pF. Maximum frequency 50 kHz.

TL/H/5703-5

Typical Applications (Continued)

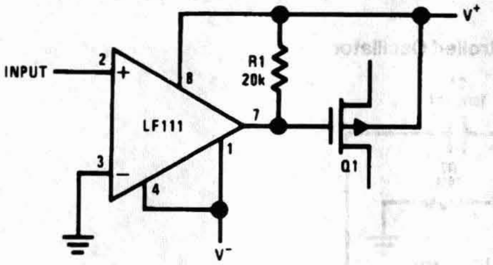
Frequency Doubler


V⁺ = 5.0V
R1
10k
INPUT
R3
5.1k
R4
100k
LF111
C2
0.01µF
LM108
C1
1000 pF
R6
5.1k
C1
0.01µF
R2
10k
C3
100 pF
LF111
1/4 DM7486
OUTPUT
R5
100k
2
3
4
8
7
1
6

Frequency range:
Input—5.0 kHz to 50 kHz
Output—10 kHz to 100 kHz

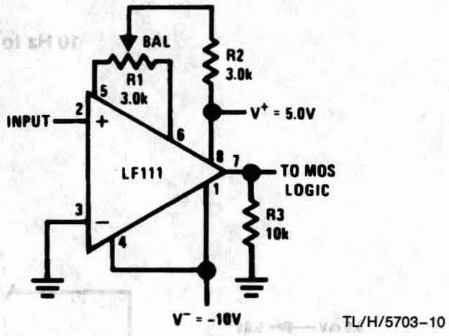
TL/H/5703–8

Zero Crossing Detector Driving MOS Switch


V⁺
INPUT
R1
20k
LF111
Q1
V⁻
2
3
4
8
7
1

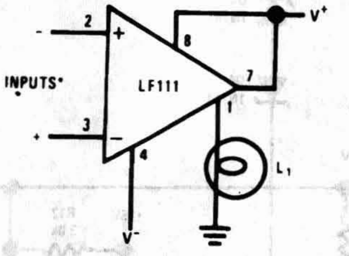
TL/H/5703–9

Zero Crossing Detector Driving MOS Logic


BAL
R1
3.0k
R2
3.0k
V⁺ = 5.0V
INPUT
LF111
TO MOS LOGIC
R3
10k
V⁻ = −10V
2
3
4
5
6
8
7
1

TL/H/5703–10

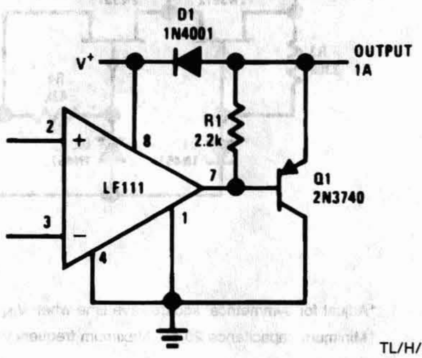
Driving Ground-Referred Load


−
INPUTS*
+
LF111
V⁺
L₁
V⁻
2
3
4
8
7
1

TL/H/5703–11

*Input polarity is reversed when using pin 1 as output.

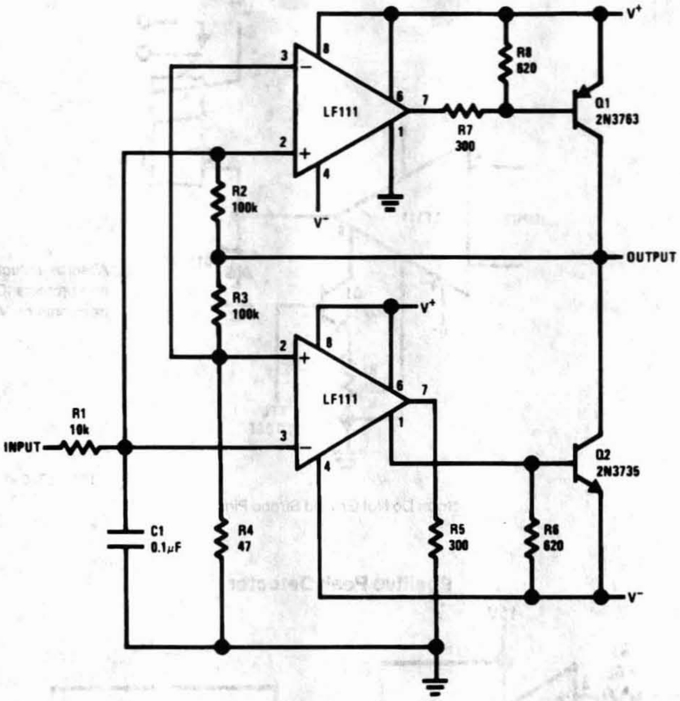
Comparator and Solenoid Driver


D1
1N4001
V⁺
OUTPUT
1A
R1
2.2k
LF111
Q1
2N3740
2
3
4
8
7
1

TL/H/5703–12

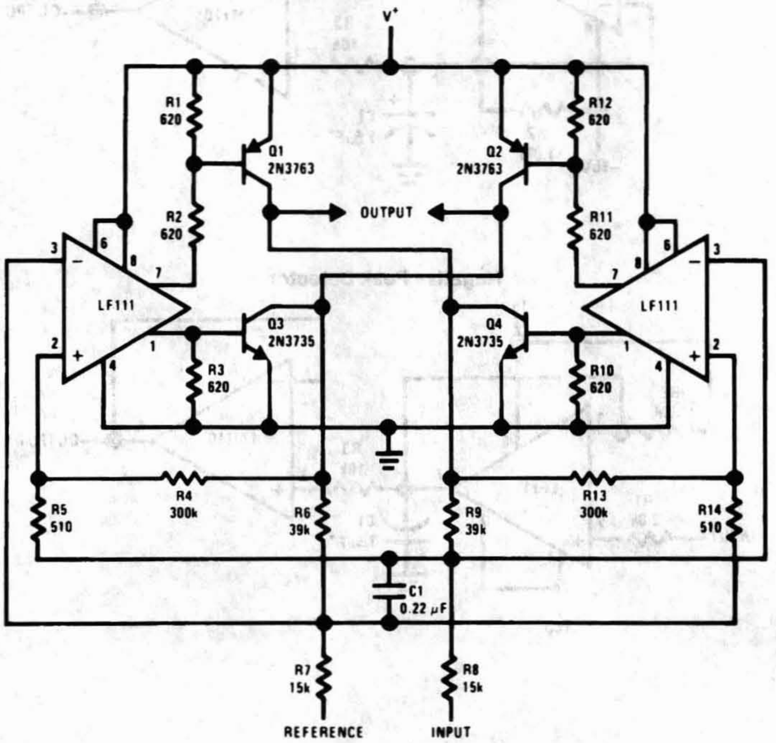
Typical Applications (Continued)

Switching Power Amplifier


V+
R8
620
Q1
2N3763
3
8
LF111
6
7
R7
300
2
1
4
V−
R2
100k
OUTPUT
R3
100k
V+
2
8
LF111
6
7
R1
10k
INPUT
3
1
4
Q2
2N3735
C1
0.1 μF
R4
47
R5
300
R6
620
V−

TL/H/5703–16

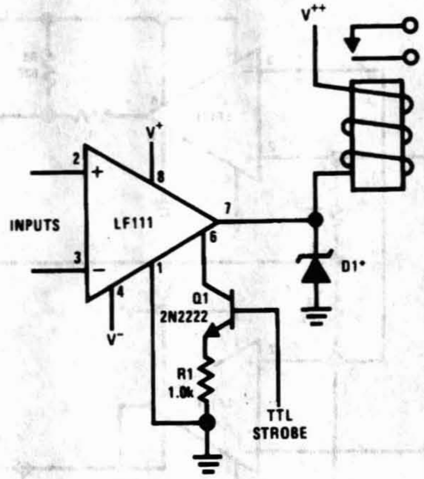
Switching Power Amplifier


V+
R1
620
Q1
2N3763
Q2
2N3763
R12
620
R2
620
OUTPUT
R11
620
3
6
8
7
LF111
2
1
4
Q3
2N3735
Q4
2N3735
7
8
6
3
LF111
1
4
2
R3
620
R10
620
R4
300k
R13
300k
R5
510
R6
39k
R9
39k
R14
510
C1
0.22 μF
R7
15k
R8
15k
REFERENCE
INPUT

TL/H/5703–17

Typical Applications (Continued)

Relay Driver with Strobe

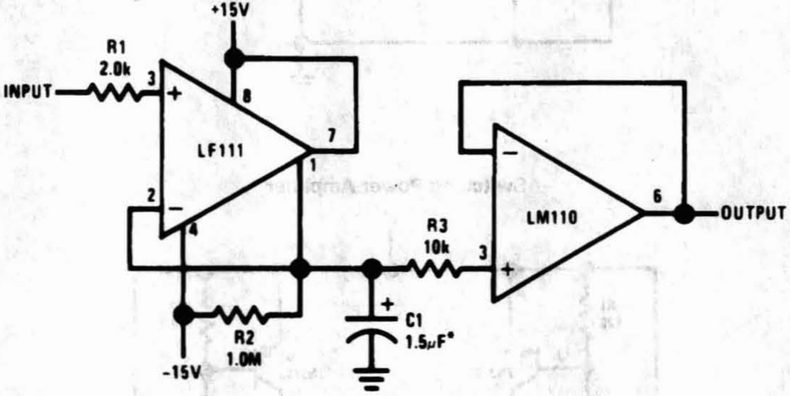

V++
V+
2
+
8
INPUTS
LF111
7
3
−
6
1
4
D1*
Q1
2N2222
V−
R1
1.0k
TTL
STROBE

*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V⁺⁺ line.

TL/H/5703-18

Note: Do Not Ground Strobe Pin.

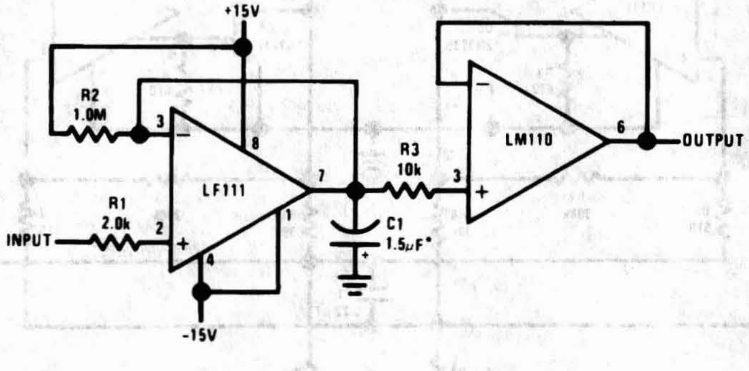
Positive Peak Detector


+15V
R1
2.0k
INPUT
3
+
8
7
LF111
1
2
−
4
−
6
LM110
OUTPUT
R3
10k
3
+
+
C1
1.5μF*
R2
1.0M
−15V

*Solid tantalum

TL/H/5703-19

Negative Peak Detector

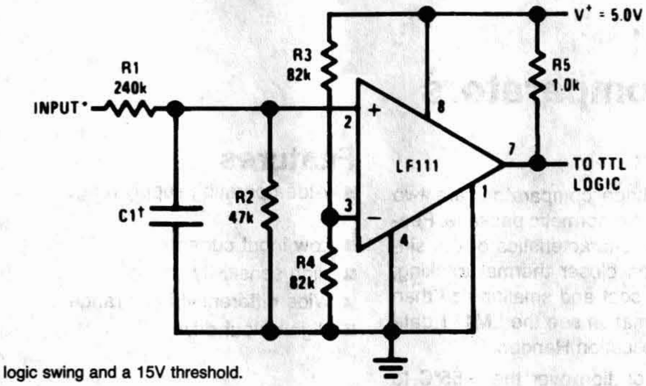

+15V
R2
1.0M
3
−
8
R3
10k
LM110
−
6
OUTPUT
7
3
LF111
+
R1
2.0k
2
1
C1
1.5μF*
INPUT
+
+
4
−15V

*Solid tantalum

TL/H/5703-20

Typical Applications (Continued)

TTL Interface with High Level Logic

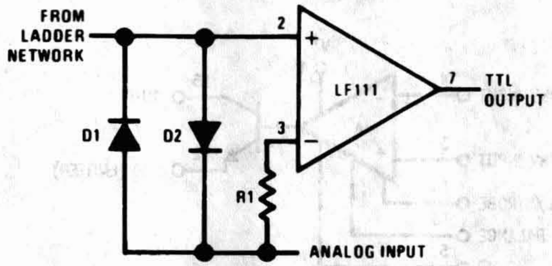

V⁺ = 5.0V
R1
240k
INPUT*
R3
82k
R5
1.0k
8
2
+
LF111
7
TO TTL
LOGIC
1
R2
47k
C1†
3
−
4
R4
82k

*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes

TL/H/5703-21

Using Clamp Diodes to Improve Response


FROM
LADDER
NETWORK
2
+
LF111
7
TTL
OUTPUT
D1
D2
3
−
R1
ANALOG INPUT

TL/H/5703-6

National Semiconductor

LH2111/LH2311
Dual Voltage Comparators

General Description

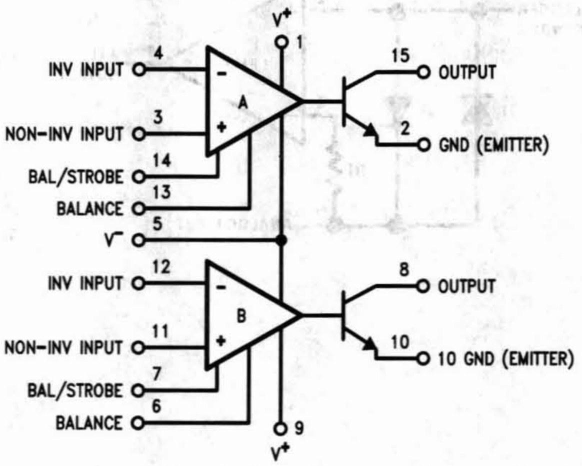
The LH2111 series of dual voltage comparators are two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook.

The LH2111 is specified for operation over the −55°C to +125°C military temperature range. The LH2311 is specified for operation over the 0°C to 70°C temperature range.

Features

■ Wide operating supply range	±15V to a single +5V
■ Low input currents	6 nA
■ High sensitivity	10 μV
■ Wide differential input range	±30V
■ High output drive	50 mA, 50V

Connection Diagram


V+
1
4
INV INPUT
15
OUTPUT
A
3
NON-INV INPUT
2
GND (EMITTER)
14
BAL/STROBE
13
BALANCE
5
V−
12
INV INPUT
8
OUTPUT
B
11
NON-INV INPUT
10
10 GND (EMITTER)
7
BAL/STROBE
6
BALANCE
9
V+

TL/K/10116–1

Order Number LH2111D, LH2111D/883 or LH2311D
See NS Package Number D16C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage ($V^+ - V^-$)	36V
Output to Negative Supply Voltage ($V_{OUT} - V^-$)	50V
Ground to Negative Supply Voltage ($GND - V^-$)	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LH2111	−55°C to +125°C
LH2311	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics Each Side (Note 3)

Parameter	Conditions	Limits		Units
		LH2111	LH2311	
Input Offset Voltage (Note 4)	$T_A = 25°C, R_S \le 50k$	3.0	7.5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	250	nA Max
Voltage Gain	$T_A = 25°C$	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	ns Typ
Saturation Voltage	$V_{IN} \le -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$	1.5	1.5	V Max
Strobe On Current	$T_A = 25°C$	3.0	3.0	mA Typ
Output Leakage Current	$V_{IN} \ge 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \le 50k$	4.0	10	mV Max
Input Offset Current (Note 4)		20	70	nA Max
Input Bias Current		150	300	nA Max
Input Voltage Range		±14	±14	V Typ
Saturation Voltage	$V^+ \ge 4.5V, V^- = 0$ $V_{IN} \le -5$ mV, $I_{SINK} \le 8$ mA	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6.0	7.5	mA Max
Negative Supply Current	$T_A = 25°C$	5.0	5.0	mA Max

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature is 150°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2 ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \le T_A \le 125°C$ for the LH2111, and $0°C \le T_A \le 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm 10$ mV.

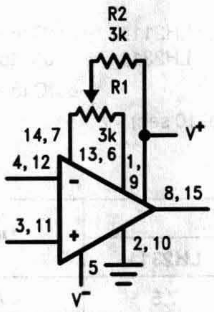
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Note 6: RETS2111X for the LH2111D and LH2111F military specifications.

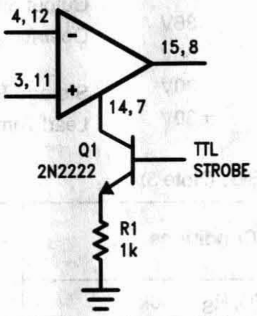
Auxiliary Circuits

Offset Balancing


R2
3k
R1
3k
14, 7
13, 6
1,
9
V+
4, 12
3, 11
8, 15
2, 10
5
V−

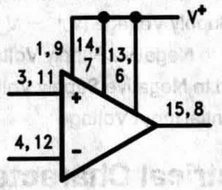
TL/K/10116–2

Strobing


4, 12
15, 8
3, 11
14, 7
Q1
2N2222
TTL
STROBE
R1
1k

TL/K/10116–3

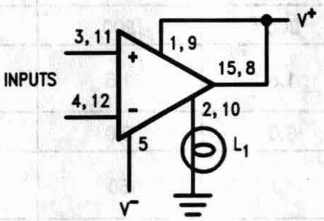
Increasing Input Stage Current*


V+
1, 9
14,
7
13,
6
3, 11
15, 8
4, 12

TL/K/10116–4

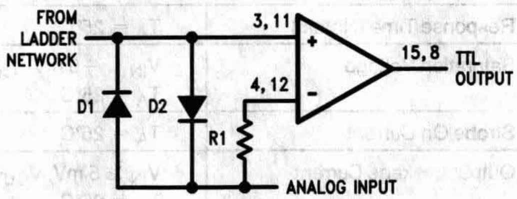
*Increases typical common mode slew from 7.0 V/μs to 18 V/μs

Driving Ground-Referred Load


V+
3, 11
1, 9
INPUTS
15, 8
4, 12
2, 10
5
L1
V−

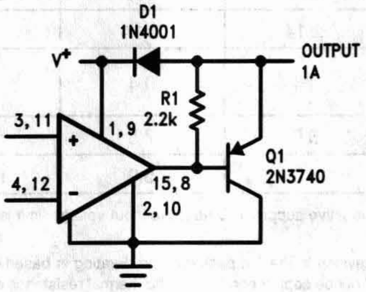
TL/K/10116–5

Using Clamp Diodes to Improve Responses


FROM
LADDER
NETWORK
3, 11
15, 8
TTL
OUTPUT
4, 12
D1
D2
R1
ANALOG INPUT

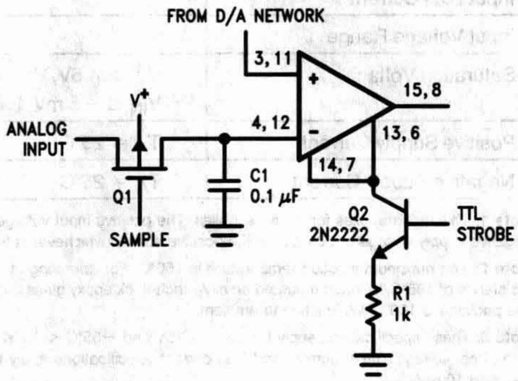
TL/K/10116–6

Comparator and Solenoid Driver


D1
1N4001
V+
OUTPUT
1A
R1
2.2k
3, 11
1, 9
Q1
2N3740
4, 12
15, 8
2, 10

TL/K/10116–7

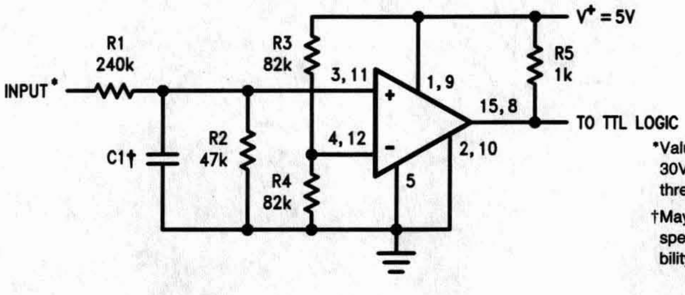
Strobing off Both Input* and Output Stages


FROM D/A NETWORK
3, 11
15, 8
V+
ANALOG
INPUT
4, 12
13, 6
14, 7
C1
0.1 μF
Q1
SAMPLE
Q2
2N2222
TTL
STROBE
R1
1k

TL/K/10116–8

*Typical input current is 50 pA with inputs strobed off

TTL Interface with High Level Logic


V+ = 5V
R1
240k
R3
82k
R5
1k
INPUT*
3, 11
1, 9
15, 8
TO TTL LOGIC
C1†
R2
47k
4, 12
2, 10
R4
82k
5

*Values shown are for a 0V to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

TL/K/10116–9

National Semiconductor

LM106/LM306 Voltage Comparator

General Description

The LM106 series are high-speed voltage comparators designed to accurately detect low-level analog signals and drive a digital load. They are equivalent to an LM710, combined with a two input NAND gate and an output buffer. The circuits can drive RTL, DTL or TTL integrated circuits directly. Furthermore, their outputs can switch voltages up to 24V at currents as high as 10 mA.

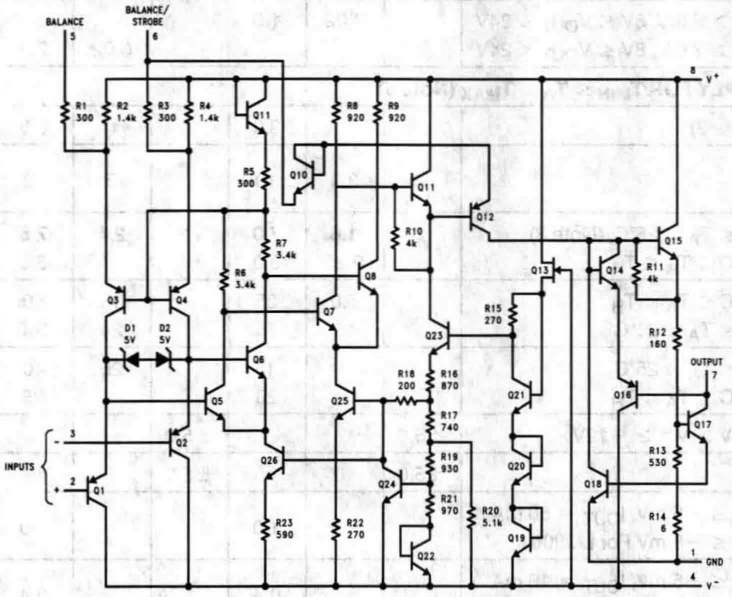
The devices have short-circuit protection which limits the inrush current when it is used to drive incandescent lamps, in addition to preventing damage from accidental shorts to the positive supply. The speed is equivalent to that of an LM710. However, they are even faster where buffers and additional logic circuitry can be eliminated by the increased flexibility of the LM106 series. They can also be operated from any negative supply voltage between −3V and −12V with little effect on performance.

The LM106 is specified for operation over the −55°C to +125°C military temperature range. The LM306 is specified for operation over 0°C to +70°C temperature range.

Features

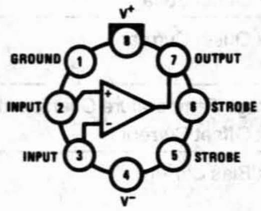
- Improved accuracy
- Fan-out of 10 with DTL or TTL
- Added logic or strobe capability
- Useful as a relay or lamp driver
- Plug-in replacement for the LM710
- 40 ns maximum response time

Schematic and Connection Diagrams


BALANCE
5
BALANCE/ STROBE
6
8
V+
R1 300
R2 1.4k
R3 300
R4 1.4k
Q11
R8 920
R9 920
R5 300
Q10
Q11
Q12
R10 4k
R7 3.4k
R6 3.4k
Q8
Q7
Q3
Q4
D1 5V
D2 5V
Q6
Q5
Q25
Q23
R15 270
Q13
Q14
R11 4k
Q15
R12 160
OUTPUT 7
Q16
Q17
R18 200
R16 870
R17 740
Q21
INPUTS
3
2
Q2
Q1
Q26
R19 930
Q20
R13 530
Q24
R21 970
R20 5.1k
Q18
R14 6
R23 590
R22 270
Q22
Q19
1 GND
4 V−

TL/H/7756–1

Metal Can


V+
8
GROUND 1
OUTPUT 7
INPUT 2
6 STROBE
INPUT 3
5 STROBE
4
V−

TL/H/7756–2

Top View

Note: Pin 4 connected to case.

Order Number LM106H, LM106H/883† or LM306H
See NS Package Number H08A

†Available per SMD# 8003701

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Positive Supply Voltage	15V
Negative Supply Voltage	−15V
Output Voltage	24V
Output to Negative Supply Voltage	30V
Differential Input Voltage	±5V
Input Voltage	±7V
Power Dissipation (Note 1)	600 mW
Output Short Circuit Duration	10 seconds
Operating Temperature Range	T_{MIN} T_{MAX}
LM106	−55°C to +125°C
LM306	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics (Note 2)

Parameter	Conditions	LM106			LM306			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 3)		0.5	2.0		1.6	5.0	mV
Input Offset Current	(Note 3)		0.7	3.0		1.8	5.0	μA
Input Bias Current			10	20		16	25	μA
Response Time	$R_L = 390\Omega$ to 5V $C_L = 15$ pF, (Note 4)		28	40		28	40	ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 100$ mA		1.0	1.5				V
	$V_{IN} \leq -7$ mV, $I_{OUT} = 100$ mA					0.8	2.0	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8V \leq V_{OUT} \leq 24V$		0.02	1.0				μA
	$V_{IN} \geq 7$ mV, $8V \leq V_{OUT} \leq 24V$					0.02	2.0	μA
THE FOLLOWING SPECIFICATIONS APPLY FOR $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 5)								
Input Offset Voltage	(Note 3)			3.0			6.5	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	10		5	20	μV/°C
Input Offset Current	$T_L \leq T_A \leq 25°C$, (Note 3)		1.8	7.0		2.4	7.5	μA
	$25°C \leq T_A \leq T_H$		0.25	3.0			5.0	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_H$		5.0	25		15	50	nA/°C
	$T_L \leq T_A \leq 25°C$		15	75		24	100	nA/°C
Input Bias Current	$T_L \leq T_A \leq 25°C$			45		25	40	μA
	$25°C \leq T_A \leq T_H$			20			25	μA
Input Voltage Range	$-7V \geq V^- \geq -12V$	±5.0			±5.0			V
Differential Input Voltage Range		±5.0			±5.0			V
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $V_{IN} \leq -8$ mV For LM306			1.0			1.0	V
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 16$ mA $V_{IN} \leq -8$ mV For LM306			0.4			0.4	V
Positive Output Level	$V_{IN} \geq 5$ mV, $I_{OUT} = -400\mu A$ $V_{IN} \geq 8$ mV For LM306	2.5		5.5	2.5		5.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8V \leq V_{OUT} \leq 24V$ $V_{IN} \geq 8$ mV For LM306 $T_L \leq T_A \leq 25°C$			1.0			2.0	μA
	$25°C < T_A \leq T_H$			100			100	μA
Strobe Current	$V_{STROBE} = 0.4V$		−1.7	−3.2		−1.7	−3.2	mA

Electrical Characteristics (Note 2) (Continued)

Parameter	Conditions	LM106			LM306			Units
		Min	Typ	Max	Min	Typ	Max	
Strobe "ON" Voltage		0.9	1.4		0.9	1.4		V
Strobe "OFF" Voltage	$I_{SINK} \leq 16$ mA		1.4	2.2		1.4	2.2	V
Positive Supply Current	$V_{IN} = -5$ mV $V_{IN} = -8$ mV for LM306		5.5	10		5.5	10	mA
Negative Supply Current			−1.5	−3.6		−1.5	−3.6	mA

Note 1: The maximum junction temperature of LM106 is 150°C, LM306 is 85°C. For operating at elevated temperatures, devices must be derated based on a thermal resistance of 170°C/W, junction to ambient, or 23°C/W, junction to case.

Note 2: These specifications apply for $-3V \geq V^- \geq -12V$, $V^+ = 12V$ and $T_A = 25°C$ unless otherwise specified. All currents into device pins are considered positive.

Note 3: The offset voltages and offset currents given are the maximum values required to drive the output down to 0.5V or up to 4.4V (0.5V or up to 4.8V for the LM306). Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain, specified supply voltage variations, and common mode voltage variations.

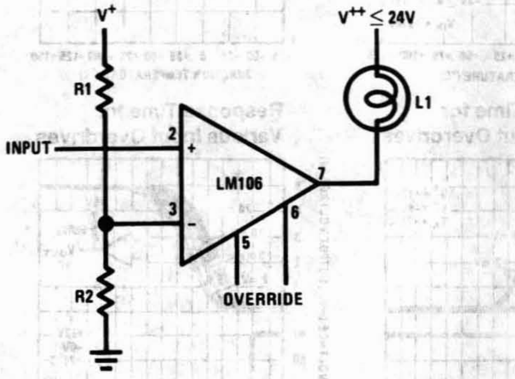
Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 5: All currents into device pins are considered positive.

Note 6: Refer to RETS106X for LM106 military specifications.

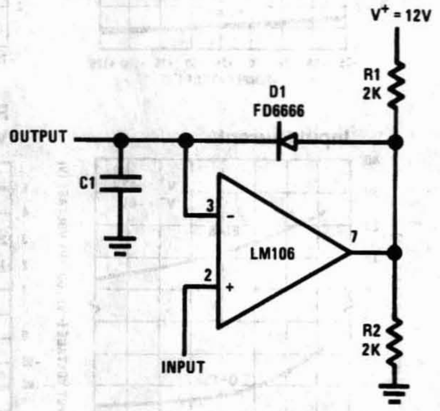
Typical Applications

Level Detector and Lamp Driver


V+
V++ ≤ 24V
R1
L1
INPUT
2
+
LM106
7
3
−
6
5
R2
OVERRIDE

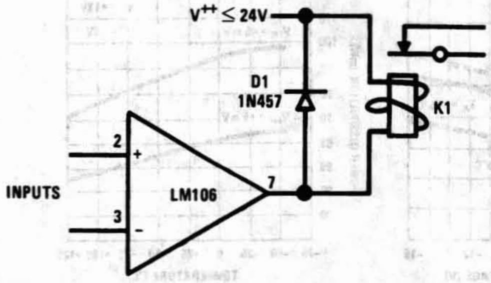
TL/H/7756-4

Fast Response Peak Detector


V+ = 12V
R1
2K
D1
FD6666
OUTPUT
C1
3
−
LM106
7
2
+
INPUT
R2
2K

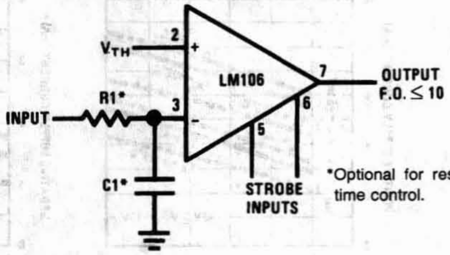
TL/H/7756-5

Relay Driver


V++ ≤ 24V
D1
1N457
K1
2
+
INPUTS
LM106
7
3
−

TL/H/7756-6

Adjustable Threshold Line Receiver

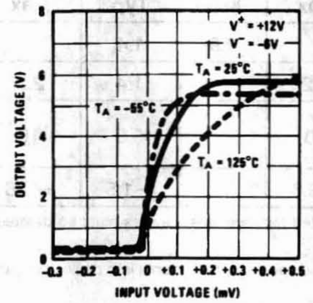

2
+
VTH
LM106
7
OUTPUT
F.O. ≤ 10
R1*
INPUT
3
−
6
5
C1*
STROBE
INPUTS

*Optional for response time control.

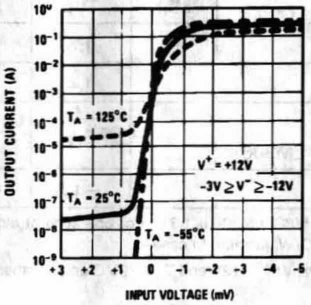
TL/H/7756-7

Typical Performance Characteristics

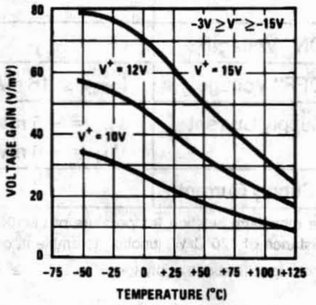
Transfer Function



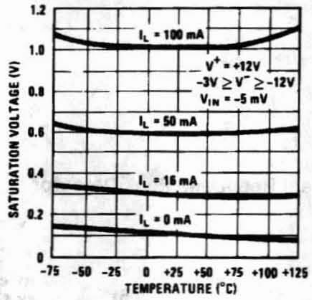
Transconductance



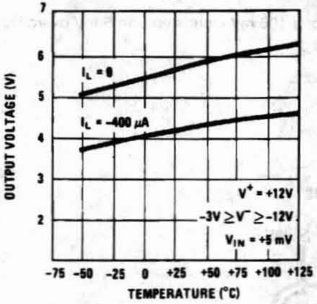
Voltage Gain



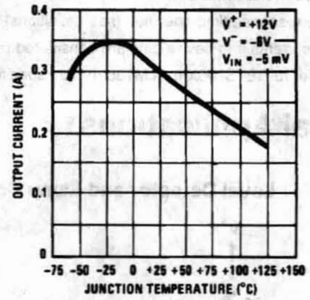
Saturation Voltage



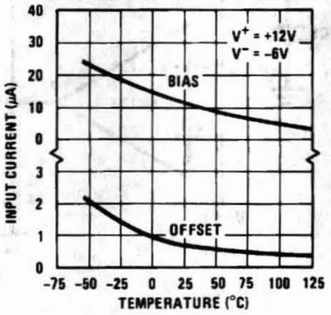
Positive Output Level



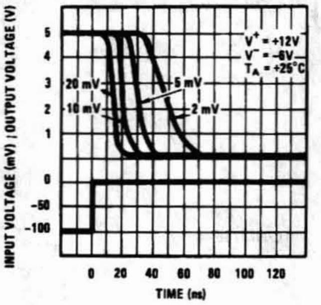
Short Circuit Output Current



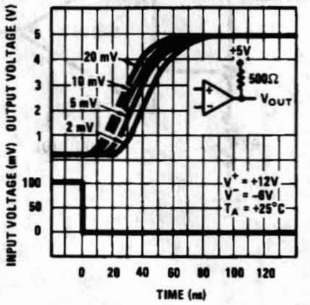
Input Current



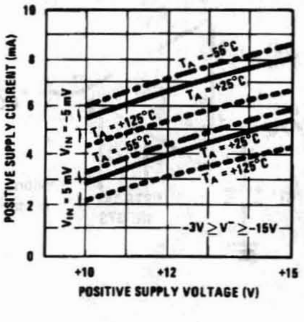
Response Time for Various Input Overdrives



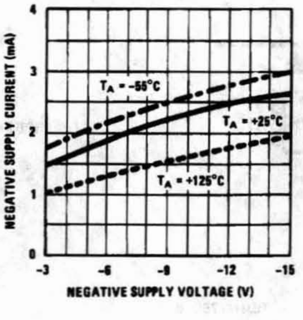
Response Time for Various Input Overdrives



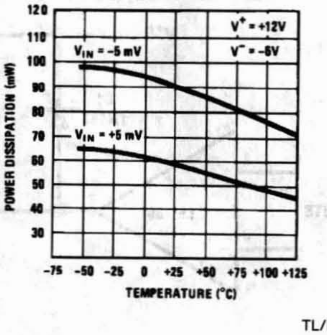
Positive Supply Current



Negative Supply Current



Power Consumption



TL/H/7756–8

National Semiconductor

LM111/LM211/LM311 Voltage Comparator

General Description

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

The LM211 is identical to the LM111, except that its performance is specified over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM311 has a temperature range of 0°C to +70°C.

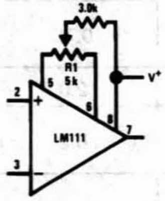
Features

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

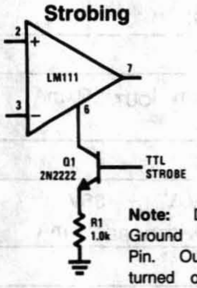
Typical Applications**

**Note: Pin connections shown on schematic diagram and typical applications are for H08 metal can package.

Offset Balancing

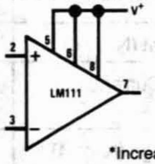

R2
3.0k
R1
5k
V+
5
6
8
2
3
7
LM111

Strobing


2
3
7
6
LM111
Q1
2N2222
TTL
STROBE
R1
1.0k

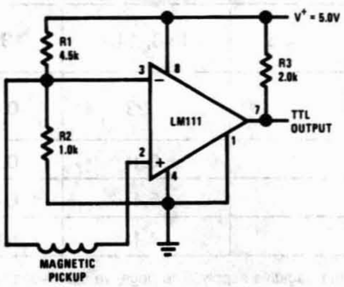
Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

Increasing Input Stage Current*

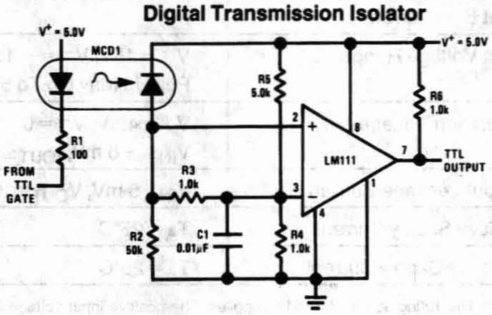

V+
5
6
8
2
3
7
LM111

*Increases typical common mode slew from 7.0V/µs to 18V/µs.

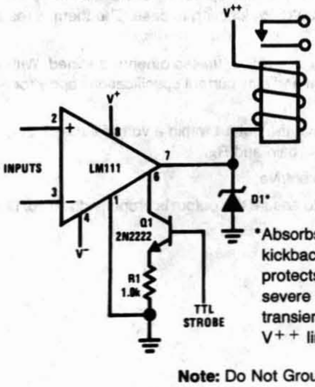
Detector for Magnetic Transducer


V+ = 5.0V
R1
4.5k
R2
1.0k
R3
2.0k
3
8
2
7
1
LM111
TTL
OUTPUT
MAGNETIC
PICKUP

Digital Transmission Isolator


V+ = 5.0V
MCD1
R1
100
FROM
TTL
GATE
R3
1.0k
R2
50k
C1
0.01µF
R4
1.0k
R5
5.0k
R6
1.0k
2
3
7
8
1
LM111
V+ = 5.0V
TTL
OUTPUT

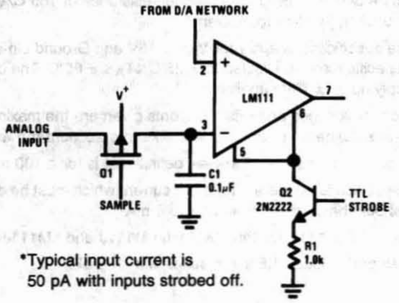
Relay Driver with Strobe


V++
V+
2
3
8
7
6
4
1
INPUTS
LM111
D1*
Q1
2N2222
R1
1.0k
V-
TTL
STROBE

*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

Note: Do Not Ground Strobe Pin.

Strobing off Both Input* and Output Stages


FROM D/A NETWORK
2
3
7
6
5
LM111
V+
ANALOG
INPUT
Q1
SAMPLE
C1
0.1µF
Q2
2N2222
TTL
STROBE
R1
1.0k

*Typical input current is 50 pA with inputs strobed off.

Note: Do Not Ground Strobe Pin.

TL/H/5704–1

Absolute Maximum Ratings for the LM111/LM211

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	50V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Output Short Circuit Duration	10 sec
Operating Temperature Range LM111	−55°C to 125°C
LM211	−25°C to 85°C
Lead Temperature (Soldering, 10 sec)	260°C
Voltage at Strobe Pin	$V^+ - 5V$

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Rating (Note 8)	300V

Electrical Characteristics for the LM111 and LM211 (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \le 50k$		0.7	3.0	mV
Input Offset Current	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \le -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current (Note 6)	$T_A = 25°C$		2.0	5.0	mA
Output Leakage Current	$V_{IN} \ge 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \le 50$ k			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range	$V^+ = 15V$, $V^- = -15V$, Pin 7 Pull-Up May Go To 5V	−14.5	13.8,-14.7	13.0	V
Saturation Voltage	$V^+ \ge 4.5V$, $V^- = 0$ $V_{IN} \le -6$ mV, $I_{OUT} \le 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \ge 5$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 110°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and Ground pin at ground, and $-55°C \le T_A \le +125°C$, unless otherwise stated. With the LM211, however, all temperature specifications are limited to $-25°C \le T_A \le +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and R_S.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 7: Refer to RETS111X for the LM111H, LM111J and LM111J-8 military specifications.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Absolute Maximum Ratings for the LM311

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage V_{74})	40V
Ground to Negative Supply Voltage V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
ESD Rating (Note 7)	300V
Output Short Circuit Duration	10 sec
Operating Temperature Range	0° to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	260°C
Voltage at Strobe Pin	$V^+ - 5V$

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) ....260°C
- Small Outline Package
  - Vapor Phase (60 seconds) ....215°C
  - Infrared (15 seconds) ....220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics for the LM311 (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \le 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \le -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current (Note 6)	$T_A = 25°C$		2.0	5.0	mA
Output Leakage Current	$V_{IN} \ge 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA $V^- =$ Pin 1 $= -5V$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \le 50K$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8, −14.7	13.0	V
Saturation Voltage	$V^+ \ge 4.5V$, $V^- = 0$ $V_{IN} \le -10$ mV, $I_{OUT} \le 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and Pin 1 at ground, and $0°C < T_A < +70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

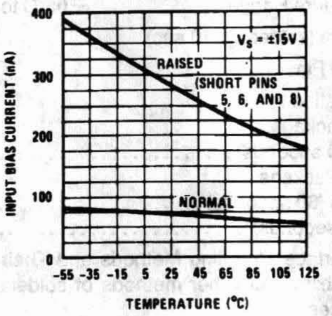
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and R_S.

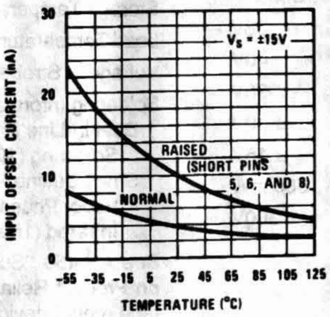
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

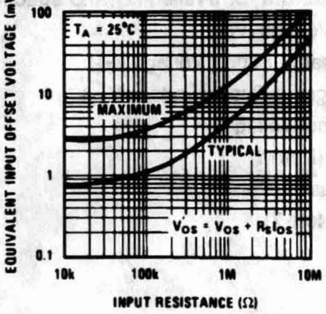
Note 6: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

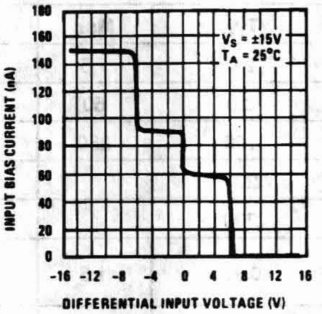
Note 7: Human body model, 1.5 kΩ in series with 100 pF.

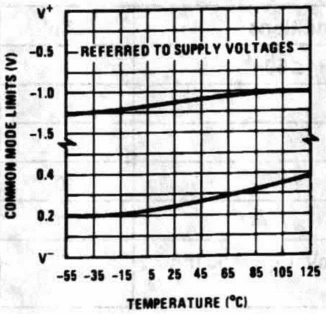
LM111/LM211 Typical Performance Characteristics

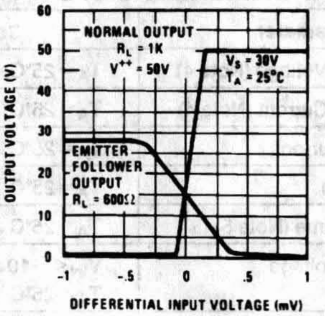

Input Bias Current

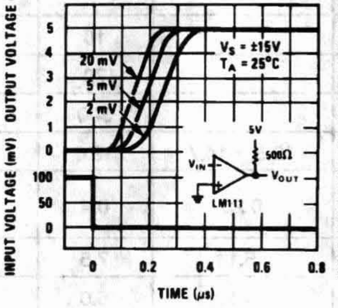

Input Offset Current

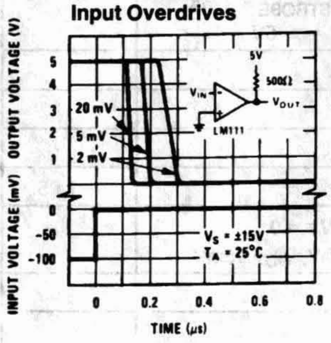

Offset Error

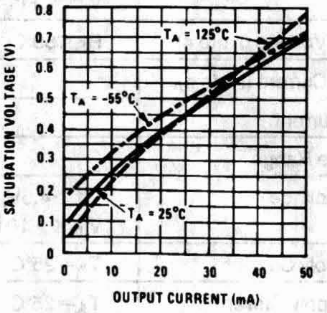

Input Characteristics

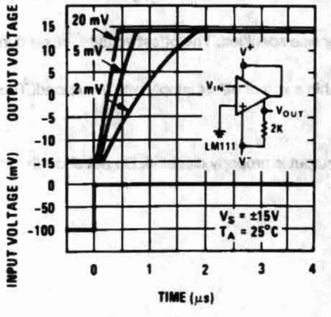

Common Mode Limits

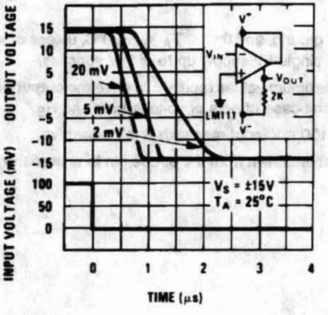

Transfer Function

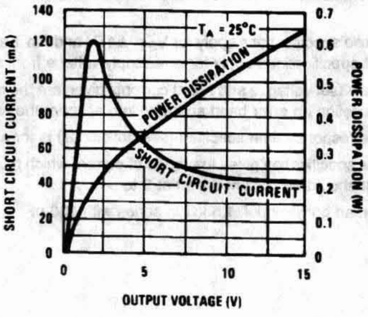

Response Time for Various Input Overdrives


Response Time for Various Input Overdrives


Output Saturation Voltage


Response Time for Various Input Overdrives

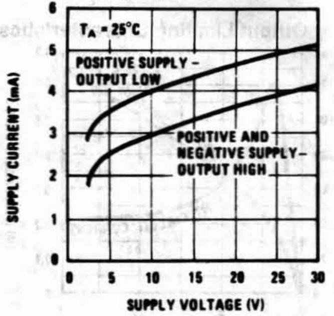

Response Time for Various Input Overdrives


Output Limiting Characteristics

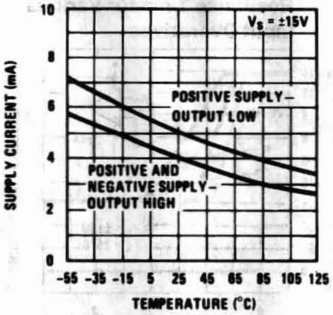
TL/H/5704–2

LM111/LM211 Typical Performance Characteristics (Continued)

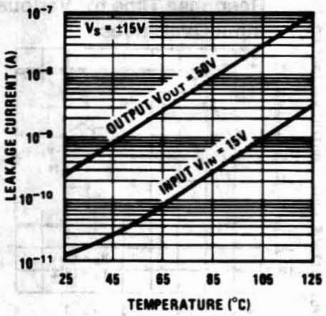
Supply Current



Supply Current



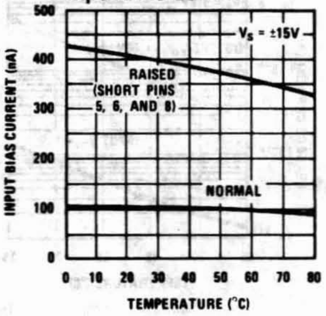
Leakage Currents



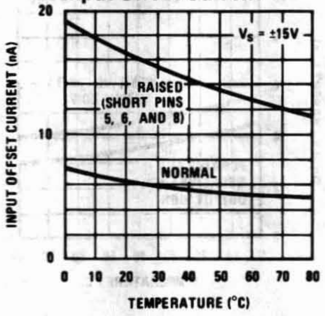
TL/H/5704–3

LM311 Typical Performance Characteristics

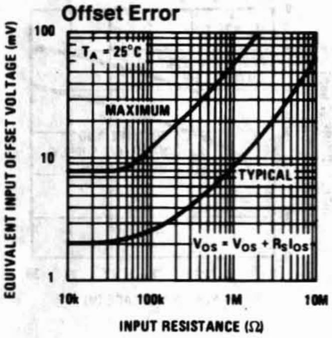
Input Bias Current



Input Offset Current

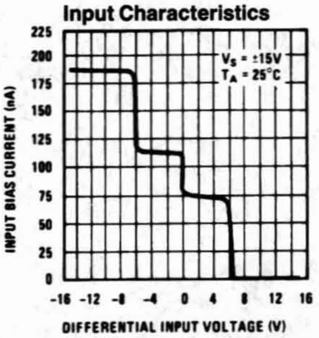


Offset Error

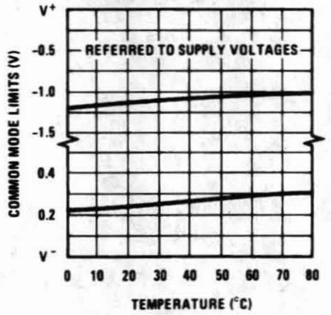


TL/H/5704–8

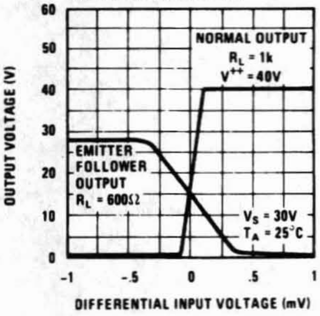
Input Characteristics



Common Mode Limits

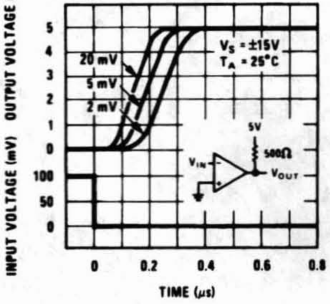


Transfer Function

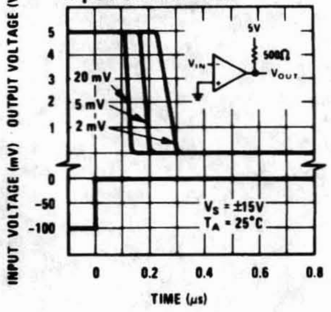


TL/H/5704–9

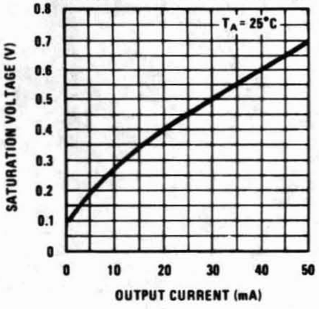
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

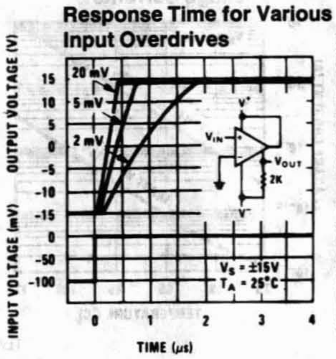


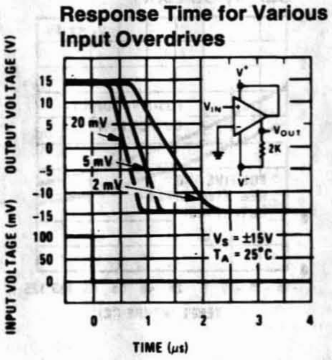
Output Saturation Voltage

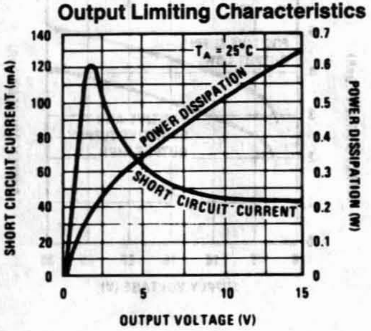


TL/H/5704–10

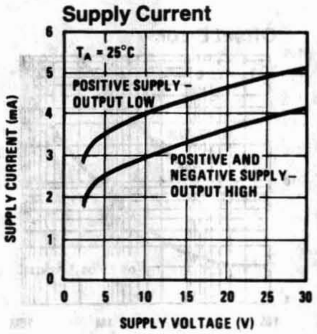
LM311 Typical Performance Characteristics (Continued)

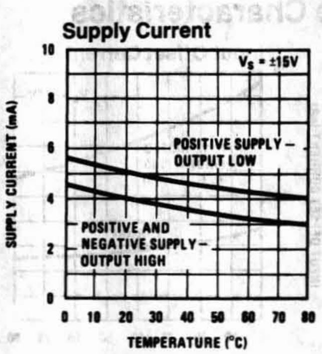

Response Time for Various Input Overdrives

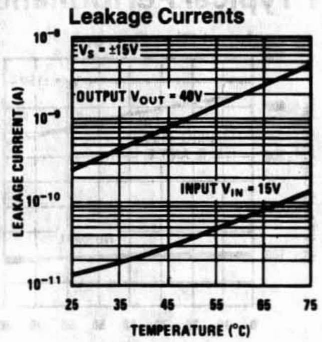

Response Time for Various Input Overdrives


Output Limiting Characteristics

TL/H/5704–11


Supply Current


Supply Current


Leakage Currents

TL/H/5704–12

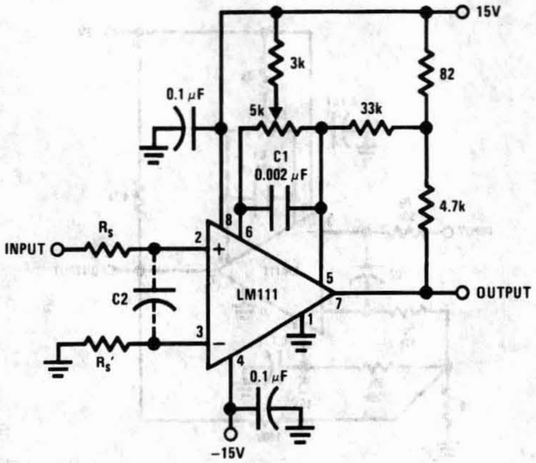
Application Hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 µF capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.
4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if $R_S = 10\ k\Omega$, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 µF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



TL/H/5704–29

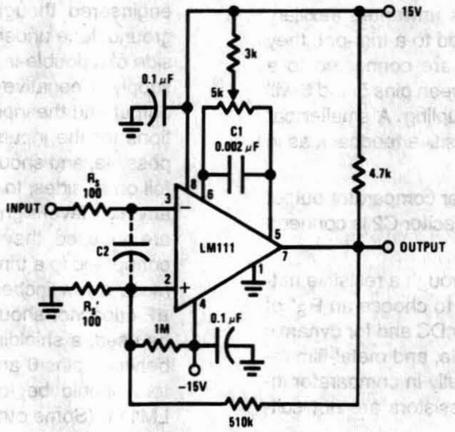
Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 1. Improved Positive Feedback

3

Application Hints (Continued)

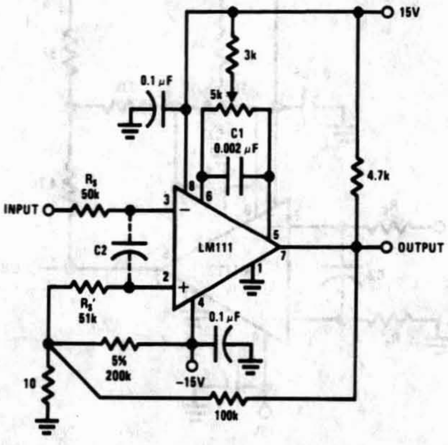
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. the circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.
8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



TL/H/5704–30

Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 2. Conventional Positive Feedback

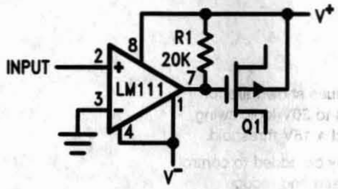


TL/H/5704–31

FIGURE 3. Positive Feedback with High Source Resistance

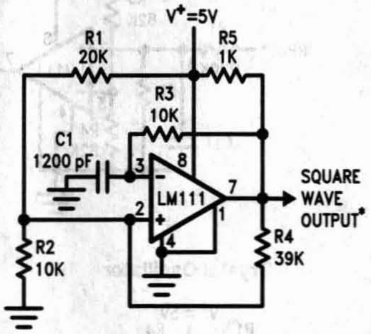
Typical Applications (Continued) (Pin numbers refer to H08 package)

Zero Crossing Detector Driving MOS Switch


V+
INPUT
2
3
8
4
7
1
LM111
R1
20K
Q1
V−

TL/H/5704-13

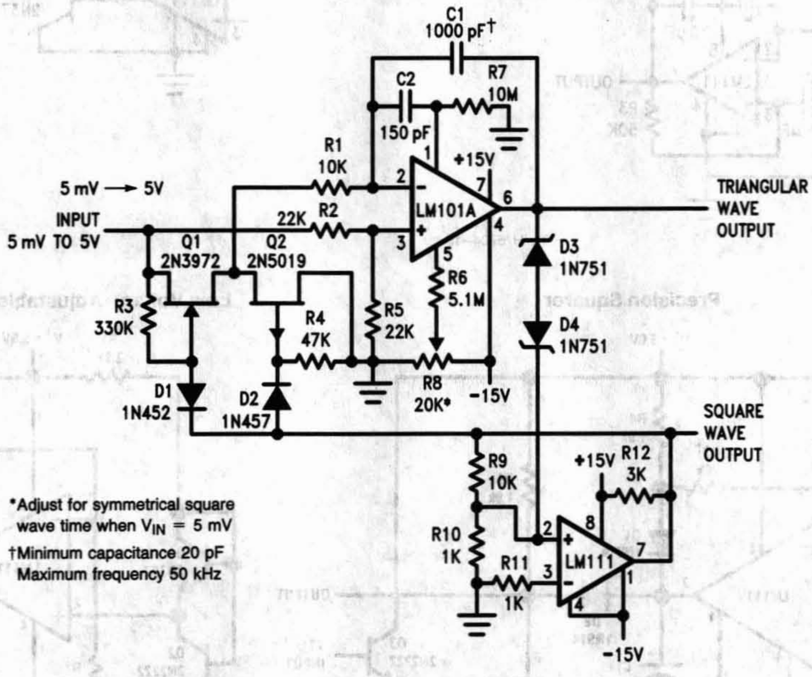
100 kHz Free Running Multivibrator


V+=5V
R1
20K
R5
1K
R3
10K
C1
1200 pF
3
8
2
7
1
4
LM111
SQUARE
WAVE
OUTPUT*
R2
10K
R4
39K

*TTL or DTL fanout of two

TL/H/5704-14

10 Hz to 10 kHz Voltage Controlled Oscillator

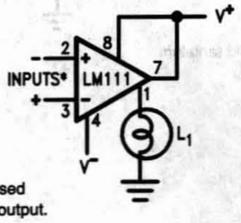

C1
1000 pF†
C2
150 pF
R7
10M
R1
10K
+15V
5 mV → 5V
INPUT
5 mV TO 5V
22K
R2
LM101A
TRIANGULAR
WAVE
OUTPUT
Q1
2N3972
Q2
2N5019
R3
330K
R4
47K
R5
22K
R6
5.1M
R8
20K*
−15V
D3
1N751
D4
1N751
D1
1N452
D2
1N457
SQUARE
WAVE
OUTPUT
R9
10K
+15V
R12
3K
R10
1K
R11
1K
LM111
−15V

*Adjust for symmetrical square wave time when V_{IN} = 5 mV

†Minimum capacitance 20 pF Maximum frequency 50 kHz

TL/H/5704-15

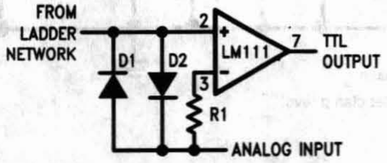
Driving Ground-Referred Load


V+
INPUTS*
LM111
2
3
8
4
7
1
V−
L1

*Input polarity is reversed when using pin 1 as output.

TL/H/5704-16

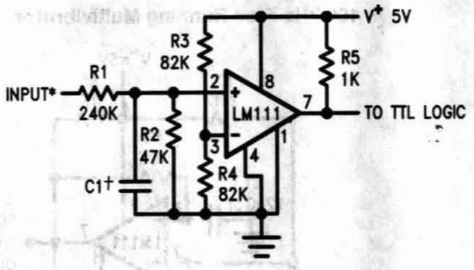
Using Clamp Diodes to Improve Response


FROM
LADDER
NETWORK
D1
D2
LM111
2
3
7
TTL
OUTPUT
R1
ANALOG INPUT

TL/H/5704-17

Typical Applications (Continued) (Pin numbers refer to H08 package)

TTL Interface with High Level Logic

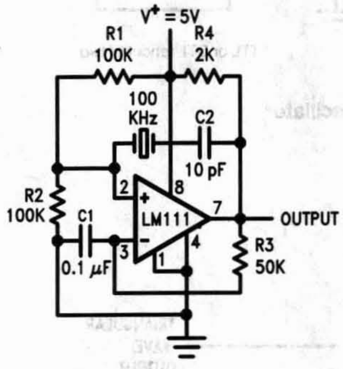

V+ 5V
R3
82K
R1
240K
INPUT*
R2
47K
C1†
R4
82K
R5
1K
LM111
2
3
8
4
7
1
TO TTL LOGIC

*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

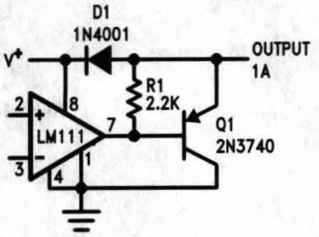
TL/H/5704-18

Crystal Oscillator


V+ = 5V
R1
100K
R4
2K
100
KHz
C2
10 pF
R2
100K
C1
0.1 µF
LM111
2
3
8
4
7
1
R3
50K
OUTPUT

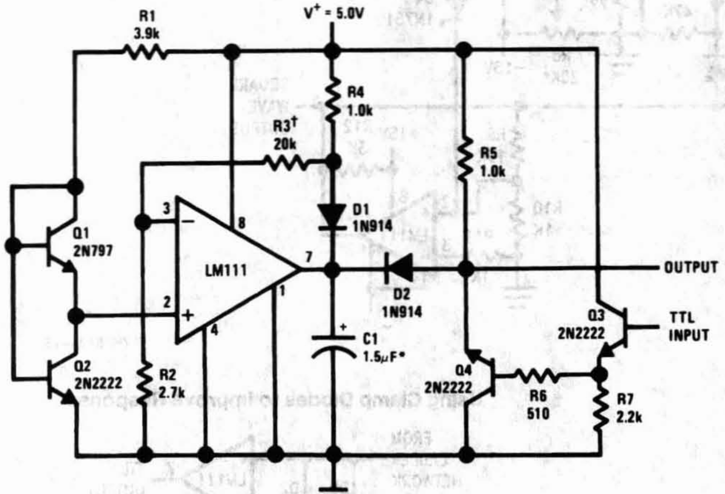
TL/H/5704-19

Comparator and Solenoid Driver


D1
1N4001
V+
OUTPUT
1A
R1
2.2K
Q1
2N3740
LM111
2
3
8
4
7
1

TL/H/5704-20

Precision Squarer

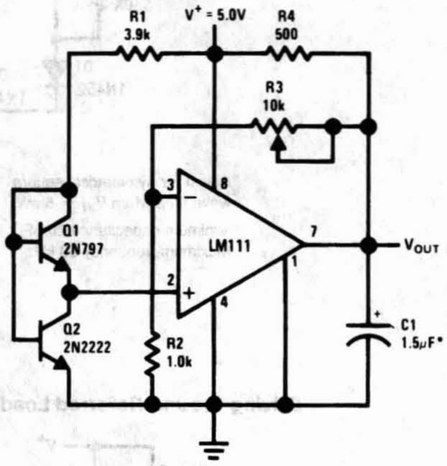

R1
3.9k
V+ = 5.0V
R4
1.0k
R3†
20k
R5
1.0k
D1
1N914
D2
1N914
Q1
2N797
Q2
2N2222
R2
2.7k
LM111
3
2
8
4
7
1
C1
1.5µF*
OUTPUT
Q3
2N2222
TTL
INPUT
Q4
2N2222
R6
510
R7
2.2k

*Solid tantalum

†Adjust to set clamp level

TL/H/5704-21

Low Voltage Adjustable Reference Supply

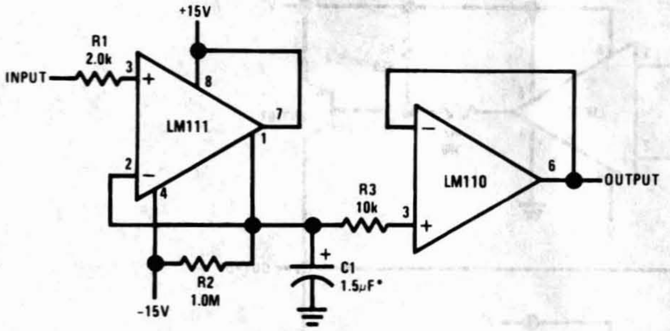

R1
3.9k
V+ = 5.0V
R4
500
R3
10k
Q1
2N797
Q2
2N2222
LM111
3
2
8
4
7
1
R2
1.0k
C1
1.5µF*
VOUT

*Solid tantalum

TL/H/5704-22

Typical Applications (Continued) (Pin numbers refer to H08 package)

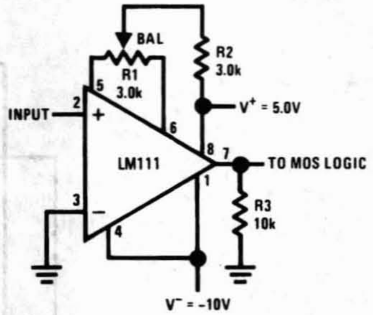
Positive Peak Detector


+15V
R1
2.0k
INPUT
3
+
8
LM111
7
1
2
−
4
R2
1.0M
−15V
+
C1
1.5μF*
R3
10k
3
+
−
LM110
6
OUTPUT

*Solid tantalum

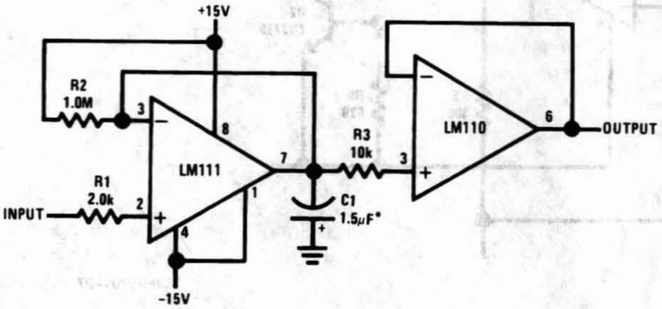
TL/H/5704–23

Zero Crossing Detector Driving MOS Logic


BAL
R1
3.0k
R2
3.0k
5
INPUT
2
+
6
LM111
8
7
1
3
−
4
V+ = 5.0V
TO MOS LOGIC
R3
10k
V− = −10V

TL/H/5704–24

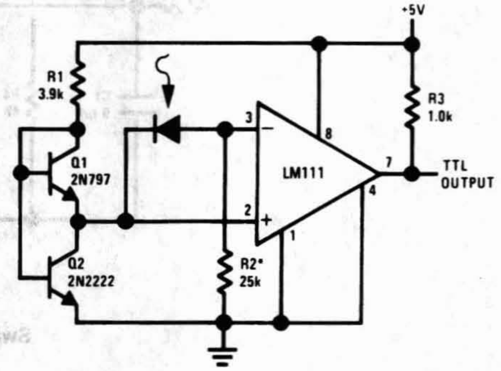
Negative Peak Detector


+15V
R2
1.0M
3
−
8
LM111
7
1
R1
2.0k
INPUT
2
+
4
−15V
C1
1.5μF*
+
R3
10k
3
+
−
LM110
6
OUTPUT

*Solid tantalum

TL/H/5704–25

Precision Photodiode Comparator

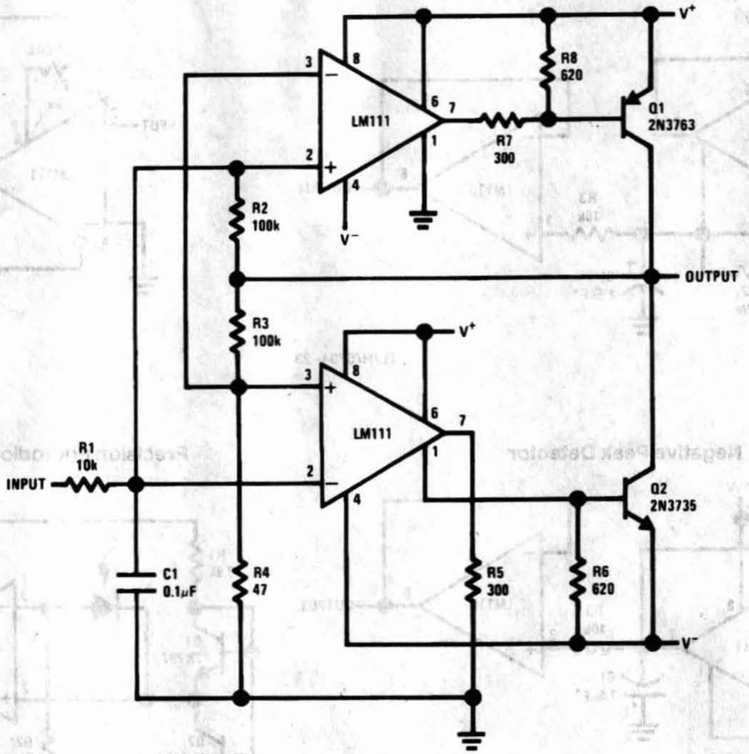

+5V
R1
3.9k
Q1
2N797
Q2
2N2222
R2*
25k
3
−
2
+
8
LM111
7
4
1
R3
1.0k
TTL
OUTPUT

TL/H/5704–26

*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

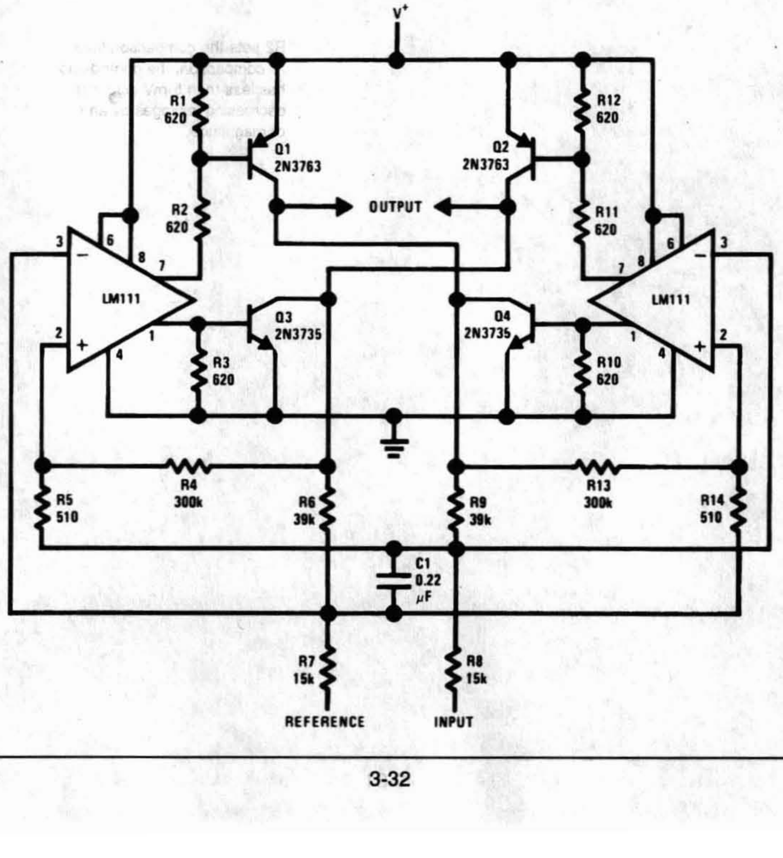
Typical Applications (Continued) (Pin numbers refer to H08 package)

Switching Power Amplifier


V+
3
8
R8
620
6
7
LM111
R7
300
Q1
2N3763
2
1
4
V−
R2
100k
OUTPUT
R3
100k
V+
3
8
6
7
LM111
1
R1
10k
INPUT
2
4
Q2
2N3735
C1
0.1μF
R4
47
R5
300
R6
620
V−

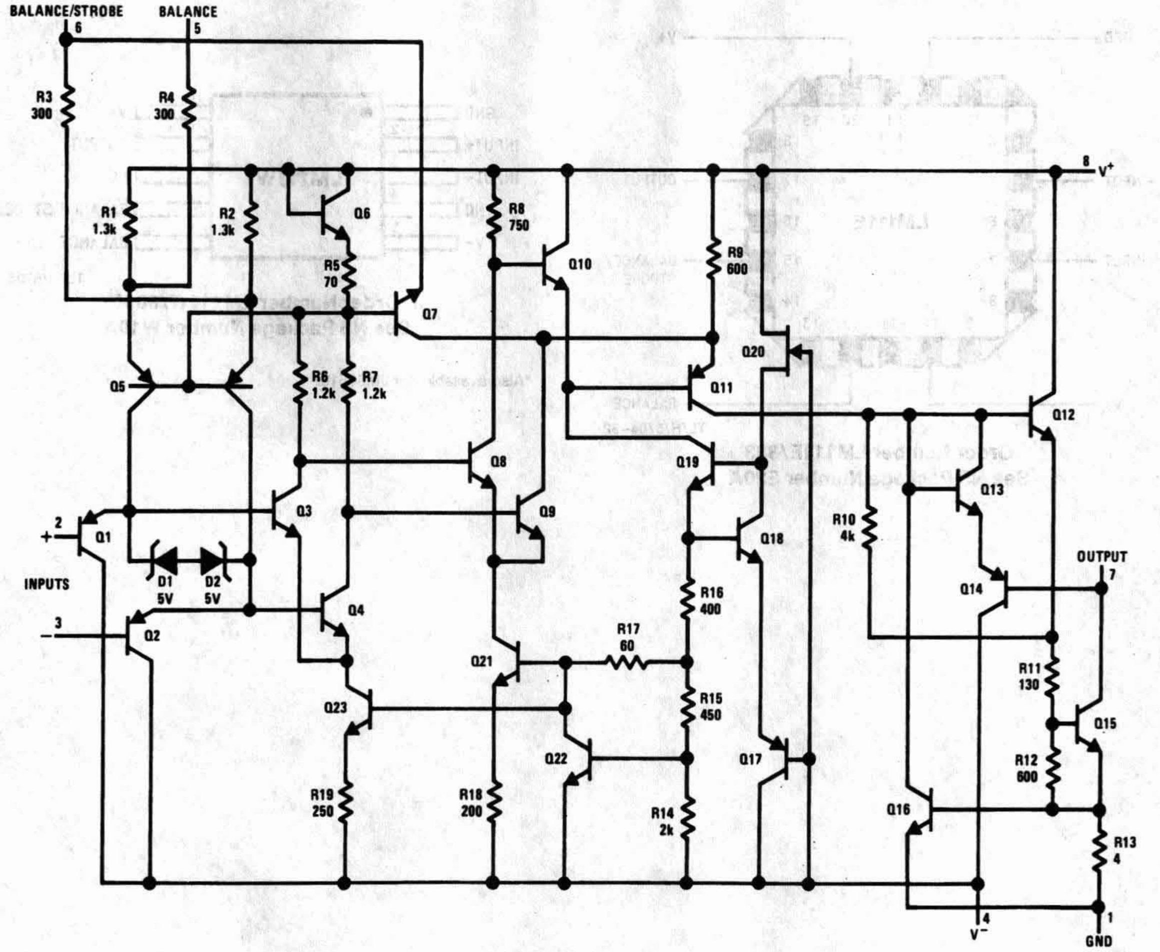
TL/H/5704-27

Switching Power Amplifier


V+
R1
620
Q1
2N3763
Q2
2N3763
R12
620
R2
620
OUTPUT
R11
620
3
6
8
7
LM111
2
1
4
Q3
2N3735
Q4
2N3735
R3
620
R10
620
7
8
6
3
LM111
1
4
2
R4
300k
R13
300k
R5
510
R6
39k
R9
39k
R14
510
C1
0.22
μF
R7
15k
R8
15k
REFERENCE
INPUT

TL/H/5704-28

Schematic Diagram**

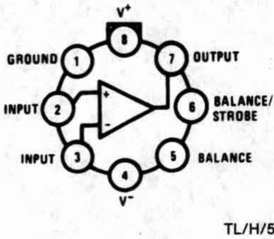

BALANCE/STROBE
6
BALANCE
5
R3
300
R4
300
R1
1.3k
R2
1.3k
Q6
R5
70
Q7
R8
750
Q10
R9
600
8
V+
Q20
Q11
Q12
Q5
R6
1.2k
R7
1.2k
Q8
Q19
Q13
Q3
Q9
R10
4k
Q18
2
+
Q1
INPUTS
D1
5V
D2
5V
R16
400
OUTPUT
7
Q14
3
−
Q2
Q4
R17
60
Q21
R11
130
R15
450
Q23
Q15
Q22
Q17
R12
600
R19
250
R18
200
R14
2k
Q16
R13
4
4
V−
1
GND

TL/H/5704-5

**Pin connections shown on schematic diagram are for H08 package.

Connection Diagrams*

Metal Can Package


V+
8
GROUND
1
OUTPUT
7
INPUT
2
+
−
6
BALANCE/
STROBE
INPUT
3
5
BALANCE
4
V−

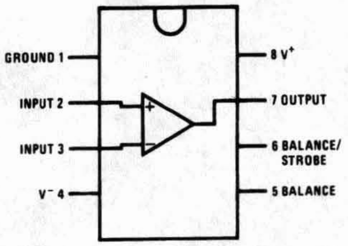
TL/H/5704-6

Top View

Note: Pin 4 connected to case

Order Number LM111H, LM111H/883*, LM211H or LM311H
See NS Package Number H08C

Dual-In-Line Package

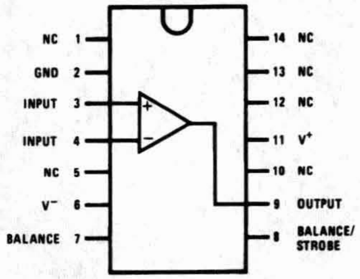

GROUND 1
8 V+
INPUT 2
+
7 OUTPUT
INPUT 3
−
6 BALANCE/
STROBE
V− 4
5 BALANCE

TL/H/5704-34

Top View

Order Number LM111J-8, LM111J-8/883*, LM211J-8, LM211M, LM311M or LM311N
See NS Package Number J08A, M08A or N08E

Dual-In-Line Package


NC 1
14 NC
GND 2
13 NC
INPUT 3
+
12 NC
INPUT 4
−
11 V+
NC 5
10 NC
V− 6
9 OUTPUT
BALANCE 7
8 BALANCE/
STROBE

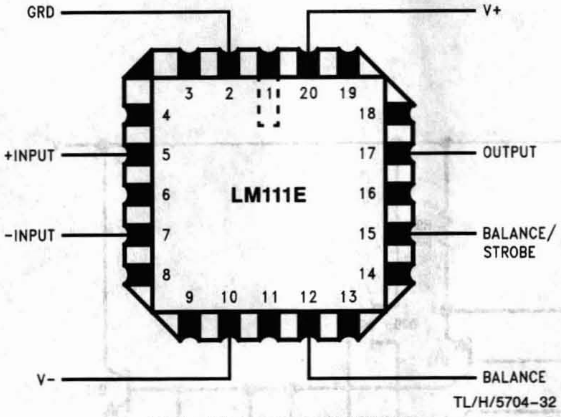
TL/H/5704-35

Top View

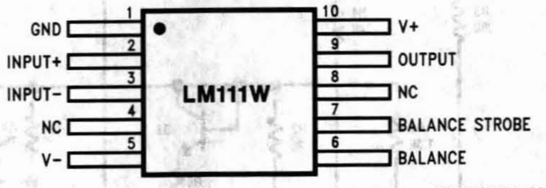
Order Number LM111J/883* or LM311N-14
See NS Package Number J14A or N14A

*Also available per JM38510/10304

Connection Diagrams (Continued)


GRD
V+
+INPUT
-INPUT
V-
OUTPUT
BALANCE/
STROBE
BALANCE
LM111E
3
2
1
20
19
4
18
5
17
6
16
7
15
8
14
9
10
11
12
13
TL/H/5704-32

Order Number LM111E/883
See NS Package Number E20A


GND
INPUT+
INPUT-
NC
V-
1
2
3
4
5
LM111W
10
9
8
7
6
V+
OUTPUT
NC
BALANCE STROBE
BALANCE
TL/H/5704-33

Order Number LM111W/883*
See NS Package Number W10A

*Also available per JM38510/10304

National Semiconductor

LM119/LM219/LM319
High Speed Dual Comparator

General Description

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

The LM319A offers improved precision over the standard LM319, with tighter tolerances on offset voltage, offset current, and voltage gain.

Features

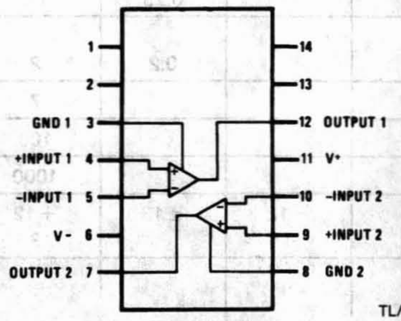
- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

The LM119 is specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319A and LM319 are specified from 0°C to +70°C.

Connection Diagrams

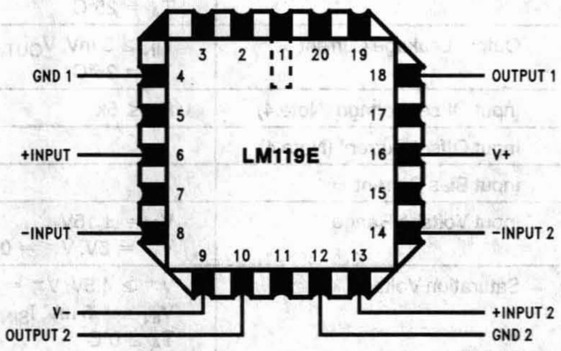
Dual-In-Line-Package


1
2
GND 1 3
+INPUT 1 4
−INPUT 1 5
V− 6
OUTPUT 2 7
14
13
12 OUTPUT 1
11 V+
10 −INPUT 2
9 +INPUT 2
8 GND 2

TL/H/5705-4

Top View

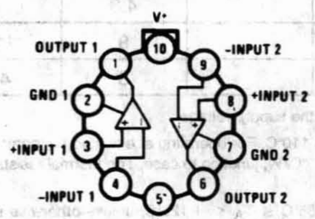
Order Number LM119J, LM119J/883*, LM219J, LM319J, LM319AM, LM319M, LM319AN or LM319N
See NS Package Number J14A, M14A or N14A


3 2 1 20 19
GND 1 4
18 OUTPUT 1
5
17
+INPUT 6
LM119E
16 V+
7
15
−INPUT 8
14 −INPUT 2
9 10 11 12 13
V−
OUTPUT 2
+INPUT 2
GND 2

TL/H/5705-8

Order Number LM119E/883
See NS Package Number E20A

Metal Can Package

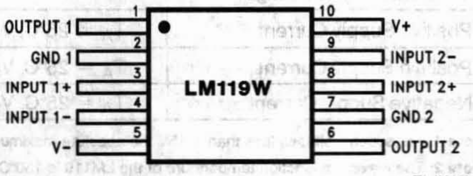

V+
10
OUTPUT 1 1
−INPUT 2 9
GND 1 2
+INPUT 2 8
+INPUT 1 3
GND 2 7
−INPUT 1 4
OUTPUT 2 6
5
V−

Case is connected to pin 5 (V⁻)

TL/H/5705-7

Top View

Order Number LM119H, LM119H/883*, or LM319H
See NS Package Number H10C


OUTPUT 1 1
GND 1 2
INPUT 1+ 3
INPUT 1− 4
V− 5
LM119W
10 V+
9 INPUT 2−
8 INPUT 2+
7 GND 2
6 OUTPUT 2

TL/H/5705-9

Order Number LM119W/883
See NS Package Number W10A

*Also available per SMD# 8601401 or JM38510/10306

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 1)	±15V
ESD rating (1.5 kΩ in series with 100 pF)	800V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Temperature Range

LM119	−55°C to 125°C
LM219	−25°C to 85°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM119/LM219			Units
		Min	Typ	Max	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \le 5k$		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		30	75	nA
Input Bias Current	$T_A = 25°C$		150	500	nA
Voltage Gain	$T_A = 25°C$ (Note 6)	10	40		V/mV
Response Time (Note 5)	$T_A = 25°C$, $V_S = \pm 15V$		80		ns
Saturation Voltage	$V_{IN} \le -5$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5	V
Output Leakage Current	$V_{IN} \ge 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	2	μA
Input Offset Voltage (Note 4)	$R_S \le 5k$			7	mV
Input Offset Current (Note 4)				100	nA
Input Bias Current				1000	nA
Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$	−12 1	±13	+12 3	V V
Saturation Voltage	$V^+ \ge 4.5V$, $V^- = 0$ $V_{IN} \le -6$ mV, $I_{SINK} \le 3.2$ mA $T_A \ge 0°C$ $T_A \le 0°C$		0.23	0.4 0.6	V V
Output Leakage Current	$V_{IN} \ge 5$ mV, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$		1	10	μA
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		8	11.5	mA
Negative Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		3	4.5	mA

Note 1: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM119 is 150°C, while that of the LM219 is 110°C. For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 19°C/W, junction to case. The thermal resistance of the J14 and N14 packages is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55°C \le T_A \le +125°C$, unless otherwise stated. With the LM219, however, all temperature specifications are limited to $-25°C \le T_A \le +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. Do not operate the device with more than 16V from ground to V_S.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: Output is pulled up to 15V through a 1.4 kΩ resistor.

Note 7: Refer to RETS119X for LM119H/883 and LM119J/883 specifications.

Absolute Maximum Ratings LM319A/319

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
ESD rating (1.5 kΩ in series with 100 pF)	800V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Temperature Range

LM319A, LM319	0°C to 70°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM319A			LM319			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \le 5k$		0.5	1.0		2.0	8.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		20	40		80	200	nA
Input Bias Current	$T_A = 25°C$		150	500		250	1000	nA
Voltage Gain	$T_A = 25°C$ (Note 6)	20	40		8	40		V/mV
Response Time (Note 5)	$T_A = 25°C$, $V_S = \pm 15V$		80			80		ns
Saturation Voltage	$V_{IN} \le -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5		0.75	1.5	V
Output Leakage Current	$V_{IN} \ge 10$ mV, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$, $T_A = 25°C$		0.2	10		0.2	10	μA
Input Offset Voltage (Note 4)	$R_S \le 5k$			10			10	mV
Input Offset Current (Note 4)				300			300	nA
Input Bias Current				1000			1200	nA
Input Voltage Range	$V_S = \pm 15V$		±13			±13		V
	$V^+ = 5V$, $V^- = 0$	1		3	1		3	V
Saturation Voltage	$V^+ \ge 4.5V$, $V^- = 0$ $V_{IN} \le -10$ mV, $I_{SINK} \le 3.2$ mA		0.3	0.4		0.3	0.4	V
Differential Input Voltage				±5			±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3			4.3		mA
Positive Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		8	12.5		8	12.5	mA
Negative Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		3	5		3	5	mA

Note 1: For supply voltages less than ±15 the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM319A and LM319 is 85°C. For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 19°C/W, junction to case. The thermal resistance of the N14 and J14 package is 100°C/W, junction to ambient. The thermal resistance of the M14 package is 115°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$, and $0°C \le T_A \le 70°C$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. Do not operate the device with more than 16V from ground to V_S.

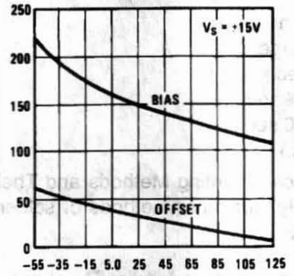
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

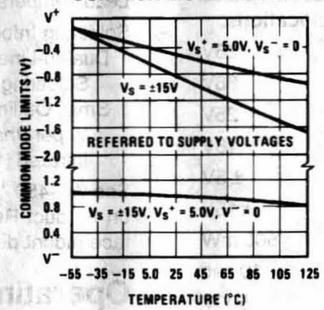
Note 6: Output is pulled up to 15V through a 1.4 kΩ resistor.

Typical Performance Characteristics LM119A/LM119/LM219

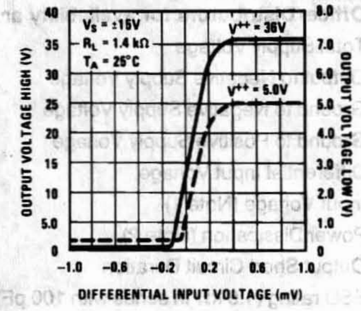
Input Currents



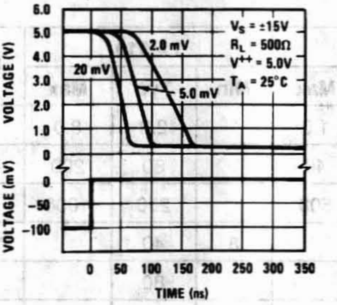
Common Mode Limits



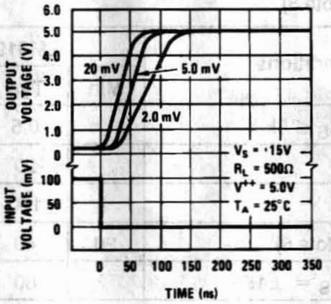
Transfer Function



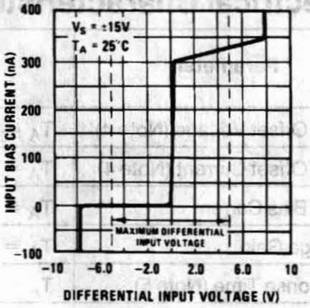
Response Time for Various Input Overdrives



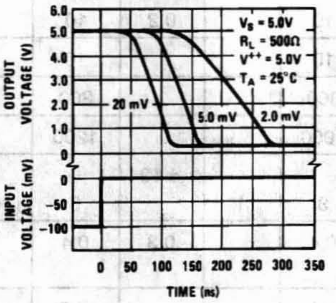
Response Time for Various Input Overdrives



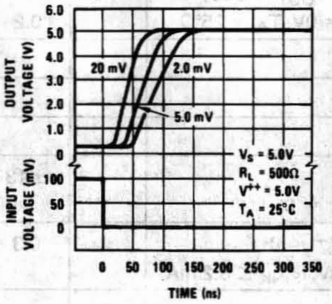
Input Characteristics



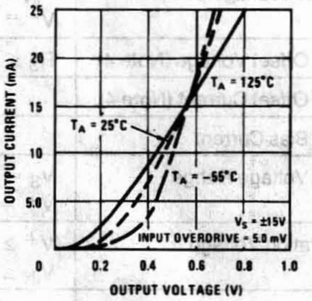
Response Time for Various Input Overdrives



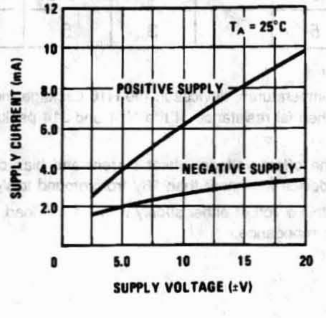
Response Time for Various Input Overdrives



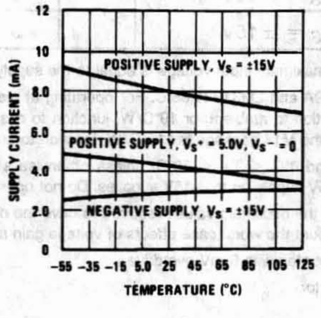
Output Saturation Voltage



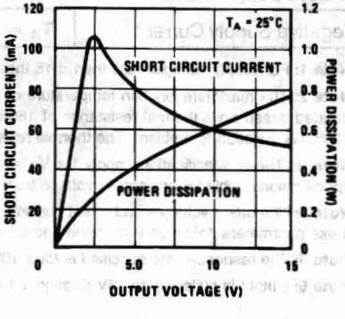
Supply Current



Supply Current



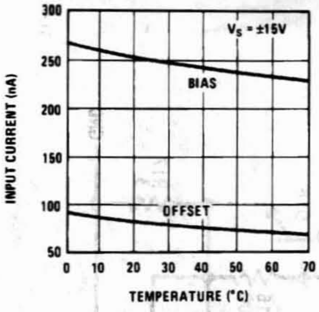
Output Limiting Characteristics



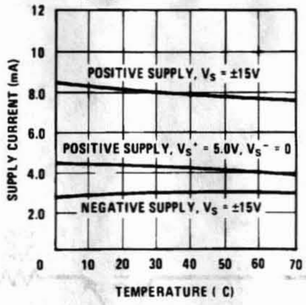
TL/H/5705–2

Typical Performance Characteristics LM319A, LM319

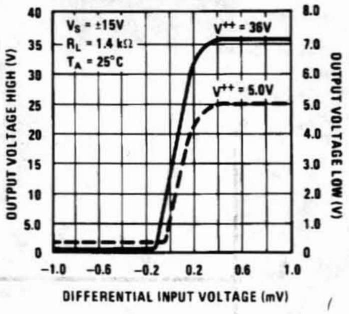
Input Currents



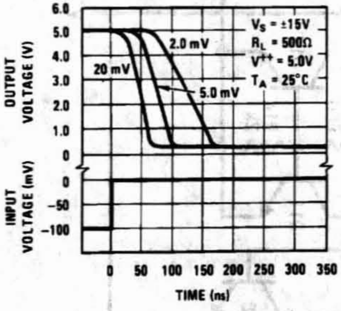
Supply Currents



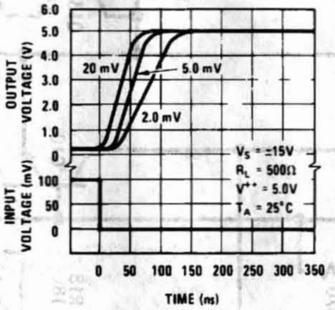
Transfer Function



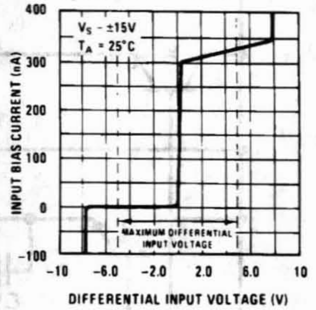
Response Time for Various Input Overdrives



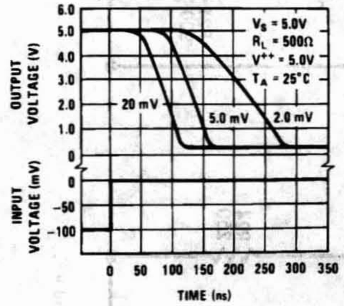
Response Time for Various Input Overdrives



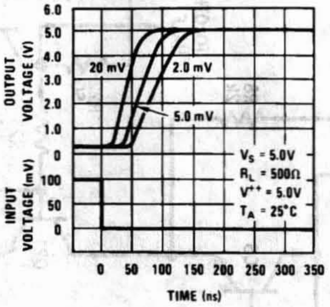
Input Characteristics



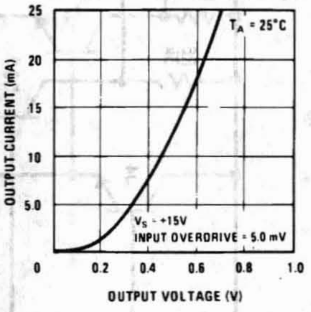
Response Time for Various Input Overdrives



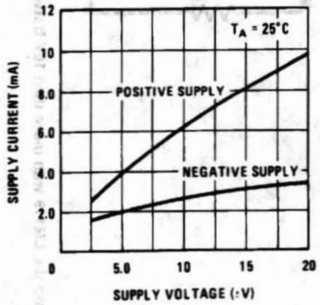
Response Time for Various Input Overdrives



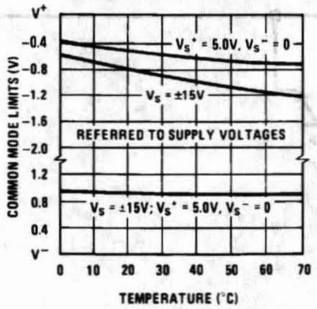
Output Saturation Voltage



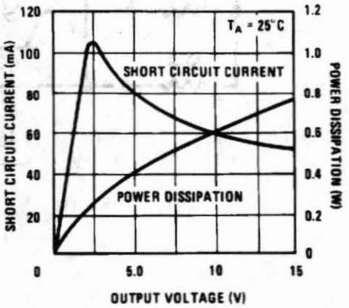
Supply Current



Common Mode Limits



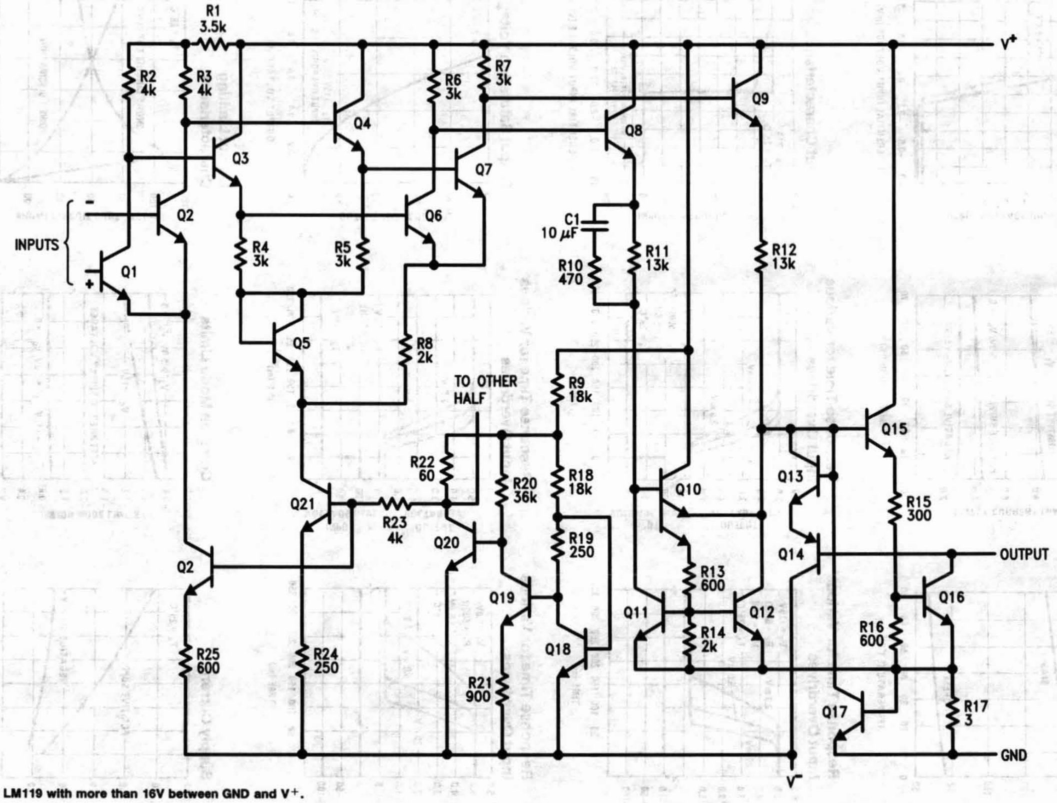
Output Limiting Characteristics



TL/H/5705–3

3

Schematic Diagram

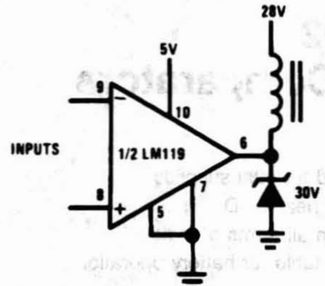

R1
3.5k
V+
R2
4k
R3
4k
R6
3k
R7
3k
Q9
Q4
Q8
Q3
Q7
INPUTS
-
+
Q2
Q6
Q1
C1
10 μF
R4
3k
R5
3k
R10
470
R11
13k
R12
13k
Q5
R8
2k
TO OTHER HALF
R9
18k
Q15
R22
60
R18
18k
Q13
Q10
Q21
R20
36k
R15
300
R23
4k
Q20
R19
250
Q14
OUTPUT
Q2
R13
600
Q19
Q16
Q11
Q12
R14
2k
Q18
R16
600
R25
600
R24
250
R21
900
Q17
R17
3
GND
V-

*Do not operate the LM119 with more than 16V between GND and V+.

TL/H/5705–1

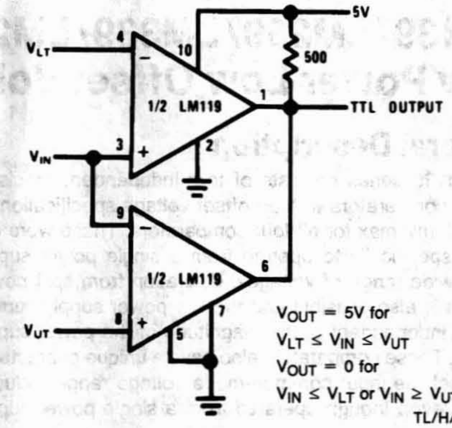
Typical Applications*

Relay Driver


28V
5V
9
10
INPUTS
1/2 LM119
6
7
30V
8
5

TL/H/5705-5

Window Detector


5V
V_{LT}
4
10
500
1/2 LM119
1
TTL OUTPUT
V_{IN}
3
2
9
1/2 LM119
6
V_{UT}
8
5
7

$V_{OUT} = 5V$ for

$V_{LT} \leq V_{IN} \leq V_{UT}$

$V_{OUT} = 0$ for

$V_{IN} \leq V_{LT}$ or $V_{IN} \geq V_{UT}$

TL/H/5705-6

*Pin numbers are for metal can package.

National Semiconductor

LM139/LM239/LM339/LM2901/LM3302
Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

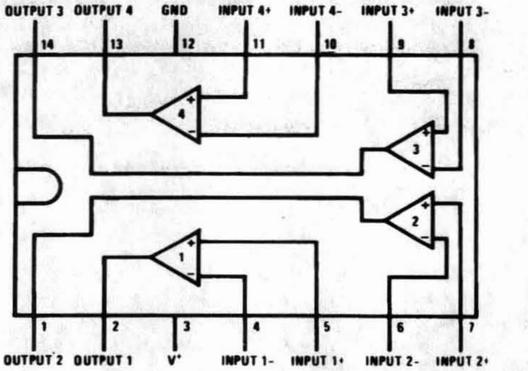
- Wide supply voltage range

LM139 series,	2 V_{DC} to 36 V_{DC} or ±1 V_{DC} to ±18 V_{DC}
LM139A series, LM2901	2 V_{DC} to 28 V_{DC}
LM3302	or ±1 V_{DC} to ±14 V_{DC}

- Very low supply current drain (0.8 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ±5 nA and offset voltage ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Connection Diagrams

Dual-In-Line Package


OUTPUT 3
OUTPUT 4
GND
INPUT 4+
INPUT 4−
INPUT 3+
INPUT 3−
14
13
12
11
10
9
8
4
3
2
1
1
2
3
4
5
6
7
OUTPUT 2
OUTPUT 1
V+
INPUT 1−
INPUT 1+
INPUT 2−
INPUT 2+

TOP VIEW

TL/H/5706–2

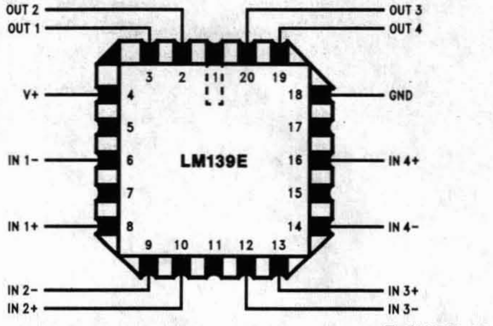
Order Number LM139J, LM139J/883*, LM139AJ, LM139AJ/883, LM239J, LM239AJ, LM339J, See NS Package Number J14A**

Order Number LM339AM, LM339M or LM2901M See NS Package Number M14A

Order Number LM339N, LM339AN, LM2901N or LM3302N See NS Package Number N14A

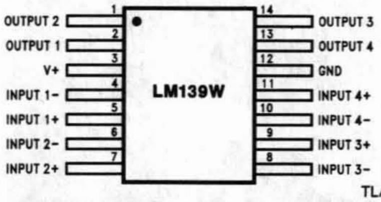
*Available per JM38510/11201

**Available per SMD# 5962-8873901


OUT 2
OUT 1
OUT 3
OUT 4
V+
GND
IN 1−
IN 4+
IN 1+
IN 4−
IN 2−
IN 2+
IN 3+
IN 3−
LM139E
3
2
1
20
19
4
18
5
17
6
16
7
15
8
14
9
10
11
12
13

TL/H/5706–26

Order Number LM139AE/883 or LM139E/883 See NS Package Number E20A


OUTPUT 2
OUTPUT 1
V+
INPUT 1−
INPUT 1+
INPUT 2−
INPUT 2+
OUTPUT 3
OUTPUT 4
GND
INPUT 4+
INPUT 4−
INPUT 3+
INPUT 3−
LM139W
1
2
3
4
5
6
7
14
13
12
11
10
9
8

TL/H/5706–27

Order Number LM139AW/883 or LM139W/883* See NS Package Number W14B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 10)

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}	28 V_{DC}
Input Voltage	-0.3 V_{DC} to $+36$ V_{DC}	-0.3 V_{DC} to $+28$ V_{DC}
Input Current ($V_{IN} < -0.3$ V_{DC}), (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1050 mW	1050 mW
Cavity DIP	1190 mW	
Small Outline Package	760 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Storage Temperature Range	-65°C to $+150$°C	-65°C to $+150$°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Operating Temperature Range		-40°C to $+85$°C
LM339/LM339A	0°C to $+70$°C	
LM239/LM239A	-25°C to $+85$°C	
LM2901	-40°C to $+85$°C	
LM139/LM139A	-55°C to $+125$°C	
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
ESD rating (1.5 kΩ in series with 100 pF)	600V	600V

Electrical Characteristics ($V^+ = 5$ V_{DC}, $T_A = 25$°C, unless otherwise stated)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		1.0	2.0		1.0	2.0		2.0	5.0		2.0	5.0		2.0	7.0		3	20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), $V_{CM} = 0V$		25	100		25	250		25	100		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$		3.0	25		5.0	50		3.0	25		5.0	50		5	50		3	100	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30$ V_{DC} (LM3302, $V^+ = 28$ V_{DC}) (Note 6)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators,		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
	$R_L = \infty$, $V^+ = 36V$, (LM3302, $V^+ = 28$ V_{DC})					1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5	mA_{DC}
Voltage Gain	$R_L \geq 15$ kΩ, $V^+ = 15$ V_{DC} $V_o = 1$ V_{DC} to 11 V_{DC}	50	200		50	200		50	200		50	200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4$ V_{DC}, $V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ,		300			300			300			300			300			300		ns
Response Time	$V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} = 1$ V_{DC}, $V_{IN(+)} = 0$, $V_O \leq 1.5$ V_{DC}	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}

Electrical Characteristics (V+ = 5 V

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Saturation Voltage	$V_{IN(-)}=1\ V_{DC}$, $V_{IN(+)}=0$, $I_{SINK}\leq 4$ mA		250	400		250	400		250	400		250	400		250	400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)}=1\ V_{DC}$, $V_{IN(-)}=0$, $V_O=5\ V_{DC}$		0.1			0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics ($V^+ = 5.0\ V_{DC}$, Note 4)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			4.0			4.0			9.0			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)}-I_{IN(-)}$, $V_{CM}=0V$			100			150			100			150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $V_{CM}=0V$ (Note 5)			300			400			300			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range	$V^+=30\ V_{DC}$ (LM3302, $V^+=28\ V_{DC}$) (Note 6)	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$			$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)}=1\ V_{DC}$, $V_{IN(+)}=0$, $I_{SINK}\leq 4$ mA			700			700			700			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)}=1\ V_{DC}$, $V_{IN(-)}=0$, $V_O=30\ V_{DC}$, (LM3302, $V_O=28\ V_{DC}$)			1.0			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			36			36			36			36			36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°)C.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to $+30\ V_{DC}$ without damage (25V for LM3302), independent of the magnitude of V^+.

Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

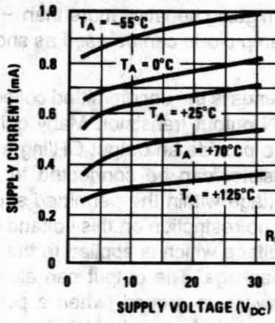
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$), at 25°C. For LM3302, V^+ from $5\ V_{DC}$ to $28\ V_{DC}$.

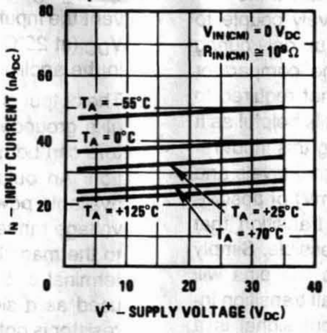
Note 10: Refer to RETS139AX for LM139A military specifications and to RETS139X for LM139 military specifications.

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

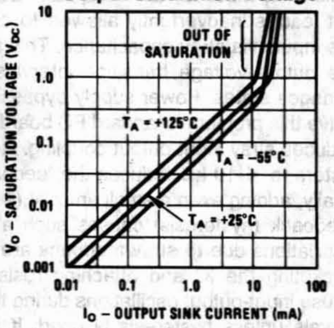
Supply Current



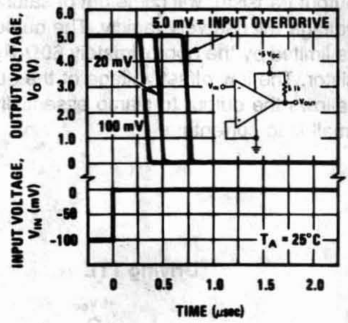
Input Current



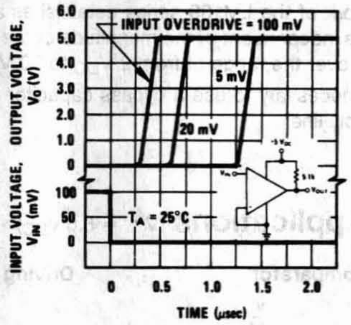
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



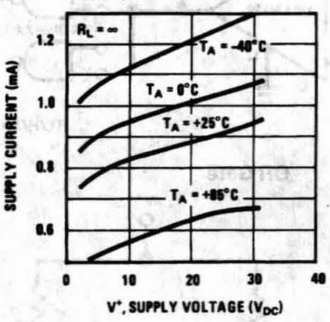
Response Time for Various Input Overdrives—Positive Transition



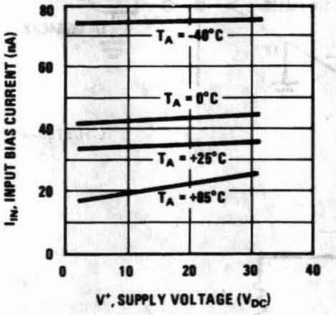
TL/H/5706-6

Typical Performance Characteristics LM2901

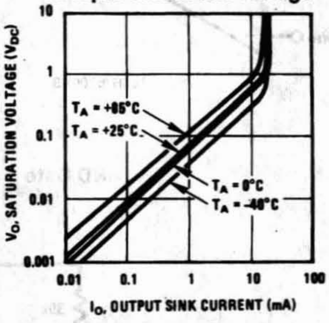
Supply Current



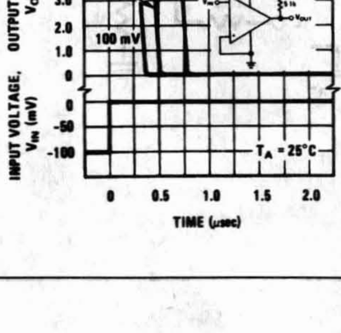
Input Current



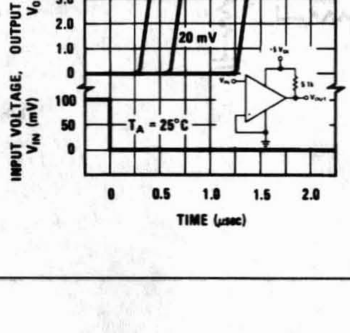
Output Saturation Voltage



Response Time for Various Input Overdrives-Negative Transition



Response Time for Various Input Overdrives-Positive Transition



TL/H/5706-7

Application Hints

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

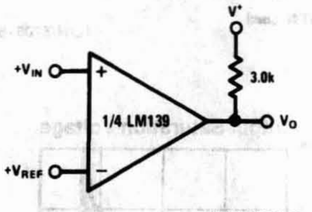
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

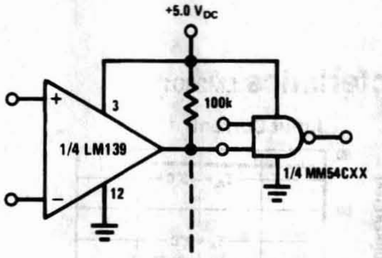
Typical Applications ($V^+ = 5.0\ V_{DC}$)

Basic Comparator



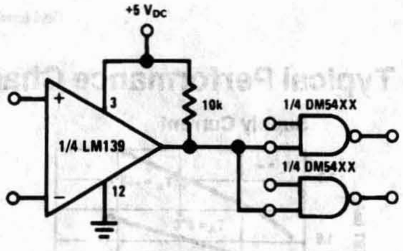
TL/H/5706-3

Driving CMOS



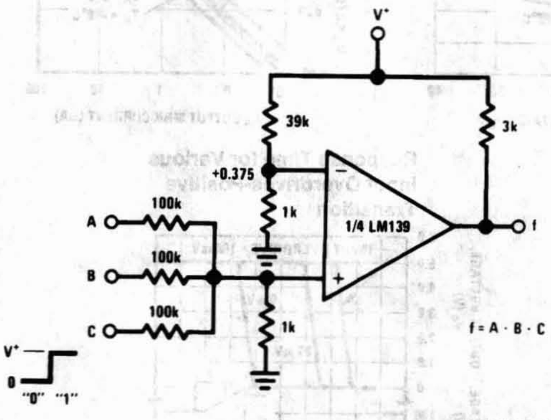
TL/H/5706-4

Driving TTL



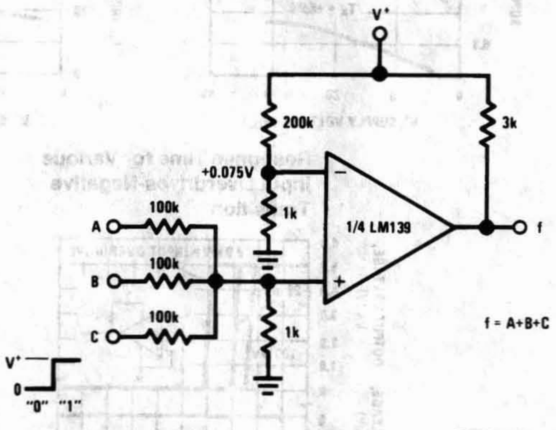
TL/H/5706-5

AND Gate



TL/H/5706-8

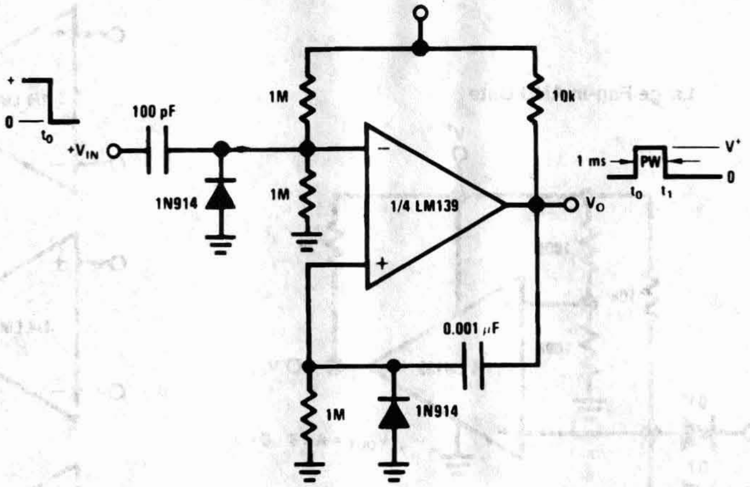
OR Gate



TL/H/5706-9

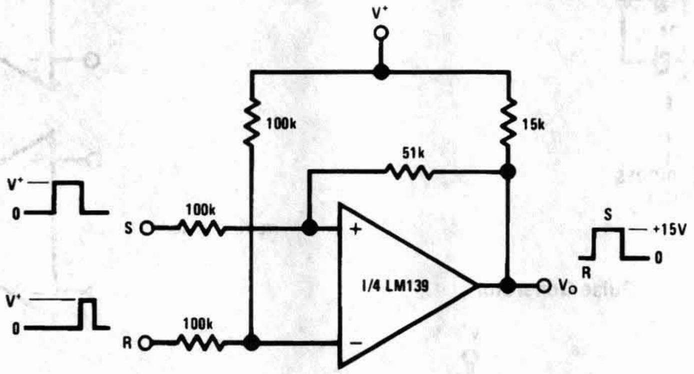
Typical Applications (V+ = 15 V_{DC}) (Continued)

One-Shot Multivibrator


V+
1M
10k
100 pF
+
0
t_0
+V_{IN}
1N914
1M
−
+
1/4 LM139
V_O
1 ms
PW
V+
0
t_0
t_1
0.001 μF
1M
1N914

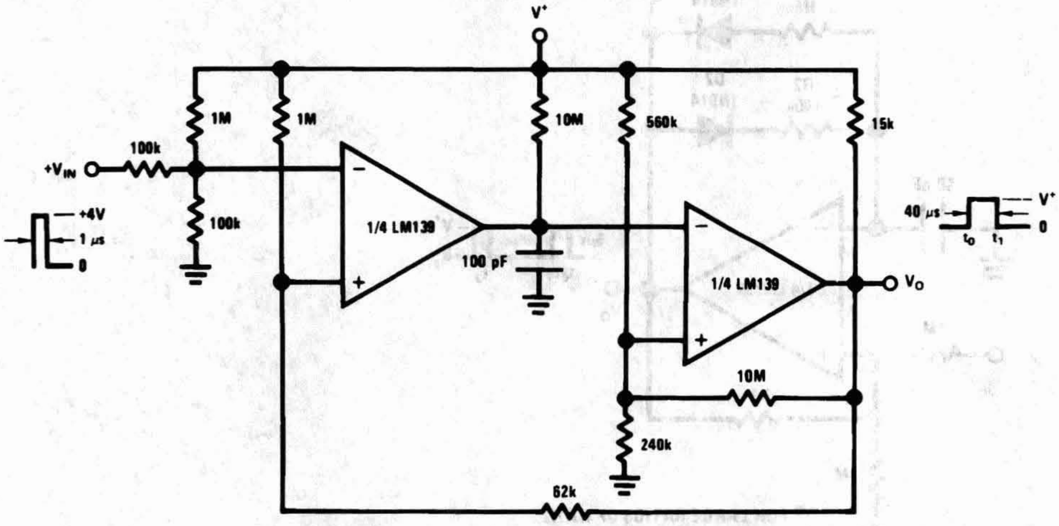
TL/H/5706–10

Bi-Stable Multivibrator


V+
100k
15k
51k
V+
0
100k
S
+
1/4 LM139
−
V_O
S
+15V
0
R
V+
0
100k
R

TL/H/5706–11

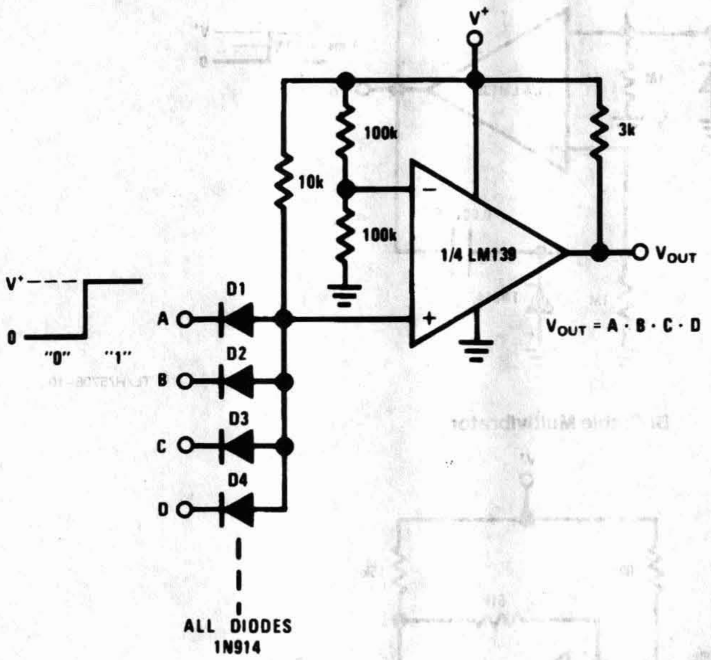
One-Shot Multivibrator with Input Lock Out


V+
1M
1M
10M
560k
15k
100k
+V_{IN}
100k
+4V
1 μs
0
−
+
1/4 LM139
100 pF
−
+
1/4 LM139
V_O
40 μs
V+
0
t_0
t_1
10M
240k
62k

TL/H/5706–12

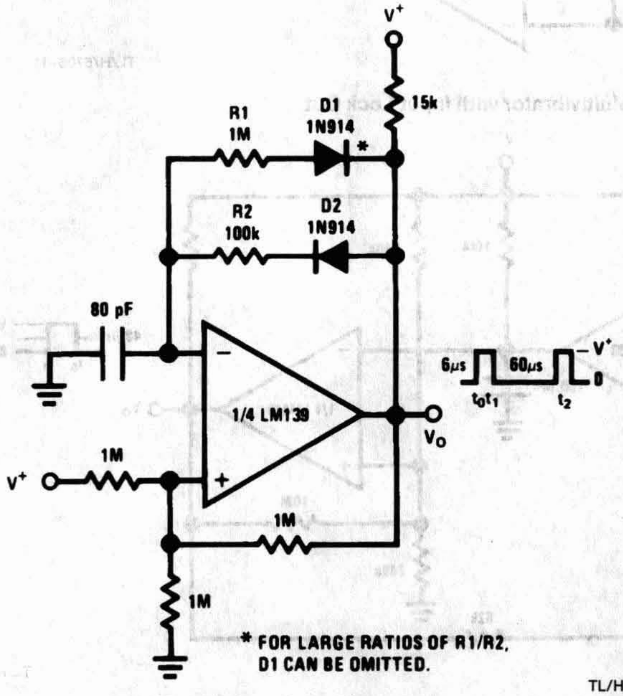
Typical Applications (V+ = 15 V_{DC}) (Continued)

Large Fan-In AND Gate


V+
100k
10k
100k
3k
1/4 LM139
VOUT
V+
0
"0"
"1"
D1
A
D2
B
D3
C
D4
D
VOUT = A · B · C · D
ALL DIODES
1N914

TL/H/5706–13

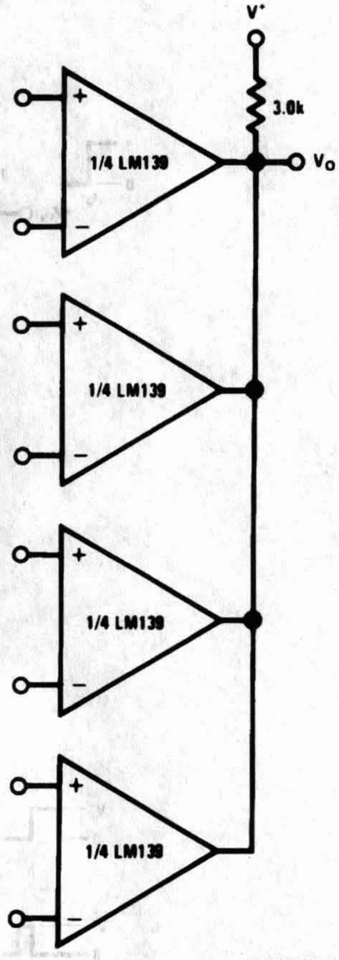
Pulse Generator


V+
15k
R1
1M
D1
1N914
*
R2
100k
D2
1N914
80 pF
1/4 LM139
VO
6μs
60μs
V+
0
t0
t1
t2
1M
V+
1M
1M

* FOR LARGE RATIOS OF R1/R2, D1 CAN BE OMITTED.

TL/H/5706–17

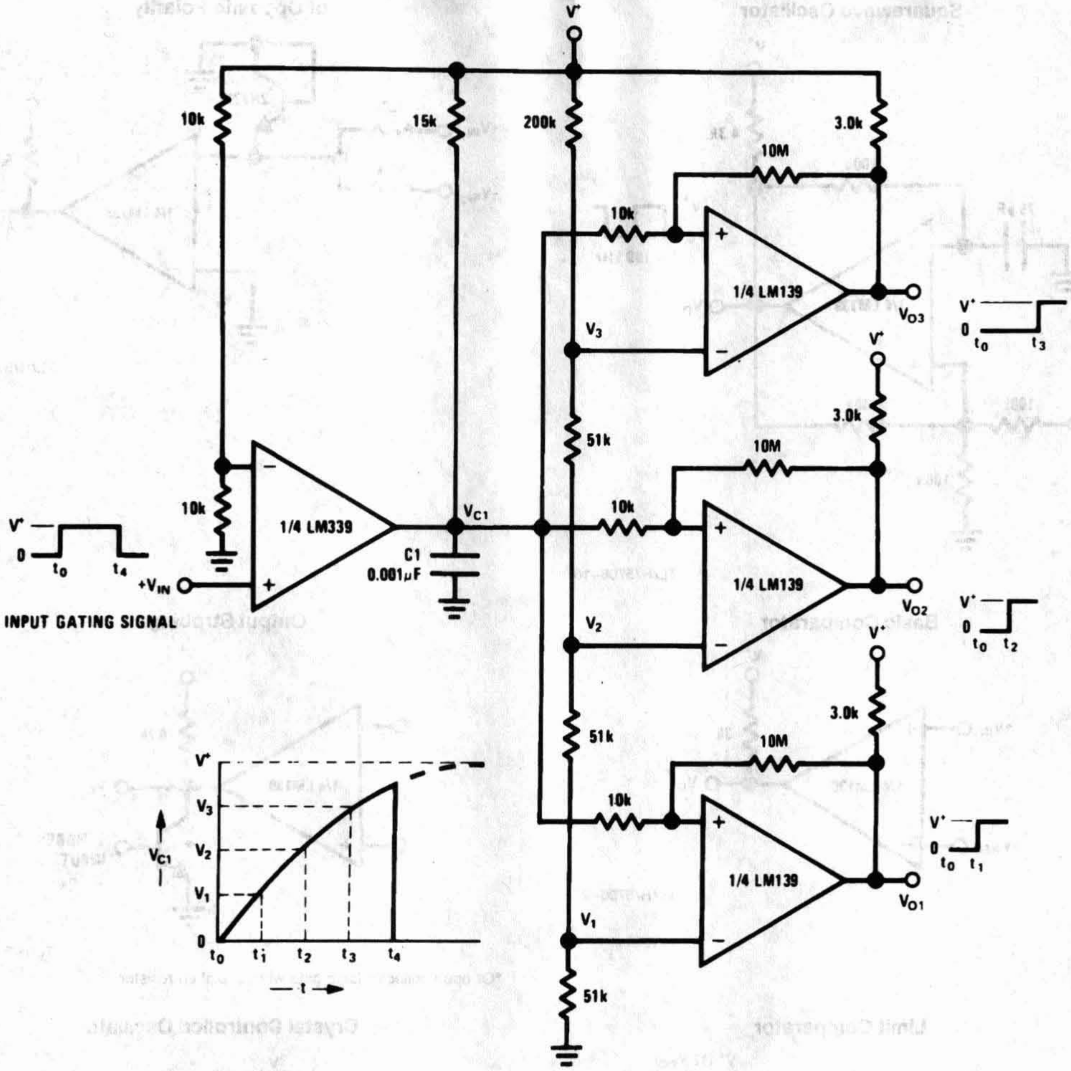
ORing the Outputs


V+
3.0k
VO
1/4 LM139
1/4 LM139
1/4 LM139
1/4 LM139

TL/H/5706–15

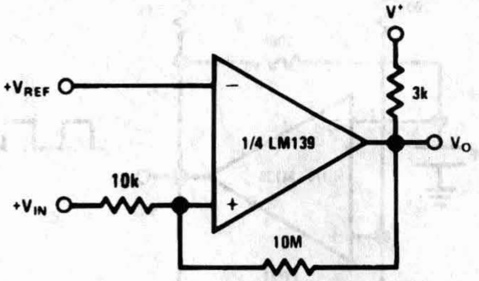
Typical Applications (V+ = 15 V_{DC}) (Continued)

Time Delay Generator


V+
10k
15k
200k
3.0k
10M
10k
+
−
1/4 LM139
V_{O3}
V+
0
t_0
t_3
V_3
51k
3.0k
10M
10k
1/4 LM139
V_{O2}
t_0
t_2
V_2
51k
3.0k
10M
10k
1/4 LM139
V_{O1}
t_0
t_1
V_1
51k
10k
1/4 LM339
V_{C1}
C1
0.001μF
10k
+V_{IN}
t_0
t_4
INPUT GATING SIGNAL
V+
V_3
V_2
V_1
0
V_{C1}
t_0
t_1
t_2
t_3
t_4
t

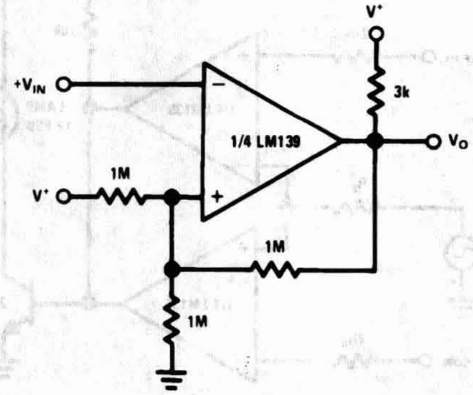
TL/H/5706-14

Non-Inverting Comparator with Hysteresis


V+
3k
+V_{REF}
−
+
1/4 LM139
V_O
10k
+V_{IN}
10M

TL/H/5706-18

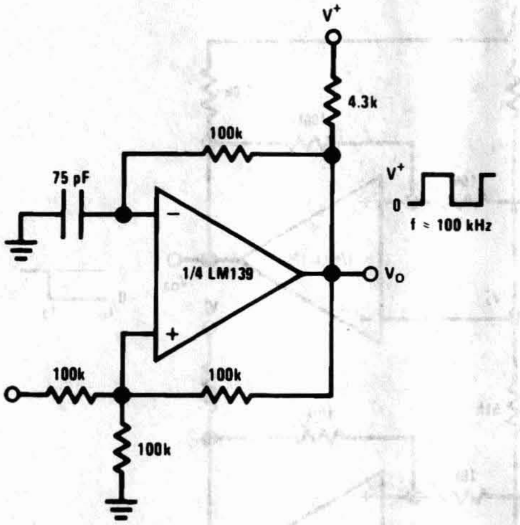
Inverting Comparator with Hysteresis


V+
3k
+V_{IN}
−
+
1/4 LM139
V_O
1M
V+
1M
1M

TL/H/5706-19

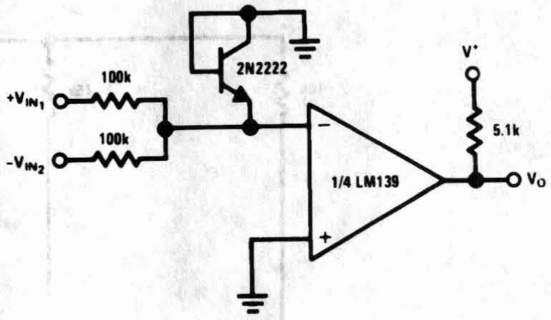
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Squarewave Oscillator


V+
4.3k
100k
75 pF
V+
0
f ≈ 100 kHz
1/4 LM139
VO
V+
100k
100k
100k

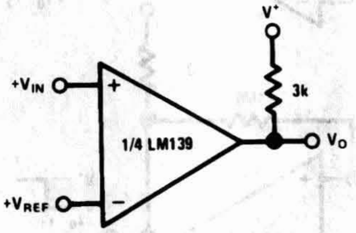
TL/H/5706-16

Comparing Input Voltages of Opposite Polarity


2N2222
+VIN1
100k
100k
-VIN2
V+
5.1k
1/4 LM139
VO

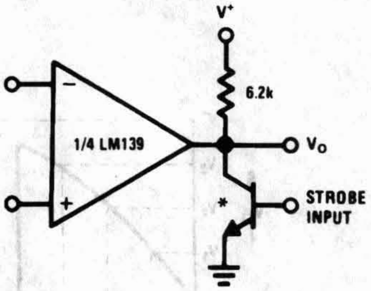
TL/H/5706-20

Basic Comparator


V+
+VIN
3k
1/4 LM139
VO
+VREF

TL/H/5706-21

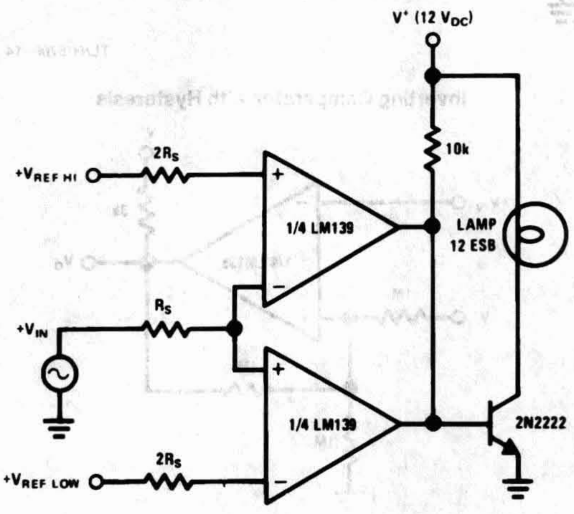
Output Strobing


V+
6.2k
1/4 LM139
VO
*
STROBE INPUT

TL/H/5706-22

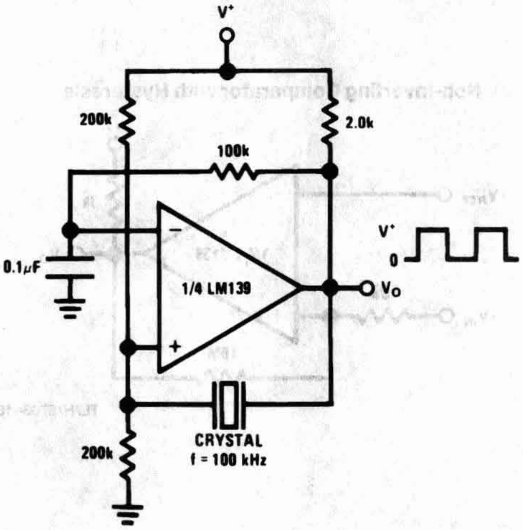
*Or open-collector logic gate without pull-up resistor

Limit Comparator


V+ (12 VDC)
10k
+VREF HI
2RS
1/4 LM139
LAMP 12 ESB
RS
+VIN
1/4 LM139
2N2222
2RS
+VREF LOW

TL/H/5706-24

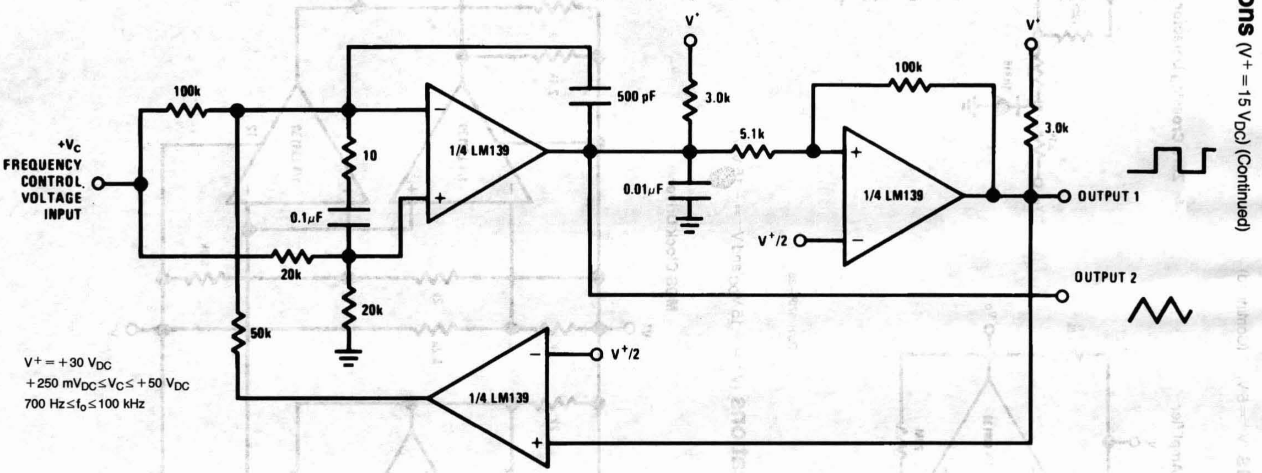
Crystal Controlled Oscillator


V+
200k
2.0k
100k
V+
0
0.1μF
1/4 LM139
VO
CRYSTAL
f = 100 kHz
200k

TL/H/5706-25

Typical Applications (V+ = 15 V_{DC}) (Continued)

Two-Decade High-Frequency VCO


+V_C
FREQUENCY
CONTROL
VOLTAGE
INPUT
100k
10
0.1μF
20k
20k
50k
1/4 LM139
1/4 LM139
1/4 LM139
500 pF
V+
3.0k
0.01μF
5.1k
100k
V+/2
V+
3.0k
OUTPUT 1
OUTPUT 2
V+/2

$V^+ = +30\ V_{DC}$

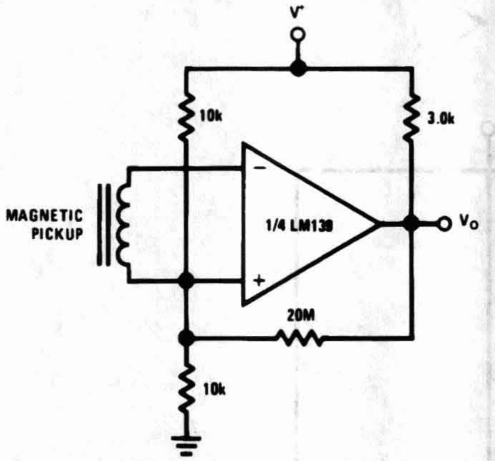
$+250\ mV_{DC} \le V_C \le +50\ V_{DC}$

$700\ Hz \le f_o \le 100\ kHz$

TL/H/5706–23

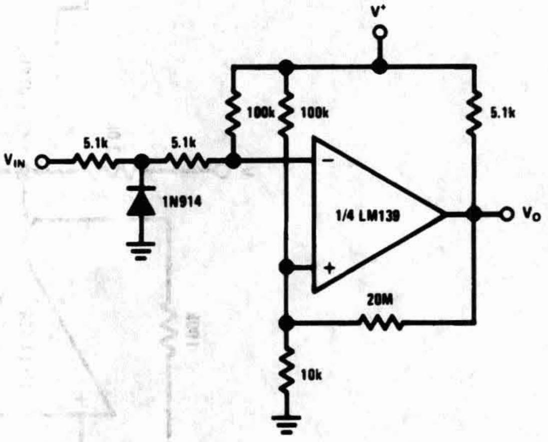
Typical Applications (V+ = 5 V_{DC}) (Continued)

Transducer Amplifier


V+
10k
3.0k
MAGNETIC PICKUP
1/4 LM139
V_O
20M
10k

TL/H/5706–28

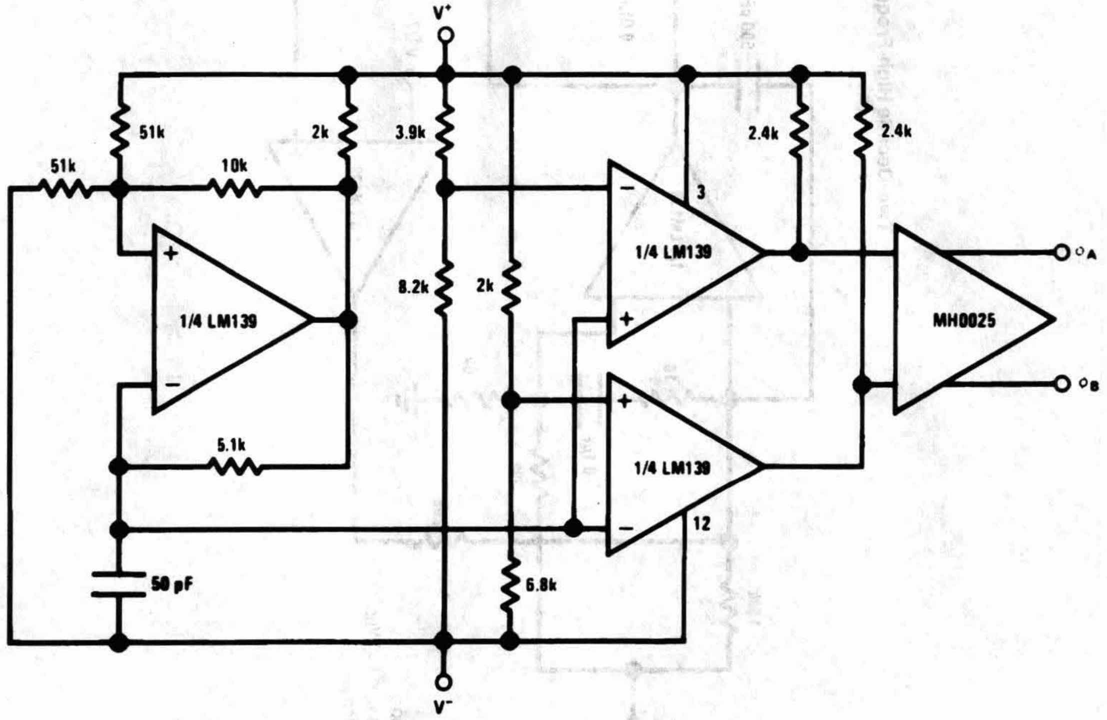
Zero Crossing Detector (Single Power Supply)


V+
100k
100k
5.1k
V_{IN}
5.1k
5.1k
1N914
1/4 LM139
V_O
20M
10k

TL/H/5706–30

Split-Supply Applications (V+ = +15 V_{DC} and V− = −15 V_{DC})

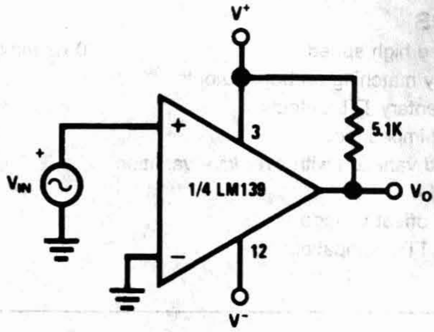
MOS Clock Driver


V+
51k
2k
3.9k
2.4k
2.4k
51k
10k
3
1/4 LM139
8.2k
2k
1/4 LM139
MH0025
ϕ_A
ϕ_B
5.1k
1/4 LM139
12
50 pF
6.8k
V−

TL/H/5706–31

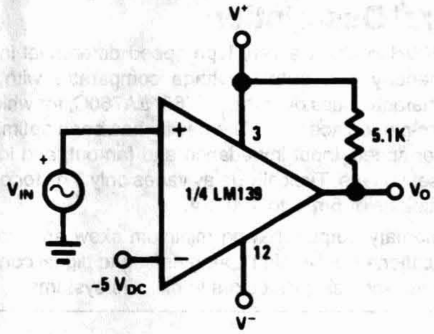
Split-Supply Applications (V+ = +15 V_{DC} and V− = −15 V_{DC}) (Continued)

Zero Crossing Detector


V+
+
3
5.1K
V_{IN}
1/4 LM139
V_O
−
12
V−

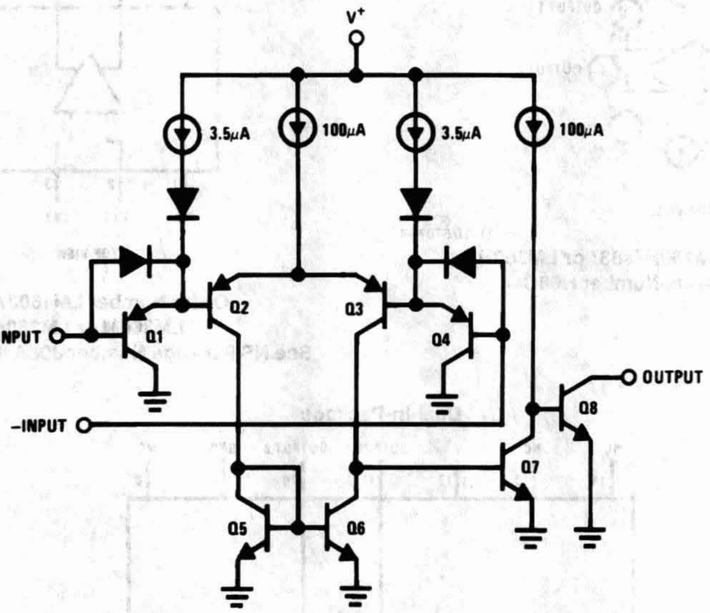
TL/H/5706–32

Comparator With a Negative Reference


V+
+
3
5.1K
V_{IN}
1/4 LM139
V_O
−5 V_{DC}
−
12
V−

TL/H/5706–33

Schematic Diagram


V+
3.5μA
100μA
3.5μA
100μA
Q2
Q3
+INPUT
Q1
Q4
OUTPUT
Q8
−INPUT
Q7
Q5
Q6

TL/H/5706–1

National Semiconductor

LM160/LM360 High Speed Differential Comparator

General Description

The LM160/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 400 mV.

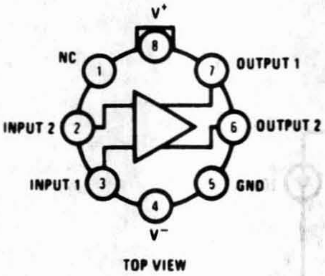
Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disk file systems.

Features

- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

Connection Diagrams

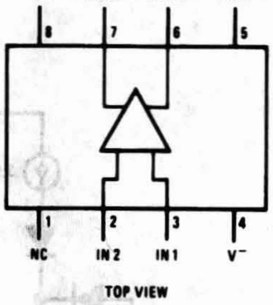
Metal Can Package


V+
8
NC
1
OUTPUT 1
7
INPUT 2
2
OUTPUT 2
6
INPUT 1
3
GND
5
4
V−
TOP VIEW

TL/H/5707–4

Order Number LM160H/883* or LM360H
See NS Package Number H08C

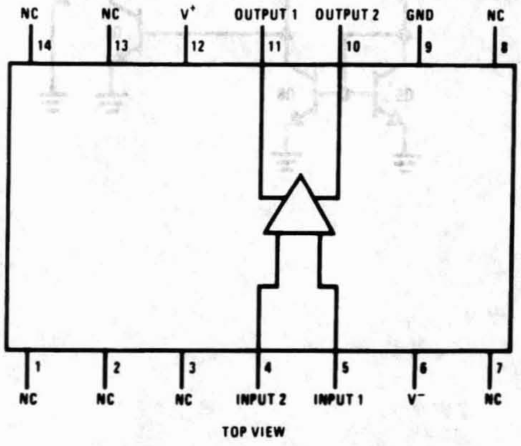
Dual-In-Line Package


V+
OUT 1
OUT 2
GND
8
7
6
5
1
2
3
4
NC
IN 2
IN 1
V−
TOP VIEW

TL/H/5707–5

Order Number LM160J/883*,
LM360M or LM360N
See NS Package Number J08A, M08A or N08E

Dual-In-Package


NC
14
NC
13
V+
12
OUTPUT 1
11
OUTPUT 2
10
GND
9
NC
8
1
NC
2
NC
3
NC
4
INPUT 2
5
INPUT 1
6
V−
7
NC
TOP VIEW

TL/H/5707–6

Order Number LM160J-14/883*
See NS Package Number J14A

*Also available in SMD# 5962-8767401

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 7)

Positive Supply Voltage	+8V
Negative Supply Voltage	−8V
Peak Output Current	20 mA
Differential Input Voltage	±5V
Input Voltage	$V^+ \geq V_{IN} \geq V^-$
ESD Tolerance (Note 8)	1600V
Operating Temperature Range	
LM160	−55°C to +125°C
LM360	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

Parameter	Conditions	Min	Typ	Max	Units
Operating Conditions Supply Voltage V_{CC}^+ Supply Voltage V_{CC}^-		 4.5 −4.5	 5 −5	 6.5 −6.5	 V V
Input Offset Voltage	$R_S \leq 200\Omega$		2	5	mV
Input Offset Current			0.5	3	μA
Input Bias Current			5	20	μA
Output Resistance (Either Output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	$T_A = 25°C$, $V_S = \pm 5V$ (Notes 1, 6) $T_A = 25°C$, $V_S = \pm 5V$ (Notes 2, 6) $T_A = 25°C$, $V_S = \pm 5V$ (Notes 3, 6)		13 12 14	25 20 	ns ns ns
Response Time Difference between Outputs (t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$) (t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$) (t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$) (t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	 $T_A = 25°C$ (Notes 1, 6) $T_A = 25°C$ (Notes 1, 6) $T_A = 25°C$ (Notes 1, 6) $T_A = 25°C$ (Notes 1, 6)		 2 2 2 2		 ns ns ns ns
Input Resistance	f = 1 MHz		17		kΩ
Input Capacitance	f = 1 MHz		3		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		8		μV/°C
Average Temperature Coefficient of Input Offset Current			7		nA/°C
Common Mode Input Voltage Range	$V_S = \pm 6.5V$	±4	±4.5		V
Differential Input Voltage Range		±5			V
Output High Voltage (Either Output)	$I_{OUT} = -320\ \mu A$, $V_S = \pm 4.5V$	2.4	3		V
Output Low Voltage (Either Output)	$I_{SINK} = 6.4$ mA		0.25	0.4	V
Positive Supply Current	$V_S = \pm 6.5V$		18	32	mA
Negative Supply Current	$V_S = \pm 6.5V$		−9	−16	mA

Note 1: Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.

Note 2: Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.

Note 3: Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

Note 4: Typical thermal impedances are as follows:

Cavity DIP (J):	θ_{jA}	135°C/W	Header (H)	θ_{jA}	165°C/W	(Still Air)
Molded DIP (N):	θ_{jA}	130°C/W			67°C/W	(400 LF/min Air Flow)
				θ_{jC}	25°C/W	

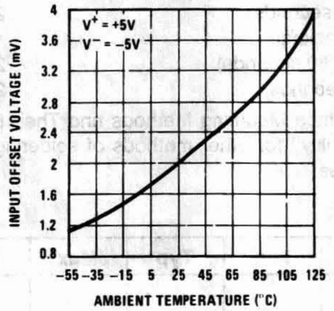
Note 5: The device may be damaged if used beyond the maximum ratings.

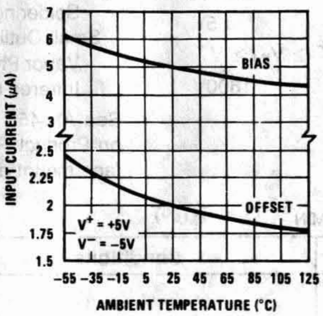
Note 6: Measurements are made in AC Test Circuit, Fanout = 1

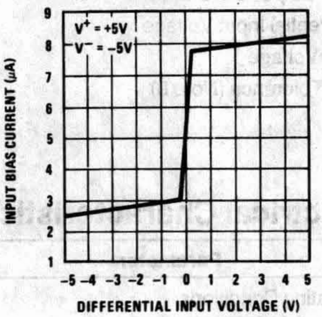
Note 7: Refer to RETS 160X for LM160H, LM160J-14 and LM160J military specifications.

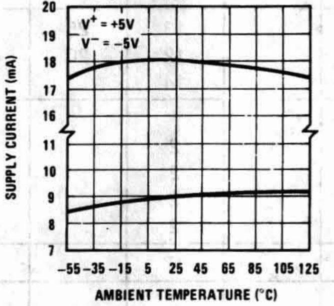
Note 8: Human body model, 1.5 kΩ in series with 100 pF.

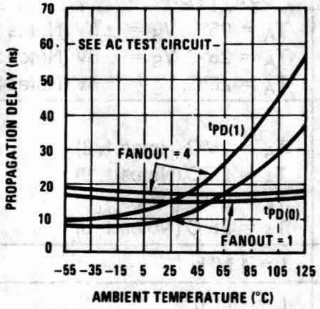
Typical Performance Characteristics

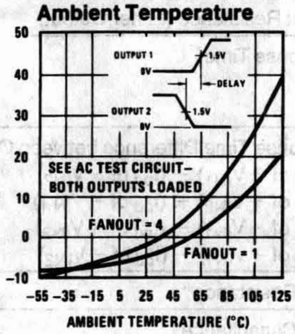

Offset Voltage

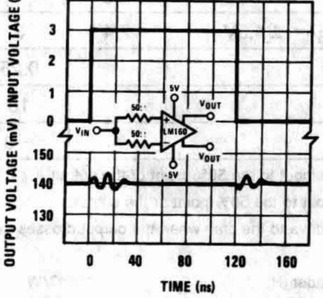

Input Currents vs Ambient Temperature


Input Characteristics


Supply Current vs Ambient Temperature

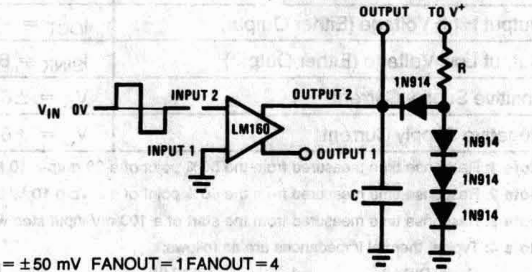

Propagation Delay vs Ambient Temperature


Delay of Output 1 With Respect to Output 2 vs Ambient Temperature


Common-Mode Pulse Response

TL/H/5707–2

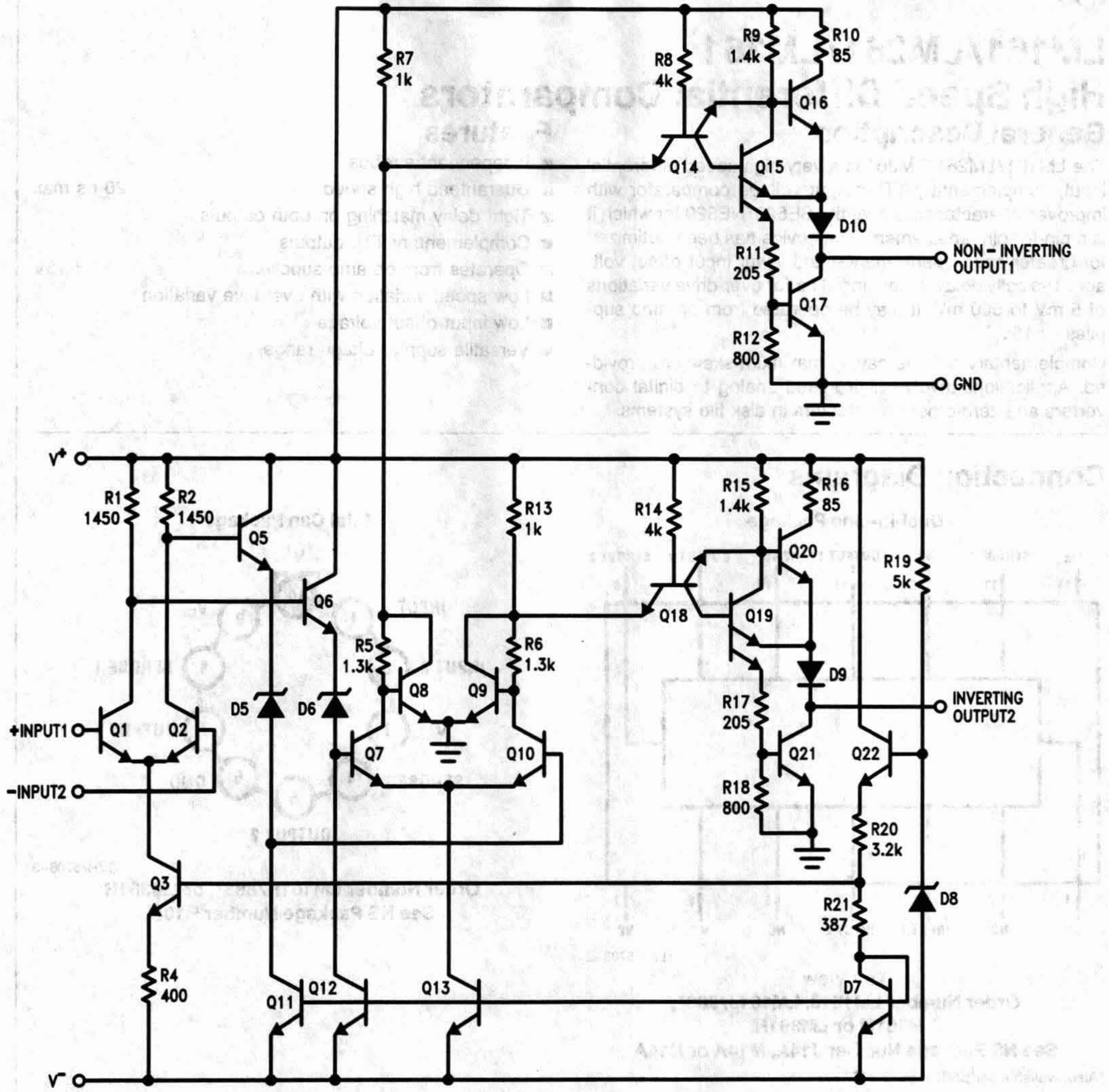
AC Test Circuit


OUTPUT
TO V+
R
1N914
OUTPUT 2
INPUT 2
VIN
0V
LM160
INPUT 1
OUTPUT 1
C
1N914
1N914
1N914

VIN = ±50 mV	FANOUT = 1	FANOUT = 4
V+ = +5V	R = 2.4k	R = 630Ω
V− = −5V	C = 15 pF	C = 30 pF

TL/H/5707–3

Schematic Diagram


R7
1k
R8
4k
R9
1.4k
R10
85
Q14
Q15
Q16
D10
R11
205
NON – INVERTING
OUTPUT1
Q17
R12
800
GND
V+
R1
1450
R2
1450
Q5
Q6
R13
1k
R14
4k
R15
1.4k
R16
85
Q20
R19
5k
Q18
Q19
R5
1.3k
R6
1.3k
Q8
Q9
D9
INVERTING
OUTPUT2
D5
D6
R17
205
+INPUT1
Q1
Q2
Q7
Q10
Q21
Q22
–INPUT2
R18
800
R20
3.2k
Q3
R21
387
D8
R4
400
D7
Q11
Q12
Q13
V−

TL/H/5707-1

National Semiconductor

LM161/LM261/LM361
High Speed Differential Comparators

General Description

The LM161/LM261/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (±15V).

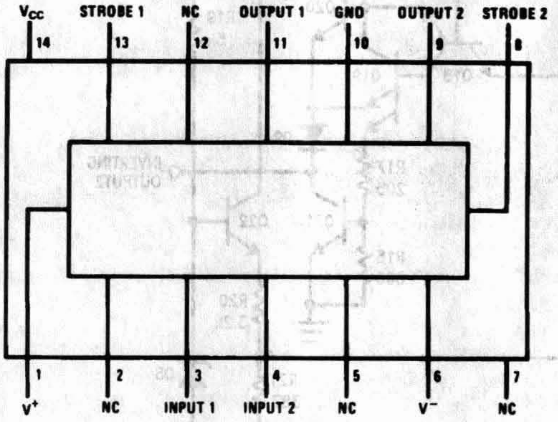
Complementary outputs having maximum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disk file systems.

Features

- Independent strobes
- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies ±15V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

Connection Diagrams

Dual-In-Line Package


V_CC
STROBE 1
NC
OUTPUT 1
GND
OUTPUT 2
STROBE 2
14
13
12
11
10
9
8
1
2
3
4
5
6
7
V⁺
NC
INPUT 1
INPUT 2
NC
V⁻
NC

TL/H/5708–2

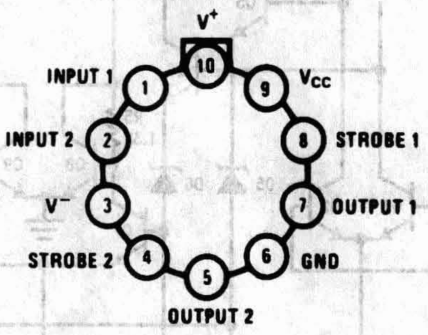
Top View

Order Number LM161J, LM161J/883*, LM361M or LM361N

See NS Package Number J14A, M14A or N14A

*Also available per SMD #5962-8757203

Metal Can Package

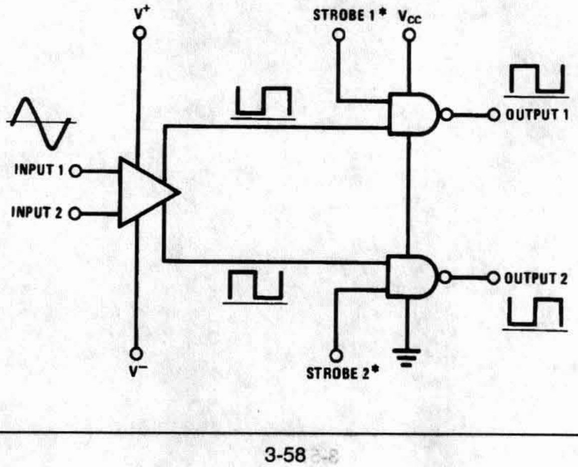

V⁺
10
INPUT 1
1
9
V_CC
INPUT 2
2
8
STROBE 1
V⁻
3
7
OUTPUT 1
STROBE 2
4
6
GND
5
OUTPUT 2

TL/H/5708–3

Order Number LM161H/883*, or LM361H

See NS Package Number H10C

Logic Diagram


V⁺
STROBE 1*
V_CC
OUTPUT 1
INPUT 1
INPUT 2
OUTPUT 2
V⁻
STROBE 2*

*Output is low when current is drawn from strobe pin.

TL/H/5708–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Positive Supply Voltage, V^+		+16V
Negative Supply Voltage, V^-		−16V
Gate Supply Voltage, V_{CC}		+7V
Output Voltage		+7V
Differential Input Voltage		±5V
Input Common Mode Voltage		±6V
Power Dissipation		600 mW
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	T_{MIN}	T_{MAX}
LM161	−55°C to	+125°C
LM261	−25°C to	+85°C
LM361	0°C to	+70°C
Lead Temp. (Soldering, 10 seconds)		260°C
For Any Device Lead Below V^-		0.3V

Operating Conditions

	Min	Typ	Max
Supply Voltage V^+			
LM161/LM261	5V		15V
LM361	5V		15V
Supply Voltage V^-			
LM161/LM261	−6V		−15V
LM361	−6V		−15V
Supply Voltage V_{CC}			
LM161/LM261	4.5V	5V	5.5V
LM361	4.75V	5V	5.25V
ESD Tolerance (Note 5)			1600V
Soldering Information			
Dual-In-Line Package			
Soldering (10 seconds)			260°C
Small Outline Package			
Vapor Phase (60 seconds)			215°C
Infrared (15 seconds)			220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \le T_A \le T_{MAX}$, unless noted)

Parameter	Conditions	Limits						Units
		LM161/LM261			LM361			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			1	3		1	5	mV
Input Bias Current	$T_A = 25°C$		5	20		10	30	μA μA
Input Offset Current	$T_A = 25°C$		2	3		2	5	μA μA
Voltage Gain	$T_A = 25°C$		3			3		V/mV
Input Resistance	$T_A = 25°C$, f = 1 kHz		20			20		kΩ
Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{SOURCE} = -0.5$ mA	2.4	3.3		2.4	3.3		V
Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{SINK} = 6.4$ mA			0.4			0.4	V
Strobe Input "1" Current (Output Enabled)	$V_{CC} = 5.25V$, $V_{STROBE} = 2.4V$			200			200	μA
Strobe Input "0" Current (Output Disabled)	$V_{CC} = 5.25V$, $V_{STROBE} = 0.4V$			−1.6			−1.6	mA
Strobe Input "0" Voltage	$V_{CC} = 4.75V$			0.8			0.8	V
Strobe Input "1" Voltage	$V_{CC} = 4.75V$	2			2			V
Output Short Circuit Current	$V_{CC} = 5.25V$, $V_{OUT} = 0V$	−18		−55	−18		−55	mA

Electrical Characteristics (Continued)

($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless noted)

Parameter	Conditions	Limits						Units
		LM161/LM261			LM361			
		Min	Typ	Max	Min	Typ	Max	
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \leq T_A \leq 125°C$			4.5				mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						5	mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \leq T_A \leq 125°C$			10				mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						10	mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \leq T_A \leq 125°C$			18				mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						20	mA
Transient Response	$V_{IN} = 50$ mV overdrive (Note 3)							
Propagation Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		14	20		14	20	ns
Propagation Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		14	20		14	20	ns
Delay Between Output A and B	$T_A = 25°C$		2	5		2	5	ns
Strobe Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		8			8		ns
Strobe Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		8			8		ns

Note 1: The device may be damaged by use beyond the maximum ratings.

Note 2: Typical thermal impedances are as follows:

	H Package	J Package	N Package
θ_{jA}	165°C/W (Still Air) 67°C/W (400 LF/Min Air Flow)	112°C/W	105°C/W
θ_{jC}	25°C/W		

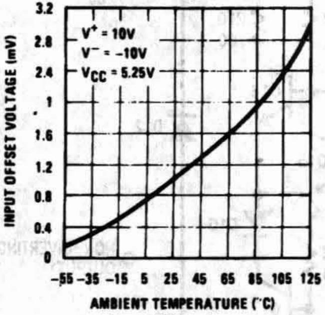
Note 3: Measurements using AC Test circuit, Fanout = 1. The devices are faster at low supply voltages.

Note 4: Refer to RETS161X for LM161H and LM161J military specifications.

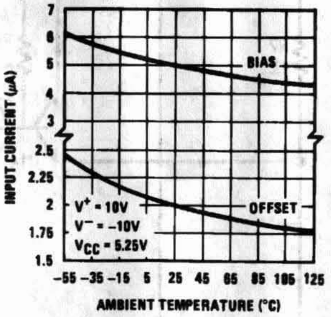
Note 5: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

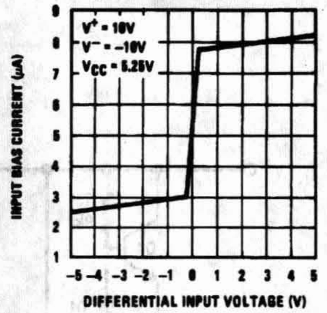
Offset Voltage



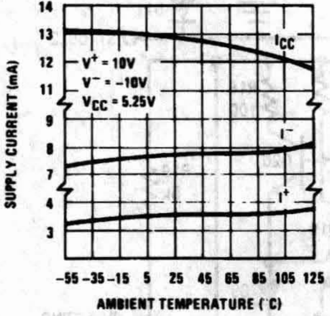
Input Currents vs Ambient Temperature



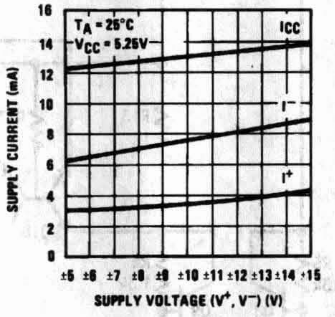
Input Characteristics



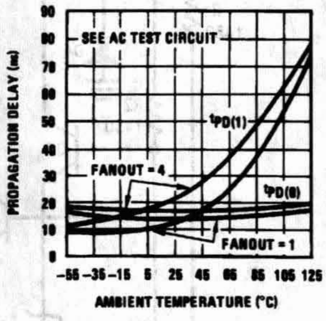
Supply Current vs Ambient Temperature



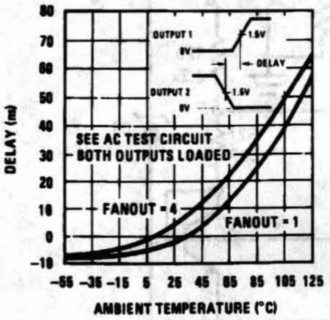
Supply Current vs Supply Voltage



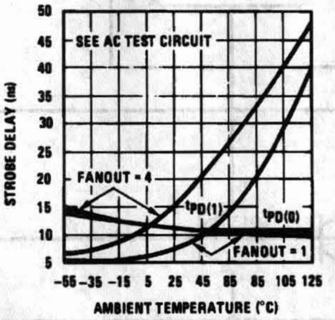
Propagation Delay vs Ambient Temperature



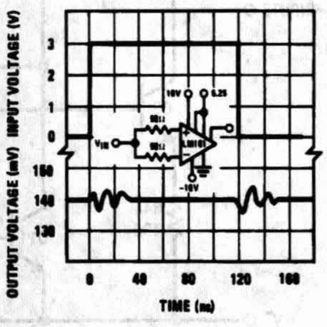
Delay of Output 1 With Respect to Output 2 vs Ambient Temperature



Strobe Delay vs Ambient Temperature

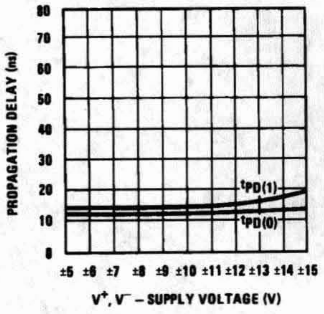


Common-Mode Pulse Response



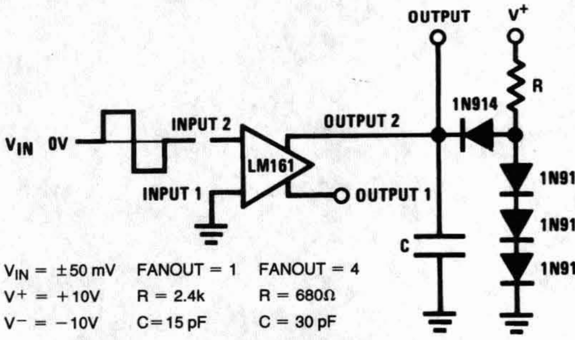
TL/H/5708–5

Propagation Delay vs Supply Voltage



TL/H/5708–7

AC Test Circuit

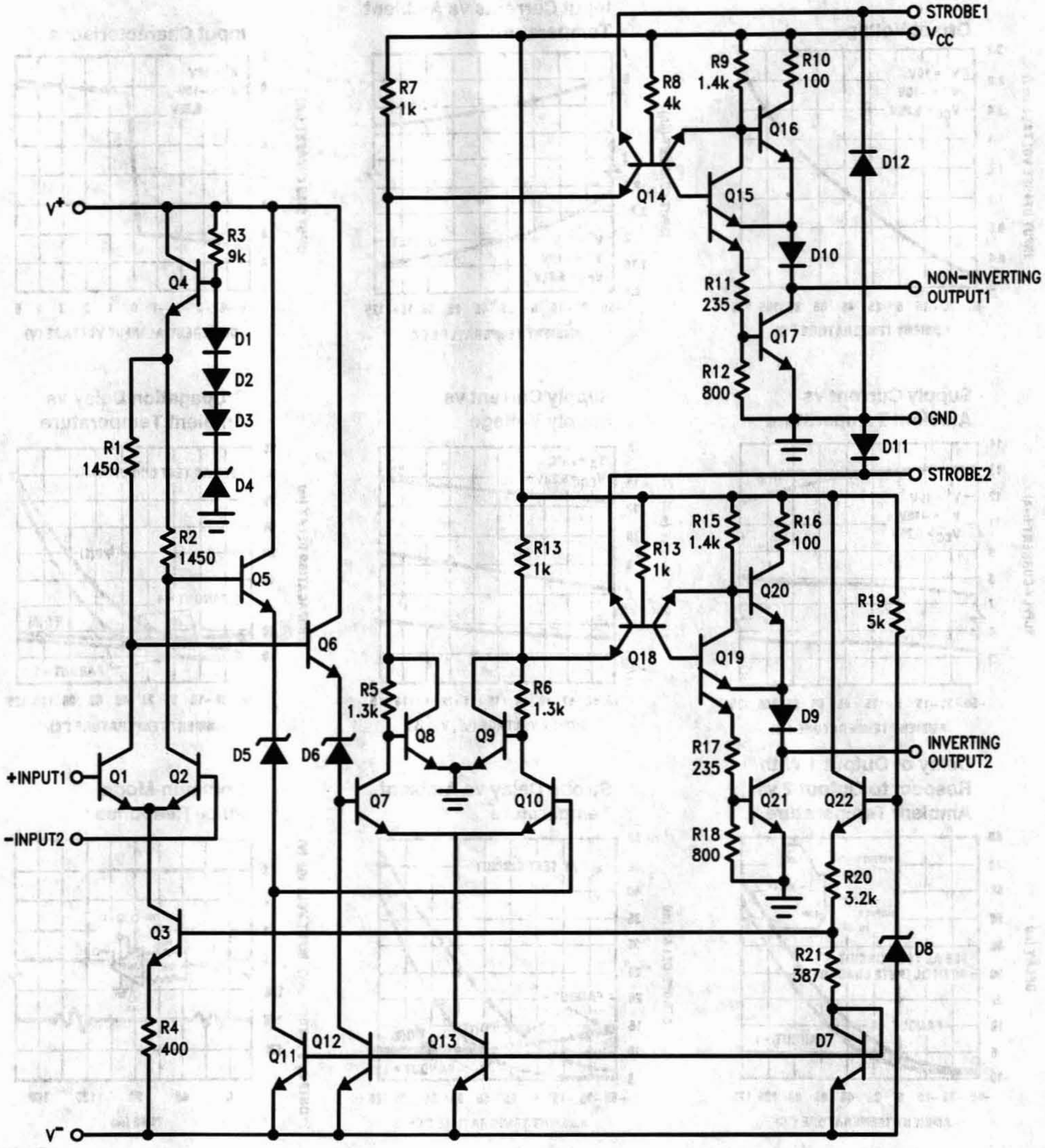

OUTPUT
V+
R
1N914
VIN 0V
INPUT 2
OUTPUT 2
LM161
INPUT 1
OUTPUT 1
1N914
1N914
1N914
C

V_{IN} = ±50 mV	FANOUT = 1	FANOUT = 4
V^+ = +10V	R = 2.4k	R = 680Ω
V^- = −10V	C = 15 pF	C = 30 pF
V_{CC} = 5.25V		

TL/H/5708–6

Schematic Diagram

LM161


STROBE1
V_{CC}
R7
1k
R8
4k
R9
1.4k
R10
100
Q16
D12
Q14
Q15
D10
NON-INVERTING
OUTPUT1
R11
235
Q17
R12
800
GND
D11
STROBE2
V^+
R3
9k
Q4
D1
D2
D3
D4
R1
1450
R2
1450
Q5
Q6
R13
1k
R13
1k
R15
1.4k
R16
100
Q20
R19
5k
Q18
Q19
D9
R5
1.3k
R6
1.3k
Q8
Q9
D5
D6
Q7
Q10
R17
235
INVERTING
OUTPUT2
Q21
Q22
+INPUT1
Q1
Q2
-INPUT2
R18
800
R20
3.2k
Q3
D8
R21
387
R4
400
Q12
Q13
Q11
D7
V^-

TL/H/5708-1

R10, R16: 85

R11, R17: 205

National Semiconductor

LM193/LM293/LM393/LM2903
Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

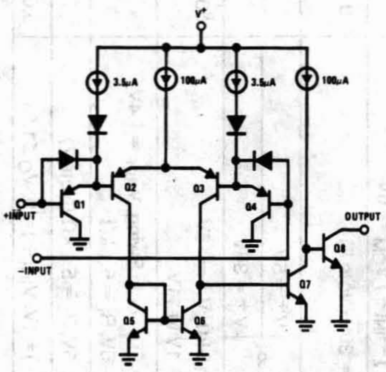
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

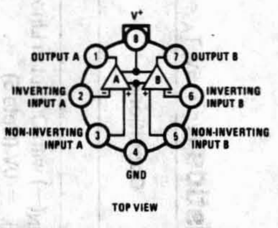
Features

- Wide supply
  - Voltage range 2.0V to 36V
  - single or dual supplies ±1.0V to ±18V
- Very low supply current drain (0.4 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage, 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams

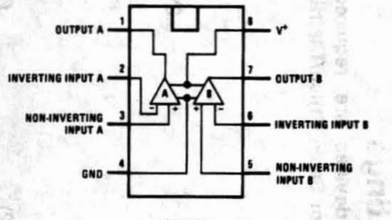

V+
3.5μA
100μA
3.5μA
100μA
+INPUT
Q1
Q2
Q3
Q4
OUTPUT
Q8
−INPUT
Q7
Q5
Q6

Metal Can Package


V+
8
OUTPUT A 1
7 OUTPUT B
INVERTING INPUT A 2
6 INVERTING INPUT B
NON-INVERTING INPUT A 3
5 NON-INVERTING INPUT B
4
GND
A
B
TOP VIEW

Order Number LM193H, LH193H/883*, LM193AH, LM193AH/883, LM293H, LM293AH, LM393H or LM393AH
See NS Package Number H08C

Dual-In-Line Package


OUTPUT A 1
INVERTING INPUT A 2
NON-INVERTING INPUT A 3
GND 4
8 V+
7 OUTPUT B
6 INVERTING INPUT B
5 NON-INVERTING INPUT B
A
B
TOP VIEW

TL/H/5709–1

Order Number LM193J/883*, LM193AJ/883, LM393J, LM393AJ, LM393M, LM2903M, LM393N, LM2903J or LM2903N
See NS Package Number J08A, M08A or N08E

*Also available per JM38510/11202

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 10)

Supply Voltage, V^+	36V
Differential Input Voltage (Note 8)	36V
Input Voltage	−0.3V to +36V
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA
Power Dissipation (Note 1)	
Molded DIP	780 mW
Metal Can	660 mW
Small Outline Package	510 mW
Output Short-Circuit to Ground (Note 2)	Continuous

Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating (1.5 kΩ in series with 100 pF)	1300V

Electrical Characteristics ($V^+ = 5V$, $T_A = 25°C$, unless otherwise stated)

Parameter	Conditions	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		1.0	2.0		1.0	2.0		1.0	5.0		1.0	5.0		2.0	7.0	mV
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, $V_{CM} = 0V$ (Note 5)		25	100		25	250		25	100		25	250		25	250	nA
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$ $V_{CM} = 0V$		3.0	25		5.0	50		3.0	25		5.0	50		5.0	50	nA
Input Common Mode Voltage Range	$V^+ = 30V$ (Note 6)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	$R_L = \infty$, $V^+ = 5V$		0.4	1		0.4	1		0.4	1		0.4	1		0.4	1.0	mA
	$V^+ = 36V$		1	2.5		1	2.5		1	2.5		1	2.5		1	2.5	mA
Voltage Gain	$R_L \geq 15$ kΩ, $V^+ = 15V$ $V_O = 1V$ to $11V$	50	200		50	200		50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4V$ $V_{RL} = 5V$, $R_L = 5.1$ kΩ		300			300			300			300			300		ns
Response Time	$V_{RL} = 5V$, $R_L = 5.1$ kΩ (Note 7)		1.3			1.3			1.3			1.3			1.5		μs
Output Sink Current	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA		250	400		250	400		250	400		250	400		250	400	mV
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN}(+) = 1V$, $V_O = 5V$		0.1			0.1			0.1			0.1			0.1		nA

Electrical Characteristics ($V^+ = 5V$) (Note 4)

Parameter	Conditions	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			4.0			4.0			9			9		9	15	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			100			150			100			150		50	200	nA
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500	nA
Input Common Mode Voltage Range	$V^+ = 30V$ (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V
Saturation Voltage	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA			700			700			700			700		400	700	mV
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN(+)} = 1V$, $V_O = 30V$			1.0			1.0			1.0			1.0			1.0	μA
Differential Input Voltage	Keep All V_{IN}'s $\geq 0V$ (or V^-, if Used), (Note 8)			36			36			36			36			36	V

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V$.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM193/LM193A, With the LM293/LM293A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM393/LM393A temperature specifications are limited to $0°C \leq T_A \leq +70°C$. The LM2903 is limited to $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

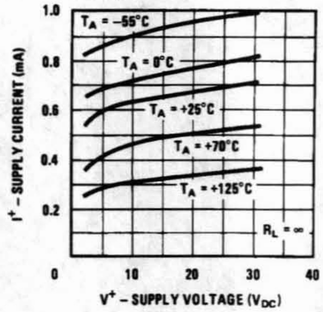
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V$ (or 0.3V below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \simeq 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$), at 25°C.

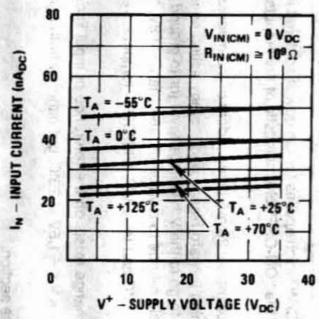
Note 10: Refer to RETS193AX for LM193AH military specifications and to RETS193X for LM193H military specifications.

Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A

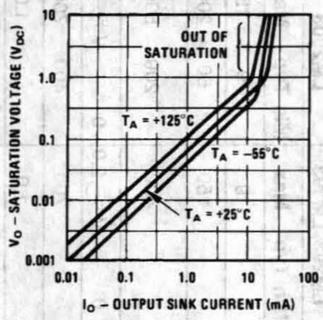
Supply Current



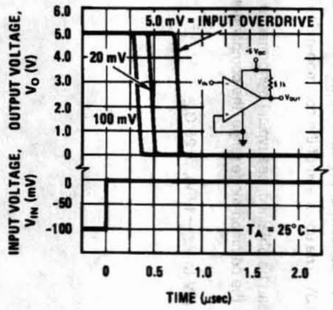
Input Current



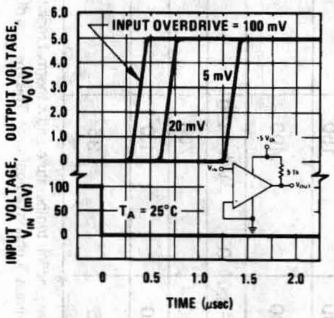
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



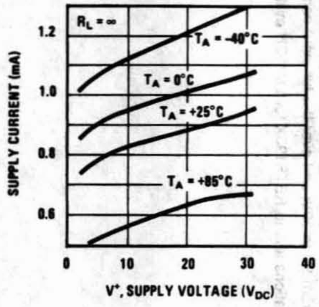
Response Time for Various Input Overdrives—Positive Transition



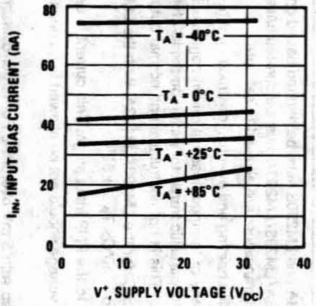
TL/H/5709–3

Typical Performance Characteristics LM2903

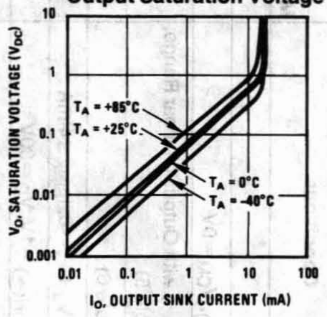
Supply Current



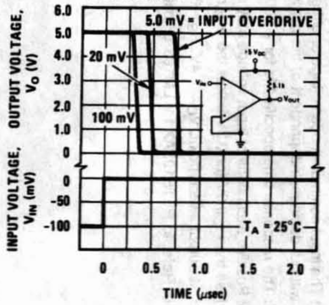
Input Current



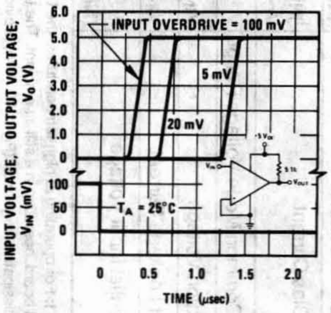
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



TL/H/5709–4

Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

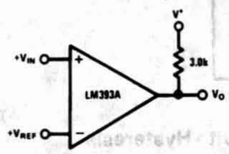
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

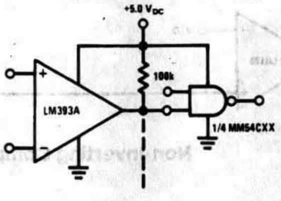
The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications ($V^+ = 5.0\ V_{DC}$)

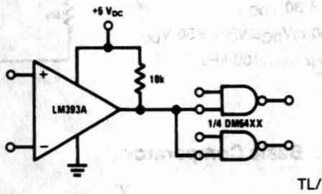
Basic Comparator



Driving CMOS



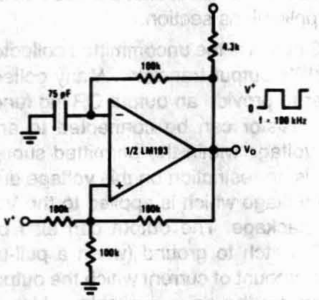
Driving TTL



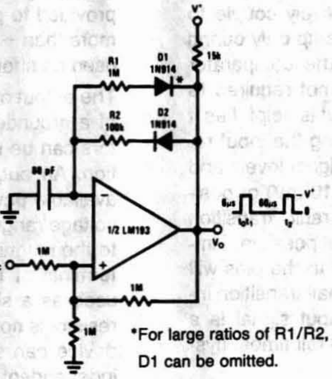
TL/H/5709–2

Typical Applications (Continued)

Squarewave Oscillator

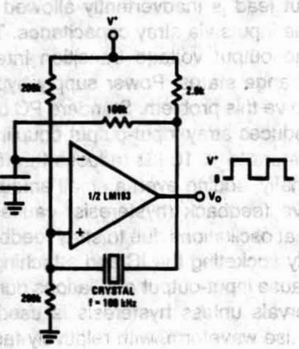

V⁺
4.3k
100k
75 pF
V⁺
0
f = 100 kHz
1/2 LM193
V₀
V⁺
100k
100k
100k

Pulse Generator

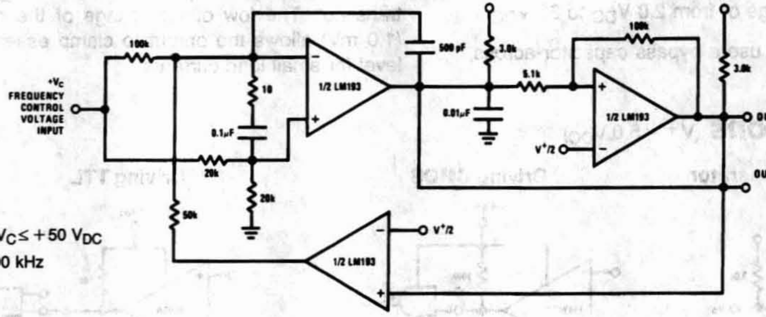

V⁺
15k
R1
1M
D1
1N914
*
R2
100k
D2
1N914
80 pF
1/2 LM193
6μs
60μs
t₀
t₁
t₂
V⁺
0
V₀
+15 V_DC
1M
1M
1M

*For large ratios of R1/R2, D1 can be omitted.

Crystal Controlled Oscillator


V⁺
200k
2.0k
100k
0.1μF
V⁺
0
1/2 LM193
V₀
CRYSTAL
f = 100 kHz
200k

Two-Decade High-Frequency VCO


+V_C
FREQUENCY CONTROL VOLTAGE INPUT
100k
10
0.1μF
20k
20k
50k
1/2 LM193
500 pF
V⁺
3.0k
0.01μF
5.1k
100k
V⁺
3.0k
1/2 LM193
V⁺/2
OUTPUT 1
OUTPUT 2
1/2 LM193
V⁺/2

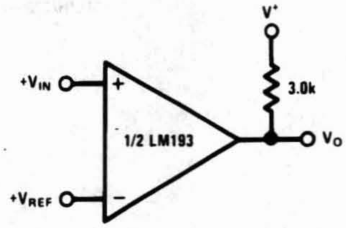
$V^+ = +30\ V_{DC}$

$+250\ mV_{DC} \leq V_C \leq +50\ V_{DC}$

$700\ Hz \leq f_o \leq 100\ kHz$

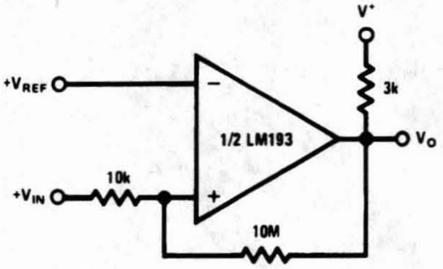
TL/H/5709-5

Basic Comparator


V⁺
3.0k
+V_IN
+
1/2 LM193
V₀
+V_REF
−

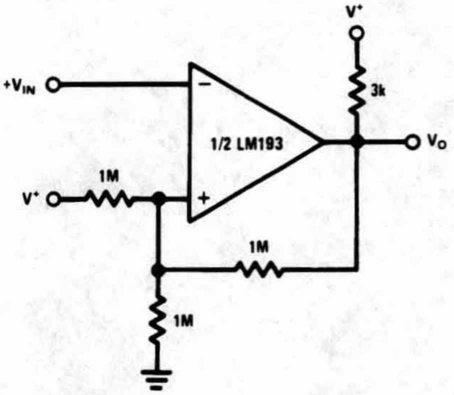
TL/H/5709-6

Non-Inverting Comparator with Hysteresis


V⁺
+V_REF
−
3k
1/2 LM193
V₀
10k
+V_IN
+
10M

TL/H/5709-9

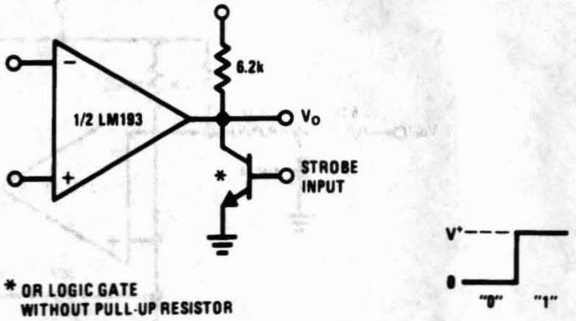
Inverting Comparator with Hysteresis


V⁺
+V_IN
−
3k
1/2 LM193
V₀
1M
V⁺
+
1M
1M

TL/H/5709-10

Typical Applications (Continued)

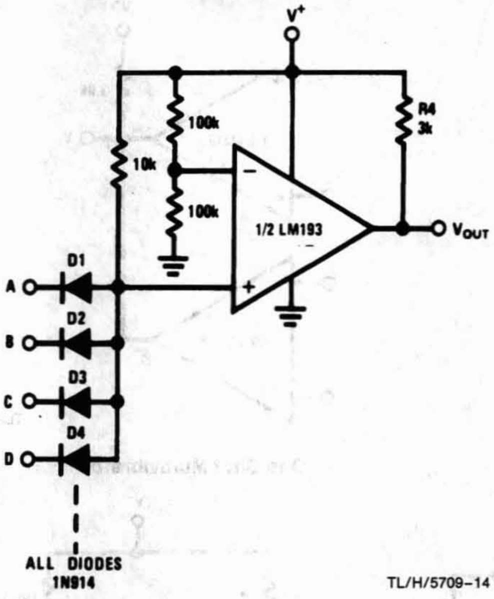
Output Strobing


V+
6.2k
1/2 LM193
VO
STROBE INPUT
*
V+
0
"0"
"1"

* OR LOGIC GATE WITHOUT PULL-UP RESISTOR

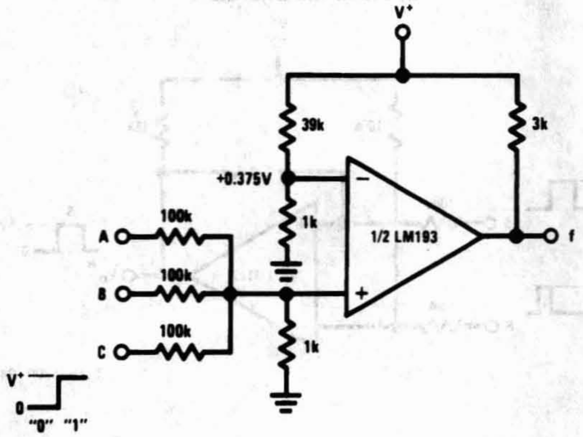
TL/H/5709–11

Large Fan-in AND Gate


V+
100k
10k
100k
R4
3k
1/2 LM193
VOUT
D1
A
D2
B
D3
C
D4
D
ALL DIODES
1N914

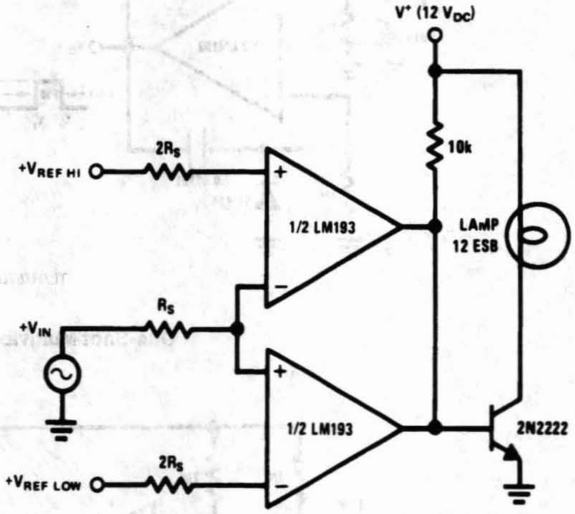
TL/H/5709–14

AND Gate


V+
39k
3k
+0.375V
1k
1/2 LM193
f
A
100k
B
100k
C
100k
1k
V+
0
"0" "1"

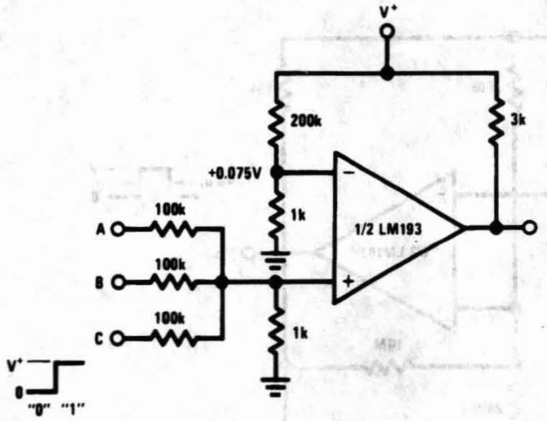
TL/H/5709–12

Limit Comparator


V+ (12 VDC)
10k
+VREF HI
2RS
1/2 LM193
LAMP
12 ESB
+VIN
RS
1/2 LM193
2N2222
+VREF LOW
2RS

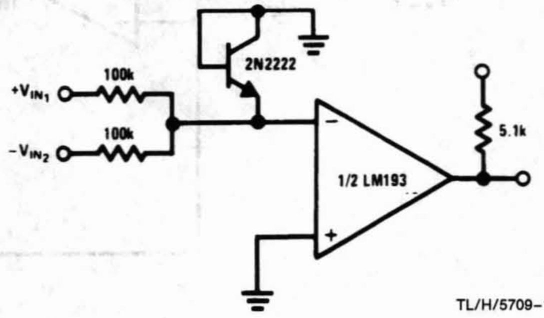
TL/H/5709–15

OR Gate


V+
200k
3k
+0.075V
1k
1/2 LM193
f
A
100k
B
100k
C
100k
1k
V+
0
"0" "1"

TL/H/5709–13

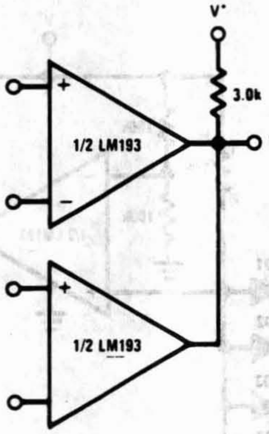
Comparing Input Voltages of Opposite Polarity


2N2222
+VIN1
100k
−VIN2
100k
5.1k
1/2 LM193

TL/H/5709–16

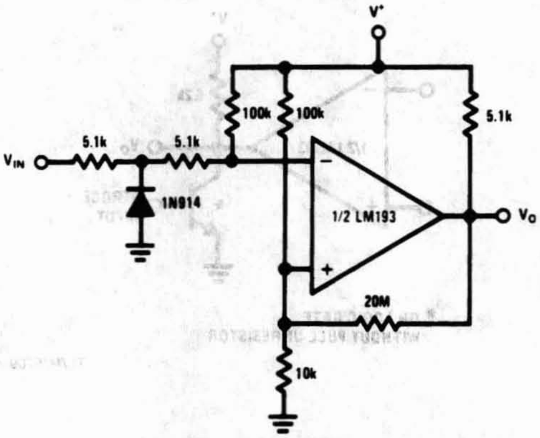
Typical Applications (Continued)

ORing the Outputs


V+
3.0k
+
−
1/2 LM193
V_O
+
1/2 LM193

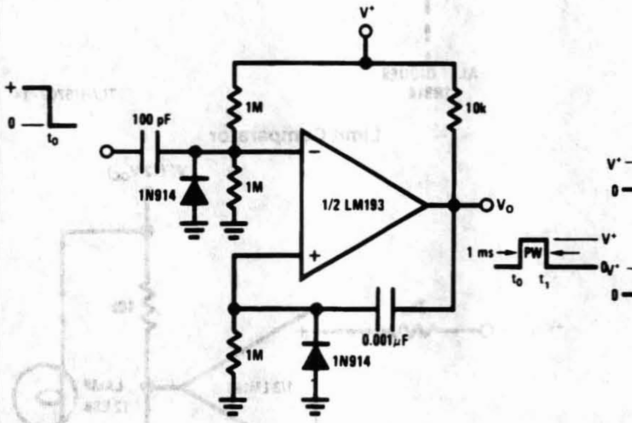
TL/H/5709-17

Zero Crossing Detector (Single Power Supply)


V+
100k
100k
5.1k
V_IN
5.1k
5.1k
1N914
−
+
1/2 LM193
V_O
20M
10k

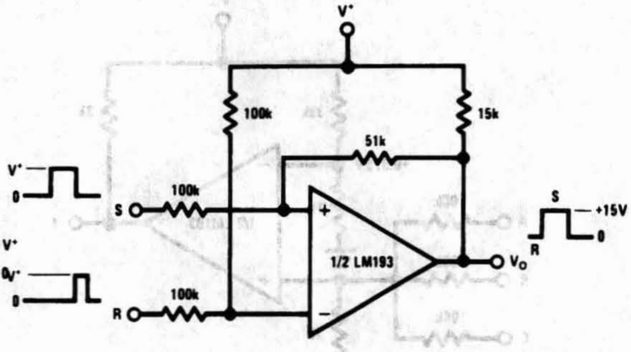
TL/H/5709-21

One-Shot Multivibrator


V+
+
0
t0
100 pF
1N914
1M
1M
10k
−
+
1/2 LM193
V_O
1M
1N914
0.001μF
1 ms
PW
t0
t1
V+
0

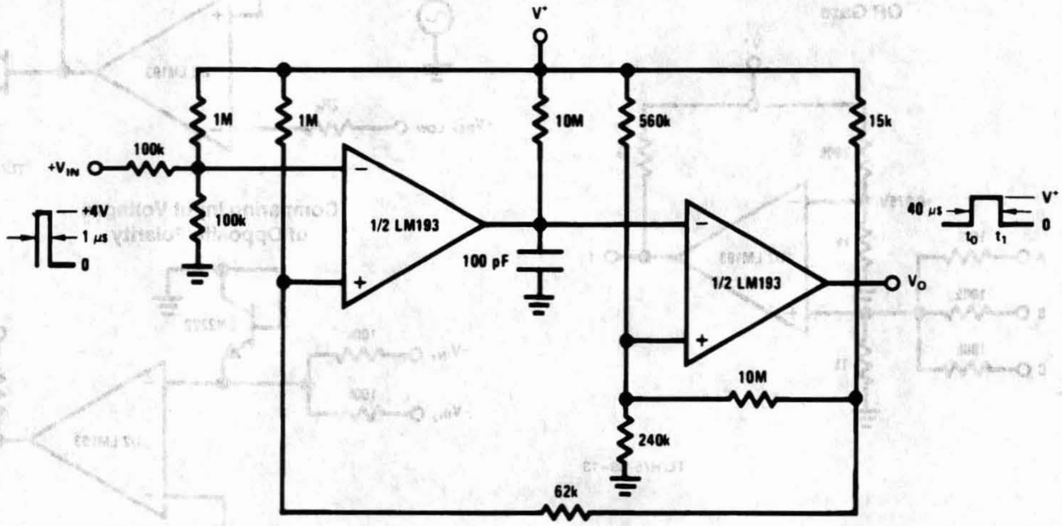
TL/H/5709-22

Bi-Stable Multivibrator


V+
100k
15k
51k
V+
0
S
100k
+
−
1/2 LM193
V_O
R
100k
V+
0
S
+15V
R
0

TL/H/5709-24

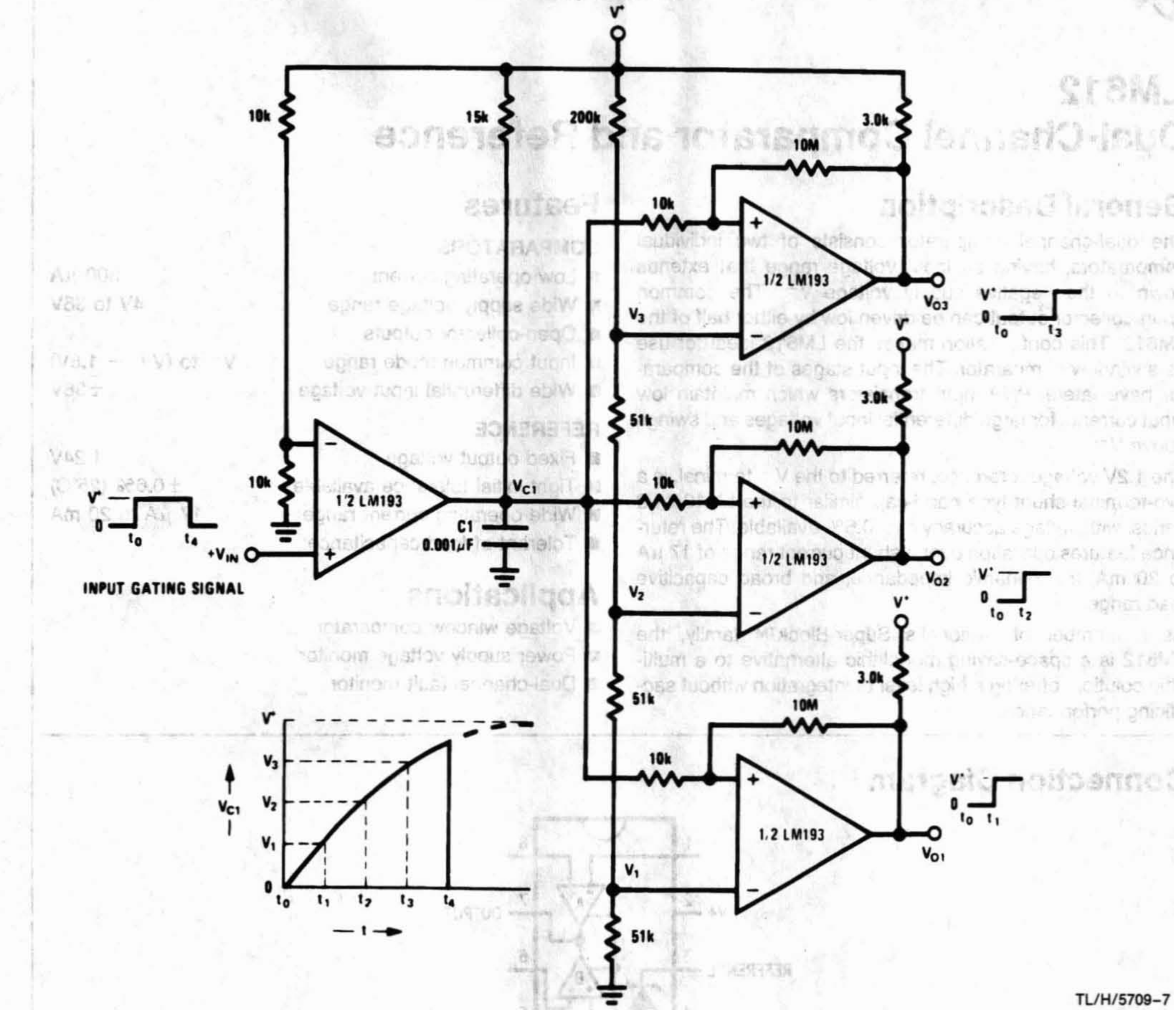
One-Shot Multivibrator with Input Lock Out


V+
1M
1M
10M
560k
15k
+V_IN
100k
100k
+4V
1 μs
0
−
+
1/2 LM193
100 pF
−
+
1/2 LM193
V_O
10M
240k
62k
40 μs
V+
0
t0
t1

TL/H/5709-23

Typical Applications (Continued) ($V^+ = V_{DC}$)

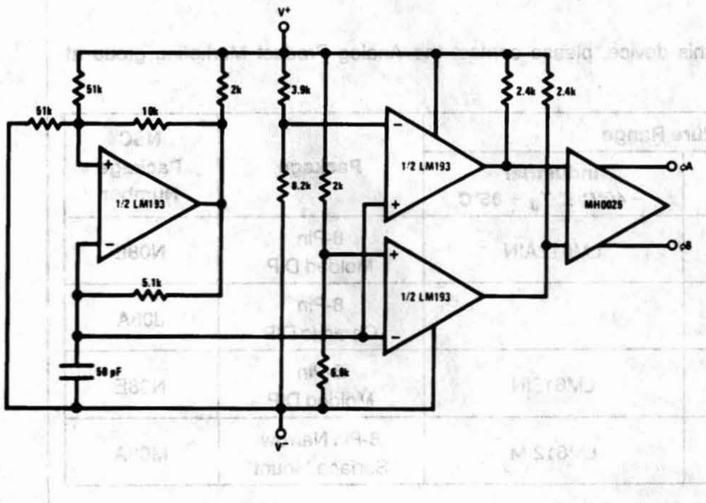
Time Delay Generator


V+
10k
15k
200k
3.0k
10M
10k
+
−
1/2 LM193
V_O3
V3
V+
0
t0
t3
3.0k
51k
10M
10k
1/2 LM193
V_O2
V2
V+
0
t0
t2
10k
1/2 LM193
V_C1
C1
0.001μF
+V_IN
V+
0
t0
t4
INPUT GATING SIGNAL
V+
3.0k
51k
10M
10k
1.2 LM193
V_O1
V1
V+
0
t0
t1
51k
V+
V3
V2
V1
V_C1
0
t0
t1
t2
t3
t4
— t →

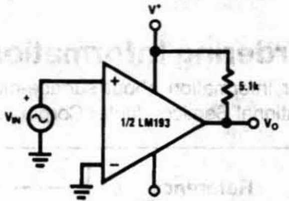
TL/H/5709–7

Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)

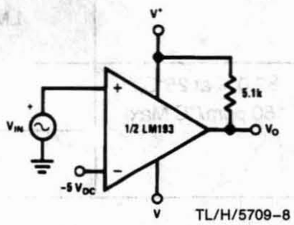
MOS Clock Driver


V+
51k
2k
3.9k
2.4k
2.4k
51k
10k
1/2 LM193
1/2 LM193
8.2k
2k
MH0025
φA
φB
1/2 LM193
5.1k
50 pF
6.8k
V−

Zero Crossing Detector


V+
5.1k
V_IN
1/2 LM193
V_O
V−

Comparator With a Negative Reference


V+
5.1k
V_IN
1/2 LM193
V_O
−5 V_DC
V

TL/H/5709–8

National Semiconductor

LM612
Dual-Channel Comparator and Reference

General Description

The dual-channel comparator consists of two individual comparators, having an input voltage range that extends down to the negative supply voltage V−. The common open-collector output can be driven low by either half of the LM612. This configuration makes the LM612 ideal for use as a window comparator. The input stages of the comparator have lateral PNP input transistors which maintain low input currents for large differential input voltages and swings above V+.

The 1.2V voltage reference, referred to the V− terminal, is a two-terminal shunt-type band-gap similar to the LM185-1.2 series, with voltage accuracy of ±0.6% available. The reference features operation over a shunt current range of 17 μA to 20 mA, low dynamic impedance, and broad capacitive load range.

As a member of National's Super-Block™ family, the LM612 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

COMPARATORS

■ Low operating current	300 μA
■ Wide supply voltage range	4V to 36V
■ Open-collector outputs	
■ Input common-mode range	V− to (V+ − 1.8V)
■ Wide differential input voltage	±36V

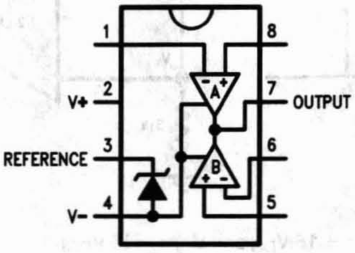
REFERENCE

■ Fixed output voltage	1.24V
■ Tight initial tolerance available	±0.6% (25°C)
■ Wide operating current range	17 μA to 20 mA
■ Tolerant of load capacitance	

Applications

- Voltage window comparator
- Power supply voltage monitor
- Dual-channel fault monitor

Connection Diagram



TL/H/11058–1

Top View

Ordering Information

For information about surface-mount packaging of this device, please contact the Analog Product Marketing group at National Semiconductor Corporation headquarters.

Reference Tolerances	Temperature Range		Package	NSC Package Number
	Military $-55°C \le T_J \le +125°C$	Industrial $-40°C \le T_J +85°C$		
±0.6% at 25°C, 80 ppm/°C Max	LM612AMN	LM612AIN	8-Pin Molded DIP	N08E
	LM612AMJ/883 (Note 13)		8-Pin Ceramic DIP	J08A
±2.0% at 25°C, 150 ppm/°C Max	LM612MN	LM612IN	8-Pin Molded DIP	N08E
		LM612IM	8-Pin Narrow Surface Mount	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except V_R (referred to V^- pin)	
(Note 2)	36V (Max)
(Note 3)	−0.3V (Min)
Current through Any Input Pin and V_R Pin	±20 mA
Differential Input Voltage	±36V
Output Short-Circuit Duration	(Note 4)
Storage Temperature Range	$-65°C \leq T_J \leq +150°C$
Maximum Junction Temperature	150°C
Thermal Resistance, Junction-to-Ambient (Note 5)	
N Package	100°C/W
Soldering Information	
N Package	
Soldering (10 seconds)	260°C
ESD Tolerance (Note 6)	±1 kV

Operating Temperature Range

LM612AI, LM612I	$-40°C \leq T_J \leq +85°C$
LM612AM, LM612M	$-55°C \leq T_J \leq +125°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = V^+/2$, $I_R = 100\ \mu A$, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 7)	LM612AM LM612AI Limits (Note 8)	LM612M LM612I Limits (Note 8)	Units
COMPARATORS						
I_S	Total Supply Current	V^+ Current, $R_{LOAD} = \infty$, $3V \leq V^+ \leq 36V$	150 **170**	250 **300**	250 **300**	μA Max μA Max
V_{OS}	Offset Voltage over V^+ Range	$4V \leq V^+ \leq 36V$, $R_L = 15\ k\Omega$	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV Max mV Max
V_{OS}	Offset Voltage over V_{CM} Range	$0V \leq V_{CM} \leq (V^+ - 1.8V)$ $V^+ = 30V$, $R_L = 15\ k\Omega$	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV Max mV Max
$\frac{\Delta V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			μV/°C
I_B	Input Bias Current		5 **8**	25 **30**	35 **40**	nA Max nA Max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA Max nA Max
A_V	Voltage Gain	$R_L = 10\ k\Omega$ to 36V, $2V \leq V_{OUT} \leq 27V$	500 **100**	50	50	V/mV Min V/mV
t_R	Large Signal Response Time	$V_{+IN} = 1.4V$, V_{-IN} = TTL Swing, $R_L = 5.1\ k\Omega$	1.5 **2.0**			μs μs
I_{SINK}	Output Sink Current	$V_{+IN} = 0V$, $V_{-IN} = 1V$, $V_{OUT} = 1.5V$	20 **13**	10 **8**	10 **8**	mA Min mA Min
		$V_{OUT} = 0.4V$	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA Min mA Min
I_L	Output Leakage Current	$V_{+IN} = 1V$, $V_{-IN} = 0V$, $V_{OUT} = 36V$	0.1 **0.2**	10	10	μA Max μA

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = V^+/2$, $I_R = 100\ \mu A$, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.** (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM612AM LM612AI Limits (Note 8)	LM612M LM612I Limits (Note 8)	Units
VOLTAGE REFERENCE (Note 9)						
V_R	Reference Voltage		1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V Min V Max
$\frac{\Delta V_R}{\Delta T}$	Average Drift with Temperature	(Note 10)	**18**	**80**	**150**	ppm/°C Max
$\frac{\Delta V_R}{kH}$	Average Drift with Time	$T_J = 40°C$ $T_J = 150°C$	400 1000			ppm/kH ppm/kH
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 11)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R[100\ \mu A]} - V_{R[17\ \mu A]}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV Max mV Max
		$V_{R[10\ mA]} - V_{R[100\ \mu A]}$ (Note 12)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV Max mV Max
R	Resistance	$\Delta V_{R[10\ mA\ to\ 0.1\ mA]}/9.9\ mA$ $\Delta V_{R[100\ \mu A\ to\ 17\ \mu A]}/83\ \mu A$	0.2 0.6	**0.56** **13**	**0.56** **13**	Ω Max Ω Max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R[V+ = 5V]} - V_{R[V+ = 36V]}$	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV Max mV Max
		$V_{R[V+ = 5V]} - V_{R[V+ = 3V]}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV Max mV Max
e_n	Voltage Noise	BW = 10 Hz to 10 kHz	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is not allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Shorting the Output to V^- will not cause power dissipation, so it may be continuous. However, shorting the Output to any more positive voltage (including V^+), will cause 80 mA (typ.) to be drawn through the output transistor. This current multiplied by the applied voltage is the power dissipation in the output transistor. If this total power causes the junction temperature to exceed 150°C, degraded reliability or destruction of the device may occur. To determine junction temperature, see Note 5.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D\ \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 90°C/W for the N package.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed for $T_J = 25°C$ (standard type face) or over the full operating temperature range **(bold type face).**

Note 9: V_R is the reference output voltage, nominally 1.24V.

Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R/V_{R[25°C]} \bullet \Delta T_J$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

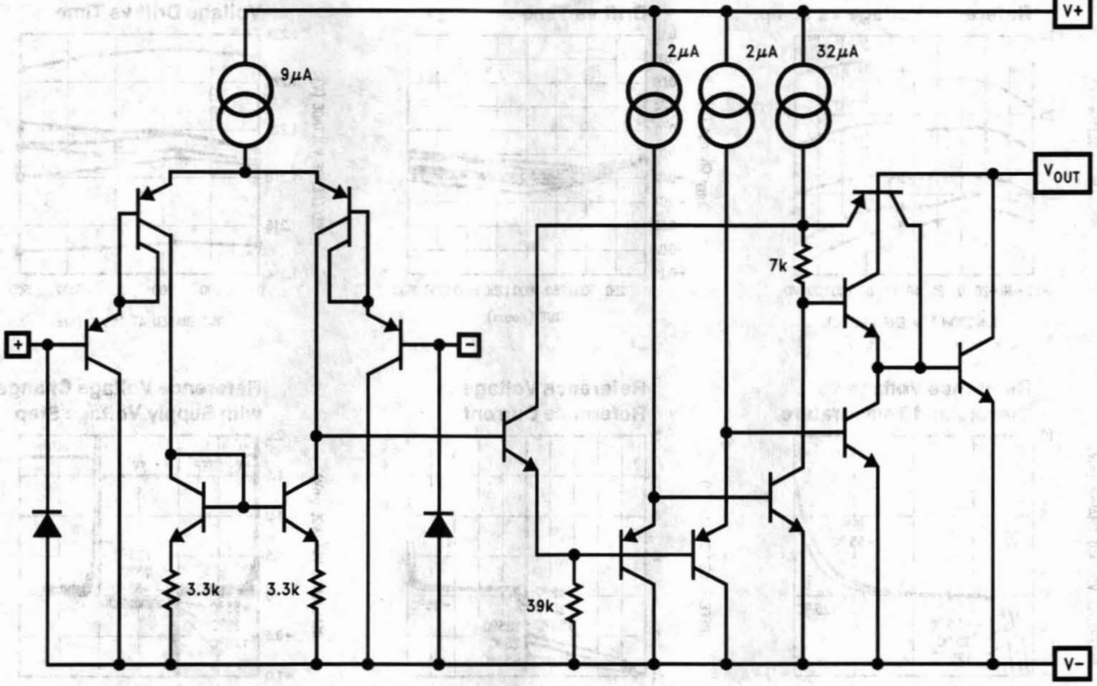
Note 11: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiralling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 12: Low contact resistance is required for accurate measurement.

Note 13: A military RETS 612AMX electrical test specification is available on request. The military screened parts can also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams

Comparator



V+
9μA
2μA
2μA
32μA
VOUT
7k
+
−
3.3k
3.3k
39k
V−

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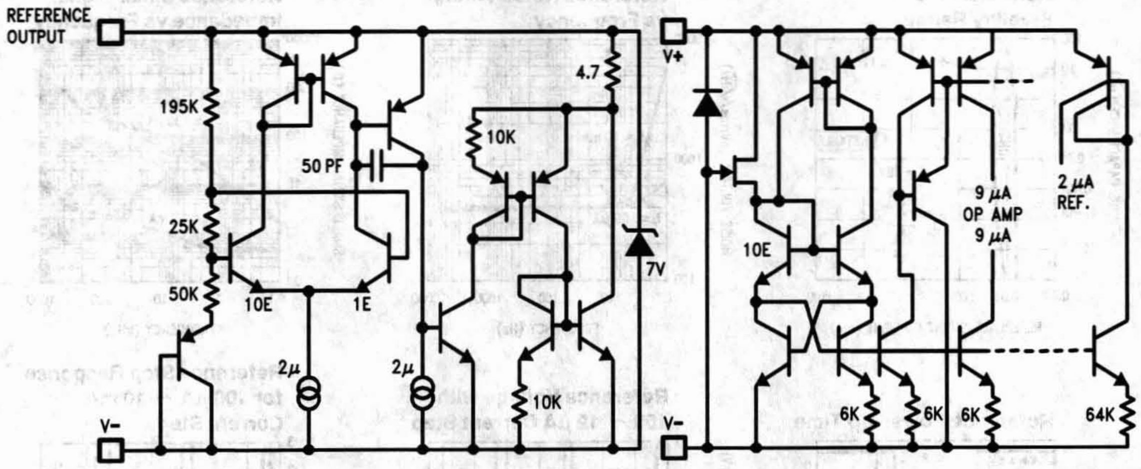
Reference

Bias



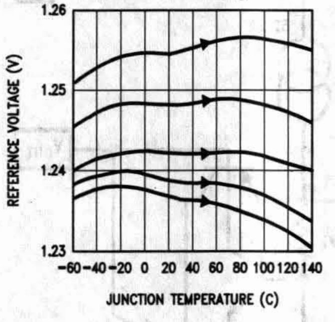
REFERENCE OUTPUT
4.7
195K
10K
50 PF
25K
7V
50K
10E
1E
2μ
2μ
10K
V−
V+
10E
9 μA
OP AMP
9 μA
2 μA
REF.
6K
6K
6K
64K
V−

TL/H/11058-3

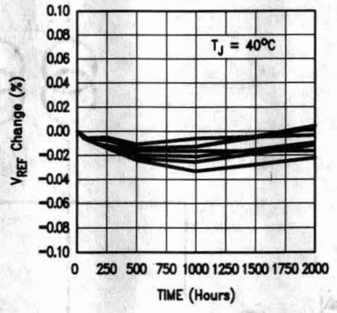
Typical Performance Characteristics (Reference)

T_J = 25°C, V^- = 0V, unless otherwise noted

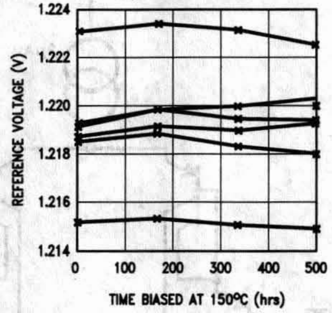
Reference Voltage vs Temp.



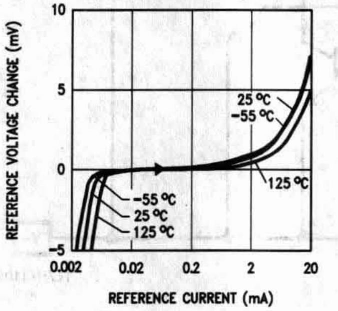
Reference Voltage Drift vs Time



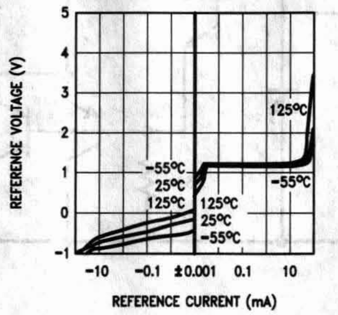
Accelerated Reference Voltage Drift vs Time



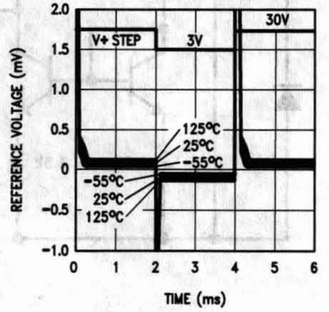
Reference Voltage vs Current and Temperature



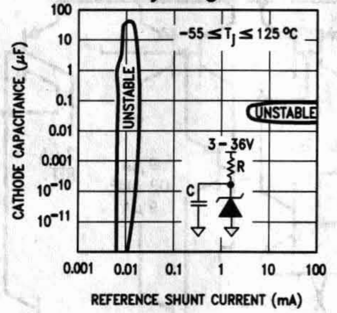
Reference Voltage vs Reference Current



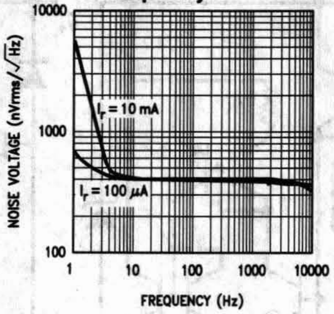
Reference Voltage Change with Supply Voltage Step



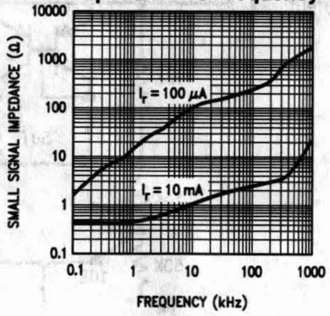
Reference AC Stability Range



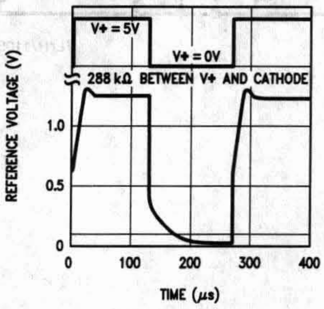
Reference Noise Voltage vs Frequency



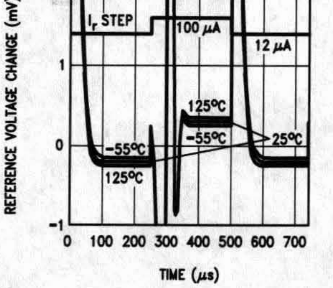
Reference Small-Signal Impedance vs Frequency



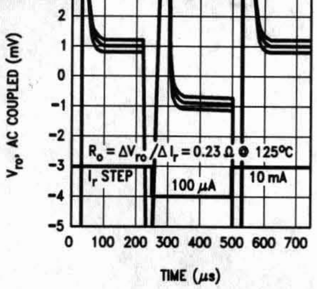
Reference Power-Up Time



Reference Voltage with 100 ∼ 12 μA Current Step



Reference Step Response for 100 μA ∼ 10 mA Current Step

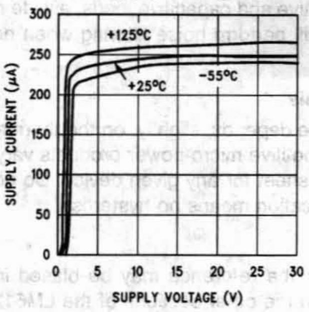


TL/H/11058–4

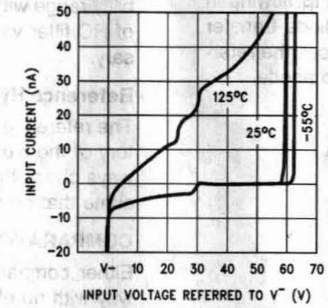
Typical Performance Characteristics (Comparators)

$T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$

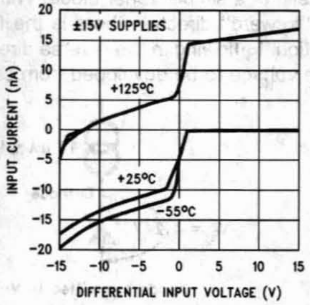
Supply Current vs Supply Voltage



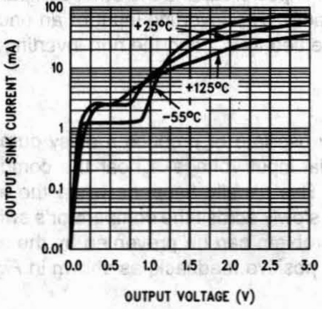
Input Bias Current vs Common-Mode Voltage



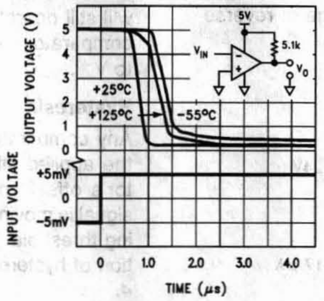
Input Current vs Differential Input Voltage



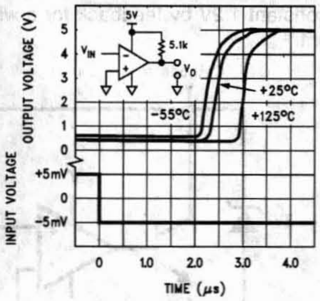
Output Saturation Voltage vs Sink Current



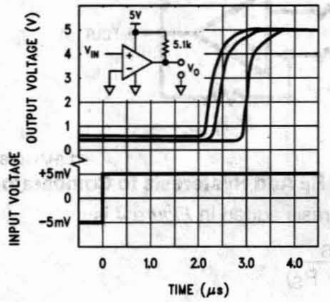
Small-Signal Response Times—Inverting Input, Negative Transition



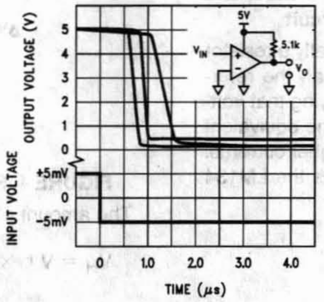
Small-Signal Response Times—Inverting Input, Positive Transition



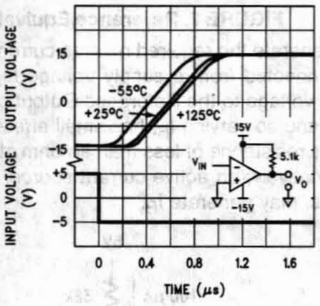
Small-Signal Response Times—Non-Inverting Input, Positive Transition



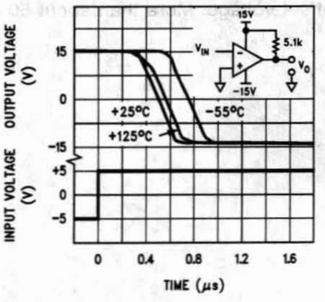
Small-Signal Response Times—Non-Inverting Input, Negative Transition



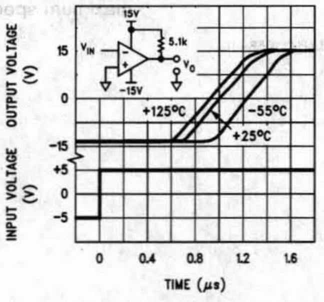
Large-Signal Response Times—Inverting Input, Positive Transition



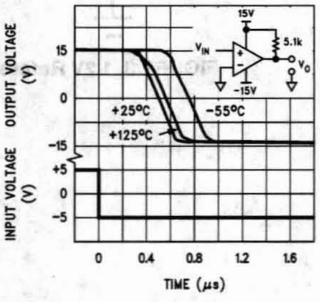
Large-Signal Response Times—Inverting Input, Negative Transition



Large-Signal Response Times—Non-Inverting Input, Positive Transition



Large-Signal Response Times—Non-Inverting Input, Negative Transition



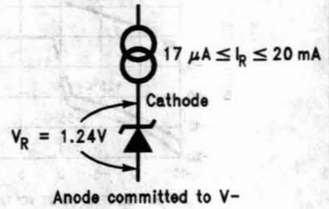
TL/H/11058–6

Application Information

VOLTAGE REFERENCE

Reference Biasing

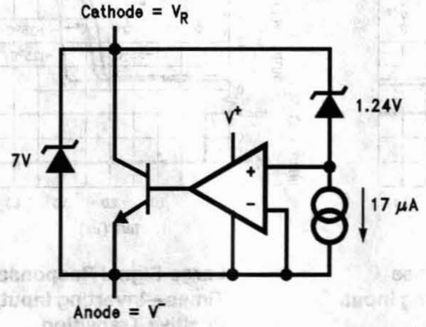
The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_R flowing in the "forward" direction there is the familiar diode transfer function. I_R flowing in the reverse direction forces the reference voltage to be developed from cathode to anode.



TL/H/11058-8

FIGURE 1. 1.24V Reference is Developed between Cathode and Anode; Current Source I_R is External

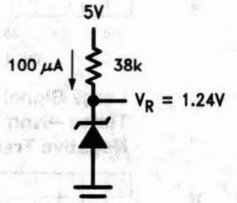
The reference equivalent circuit reveals how V_R is held at the constant 1.2V by feedback for a wide range of reverse current.



TL/H/11058-9

FIGURE 2. Reference Equivalent Circuit

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage to the Reference Output pin. Varying that voltage, and so varying I_R, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_R.



TL/H/11058-10

FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA the reference is stable for any value of capacitance. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering when necessary.

Reference Hysteresis

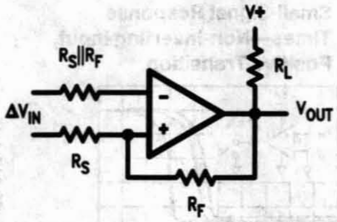
The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the datasheet for any given device. Do not assume that no specification means no hysteresis.

COMPARATORS

Either comparator or the reference may be biased in any way with no effect on the other sections of the LM612, except when a substrate diode conducts (see Electrical Characteristics Note 3). For example, one or both inputs of one comparator may be outside the input voltage range limits, the reference may be unpowered, and the other comparator will still operate correctly. The inverting input of an unused comparator should be tied to V^- and the non-inverting tied to V^+.

Hysteresis

Any comparator may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis, or positive feedback, as shown in *Figure 4*.



TL/H/11058-11

FIGURE 4. R_S and R_F Add Hysteresis to Comparator

The amount of hysteresis added in *Figure 4* is

$$V_H = V^+ \times \frac{R_S}{(R_F + R_S)}$$

$$\approx V^+ \times \frac{R_S}{R_F} \quad \text{for } R_F >> R_S$$

A good rule of thumb is to add hysteresis of at least the maximum specified offset voltage. More than about 50 mV

Application Information (Continued)

of hysteresis can substantially reduce the accuracy of the comparator, since the offset voltage is effectively being increased by the hysteresis when the comparator output is high.

It is often a good idea to decrease the amount of hysteresis until oscillations are observed, then use three times that minimum hysteresis in the final circuit. Note that the amount of hysteresis needed is greatly affected by layout. The amount of hysteresis should be rechecked each time the layout is changed, such as changing from a breadboard to a P.C. board.

Input Stage

The input stage uses lateral PNP input transistors which, unlike those of many op amps, have breakdown voltage BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

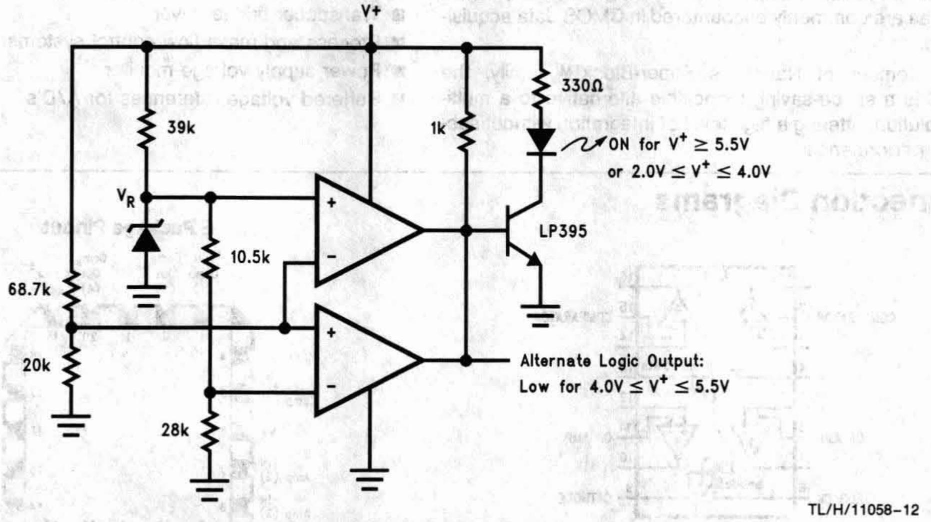
The guaranteed common-mode input voltage range for an LM612 is $V^- \leq V_{CM} \leq (V^+ - 1.8V)$, over temperature. This is the voltage range in which the comparisons must be made. If both inputs are within this range, the output will be at the correct state. If one input is within this range, and the other input is less than $(V^- + 32V)$, even if this is greater than V^+, the output will be at the correct state. If, however, either or both inputs are driven below V^-, and either input current exceeds 10 μA, the output state is not guaranteed to be correct. If both inputs are above $(V^+ - 1.8V)$, the output state is also not guaranteed to be correct.

Output Stage

The comparators have a common open-collector output stage which requires a pull-up resistor to a positive supply voltage for the output to switch properly. When the internal output transistor is off, the output (HIGH) voltage will be pulled up to this external positive voltage.

To ensure that the LOW output voltage is under the TTL-low threshold, the output transistor's load current must be less than 0.8 mA (over temperature) when it turns on. This impacts the minimum value of the pull-up resistor.

Typical Applications



TL/H/11058-12

Power Supply Monitor with Indicator

National Semiconductor

LM613 Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

General Description

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

■ Low operating current (Op Amp)	300 μA
■ Wide supply voltage range	4V to 36V
■ Wide common-mode range	V^- to (V^+ − 1.8V)
■ Wide differential input voltage	±36V
■ Available in plastic package rated for Military Temp. Range Operation	

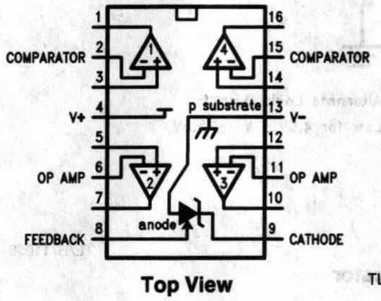
REFERENCE

■ Adjustable output voltage	1.2V to 6.3V
■ Tight initial tolerance available	±0.6%
■ Wide operating current range	17 μA to 20 mA
■ Tolerant of load capacitance	

Applications

- Transducer bridge driver
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

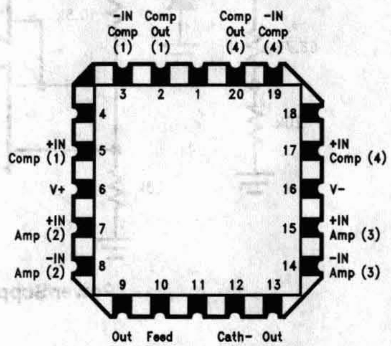
Connection Diagrams


1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
COMPARATOR
COMPARATOR
V+
V−
p substrate
OP AMP
OP AMP
FEEDBACK
CATHODE
anode
1
2
3
4

Top View

TL/H/9226–1

E Package Pinout


−IN Comp (1)
Comp Out (1)
Comp Out (4)
−IN Comp (4)
3
2
1
20
19
4
18
+IN Comp (1)
5
17
+IN Comp (4)
V+
6
16
V−
+IN Amp (2)
7
15
+IN Amp (3)
−IN Amp (2)
8
14
−IN Amp (3)
9
10
11
12
13
Out Amp (2)
Feed Back
Cath-ode
Out Amp (3)

TL/H/9226–48

Ordering Information

Reference Tolerance & V_{OS}	Temperature Range			Package	NSC Drawing
	Military −55°C ≤ T_A ≤ +125°C	Industrial −40°C ≤ T_A ≤ +85°C	Commercial 0°C ≤ T_A ≤ +70°C		
±0.6% 80 ppm/°C Max. V_{OS} ≤ 3.5 mV	LM613AMN	LM613AIN	—	16-Pin Molded DIP	N16E
	LM613AMJ/883 (Note 14)	—	—	16-Pin Ceramic DIP	J16A
	LM613AME/883 (Note 14)	—	—	20-Pin LCC	E20A
±2.0% 150 ppm/°C Max. V_{OS} ≤ 5.0 mV Max.	LM613MN	LM613IN	LM613CN	16-Pin Molded DIP	N16E
	—	LM613IWM		16-Pin Wide Surface Mount	M16B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except V_R (referred to V^- pin)	
(Note 2)	36V (Max)
(Note 3)	−0.3V (Min)
Current through Any Input Pin & V_R Pin	±20 mA
Differential Input Voltage	
Military and Industrial	±36V
Commercial	±32V
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Maximum Junction Temperature (Note 4)	150°C
Thermal Resistance, Junction-to-Ambient (Note 5)	
N Package	100°C/W
WM Package	150°C/W
Soldering Information (10 Seconds)	
N Package	260°C
WM Package	220°C
ESD Tolerance (Note 6)	±1 kV

Operating Temperature Range

LM613AI, LM613BI	−40°C to +85°C
LM613AM, LM613M	−55°C to +125°C
LM613C	$0°C \le T_J \le +70°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ (32V for LM613C)	450 **550**	940 **1000**	1000 **1070**	μA (Max) μA (Max)
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	2.8 **3**	V (Min) V (Min)
			46 **43**	36 **36**	32 **32**	V (Max) V (Max)
OPERATIONAL AMPLIFIERS						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$ ($4V \le V^+ \le 32V$ for LM613C)	1.5 **2.0**	3.5 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
V_{OS2}	V_{OS} Over V_{CM}	$V_{CM} = 0V$ through $V_{CM} =$ $(V^+ - 1.8V)$, $V^+ = 30V$, $V^- = 0V$	1.0 **1.5**	3.5 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 8)	**15**			μV/°C (Max)
I_B	Input Bias Current		10 **11**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
$\frac{I_{OS1}}{\Delta T}$	Average Offset Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1000			MΩ
C_{IN}	Input Capacitance	Common-Mode	6			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection Ratio	$V^+ = 30V$, $0V \le V_{CM} \le (V^+ - 1.8V)$ $CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	95 **90**	80 **75**	75 **70**	dB (Min) dB (Min)
PSRR	Power Supply Rejection Ratio	$4V \le V^+ \le 30V$, $V_{CM} = V^+/2$, $PSRR = 20 \log (\Delta V^+/V_{OS})$	110 **100**	80 **75**	75 **70**	dB (Min) dB (Min)
A_V	Open Loop Voltage Gain	$R_L = 10\ k\Omega$ to GND, $V^+ = 30V$, $5V \le V_{OUT} \le 25V$	500 **50**	100 **40**	94 **40**	V/mV (Min)

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over **Operating Temperature Range.** (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
OPERATIONAL AMPLIFIERS (Continued)						
SR	Slew Rate	$V^+ = 30V$ (Note 9)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/μs
GBW	Gain Bandwidth	$C_L = 50\ pF$	0.8 **0.5**			MHz MHz
V_{O1}	Output Voltage Swing High	$R_L = 10\ k\Omega$ to GND, $V^+ = 36V$ (32V for LM613C)	$V^+ - 1.4$ $\mathbf{V^+ - 1.6}$	$V^+ - 1.7$ $\mathbf{V^+ - 1.9}$	$V^+ - 1.8$ $\mathbf{V^+ - 1.9}$	V (Min) V (Min)
V_{O2}	Output Voltage Swing Low	$R_L = 10\ k\Omega$ to V^+, $V^+ = 36V$ (32V for LM613C)	$V^- + 0.8$ $\mathbf{V^- + 0.9}$	$V^- + 0.9$ $\mathbf{V^- + 1.0}$	$V^- + 0.95$ $\mathbf{V^- + 1.0}$	V (Max) V (Max)
I_{OUT}	Output Source Current	$V_{OUT} = 2.5V$, $V^+_{IN} = 0V$, $V^-_{IN} = -0.3V$	25 **15**	20 **13**	16 **13**	mA (Min) mA (Min)
I_{SINK}	Output Sink Current	$V_{OUT} = 1.6V$, $V^+_{IN} = 0V$, $V^-_{IN} = 0.3V$	17 **9**	14 **8**	13 **8**	mA (Min) mA (Min)
I_{SHORT}	Short Circuit Current	$V_{OUT} = 0V$, $V^+_{IN} = 3V$, $V^-_{IN} = 2V$	30 **40**	50 **60**	50 **60**	mA (Max) mA (Max)
		$V_{OUT} = 5V$, $V^+_{IN} = 2V$, $V^-_{IN} = 3V$	30 **32**	60 **80**	70 **90**	mA (Max) mA (Max)
COMPARATORS						
V_{OS}	Offset Voltage	$4V \leq V^+ \leq 36V$ (32V for LM613C), $R_L = 15\ k\Omega$	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{V_{CM}}$	Offset Voltage over V_{CM}	$0V \leq V_{CM} \leq 36V$ $V^+ = 36V$, (32V for LM613C)	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			μV/°C (Max)
I_B	Input Bias Current		5 **8**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
A_V	Voltage Gain	$R_L = 10\ k\Omega$ to 36V (32V for LM613C) $2V \leq V_{OUT} \leq 27V$	500 **100**			V/mV V/mV
t_r	Large Signal Response Time	$V^+_{IN} = 1.4V$, V^-_{IN} = TTL Swing, $R_L = 5.1\ k\Omega$	1.5 **2.0**			μs μs
I_{SINK}	Output Sink Current	$V^+_{IN} = 0V$, $V^-_{IN} = 1V$, $V_{OUT} = 1.5V$	20 **13**	10 **8**	10 **8**	mA (Min) mA (Min)
		$V_{OUT} = 0.4V$	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA (Min) mA (Min)
I_{LEAK}	Output Leakage Current	$V^+_{IN} = 1V$, $V^-_{IN} = 0V$, $V_{OUT} = 36V$ (32V for LM613C)	0.1 **0.2**	10	10	μA (Max) μA (Max)

Electrical Characteristics These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over **Operating Temperature Range**. (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
VOLTAGE REFERENCE						
V_R	Voltage Reference	(Note 10)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V (Min) V (Max)
$\frac{\Delta V_R}{\Delta T}$	Average Temp. Drift	(Note 11)	**10**	**80**	**150**	ppm/°C (Max)
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 12)	**3.2**			µV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV (Max) mV (Max)
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 13)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV (Max) mV (Max)
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}/9.9\ mA$ $\Delta V_{R(100 \rightarrow 17\ \mu A)}/83\ \mu A$	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω (Max) Ω (Max)
$\frac{V_R}{\Delta V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro = Vr)} - V_{R(Vro = 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV (Max) mV (Max)
$\frac{V_R}{\Delta V^+}$	V_R Change with V_{ANODE} Change	$V_{R(V^+ = 5V)} - V_{R(V^+ = 36V)}$ ($V^+ = 32V$ for LM613C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV (Max) mV (Max)
		$V_{R(V^+ = 5V)} - V_{R(V^+ = 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV (Max) mV (Max)
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \leq V_{FB} \leq 5.06V$	22 **29**	35 **40**	50 **55**	nA (Max) nA (Max)
e_n	V_R Noise	10 Hz to 10 kHz, $V_{RO} = V_R$	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Simultaneous short-circuit of multiple comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D\ \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 90°C/W for the N package, and 135°C/W for the WM package.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for $T_J = 25°C$; values in **bold face type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold type face).**

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @ 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 10: V_R is the Cathode-to-feedback voltage, nominally 1.244V.

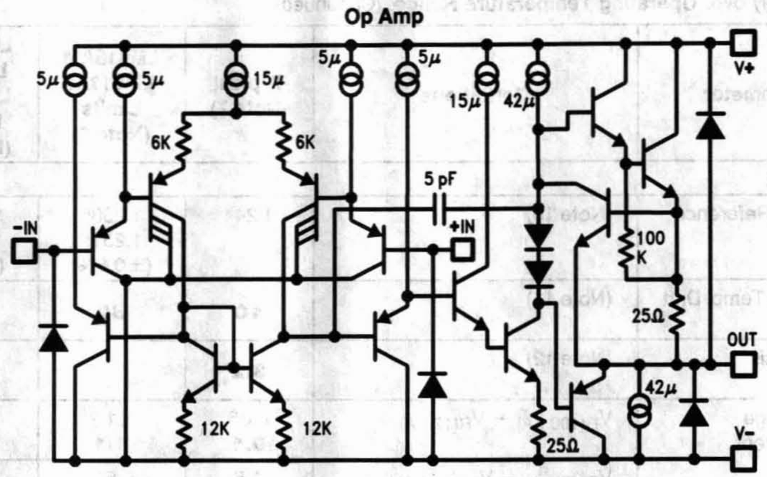
Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R/(V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 12: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 13: Low contact resistance is required for accurate measurement.

Note 14: A military RETS 613AMX electrical test specification is available on request. The Military screened parts can also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams


Op Amp
5µ
5µ
15µ
5µ
5µ
15µ
42µ
V+
6K
6K
5 pF
-IN
+IN
100 K
25Ω
OUT
42µ
12K
12K
25Ω
V−

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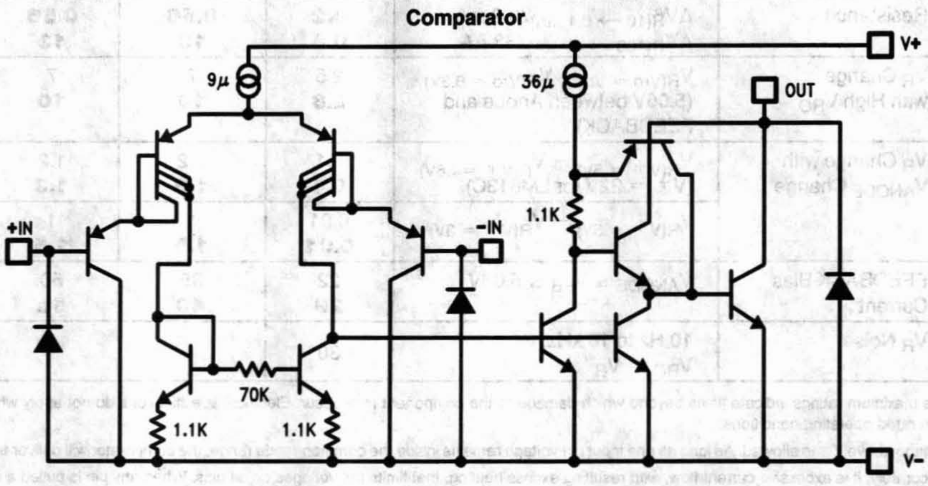
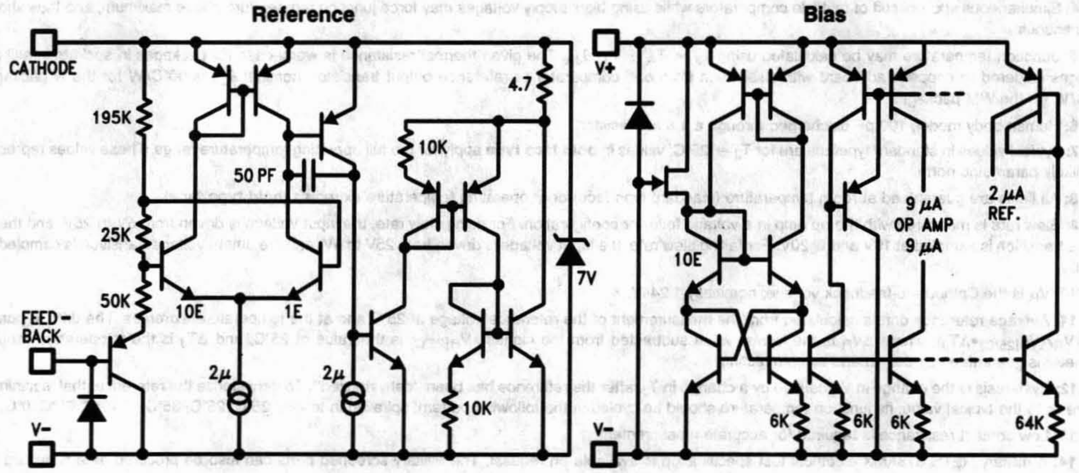

Comparator
V+
9µ
36µ
OUT
+IN
-IN
1.1K
70K
1.1K
1.1K
V−

TL/H/9226-3

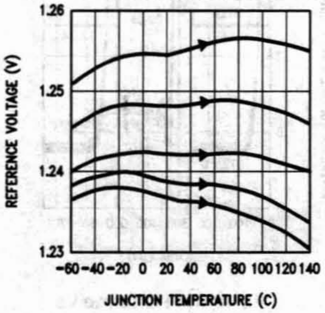

Reference
CATHODE
4.7
195K
10K
50 PF
25K
7V
50K
10E
1E
FEED-BACK
2µ
2µ
10K
V−
Bias
V+
9 µA OP AMP
9 µA
2 µA REF.
10E
6K
6K
6K
64K
V−

TL/H/9226-4

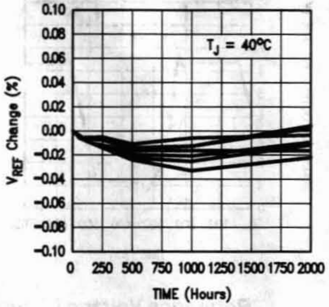
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

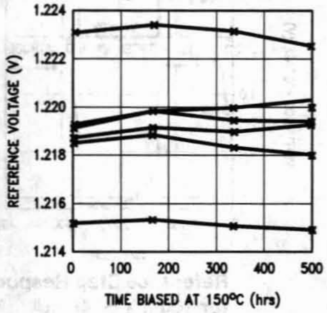
Reference Voltage vs Temp.



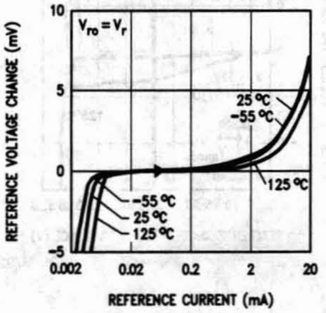
Reference Voltage Drift



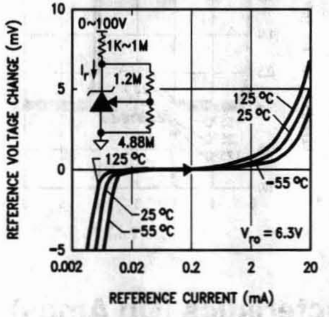
Accelerated Reference Voltage Drift vs Time



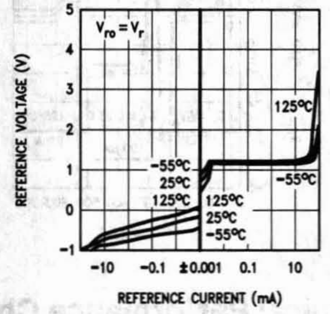
Reference Voltage vs Current and Temperature



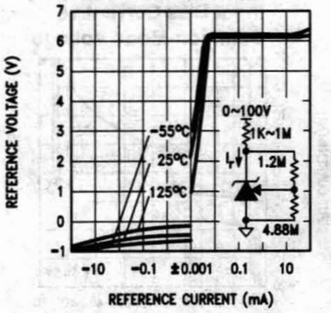
Reference Voltage vs Current and Temperature



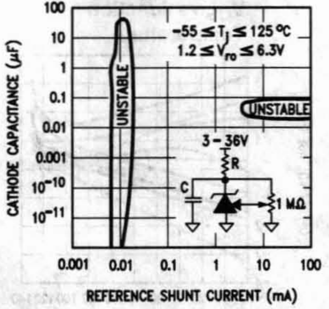
Reference Voltage vs Reference Current



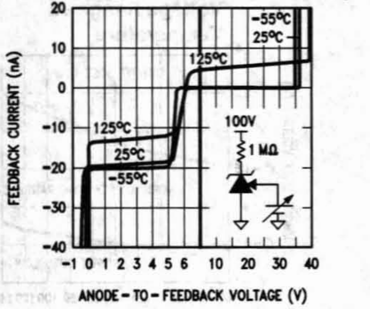
Reference Voltage vs Reference Current



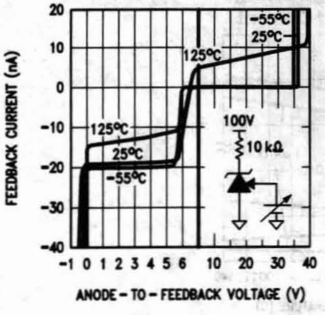
Reference AC Stability Range



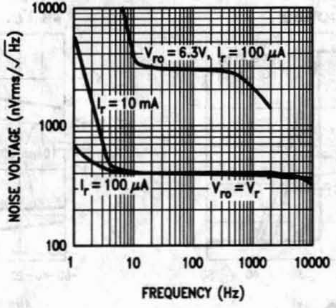
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



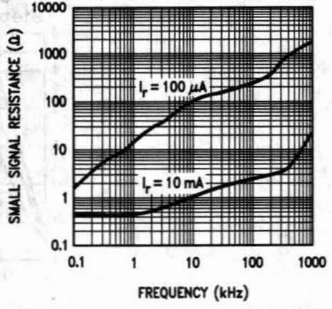
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency



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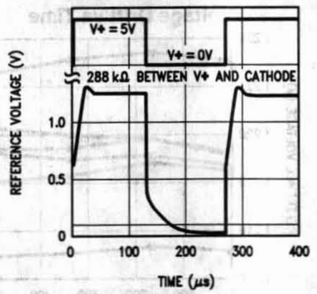
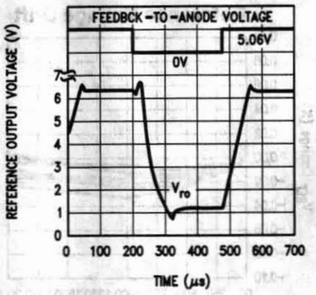
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

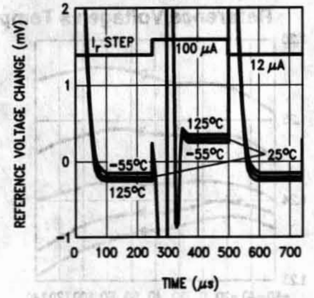
Reference Power-Up Time



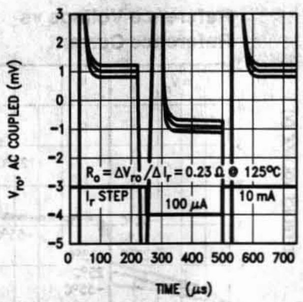
Reference Voltage with FEEDBACK Voltage Step



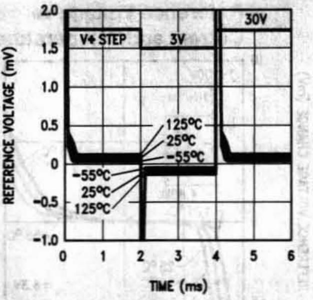
Reference Voltage with 100 ~ 12 µA Current Step



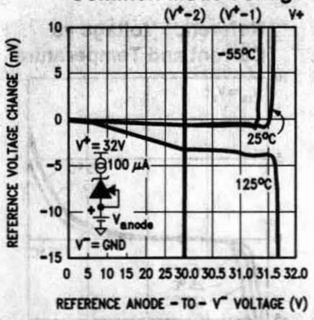
Reference Step Response for 100 µA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step



Reference Change vs Common-Mode Voltage

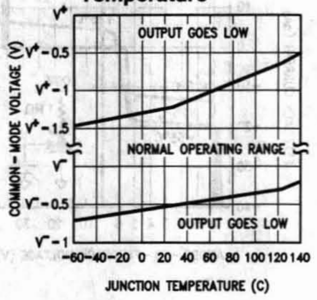


TL/H/9226-6

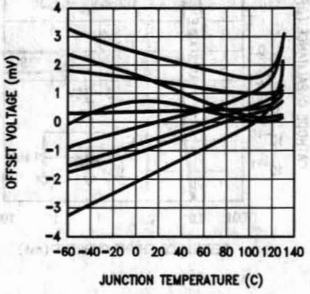
Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = 0V, V_{CM} = $V^+/2$, V_{OUT} = $V^+/2$, T_J = 25°C, unless otherwise noted

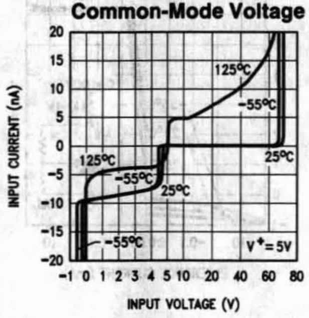
Input Common-Mode Voltage Range vs Temperature



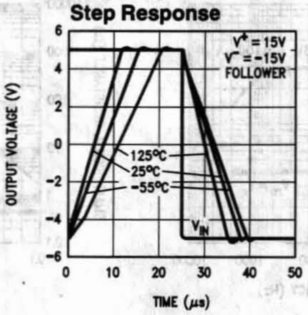
V_{OS} vs Junction Temperature



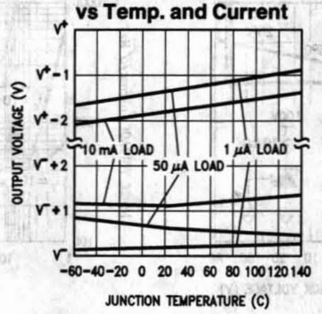
Input Bias Current vs Common-Mode Voltage



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

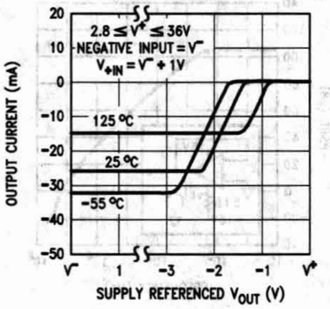


TL/H/9226-7

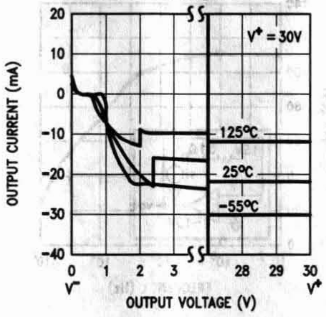
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

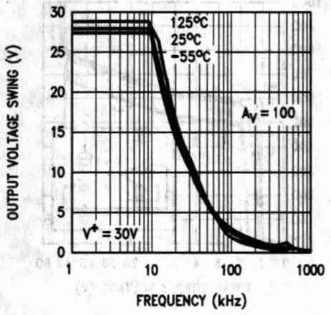
Output Source Current vs Output Voltage and Temp.



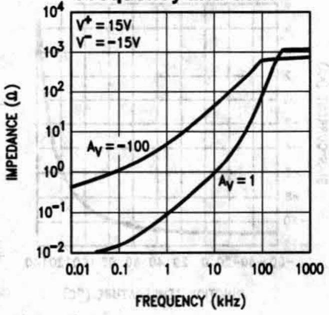
Output Sink Current vs Output Voltage



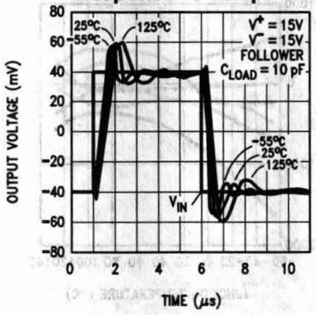
Output Swing, Large Signal



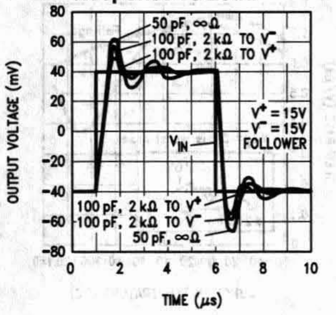
Output Impedance vs Frequency and Gain



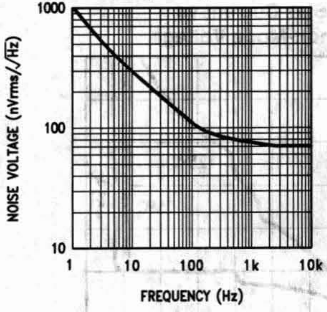
Small Signal Pulse Response vs Temp.



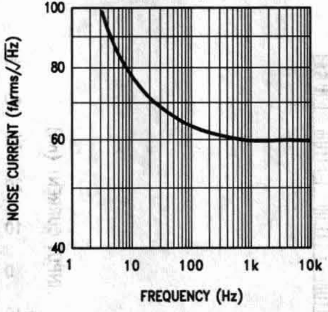
Small-Signal Pulse Response vs Load



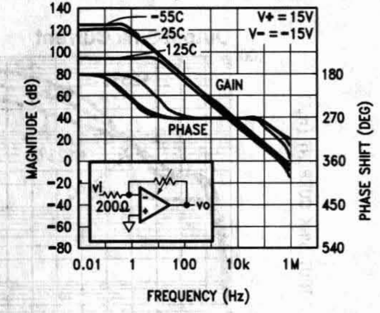
Op Amp Voltage Noise vs Frequency



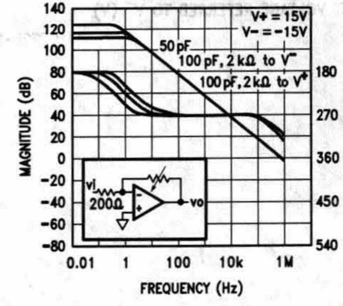
Op Amp Current Noise vs Frequency



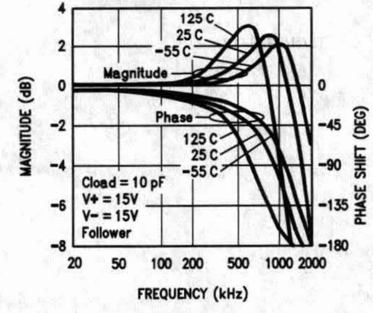
Small-Signal Voltage Gain vs Frequency and Temperature



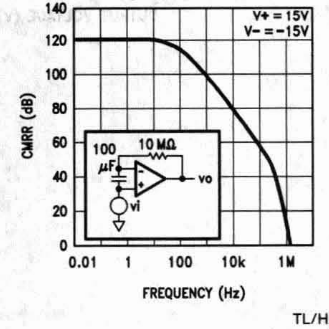
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

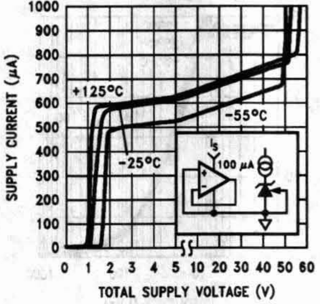


TL/H/9226–8

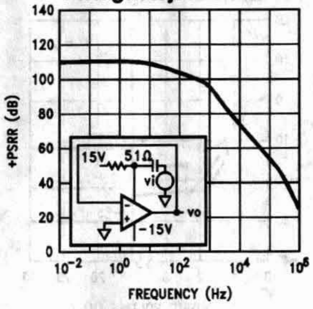
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V, V^- = GND = 0V, V_{CM} = V^+/2, V_{OUT} = V^+/2, T_J = 25°C$, unless otherwise noted

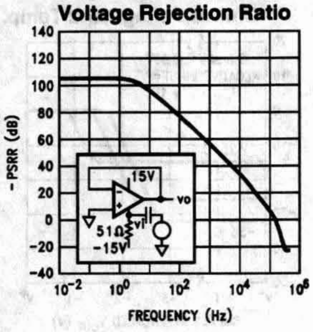
Power Supply Current vs Power Supply Voltage



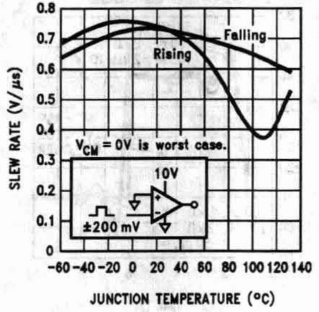
Positive Power Supply Voltage Rejection Ratio



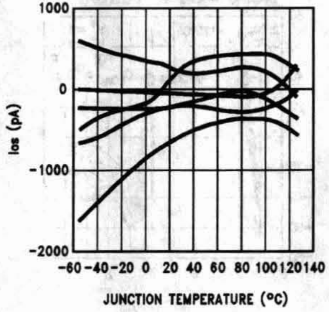
Negative Power Supply Voltage Rejection Ratio



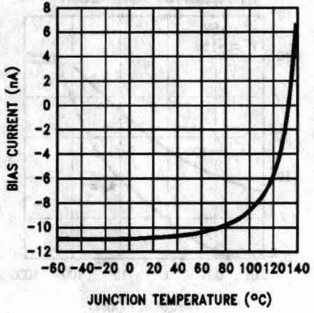
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature



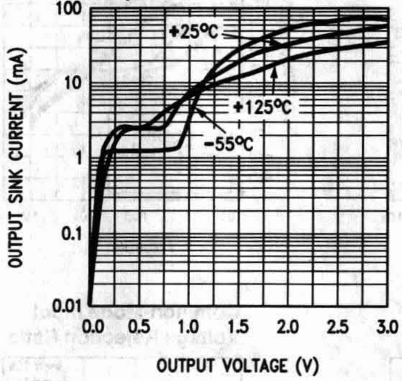
Input Bias Current vs Junction Temperature



TL/H/9226–9

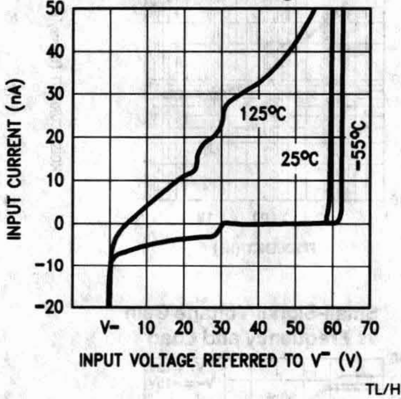
Typical Performance Characteristics (Comparators)

Output Sink Current



TL/H/9226–10

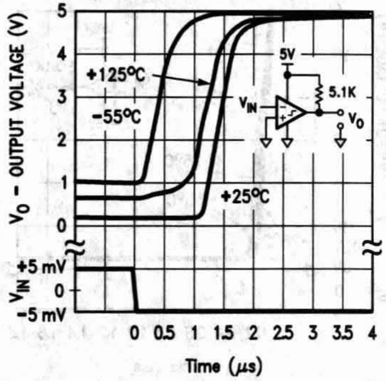
Input Bias Current vs Common-Mode Voltage



TL/H/9226–11

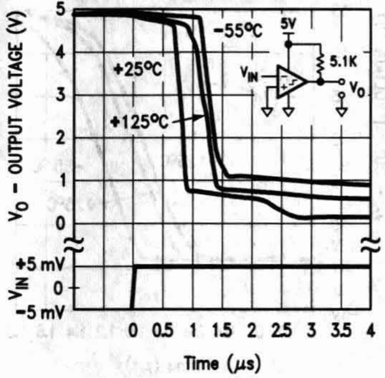
Typical Performance Characteristics (Comparators) (Continued)

Comparator Response Times—Inverting Input, Positive Transition



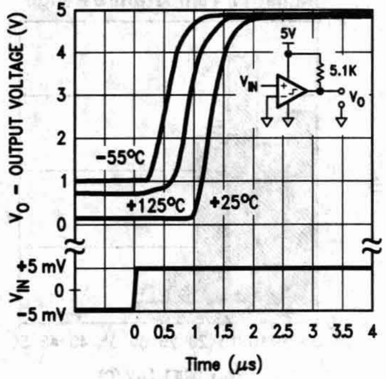
TL/H/9226–12

Comparator Response Times—Inverting Input, Negative Transition



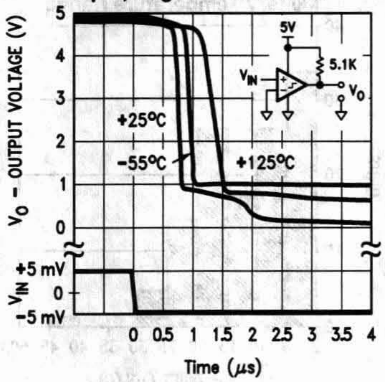
TL/H/9226–13

Comparator Response Times—Non-Inverting Input, Positive Transition



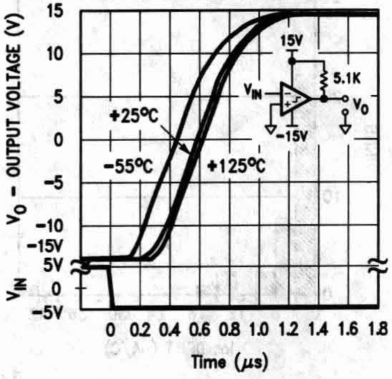
TL/H/9226–14

Comparator Response Times—Non-Inverting Input, Negative Transition



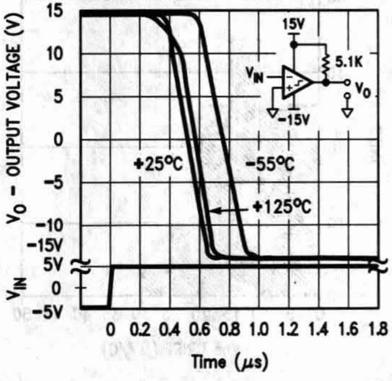
TL/H/9226–15

Comparator Response Times—Inverting Input, Positive Transition



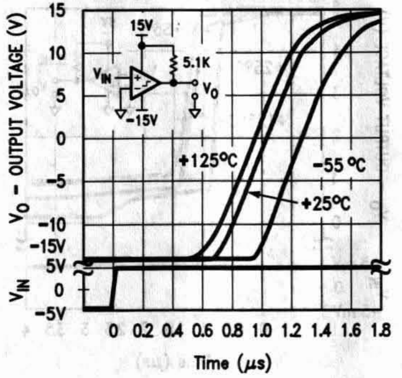
TL/H/9226–16

Comparator Response Times—Inverting Input, Negative Transition

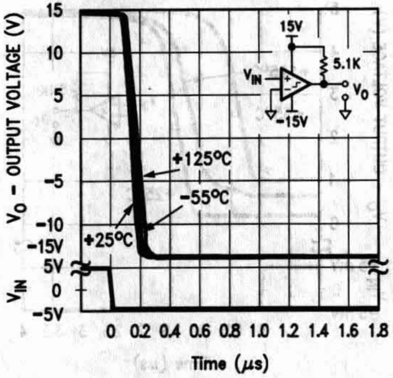


TL/H/9226–17

Typical Performance Characteristics (Comparators) (Continued)

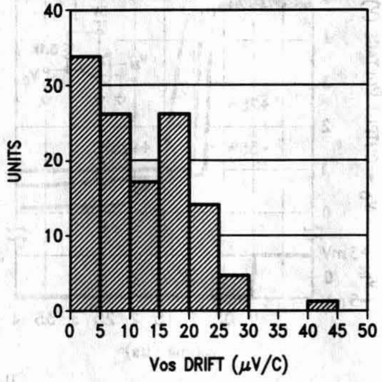

Comparator Response Times—Non-Inverting Input, Positive Transition

TL/H/9226–18

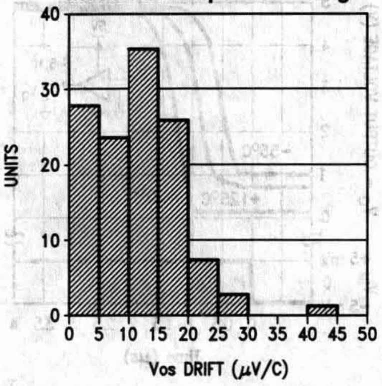

Comparator Response Times—Non-Inverting Input, Negative Transition

TL/H/9226–19

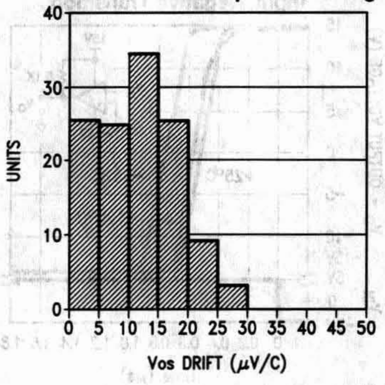
Typical Performance Distributions


Average V_{OS} Drift Military Temperature Range

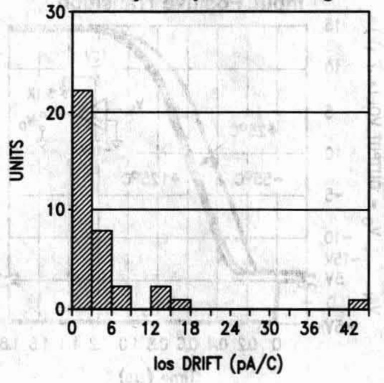
TL/H/9226–20


Average V_{OS} Drift Industrial Temperature Range

TL/H/9226–21

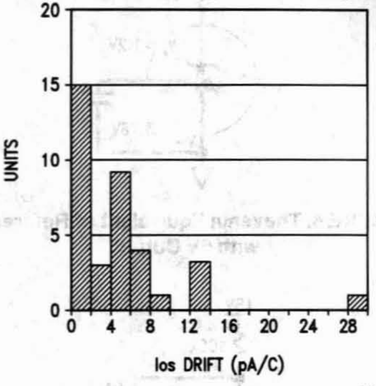

Average V_{OS} Drift Commercial Temperature Range

TL/H/9226–22

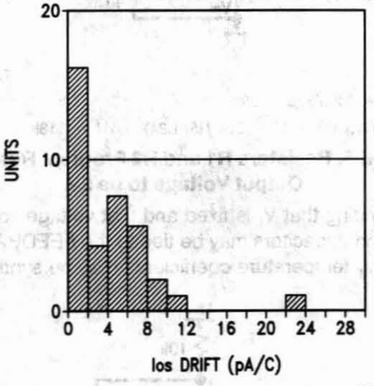

Average I_{OS} Drift Military Temperature Range

TL/H/9226–23

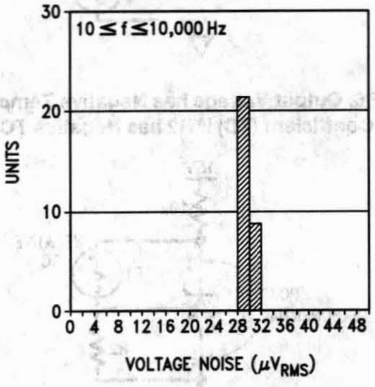
Typical Performance Distributions (Continued)


Average I_{OS} Drift Industrial Temperature Range

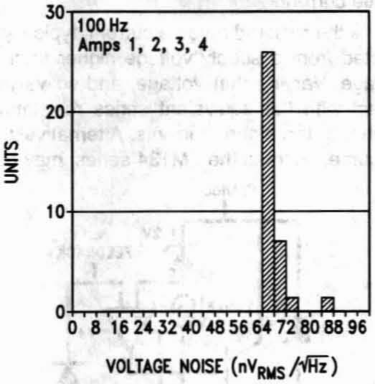
TL/H/9226-24


Average I_{OS} Drift Commercial Temperature Range

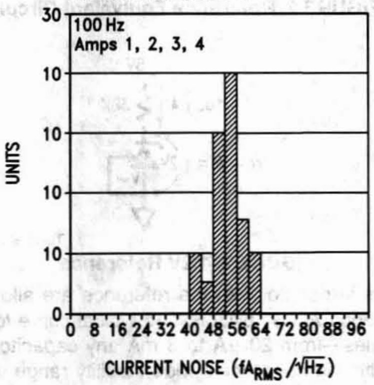
TL/H/9226-25


Voltage Reference Broad-Band Noise Distribution

TL/H/9226-26


Op Amp Voltage Noise Distribution

TL/H/9226-27


Op Amp Current Noise Distribution

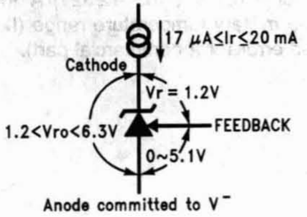
TL/H/9226-28

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ =$ 3V is allowed.



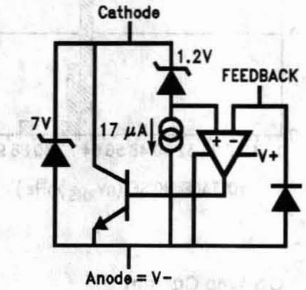
TL/H/9226-29

FIGURE 1. Voltage Associated with Reference (current source I_r is external)

Application Information (Continued)

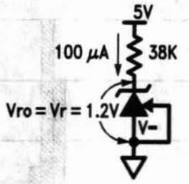
The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.



TL/H/9226-30

FIGURE 2. Reference Equivalent Circuit



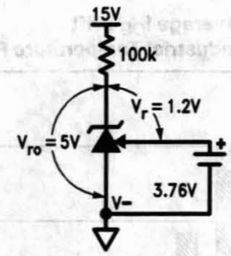
TL/H/9226-31

FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

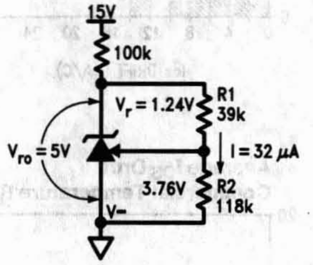
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constaint V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—$I \geq 32$ μA for the military grade over the military temperature range ($I \geq 5.5$ μA for a 1% untrimmed error for a commercial part).



TL/H/9226-32

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



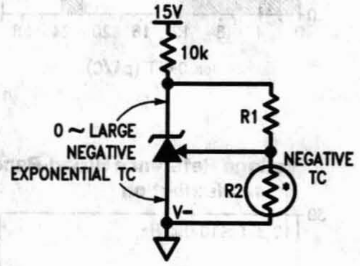
TL/H/9226-33

$R1 = Vr/I = 1.24/32\mu = 39k$

$R2 = R1\ \{(Vro/Vr) - 1\} = 39k\ \{(5/1.24) - 1)\} = 118k$

FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



TL/H/9226-34

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

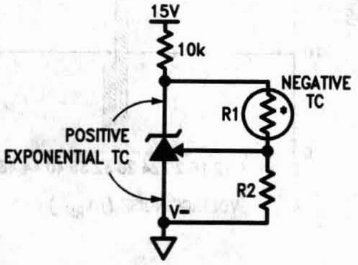


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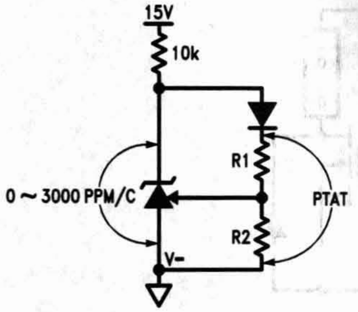
FIGURE 7. Output Voltage has Positive TC If R1 has Negative TC

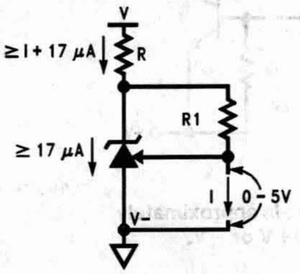
Application Information (Continued)



TL/H/9226–36

FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

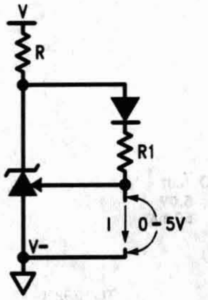
Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



TL/H/9226–37

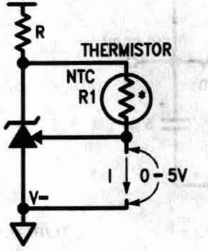
I = Vr/R1 = 1.24/R1

FIGURE 9. Current Source is Programmed by R1



TL/H/9226–38

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9226–39

FIGURE 11. Negative-TC Current Source

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS AND COMPARATORS

Any amp, comparator, or the reference may be biased in any way with no effect on the other sections of the LM613, except when a substrate diode conducts (see Electrical Characteristics Note 1). For example, one amp input may be outside the common-mode range, another amp may be operating as a comparator, and all other sections may have all terminals floating with no effect on the others. Tying inverting input to output and non-inverting input to V^- on unused amps is preferred. Unused comparators should have non-inverting input and output tied to V^+, and inverting input tied to V^-. Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like the LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 µA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 µA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.
2) Cross-Over Distortion: The LM613 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Comparator Output Stage

The comparators, like the LM139 series, have open-collector output stages. A pull-up resistor must be added from each output pin to a positive voltage for the output transistor to switch properly. When the output transistor is OFF, the output voltage will be this external positive voltage.

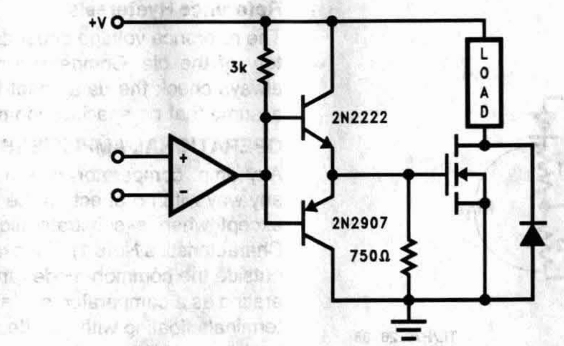
For the output voltage to be under the TTL-low voltage threshold when the output transistor is ON, the output current must be less than 8 mA (over temperature). This impacts the minimum value of pull-up resistor.

The offset voltage may increase when the output voltage is low and the output current is less than 30 µA. Thus, for best accuracy, the pull-up resistor value should be low enough to allow the output transistor to sink more than 30 µA.

Op Amp and Comparator Input Stage

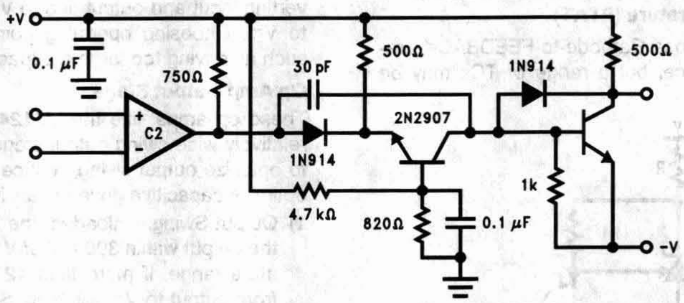
The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications


+V
3k
2N2222
2N2907
750Ω
L O A D

TL/H/9226-40

FIGURE 12. High Current, High Voltage Switch


+V
0.1 μF
750Ω
30 pF
500Ω
1N914
500Ω
C2
1N914
2N2907
4.7 kΩ
820Ω
0.1 μF
1k
−V

TL/H/9226-41

FIGURE 13. High Speed Level Shifter. Response time is approximately 1.5 μs, where output is either approximately +V or −V.

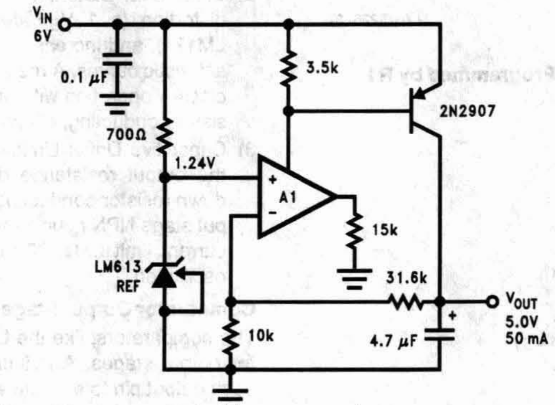

V_{IN} 6V
0.1 μF
3.5k
2N2907
700Ω
1.24V
A1
15k
LM613 REF
31.6k
V_{OUT} 5.0V 50 mA
10k
4.7 μF

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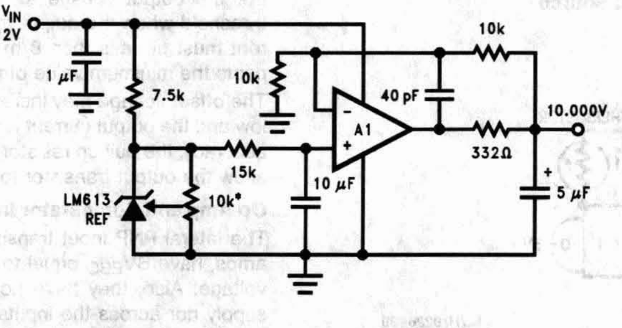
FIGURE 14. Low Voltage Regulator. Dropout voltage is approximately 0.2V.


V_{IN} 12V
1 μF
7.5k
10k
10k
40 pF
A1
10.000V
15k
332Ω
LM613 REF
10k*
10 μF
5 μF

*10k must be low t.c. trimpot

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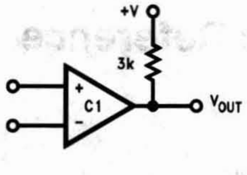
FIGURE 15. Ultra Low Noise, 10.00V Reference. Total output noise is typically 14 μV_{RMS}.

Typical Applications (Continued)



TL/H/9226-44

FIGURE 16. Basic Comparator

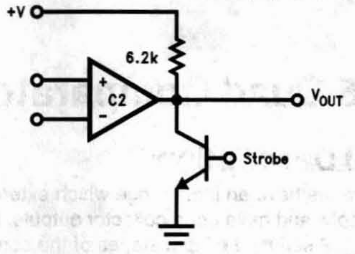

+V
6.2k
C2
+
−
VOUT
Strobe

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FIGURE 17. Basic Comparator with External Strobe

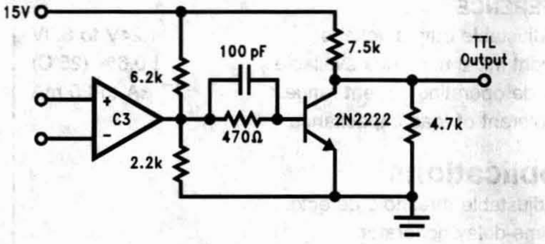
15V
6.2k
2.2k
C3
+
−
100 pF
470Ω
7.5k
TTL Output
2N2222
4.7k

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FIGURE 18. Wide-Input Range Comparator with TTL Output

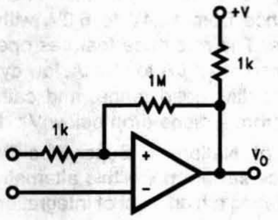

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FIGURE 19. Comparator with Hysteresis ($\Delta V_H = {}^{+}V(1k/1M)$)

National Semiconductor

LM615 Quad Comparator and Adjustable Reference

General Description

The comparators have an input range which extends to the negative supply, and have open-collector outputs. Improved over the LM139 series, the input stages of the comparators have lateral PNP input transistors which enable low input currents for large differential input voltages and swings above V+.

The voltage reference is a three-terminal shunt-type bandgap, and is referred to the V− terminal. Two resistors program the reference from 1.24V to 6.3V, with accuracy of ±0.6% available. The reference features operation over a shunt current range of 17 μA to 20 mA, low dynamic impedance, broad capacitive load range, and cathode terminal voltage ranging from a diode-drop below V− to above V+.

As a member of National's Super-Block™ family, the LM615 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features

COMPARATORS

■ Low operating current	600 μA
■ Wide supply voltage range	4V to 36V
■ Open-collector outputs	
■ Input common-mode range	V− to (V+ − 1.8V)
■ Wide differential input voltage	±36V

REFERENCE

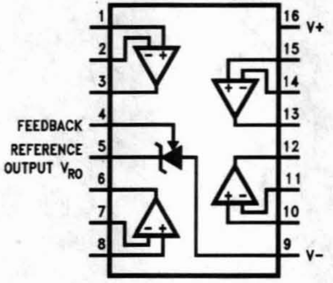
■ Adjustable output voltage	1.24V to 6.3V
■ Tight initial tolerance available	±0.6% (25°C)
■ Wide operating current range	17 μA to 20 mA
■ Tolerant of load capacitance	

Applications

- Adjustable threshold detector
- Time-delay generator
- Voltage window comparator
- Power supply monitor
- RGB level detector

Connection Diagram

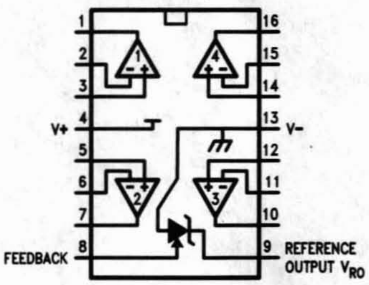
M Package



TL/H/11057-24

Top View

N Package



TL/H/11057-1

Top View

Ordering Information

For information about surface-mount packaging of this device, please contact the Analog Product Marketing group at National Semiconductor Corp. headquarters.

Reference Tolerances	Temperature Range		Package	NSC Package Number
	Military −55°C ≤ T_J ≤ +125°C	Industrial −40°C ≤ T_J ≤ +85°C		
±0.6% at 25°C, 80 ppm/°C max	LM615AMN	LM615AIN	16-Pin Molded DIP	N16A
	LM615AMJ/883 (Note 13)		16-Pin Ceramic DIP	J16A
±2.0% at 25°C, 150 ppm/°C max	LM615MN	LM615IN	16-Pin Molded DIP	N16A
		LM615IM	16-Pin Narrow Surface Mount	M16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except V_{RO} (referred to V− pin)	
(Note 2)	36V (Max)
(Note 3)	−0.3V (Min)
Current through Any Input Pin and V_{RO} Pin	±20 mA
Differential Input Voltage	±36V
Output Short-Circuit Duration	(Note 4)
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Maximum Junction Temperature	150°C
Thermal Resistance, Junction-to-Ambient (Note 5)	
N Package	95°C/W
Soldering Information	
N Package Soldering (10 seconds)	260°C
ESD Tolerance (Note 6)	±1 kV

Operating Temperature Range

LM615AI, LM615I	$-40°C \le T_J \le +85°C$
LM615A, LM615M	$-55°C \le T_J \le +125°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = V^+/2$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 7)	LM615AM LM615AI Limits (Note 8)	LM615M LM615I Limits (Note 8)	Units
COMPARATORS						
I_S	Total Supply Current	V^+ Current, $R_{LOAD} = \infty$, $3V \le V^+ \le 36V$	250 **350**	550 **600**	600 **650**	µA max µA max
V_{OS}	Offset Voltage over V^+ Range	$4V \le V^+ \le 36V$, $R_L = 15\ k\Omega$	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV max mV max
V_{OS}	Offset Voltage over V_{CM} Range	$0V \le V_{CM} \le (V^+ - 1.8V)$ $V^+ = 30V$, $R_L = 15\ k\Omega$	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV max mV max
$\frac{\Delta V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			µV/°C
I_B	Input Bias Current		−5 **−8**	25 **30**	35 **40**	nA max nA max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA max nA max
A_V	Voltage Gain	$R_L = 10\ k\Omega$ to 36V, $2V \le V_{OUT} \le 27V$	500 **100**	50	50	V/mV min V/mV
t_R	Large Signal Response Time	$V_{+IN} = 1.4V$, $V_{-IN} =$ TTL Swing, $R_L = 5.1\ k\Omega$	1.5 **2.0**			µs µs
I_{SINK}	Output Sink Current	$V_{+IN} = 0V$, $V_{-IN} = 1V$, $V_{OUT} = 1.5V$	20 **13**	10 **8**	10 **8**	mA min mA min
		$V_{OUT} = 0.4V$	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA min mA min
I_L	Output Leakage Current	$V_{+IN} = 1V$, $V_{-IN} = 0V$, $V_{OUT} = 36V$	0.1 **0.2**	10	10	µA max µA

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = V^+/2$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**. (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM615AM LM615AI Limits (Note 8)	LM615M LM615I Limits (Note 8)	Units
VOLTAGE REFERENCE (Note 9)						
V_R	Reference Voltage		1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V min V max
$\frac{\Delta V_R}{\Delta T}$	Average Drift with Temperature	(Note 10)	**18**	**80**	**150**	ppm/°C max
$\frac{\Delta V_R}{kH}$	Average Drift with Time	$T_J = 40°C$ $T_J = 150°C$	400 1000			ppm/kH ppm/kH
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 11)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R[100\ \mu A]} - V_{R[17\ \mu A]}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV max mV max
		$V_{R[10\ mA]} - V_{R[100\ \mu A]}$ (Note 12)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV max mV max
R	Resistance	$\Delta V_{R[10\ mA\ to\ 0.1\ mA]}/9.9\ mA$ $\Delta V_{R[100\ \mu A\ to\ 17\ \mu A]}/83\ \mu A$	0.2 0.6	**0.56** **13**	**0.56** **13**	Ω max Ω max
$\frac{\Delta V_R}{\Delta V_{RO}}$	V_R Change with V_{RO}	$V_{R[V_{RO} = V_R]} - V_{R[V_{RO} = 6.3V]}$	2.5 **2.8**	5 **10**	5 **10**	mV max mV max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R[V+ = 5V]} - V_{R[V+ = 36V]}$	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV max mV max
		$V_{R[V+ = 5V]} - V_{R[V+ = 3V]}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV max mV max
I_{FB}	FEEDBACK Bias Current	$V^- \leq V_{FB} \leq 5.06V$	22 **29**	35 **40**	50 **55**	nA max nA max
e_n	Voltage Noise	BW = 10 Hz to 10 kHz	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Shorting an Output to V^- will not cause power dissipation, so it may be continuous. However, shorting an Output to any more positive voltage (including V^+), will cause 80 mA (typ.) to be drawn through the output transistor. This current multiplied by the applied voltage is the power dissipation in the output transistor. If the total power from all shorted outputs causes the junction temperature to exceed 150°C, degraded reliability or destruction of the device may occur. To determine junction temperature, see Note 5.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D\ \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 80 °C/W for the N package.

Note 6: Human body model, 100 pF discharge through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed for $T_J = +25°C$ (standard type face) or over the full operating temperature range **(bold type face)**.

Note 9: V_{RO} is the reference output voltage, which may be set for 1.2V to 6.3V (see Application Information). V_R is the V_{RO}-to-FEEDBACK voltage (nominally 1.244V).

Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R/V_{R[25°C]} \bullet \Delta T_J$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

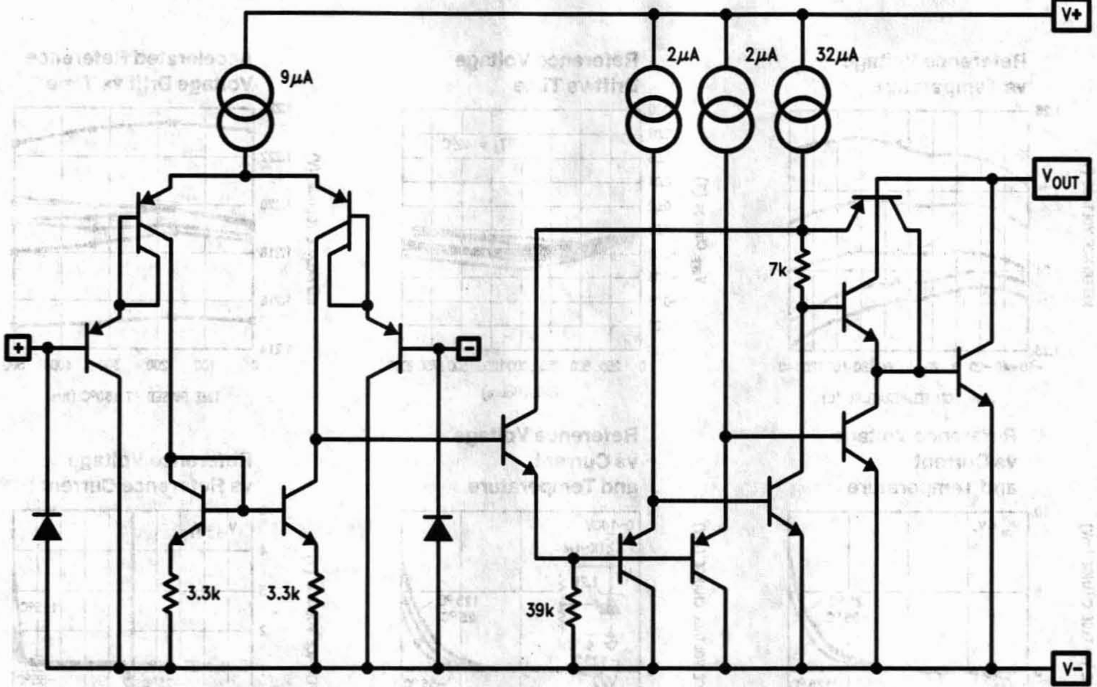
Note 11: Hysteresis is the change in V_{RO} caused by a change in T_J, after the reference has been "dehysterized." To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 12: Low contact resistance is required for accurate measurement.

Note 13: A military RETS electrical test specification is available on request. The LM615AMJ/883 may also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams

Comparator


V+
9μA
2μA
2μA
32μA
V_OUT
7k
+
−
3.3k
3.3k
39k
V−

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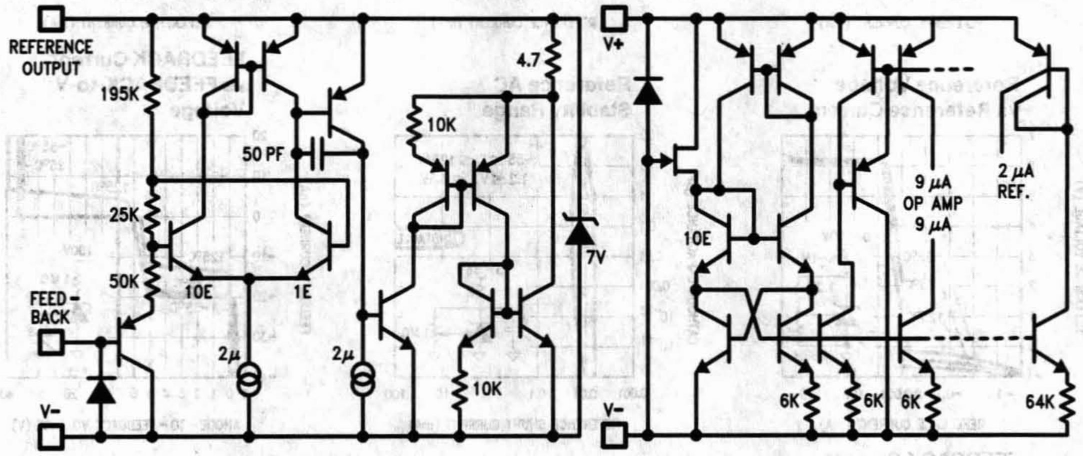
Reference

Bias

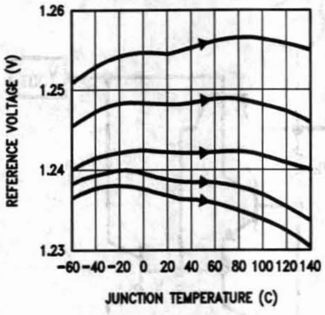

REFERENCE OUTPUT
195K
50 PF
4.7
10K
25K
7V
50K
10E
1E
FEED-BACK
2μ
2μ
10K
V−
V+
10E
9 μA OP AMP 9 μA
2 μA REF.
6K
6K
6K
64K
V−

TL/H/11057-3

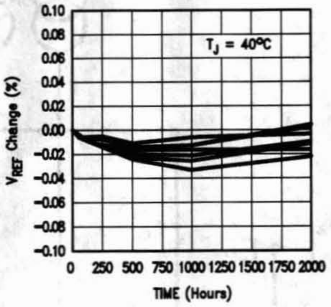
Typical Performance Characteristics (Reference)

$T_J = 25°C$, FEEDBACK pin shorted to $V^- = 0V$, unless otherwise noted.

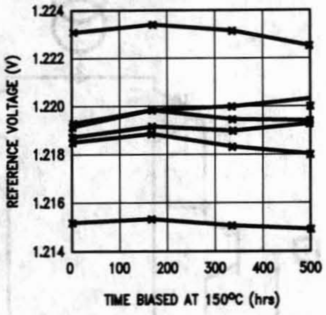
Reference Voltage vs Temperature



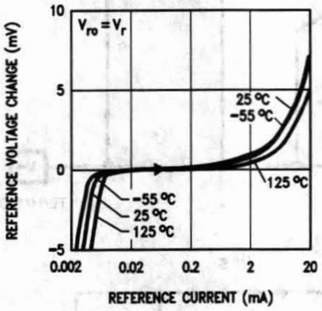
Reference Voltage Drift vs Time



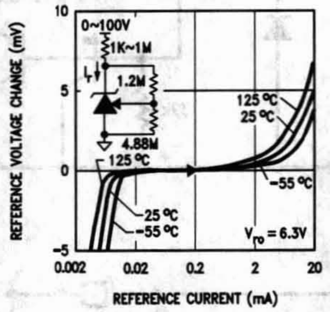
Accelerated Reference Voltage Drift vs Time



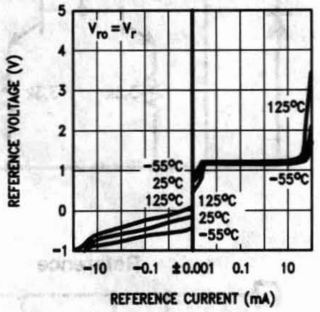
Reference Voltage vs Current and Temperature



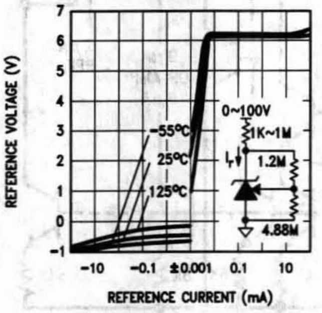
Reference Voltage vs Current and Temperature



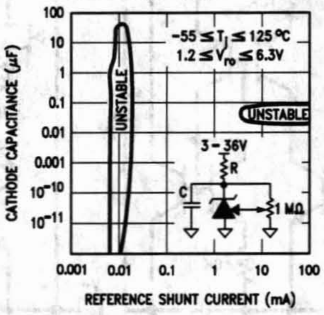
Reference Voltage vs Reference Current



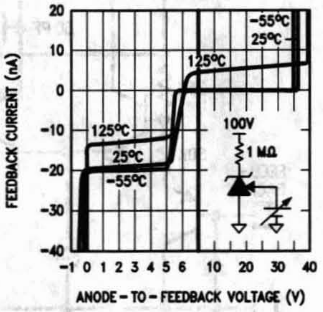
Reference Voltage vs Reference Current



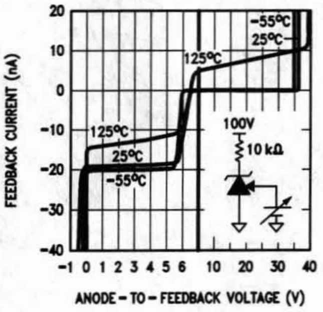
Reference AC Stability Range



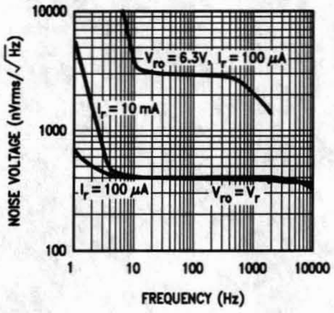
FEEDBACK Current vs FEEDBACK-to-V⁻ Voltage



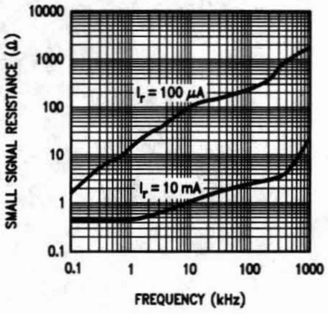
FEEDBACK Current vs FEEDBACK-to-V⁻ Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency

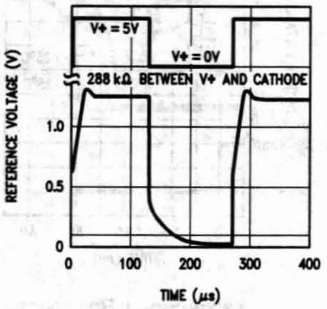


TL/H/11057–4

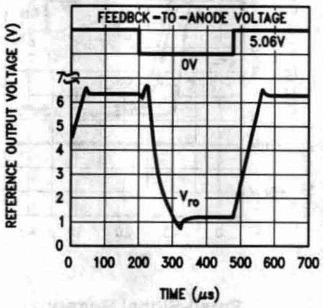
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted.

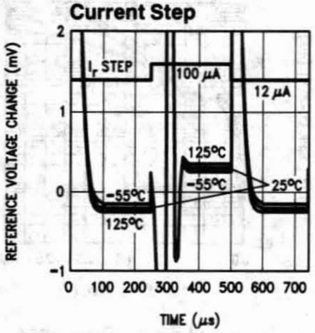
Reference Power-Up Time



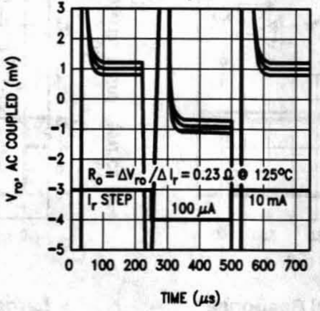
Reference Voltage with FEEDBACK Voltage Step



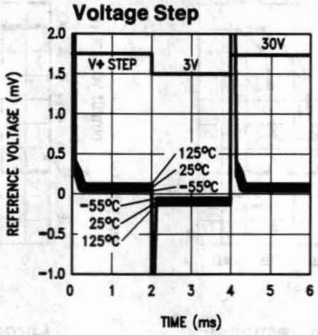
Reference Voltage with 100 ~ 12 µA Current Step



Reference Step Response for 100 µ ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step

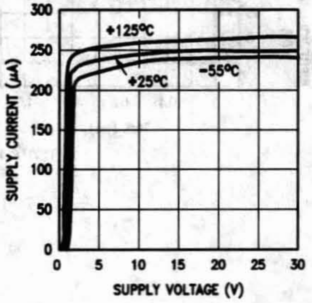


TL/H/11057–5

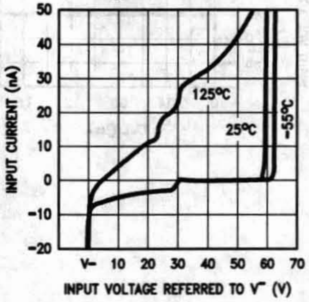
Typical Performance Characteristics (Comparators)

T_J = 25°C, V^+ = 5V, V^- = 0V, unless otherwise noted

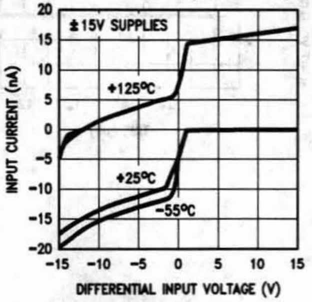
Supply Current vs Supply Voltage



Input-Bias Current vs Common-Mode Voltage



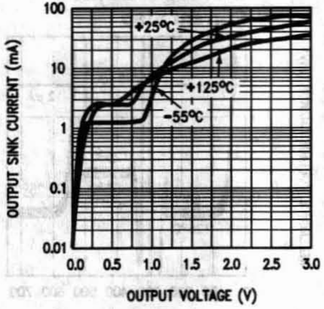
Input Current vs Differential Input Voltage



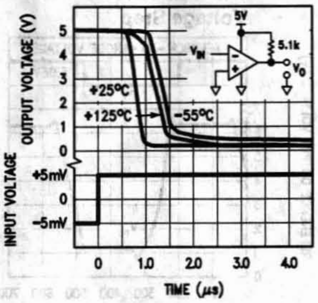
TL/H/11057–6

Typical Performance Characteristics (Comparators) (Continued)

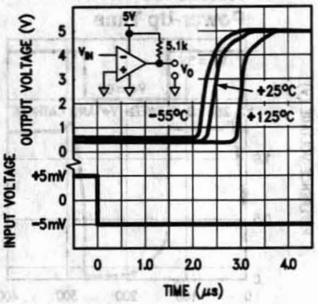
Output Saturation Voltage vs Sink Current



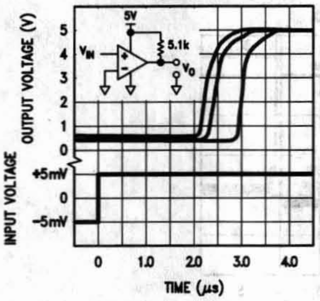
Small-Signal Response Times—Inverting Input, Negative Transition



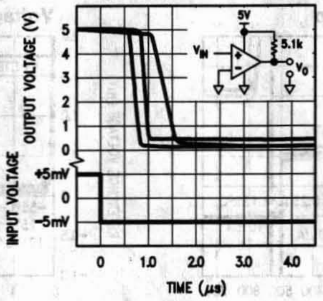
Small-Signal Response Times—Inverting Input, Positive Transition



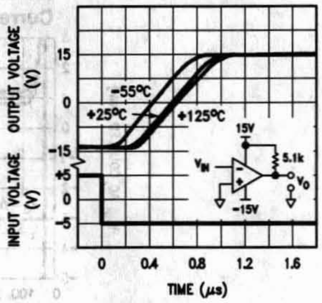
Small-Signal Response Times Non-Inverting Input, Positive Transition



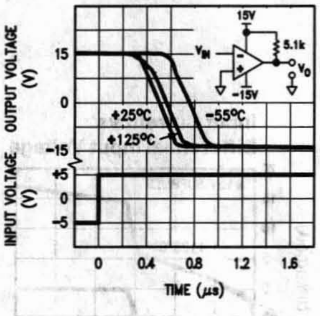
Small-Signal Response Times—Non-Inverting Input, Negative Transition



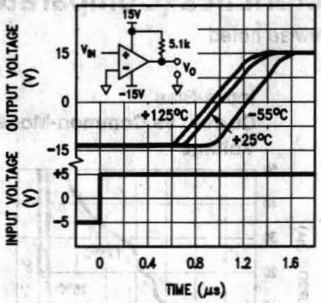
Large-Signal Response Times—Inverting Input, Positive Transition



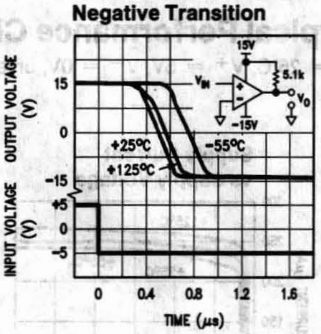
Large-Signal Response Times-Inverting Input, Negative Transition



Large-Signal Response Times—Non-Inverting Input, Positive Transition



Large-Signal Response Times—Non-Inverting Input, Negative Transition



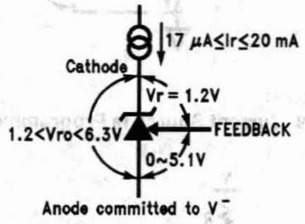
TL/H/11057–8

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with V^+ = 3V is allowed.



TL/H/11057–9

FIGURE 1. Voltage Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.

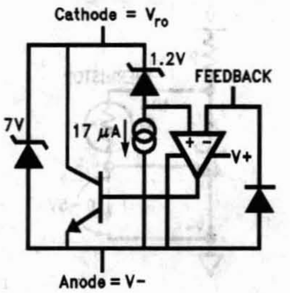


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FIGURE 2. Reference Equivalent Circuit

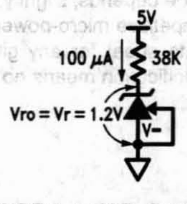

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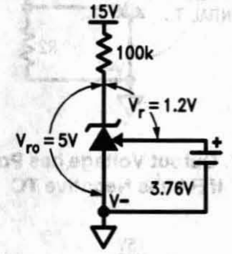
FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

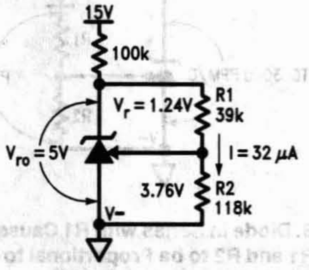
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for V_{ro} = 5V. Connecting a resistor across the constant V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with R2 = 3.76/I. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—I ≥ 32 μA for the military grade over the military temperature range (I ≥ 5.5 μA for a 1% untrimmed error for an industrial temperature range part).



TL/H/11057–12

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



TL/H/11057–13

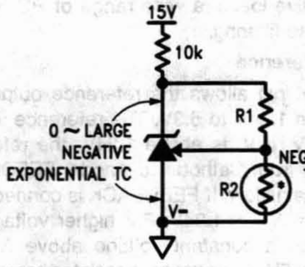
$R1 = V_r/I = 1.24/32\mu = 39k$

$R2 = R1\,[(V_{ro}/V_r) - 1] = 39k\,[(5/1.24) - 1] = 118k$

FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

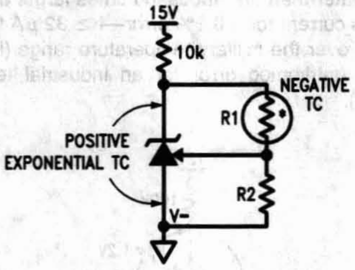
Application Information (Continued)

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.


15V
10k
R1
0 ~ LARGE NEGATIVE EXPONENTIAL TC
NEGATIVE TC
R2
V−

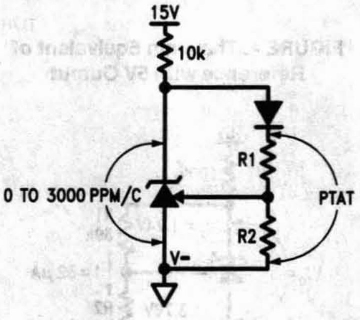
TL/H/11057-14

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC


15V
10k
NEGATIVE TC
R1
POSITIVE EXPONENTIAL TC
R2
V−

TL/H/11057-15

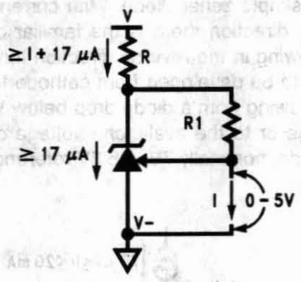
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC


15V
10k
R1
0 TO 3000 PPM/C
PTAT
R2
V−

TL/H/11057-16

FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

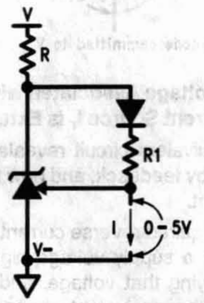
Connecting a resistor across V_{RO}-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.


V
≥ I + 17 μA
R
R1
≥ 17 μA
I
0 − 5V
V−

TL/H/11057-17

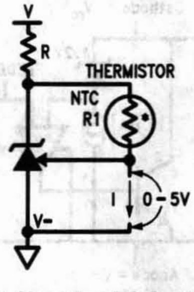
$I = V_r/R1 = 1.24/R1$

FIGURE 9. Current Source is Programmed by R1



TL/H/11057-18

FIGURE 10. Proportional-to-Absolute-Temperature Current Source


V
R
THERMISTOR
NTC
R1
I
0 − 5V
V−

TL/H/11057-19

FIGURE 11. Negative-TC Current Source

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

Application Information (Continued)

COMPARATORS

Any of the comparators or the reference may be biased in any way with no effect on the other sections of the LM615, except when a substrate diode conducts (see Electrical Characteristics Note 3). For example, one or both inputs of one comparator may be outside the input voltage range limits, the reference may be unpowered, and the other comparators will still operate correctly. Unused comparators should have inverting input and output tied to V$^-$, and non-inverting input tied to V$^+$.

Hysteresis

Any comparator may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis, or positive feedback, as shown in *Figure 12*.

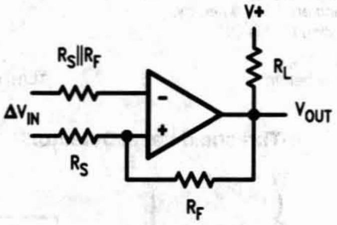


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FIGURE 12. R_S and R_F Add Hysteresis to Comparator

The amount of hysteresis added in *Figure 12* is

$$V_H = V^+ \times \frac{R_S}{(R_F + R_S)}$$

$$\approx V^+ \times \frac{R_S}{R_F} \quad \text{for } R_F \gg R_S$$

A good rule of thumb is to add hysteresis of at least the maximum specified offset voltage. More than about 50 mV of hysteresis can substantially reduce the accuracy of the comparator, since the offset voltage is effectively being increased by the hysteresis when the comparator output is high.

It is often a good idea to decrease the amount of hysteresis until oscillations are observed, then use three times that minimum hysteresis in the final circuit. Note that the amount of hysteresis needed is greatly affected by layout. The amount of hysteresis should be rechecked each time the layout is changed, such as changing from a breadboard to a P.C. board.

Input Stage

The input stage uses lateral PNP input transistors which, unlike those of many op amps, have breakdown voltage BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

The guaranteed common-mode input voltage range for an LM615 is $V^- \le V_{CM} \le (V^+ - 1.8V)$, over temperature. This is the voltage range in which the comparisons must be made. If both inputs are within this range, the output will be at the correct state. If one input is within this range, and the other input is less than $(V^- + 32V)$, even if this is greater than V$^+$, the output will be at the correct state. If, however, either or both inputs are driven below V$^-$, and either input current exceeds 10 µA, the output state is not guaranteed to be correct. If both inputs are above $(V^+ - 1.8V)$, the output state is also not guaranteed to be correct.

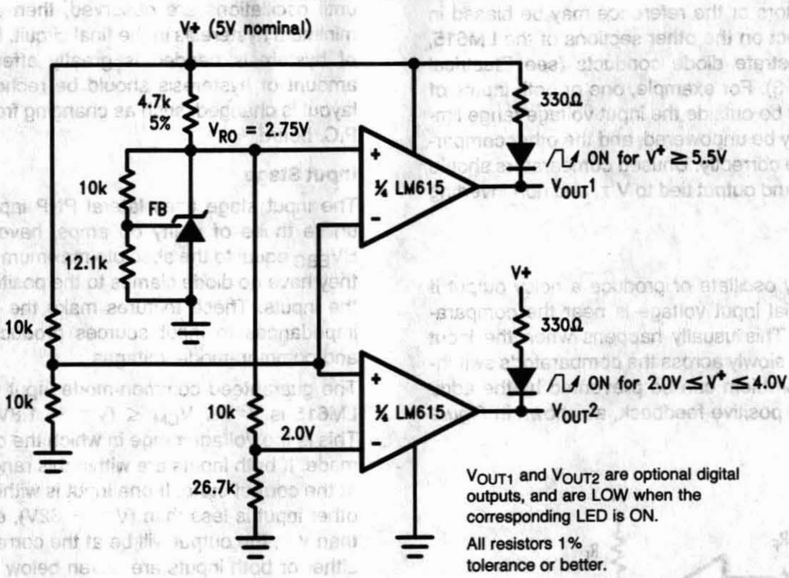
Output Stage

The comparators have open-collector output stages which require a pull-up resistor from each output pin to a positive supply voltage of the output to switch properly. When the internal output transistor is off, the output (HIGH) voltage will be pulled up to this external positive voltage.

To ensure that the LOW output voltage is under the TTL-low threshold, the output transistor's load current must be less than 0.8 mA (over temperature) when it turns on. This impacts the minimum value of the pull-up resistor.

Typical Applications

Power Supply Monitor


V+ (5V nominal)
4.7k
5%
V_{RO} = 2.75V
10k
FB
12.1k
10k
10k
10k
2.0V
26.7k
330Ω
ON for $V^+ \geq 5.5V$
$V_{OUT}1$
¼ LM615
V+
330Ω
ON for $2.0V \leq V^+ \leq 4.0V$
$V_{OUT}2$
¼ LM615

V_{OUT1} and V_{OUT2} are optional digital outputs, and are LOW when the corresponding LED is ON.

All resistors 1% tolerance or better.

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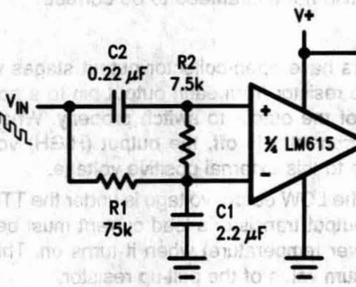
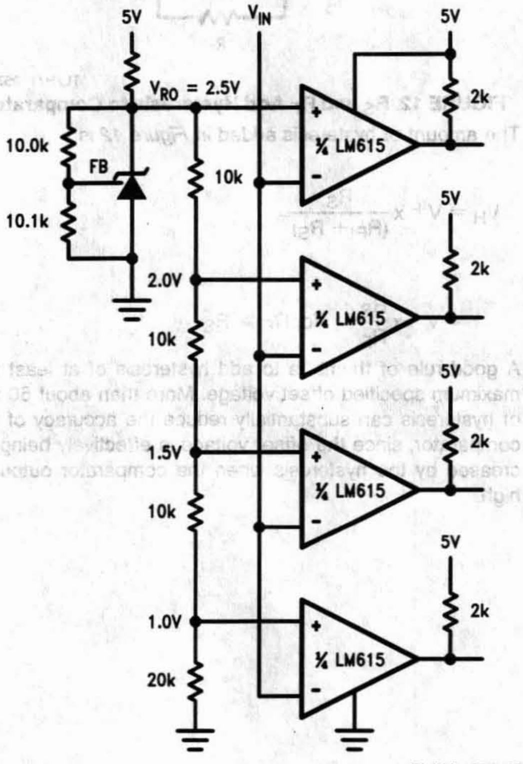
Tracking Comparator


V+
C2
0.22 µF
R2
7.5k
1k
V_{IN}
¼ LM615
V_{OUT}
R1
75k
C1
2.2 µF

TL/H/11057-22

R1–C1 removes the low-frequency signal component, so that through R2–C2 the higher-frequency component is detected.

4-Threshold Level Detector


5V
V_{IN}
5V
V_{RO} = 2.5V
10.0k
FB
10.1k
10k
2k
¼ LM615
5V
2.0V
2k
¼ LM615
10k
5V
1.5V
2k
¼ LM615
10k
5V
1.0V
2k
¼ LM615
20k

TL/H/11057-23

National Semiconductor

LM710 Voltage Comparator

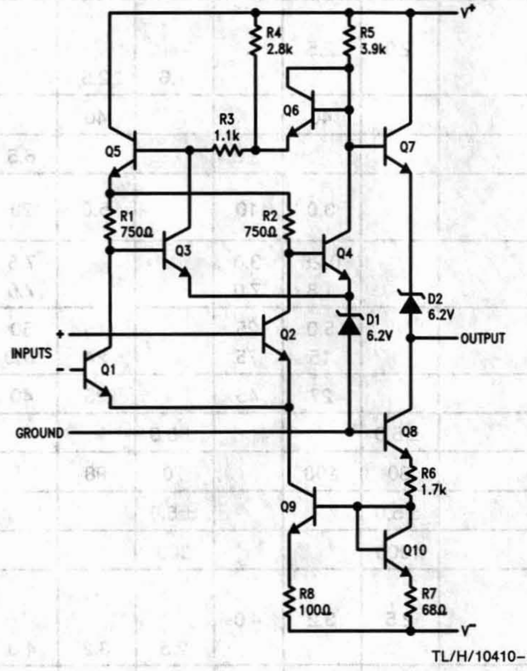
General Description

The LM710 series are high-speed voltage comparators intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

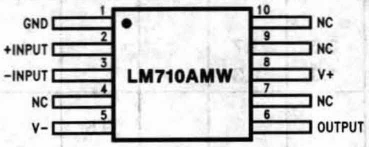
The LM710 series are useful as pulse height discriminators, voltage comparators in high-speed A/D converters or go, no-go detectors in automatic test equipment. They also have applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the units suggests them for applications replacing relatively simple discrete component circuitry.

Schematic and Connection Diagrams


V+
R4 2.8k
R5 3.9k
Q6
R3 1.1k
Q5
Q7
R1 750Ω
R2 750Ω
Q3
Q4
D2 6.2V
D1 6.2V
Q2
OUTPUT
+
INPUTS
-
Q1
GROUND
Q8
R6 1.7k
Q9
Q10
R8 100Ω
R7 68Ω
V−

TL/H/10410-1

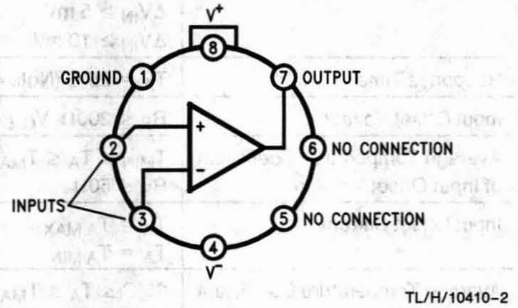
Ceramic Flatpak Package


GND 1
+INPUT 2
-INPUT 3
NC 4
V- 5
10 NC
9 NC
8 V+
7 NC
6 OUTPUT
LM710AMW

TL/H/10410-9

Order Number LM710AMW/883*
See NS Package Number W10A

Metal Can Package


V+
8
GROUND 1
7 OUTPUT
2
6 NO CONNECTION
INPUTS
3
5 NO CONNECTION
4
V−
+
−

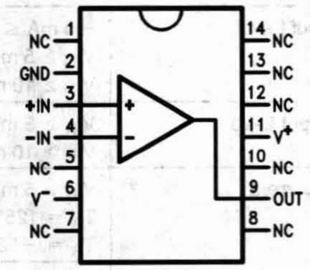
TL/H/10410-2

Top View

Note: Pin 4 is connected to case.

Order Number LM710AMH/883*, LM710H,
LM710H/883 or LM710CH
See NS Package Number H08C

Dual-In-Line Package


NC 1
GND 2
+IN 3
−IN 4
NC 5
V− 6
NC 7
14 NC
13 NC
12 NC
11 V+
10 NC
9 OUT
8 NC
+
−

TL/H/10410-3

Top View

Order Number
LM710AMJ/883* or LM710CN
See NS Package Number N14A or J14A

*Also available per JM38510/10301

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage	+14V
Negative Supply Voltage	−7V
Peak Output Current	10 mA
Output Short Circuit Duration	10 seconds
Differential Input Voltage	±5V
Input Voltage	±7V

Power Dissipation	
TO-99 (Note 1)	700 mW
Plastic Dual-In-Line Package (Note 2)	950 mW
Operating Temperature Range	
LM710	−55°C to +125°C
LM710C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM710			LM710C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$, $T_A = 25°C$		0.6	2.0		1.6	5.0	mV
Input Offset Current	$V_{OUT} = 1.4V$, $T_A = 25°C$		0.75	3.0		1.8	5.0	μA
Input Bias Current	$T_A = 25°C$		13	20		16	25	μA
Voltage Gain	$T_A = 25°C$	1250	1700		1000	1500		
Output Resistance	$T_A = 25°C$		200			200		Ω
Output Sink Current	$V_{OUT} = 0$, $T_A = 25°C$ $\Delta V_{IN} \geq 5$ mV $\Delta V_{IN} \geq 10$ mV	 2.0 	 2.5 		 1.6	 2.5		 mA mA
Response Time	$T_A = 25°C$ (Note 4)		40			40		ns
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$			3.0			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$T_{MIN} \leq T_A \leq T_{MAX}$ $R_S \leq 50\Omega$		3.0	10		5.0	20	μV/°C
Input Offset Current	$T_A = T_{A\,MAX}$ $T_A = T_{A\,MIN}$		0.25 1.8	3.0 7.0			7.5 7.5	μA μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{MAX}$ $T_{MIN} \leq T_A \leq 25°C$		5.0 15	25 75		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_A = T_{MIN}$		27	45		25	40	μA
Input Voltage Range	$V^- = -7V$	±5.0			±5.0			V
Common-Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		70	98		dB
Differential Input Voltage Range		±5.0			±5.0			V
Voltage Gain		1000			800			V/V
Positive Output Level	$-5\text{ mA} \leq I_{OUT} \leq 0$ $V_{IN} \geq 5$ mV $V_{IN} \geq 10$ mV	 2.5 	 3.2 	 4.0 	 2.5	 3.2	 4.0	 V V
Negative Output Level	$V_{IN} \geq 5$ mV $V_{IN} \geq 10$ mV	−1.0 	−0.5 	0 	 −1.0	 −0.5	 0	V V
Output Sink Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 0$ $T_A = 125°C$ $T_A = -55°C$	 0.5 1.0	 1.7 2.3					 mA mA
	$V_{IN} \geq 10$ mV, $V_{OUT} = 0$ $0°C \leq T_A \leq +70°C$				0.5			mA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM710			LM710C			Units
		Min	Typ	Max	Min	Typ	Max	
Positive Supply Current	$V_{IN} \geq 5$ mV		5.2	9.0				mA
	$V_{IN} \geq 10$ mV					5.2	9.0	mA
Negative Supply Current	$V_{IN} \geq 5$ mV		4.6	7.0				mA
	$V_{IN} \geq 10$ mV					4.6	7.0	mA
Power Consumption	$I_{OUT} = 0$							
	$V_{IN} \geq 5$ mV		90	150				mW
	$V_{IN} \geq 10$ mV						150	mW

Note 1: Rating applies for ambient temperatures of 25°C; derate linearly at 5.6 mW/°C for ambient temperatures above 25°C.

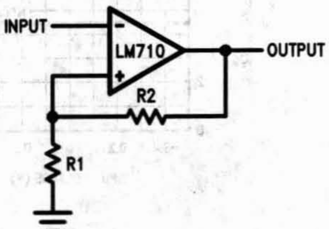
Note 2: Derate linearly at 9.5 mW/°C for ambient temperatures above 25°C.

Note 3: These specifications appy for $V^+ = 12V$, $V^- = -6V$, $-55°C \leq T_A \leq +125°C$ for LM710 and $0°C \leq T_A \leq +70°C$ for LM710C unless otherwise specified: The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at 25°C, and 1V at 125°C for LM710 and 1.5V at 0°C, 1.4V at 25°C, and 1.2V at 70°C for LM710C.

Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive (LM710) or a 10 mV overdrive (LM710C).

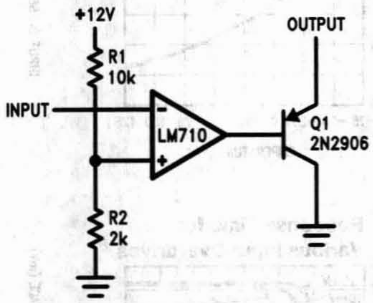
Typical Applications

Schmitt Trigger


INPUT
LM710
OUTPUT
R2
R1

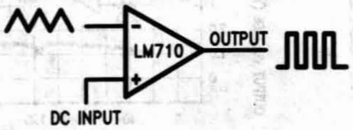
TL/H/10410–4

Line Receive with Increased Output Sink Current


+12V
R1
10k
OUTPUT
INPUT
LM710
Q1
2N2906
R2
2k

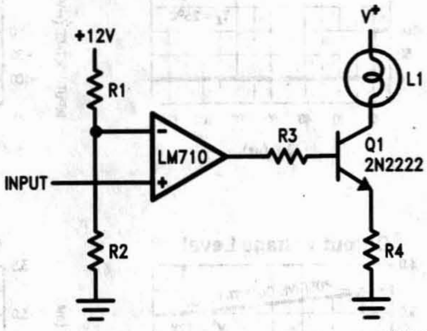
TL/H/10410–5

Pulse Width Modulator


LM710
OUTPUT
DC INPUT

TL/H/10410–6

Level Detector with Lamp Driver

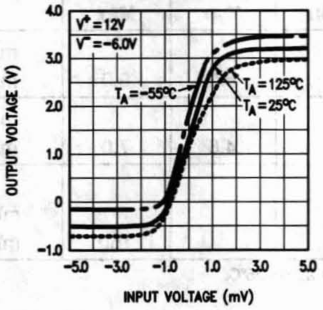

V+
+12V
L1
R1
R3
Q1
2N2222
LM710
INPUT
R2
R4

TL/H/10410–7

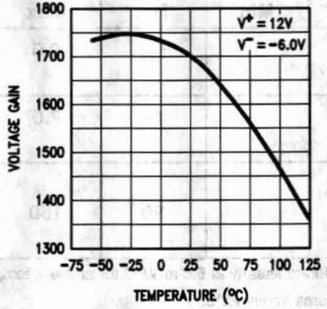
3

Typical Performance Characteristics

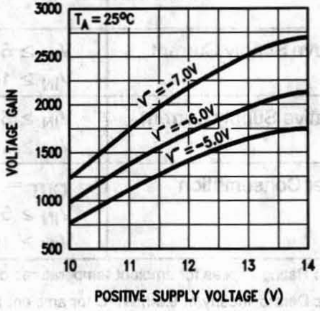
Transfer Function



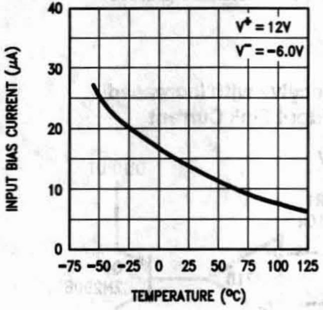
Voltage Gain



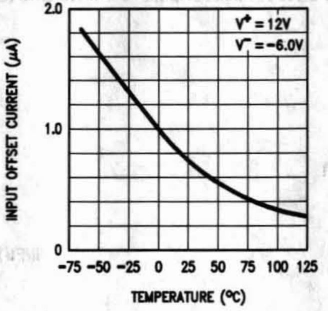
Voltage Gain



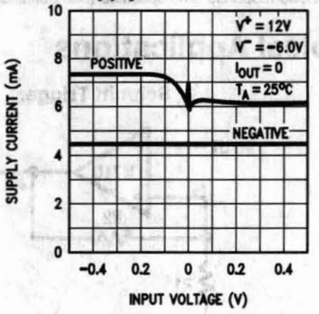
Input Bias Current



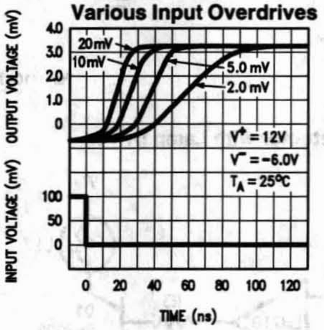
Input Offset Current



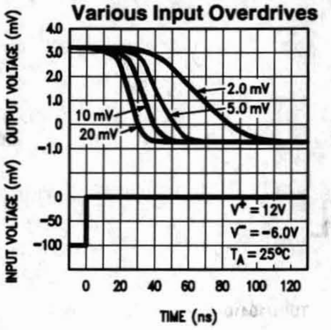
Supply Current



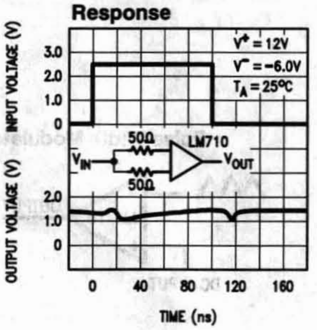
Response Time for Various Input Overdrives



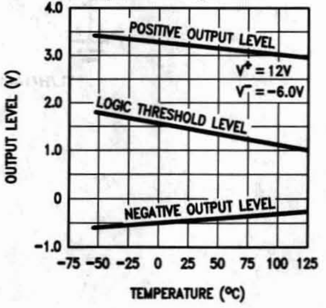
Response Time for Various Input Overdrives



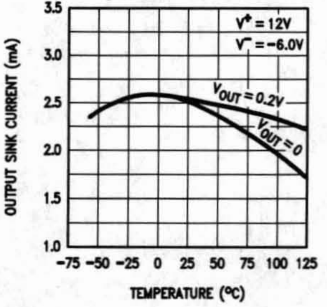
Common Mode Pulse Response



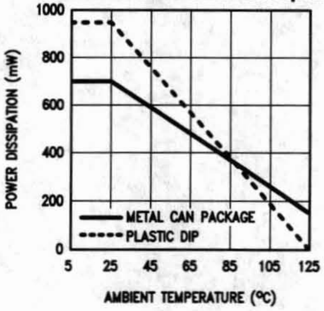
Output Voltage Level



Output Sink Current



Maximum Power Dissipation



TL/H/10410–8

National Semiconductor

LM760
High Speed Differential Comparator

General Description

The LM760 is a differential voltage comparator offering considerable speed improvement over the LM710 family and operates from symmetric supplies of ±4.5V to ±6.5V. The LM760 can be used in high speed analog-to-digital conversion systems and as a zero crossing detector in disc file and tape amplifiers. The LM760 output features balanced rise and fall times for minimum skew and close matching between the complementary outputs. The outputs are TTL compatible with a minimum sink capability of two gate loads.

Features

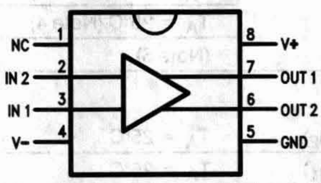
- Guaranteed high speed— 25 ns response time
- Guaranteed delay matching on both outputs
- Complementary TTL compatible outputs
- High sensitivity
- Standard supply voltages

Applications

- High speed A-to-D
- Peak or zero detector

Connection Diagram

8-Lead DIP



TL/H/10067-3

Top View

Ordering Information

Temperature Range Commercial 0°C to +70°C	Package Type	NSC Package Drawing
LM760CN	8-lead Plastic DIP	N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Metal Can and Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Military (LM760)	−55°C to +125°C
Commercial (LM760C)	0°C to +70°C
Lead Temperature	
Metal Can and Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP (Soldering, 10 sec.)	265°C

Positive Supply Voltage	+8.0V
Negative Supply Voltage	−8.0V
Peak Output Current	10 mA
Differential Input Voltage	±5.0V
Input Voltage	$V^+ \geq V_I \geq V^-$
ESD Susceptibility	TBD

LM760
Electrical Characteristics

$V_{CC} = \pm 4.5V$ to $\pm 6.5V$, $T_A = -55°C$ to $+125°C$, $T_A = 25°C$ for typical figures, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current			0.5	7.5	μA
I_{IB}	Input Bias Current			8.0	60	μA
R_O	Output Resistance (Either Output)	$V_O = V_{OH}$		100		Ω
t_{PD}	Response Time	$T_A = 25°C$ (Note 3)		18	30	ns
		$T_A = 25°C$ (Note 4)			25	
		(Note 5)		16		
Δt_{PD}	Response Time Difference between Outputs (Note 1) (t_{PD} of $+V_{I1}$) − (t_{PD} of $-V_{I2}$)	$T_A = 25°C$			5.0	ns
	(t_{PD} of $+V_{I2}$) − (t_{PD} of $-V_{I1}$)	$T_A = 25°C$			5.0	
	(t_{PD} of $+V_{I1}$) − (t_{PD} of $+V_{I2}$)	$T_A = 25°C$			7.5	
	(t_{PD} of $-V_{I1}$) − (t_{PD} of $-V_{I2}$)	$T_A = 25°C$			7.5	
R_I	Input Resistance	f = 1.0 MHz		12		kΩ
C_I	Input Capacitance	f = 1.0 MHz		8.0		pF
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = -55°C$ to $+125°C$		3.0		μV/°C
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	$T_A = +25°C$ to $+125°C$		2.0		nA/°C
		$T_A = +25°C$ to $-55°C$		7.0		
V_{IR}	Input Voltage Range	$V_{CC} = \pm 6.5V$	±4.0	±4.5		V
V_{IDR}	Differential Input Voltage Range			±5.0		V
V_{OH}	Output Voltage HIGH (Either Output)	$0\ mA \leq I_{OH} \leq 5.0\ mA$ $V_{CC} = +5.0V$	2.4	3.2		V
		$I_{OH} = 80\ \mu A$, $V_{CC} = \pm 4.5V$	2.4	3.0		
V_{OL}	Output Voltage LOW (Either Output)	$I_{OL} = 3.2\ mA$		0.25	0.4	V
I^+	Positive Supply Current	$V_{CC} = \pm 6.5V$		18	32	mA
I^-	Negative Supply Current	$V_{CC} = \pm 6.5V$		9.0	16	mA

LM760C
Electrical Characteristics

V_{CC} = ±4.5V to ±6.5V, T_A = 0°C to +70°C, T_A = 25°C for typical figures, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current			0.5	7.5	μA
I_{IB}	Input Bias Current			8.0	60	μA
R_O	Output Resistance (Either Output)	$V_O = V_{OH}$		100		Ω
t_{PD}	Response Time	T_A = 25°C (Note 3)		18	30	ns
		T_A = 25°C (Note 4)			25	
		(Note 5)		16		
Δt_{PD}	Response Time Difference between Outputs (Note 1) (t_{PD} of $+V_{I1}$) − (t_{PD} of $-V_{I2}$)	T_A = 25°C			5.0	ns
	(t_{PD} of $+V_{I2}$) − (t_{PD} of $-V_{I1}$)	T_A = 25°C			5.0	
	(t_{PD} of $+V_{I1}$) − (t_{PD} of $+V_{I2}$)	T_A = 25°C			10	
	(t_{PD} of $-V_{I1}$) − (t_{PD} of $-V_{I2}$)	T_A = 25°C			10	
R_I	Input Resistance	f = 1.0 MHz		12		kΩ
C_I	Input Capacitance	f = 1.0 MHz		8.0		pF
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, T_A = 0°C to +70°C		3.0		μV/°C
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	T_A = +25°C to +70°C		5.0		nA/°C
		T_A = +25°C to 0°C		10		
V_{IR}	Input Voltage Range	V_{CC} = ±6.5V	±4.0	±4.5		V
V_{IDR}	Differential Input Voltage Range			±5.0		V
V_{OH}	Output Voltage HIGH (Either Output)	0 mA ≤ I_{OH} ≤ 5.0 mA V_{CC} = +5.0V	2.4	3.2		V
		I_{OH} = 80 μA, V_{CC} = ±4.5V	2.5	3.0		
V_{OL}	Output Voltage LOW (Either Output)	I_{OL} = 3.2 mA		0.25	0.4	V
I+	Positive Supply Current	V_{CC} = ±6.5V		18	34	mA
I−	Negative Supply Current	V_{CC} = ±6.5V		9.0	16	mA

Note 1: $T_{J\ Max}$ = 150°C.

Note 2: Ratings apply to ambient temperature at 25°C.

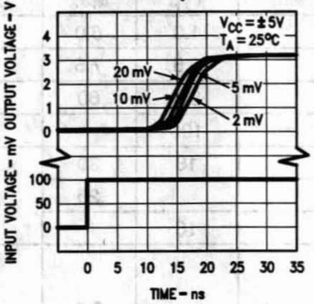
Note 3: Response time measured from the 50% point of a 30 mV_{P-P} 10 MHz sinusoidal input to the 50% point of the output.

Note 4: Response time measured from the 50% point of a 2.0 V_{P-P} 10 MHz sinusoidal input to the 50% point of the output.

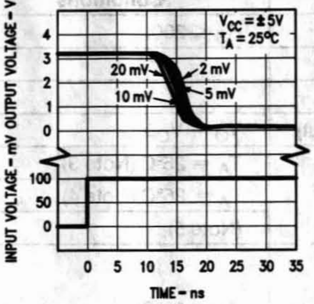
Note 5: Response time measured from the start of a 100 mV input step with 5.0 mV overdrive to the time when the output crosses the logic threshold.

Typical Performance Characteristics

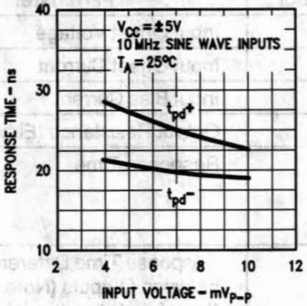
Response Time for Various Output Overdrives



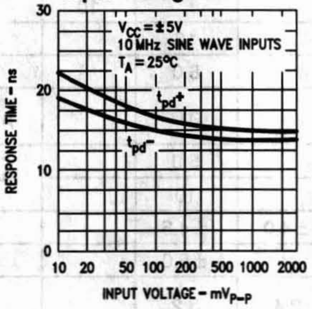
Response Time for Various Input Overdrives



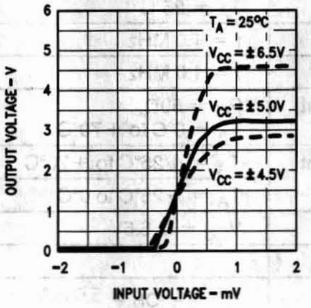
Response Time vs Input Voltage



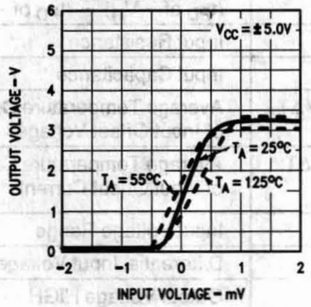
Response Time vs Input Voltage



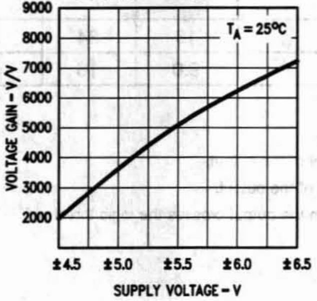
Voltage Transfer Characteristic



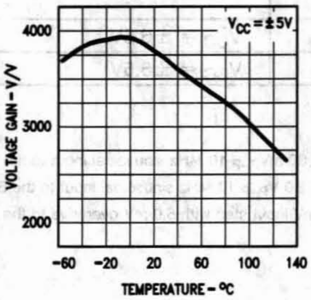
Voltage Transfer Characteristic



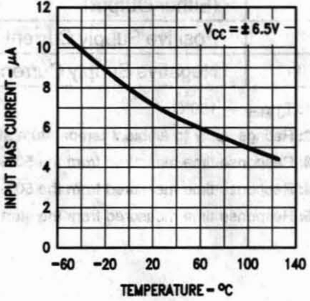
Voltage Gain vs Supply Voltage



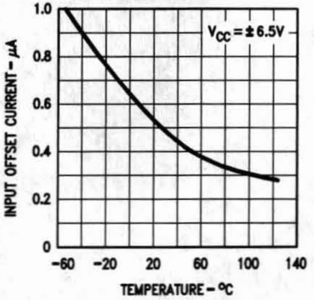
Voltage Gain vs Temperature



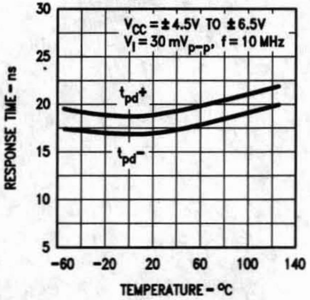
Input Bias Current vs Temperature



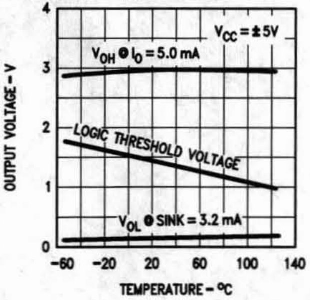
Input Offset Current vs Temperature



Response Time vs Temperature

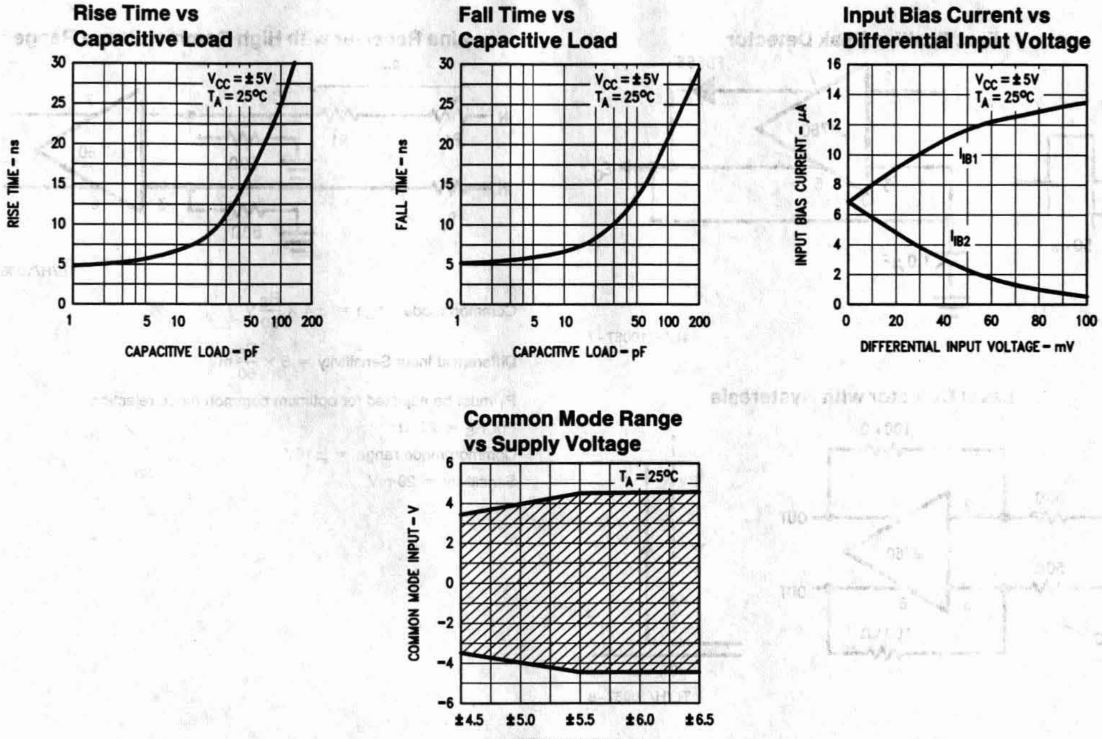


Output Voltage Levels vs Temperature



TL/H/10067–5

Typical Performance Characteristics (Continued)



Rise Time vs Capacitive Load

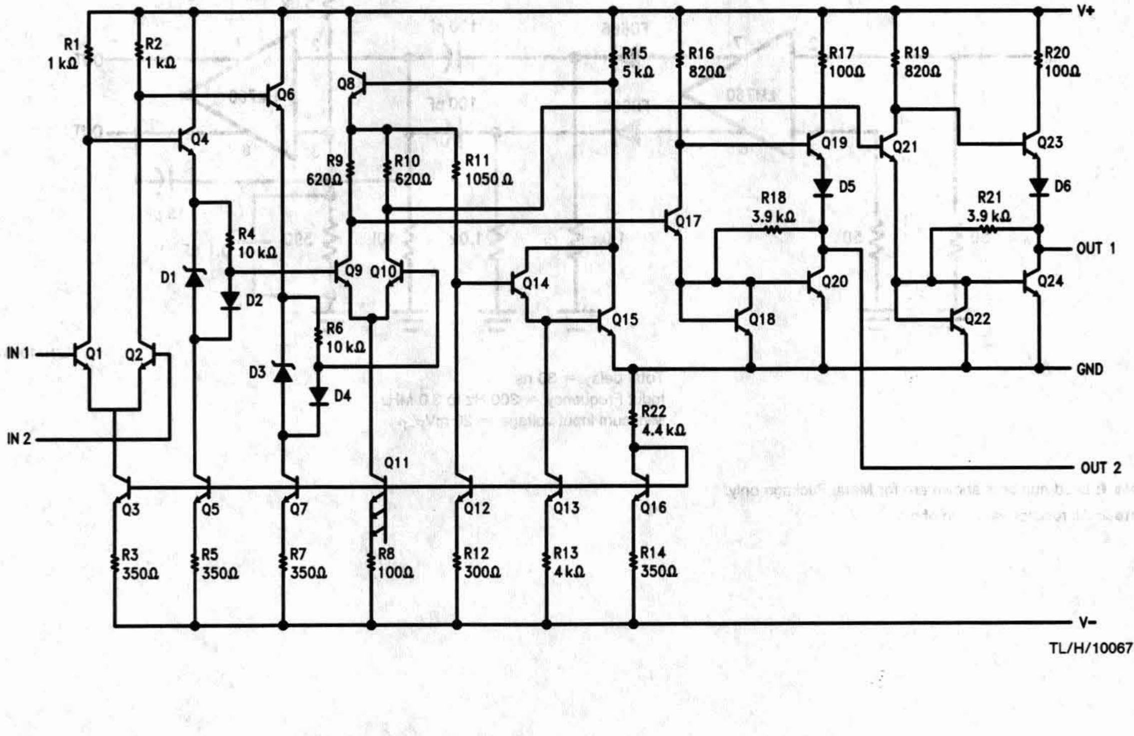
Fall Time vs Capacitive Load

Input Bias Current vs Differential Input Voltage

Common Mode Range vs Supply Voltage

TL/H/10067-6

Equivalent Circuit

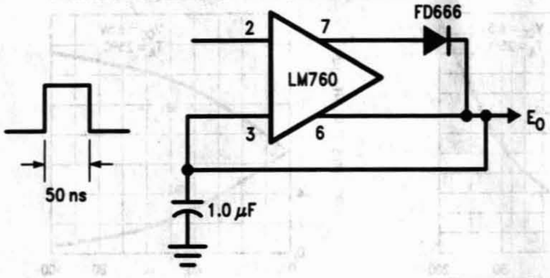


V+
V−
GND
IN 1
IN 2
OUT 1
OUT 2
R1 1 kΩ
R2 1 kΩ
R3 350Ω
R4 10 kΩ
R5 350Ω
R6 10 kΩ
R7 350Ω
R8 100Ω
R9 620Ω
R10 620Ω
R11 1050 Ω
R12 300Ω
R13 4 kΩ
R14 350Ω
R15 5 kΩ
R16 820Ω
R17 100Ω
R18 3.9 kΩ
R19 820Ω
R20 100Ω
R21 3.9 kΩ
R22 4.4 kΩ
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
D1
D2
D3
D4
D5
D6

TL/H/10067-4

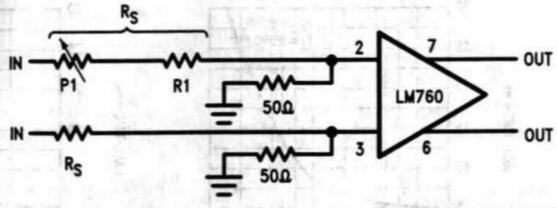
Typical Applications (Note 1)

Fast Positive Peak Detector


FD666
2
7
LM760
3
6
E_O
50 ns
1.0 µF

TL/H/10067-7

Line Receiver with High Common Mode Range


R_S
IN
P1
R1
50Ω
IN
R_S
50Ω
2
7
LM760
3
6
OUT
OUT

TL/H/10067-10

Common mode range = $\pm 4 \times \frac{R_S}{50}$ V

Differential Input Sensitivity = $5 \times \frac{R_S}{50}$ mV

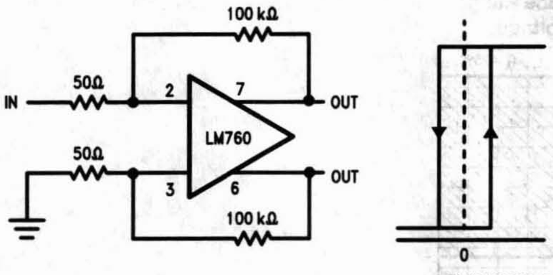
P_1 must be adjusted for optimum common mode rejection.

For $R_S = 200\Omega$:

Common mode range = ±16V

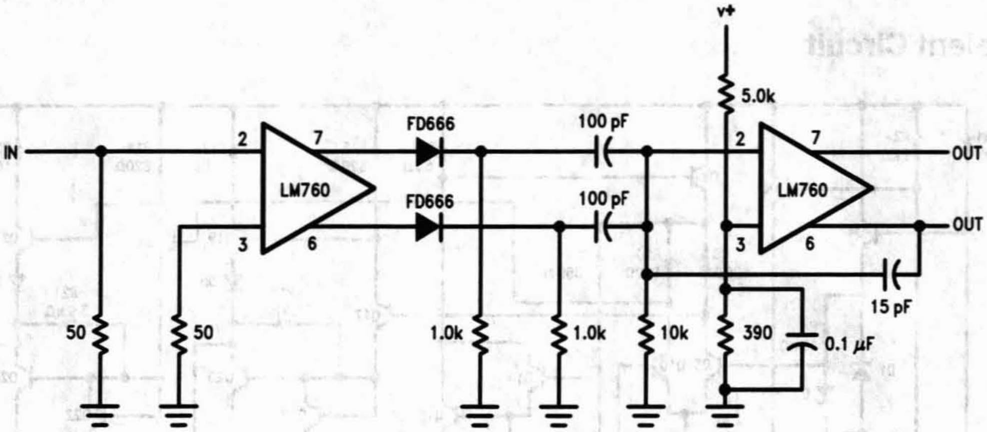
Sensitivity = 20 mV

Level Detector with Hysteresis


100 kΩ
50Ω
IN
2
7
LM760
OUT
50Ω
3
6
OUT
100 kΩ
0

TL/H/10067-8

Zero Crossing Detector (Note 2)


V+
5.0k
IN
2
7
LM760
3
6
FD666
FD666
100 pF
100 pF
2
7
LM760
3
6
OUT
OUT
15 pF
50
50
1.0k
1.0k
10k
390
0.1 µF

TL/H/10067-9

Total delay = 30 ns

Input Frequency = 300 Hz to 3.0 MHz

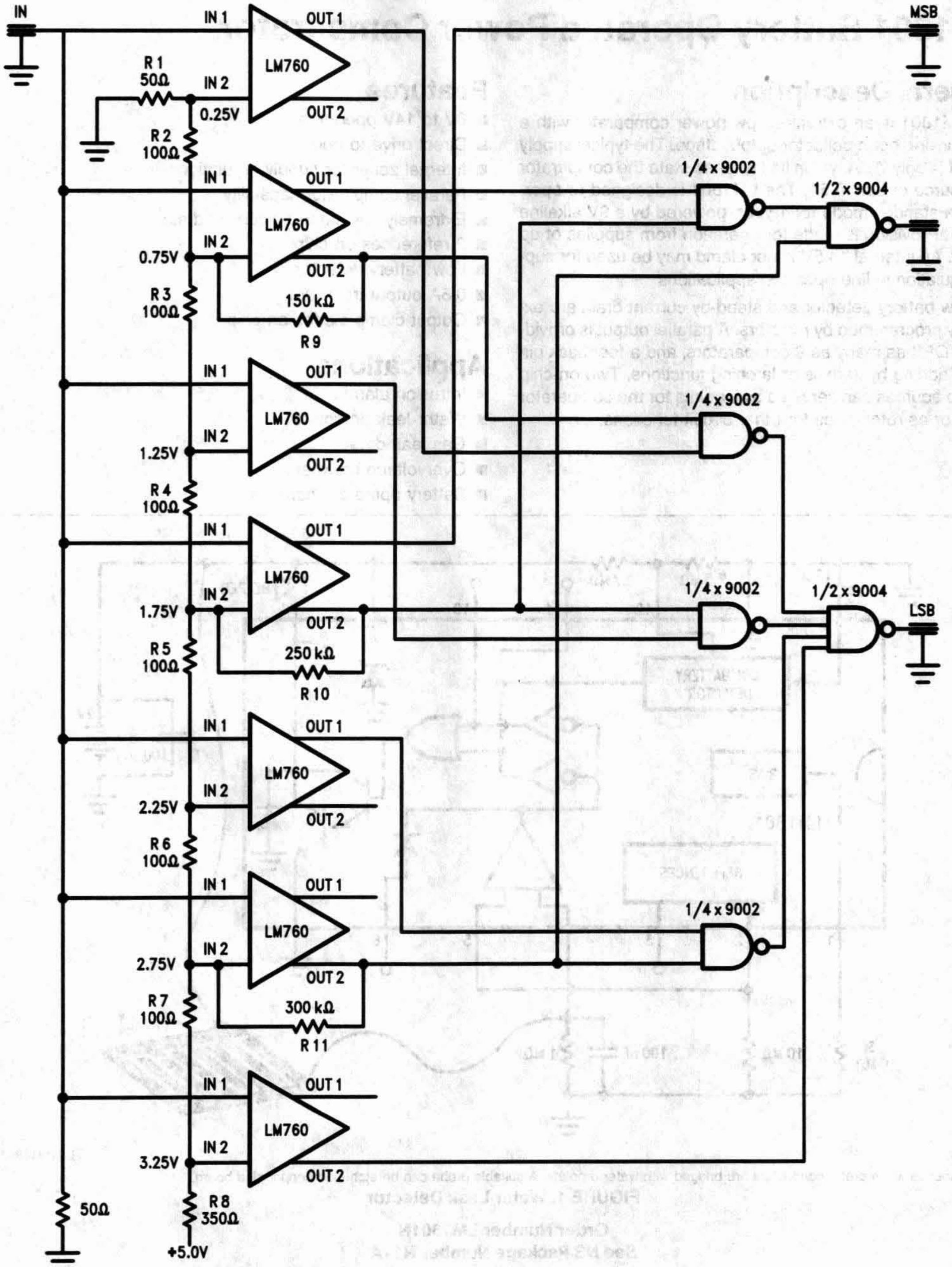
Minimum input voltage = 20 mV_{P-P}

Note 1: Lead numbers shown are for Metal Package only.

Note 2: All resistor values in ohms.

Typical Applications (Note 1) (Continued)

High Speed 3-Bit A/D Converter


IN
IN 1
OUT 1
LM760
IN 2
OUT 2
MSB
R 1
50Ω
0.25V
R 2
100Ω
0.75V
R 3
100Ω
150 kΩ
R 9
1/4 x 9002
1/2 x 9004
1.25V
R 4
100Ω
1.75V
R 5
100Ω
250 kΩ
R 10
LSB
2.25V
R 6
100Ω
2.75V
R 7
100Ω
300 kΩ
R 11
3.25V
50Ω
R 8
350Ω
+5.0V

TL/H/10067-11

Input voltage range = 3.5V
Typical conversion speed = 30 ns

National Semiconductor

LM1801 Battery Operated Power Comparator

General Description

The LM1801 is an extremely low power comparator with a high current, open-collector output stage. The typical supply current is only 7 μA, yet in its switched state the comparator can source or sink 0.5A. The LM1801 is designed to operate in a standby mode for 1 year, powered by a 9V alkaline battery. Provision is made for operation from supplies of up to 14V. An internal 14.5V zener clamp may be used for supply regulation in line operated applications.

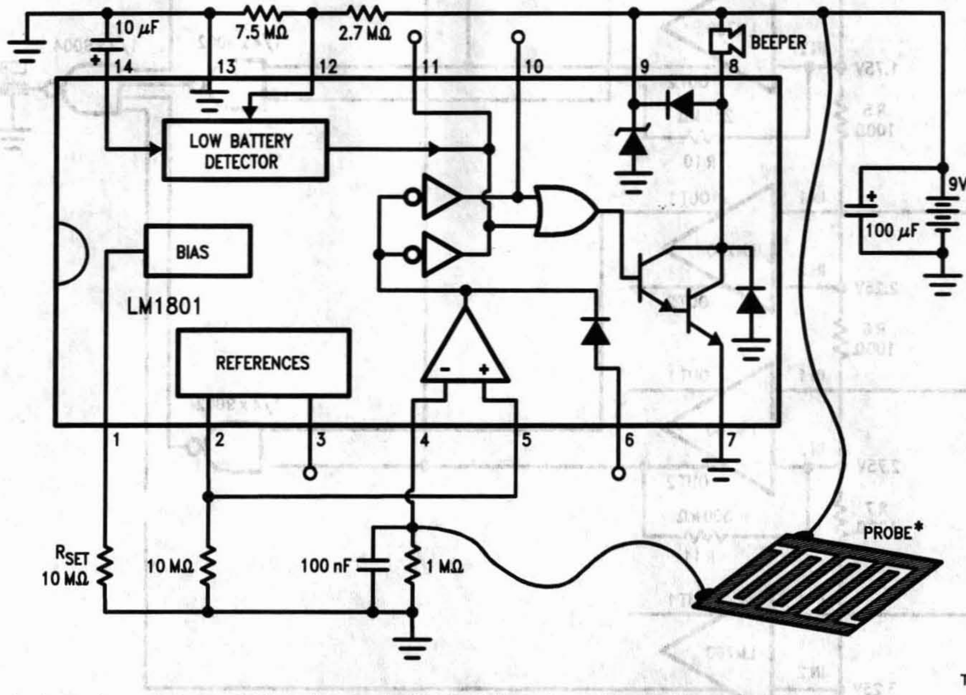
The low battery detector and stand-by current drain are externally programmed by resistors. A parallel output is provided to "OR" as many as 9 comparators, and a feedback pin allows adding hysteresis or latching functions. Two on-chip voltage sources can serve as bias points for the comparator inputs or as references for other circuit functions.

Features

- 8V to 14V operation
- Direct drive to horn
- Internal zener for supply regulation
- Parallel comparator capability
- Extremely low stand-by current drain
- 2 references on chip
- Low battery detector
- 0.5A output transistor
- Output clamp diodes on chip

Applications

- Intrusion alarms
- Water leak detectors
- Gas leak detectors
- Overvoltage crowbars
- Battery operated monitors



*Alarm sounds when probe conductors are bridged with water droplets. A suitable probe can be etched in copper clad board.

FIGURE 1. Water Leak Detector

Order Number LM1801N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	14V
Input Voltage	−0.3V to 14V
Input Differential Voltage	±14V
Power Dissipation (Note 1)	1176 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

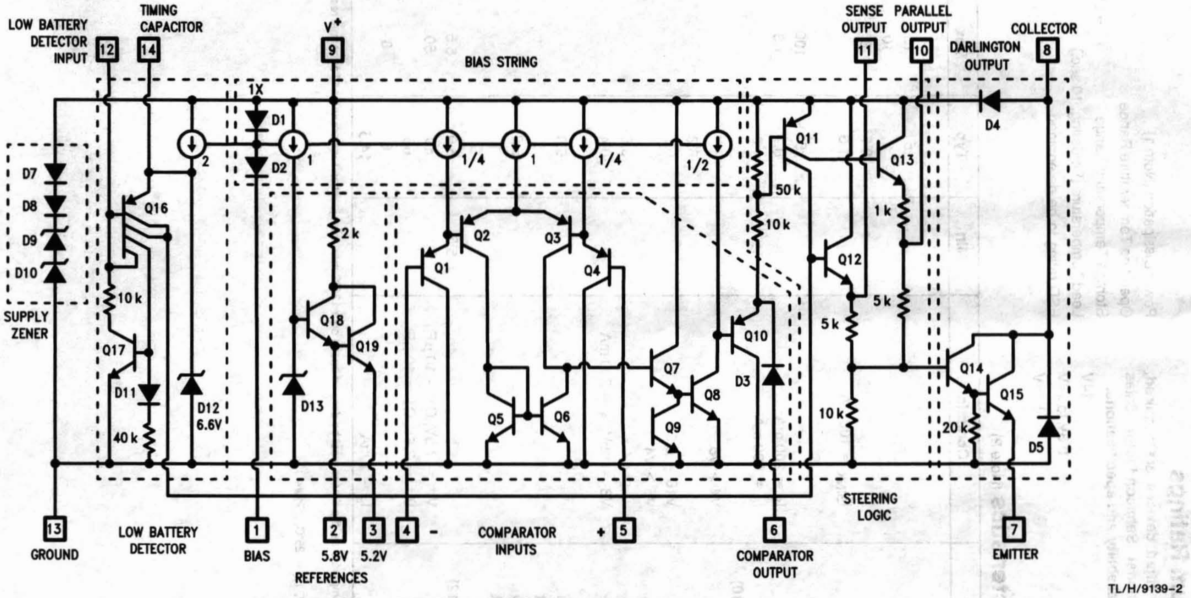
Electrical Characteristics (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
Comparator					
Input Offset Voltage			5	15	mV
Input Bias Current			2	10	nA
Input Offset Current			0.5	8	nA
Pin 6 Output Low	$I_{SINK} = 100\ \mu A$		1.5		V
Output Stage (Pin 8)					
Leakage Current			5	100	nA
Saturation Voltage	$I_8 = 200$ mA		0.7	1.3	V
Saturation Voltage	$I_8 = 500$ mA		1.9		V
Common Alarm Line (Pin 10)					
Drive Capabilities	$V4 > V5$				
Output Voltage High			6.8		V
Output Current	$V10 = 0.0V$		6.5		mA
Driver Requirements	$V5 > V4$				
Input Voltage			3.6		V
Input Current	$V8 = 1.5V$, $I_8 = 200$ mA		0.4		mA
Regulator					
Pin 2 Reference Voltage			5.8		V
Temperature Coefficient			5		mV/°C
Pin 3 Reference Voltage			5.2		V
Temperature Coefficient			7		mV/°C
Battery Check Oscillator					
Threshold Voltage (Pin 12)		5.5	6.0	6.5	V
Period	$V^+ = 7.5V$, $C1 = 10\ \mu F$		40	50	s
Beep Pulse Width	$V^+ = 7.5V$, $C1 = 10\ \mu F$		60		ms
Supply Current (Note 3)			6	8	μA
Zener Clamp Voltage, V9	$I_9 = 1$ mA		14.5		V

Note 1: For operating at elevated temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 85°C/W junction to ambient.

Note 2: $R_{SET} = 10\ M\Omega$, $V^+ = 9V$, $T_A = 25°C$, *(Figure 1)*.

Note 3: Output OFF.


LOW BATTERY DETECTOR INPUT
12
TIMING CAPACITOR
14
V+
9
BIAS STRING
SENSE OUTPUT
11
PARALLEL OUTPUT
10
DARLINGTON OUTPUT
COLLECTOR
8
1X
D1
D2
D4
2
1
1/4
1
1/4
1/2
Q11
Q13
D7
D8
D9
D10
Q16
50 k
10 k
1 k
2 k
Q2
Q3
Q1
Q4
Q12
SUPPLY ZENER
10 k
Q18
Q19
5 k
5 k
Q10
Q17
Q7
Q8
Q14
Q15
D11
D12 6.6V
D13
D3
40 k
Q5
Q6
Q9
10 k
20 k
D5
13
GROUND
LOW BATTERY DETECTOR
1
BIAS
2
5.8V
3
5.2V
REFERENCES
4
-
COMPARATOR INPUTS
+
5
6
COMPARATOR OUTPUT
STEERING LOGIC
7
EMITTER

TL/H/9139-2

FIGURE 2. LM1801 Internal Schematic

Applications Hints

CIRCUIT OPERATION

The LM1801 includes a bias string, comparator, steering logic, output transistor, supply clamp, low voltage detector, and reference. An internal schematic is shown in *Figure 2.*

The chip is biased by a group of current sources that are controlled externally by a fixed resistor, R_{set}. In normal, or standby operation the supply current drain is nominally 6 times the set current at pin 1. The voltage at pin 1 is two forward diode potentials (D1 + D2 = 1.2V typical) less than the positive supply voltage. Practical values of R_{set} range from 100 kΩ to 10 MΩ. Higher currents are useful where speed is important, while lower currents promote long battery life.

The total standby current drain of the LM1801 will include, in addition to the above, the current drawn by the external circuits connected at pins 2, 3, and 12. These are the resistive dividers used to set the low battery threshold and comparator threshold.

The voltage comparator consists of devices Q1 through Q10. The input features a common mode range from less than 300 mV to $V^+ - 1.2V$. If the non-inverting input is within this range, the output state remains valid for inverting inputs of 0V to V^+. If the inverting input is within the common mode range, valid comparisons hold for non-inverting inputs of 300 mV to V^+. The comparator may not switch low if the positive input is grounded.

With a set resistance of 10 MΩ, comparator input bias currents of 2 nA are typical. This allows the use of high-value resistors (10 MΩ) at the comparator inputs which help minimize total supply current. The comparator's output is available through a steering diode (D3) for latching or hysteresis functions.

The comparator output is also coupled internally to the steering logic (Q11–Q13). The comparator, low battery detector, and parallel output (pin 10) functions are OR'd in the logic circuit. In addition, the comparator output is steered to the parallel output. If the parallel outputs (pin 10) of two or more chips are wired together along with a common ground, the comparator on any one chip can cause all of the other output stages to switch, as well as its own output. Outputs are switched when the inverting comparator input is positive with respect to the non-inverting input. Low battery functions are coupled to the steering logic via Q12, and therefore do not affect the parallel output (Q13).

If the sense outputs (pin 11) of two or more chips are wired together, the comparator and low battery detector will cause all outputs to switch.

The output transistor is a 0.5A Darlington. Included in this structure are two clamp diodes. D4 clamps positive collector voltage excursions to the supply, and D5 clamps negative excursions to ground.

The output transistor is normally operated with the emitter grounded. Under these conditions the collector is guaranteed to saturate no higher than 1.3V at 200 mA. 1.9V saturation voltage is typical at 500 mA. The emitter may also be used as an output, and it can swing from ground potential up to 5V on a 9V supply. Emitter swing in the positive direction is limited in the parallel output mode.

A low battery detector with a 6V threshold is also included on chip. This circuit consists of Q16, Q17, D11, and D12. When pin 12, the battery sense input, is higher than 6V, D12 clamps the emitter of Q16 to 6.6V, and the output from the current source flows through the zener to ground. If pin 14 drops below 6V, Q16 is biased ON, and current is drawn away from the zener and into Q16. The SCR formed by Q16 and Q17 is triggered when Q16 is biased ON. The capacitor at pin 14 is discharged, part of its charge flows to the steering logic to pulse the output transistor, and the remainder holds the SCR in its ON state.

When the timing capacitor has discharged, conduction in Q16 and Q17 is commutated. Note that the output from the current source is less than the sustaining current required by the SCR. The current source slowly charges the capacitor until the voltage across it rises 0.6V above pin 12, where the cycle repeats itself. If pin 12 rises above 6V, the zener clamps the voltage at pin 14 and the low battery detector remains OFF.

Pin 12 is biased from an external resistive divider. The divider should be designed to detect at no lower than $V^+ = 7V$. The detector will continue to work at lower voltages providing pin 12 is at least 1V below the supply. For a 9V alkaline battery a threshold of 8.2V is common. A resistive divider of 2.7 MΩ and 7.5 MΩ provides the appropriate threshold.

In many applications the on-chip references can provide bias points. The references are driven from D13, and buffered by Q18 and Q19. If only one bias point is needed the first reference (pin 2) should be used, and the unused output (pin 3) may be left open. The tiny leakage currents in Q18 can cause Q19 (pin 3) to drift upward if a 10 MΩ load resistor is not included at pin 2. The combined output current from pins 2 and 3 should not exceed 1 mA. If neither reference output is used, pins 2 and 3 should be left open.

The last section of the LM1801 is the supply zener. It is built from a series combination of two diodes and two zeners. The breakdown voltage at 1 mA is 14.5V, and the series resistance is about 200Ω. In line operated applications the zener may be used for supply regulation or transient protection. The zener is designed to carry up to 10 mA.

Applications Hints (Continued)

DESIGN HINTS

If the comparator inputs are subjected to electrostatic discharges (ESD), a series resistance is recommended to provide protection. Given the low input bias currents, 100 kΩ resistors can be added without affecting circuit performance, yet they greatly enhance static protection. The LM1801 is not designed to withstand reverse battery.

With a 10 MΩ R_{set}, the LM1801 responds to an input in approximately 2.5 µs, and turns OFF in 200 µs. Higher set currents decrease the response time. With $R_{set} = 1\ M\Omega$, the output switches low in 0.5 µs, and high in 50 µs, and with $R_{set} = 100\ k\Omega$, the response times are reduced to 0.2 µs and 12 µs.

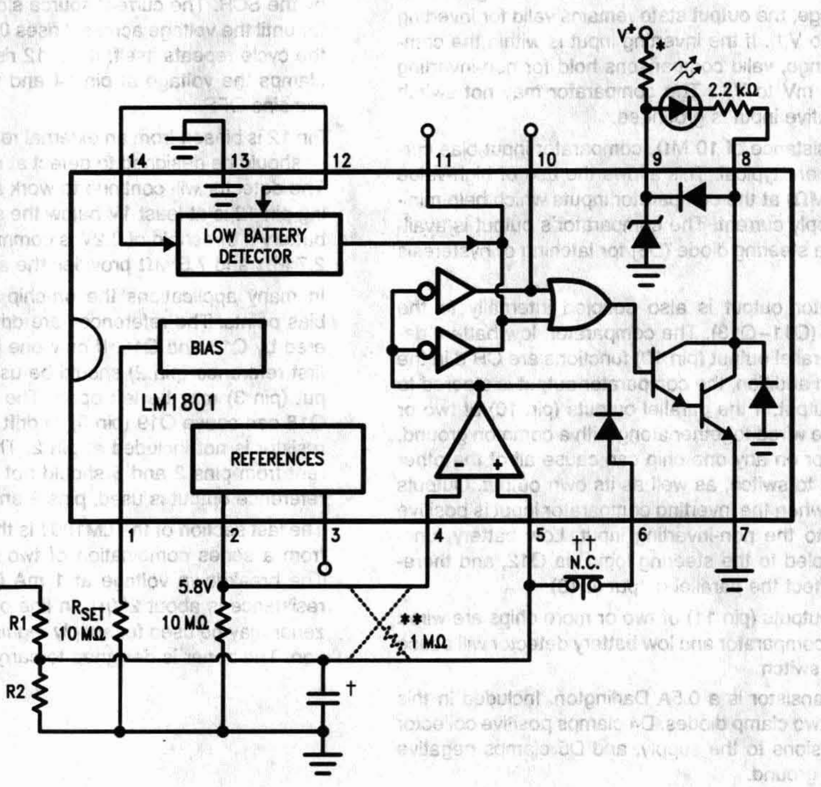
When the circuit is in the standby state ($V5 > V4$), the current consumption in a typical application such as *Figure 1* is less than approximately 7 µA. However, when the comparator switches LOW ($V4 > V5$), the supply current increases to 3 mA owing to the Darlington base current. Therefore, to realize maximum battery life, any application should be devised so that $V5 > V4$ in the standby or resting state.

The output stage can drive lamps, LEDs, buzzers, beepers, relays, motors, and solenoids. However, the low battery detector is not compatible with every load. Since the low battery detector generates only a short pulse (60 ms typical), it is intended for use with buzzers and beepers. Depending on the response time and resonant frequency, some buzzers may only produce a single click. Self-oscillating beepers usually start instantly and produce a recognizable "tweet" when a low battery condition is detected. Incandescent lamps, large relays and solenoids will do absolutely nothing when pulsed by the low battery detector.

Self-oscillating beepers are readily available, such as the Sonalert SNP428 and the Panasonic EAL-069A. These units are guaranteed to self-start when power is applied.

To defeat the low battery detector, short pins 12 and 14 together, and do not connect them to anything else.

Circuit board assembly procedures should include a thorough cleaning to remove flux and other residues. The input pins are often biased by very high impedance sources and even a 10 MΩ leakage path can upset circuit operation.



TL/H/9139–3

$R_1 + R_2 = 10\ M\Omega$

$$V_{TRIP} = \left(\frac{R_1 + R_2}{R_2}\right) 5.8V$$

Minimum trip voltage = 5.8V

*Use series resistor for supplies > 14V. Select for $I_{ZENER} = 5\ mA$.

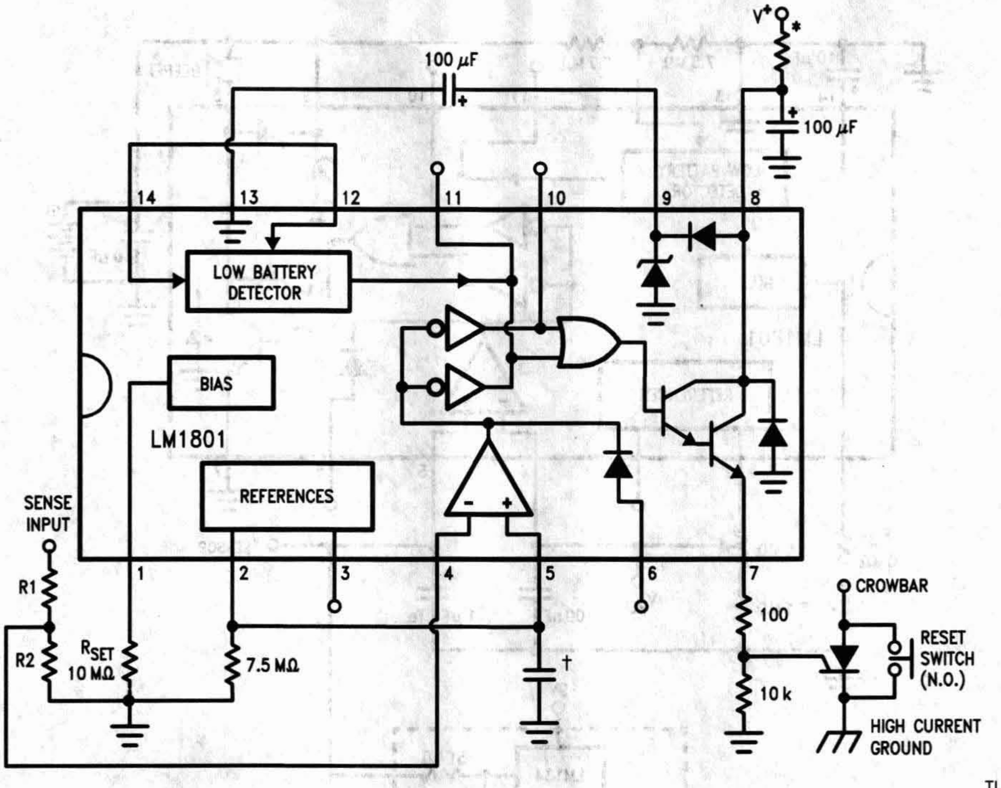
**Reverse connections and add 1 MΩ resistor for overvoltage indication.

†Optional filter capacitor, 1 nF to 100 nF.

††Push to reset. Eliminate pin 6 connection for non-latching operation.

FIGURE 3. Under (Over) Voltage Indicator

Applications Hints (Continued)


V+
*
100 µF
100 µF
14
13
12
11
10
9
8
LOW BATTERY DETECTOR
BIAS
LM1801
REFERENCES
-
+
SENSE INPUT
R1
R2
RSET 10 MΩ
7.5 MΩ
1
2
3
4
5
6
7
†
100
10 k
CROWBAR
RESET SWITCH (N.O.)
HIGH CURRENT GROUND

TL/H/9139–4

$R_1 + R_2 = 10\ M\Omega$

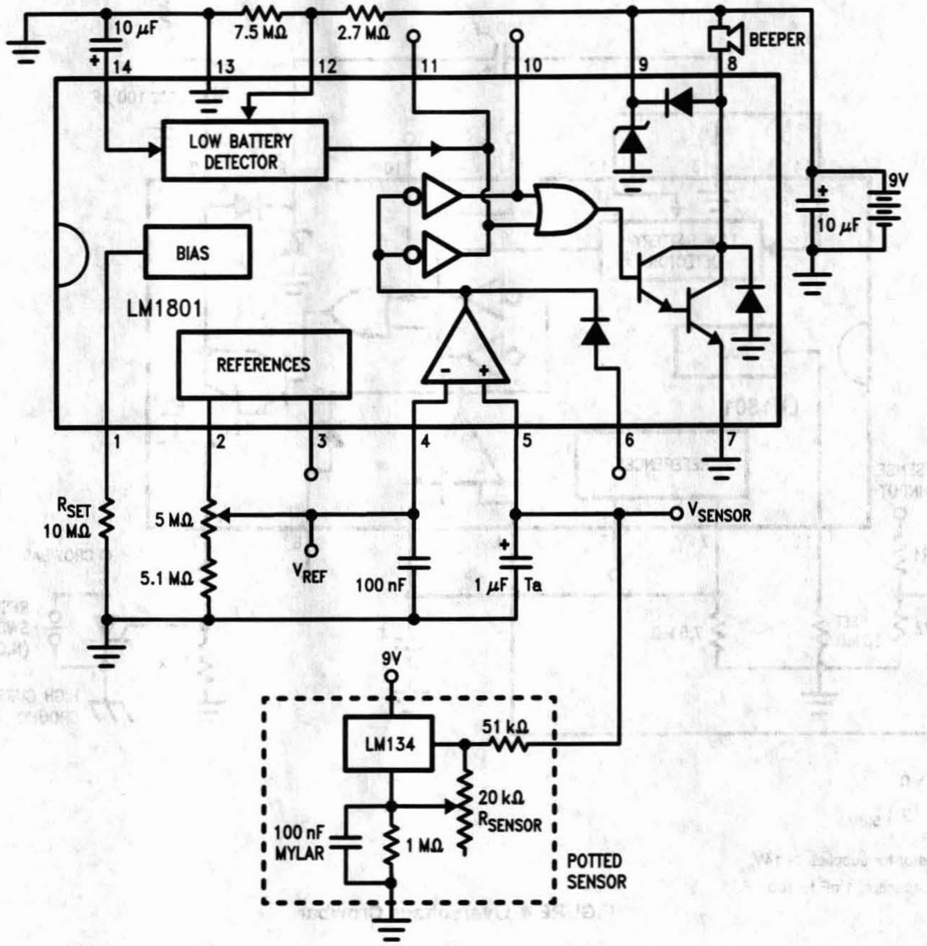
$V_{TRIP} = \left(\frac{R_1 + R_2}{R_2}\right) 5.8V$

*Use series resistor for supplies > 14V.

†Optional filter capacitor, 1 nF to 100 nF.

FIGURE 4. Overvoltage Crowbar

Applications Hints (Continued)


10 μF
7.5 MΩ
2.7 MΩ
BEEPER
14
13
12
11
10
9
8
LOW BATTERY DETECTOR
BIAS
LM1801
REFERENCES
9V
10 μF
1
2
3
4
5
6
7
R_{SET} 10 MΩ
5 MΩ
5.1 MΩ
V_{REF}
100 nF
1 μF
Ta
V_{SENSOR}
9V
LM134
51 kΩ
20 kΩ
R_{SENSOR}
100 nF MYLAR
1 MΩ
POTTED SENSOR

TL/H/9139–5

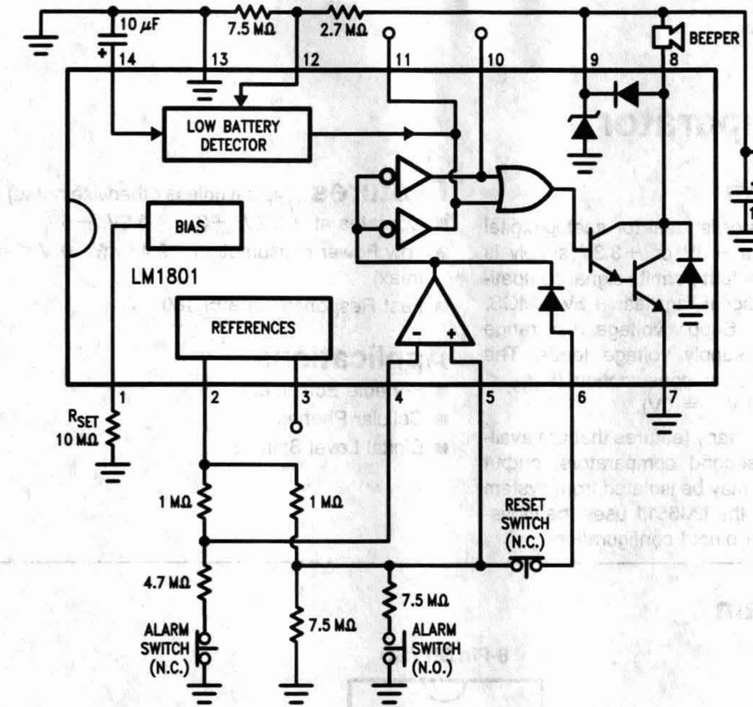
To set trip point, trim V_{REF} to 4.5V. Trim R_{SENSOR} at room temperature (23°C) for:

$$V_{SENSOR} = 4.5\left(\frac{273 + 23}{T_X + 273}\right)$$

where T_X is the desired trip point temperature in °C. As shown, the alarm is activated for over temperature conditions. Reverse the comparator connections for under temperature alarm. The 20 kΩ potentiometer allows an adjustment range of −55°C to +60°C. Add a 10k fixed resistance in series with the potentiometer for a +50°C to +125°C adjustment range. R_{SENSOR} can be replaced by a fixed resistor once the desired value is found. V_{REF} is used as a final adjustment.

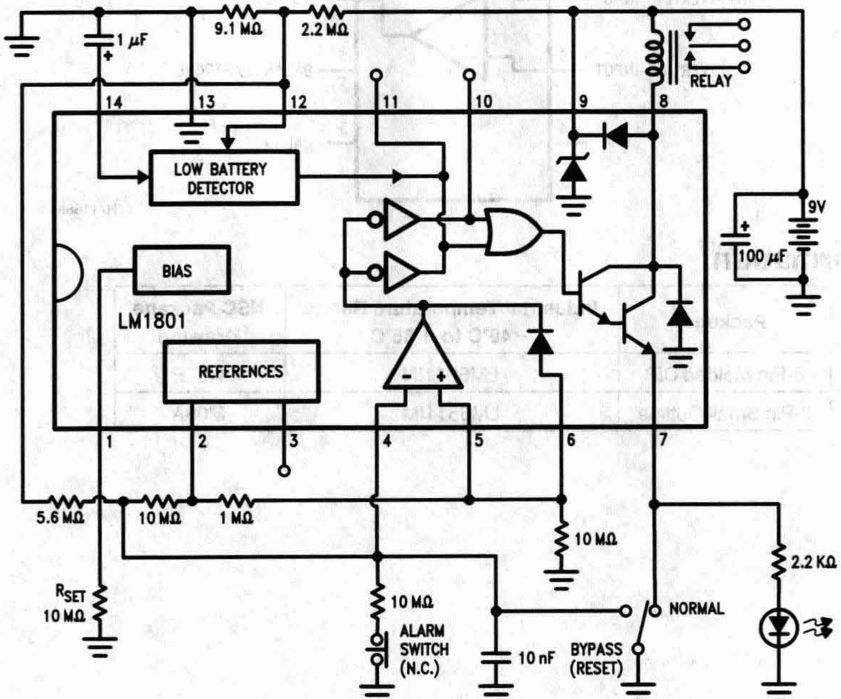
FIGURE 5. Over (Under) Temperature Alarm

Applications Hints (Continued)


10 µF
7.5 MΩ
2.7 MΩ
14
13
12
11
10
9
8
BEEPER
LOW BATTERY DETECTOR
BIAS
LM1801
REFERENCES
9V
100 µF
1
2
3
4
5
6
7
RSET 10 MΩ
1 MΩ
1 MΩ
RESET SWITCH (N.C.)
4.7 MΩ
7.5 MΩ
7.5 MΩ
ALARM SWITCH (N.C.)
ALARM SWITCH (N.O.)

TL/H/9139–6

FIGURE 6. Simple Alarm Circuit


1 µF
9.1 MΩ
2.2 MΩ
14
13
12
11
10
9
8
RELAY
LOW BATTERY DETECTOR
9V
100 µF
BIAS
LM1801
REFERENCES
1
2
3
4
5
6
7
5.6 MΩ
10 MΩ
1 MΩ
10 MΩ
2.2 KΩ
RSET 10 MΩ
10 MΩ
NORMAL
ALARM SWITCH (N.C.)
10 nF
BYPASS (RESET)

TL/H/9139–7

FIGURE 7. Full-Featured Intrusion Alarm

National Semiconductor

LM6511
180 ns 3V Comparator

General Description

The LM6511 voltage comparator is ideal for analog-digital interface circuitry when only a +3V or +3.3V supply is available. The open-collector output permits signal compatibility with a wide variety of digital families: +5V CMOS, +3V CMOS, TTL and so on. Supply voltage may range from 2.7V to 36V between supply voltage leads. The LM6511 operates with little power consumption ($P_{diss} <$ 9.45 mW at $V^+ = +2.7V$ and $V^- = 0V$).

This voltage comparator offers many features that are available in traditional sub-microsecond comparators: output sync strobe, inputs and output may be isolated from system ground, and wire-ORing. Also, the LM6511 uses the industry-standard, single comparator pinout configuration.

Features (Typical unless otherwise noted)

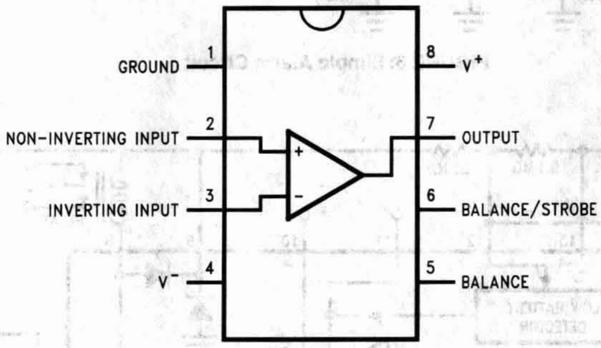
- Operates at +2.7V, +3V, +3.3V, +5V
- Low Power consumption <9.45 mW @ $V^+ = 2.7V$ (max)
- Fast Response Time of 180 ns

Applications

- Portable Equipment
- Cellular Phones
- Digital Level Shifting

Connection Diagram

8-Pin DIP/SO



TL/H/11888-1

Ordering Information

Package	Industrial Temperature Range −40°C to +85°C	NSC Package Drawing
8-Pin Molded DIP	LM6511IN	N08E
8-Pin Small Outline	LM6511IM	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	−0.3 to +36V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Differential Input Voltage	±30V
Input Voltage	(Note 2)
Storage Temperature Range	−65°C to +150°C
Soldering Information:	
DIP Package (Soldering in 10 sec)	260°C
SO Package (Vapor Phase in 60 sec)	215°C
SO Package (Infrared in 15 sec)	220°C
Power Dissipation	500 mW
Output Short Circuit Duration	10s
Junction Temperature	150°C
ESD Rating (C = +100 pF, R = 1.5 kΩ)	300V

Operating Ratings (Note 1)

Supply Voltage	2.5V to 30V
Temperature Range	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
DIP Package	110°C/W
SO Package	170°C/W

DC Electrical Characteristics

Unlesss otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 2.7V, V^- = 0V, 50Ω ≤ R_L ≤ 50kΩ, and I_L = 1.0 mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I Limit	Units (Limits)
V_{OS}	Offset Voltage	$R_S \le 50$ kΩ (Note 3)	1.5	5 **8**	mV max
I_B	Input Bias Current		38	130 **200**	nA max
I_{OS}	Input Offset Current	$R_S \le 50$ kΩ (Note 3)	1.5	20 **50**	
I_S	Positive Supply Current		2.7	3.5 **5**	mA max
	Negative Supply Current		1.5	2.0 **2.5**	
V_{SAT}	Saturation Voltage	$V_{IN} \le 10$ mV I_{SINK} = 8 mA	0.23	0.4 **0.4**	V max
A_V	Large Signal Voltage Gain	ΔV_{OUT} = 2V	40		V/mV
CMRR	Common Mode Rejection Ratio		72		dB
I_{STROBE}	Strobe ON Current	(Note 5)	2.0	5.0	mA max
V_{IN}	Input Voltage Range			0.50	V min
				$V^+ - 1.25$	V max
	Output Leakage Current	$V_{IN} \ge 10$ mV, V_{OUT} = 35V, I_{STROBE} = 3 mA	0.2		nA max

AC Electrical Characteristics

Unlesss otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ - 2.7V$, $V^- = 0V$, $50\Omega \leq R_L \leq 50\ k\Omega$, and $I_L = 1.0\ mA$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical	LM6511I	Units (Limits)
				Limit	
T_R	Response Time	(Note 4)	180		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

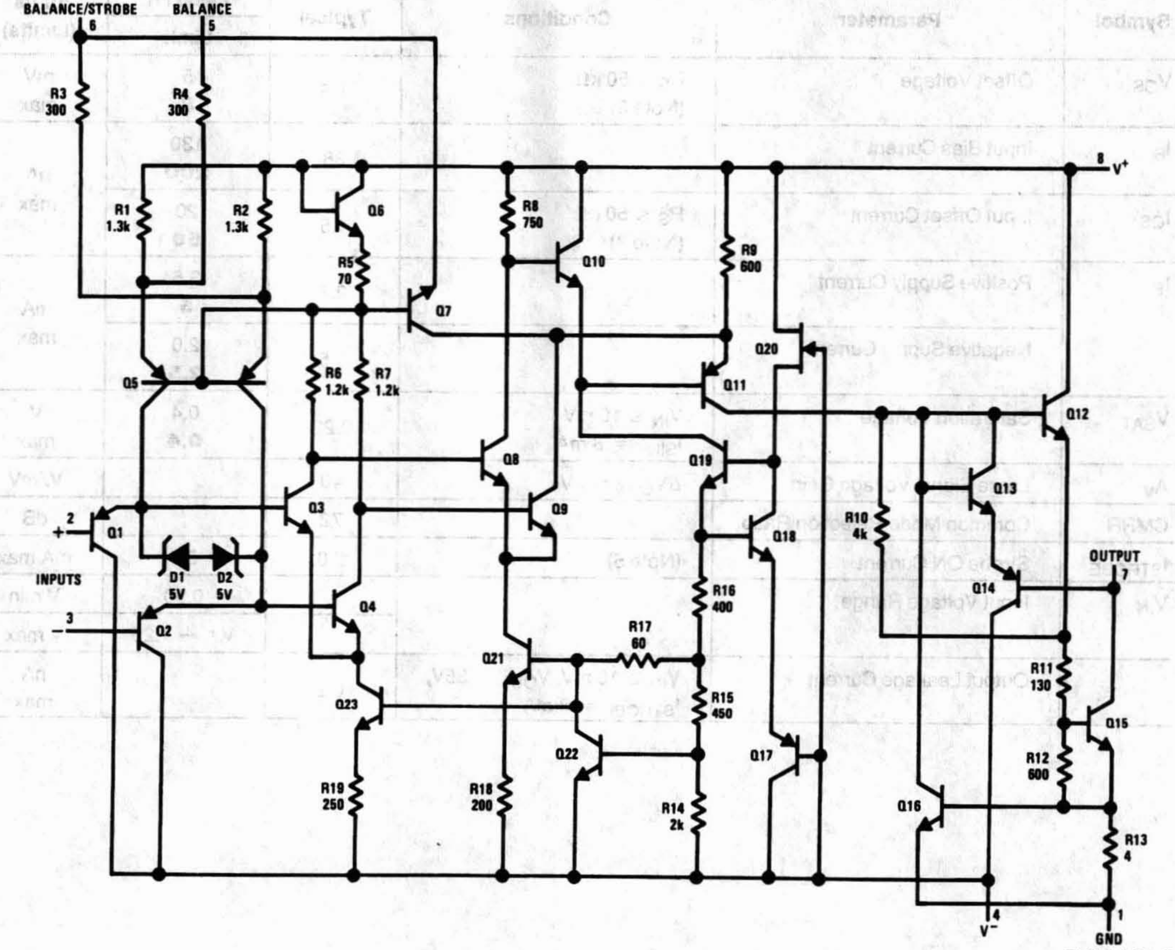
Note 2: The positive input voltage limit is 30V above the negative supply voltage. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply voltage, whichever is less.

Note 3: The offset voltage and offset current limits are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Therefore, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 4: This specification is for a 100 mV input step with a 25 mV overdrive.

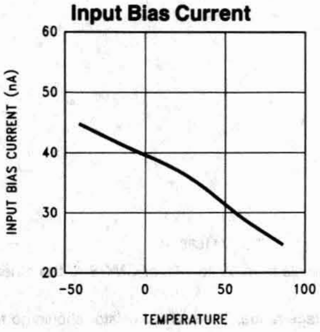
Note 5: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 mA to 5 mA.

Schematic Diagram

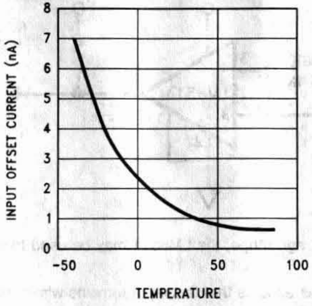

BALANCE/STROBE
6
BALANCE
5
R3 300
R4 300
R1 1.3k
R2 1.3k
Q6
R5 70
Q7
R8 750
Q10
R9 600
8
V+
Q20
Q5
R6 1.2k
R7 1.2k
Q11
Q12
Q8
Q19
Q13
Q3
Q9
R10 4k
2
+
Q1
Q18
INPUTS
D1 5V
D2 5V
OUTPUT
7
Q14
R16 400
3
−
Q2
Q4
R17 60
Q21
R11 130
R15 450
Q23
Q15
Q22
Q17
R12 600
R19 250
R18 200
R14 2k
Q16
R13 4
4
V−
1
GND

TL/H/11888–5

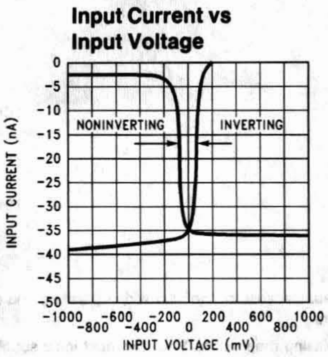
LM6511 Typical Performance Characteristics V_S = 3V unless otherwise noted



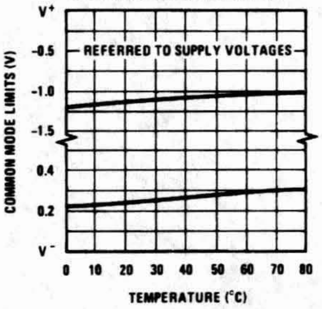
Input Bias Current



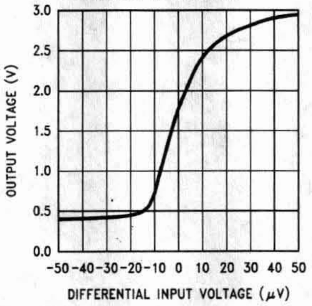
Input Offset Current



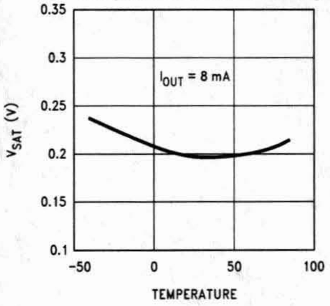
Input Current vs Input Voltage



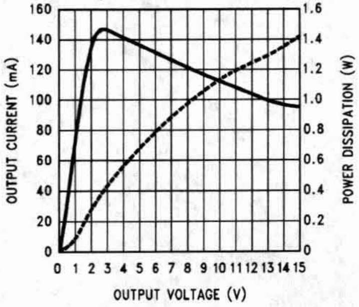
Common Mode Limits



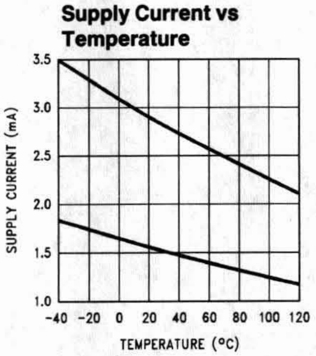
Transfer Function



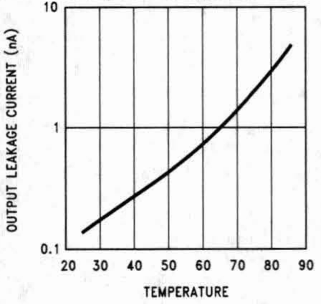
Output Saturation Voltage



Output Current Limiting

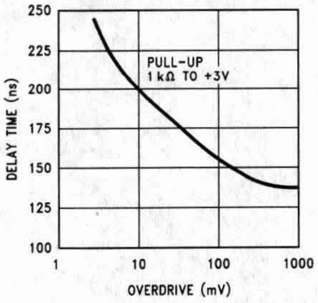


Supply Current vs Temperature



Output Leakage Current

TL/H/11888-2

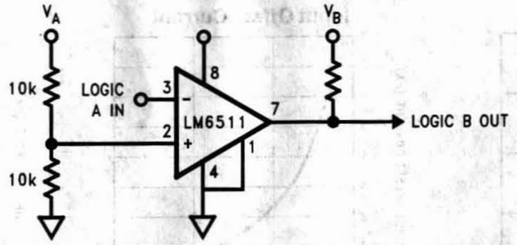


Propagation Delay vs Overdrive

TL/H/11888-3

Typical Application

Universal Logic Level Shifter


V_A
V_B
10k
10k
LOGIC
A IN
3
2
8
7
1
4
−
+
LM6511
LOGIC B OUT

TL/H/11888–4

Notes: Because of the very wide operating and output voltage range, the LM6511 may be used to shift logic levels from 3V to TTL or CMOS to the other way around.

By biasing the input to ½ of the input logic supply (V_A), this assures that this input remains within the input voltage range. The pull-up resistor should go to the output logic supply (V_B).

National Semiconductor

LMC6762 Dual/LMC6764 Quad MicroPower, Rail-To-Rail Input and Output CMOS Comparator

General Description

The LMC6762/4 is an ultra low power dual/quad comparator with a maximum supply current of 10 μA/comparator. It is designed to operate over a wide range of supply voltages, from 2.7V to 15V. The LMC6762/4 has guaranteed specs at 2.7V to meet the demands of 3V digital systems.

The LMC6762/4 has an input common-mode voltage range which exceeds both supplies. This is a significant advantage in low-voltage applications. The LMC6762/4 also features a push-pull output that allows direct connections to logic devices without a pull-up resistor.

A quiescent power consumption of 50 μW/amplifier (@ $V^+ = 5V$) makes the LMC6762/4 ideal for applications in portable phones and hand-held electronics. The ultra-low supply current is also independent of power supply voltage. Guaranteed operation at 2.7V and a rail-to-rail performance makes this device ideal for battery-powered applications.

Refer to the LMC6772/4 datasheet for an open-drain version of this device.

Features (Typical unless otherwise noted)

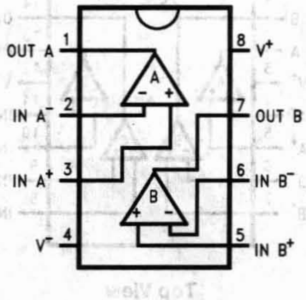
- Low power consumption (Guaranteed) $I_S = 10\ \mu A/comp$
- Wide range of supply voltages 2.7V to 15V
- Rail-to-rail input common mode voltage range
- Rail-to-rail output swing (Within 100 mV of the supplies, @ $V^+ = 2.7V$, and $I_{LOAD} = 2.5\ mA$)
- Short circuit protection 40 mA
- Propagation delay (@ $V^+ = 5V$, 100 mV overdrive) 4 μs

Applications

- Laptop computers
- Mobile phones
- Metering systems
- Hand-held electronics
- RC timers
- Alarm and monitoring circuits
- Window comparators, multivibrators

Connection Diagrams

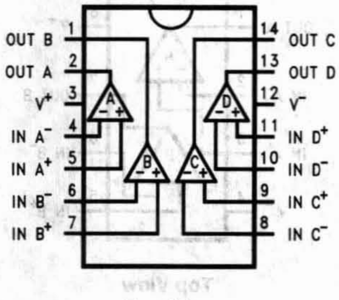
8-Pin DIP/SO



TL/H/12320–1

Top View

14-Pin DIP/SO



TL/H/12320–2

Top View

Ordering Information

Package	Temperature Range −40°C to +85°C	NSC Drawing	Transport Media
8-Pin Molded DIP	LMC6762AIN, LMC6762BIN	N08E	Rails
8-Pin Small Outline	LMC6762AIM, LMC6762BIM LMC6762AIMX, LMC6762BIMX	M08A M08A	Rails Tape and Reel
14-Pin Molded DIP	LMC6764AIN, LMC6764BIN	N08E	Rails
14-Pin Small Outline	LMC6764AIM, LMC6764BIM LMC6762AIMX, LMC6762BIMX	M14A M14A	Rails Tape and Reel

National Semiconductor

ADVANCE INFORMATION

LMC6772 Dual, LMC6774 Quad, Micro-Power Rail-To-Rail Input and Open Drain Output CMOS Comparator

General Description

The LMC6772/4 is an ultra low power dual/quad comparator with a maximum 10 μA/comparator power supply current. It is designed to operate over a wide range of supply voltages, from 2.7V to 15V. The LMC6772/4 has guaranteed specs at 2.7V to meet the demands of 3V digital systems.

The LMC6772/4 has an input common-mode voltage range which exceeds both rails. This is a significant advantage in low-voltage applications. The LMC6772/4 also features an open-drain output. This architecture is ideal for mixed supply voltage systems as an external resistor can be used to pull the output up to +15V, regardless of the supply voltage.

A quiescent power consumption of 50 μW/Amplifier (@V_S = 5V) makes the LMC6772/4 ideal for applications in portable phones and hand-held electronics. The ultra-low supply current is also independent of the power supply voltage. Guaranteed operation at 2.7V and rail-to-rail performance make the device ideal for battery-powered applications.

Features (Typical unless otherwise noted)

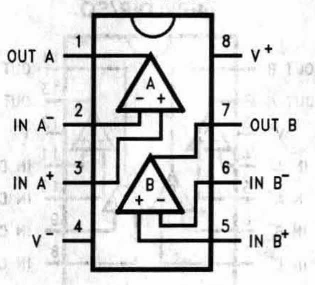
- Low power consumption I_S = 10 μA/comp
- Wide range of supply voltages 2.7V to 15V
- Rail-to-Rail Input Common Mode Voltage Range
- Open-drain output stage
- Short circuit protection 40 mA
- Propagation delay (@V_S = 5V, 100 mV overdrive) 5 μs
- Refer to the LMC6762/4 datasheet for a device with similar specs and a push-pull output stage

Applications

- Laptop computers
- Mobile Phones
- Metering systems
- Hand-held electronics
- RC timers, Window Comparators, Multivibrators
- Alarm and monitoring circuits

Connection Diagrams

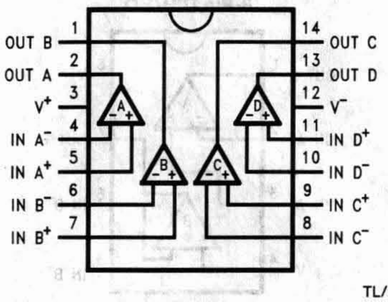
8-Pin DIP/SO



TL/H/12347-1

Top View

14-Pin DIP/SO



TL/H/12347-2

Top View

Package	Temperature Range Industrial, −40°C to +85°C	NSC Drawing	Transport Media
8-Pin Molded DIP	LMC6772AIN, LMC6772BIN	N08E	Rails
8-Pin Small Outline	LMC6772AIM, LMC6772BIM	M08A	Rails
	LMC6772AIMX, LMC6772BIMX		Tape and Reel
14-Pin Molded DIP	LMC6774AIN, LMC6774BIN	N14A	Rails
14-Pin Small Outline	LMC6774AIM, LMC6774BIM	M14A	Rails
	LMC6774AIMX, LMC6774BIMX		Tape and Reel

National Semiconductor

PRELIMINARY

LMC7211
Tiny CMOS Comparator with Rail-to-Rail Input

General Description

The LMC7211 is a micropower CMOS comparator available in the space saving SOT23-5 package. This makes the comparator ideal for space and weight critical designs. The LMC7211 is available in SO-8 surface mount packages and in conventional 8-pin DIP packages. The LMC7211 is supplied in two offset voltage grades, 5 mV and 15 mV.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The rail-to-rail input voltage makes the LMC7211 a good choice for sensor interfacing, such as light detector circuits, optical and magnetic sensors, and alarm and status circuits.

The Tiny Comparator's outside dimensions (length x width x height) of 3.05mm x 3.00mm x 1.43mm allow it to fit into tight spaces on PC boards.

Features

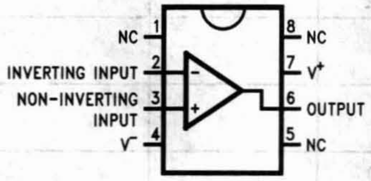
- Tiny SOT 23-5 package saves space
- Package is less than 1.43 mm thick
- Guaranteed specs at 2.7V, 5V, 15V supplies
- Typical supply current 7 μA at 5V
- Response time of 8 μs at 5V
- LMC7211—push-pull output
- Input common-mode range beyond V− and V+
- Low input current

Applications

- Battery Powered Products
- Notebooks and PDAs
- PCMCIA cards
- Mobile Communications
- Alarm and Security circuits
- Direct Sensor Interface
- Replaces amplifiers used as comparators with better performance and lower current

Connection Diagrams

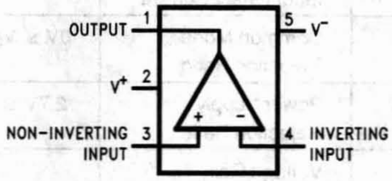
8-Pin DIP/SO-8



TL/H/12337-1

Top View

5-Pin SOT23-5



TL/H/12337-2

Top View

Package	Ordering Information	NSC Drawing Number	Package Marking	Transport Media
8-Pin DIP	LMC7211AIN	N08E	LMC7211AIN	rails
8-Pin DIP	LMC7211BIN	N08E	LMC7211BIN	rails
8-Pin SO-8	LMC7211AIM	M08A	LM7211AIM	rails
8-Pin SO-8	LMC7211BIM	M08A	LM7211BIM	rails
8-Pin SO-8	LMC7211AIMX	M08A	LM7211AIM	2.5k units tape and reel
8-Pin SO-8	LMC7211BIMX	M08A	LM7211BIM	2.5k units tape and reel
5-Pin SOT 23-5	LMC7211AIM5	MA05A	C00A	250 units tape and reel
5-Pin SOT 23-5	LMC7211BIM5	MA05A	C00B	250 units tape and reel
5-Pin SOT 23-5	LMC7211AIM5X	MA05A	C00A	3k units tape and reel
5-Pin SOT 23-5	LMC7211BIM5X	MA05A	C00B	3k units tape and reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2 kV
Differential Input Voltage	(V_{CC}) +0.3V to ($-V_{CC}$)$-$0.3V
Voltage at Input/Output Pin	(V_{CC}) + 0.3V to ($-V_{CC}$)$-$0.3V
Supply Voltage ($V^+ - V^-$)	16V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±20 mA
Current at Power Supply Pin	40 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.7 \leq V_{CC} \leq 15V$
Junction Temperature Range	
LMC7211AI, LMC7211BI	$-40°C \leq T_J \leq +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-pin Molded DIP	115°C/W
SO-8 Package, 8-Pin Surface Mount	165°C/W
M05A Package, 5-Pin Surface Mount	325°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7211AI Limit (Note 6)	LMC7211BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift		1.0			μV/°C
	Input Offset Voltage Average Drift		3.3			μV/Month
I_B	Input Current		0.04			pA
I_{OS}	Input Offset Current		0.02			pA
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 2.7V$	75			dB
PSRR	Power Supply Rejection Ratio	$2.7V \leq V^+ \leq 5V$	80			dB
A_V	Voltage Gain		100			dB
CMVR	Input Common-Mode Voltage Range	CMRR > 55 dB	3.0	2.9 **2.7**	2.9 **2.7**	V min
		CMRR > 55 dB	−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OH}	Output Voltage High	$I_{load} = 2.5$ mA	2.5	2.4 **2.3**	2.4 **2.3**	V max
V_{OL}	Output Voltage Low	$I_{load} = 2.5$ mA	0.2	0.3 **0.4**	0.3 **0.4**	V max
I_S	Supply Current	V_{OUT} = low	7	12 **14**	12 **14**	μA max

5.0V and 15.0V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V and 15V, V^- = 0V, V_{CM} = V_O = $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7211AI Limit (Note 6)	LMC7211BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift	V^+ = 5V	1.0			μV/°C
		V^+ = 15V	4.0			
	Input Offset Voltage Average Drift	V^+ = 5V	3.3			μV/Month
		V^+ = 15V	4.0			
I_B	Input Current		0.04			pA
I_{OS}	Input Offset Current		0.02			pA
CMRR	Common Mode Rejection Ration	V^+ = 5.0V	75			dB
		V^+ = 15.0V	82			dB
PSRR	Power Supply Rejection Ratio	5V ≤ V^+ ≤ 10V	80			dB
A_V	Voltage Gain		100			dB
CMVR	Input Common-Mode Voltage Range	V^+ = 5.0V CMRR > 55 dB	5.3	5.2 **5.0**	5.2 **5.0**	V min
		V^+ = 5.0V CMRR > 55 dB	−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
		V^+ = 15.0V CMRR > 55 dB	15.3	15.2 **15.0**	15.2 **15.0**	V max
		V^+ = 15.0V CMRR > 55 dB	−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OH}	Output Voltage High	V^+ = 5V I_{load} = 5 mA	4.8	4.6 **4.45**	4.6 **4.45**	mV max
		V^+ = 15V I_{load} = 5 mA	14.8	14.6 **14.45**	14.6 **14.45**	mV max
V_{OL}	Output Voltage Low	V^+ = 5V I_{load} = 5 mA	0.2	0.40 **0.55**	0.40 **0.55**	mV min
		V^+ = 15V I_{load} = 5 mA	0.2	0.40 **0.55**	0.40 **0.55**	mV min
I_S	Supply Current	V_{OUT} = low	7	14 **18**	14 **18**	μA max
I_{SC}	Short Circuit Current	Sourcing	30			mA min
		Sinking	45			mA min

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$. **Boldface** limits apply at the temperature extreme.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC7211AI Limit (Note 6)	LMC7211BI Limit (Note 6)	Units
t_{rise}	Rise Time	f = 10 kHz, Cl = 50 pF, Overdrive = 10 mV		0.3			μs
t_{fall}	Fall Time	f = 10 kHz, Cl = 50 pF, Overdrive = 10 mV		0.3			μs
t_{PHL}	Propagation Delay (High to Low)	f = 10 kHz, Cl = 50 pF	10 mV	10			μs
			100 mV	4			
		V+ = 2.7V, f = 10 kHz, Cl = 50 pF	10 mV	10			μs
			100 mV	4			
t_{PLH}	Propagation Delay (Low to High)	f = 10 kHz, Cl = 50p	10 mV	6			μs
			100 mV	4			
		V+ = 2.7V, f = 10 kHz, Cl = 50 pF	10 mV	7			μs
			100 mV	4			

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

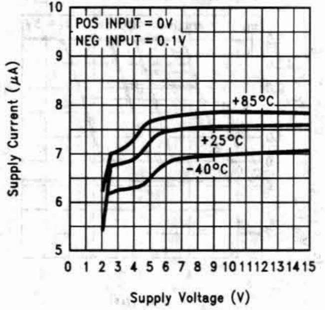
Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

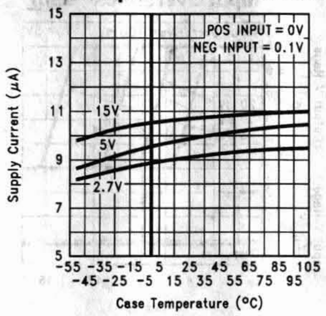
Note 6: All limits are guaranteed by testing or statistical analysis.

Typical Performance Characteristics Single Supply $T_A = 25°C$ unless specified

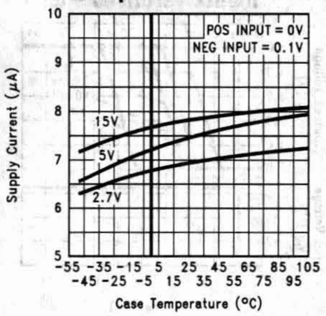
Supply Current vs Supply Voltage



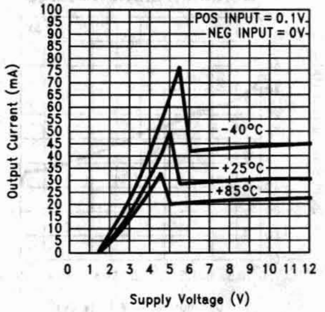
Supply Current vs Temperature while Sourcing



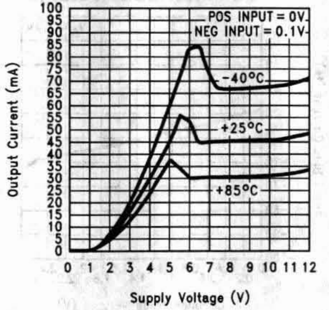
Supply Current vs Temperature while Sinking



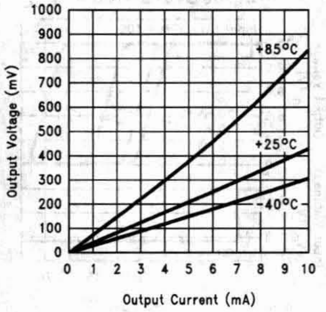
Output Sourcing Current vs Supply Voltage



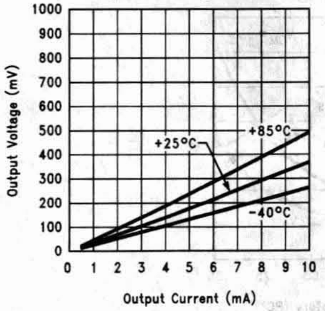
Output Sinking Current vs Supply Voltage



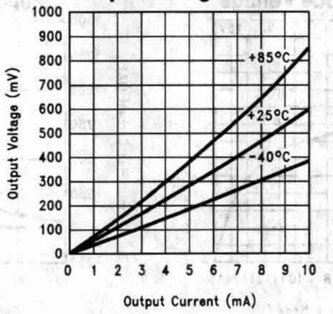
Output Sourcing Current vs Output Voltage @ 5V



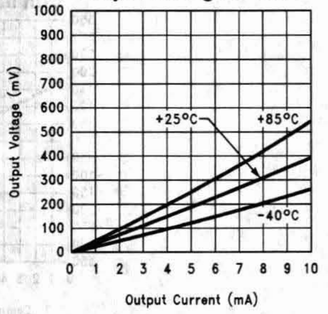
Output Sinking Current vs Output Voltage @ 5V



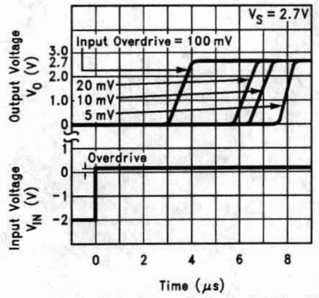
Output Sourcing Current vs Output Voltage @ 15V



Output Sinking Current vs Output Voltage @ 15V

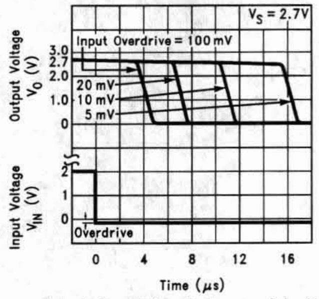


Response Time for Various Input Overdrives $-t_{PLH}$



Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives $-t_{PHL}$

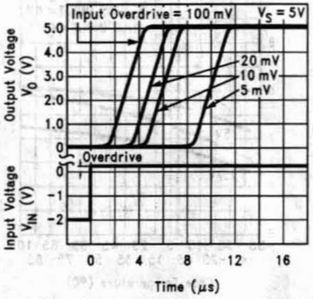


Input Overdrive Referenced to V_{OS}

TL/H/12337–3

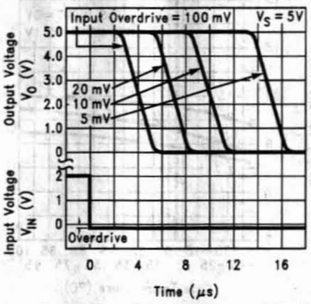
Typical Performance Characteristics Single Supply, $T_A = 25°C$ unless specified (Continued)

Response Time for Various Input Overdrives $-t_{PLH}$



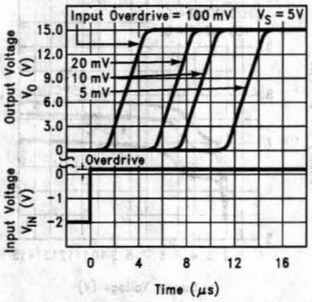
Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives $-t_{PHL}$



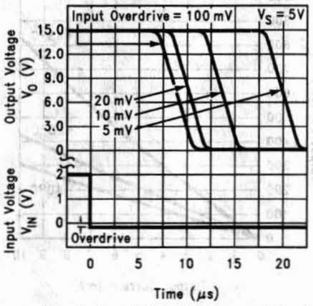
Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives $-t_{PLH}$



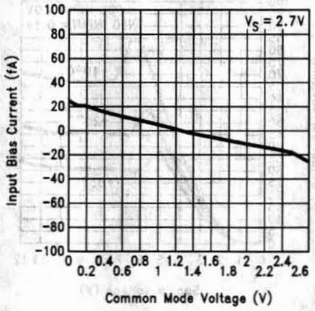
Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives $-t_{PHL}$

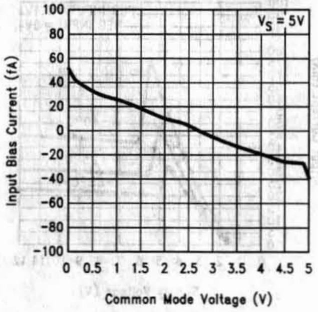


Input Overdrive Referenced to V_{OS}

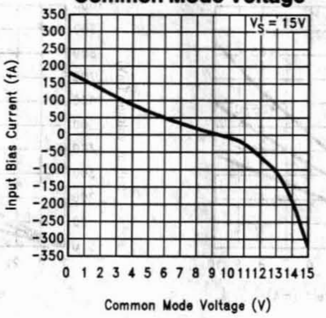
Input Bias Current vs Common Mode Voltage



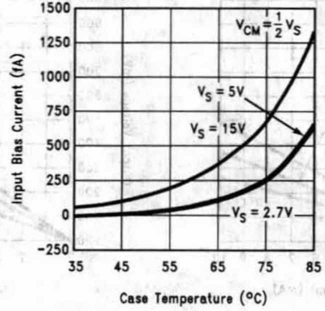
Input Bias Current vs Common Mode Voltage



Input Bias Current vs Common Mode Voltage



Input Bias Current vs Temperature



TL/H/12337-4

Application Information

1.0 Benefits of the LMC7211 Tiny Comparator

Size. The small footprint of the SOT 23-5 packaged Tiny Comparator, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

Height. The height (0.056 inches, 1.43 mm) of the Tiny Comparator makes it possible to use it in PCMCIA type III cards.

Simplified Board Layout. The Tiny Comparator can simplify board layout in several ways. First, by placing a comparator where comparators are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny Comparators instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

DIPs available for prototyping. LMC7211 comparators packaged in conventional 8-pin dip packages can be used for prototyping and evaluation without the need to use surface mounting in early project stages.

Low Supply Current. The typical 7 µA supply current of the LMC7211 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Wide Voltage Range. The LMC7211 is characterized at 15V, 5V and 2.7V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7211 a good choice for devices where the voltage may vary over the life of the batteries.

Digital Outputs Representing Signal Level. Comparators provide a high or low digital output depending on the voltage levels of the (+) and (−) inputs. This makes comparators useful for interfacing analog signals to microprocessors and other digital circuits. The LMC7211 can be thought of as a one-bit a/d converter.

Push-Pull Output. The push-pull output of the LMC7211 is capable of both sourcing and sinking milliamp level currents even at a 2.7 volt supply. This can allow the LMC7211 to drive multiple logic gates.

Driving LEDs (Light Emitting Diodes). With a 5 volt power supply, the LMC7211's output sinking current can drive small, high efficiency LEDs for indicator and test point circuits. The small size of the Tiny package makes it easy to find space to add this feature to even compact designs.

Input range to Beyond Rail to Rail. The input common mode range of the LMC7211 is slightly larger than the actual power supply range. This wide input range means that the comparator can be used to sense signals close to the power supply rails. This wide input range can make design easier by eliminating voltage dividers, amplifiers, and other front end circuits previously used to match signals to the limited input range of earlier comparators. This is useful to power supply monitoring circuits which need to sense their own power supply, and compare it to a reference voltage which is close to the power supply voltage. The wide input range can also be useful for sensing the voltage drop across a current sense resistor for battery chargers.

Zero Crossing Detector. Since the LMC7211's common mode input range extends below ground even when powered by a single positive supply, it can be used with large input resistors as a zero crossing detector.

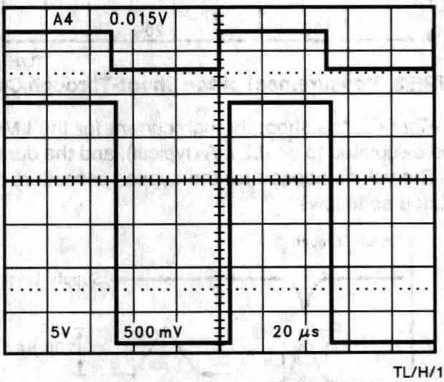
Low Input Currents and High Input Impedance. These characteristics allow the LMC7211 to be used to sense high impedance signals from sensors. They also make it possible to use the LMC7211 in timing circuits built with large value resistors. This can reduce the power dissipation of timing circuits. For very long timing circuits, using high value resistors can reduce the size and cost of large value capacitors for the same R-C time constant.

Direct Sensor Interfacing. The wide input voltage range and high impedance of the LMC7211 may make it possible to directly interface to a sensor without the use of amplifiers or bias circuits. In circuits with sensors which can produce outputs in the tens to hundreds of millivolts, the LMC7211 can compare the sensor signal with an appropriately small reference voltage. This may be done close to ground or the positive supply rail. Direct sensor interfacing may eliminate the need for an amplifier for the sensor signal. Eliminating the amplifier can save cost, space, and design time.

2.0 Low Voltage Operation

Comparators are the common devices by which analog signals interface with digital circuits. The LMC7211 has been designed to operate at supply voltages of 2.7V without sacrificing performance to meet the demands of 3V digital systems.

At supply voltages of 2.7V, the common-mode voltage range extends 200 mV (guaranteed) below the negative supply. This feature, in addition to the comparator being able to sense signals near the positive rail, is extremely useful in low voltage applications.



TL/H/12337-5

FIGURE 1. Even at Low-Supply Voltage of 2.7V, an Input Signal which Exceeds the Supply Voltages Produces No Phase Inversion at the Output

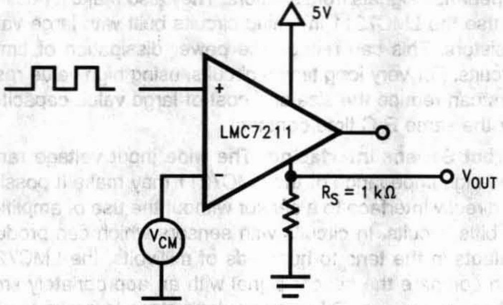
At $V^+ = 2.7V$ propagation delays are $t_{PLH} = 4$ µs and $t_{PHL} = 4$ µs with overdrives of 100 mV.

Please refer to the performance curves for more extensive characterization.

Application Information (Continued)

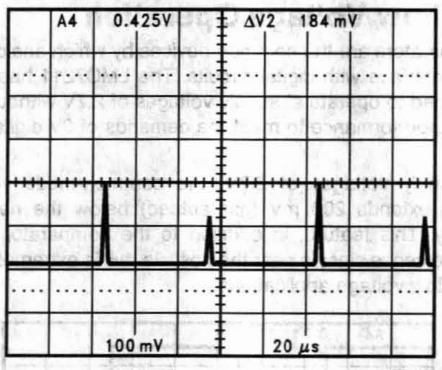
3.0 Shoot-Through Current

The shoot-through current is defined as the current surge, above the quiescent supply current, between the positive and negative supplies of a device. The current surge occurs when the output of the device switches states. The shoot-through current results in glitches in the supply voltages. Usually, glitches in the supply lines are prevented by bypass capacitors. When the glitches are minimal, the value of the bypass capacitors can be reduced.



TL/H/12337-6

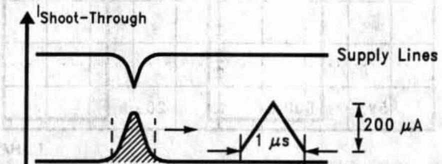
FIGURE 2. Circuit for Measurement of the Shoot-Through Current



TL/H/12337-7

FIGURE 3. Measurement of the Shoot-Through Current

From *Figure 3*, the shoot-through current for the LMC7211 can be calculated to be 0.2 mA (typical), and the duration is 1 µs. The values needed for the bypass capacitors can be calculated as follows:



TL/H/12337-8

Area of Δ = ½ (1 µs × 200 µA)
= 100 pC

The capacitor needs to supply 100 picocolumb. To avoid large shifts in the comparator threshold due to changes in the voltage level, the voltage drop at the bypass capacitor should be limited to 100 mV or less.

The charge needed (100 picocolumb) and the allowable voltage drop (100 mV) will give us the minimum capacitor value required.

$$\Delta Q = C(\Delta V)$$

$$C = \Delta Q/\Delta V = 100\ \text{picocolumb}/100\ \text{mV}$$

$$C = 10^{-10}/10^{-1} = 10^{-9} = 1\ \text{nF} = 0.001\ \mu\text{F}$$

$$10^{-9} = 1\ \text{nF} = 0.001\ \mu\text{F}$$

The voltage drop of ~100 mV will cause a threshold shift in the comparator. This threshold shift will be reduced by the power supply rejection ratio, (PSRR). The PSRR which is applicable here is not the DC value of PSRR (~80 dB), but a transient PSRR which will be usually about 20 dB–40 dB, depending on the circuit and the speed of the transient. This will result in an effective threshold shift of about 1 mV to 10 mV.

For precision and level sensing circuits, it is generally a good goal to reduce the voltage delta on the power supply to a value equal to or less than the hysteresis of the comparator circuit. If the above circuit was to be used with 50 mV of hysteresis, it would be reasonable to increase the bypass capacitor to 0.01 µF to reduce the voltage delta to 10 mV. Larger values may be useful for obtaining more accurate and consistent switching.

Note that the switching current of the comparator can spread to other parts of the board as noise. The bypass capacitor reduces this noise. For low noise systems this may be reason to make the capacitor larger.

For non-precision circuits, such as using a comparator to determine if a push-button switch is on or off, it is often cheaper and easier to use a larger value of hysteresis and a small value or bypass capacitance. The low shoot-through current of the LMC7211 can allow the use of smaller and less expensive bypass capacitors in non-critical circuits.

4.0 Output Short Circuit Current

The LMC7211 has short circuit protection of 40 mA. However, it is not designed to withstand continuous short circuits, transient voltage or current spikes, or shorts to any voltage beyond the supplies. A resistor in series with the output should reduce the effect of shorts. For outputs which send signals off PC boards additional protection devices, such as diodes to the supply rails, and varistors may be used.

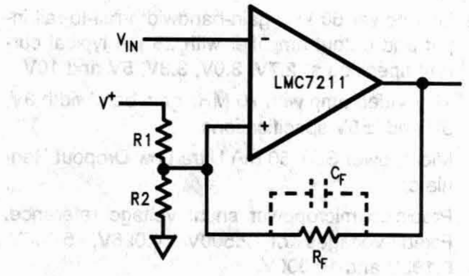
5.0 Hysteresis

If the input signal is very slow or very noisy, the comparator output might trip several times as the input signal passes through the threshold. Using positive feedback to add hysteresis to the switching can reduce or eliminate this problem. The positive feedback can be added by a high value resistor (R_F). This will result in two switching thresholds, one for increasing signals and one for decreasing signals. A capacitor can be added across R_F to increase the switching speed and provide more short term hysteresis. This can result in greater noise immunity for the circuit.

See *Figures 4, 5* and *6.*

Application Information (Continued)

Note that very heavy loading of the comparator output, such as LED drive or bipolar logic gates, will change the output voltage and shift the voltage thresholds.

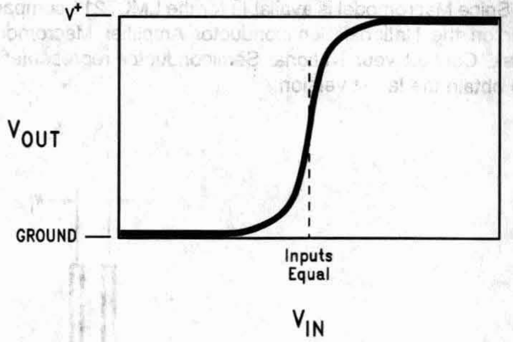


TL/H/12337-9

$R_F \gg R_1$ and
$R_F \gg R_2$

FIGURE 4. Positive Feedback for Hysteresis

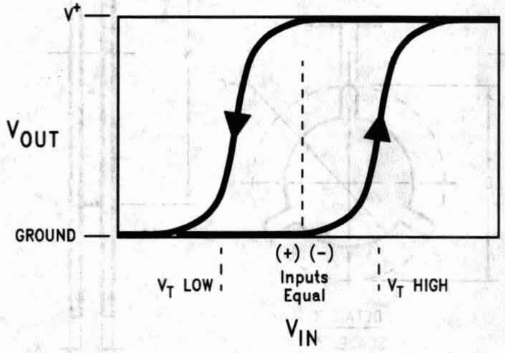
Without Positive Feedback (No Hysteresis)



TL/H/12337-10

FIGURE 5

With Positive Feedback (Hysteresis or Memory)

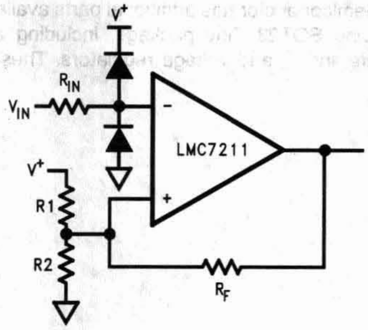


TL/H/12337-11

FIGURE 6

6.0 Input Protection

If input signals are like to exceed the common mode range of the LMC7211, or it is likely that signals may be present when power is off, damage to the LMC7211 may occur. Large value (100 kΩ to MΩ) input resistors may reduce the likelihood of damage by limiting the input currents. Since the LMC7211 has very low input leakage currents, the effect on accuracy will be small. Additional protection may require the use of diodes, as shown in *Figure 7*. Note that diode leakage current may affect accuracy during normal operation. The R-C time constant of R_{IN} and the diode capacitance may also slow response time.



TL/H/12337-12

FIGURE 7

7.0 Layout Considerations

The LMC7211 is not an especially fast comparator, so high speed design practices are not required. The LMC7211 is capable of operating with very high impedance inputs, so precautions should be taken to reduce noise pickup with high impedance (~ 100 kΩ and greater) designs and in electrically noisy environments.

Keeping high value resistors close to the LMC7211 and minimizing the size of the input nodes is a good practice. With multilayer designs, try to avoid long loops which could act as inductors (coils). Sensors which are not close to the comparator may need twisted pair or shielded connections to reduce noise.

8.0 Open Drain Output, Dual and Quad Versions

The LMC7221 is a comparator similar to the LMC7211, but with an open drain output which allows the output voltage to be different (higher or lower) than the supply voltage. The open drain output is like the open collector output of a logic gate. This makes the LMC7221 very useful for mixed voltage systems. Many systems will have different voltages for the analog and microprocessor sections. Please see the LMC7221 datasheet for details.

The performance of the LMC7211 is available in dual devices. Please see the LMC6762 datasheet for details on a dual push-pull output device. For a dual device with open drain outputs, please see the LMC6772 datasheet.

Application Information (Continued)

Rail-to-Rail Input Low Power Comparators—

Push-Pull Output

LMC7211	Tiny, SOT23-5, DIP	Single
LMC6762	SO-8, DIP	Dual

Open Drain Output

LMC7221	Tiny, SOT23-5, DIP	Single
LMC6772	SO-8, DIP	Dual

9.0 Additional SOT23-5 Tiny Devices

National Semiconductor has additional parts available in the space saving SOT23 Tiny package, including amplifiers, voltage references, and voltage regulators. These devices include—

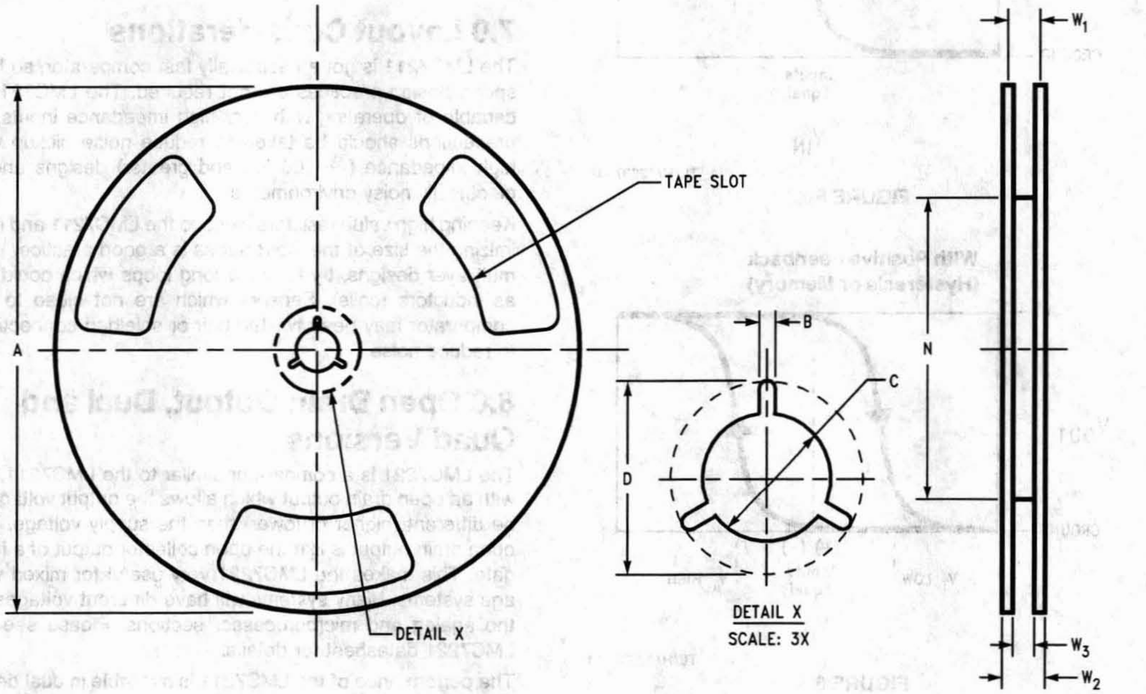
LMC7101	1 MHz gain-bandwidth rail-to-rail input and output amplifier—high input impedance and high gain 700 μA typical current 2.7V, 3V, 5V and 15V specifications.
LMC7111	Low power 50 kHz gain-bandwidth rail-to-rail input and output amplifier with 25 μA typical current specified at 2.7V, 3.0V, 3.3V, 5V and 10V.
LM7131	Tiny Video amp with 70 MHz gain bandwidth 3V, 5V and ±5V specifications.
LP2980	Micropower SOT 50 mA Ultra Low-Dropout Regulator.
LM4040	Precision micropower shunt voltage reference. Fixed voltages of 2.500V, 4.096V, 5.000V, 8.192V and 10.000V.
LM4041	Precision micropower shut voltage reference 1.225V and adjustable.

Contact your National Semiconductor representative for the latest information.

10.0 Spice Macromodel

A Spice Macromodel is available for the LMC7211 comparator on the National Semiconductor Amplifier Macromodel disk. Contact your National Semiconductor representative to obtain the latest version.

REEL DIMENSIONS



TL/H/12337-13

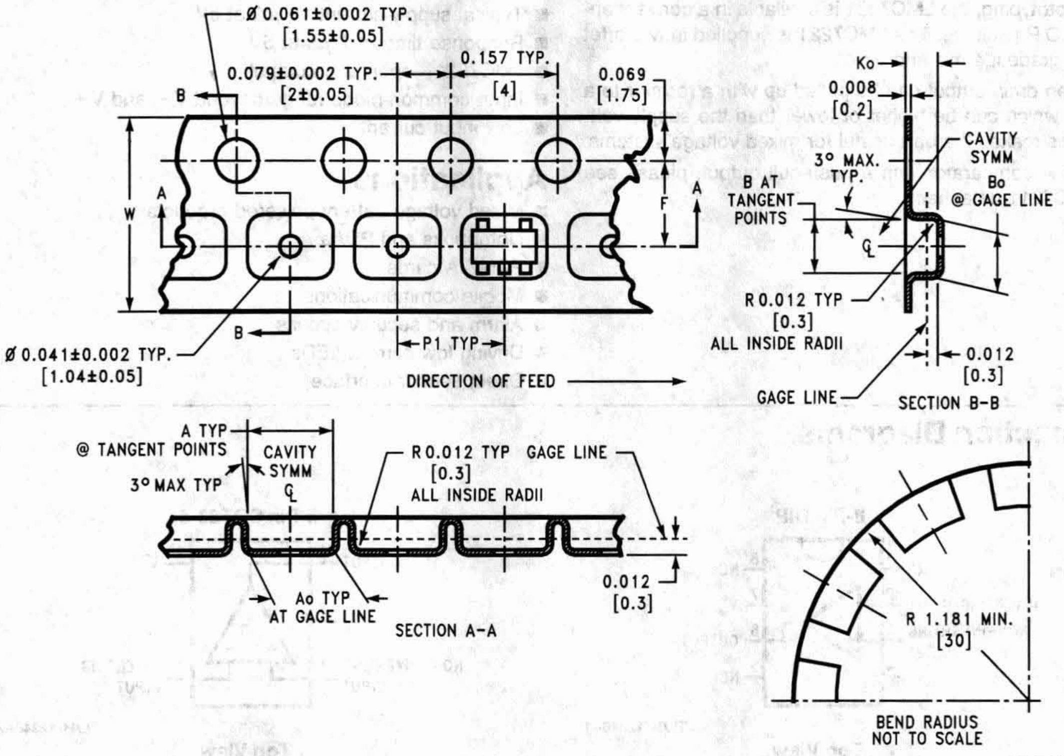
8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/−0.000 8.40 + 1.50/−0.00	0.567 14.40	W1+ 0.078/−0.039 W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

TAPE DIMENSIONS



Ø 0.061±0.002 TYP.
[1.55±0.05]
0.079±0.002 TYP.
[2±0.05]
0.157 TYP.
[4]
0.069
[1.75]
B
W
A
F
A
Ø 0.041±0.002 TYP.
[1.04±0.05]
B
P1 TYP
DIRECTION OF FEED
Ko
0.008
[0.2]
3° MAX.
TYP.
CAVITY
SYMM
Bo
@ GAGE LINE
B AT
TANGENT
POINTS
℄
R 0.012 TYP
[0.3]
ALL INSIDE RADII
0.012
[0.3]
GAGE LINE
SECTION B-B
A TYP
@ TANGENT POINTS
3° MAX TYP
CAVITY
SYMM
℄
R 0.012 TYP
[0.3]
ALL INSIDE RADII
GAGE LINE
0.012
[0.3]
Ao TYP
AT GAGE LINE
SECTION A-A
R 1.181 MIN.
[30]
BEND RADIUS
NOT TO SCALE

TL/H/12337-14

8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

National Semiconductor

ADVANCE INFORMATION

LMC7221
Tiny CMOS Comparator with Rail-To-Rail Input and Open Drain Output

General Description

The LM7221 is a micropower CMOS comparator available in the space saving SOT23-5 package. This makes this comparator ideal for space and weight critical designs. For easy prototyping, the LMC7221 is available in a conventional 8-pin DIP package. The LMC7221 is supplied in two offet voltage grades, 4 mV and 9 mV.

The open drain output can be pulled up with a resistor to a voltage which can be higher or lower than the supply voltage—this makes the part useful for mixed voltage systems.

For a tiny comparator with a push-pull output, please see the LMC7211 datasheet.

Features

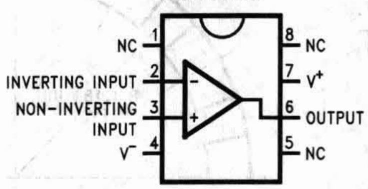
- Tiny SOT 23-5 package saves space
- Package is less than 1.43 mm thick
- Guaranteed specs at 2.7V, 5V, 15V supplies
- Typical supply current 10 µA at 5V
- Response time of 7 µs at 5V
- LMC7221—open drain output
- Input common-mode range beyond V− and V+
- Low input current

Applications

- Mixed voltage battery powered products
- Notebooks and PDAs
- PCMCIA cards
- Mobile communications
- Alarm and security circuits
- Driving low current LEDs
- Direct sensor interface

Connection Diagrams

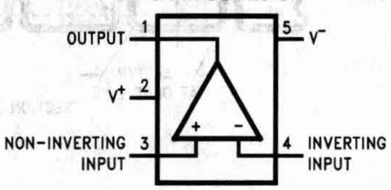
8-Pin DIP



TL/H/12346-1

Top View

5-Pin SOT23-5



TL/H/12346-2

Top View

Ordering Information

Package	Ordering Information	NSC Drawing Number	Package Marking	Transport Media
8-Pin DIP	LMC7221AIN	N08E	LMC7221AIN	Rails
8-Pin DIP	LMC7221BIN	N08E	LMC7221BIN	Rails
5-Pin SOT 23-5	LMC7221AIM5	MA05A	C01A	250 Units on Tape and Reel
5-Pin SOT 23-5	LMC7221BIM5	MA05A	C01B	250 Units on Tape and Reel
5-Pin SOT 23-5	LMC7221AIM5X	MA05A	C01A	3k Units Tape and Reel
5-Pin SOT 23-5	LMC7221BIM5X	MA05A	C01B	3k Units Tape and Reel

National Semiconductor

LP311 Voltage Comparator

General Description

The LP311 is a low power version of the industry-standard LM311. It takes advantage of stable high-value ion-implanted resistors to perform the same function as an LM311, with a 30:1 reduction in power drain, but only a 6:1 slowdown of response time. Thus the LP311 is well suited for battery-powered applications, and all other applications where fast response is not needed. It operates over a wide range of supply voltages from 36V down to a single 3V supply, with less than 200 μA drain, but it is still capable of driving a 25 mA load. The LP311 is quite easy to apply without any oscillation, if ordinary precautions are taken to minimize stray coupling from the output to either input or to the balance pins (as described in the LM311 datasheet Application Hints).

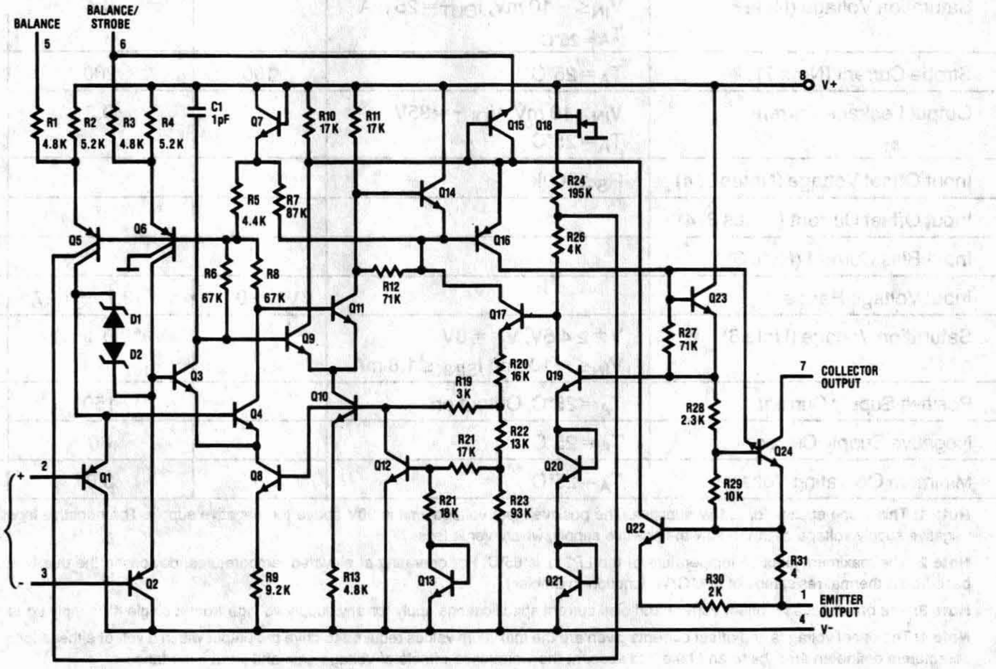
Features

- Low power drain, 900 μW on 5V supply
- Operates from ±15V or a single supply as low as 3V
- Output can drive 25 mA
- Emitter output can swing below negative supply
- Response time: 1.2 μs
- Same pin-out as LM311
- Low input currents: 2 nA of offset, 15 nA of bias
- Large common-mode input range: −14.6V to 13.6V with ±15V supply

Applications

- Level-detector for battery-powered instruments
- Low-power lamp or relay driver
- Low-power zero-crossing detector

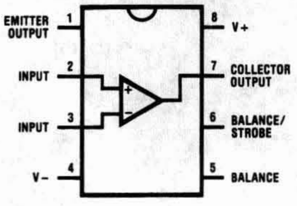
Schematic Diagram


BALANCE
5
BALANCE/STROBE
6
8 V+
R1 4.8K
R2 5.2K
R3 4.8K
R4 5.2K
C1 1pF
Q7
R10 17K
R11 17K
Q15
Q18
R5 4.4K
R7 87K
Q14
R24 195K
Q5
Q6
Q16
R26 4K
R6 67K
R8 67K
R12 71K
Q11
Q17
Q23
D1
D2
Q9
R27 71K
Q3
R20 16K
R19 3K
Q19
7 COLLECTOR OUTPUT
Q4
Q10
R28 2.3K
Q24
R21 17K
R22 13K
2
+
Q1
Q8
Q12
Q20
R29 10K
INPUTS
R21 18K
R23 93K
Q22
3
-
Q2
R9 9.2K
R13 4.8K
Q13
Q21
R31 4
R30 2K
1 EMITTER OUTPUT
4 V-

TL/H/5711–7

Connection Diagram

Dual-In-Line Package


EMITTER OUTPUT 1
INPUT 2
INPUT 3
V− 4
8 V+
7 COLLECTOR OUTPUT
6 BALANCE/STROBE
5 BALANCE
+
−

TL/H/5711–4

Top View

Order Number LP311M or LP311N
See NS Package Numbers M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage (V_{8-4})	36V
Collector Output to Negative Supply Voltage (V_{7-4})	40V
Collector Output to Emitter Output	40V
Emitter Output to Negative Supply Voltage (V_{1-4})	±30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics

These specifications apply for $V_S = \pm 15V$ and $0°C \le T_A \le 70°C$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Notes 3, 4)	$T_A = 25°C$, $R_S \le 100k$		2.0	7.5	mV
Input Offset Current (Notes 3, 4)	$T_A = 25°C$		2.0	25	nA
Input Bias Current (Note 3)	$T_A = 25°C$		15	100	nA
Voltage Gain	$T_A = 25°C$, $R_L = 5k$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		1.2		μs
Saturation Voltage (Note 6)	$V_{IN} \le -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.4	1.5	V
Strobe Current (Note 7)	$T_A = 25°C$	100	200	300	μA
Output Leakage Current	$V_{IN} \ge 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	100	nA
Input Offset Voltage (Notes 3, 4)	$R_S \le 100k$			10	mV
Input Offset Current (Notes 3, 4)				35	nA
Input Bias Current (Note 3)				150	nA
Input Voltage Range		$V^- + 0.5$	+13.7, −14.7	$V^+ - 1.5$	V
Saturation Voltage (Note 6)	$V^+ \ge 4.5V$, $V^- = 0V$ $V_{IN} \le -10$ mV, $I_{SINK} \le 1.6$ mA		0.1	0.4	V
Positive Supply Current	$T_A = 25°C$, Output on		150	300	μA
Negative Supply Current	$T_A = 25°C$		80	180	μA
Minimum Operating Voltage	$T_A = 25°C$		3.0	3.5	V

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LP311 is 85°C. For operating at elevated temperatures, devices in the dual-in-line package must be derated based on a thermal resistance of 160°C/W, junction to ambient.

Note 3: The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 4V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

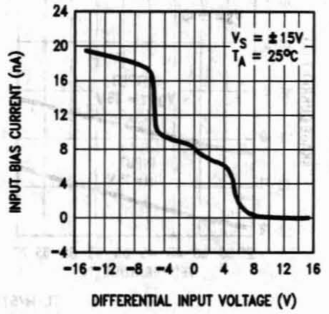
Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Note 6: Saturation voltage specification applies to collector-emitter voltage (V7-1) for $V_{COLLECTOR} \le (V^+ - 3V)$.

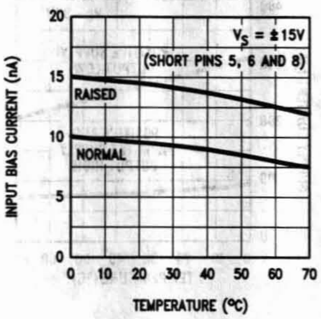
Note 7: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground. It should be current driven, 100 μA to 300 μA.

Typical Performance Characteristics

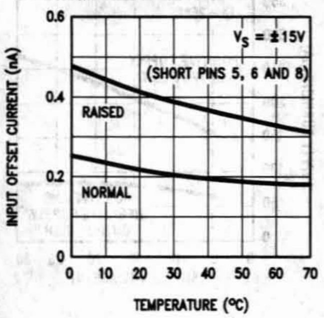
Input Characteristics



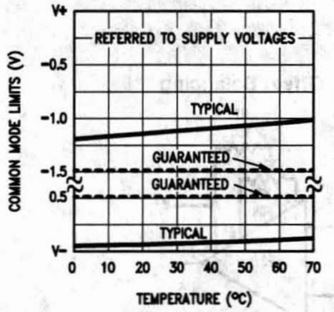
Input Bias Current



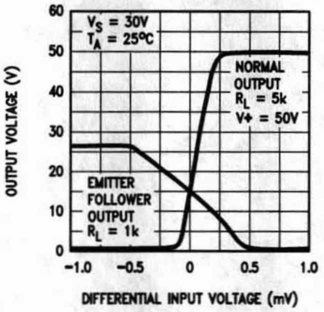
Input Offset Current



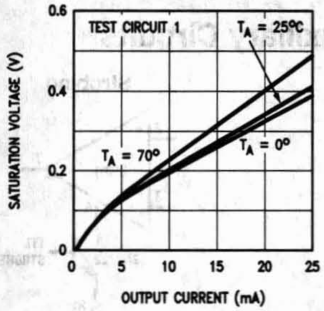
Common Mode Limits



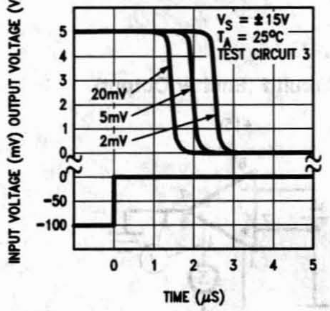
Transfer Function



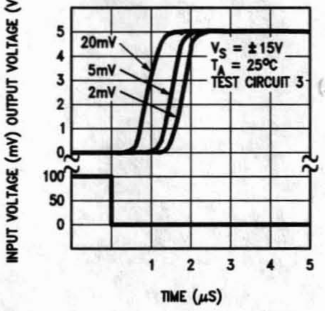
Output Saturation Voltage (Collector Output)



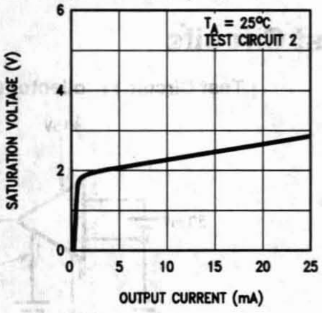
Response Time for Various Input Overdrives



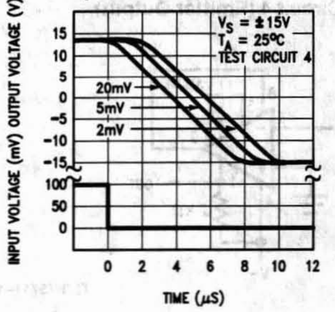
Response Time for Various Input Overdrives



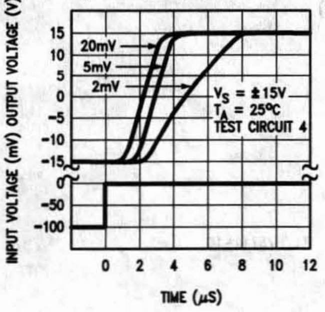
Output Saturation Voltage (Emitter Output)



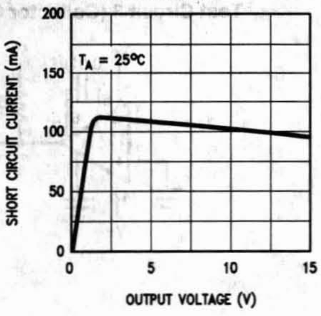
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

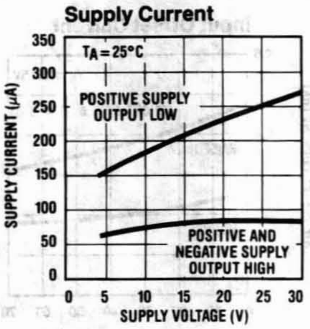


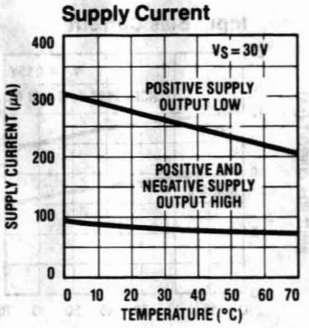
Output Limiting Characteristics

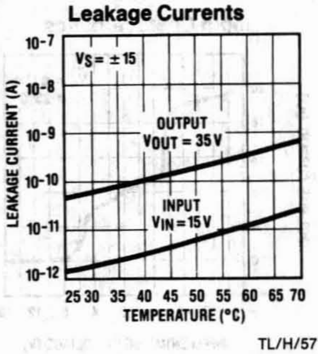


TL/H/5711-5

Typical Performance Characteristics (Continued)


Supply Current


Supply Current


Leakage Currents

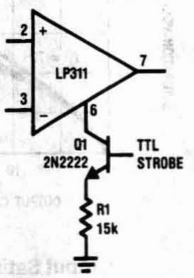
TL/H/5711–6

Applications Information

For applications information and typical applications, refer to the LM311 datasheet.

Auxiliary Circuits

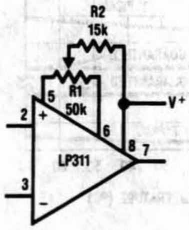
Strobing


2
+
3
−
LP311
7
6
Q1
2N2222
TTL
STROBE
R1
15k

TL/H/5711–1

Note: Do not ground strobe pin.

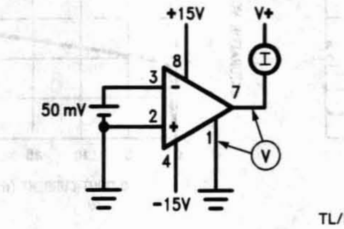
Offset Balancing


R2
15k
R1
50k
5
6
V+
2
+
8
7
LP311
3
−

TL/H/5711–2

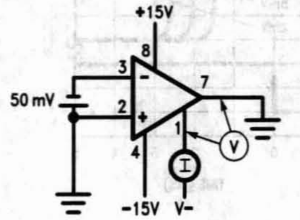
Test Circuits

Test Circuit 1 (Collector Output)


+15V
V+
I
8
3
−
7
50 mV
2
+
1
4
V
−15V

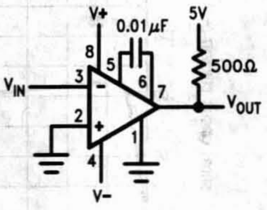
TL/H/5711–8

Test Circuit 2 (Emitter Output)


+15V
8
3
−
7
50 mV
2
+
1
V
4
I
−15V
V−

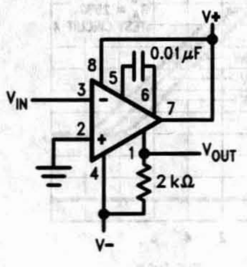
TL/H/5711–9

Test Circuit 3 (Collector Output)


V+
0.01µF
5V
8
5
6
500Ω
VIN
3
−
7
VOUT
2
+
1
4
V−

TL/H/5711–10

Test Circuit 4 (Emitter Output)


V+
0.01µF
8
5
6
VIN
3
−
7
2
+
VOUT
1
4
2 kΩ
V−

TL/H/5711–11

National Semiconductor

LP339 Ultra-Low Power Quad Comparator

General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 μA of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

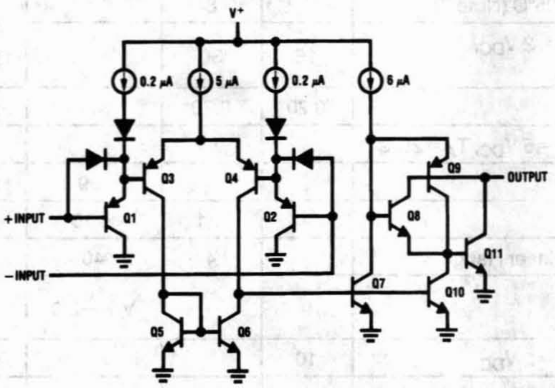
Advantages

- Ultra-low power supply drain suitable for battery applications
- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

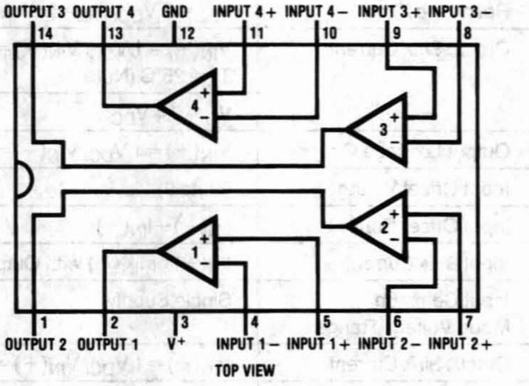
Features

- Ultra-low power supply current drain (60 μA)—independent of the supply voltage (75 μW/comparator at +5 V_{DC})
- Low input biasing current 3 nA
- Low input offset current ±0.5 nA
- Low input offset voltage ±2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at $V_O = 2\ V_{DC}$)
- Supply Input protected against reverse voltages

Schematic and Connection Diagrams


V+
0.2 μA
5 μA
0.2 μA
6 μA
Q3
Q4
Q9
OUTPUT
+INPUT
Q1
Q2
Q8
Q11
−INPUT
Q7
Q10
Q5
Q6

TL/H/5226–1


OUTPUT 3
OUTPUT 4
GND
INPUT 4+
INPUT 4−
INPUT 3+
INPUT 3−
14
13
12
11
10
9
8
4
3
1
2
1
2
3
4
5
6
7
OUTPUT 2
OUTPUT 1
V+
INPUT 1−
INPUT 1+
INPUT 2−
INPUT 2+
TOP VIEW

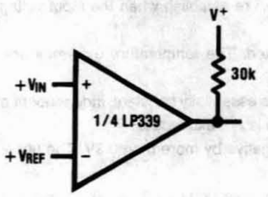
TL/H/5226–2

Order Number LP339M for S.O. Package
See NS Package Number M14A

Order Number LP339N for Dual-In-Line Package
See NS Package Number N14A

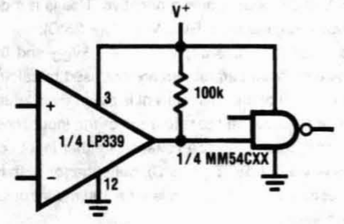
Typical Applications ($V^+ = 5.0\ V_{DC}$)

Basic Comparator


V+
30k
+VIN
+VREF
1/4 LP339

TL/H/5226–3

Driving CMOS


V+
100k
3
12
1/4 LP339
1/4 MM54CXX

TL/H/5226–4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	±36 V_{DC}
Input Voltage	−0.3 V_{DC} to 36 V_{DC}
Power Dissipation (Note 1) Molded DIP	570 mW
Output Short Circuit to GND (Note 2)	Continuous
Input Current $V_{IN} < -0.3$ V_{DC} (Note 3)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65° to +150°C
Soldering Information:	
Dual-In-Line Package (10 sec.)	+260°C
S.O. Package:	
Vapor Phase (60 sec.)	+215°C
Infrared (15 sec.)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (V+ = 5 V_{DC}, Note 4)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25°C$ (Note 9)		±2	±5	mV_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with the Output in the Linear Range, $T_A = 25°C$ (Note 5)		2.5	25	nA_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$, $T_A = 25°C$		±0.5	±5	nA_{DC}
Input Common Mode Voltage Range	$T_A = 25°C$ (Note 6)	0		V+ −1.5	V_{DC}
Supply Current	R_L = Infinite on all Comparators, $T_A = 25°C$		60	100	μA_{DC}
Voltage Gain	$V_O = 1$ V_{DC} to 11 V_{DC}, $R_L = 15$ kΩ, V+ = 15 V_{DC}, $T_A = 25°C$		500		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4$ V_{DC}, $V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ, $T_A = 25°C$		1.3		μSec
Response Time	$V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ, $T_A = 25°C$ (Note 7)		8		μSec
Output Sink Current	$V_{IN}(-) = 1$ V_{DC}, $V_{IN}(+) = 0$, $V_O = 2$ V_{DC}, $T_A = 25°C$ (Note 11)	15	30		mA_{DC}
	$V_O = 0.4$ V_{DC}	0.20	0.70		mA_{DC}
Output Leakage Current	$V_{IN}(+) = 1$ V_{DC}, $V_{IN}(-) = 0$, $V_O = 5$ V_{DC}, $T_A = 25°C$		0.1		nA_{DC}
Input Offset Voltage	(Note 9)			±9	mV_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$		±1	±15	nA_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range		4	40	nA_{DC}
Input Common Mode Voltage Range	Single Supply	0		V+ −2.0	V_{DC}
Output Sink Current	$V_{IN}(-) = 1$ V_{DC}, $V_{IN}(+) = 0$, $V_O = 2$ V_{DC}	10			mA_{DC}
Output Leakage Current	$V_{IN}(+) = 1$ V_{DC}, $V_{IN}(-) = 0$, $V_O = 30$ V_{DC}			1.0	μA_{DC}
Differential Input Voltage	All $V_{IN's} \geq 0$ V_{DC} (or V− on split supplies) (Note 8)			36	V_{DC}

Note 1: For elevated temperature operation, T_j max is 125°C for the LP339. θ_{ja} (junction to ambient) is 175°C/W for the LP339N and 120°C/W for the LP339M when either device is soldered in a printed circuit board in a still air environment. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 50 mA.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input clamp diodes. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V+ voltage level (or to ground for a large input overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than −0.3 V_{DC} ($T_A = 25°C$).

Note 4: These specifications apply for V+ = 5V_{DC} and $0°C \leq T_A \leq 70°$ C, unless otherwise stated. The temperature extremes are guaranteed but not 100% production tested. These parameters are not used to calculate outgoing AQL.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or the input lines as long as the common-mode range is not exceeded.

Note 6: The input common-mode voltage or either input voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V ($T_A = 25°C$), but either or both inputs can go to 30 V_{DC} without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 1.3 μs can be obtained. See Typical Performance Characteristics section.

Electrical Characteristics (V+ = 5 V_{DC}, Note 4) (Continued)

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) at $T_A = 25°C$.

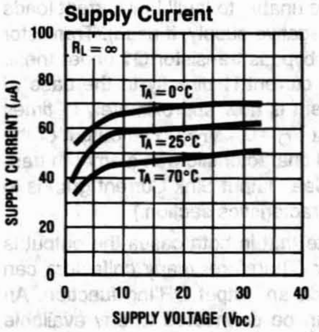
Note 9: At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5 V_{DC}; and over the full input common-mode range (0 V_{DC} to V+ −1.5 V_{DC}).

Note 10: For input signals that exceed V+, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

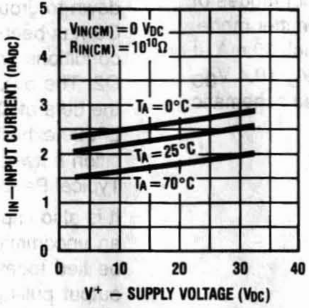
Note 11: The output sink current is a function of the output voltage. The LP339 has a bi-modal output section which allows it to sink large currents via a Darlington connection at output voltages greater than approximately 1.5 V_{DC} and sink lower currents below this point. (See typical characteristics section and applications section).

Typical Performance Characteristics

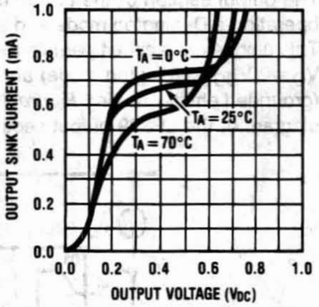
Supply Current



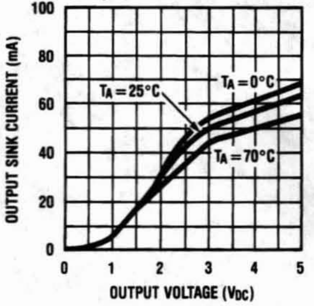
Input Current



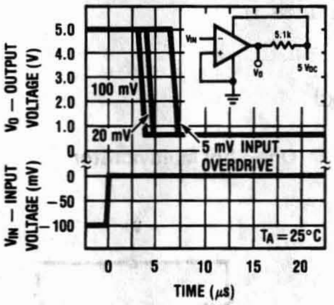
Output Sink Current



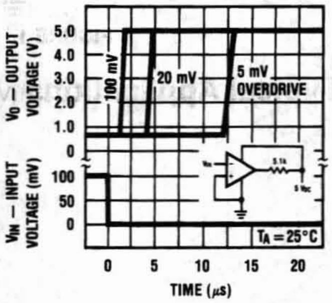
Output Sink Current



Response Times for Various Input Overdrives — Negative Transition



Response Times for Various Input Overdrives — Positive Transition



TL/H/5226-10

Application Hints

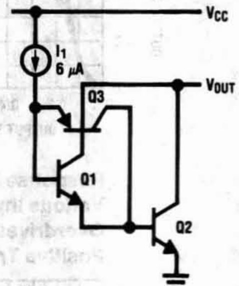
All pins of any unused comparators should be grounded.

The bias network of the LP339 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the application section.

The output section of the LP339 has two distinct modes of operation-a Darlington mode and a grounded emitter mode. This unique drive circuit permits the LP339 to sink 30 mA at $V_O = 2\ V_{DC}$ (Darlington mode) and 700 μA at $V_O = 0.4\ V_{DC}$ (grounded emitter mode). *Figure 1* is a simplified schematic diagram of the LP339 output section.



TL/H/5226–11

FIGURE 1

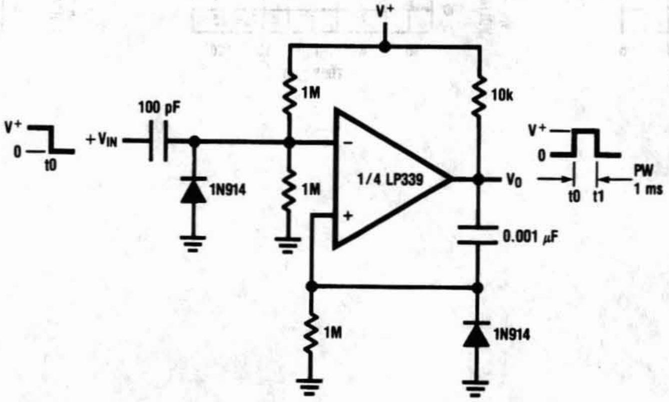
Notice that the output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough ($V_O \geq 1\ V_{DC}$), Q1 is not saturated and the output current is limited only by the product of the betas of Q1, Q2 and I1 (and the 60Ω R_{SAT} of Q2). The LP339 is thus capable of driving LED's, relays, etc. in this mode while maintaining an ultra-low power supply current of typically 60 μA.

If transistor Q3 were omitted, and the output voltage allowed to drop below about 0.8 V_{DC}, transistor Q1 would saturate and the output current would drop to zero. The circuit would, therefore, be unable to 'pull' low current loads down to ground (or the negative supply, if used). Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the beta of Q2 (700 μA at $V_O = 0.4\ V_{DC}$). The output of the LP339 exhibits a bi-modal characteristic with a smooth transition between modes. (See Output Sink Current graphs in Typical Performance Characteristics section.)

It is also important to note that in both cases the output is an uncommitted collector. Therefore, many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the LP339 package.

Typical Applications ($V^+ = 15\ V_{DC}$)

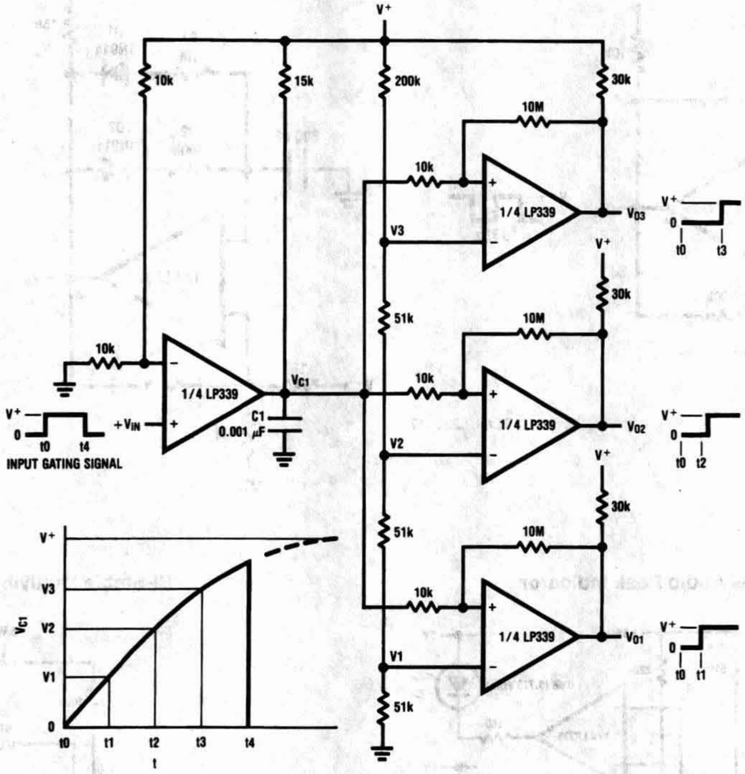
One-Shot Multivibrator



TL/H/5226–13

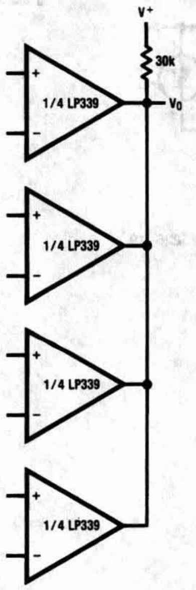
Typical Applications ($V^+ = 15\ V_{DC}$)

Time Delay Generator


V+
10k
15k
200k
30k
10M
10k
1/4 LP339
V03
V+
0
t0
t3
V3
51k
30k
10M
10k
1/4 LP339
V02
t0
t2
V2
10k
1/4 LP339
VC1
C1
0.001 μF
+VIN
V+
0
t0
t4
INPUT GATING SIGNAL
51k
30k
10M
10k
1/4 LP339
V01
t0
t1
V1
51k
V+
V3
V2
V1
0
VC1
t0
t1
t2
t3
t4
t

TL/H/5226–15

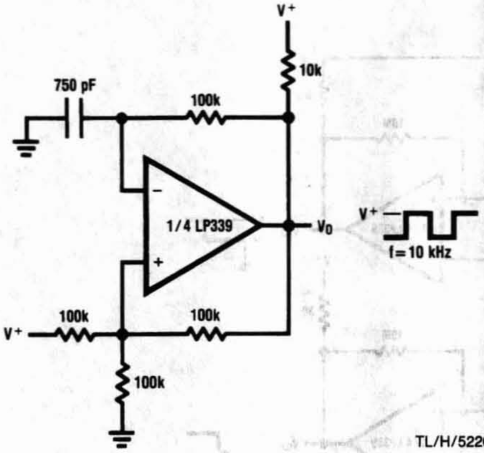
ORing the Outputs


V+
30k
VO
1/4 LP339
1/4 LP339
1/4 LP339
1/4 LP339

TL/H/5226–16

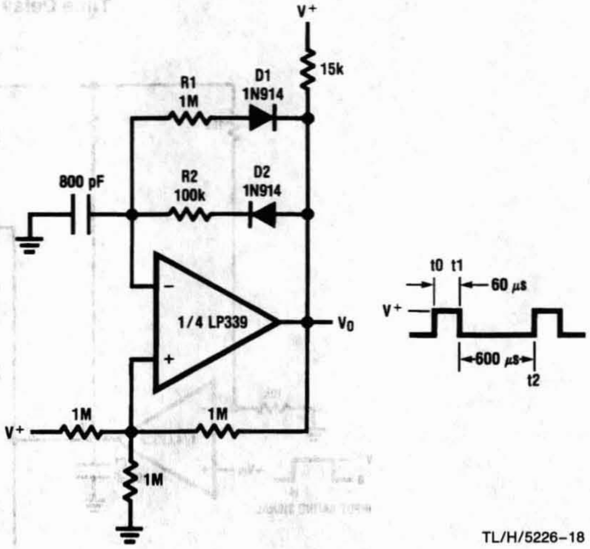
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)

Squarewave Oscillator


V+
10k
750 pF
100k
1/4 LP339
V0
V+
f = 10 kHz
100k
100k
100k

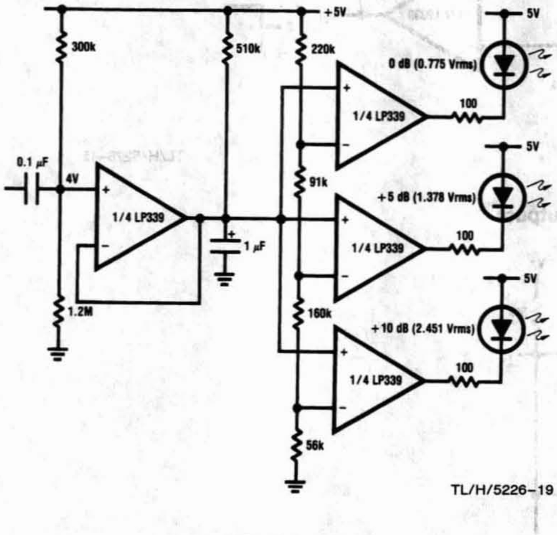
TL/H/5226-17

Pulse Generator


V+
15k
R1
1M
D1
1N914
800 pF
R2
100k
D2
1N914
1/4 LP339
V0
t0 t1
60 µs
V+
600 µs
t2
1M
1M
1M

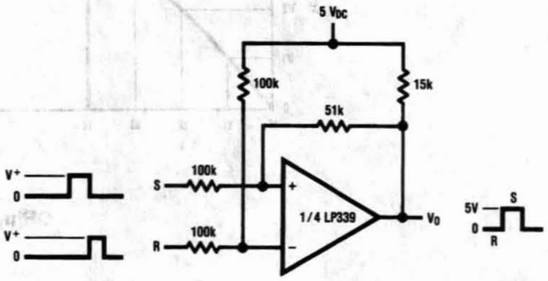
TL/H/5226-18

Three Level Audio Peak Indicator


+5V
300k
510k
220k
5V
0 dB (0.775 Vrms)
1/4 LP339
100
0.1 µF
4V
1/4 LP339
91k
5V
+5 dB (1.378 Vrms)
1 µF
1/4 LP339
100
1.2M
160k
5V
+10 dB (2.451 Vrms)
1/4 LP339
100
56k

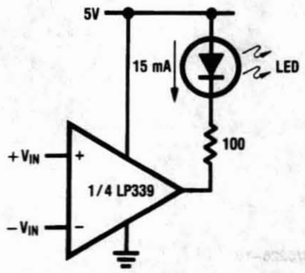
TL/H/5226-19

Bi-Stable Multivibrator


5 VDC
100k
15k
51k
V+
0
S
100k
1/4 LP339
V0
V+
0
R
100k
5V
0
S
R

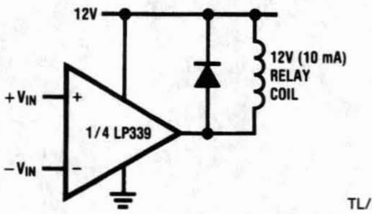
TL/H/5226-21

LED Driver


5V
15 mA
LED
100
+VIN
1/4 LP339
−VIN

TL/H/5226-22

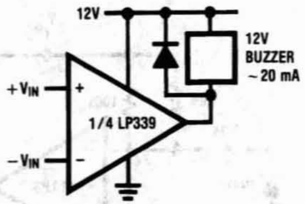
Relay Driver


12V
12V (10 mA)
RELAY
COIL
+VIN
1/4 LP339
−VIN

TL/H/5226-23

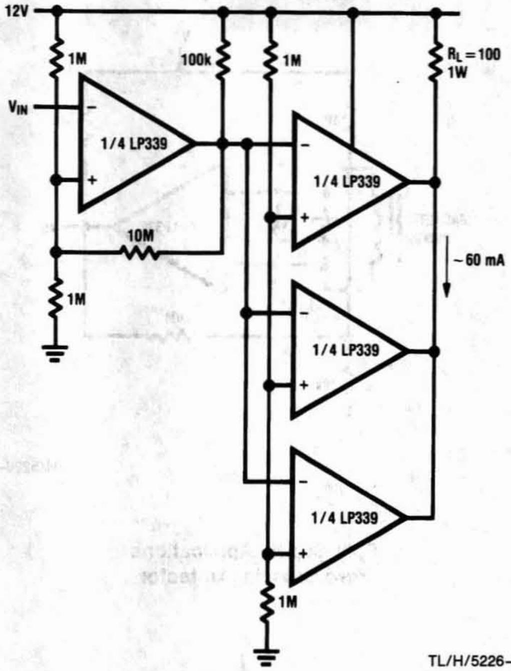
Typical Applications (Continued) (Single Supply)

Buzzer Driver


12V
12V
BUZZER
~20 mA
+VIN
1/4 LP339
−VIN

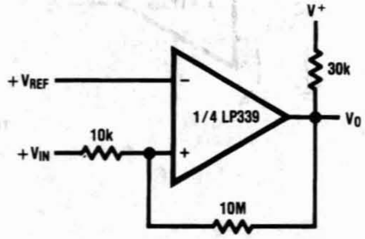
TL/H/5226-24

Comparator With 60 mA Sink Capability


12V
1M
100k
1M
RL = 100
1W
VIN
1/4 LP339
1/4 LP339
~60 mA
10M
1M
1/4 LP339
1/4 LP339
1M

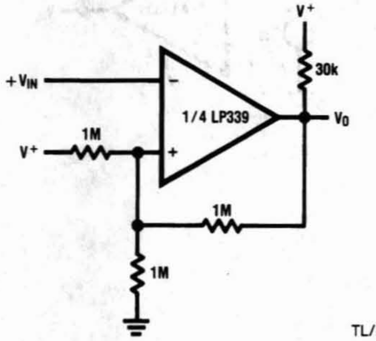
TL/H/5226-25

Non-Inverting Comparator with Hysteresis


V+
30k
+VREF
1/4 LP339
VO
10k
+VIN
10M

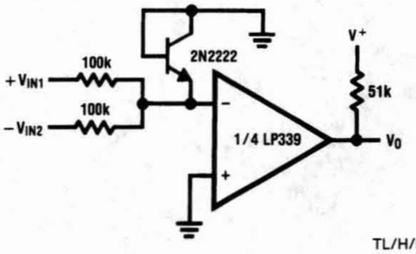
TL/H/5226-26

Inverting Comparator with Hysteresis


V+
30k
+VIN
1/4 LP339
VO
1M
V+
1M
1M

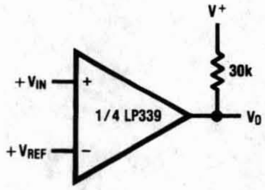
TL/H/5226-27

Comparing Input Voltages of Opposite Polarity


2N2222
V+
100k
+VIN1
51k
100k
−VIN2
1/4 LP339
VO

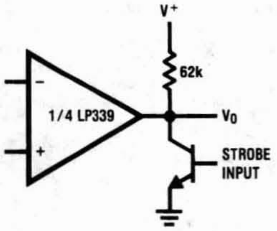
TL/H/5226-28

Basic Comparator


V+
30k
+VIN
1/4 LP339
VO
+VREF

TL/H/5226-29

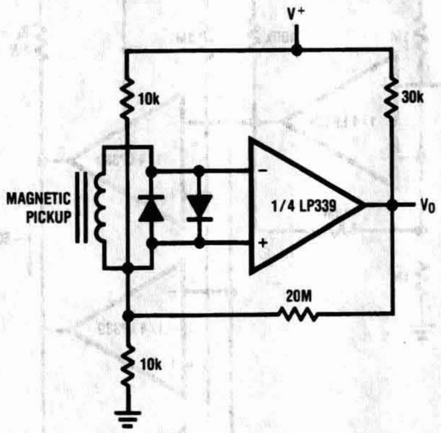
Output Strobing


V+
62k
1/4 LP339
VO
STROBE
INPUT

TL/H/5226-30

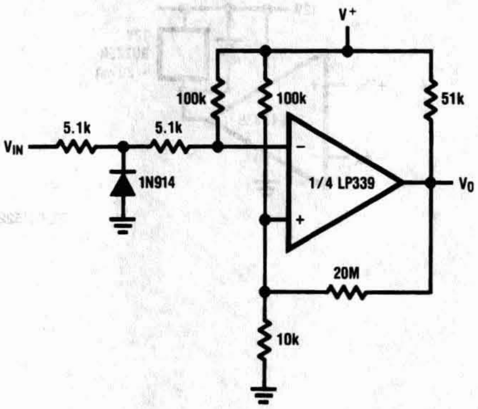
Typical Applications (Continued) (Single Supply)

Transducer Amplifier


V+
10k
30k
MAGNETIC PICKUP
1/4 LP339
VO
20M
10k

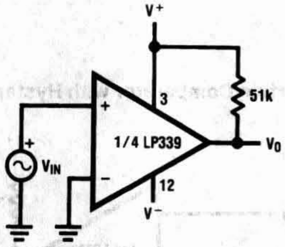
TL/H/5226-31

Zero Crossing Detector (Single Power Supply)


V+
100k
100k
51k
5.1k
5.1k
VIN
1N914
1/4 LP339
VO
20M
10k

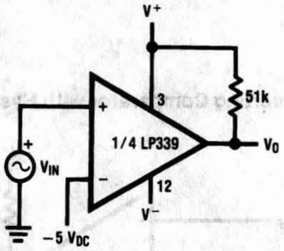
TL/H/5226-32

Split-Supply Applications Zero Crossing Detector


V+
51k
3
1/4 LP339
VIN
VO
12
V−

TL/H/5226-33

Comparator With a Negative Reference


V+
51k
3
1/4 LP339
VIN
VO
12
V−
−5 VDC

TL/H/5226-34

Section 4

Active Matrix/LCD Display Drivers

Section 4 Contents

LM6104 Quad Gray Scale Current Feedback Amplifier 4-3
LM8305 STN LCD Display Bias Voltage Source 4-7
LMC6008 8 Channel Buffer 4-8

National Semiconductor

LM6104
Quad Gray Scale Current Feedback Amplifier

General Description

The LM6104 quad amplifier meets the requirements of battery operated liquid crystal displays by providing high speed while maintaining low power consumption.

Combining this high speed with high integration, the LM6104 conserves valuable board space in portable systems with a cost effective, surface mount quad package.

Built on National's advanced high speed VIP™ (Vertically Integrated PNP) process, the LM6104 current feedback architecture is easily compensated for speed and loading conditions. These features make the LM6104 ideal for buffering grey levels in liquid crystal displays.

Features (Typical unless otherwise noted)

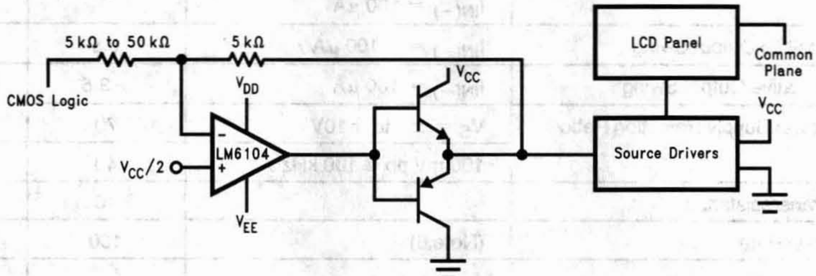
Low power	I_S = 875 μA/amplifier
Slew rate	100V/μs
−3dB bandwidth (R_F = 1 kΩ)	30 MHz
High output drive	±5V into 100Ω
Wide operating range	V_S = 5V to ±12V
High integration	Quad surface mount

Applications

- Grey level buffer for liquid crystal displays
- Column buffer for portable LCDs
- Video distribution amplifiers, video line drivers
- Hand-held, high speed signal conditioning

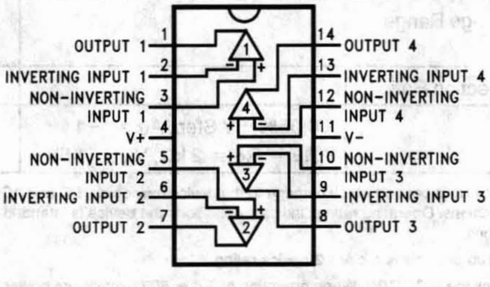
Typical Application

LCD Buffer Application for Grey Levels


5 kΩ to 50 kΩ
5 kΩ
CMOS Logic
V_{DD}
LM6104
$V_{CC}/2$
V_{EE}
V_{CC}
LCD Panel
Common Plane
V_{CC}
Source Drivers

TL/H/11979–1

Connection Diagram


OUTPUT 1
INVERTING INPUT 1
NON-INVERTING INPUT 1
V+
NON-INVERTING INPUT 2
INVERTING INPUT 2
OUTPUT 2
OUTPUT 4
INVERTING INPUT 4
NON-INVERTING INPUT 4
V−
NON-INVERTING INPUT 3
INVERTING INPUT 3
OUTPUT 3
1
2
3
4
5
6
7
14
13
12
11
10
9
8

TL/H/11979–2

Order Number LM6104M
See NS Package Number M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	24V
Differential Input Voltage	±6V
Input Voltage	±Supply Voltage
Inverting Input Current	15 mA
Soldering Information	
Vapor Phase (60s)	215°C
Infrared (15s)	220°C
Storage Temperature Range	$-65°C \leq T_J \leq +150°C$
Maximum Junction Temperature	150°C
ESD Rating (Note 2)	2000V

Operating Ratings

Supply Voltage Range	4.75V to 24V
Junction Temperature Range (Note 3)	
LM6104M	$-20° \leq T_J \leq +80°C$

Electrical Characteristics

The following specifications apply for $V+ = 8V$, $V- = -5V$, $R_L = R_F = 2\ k\Omega$ and $0° \leq T_J \leq 60°C$ unless otherwise noted.

Symbol	Parameter	Conditions	LM6104M Typical (Note 4)	LM6104M Limits (Note 5)	Units
V_{OS}	Input Offset Voltage		10	30	mV max
I_B	Inverting Input Bias Current		5.0	20	μA max
	Non-Inverting Input Bias Current		0.5	2	μA max
I_S	Supply Current	$V_O = 0V$	3.5	4.0	mA max
I_{SC}	Output Source Current	$V_O = 0V$ $I_{IN(-)} = -100\ \mu A$	60	45	mA min
	Output Sink Current	$V_O = 0V$ $I_{IN(-)} = 100\ \mu A$	60	45	mA min
V_O	Positive Output Swing	$I_{IN(-)} = -100\ \mu A$	6.5	6.1	V min
	Negative Output Swing	$I_{IN(-)} = 100\ \mu A$	−3.5	−3.1	V max
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4$ to $\pm 10V$	70	60	dB min
		100 mV pp @ 100 kHz	40	30	dB min
R_T	Transresistance		10	5	MΩ min
SR	Slew Rate	(Note 6)	100	55	V/μs min
BW	Bandwidth	$A_V = -1$ $R_{IN} = R_F = 2\ k\Omega$	7.5	5.0	MHz
	Amp-to-Amp Isolation	$R_L = 2\ k\Omega$ $F = 1\ MHz$	60		dB
CMVR	Common Mode Voltage Range		$V^+ - 1.4V$ $V^- + 1.4V$		V
CMRR	Common Mode Rejection Ratio		60		dB
t_S	Settling Time	0.05%, 5V Step, $A_V = -1$ $R_F = R_S = 2\ k\Omega$, $V_S = \pm 5V$	240		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under the conditions.

Note 2: Human body model 1.5 kΩ and 100 pF. This is a class 2 device rating.

Note 3: Thermal resistance of the SO package is 98°C/W. When operating at $T_A = 80°C$, maximum power dissipation is 700 mW.

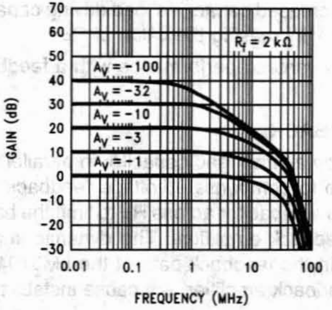
Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits guaranteed at operating temperature extremes.

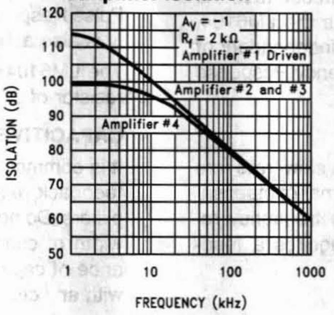
Note 6: $A_V = -1$ with $R_{IN} = R_F = 2\ k\Omega$. Slew rate is calculated from the 25% to the 75% point on both rising and falling edges. Output swing is −0.6V to +5.6V and 5.6V to 0.6V.

Typical Performance Characteristics

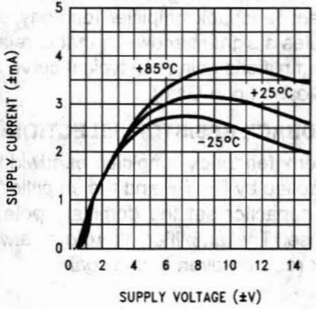
Frequency Response vs Closed Loop Gain



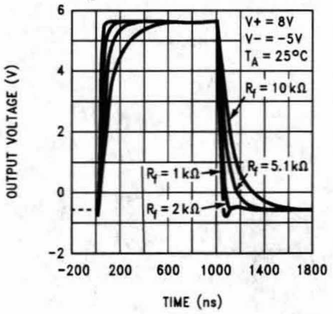
Amplifier to Amplifier Isolation



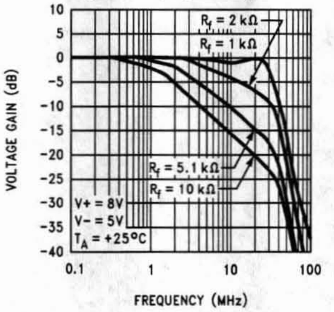
Supply Current vs Supply Voltage



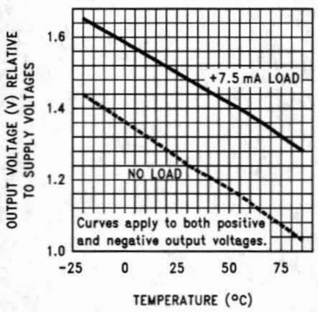
Large Signal Pulse Response
$A_V = -1$



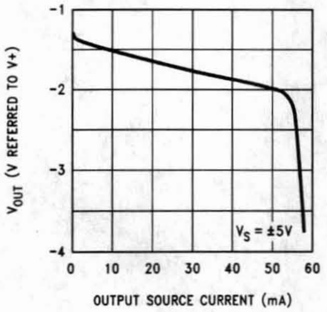
Frequency Response vs R_F
$A_V = -1, R_F = R_G$



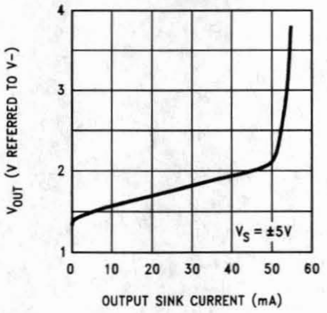
V_{OUT} Referred to Supplies
$V_S = \pm 5V$
$I_{IN} = \pm 100\ \mu A$



LM6104 Output Voltage vs Source Current



LM6104 Output Voltage vs Sink Current



TL/H/11979-3

Applications Information

CURRENT FEEDBACK TOPOLOGY

The small-signal bandwidth of conventional voltage feedback amplifiers is inversely proportional to the closed-loop gain based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6104, enables a signal bandwidth that is relatively independent of the amplifier's gain (see typical curve Frequency Response vs Closed Loop Gain).

FEEDBACK RESISTOR SELECTION: R_F

Current feedback amplifier bandwidth and slew rate are controlled by R_F. R_F and the amplifier's internal compensation capacitor set the dominant pole in the frequency response. The amplifier, therefore, always requires a feedback resistor, even in unity gain.

Bandwidth and slew rate are inversely proportional to the value of R_F (see typical curve Frequency Response vs R_F). This makes the amplifier especially easy to compensate for a desired pulse response (see typical curve Large Signal Pulse Response). Increased capacitive load driving capability is also achieved by increasing the value of R_F.

The LM6104 has guaranteed performance with a feedback resistor of 2 kΩ.

CAPACITIVE FEEDBACK

It is common to place a small lead capacitor in parallel with feedback resistance to compensate voltage feedback amplifiers. Do not place a capacitor across R_F to limit the bandwidth of current feedback amplifiers. The dynamic impedance of capacitors in the feedback path of the LM6104, as with any current feedback amplifier, will cause instability.

National Semiconductor

LM8305—STN LCD Display Bias Voltage Source

General Description

The LM8305M contains five buffered voltage sources to provide the voltage ratios required to drive a standard STN LCD display panel using a time-multiplexed voltage waveform to activate, or deactivate, a pixel once every picture frame. The internal resistor array features a binary weighted array to allow the user to select the proper ratio for the display being driven. The user can use an external resistor to set the ratio, if desired.

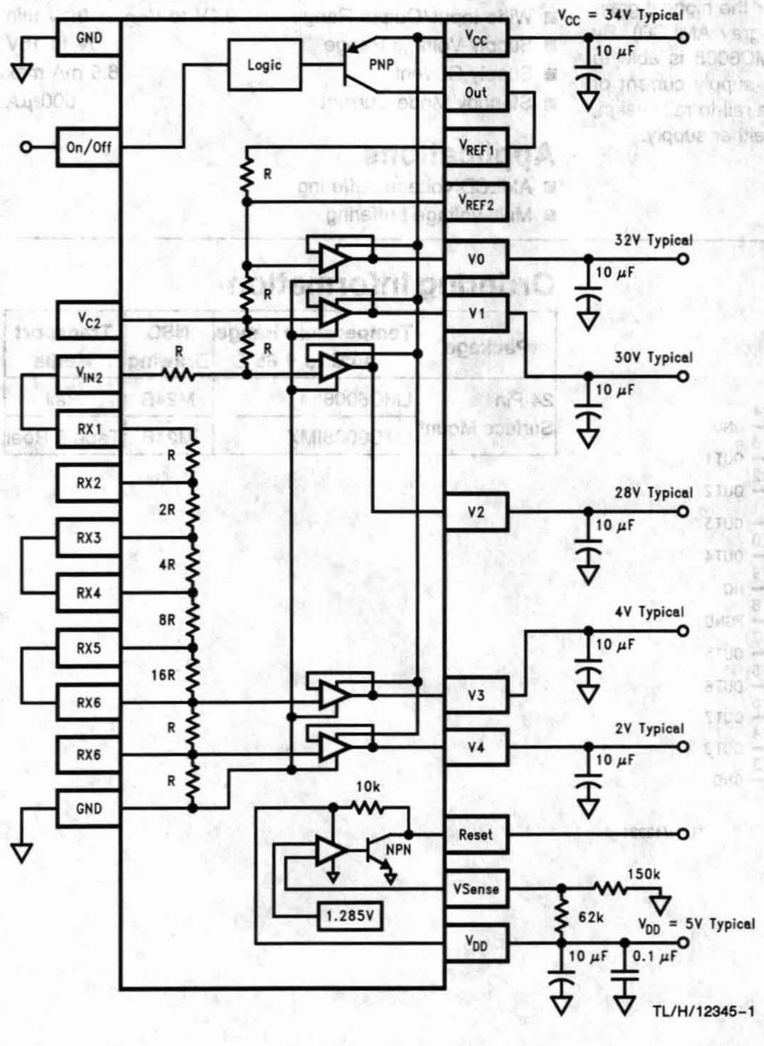
The LM8305 has a maximum operating supply voltage of 50V to support higher multiplexing rates.

The LM8305 also features an internal high side PNP switch, and an independent voltage comparator with an internal bandgap reference.

Features

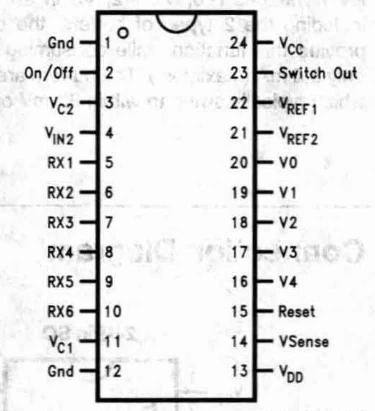
- High operating voltages, 50V maximum
- Internal resistor array with binary weighting
- Ratios from 1/6 to 1/37
- Optional external resistors
- High-side PNP switch from V_{CC}
- Separate voltage comparator circuit with band-gap voltage reference
- Surface mount 24-pin package

Typical Application


V_{CC} = 34V Typical
10 µF
GND
Logic
PNP
V_{CC}
Out
On/Off
V_{REF1}
R
V_{REF2}
32V Typical
V0
10 µF
R
V1
V_{C2}
R
30V Typical
V_{IN2}
R
10 µF
RX1
R
RX2
2R
V2
28V Typical
10 µF
RX3
4R
RX4
8R
4V Typical
RX5
16R
10 µF
V3
RX6
R
2V Typical
RX6
V4
10 µF
R
GND
10k
Reset
NPN
VSense
150k
1.285V
62k
V_{DD} = 5V Typical
V_{DD}
10 µF
0.1 µF

TL/H/12345-1

Connection Diagram


Gnd 1
On/Off 2
V_{C2} 3
V_{IN2} 4
RX1 5
RX2 6
RX3 7
RX4 8
RX5 9
RX6 10
V_{C1} 11
Gnd 12
24 V_{CC}
23 Switch Out
22 V_{REF1}
21 V_{REF2}
20 V0
19 V1
18 V2
17 V3
16 V4
15 Reset
14 VSense
13 V_{DD}

TL/H/12345-2

Top View

See NS Package Number M24B
Order Number LM8305M

National Semiconductor

LMC6008
8 Channel Buffer

General Description

The LMC6008 octal buffer is designed for use in an active matrix liquid-crystal display (AMLCD), specifically to buffer the gray-level voltages going to the inputs of the column driver integrated circuits. In an 8-gray-level (512 color) or 16-gray-level (4096 color) AMLCD, the function of the column drivers is to switch the gray-level voltage inputs to the AMLCD columns. Thus, the voltage buffers must be able to drive the column capacitance of the entire display panel. The LMC6008 AC characteristics, including settling time, are specified for a capacitive load of 0.1 μF for this reason.

The LMC6008 contains 4 high-speed buffers and 4 low-power buffers. The high-speed buffers can provide an output current of at least 250 mA (minimum), and the low-power buffers can provide at least 150 mA (minimum). The high-speed buffers are intended to be used for the highest gray-level voltages (V0, V1, V2, V3 in an 8-gray AMLCD). By including the 2 types of buffers, the LMC6008 is able to provide this function while consuming a supply current of only 6.5 mA (maximum). The buffers are a rail-to-rail design, which typically swing to within 30 mV of either supply.

The LMC6008 also contains a standby function which puts the buffer into a high-impedance mode. The supply current in the standby mode is a low 500 μA max. Also, a thermal limit circuit is included to protect the device from overload conditions.

Features

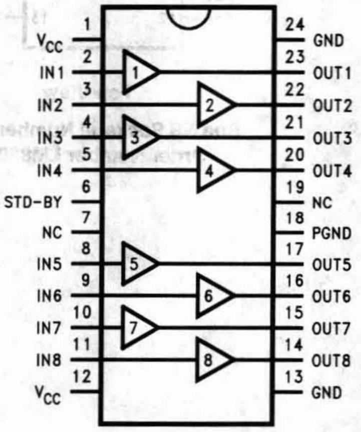
- High Output Current:
  - High Speed Buffers 250 mA min
  - Low Power Buffers 150 mA min
- Slew Rate:
  - High Speed Buffers 1.7 V/μs
  - Low Power Buffers 0.85V/μs
- Settling Time, $C_L = 0.1\ \mu F$ 16 μs max
- Wide Input/Output Range 0.1V to V_{CC} − 0.1V min
- Supply Voltage Range 5V to 16V
- Supply Current 6.5 mA max
- Standby Mode Current 500 μA

Applications

- AMLCD voltage buffering
- Multi-voltage buffering

Connection Diagram

24-Pin SO



Top View

Note: Buffers 1, 3, 5 and 7 are High Speed and Buffers 2, 4, 6 and 8 are Low Speed.

Ordering Information

Package	Temperature Range −40°C to +85°C	NSC Drawing	Transport Media
24-Pin Surface Mount	LMC6008IM	M24B	Rail
	LMC6008IMX	M24B	Tape & Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Voltage at Input Pin	$V^+ + 0.4V, V^- - 0.4V$
Voltage at Output Pin	$V^+ + 0.4V, V^- - 0.4V$
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (soldering, 10 sec.)	260°C
Storage Temperature Range	−55°C to +150°C
Junction Temperature (Note 4)	150°C
Power Dissipation (Note 4)	Internally Limited

Operating Ratings (Note 1)

Supply Voltage	$4.5V \leq V^+ \leq 16V$
Temperature Range	−20°C to +100°C
Thermal Resistance (θ_{JA})	
M Package, 24-Pin Surface Mount	50°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V_{CC} = 14.5V$ and $R_L = 0$.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6008 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$		25	mV max
A_V		$V_O = 10\ V_{PP}$		0.985	V/V
I_B	Input Bias Current			300	nA max
I_{LP}	Peak Load Current	Hi Speed Buffers $V_O = 13\ V_{PP}$		−250	mA max
				+250	mA min
I_{LP}	Peak Load Current	Lo Speed Buffers $V_O = 13\ V_{PP}$		−150	mA max
				+150	mA min
V_{ERR}	Output Voltage Difference (Note 9)		35		mV max
V_{IH}	Standby Logic High Voltage			3.30	V min
V_{IL}	$I_{STANDBY}$ Logic Low Voltage			1.80	V max
I_{IH}	Standby High Input Current			1.0	μA max
I_{IL}	Standby Low Input Current			1.0	μA max
$I_{O\ (STD\text{-}BY)}$	Output Leakage Current	$V_{STD\text{-}BY}$ = High		5	μA max
I_{CC}	Supply Current	V_{IL} = Low, $V_{IN} = 7.25V$		6.5	mA max
$I_{STD\text{-}BY}$	Standby Current	$V_{STD\text{-}BY}$ = High		500	μA max
PSRR	Power Supply Rejection Ratio	$5V < V_{CC} < 14.5V$		55	dB min
V_O	Voltage Output Swing			0.1	V min
				$V_{CC} - 0.1$	V max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V_{CC} = 14.5V$ and $R_L = 0\Omega$.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6008 Limit (Note 6)	Units
SR	Slew Rate	Buffers 1, 3, 5, 7 (Note 3)		1.70	V/μs min
		Buffers 2, 4, 6, 8 (Note 3)		0.85	V/μs min
t_S	Settling Time	(Notes 3, 7)		16	μs max
t_{ON}	Standby Response Time ON			10	μs max
t_{OFF}	Standby Response Time OFF			10	μs max
PBW	Power Bandwidth	$V_O = 10\ V_{PP}$ for Hi-Speed $V_O = 5\ V_{PP}$ for Lo-Speed (Note 3)		45	KHz min
C_L	Load Capacitance			0.1	μF max

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: The Load is a series connection of a 0.1 μF capacitor and a 1Ω resistor.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$, where the junction-to-ambient thermal resistance $\theta_{JA} = 50°C/W$. If the maximum allowable power dissipation is exceeded, the thermal limit circuit will limit the die temperature to approximately 160°C. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: The settling time is measured from the input transition to a point 50 mV of the final value, for both rising and falling transitions. The input swing is 0.5V to 13.5V for buffers 1, 3, 5, 7 and 3.75V to 10.25V for buffers 2, 4, 6, 8. Input rise time should be less than 1 μs.

Note 8: High-Speed Buffers are 1, 3, 5, 7 and Low-Speed Buffers are 2, 4, 6, 8.

Note 9: Output Voltage Difference is the difference between the highest and lowest buffer output voltage when all buffer inputs are at identical voltages.

Section 5
Special Functions

Section 5 Contents

DH0006/DH0006C Current Drivers 5-3
DH0034 High Speed Dual Level Translator 5-7
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LM3146 High Voltage Transistor Array 5-47
LP395 Ultra Reliable Power Transistor 5-52

National Semiconductor

DH0006/DH0006C* Current Drivers

General Description

The DH0006/DH0006C is an integrated high voltage, high current driver designed to accept standard DTL or TTL logic levels and drive a load of up to 400 mA at 28V. AND inputs are provided along with an Expander connection, should additional gating be required. The addition of an external capacitor provides control of the rise and fall times of the output in order to decrease cold lamp surges or to minimize electromagnetic interference if long lines are driven.

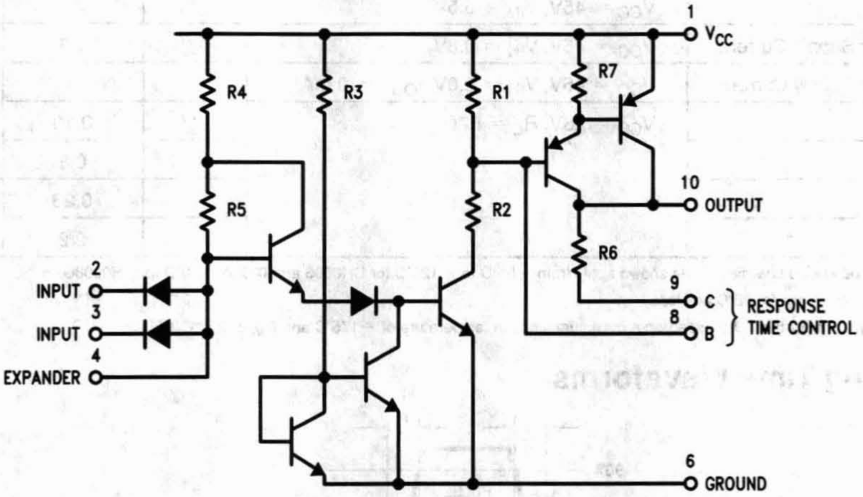
Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

Features

- Operation from a Single +10V to +45 Power Supply
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply
- 1.5A, 50 ms, Pulse Current Capability

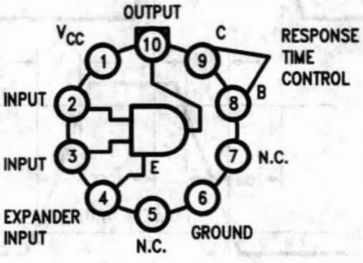
*Previously called NH0006/NH0006C

Schematic and Connection Diagrams


1
VCC
R4
R3
R1
R7
R5
R2
10
OUTPUT
R6
9
C
8
B
RESPONSE
TIME CONTROL
2
INPUT
3
INPUT
4
EXPANDER
6
GROUND

TL/K/10120–1

Metal Can Package


OUTPUT
VCC
C
RESPONSE
TIME
CONTROL
B
1
10
9
8
INPUT
2
INPUT
3
E
7
N.C.
4
5
6
EXPANDER
INPUT
N.C.
GROUND

TL/K/10120–2

Top View

Order Number DH0006H or DH0006CH
See NS Package Number H10F

5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current (50 ms On/1 sec Off)	1.5A
Operating Temperature	
DH0006	−55°C to +125°C
DH0006C	0°C to +70°C
Storage Temperature	−65°C to +150°C

Electrical Characteristics (Note 1)

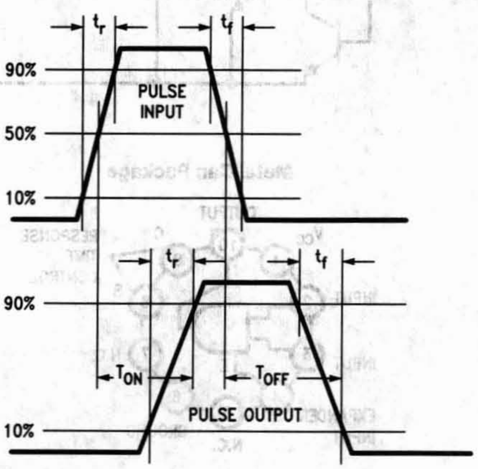
Parameter	Conditions	Min	Typ (Note 2)	Max	Units
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 400 mA	26.5	27.0		
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1k		0.001	0.01	
Logical "1" Output Voltage	V_{CC} = 10V, V_{IN} = 2.0V, I_{OUT} = 150 mA	8.8	9.2		
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V V_{CC} = 45V, V_{IN} = 5.5V		0.5	5.0 100	µA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0.8V		1.6	2.0	mA
"On" Power Supply Current	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 0 mA			8	mA
Rise Time	V_{CC} = 28V, R_L = 82Ω		0.10		µs
Fall Time			0.8		
T_{on}			0.26		
T_{off}			2.2		

Note 1: Unless otherwise specified, limits shown apply from −55°C to +125°C for DH0006 and 0°C to +70°C for DH0006C.

Note 2: Typical values are for 25°C ambient.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and θ_{JA} of 210°C/W.

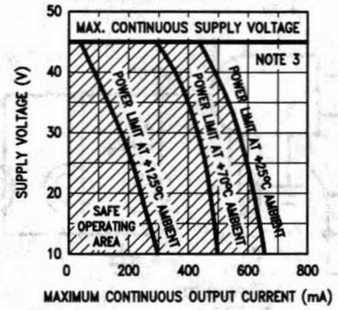
Switching Time Waveforms



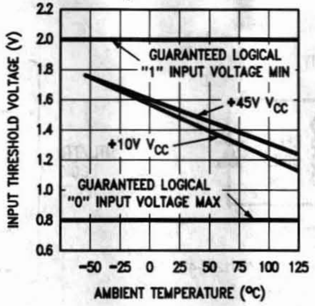
TL/K/10120-6

Typical Performance Characteristics

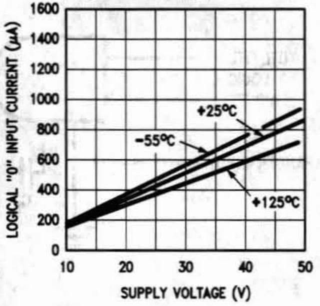
Maximum Continuous Output Current for TO-5



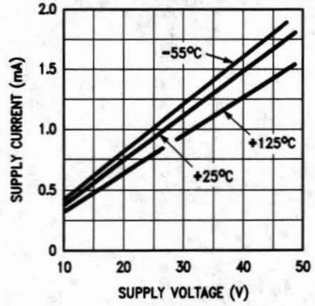
Input Threshold Voltage vs Temperature



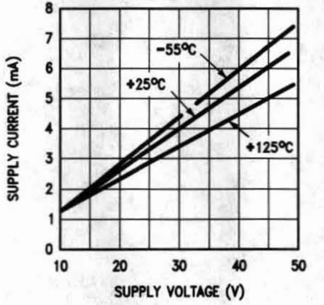
Logical "0" Input Current



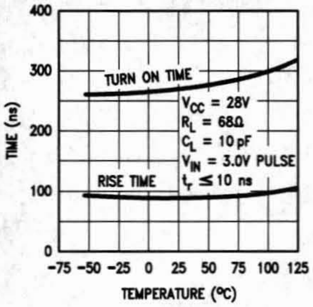
"OFF" Supply Current Drain



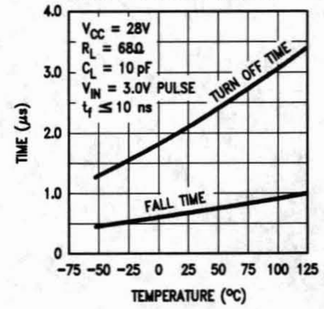
"ON" Supply Current Drain



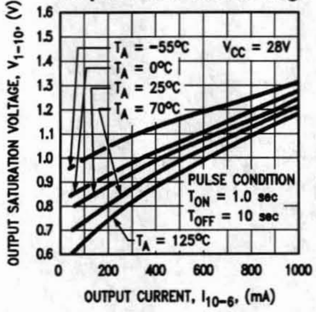
Turn On and Rise Time



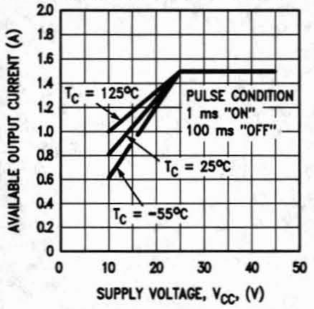
Turn Off and Fall Time



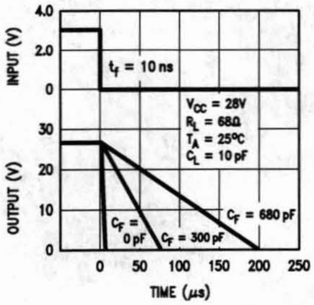
Output Saturation Voltage



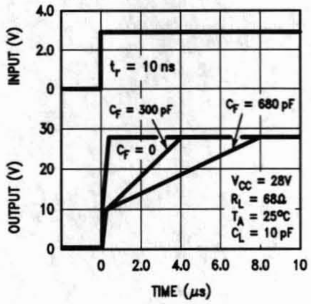
Available Output Current



Turn Off Control



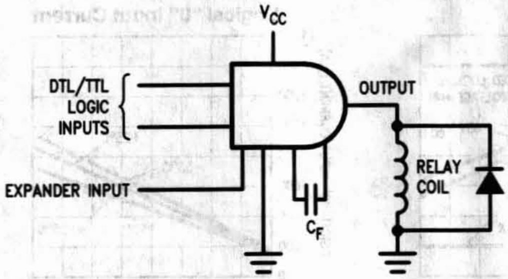
Turn On Control



TL/K/10120–7

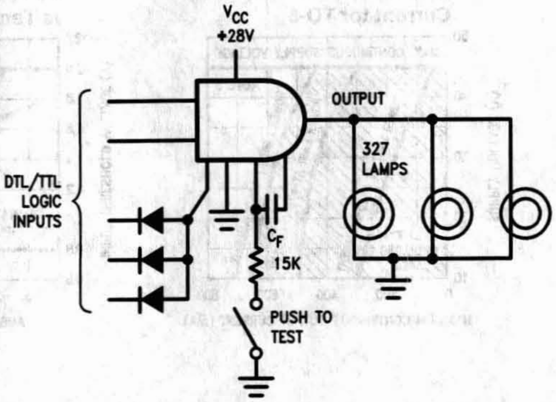
Typical Applications

Relay Driver


V_{CC}
DTL/TTL LOGIC INPUTS
OUTPUT
RELAY COIL
EXPANDER INPUT
C_F

TL/K/10120-4

Lamp Driver with Expanded Inputs


V_{CC}
+28V
OUTPUT
327 LAMPS
DTL/TTL LOGIC INPUTS
C_F
15K
PUSH TO TEST

TL/K/10120-5

National Semiconductor

DH0034
High Speed Dual Level Translator

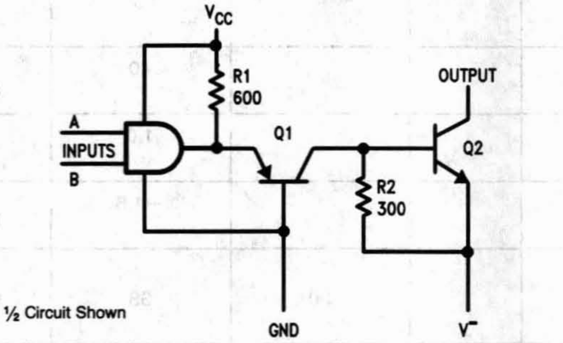
General Description

The DH0034 is a high speed level translator suitable for interfacing to MOS or junction FET analog switches. It may also be used as a universal logic level shifter capable of accepting TTL/DTL input levels and shifting to CML, MOS, or SLT levels.

Features

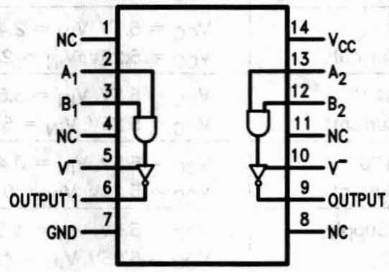
- Fast switching, t_{pd0}: typically 15 ns; t_{pd1}: typically 35 ns
- Large output voltage range: 25V
- Input is TTL/DTL compatible
- Low output leakage: typically 0.1 μA

Schematic and Connection Diagrams


V_{CC}
R1
600
OUTPUT
A
INPUTS
B
Q1
Q2
R2
300
½ Circuit Shown
GND
V^-

TL/K/10122-1

Dual-In-Line Package


NC
1
A_1
2
B_1
3
NC
4
V^-
5
OUTPUT 1
6
GND
7
14
V_{CC}
13
A_2
12
B_2
11
NC
10
V^-
9
OUTPUT 2
8
NC

TL/K/10122-3

Top View

Order Number DH0034D-MIL or DH0034CD

See NS Package Number D14D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Supply Voltage	7.0V
Negative Supply Voltage	−30V
Positive Supply Voltage	+25V
Differential Supply Voltage	25V
Maximum Output Current	100 mA
Power Dissipation	(Note 4)
Input Voltage	+5.5V
Operating Temperature Range	
DH0034D-MIL	−55°C to +125°C
DH0034CD	0°C to +85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (See Notes 1 and 2)

Parameter	Conditions	DH0034			Units
		Min	Typ	Max	
Logical "1" Input Voltage	V_{CC} = 4.5V V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	V_{CC} = 5.5V V_{CC} = 5.25V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 2.4V V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V V_{CC} = 5.25V, V_{IN} = 5.5V			1.0	mA
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V V_{CC} = 5.25V, V_{IN} = 0.4V			−1.6	mA
Power Supply Current Logic "0"	V_{CC} = 5.5V, V_{IN} = 4.5V V_{CC} = 5.25V, V_{IN} = 4.5V (Note 3)		30	38	mA
Power Supply Current Logic "1"	V_{CC} = 5.5V, V_{IN} = 0V V_{CC} = 5.25V, V_{IN} = 0V (Note 3)		37	48	mA
Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OUT} = 100 mA V_{CC} = 4.5V, I_{OUT} = 50 mA		V^- + 0.50 V^- + 0.3	 V^- + 0.50	V
Output Leakage Current	V_{CC} = 5.5V, V_{IN} = 0.8V $V^+ - V^-$ = 25V		0.1	5.0	μA
Transition Time to Logical "0"	V_{CC} = 5.0V, V_3 = 0V, T_A = 25°C V^- = 25V, R_L = 510Ω		15	25	ns
Transition Time to Logical "1"	V_{CC} = 5.0V, T_A = 25°C V^- = −25V, R_L = 510Ω		35	75	ns

Note 1: The specifications apply over the temperature range −55°C to +125°C for the DH0034D-MIL and over the temperature range −25°C to +85°C for DH0034CD with a 510Ω resistor connected between output and ground, and V^- connected to −25V, unless otherwise specified.

Note 2: All typical values are for T_A = 25°C.

Note 3: Current measured is total drawn from V_{CC} supply.

Note 4: Power rating for the Cavity DIP based on a maximum junction temperature of 175°C and θ_{JA} = 180°C/W.

Theory of Operation

When both inputs of the DH0034 are raised to logic "1", the input AND gate is turned "on" allowing Q1's emitter to become forward biased. Q1 provides a level shift and constant output current. The collector current is essentially the same as the emitter which is given by

$$\frac{V_{CC} - V_{BE}}{R1}$$

Approximately 7.0 mA flows out of Q1's collector.

About 2 mA of Q1's collector current is drawn off by pull down resistor, R2. The balance, 5 mA, is available as base drive to Q2 and to charge its associated Miller capacitance. The output is pulled to within a V_{SAT} of V^-. When either (or both) input to the DH0034 is lowered to logic "0", the AND gate output drops to 0.2V turning Q1 off. Deprived of base drive Q2 rapidly turns off causing the output to rise to the V_3 supply voltage. Since Q2's emitter operates between 0.6V and 0.2V, the speed of the DH0034 is greatly enhanced.

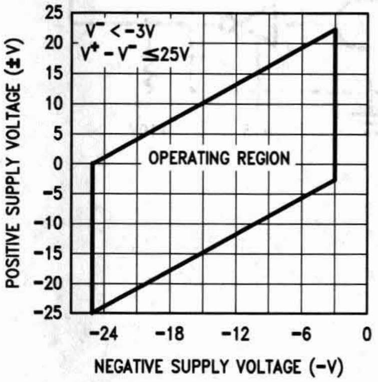
Applications Information

1. Paralleling the Outputs

The outputs of the DH0034 may be paralleled to increase output drive capability or to accomplish the "wire OR". In order to prevent current hogging by one output transistor or the other, resistors of 2Ω/100 mA value should be inserted between the emitters of the output transistors and the minus supply.

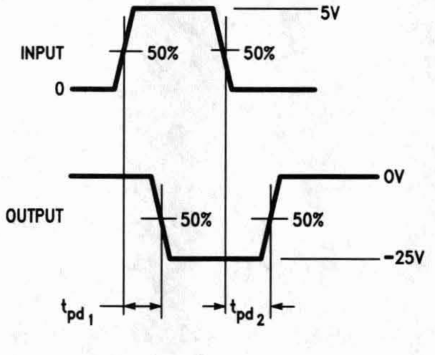
2. Recommended Output Voltage Swing

The graph shows boundary conditions which govern proper operation of the DH0034. **The range of operation for the negative supply is shown on the X axis and must be between −3V and −25V.** The allowable range for the positive supply is governed by the value chosen for V^-. V^+ may be selected by drawing a vertical line through the selected value for V^- and terminated by the boundaries of the operating region. For example, a value of V^- equal to −6V would dictate values of V^+ between −5V and +19V. In general, it is desirable to maintain at least 5V difference between the supplies.



TL/K/10122-6

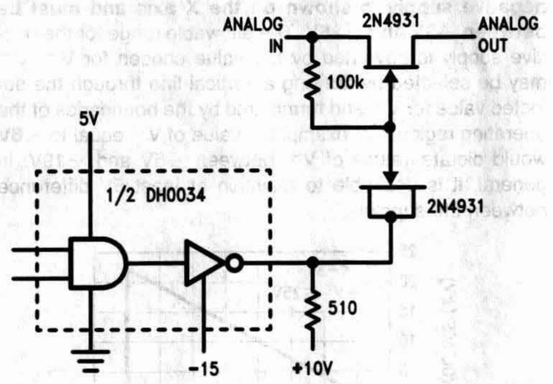
Switching Time Waveforms



TL/K/10122-7

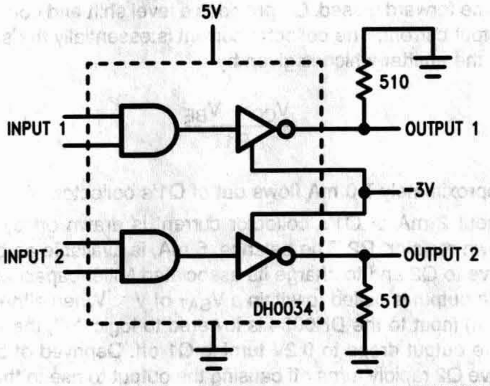
Typical Applications

5 MHz Analog Switch


ANALOG IN
2N4931
ANALOG OUT
100k
5V
1/2 DH0034
2N4931
510
-15
+10V

TL/K/10122-4

TTL to IBM (SLT) Logic Levels


5V
510
INPUT 1
OUTPUT 1
-3V
INPUT 2
OUTPUT 2
510
DH0034

TL/K/10122-5

National Semiconductor

DH0035/DH0035C
PIN Diode Driver

General Description

The DH0035/DH0035C is a high speed digital driver designed to drive PIN diodes in RF modulators and switches. The device is used in conjunction with an input buffer such as the DM7830/DM8830 or DM5440/DM7440.

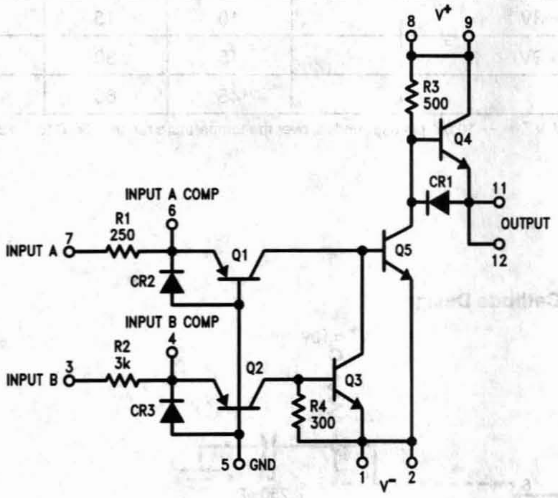
Features

- Large output voltage swing—30V
- Peak output current in excess of 1A
- Inputs TTL/DTL compatible
- Short propagation delay—10 ns
- High repetition rate—5 MHz

The DH0035/DH0035C is capable of driving a variety of PIN diode types including parallel, serial, anode grounded and cathode grounded. For additional information, see *AN-49 PIN Diode Drivers.*

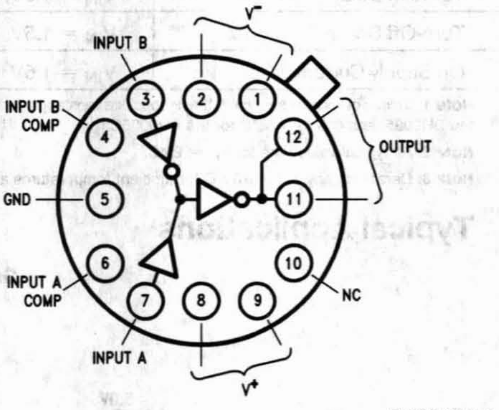
The DH0035 is guaranteed over the temperature range −55°C to +125°C whereas the DH0035C is guaranteed from 0°C to +85°C.

Schematic and Connection Diagrams


8
V+
9
R3
500
Q4
CR1
11
OUTPUT
12
INPUT A COMP
6
R1
250
7
INPUT A
CR2
Q1
Q5
INPUT B COMP
4
R2
3k
3
INPUT B
CR3
Q2
Q3
R4
300
5 GND
1
V−
2

TL/K/10124–1

Metal Can Package


V−
INPUT B
3
2
1
INPUT B COMP
4
12
OUTPUT
GND
5
11
6
10
INPUT A COMP
7
8
9
NC
INPUT A
V+

TL/K/10124–2

Top View

Order Number DH0035G-MIL or DH0035CG
See NS Package Number G12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V^- Supply Voltage Differential (Pin 5 to Pin 1 or 2)	40V
V^+ Supply Voltage Differential (Pin 1 or 2 to Pin 8 or 9)	30V
Input Current (Pin 3 or 7)	±75 mA
Peak Output Current	±1.0A
Power Dissipation (Note 3)	1.5W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DH0035	−55°C to +125°C
DH0035C	0°C to +85°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	Limits			Units
		Min	Typ	Max	
Input Logic "1" Threshold	$V_{OUT} = -8V$, $R_L = 100\Omega$		1.0	2.0	V
Input Logic "0" Threshold	$V_{OUT} = +8V$, $R_L = 100\Omega$	0.4	0.6		V
Positive Output Swing	$I_{OUT} = 100$ mA	7.0	+8.0		V
Negative Output Swing	$I_{OUT} = 100$ mA		−8.0	−7.0	V
Positive Short Circuit Current	$V_{IN} = 0V$, $R_L = 0\Omega$ (Pulse Test, Duty Cycle ≤ 3%)	400	800		mA
Negative Short Circuit Current	$V_{IN} = 1.5V$, $I_{IN} = 50$ mA, $R_L = 0\Omega$ (Pulse Test, Duty Cycle ≤ 3%)	800	1000		mA
Turn-On Delay	$V_{IN} = 1.5V$, $V_{OUT} = -3V$		10	15	ns
Turn-Off Delay	$V_{IN} = 1.5V$, $V_{OUT} = +3V$		15	30	ns
On Supply Current	$V_{IN} = 1.5V$		45	60	mA

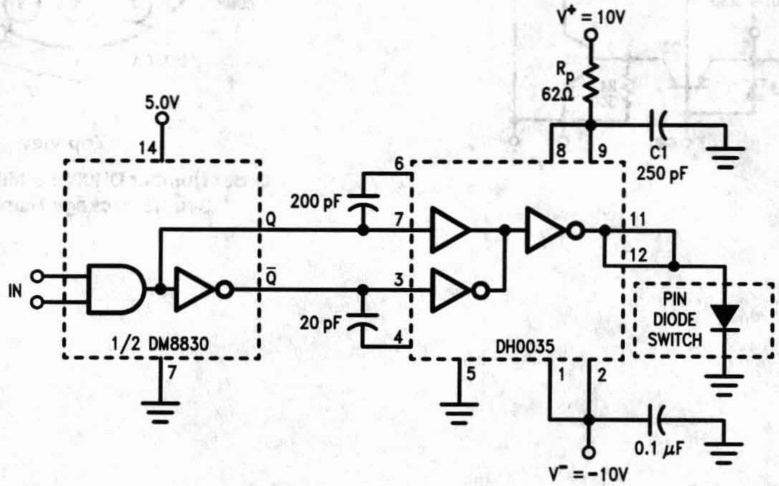
Note 1: Unless otherwise specified, these specifications apply for $V^+ = 10.0V$, $V^- = -10.0V$, pin 5 grounded, over the temperature range −55°C to +125°C for the DH0035, and 0°C to +85°C for the DH0035C.

Note 2: All typical values are for $T_A = 25°C$.

Note 3: Derate linearly at 10 mW/°C for ambient temperatures above 25°C.

Typical Applications

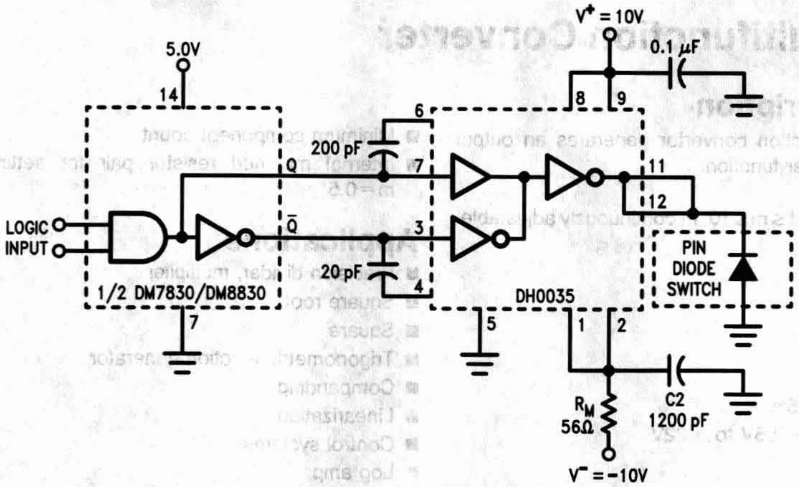
Grounded Cathode Design



Note: Cathode grounded PIN diode: $R_p = 62\Omega$ limits diode forward current to 100 mA. Typical switching for HP33604A, RF turn-on 25 ns, turn-off 5 ns. C2 = 250 pF, $R_p = 0\Omega$, C1 = 0.1F.

Typical Applications (Continued)

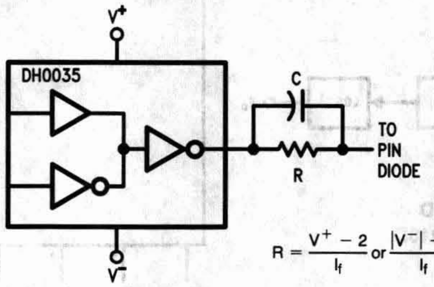
Grounded Anode Design


V+ = 10V
0.1 µF
5.0V
14
8
9
6
200 pF
Q
7
11
12
LOGIC
INPUT
Q̄
3
20 pF
4
PIN
DIODE
SWITCH
1/2 DM7830/DM8830
DH0035
7
5
1
2
RM
56Ω
C2
1200 pF
V− = −10V

TL/K/10124–4

Note: Anode Grounded PIN diode: $R_M = 56\Omega$ limits diode forward current to 100 mA. Typical switching for HP33622A, RF turn-on 5 ns; turn-off 4 ns. $C1 = 470$ pF, $C2 = 0.1\ \mu F$, $R_M = 0\Omega$.

Alternate Current Limiting


V+
DH0035
C
TO
PIN
DIODE
R
V−

$$R = \frac{V^+ - 2}{I_f} \text{ or } \frac{|V^-| - 2}{I_f}$$

TL/K/10124–5

National Semiconductor

LH0094 Multifunction Converter

General Description

The LH0094 multifunction converter generates an output voltage per the transfer function:

$$E_O = V_y \left(\frac{V_Z}{V_X}\right)^m, \; 0.1 \le m \le 10, \text{ m continuously adjustable}$$

m is set by 2 resistors.

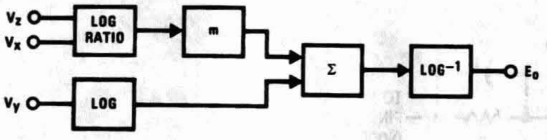
Features

- Low cost
- Versatile
- High accuracy—0.05%
- Wide supply range—±5V to ±22V
- Minimum component count
- Internal matched resistor pair for setting m=2 and m=0.5

Applications

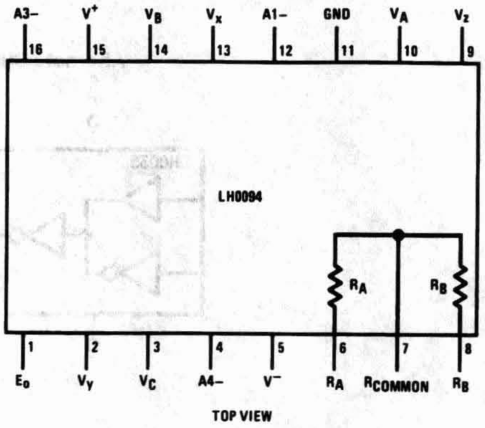
- Precision divider, multiplier
- Square root
- Square
- Trigonometric function generator
- Companding
- Linearization
- Control systems
- Log amp

Block and Connection Diagrams

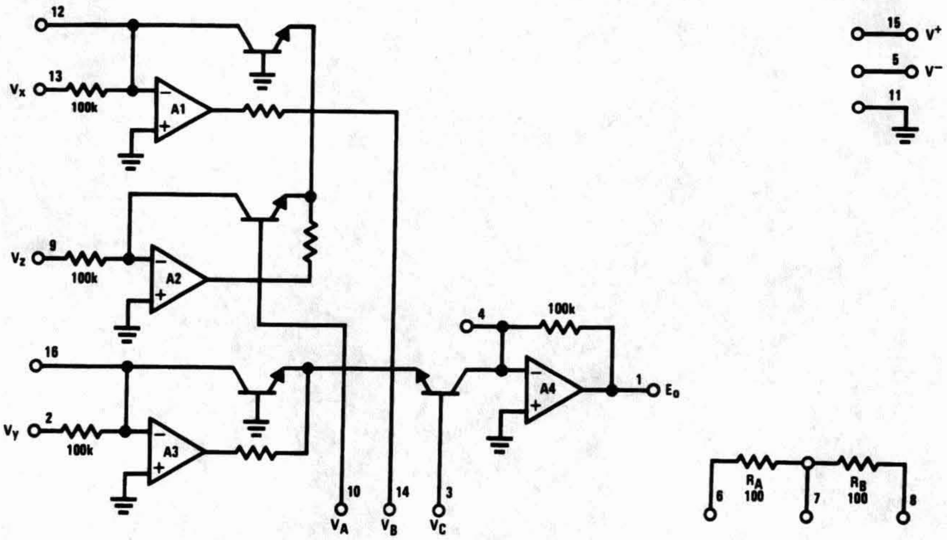

V_z
V_x
LOG RATIO
m
Σ
LOG^-1
E_o
V_y
LOG

Order Number LH0094CD
See NS Package Number D16D

Dual-In-Line Package


A3−
V+
V_B
V_x
A1−
GND
V_A
V_z
16
15
14
13
12
11
10
9
LH0094
R_A
R_B
1
2
3
4
5
6
7
8
E_o
V_y
V_C
A4−
V−
R_A
R_COMMON
R_B
TOP VIEW

Simplified Schematic


12
V_x
13
100k
A1
V_z
9
100k
A2
16
V_y
2
100k
A3
4
100k
A4
1
E_o
10
V_A
14
V_B
3
V_C
15
V+
5
V−
11
R_A
100
R_B
100
6
7
8

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Input Voltage	±22V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LH0094CD	−25°C to +85°C
Storage Temperature Range	
LH0094CD	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics

$V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified. Transfer function: $E_O = V_Y \frac{V_Z{}^m}{V_X}$; $0.1 \le m \le 10$; $0V \le V_X, V_Y, V_Z \le 10V$

Parameter	Conditions	LH0094C Min	LH0094C Typ	LH0094C Max	Units
ACCURACY					
Multiply	$E_O = V_Z V_Y$ ($0.03 \le V_Y \le 10V$; $0.01 \le V_Z \le 10V$)				% F.S.
Untrimmed	*(Figure 2)*		0.45	0.9	(10V)
External Trim	*(Figure 3)*		0.1		% F.S.
	vs. Temperature		0.2		mV/°C
Divide	$E_O = 10V_Z/V_X$				
Untrimmed	*(Figure 4)*, $0.5 \le V_X \le 10$; $0.01 \le V_Z \le 10$)		0.45	0.9	% F.S.
External Trim	*(Figure 5)*, ($0.1 \le V_X \le 10$; $0.01 \le V_Z \le 10$)		0.1		% F.S.
	vs. Temperature		0.2		mV/°C
Square Root	$E_O = 10\sqrt{V_Z/10}$				
Untrimmed	*(Figure 8)*, ($0.03 \le V_Z \le 10$		0.45	0.9	% F.S.
External Trim	*(Figure 9)*, ($0.01 \le V_Z \le 10$		0.15		% F.S.
Square	$E_O = 10\ (V_Z/10)^2$ ($0.1 \le V_Z \le 10$)				
Untrimmed	*(Figure 6)*	1.0	2.0	% F.S.	
External Trim	*(Figure 7)*	0.15		% F.S.	
Low Level Square Root	$E_O = \sqrt{10V_Z}$; $5.0mV \le V_Z \le 10V$, *(Figure 10)*		0.05		% F.S.
Exponential Circuits	$m = 0.2$, $E_O = 10\ (V_Z/10)^2$ *(Figure 11)*, ($0.1 \le V_Z \le 10$)		0.08		% F.S.
	$m = 5.0$, $E_O = 10\ (V_Z/10)^5$ *(Figure 11)*, ($1.0 \le V_Z \le 10$)		0.08		% F.S.
OUTPUT OFFSET					
	$V_X = 10V$, $V_Y = V_Z = 0$		5.0	10	mV
AC CHARACTERISTICS					
3 dB Bandwidth	$m = 1.0$, $V_X = 10V$, $V_Y = 0.1\ V_{rms}$		10		kHz
Noise	10 Hz to 1.0 kHz, $m = 1.0$, $V_Y = V_Z = 0V$				
	$V_X = 10V$		100		µV/rms
	$V_X = 0.1V$		300		µV/rms
EXPONENT					
m		0.2 to 5.0	0.1 to 10		
INPUT CHARACTERISTICS					
Input Voltage	(For Rated Performance)	0		10	V
Input Impedance	(All Inputs)	98	100		kΩ
OUTPUT CHARACTERISTICS					
Output Swing	($R_L \le 10k$)	10	12		V
Output Impedance			1.0		Ω
Supply Current	($V_S = \pm 15V$) (Note 1)		3.0	5.0	mA

Note 1: Refer to RETS0094D drawing for specifications of the military LH00940 version.

Applications Information

GENERAL INFORMATION

Power supply bypass capacitors (0.1 μF) are recommended for all applications.

The LH0094 series is designed for positive input signals only. However, negative input up to the supply voltage will not damage the device.

A clamp diode (*Figure 1*) is recommended for those applications in which the inputs may be subjected to open circuit or negative input signals.

For basic applications (multiply, divide, square, square root) it is possible to use the device without any external adjustments or components. Two matched resistors are provided internally to set m for square or square root.

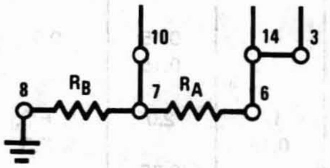
When using external resistors to set m, such resistors should be as close to the device as possible.

SELECTION OF RESISTORS TO SET m

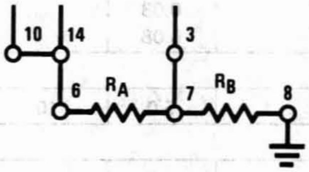
Internal Matched Resistors

R_A and R_B are matched internal resistors. They are 100Ω ± 10%, but matched to 0.1%.

(a) m = 2*



(b) m = 0.5*



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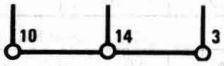
*No external resistors required, strap as indicated

External Resistors

The exponent is set by 2 external resistors or it may be continuously varied by a single trim pot. (R1 + R2 ≤ 500Ω.

(a) m = 1



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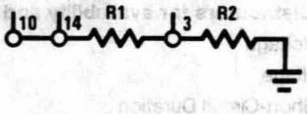
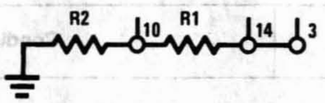
(b) m < 1



$$m = \frac{R2}{R1 + R2} \quad R1 + R2 \approx 200\Omega$$

(c) m > 1



$$m = \frac{R1 + R2}{R2}$$

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ACCURACY (ERROR)

The accuracy of the LH0094 is specified for both externally adjusted and unadjusted cases.

Although it is customary to specify the errors in percent of full-scale (10V), it is seen from the typical performance curves that the actual errors are in percent of reading. Thus, the specified errors are overly conservative for small input voltages. An example of this is the LH0094 used in the multiplication mode. The specified typical error is 0.25% of full-scale (25 mV). As seen from the curve, the unadjusted error is ≈25 mV at 10V input, but the error is less than 10 mV for inputs up to 1V. Note also that if either the multiplicand or the multiplier is at less than 10V, (5V for example) the unadjusted error is less. Thus, the errors specified are at full-scale—the worst case.

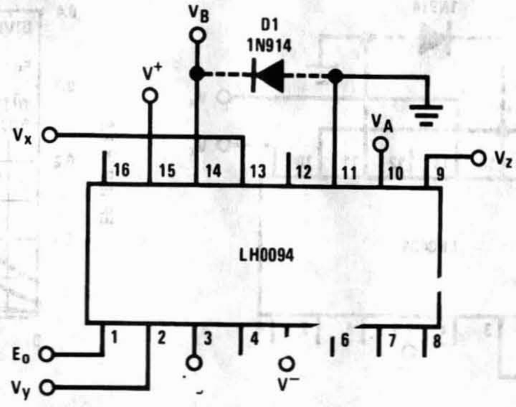
The LH0094 is designed such that the user is able to externally adjust the gain and offset of the device—thus trim out all of the errors of conversion. In most applications, the gain adjustment is the only external trim needed for super accuracy—except in division mode, where a denominator offset adjust is needed for small denominator voltages.

EXPONENTS

The LH0094 is capable of performing roots to 0.1 and powers up to 10. However, care should be taken when applying these exponent—otherwise, results may be misinterpreted. For example, consider the $\frac{1}{10}$th power of a number: i.e., 0.001 raised to 0.1 power is 0.5011; 0.1 raised to the 0.1 power is 0.7943; and 10 raised to the 0.1 power is 1.2589. Thus, it is seen that while the input has changed 4 decades, the output has only changed a little more than a factor of 2. It is also seen that with as little as 1 mV of offset, the output will also be greater than zero with zero input.

Applications Information (Continued)

1. CLAMP DIODE CONNECTION


VB
D1
1N914
V+
VX
VA
VZ
16
15
14
13
12
11
10
9
LH0094
1
2
3
4
6
7
8
E0
VY
V−

$E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$

$0.1 \le m \le 10$

Note. This clamp diode connection is recommended for those applications in which the inputs may be subject to open circuit or negative signals.

FIGURE 1. Clamp Diode Connection

2. MULTIPLY

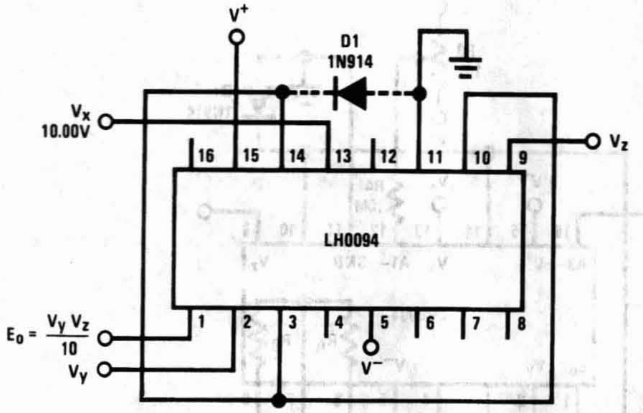

V+
D1
1N914
VX
10.00V
VZ
16
15
14
13
12
11
10
9
LH0094
1
2
3
4
5
6
7
8
V−
E0 = VY VZ / 10
VY

FIGURE 2a. LH0094 Used to Multiply (No External Adjustment)

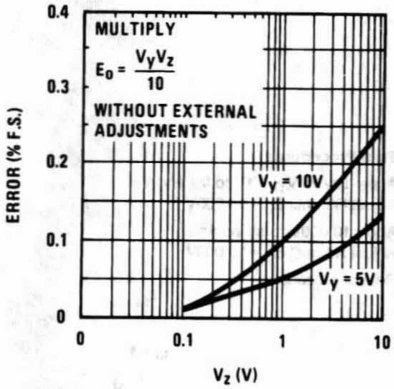
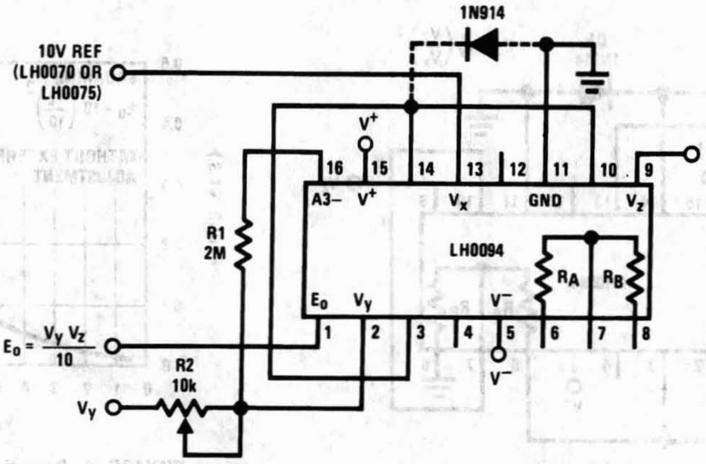


FIGURE 2b. Typical Performance of LH0094 in Multiply Mode Without External Adjustment


D1
1N914
10V REF
(LH0070 OR LH0075)
V+
VZ
16
15
14
13
12
11
10
9
A3−
V+
VX
GND
VZ
R1
2M
LH0094
RA
RB
E0
VY
V−
1
2
3
4
5
6
7
8
V−
E0 = VY VZ / 10
R2
10k
VY

$E_O = \frac{V_Y V_Z}{10}$ $\quad m = 1$

Trim Procedure

Set $V_Z = V_Y = 10V$

Adjust R2 until output = 10.000V

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FIGURE 3. Precision Multiplier (0.02% Typ) with 1 External Adjustment

Applications Information (Continued)

3. DIVIDE

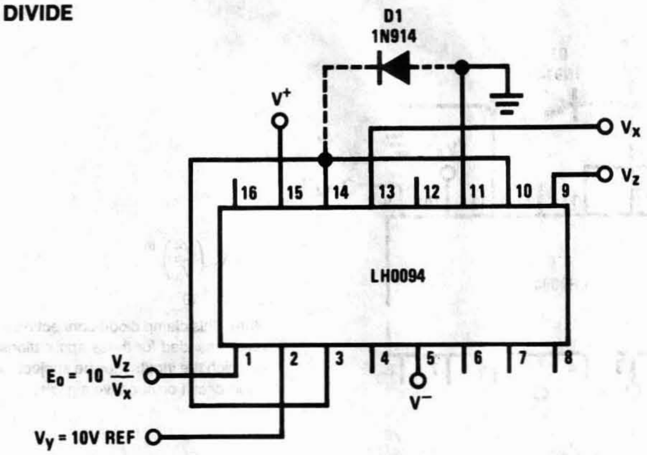

D1
1N914
V+
V_X
V_Z
16
15
14
13
12
11
10
9
LH0094
1
2
3
4
5
6
7
8
$E_O = 10\frac{V_Z}{V_X}$
V−
V_Y = 10V REF

FIGURE 4a. LH0094 Used to Divide (No External Adjustment)

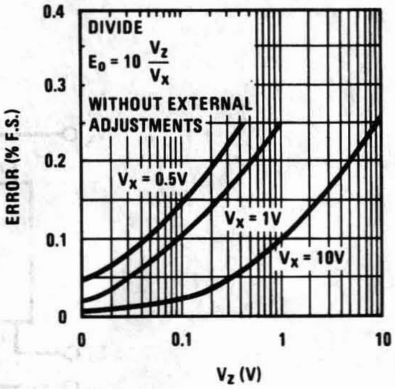


FIGURE 4b. Typical Performance, Divide Mode, Without External Adjustments

Trim Procedures

Apply 10V to V_Y, 0.1V to V_X and V_Z.
Adjust R3 until E_O = 10.000V.

Apply 10.000V to all inputs.
Adjust R2 until E_O = 10.000V

Repeat procedure.

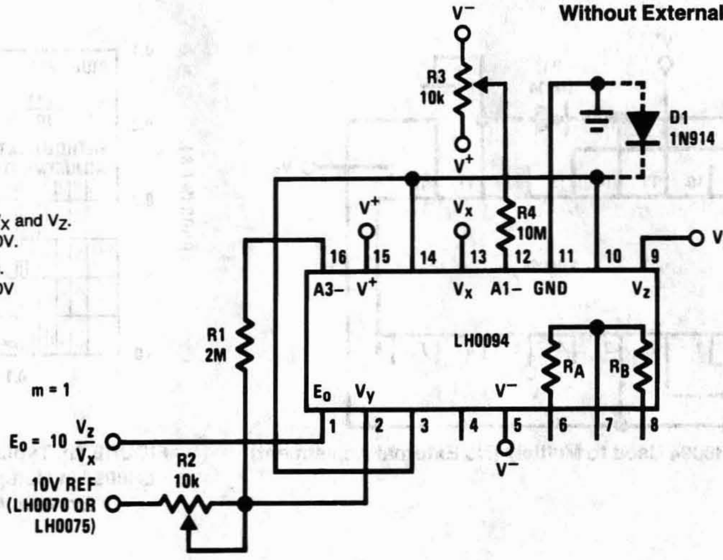
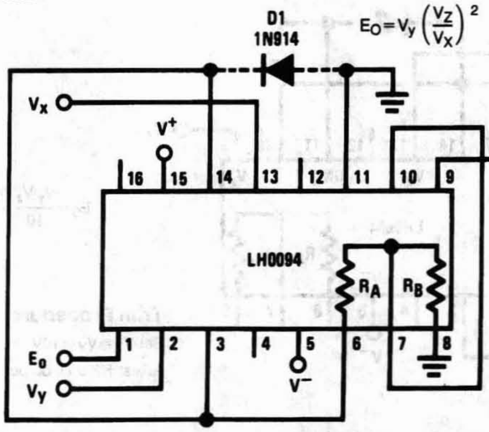

V−
R3
10k
V+
D1
1N914
V+
V_X
R4
10M
V_Z
16
15
14
13
12
11
10
9
A3−
V+
V_X
A1−
GND
V_Z
LH0094
R1
2M
R_A
R_B
m = 1
E_O
V_Y
V−
1
2
3
4
5
6
7
8
$E_O = 10\frac{V_Z}{V_X}$
V−
R2
10k
10V REF
(LH0070 OR
LH0075)

FIGURE 5. Precision Divider (0.05% Typ)

4. SQUARE


D1
1N914
$E_O = V_Y\left(\frac{V_Z}{V_X}\right)^2$
V_X
V+
V_Z
16
15
14
13
12
11
10
9
LH0094
R_A
R_B
1
2
3
4
5
6
7
8
E_O
V_Y
V−

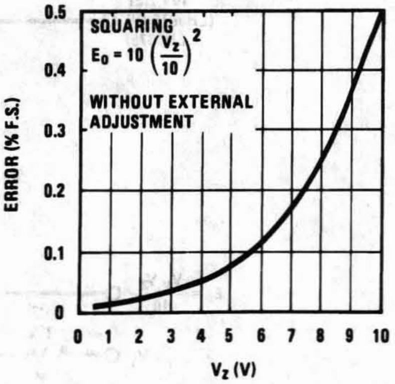


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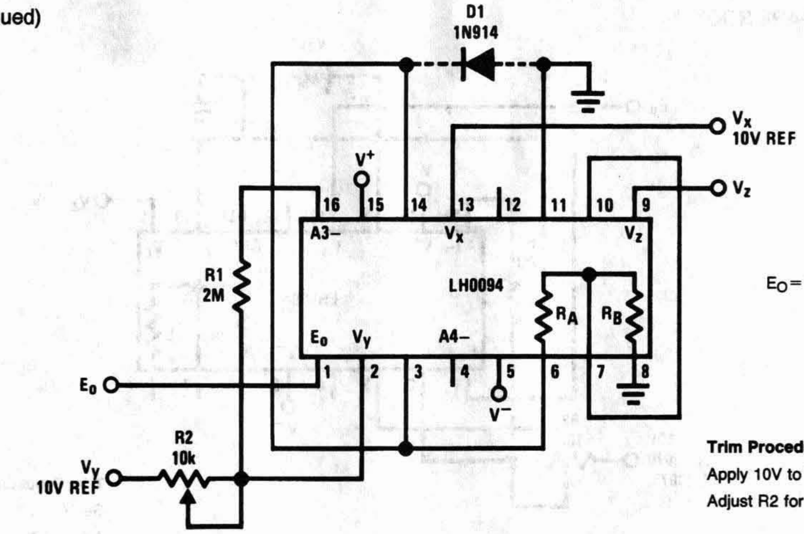
FIGURE 6a. Basic Connection of LH0094 (m = 2) without External Adjustment Using Internal Resistors to Set m

FIGURE 6b. Squaring Mode without External Adjustment

Applications Information (Continued)

4. SQUARE (Continued)


D1
1N914
V_x
10V REF
V^+
V_z
16
15
14
13
12
11
10
9
A3−
V_x
V_z
R1
2M
LH0094
R_A
R_B
E_o
V_y
A4−
1
2
3
4
5
6
7
8
V^-
E_o
R2
10k
V_y
10V REF

$$E_O = 10\left(\frac{V_Z}{10}\right)^2$$

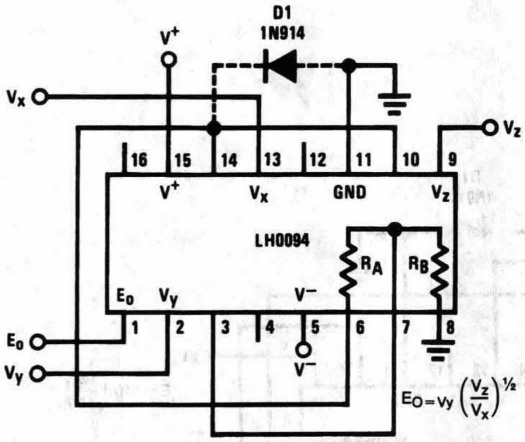
Trim Procedure

Apply 10V to V_Z

Adjust R2 for 10.000V at output

FIGURE 7. Precision Squaring Circuit (0. 15% Typ)

5. SQUARE ROOT


D1
1N914
V^+
V_x
V_z
16
15
14
13
12
11
10
9
V^+
V_x
GND
V_z
LH0094
R_A
R_B
E_o
V_y
V^-
1
2
3
4
5
6
7
8
V^-
E_o
V_y

$$E_O = V_Y\left(\frac{V_Z}{V_X}\right)^{1/2}$$

FIGURE 8a. Basic Connection of LH0094 (m = 0.5) without External Adjustment Using Internal Resistors to Set m

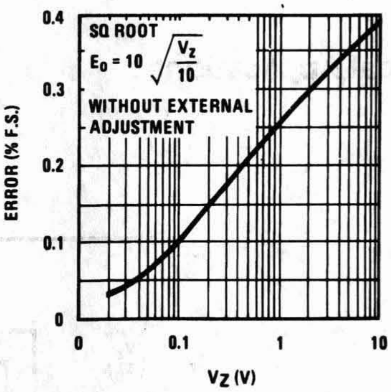
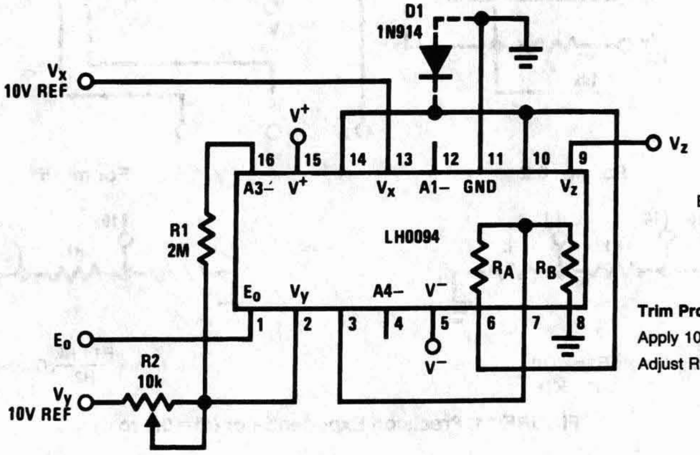


FIGURE 8b. Typical Performance Curve Square Root, No External Adjustment


D1
1N914
V_x
10V REF
V^+
V_z
16
15
14
13
12
11
10
9
A3−
V^+
V_x
A1−
GND
V_z
R1
2M
LH0094
R_A
R_B
E_o
V_y
A4−
V^-
1
2
3
4
5
6
7
8
V^-
E_o
R2
10k
V_y
10V REF

$$E_O = 10\sqrt{\frac{V_Z}{10}}$$

Trim Procedure

Apply 10V to all inputs.

Adjust R2 until $E_O = 10.000V$

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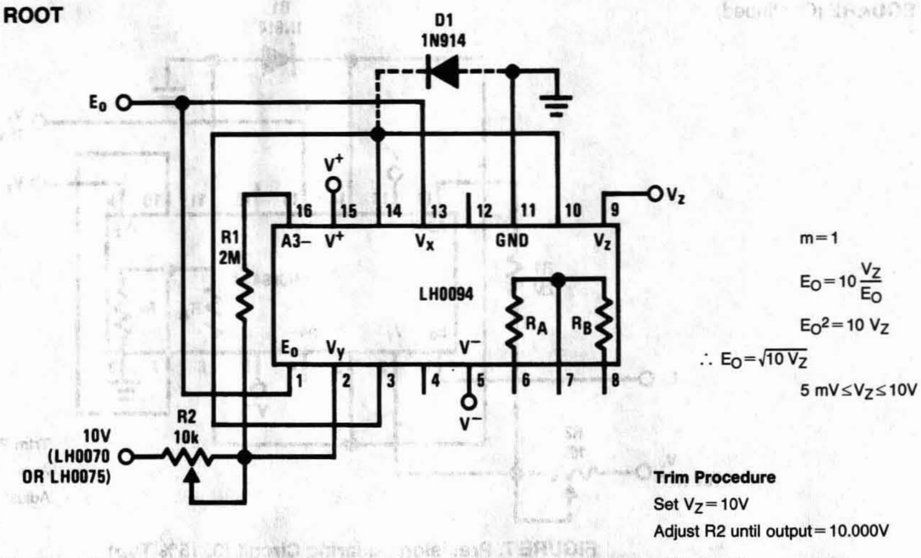
FIGURE 9. Precision Square Rooter (0.15% Typ)

Applications Information (Continued)

6. LOW LEVEL SQUARE ROOT


D1
1N914
E_0
V^+
16
15
14
13
12
11
10
9
V_Z
A3−
V^+
V_x
GND
V_Z
R1
2M
LH0094
R_A
R_B
E_0
V_y
V^-
1
2
3
4
5
6
7
8
V^-
10V
(LH0070
OR LH0075)
R2
10k

m = 1

$E_O = 10 \frac{V_Z}{E_O}$

$E_O^2 = 10\ V_Z$

$\therefore\ E_O = \sqrt{10\ V_Z}$

$5\ mV \leq V_Z \leq 10V$

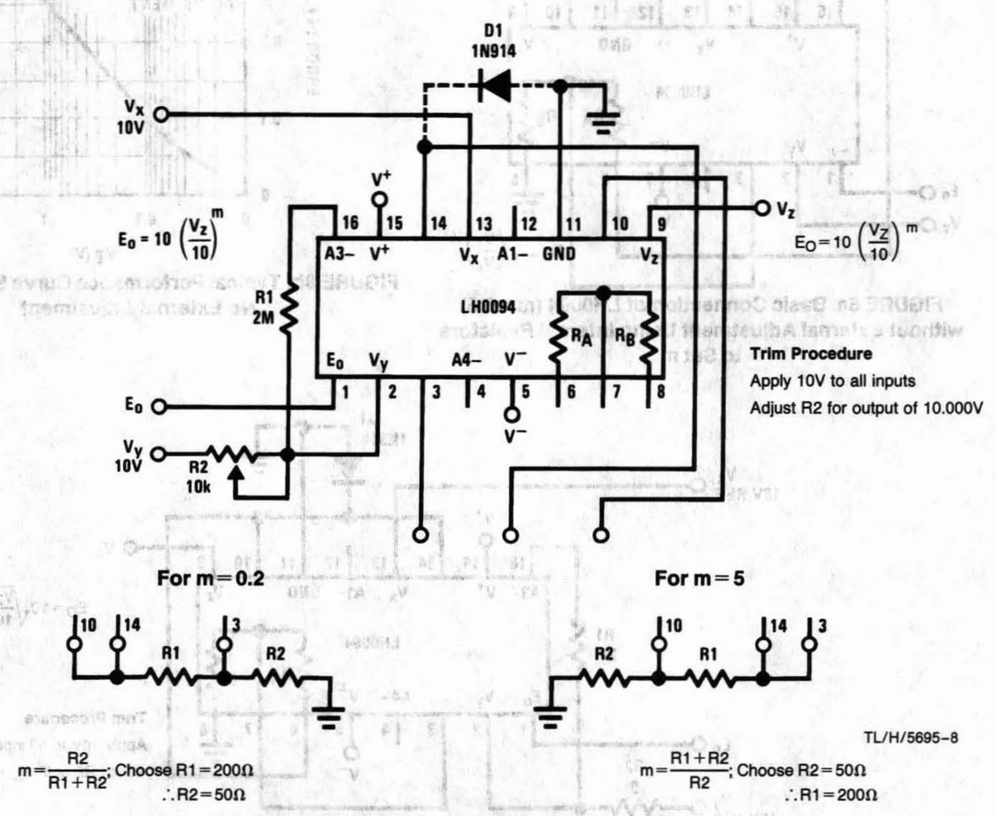
Trim Procedure

Set $V_Z = 10V$

Adjust R2 until output = 10.000V

FIGURE 10. 3-Decade Precision Square Root Circuit Using the LH0094 with m = 1

Typical Applications


D1
1N914
V_x
10V
V^+
$E_0 = 10 \left(\frac{V_Z}{10}\right)^m$
16
15
14
13
12
11
10
9
V_Z
A3−
V^+
V_x
A1−
GND
V_Z
R1
2M
LH0094
R_A
R_B
E_0
V_y
A4−
V^-
1
2
3
4
5
6
7
8
V^-
E_0
V_y
10V
R2
10k
For m = 0.2
10
14
3
R1
R2
For m = 5
10
14
3
R2
R1
TL/H/5695-8

$E_O = 10 \left(\frac{V_Z}{10}\right)^m$

Trim Procedure

Apply 10V to all inputs

Adjust R2 for output of 10.000V

$m = \frac{R2}{R1 + R2}$; Choose R1 = 200Ω

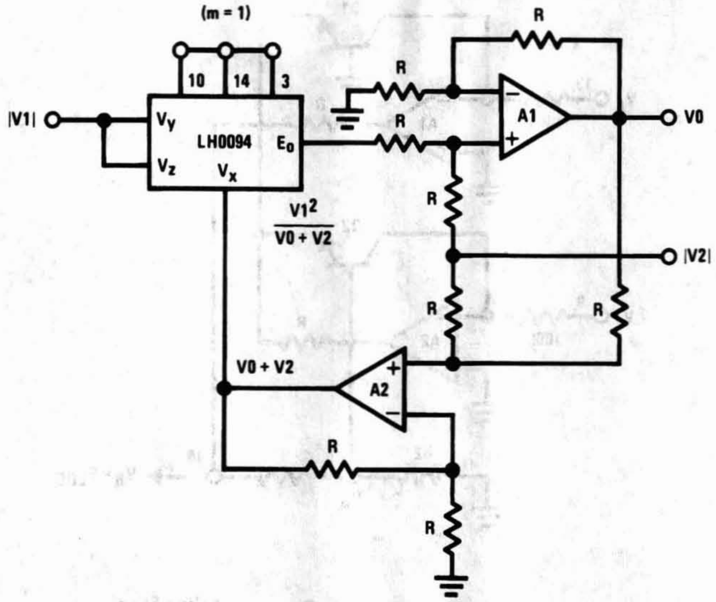
$\therefore R2 = 50Ω$

$m = \frac{R1 + R2}{R2}$; Choose R2 = 50Ω

$\therefore R1 = 200Ω$

FIGURE 11. Precision Exponentiator (m = 0.2 to 5)

Typical Applications (Continued)


(m = 1)
10
14
3
|V1|
V_y
LH0094
E_o
V_z
V_x
$\frac{V1^2}{V0 + V2}$
R
R
R
A1
V0
R
|V2|
R
R
V0 + V2
A2
R
R

Note. The LH0094 may be used to generate a voltage equivalent to:

$$V0 = \sqrt{V1^2 + V2^2}$$

$$V0 = V2 + \frac{V1^2}{V0 + V2}$$

$$V0^2 + V0\ V2 = V2\ V0 + V2^2 + V1^2$$

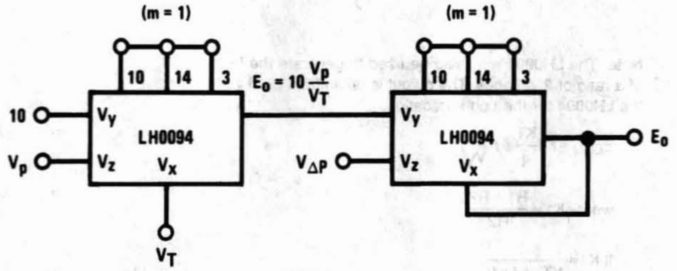
$$V0^2 = V1^2 + V2^2$$

$$\therefore\ V0 = \sqrt{V1^2 + V2^2} \qquad V1, V2\ \ 0 \rightarrow 10V$$

$R \approx 10k$

National Semiconductor resistor array RA08—10k is recommended

FIGURE 12. Vector Magnitude Function


(m = 1)
(m = 1)
10
14
3
10
14
3
$E_o = 10\frac{V_p}{V_T}$
10
V_y
LH0094
V_p
V_z
V_x
V_T
V_y
LH0094
$V_{\Delta P}$
V_z
V_x
E_o

TL/H/5695-9

Note. The LH0094 may be used in direct measurement of gas flow.

$$\text{Flow} = k\sqrt{\frac{P\Delta P}{T}}$$

$$E_O = 10\frac{V_P}{V_T} \times \frac{V_{\Delta P}}{E_O}$$

$$E_O^2 = 10\frac{V_P\,V_{\Delta P}}{VT}$$

$$E_O = \sqrt{10\frac{VP\,V_{\Delta P}}{VT}}$$

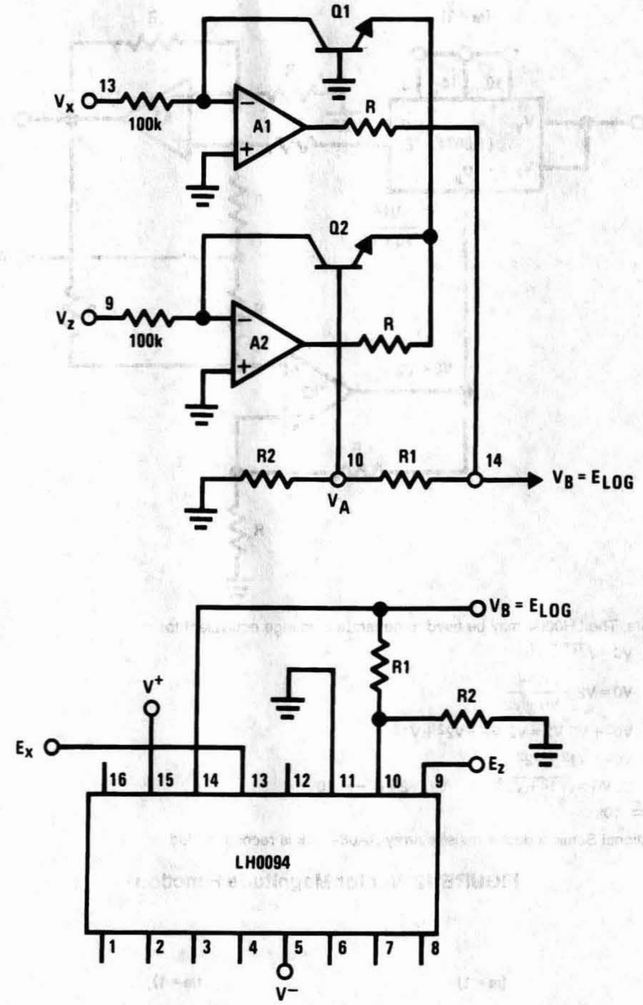
P = Absolute pressure

T = Absolute temperature

ΔP = Pressure drop

FIGURE 13. Mass Gas Flow Circuit

Typical Applications (Continued)


Q1
V_X
13
100k
A1
R
Q2
V_Z
9
100k
A2
R
R2
10
R1
14
$V_B = E_{LOG}$
V_A
$V_B = E_{LOG}$
R1
R2
V^+
E_X
E_Z
16
15
14
13
12
11
10
9
LH0094
1
2
3
4
5
6
7
8
V^-

TL/H/5695-10

Note. The LH0094 may also be used to generate the Log of a ratio of 2 voltages. The output is taken from pin 14 of the LH0094 for the Log application.

$$E_{LOG} = K1 \frac{KT}{q} \ell n \frac{V_Z}{V_X}$$

$$\text{where } K1 = \frac{R1 + R2}{R2}$$

$$\text{If } K1 = \frac{1}{KT/q \ell n10}$$

$$\text{then } E_{LOG} = \text{Log}_{10} \frac{V_Z}{V_X}$$

$R1 = 15.9\ R2$

$R2 \approx 400\Omega$

R2 must be a thermistor with a tempco of ≈ 0.33%/°C to be compensated over temperature.

FIGURE 14. Log Amp Application

National Semiconductor

LM194/LM394 Supermatch Pair

General Description

The LM194 and LM394 are junction isolated ultra well-matched monolithic NPN transistor pairs with an order of magnitude improvement in matching over conventional transistor pairs. This was accomplished by advanced linear processing and a unique new device structure.

Electrical characteristics of these devices such as drift versus initial offset voltage, noise, and the exponential relationship of base-emitter voltage to collector current closely approach those of a theoretical transistor. Extrinsic emitter and base resistances are much lower than presently available pairs, either monolithic or discrete, giving extremely low noise and theoretical operation over a wide current range. Most parameters are guaranteed over a current range of 1 μA to 1 mA and 0V up to 40V collector-base voltage, ensuring superior performance in nearly all applications.

To guarantee long term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation due to reverse biased emitter current—the most common cause of field failures in matched devices. The parasitic isolation junction formed by the diodes also clamps the substrate region to the most negative emitter to ensure complete isolation between devices.

The LM194 and LM394 will provide a considerable improvement in performance in most applications requiring a closely matched transistor pair. In many cases, trimming can be eliminated entirely, improving reliability and decreasing costs. Additionally, the low noise and high gain make this device attractive even where matching is not critical.

The LM194 and LM394/LM394B/LM394C are available in an isolated header 6-lead TO-5 metal can package. The LM394/LM394B/LM394C are available in an 8-pin plastic dual-in-line package. The LM194 is identical to the LM394 except for tighter electrical specifications and wider temperature range.

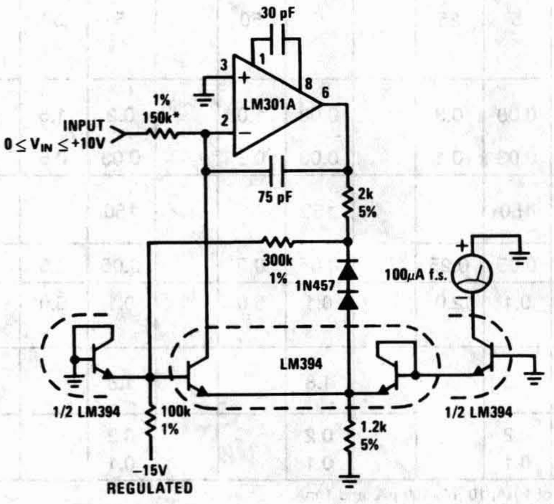
Features

- Emitter-base voltage matched to 50 μV
- Offset voltage drift less than 0.1 μV/°C
- Current gain (h_{FE}) matched to 2%
- Common-mode rejection ratio greater than 120 dB
- Parameters guaranteed over 1 μA to 1 mA collector current
- Extremely low noise
- Superior logging characteristics compared to conventional pairs
- Plug-in replacement for presently available devices

Typical Applications

Low Cost Accurate Square Root Circuit

$I_{OUT} = 10^{-5} \cdot \sqrt{10\, V_{IN}}$

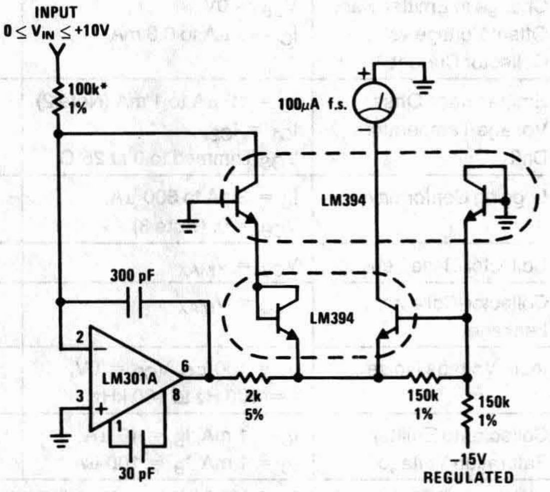


TL/H/9241–1

*Trim for full scale accuracy

Low Cost Accurate Squaring Circuit

$I_{OUT} = 10^{-6} (V_{IN})^2$



TL/H/9241–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Collector Current	20 mA
Collector-Emitter Voltage	V_{MAX}
Collector-Emitter Voltage	35V
LM394C	20V
Collector-Base Voltage	35V
LM394C	20V
Collector-Substrate Voltage	35V
LM394C	20V
Collector-Collector Voltage	35V
LM394C	20V

Base-Emitter Current	±10 mA
Power Dissipation	500 mW
Junction Temperature	
LM194	−55°C to +125°C
LM394/LM394B/LM394C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Metal Can Package (10 sec.)	260°C
Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($T_J = 25°C$)

Parameter	Conditions	LM194			LM394			LM394B/394C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Current Gain (h_{FE})	V_{CB} = 0V to V_{MAX} (Note 1)										
	I_C = 1 mA	350	700		300	700		225	500		
	I_C = 100 µA	350	550		250	550		200	400		
	I_C = 10 µA	300	450		200	450		150	300		
	I_C = 1 µA	200	300		150	300		100	200		
Current Gain Match, (h_{FE} Match)	V_{CB} = 0V to V_{MAX} I_C = 10 µA to 1 mA		0.5	2		0.5	4		1.0	5	%
$= \frac{100\,[\Delta I_B]\,[h_{FE(MIN)}]}{I_C}$	I_C = 1 µA		1.0			1.0			2.0		%
Emitter-Base Offset Voltage	V_{CB} = 0 I_C = 1 µA to 1 mA		25	100		25	150		50	200	µV
Change in Emitter-Base Offset Voltage vs Collector-Base Voltage (CMRR)	(Note 1) I_C = 1 µA to 1 mA, V_{CB} = 0V to V_{MAX}		10	25		10	50		10	100	µV
Change in Emitter-Base Offset Voltage vs Collector Current	V_{CB} = 0V, I_C = 1 µA to 0.3 mA		5	25		5	50		5	50	µV
Emitter-Base Offset Voltage Temperature Drift	I_C = 10 µA to 1 mA (Note 2) $I_{C1} = I_{C2}$		0.08	0.3		0.08	1.0		0.2	1.5	µV/°C
	V_{OS} Trimmed to 0 at 25°C		0.03	0.1		0.03	0.3		0.03	0.5	µV/°C
Logging Conformity	I_C = 3 nA to 300 µA, V_{CB} = 0, (Note 3)		150			150			150		µV
Collector-Base Leakage	$V_{CB} = V_{MAX}$		0.05	0.25		0.05	0.5		0.05	0.5	nA
Collector-Collector Leakage	$V_{CC} = V_{MAX}$		0.1	2.0		0.1	5.0		0.1	5.0	nA
Input Voltage Noise	I_C = 100 µA, V_{CB} = 0V, f = 100 Hz to 100 kHz		1.8			1.8			1.8		$nV/\sqrt{Hz}$
Collector to Emitter Saturation Voltage	I_C = 1 mA, I_B = 10 µA		0.2			0.2			0.2		V
	I_C = 1 mA, I_B = 100 µA		0.1			0.1			0.1		V

Note 1: Collector-base voltage is swept from 0 to V_{MAX} at a collector current of 1 µA, 10 µA, 100 µA, and 1 mA.

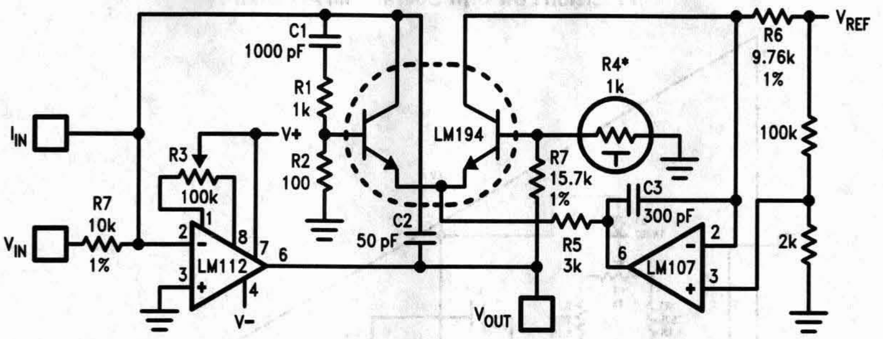
Note 2: Offset voltage drift with V_{OS} = 0 at T_A = 25°C is valid only when the ratio of I_{C1} to I_{C2} is adjusted to give the initial zero offset. This ratio must be held to within 0.003% over the entire temperature range. Measurements taken at +25°C and temperature extremes.

Note 3: Logging conformity is measured by computing the best fit to a true exponential and expressing the error as a base-emitter voltage deviation.

Note 4: Refer to RETS194X drawing of military LM194H version for specifications.

Typical Applications (Continued)

Fast, Accurate Logging Amplifier, V_{IN} = 10V to 0.1 mV or I_{IN} = 1 mA to 10 nA

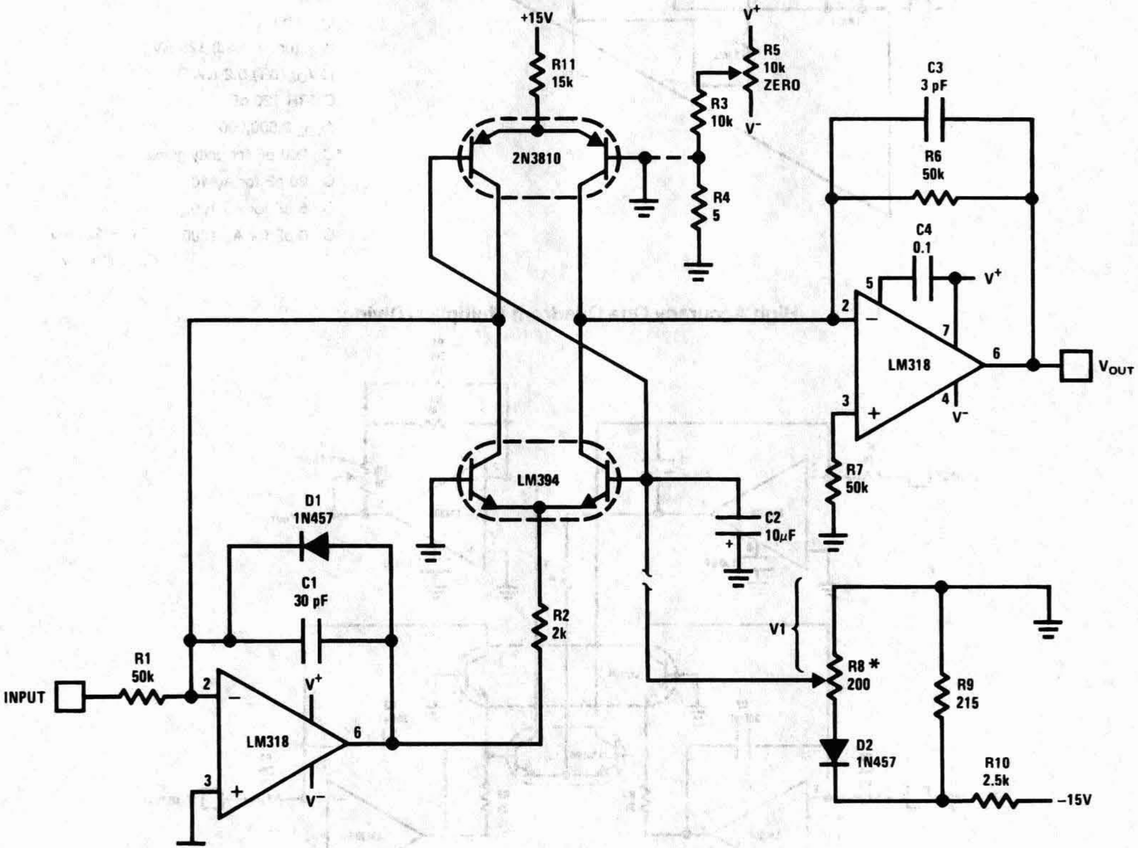

C1
1000 pF
R1
1k
R2
100
V+
R3
100k
R7
10k
1%
I_{IN}
V_{IN}
LM112
1
2
3
4
6
7
8
V−
C2
50 pF
LM194
R7
15.7k
1%
R5
3k
V_{OUT}
R4*
1k
C3
300 pF
LM107
2
3
6
R6
9.76k
1%
V_{REF}
100k
2k

TL/H/9241–3

*1 kΩ (±1%) at 25°C, +3500 ppm/°C.
Available from Vishay Ultronix,
Grand Junction, CO, Q81 Series.

$$V_{OUT} = -\log_{10}\left(\frac{V_{IN}}{V_{REF}}\right)$$

Voltage Controlled Variable Gain Amplifier


+15V
R11
15k
2N3810
V^+
R5
10k
ZERO
V^-
R3
10k
R4
5
C3
3 pF
R6
50k
C4
0.1
5
V^+
2
7
LM318
6
3
4
V^-
V_{OUT}
R7
50k
LM394
C2
10µF
+
D1
1N457
C1
30 pF
R2
2k
R1
50k
INPUT
2
V^+
LM318
6
3
+
V^-
V1
R8 *
200
R9
215
D2
1N457
R10
2.5k
−15V

TL/H/9241–4

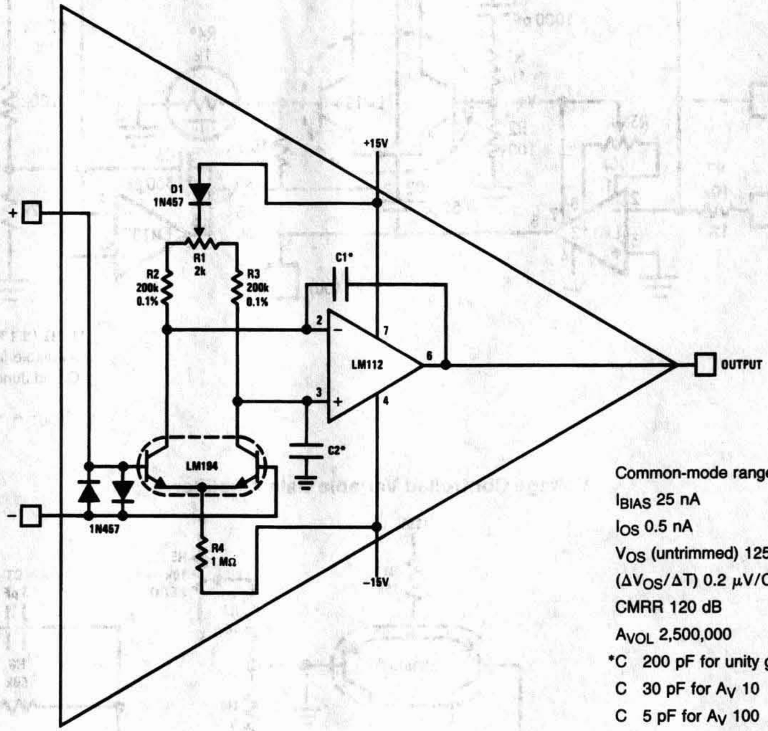
*R8–R10 and D2 provide a temperature independent gain control.
G = −336 V1 (dB)

Distortion < 0.1%
Bandwidth > 1 MHz
100 dB gain range

5

Typical Applications (Continued)

Precision Low Drift Operational Amplifier


+15V
D1
1N457
R1
2k
R2
200k
0.1%
R3
200k
0.1%
C1*
2
7
LM112
6
3
4
C2*
LM194
+
−
1N457
R4
1 MΩ
−15V
OUTPUT

Common-mode range 10V

I_{BIAS} 25 nA

I_{OS} 0.5 nA

V_{OS} (untrimmed) 125 μV

($\Delta V_{OS}/\Delta T$) 0.2 μV/C

CMRR 120 dB

A_{VOL} 2,500,000

*C 200 pF for unity gain

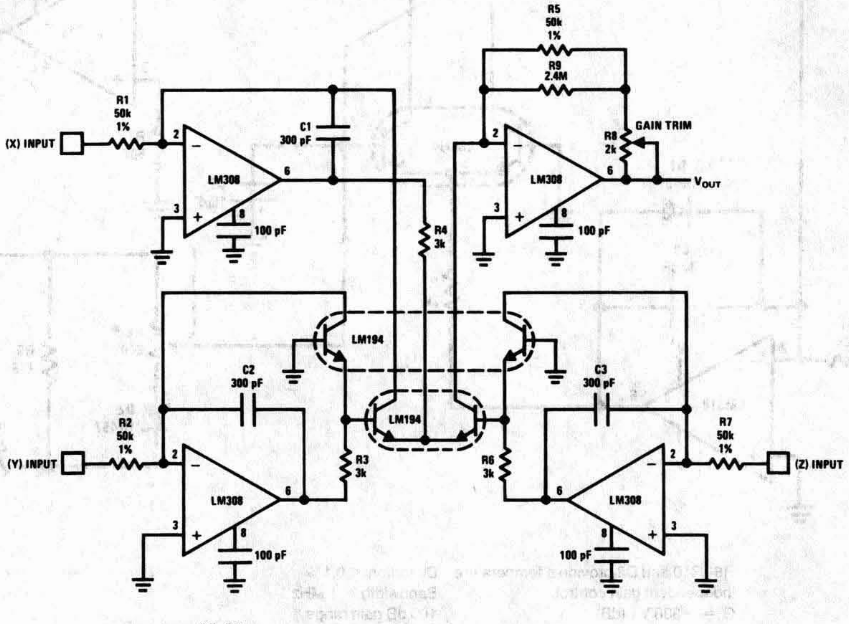
C 30 pF for A_V 10

C 5 pF for A_V 100

C 0 pF for A_V 1000

TL/H/9241-5

High Accuracy One Quadrant Multiplier/Divider


R1
50k
1%
(X) INPUT
2
3
LM308
6
8
100 pF
C1
300 pF
R4
3k
R5
50k
1%
R9
2.4M
GAIN TRIM
R8
2k
LM308
V_{OUT}
100 pF
LM194
LM194
C2
300 pF
C3
300 pF
R2
50k
1%
(Y) INPUT
LM308
100 pF
R3
3k
R6
3k
LM308
100 pF
R7
50k
1%
(Z) INPUT

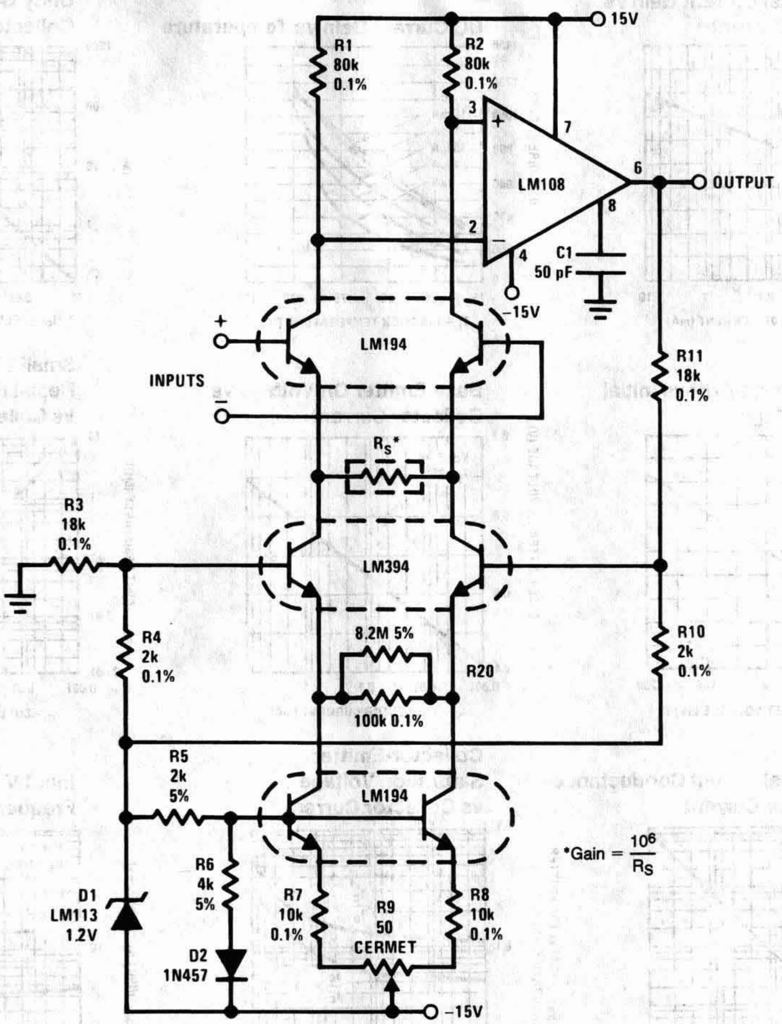
TL/H/9241-6

$$V_{OUT} = \frac{(X)\,(Y)}{(Z)}\text{; positive inputs only.}$$

*Typical linearity 0.1%

Typical Applications (Continued)

High Performance Instrumentation Amplifier


R1
80k
0.1%
R2
80k
0.1%
15V
3
7
LM108
6
OUTPUT
8
2
4
C1
50 pF
−15V
+
INPUTS
−
LM194
R11
18k
0.1%
R_S*
R3
18k
0.1%
LM394
R4
2k
0.1%
8.2M 5%
R20
100k 0.1%
R10
2k
0.1%
R5
2k
5%
LM194
$\text{*Gain} = \frac{10^6}{R_S}$
R6
4k
5%
D1
LM113
1.2V
R7
10k
0.1%
R9
50
CERMET
R8
10k
0.1%
D2
1N457
−15V

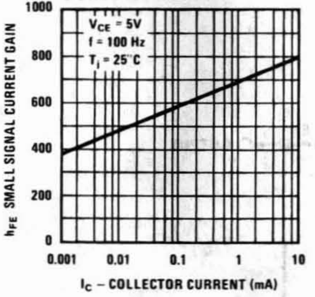
TL/H/9241-7

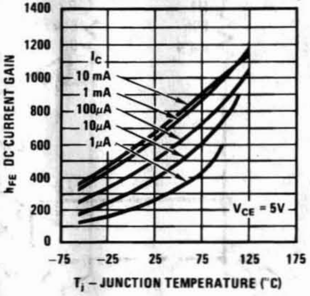
Performance Characteristics

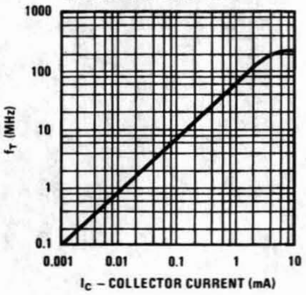
	G = 10,000	G = 1,000	G = 100	G = 10	
Linearity of Gain (± 10V Output)	≤0.01	≤0.01	≤0.02	≤0.05	%
Common-Mode Rejection Ratio (60 Hz)	≥120	≥120	≥110	≥90	dB
Common-Mode Rejection Ratio (1 kHz)	≥110	≥110	≥90	≥70	dB
Power Supply Rejection Ratio					
+ Supply	>110	>110	>110	>110	dB
− Supply	>110	>110	>90	>70	dB
Bandwidth (−3 dB)	50	50	50	50	kHz
Slew Rate	0.3	0.3	0.3	0.3	V/μs
Offset Voltage Drift**	≤0.25	≤0.4	2	≤10	μV/°C
Common-Mode Input Resistance	$>10^9$	$>10^9$	$>10^9$	$>10^9$	Ω
Differential Input Resistance	$>3 \times 10^8$	$>3 \times 10^8$	$>3 \times 10^8$	$>3 \times 10^8$	Ω
Input Referred Noise (100 Hz ≤ f ≤ 10 kHz)	5	6	12	70	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
Input Bias Current	75	75	75	75	nA
Input Offset Current	1.5	1.5	1.5	1.5	nA
Common-Mode Range	±11	±11	±11	±10	V
Output Swing (R_L = 10 kΩ)	±13	±13	±13	±13	V

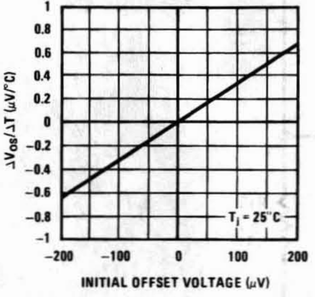
**Assumes ≤ 5 ppm/°C tracking of resistors

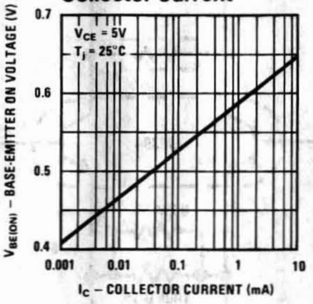
Typical Performance Characteristics

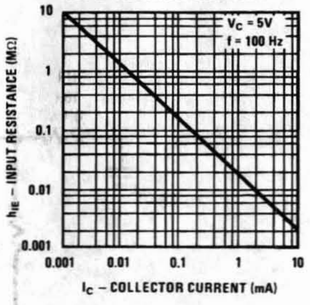

Small Signal Current Gain vs Collector Current

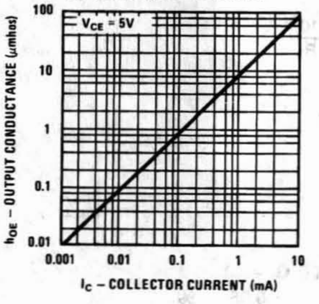

DC Current Gain vs Temperature

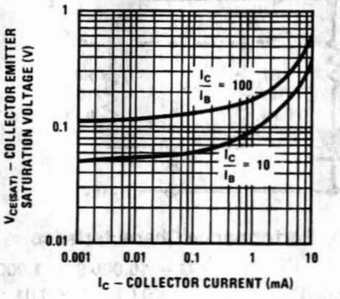

Unity Gain Frequency (f_t) vs Collector Current

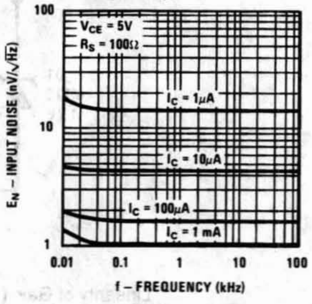

Offset Voltage Drift vs Initial Offset Voltage

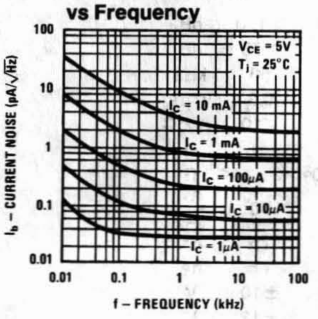

Base-Emitter On Voltage vs Collector Current

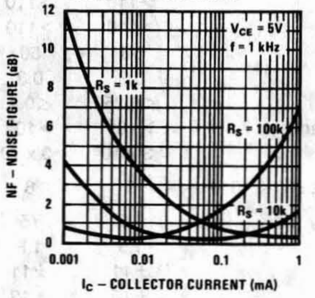

Small Signal Input Resistance (h_{ie}) vs Collector Current

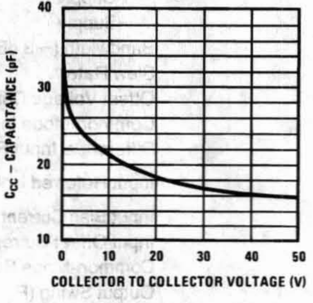

Small Signal Output Conductance vs Collector Current


Collector-Emitter Saturation Voltage vs Collector Current


Input Voltage Noise vs Frequency


Base Current Noise vs Frequency

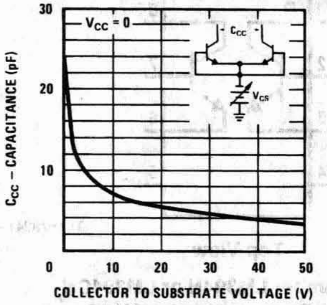

Noise Figure vs Collector Current


Collector to Collector Capacitance vs Reverse Bias Voltage

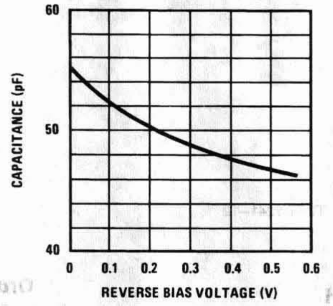
TL/H/9241–8

Typical Performance Characteristics (Continued)

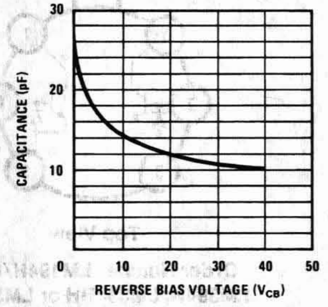
Collector to Collector Capacitance vs Collector-Substrate Voltage



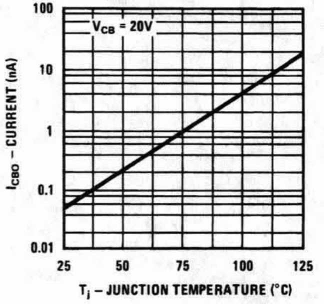
Emitter-Base Capacitance vs Reverse Bias Voltage



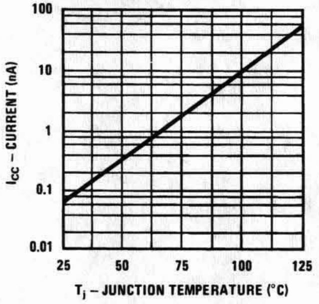
Collector-Base Capacitance vs Reverse Bias Voltage



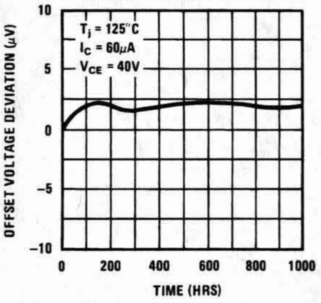
Collector-Base Leakage vs Temperature



Collector to Collector Leakage vs Temperature

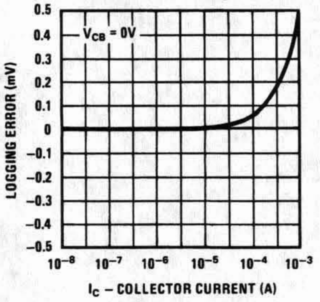


Offset Voltage Long Term Stability at High Temperature



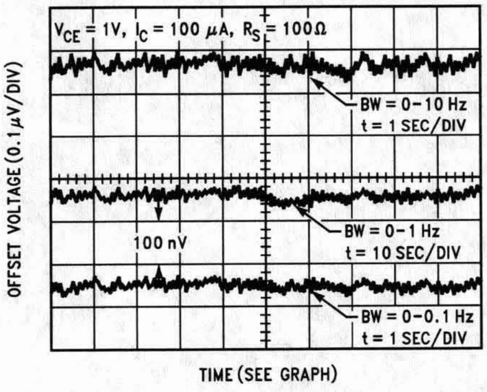
TL/H/9241–9

Emitter-Base Log Conformity



TL/H/9241–10

Low Frequency Noise of Differential Pair*

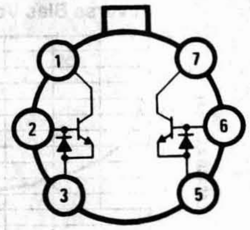


TL/H/9241–11

*Unit must be in still air environment so that differential lead temperature is held to less than 0.0003°C.

Connection Diagrams

Metal Can Package

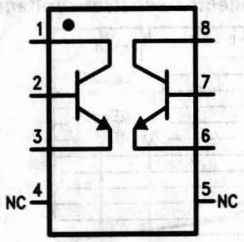


TL/H/9241–12

Top View

Order Number LM194H/883*, LM394H, LM394BH or LM394CH
See NS Package Number H06C

Dual-In-Line and Small Outline Packages



TL/H/9241–13

Top View

Order Number LM394N or LM394CN
See NS Package Number N08E

*Available per SMD #5962-8777701

National Semiconductor

LM195/LM395 Ultra Reliable Power Transistors

General Description

The LM195/LM395 are fast, monolithic power transistors with complete overload protection. These devices, which act as high gain power transistors, have included on the chip, current limiting, power limiting, and thermal overload protection making them virtually impossible to destroy from any type of overload. In the standard TO-3 transistor power package, the LM195 will deliver load currents in excess of 1.0A and can switch 40V in 500 ns.

The inclusion of thermal limiting, a feature not easily available in discrete designs, provides virtually absolute protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive heating.

The LM195 offers a significant increase in reliability as well as simplifying power circuitry. In some applications, where protection is unusually difficult, such as switching regulators, lamp or solenoid drivers where normal power dissipation is low, the LM195 is especially advantageous.

The LM195 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LM195 as with any power transistor. When the device is used as an emitter follower with low source impedance, it is necessary to insert a 5.0k resistor in series with the base lead to prevent possible emitter follower oscillations. Although the device is usually stable as an emitter follower, the resistor eliminates the possibility of trouble without degrading performance. Finally, since it has good high frequency response, supply bypassing is recommended.

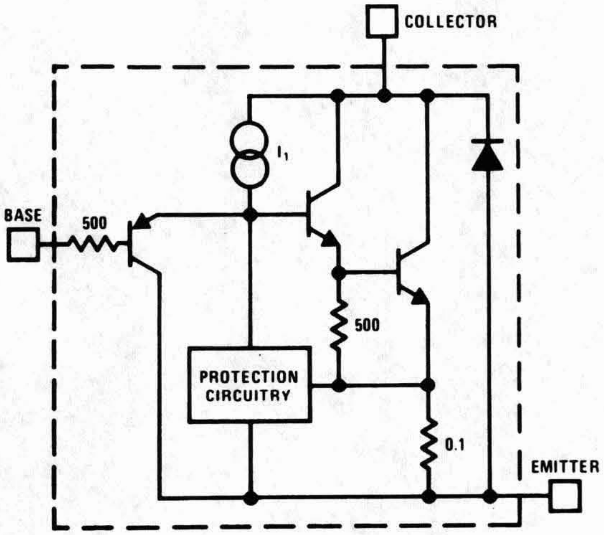
For low-power applications (under 100 mA), refer to the LP395 Ultra Reliable Power Transistor.

The LM195/LM395 are available in standard TO-3 power packages and solid Kovar TO-5. The LM195 is rated for operation from −55°C to +150°C and the LM395 from 0°C to +125°C.

Features

- Internal thermal limiting
- Greater than 1.0A output current
- 3.0 μA typical base current
- 500 ns switching time
- 2.0V saturation
- Base can be driven up to 40V without damage
- Directly interfaces with CMOS or TTL
- 100% electrical burn-in

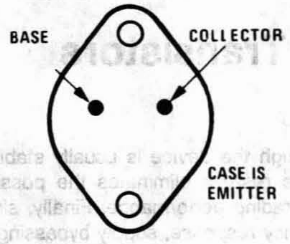
Simplified Circuit



TL/H/6009–1

Connection Diagrams

TO-3 Metal Can Package

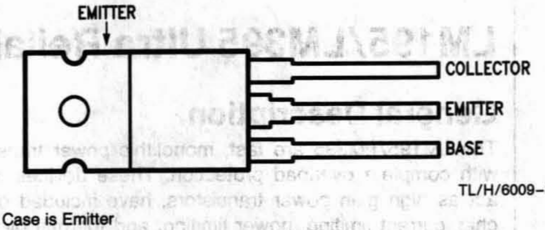

BASE
COLLECTOR
CASE IS EMITTER

TL/H/6009-2

Bottom View

Order Number LM195K/883
See NS Package Number K02A

TO-220 Plastic Package

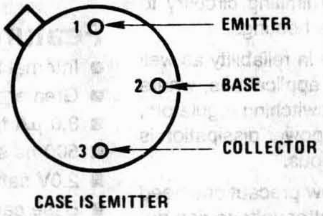

EMITTER
COLLECTOR
EMITTER
BASE
Case is Emitter

TL/H/6009-3

Top View

Order Number LM395T
See NS Package Number T03B

TO-5 Metal Can Package


1
EMITTER
2
BASE
3
COLLECTOR
CASE IS EMITTER

TL/H/6009-4

Bottom View

Order Number LM195H/883
See NS Package Number H03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Collector to Emitter Voltage	
LM195	42V
LM395	36V
Collector to Base Voltage	
LM195	42V
LM395	36V
Base to Emitter Voltage (Forward)	
LM195	42V
LM395	36V
Base to Emitter Voltage (Reverse)	20V
Collector Current	Internally Limited
Power Dissipation	Internally Limited
Operating Temperature Range	
LM195	−55°C to +150°C
LM395	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Preconditioning

100% Burn-In In Thermal Limit

Electrical Characteristics (Note 1)

Parameter	Conditions	LM195			LM395			Units
		Min	Typ	Max	Min	Typ	Max	
Collector-Emitter Operating Voltage (Note 3)	$I_Q \le I_C \le I_{MAX}$			42			36	V
Base to Emitter Breakdown Voltage	$0 \le V_{CE} \le V_{CEMAX}$	42			36	60		V
Collector Current								
TO-3, TO-220	$V_{CE} \le 15V$	1.2	2.2		1.0	2.2		A
TO-5	$V_{CE} \le 7.0V$	1.2	1.8		1.0	1.8		A
Saturation Voltage	$I_C \le 1.0A$, $T_A = 25°C$		1.8	2.0		1.8	2.2	V
Base Current	$0 \le I_C \le I_{MAX}$ $0 \le V_{CE} \le V_{CEMAX}$		3.0	5.0		3.0	10	μA
Quiescent Current (I_Q)	$V_{be} = 0$ $0 \le V_{CE} \le V_{CEMAX}$		2.0	5.0		2.0	10	mA
Base to Emitter Voltage	$I_C = 1.0A$, $T_A = +25°C$		0.9			0.9		V
Switching Time	$V_{CE} = 36V$, $R_L = 36\Omega$, $T_A = 25°C$		500			500		ns
Thermal Resistance Junction to Case (Note 2)	TO-3 Package (K)		2.3	3.0		2.3	3.0	°C/W
	TO-5 Package (H)		12	15		12	15	°C/W
	TO-220 Package (T)					4	6	°C/W

Note 1: Unless otherwise specified, these specifications apply for $-55°C \le T_j \le +150°C$ for the LM195 and $0°C \le +125°C$ for the LM395.

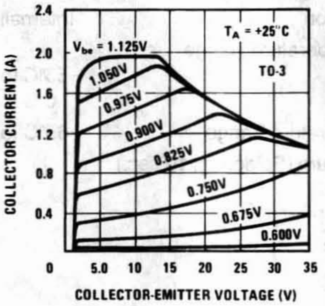
Note 2: Without a heat sink, the thermal resistance of the TO-5 package is about +150°C/W, while that of the TO-3 package is +35°C/W.

Note 3: Selected devices with higher breakdown available.

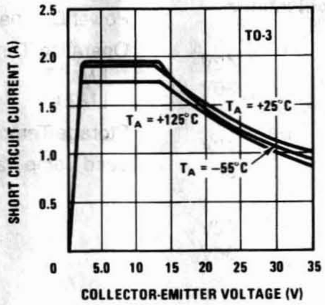
Note 4: Refer to RETS195H and RETS195K drawings of military LM195H and LM195K versions for specifications.

Typical Performance Characteristics (for K and T Packages)

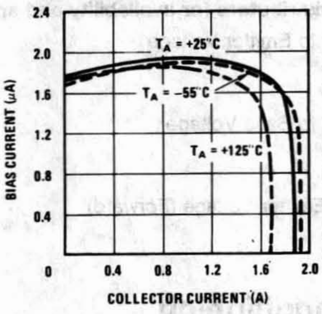
Collector Characteristics



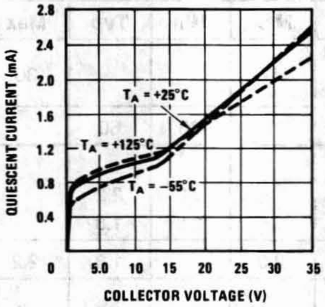
Short Circuit Current



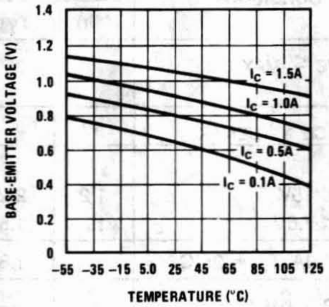
Bias Current



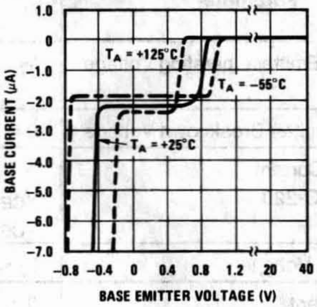
Quiescent Current



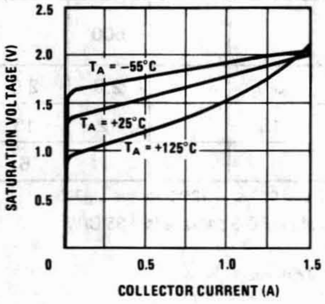
Base Emitter Voltage



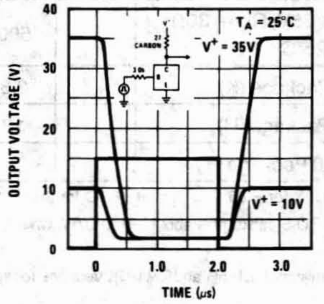
Base Current



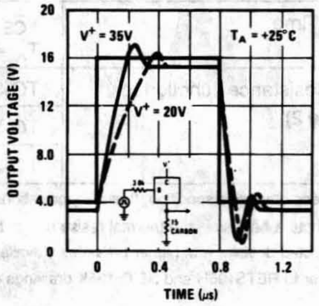
Saturation Voltage



Response Time



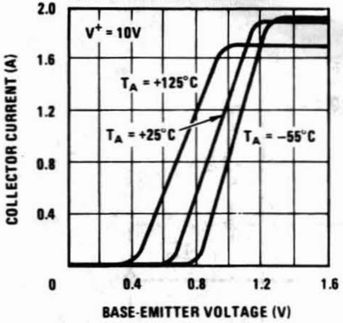
Response Time



TL/H/6009–6

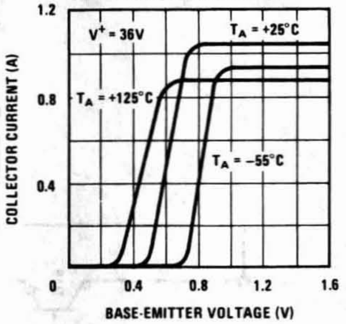
Typical Performance Characteristics (for K and T Packages) (Continued)

10V Transfer Function



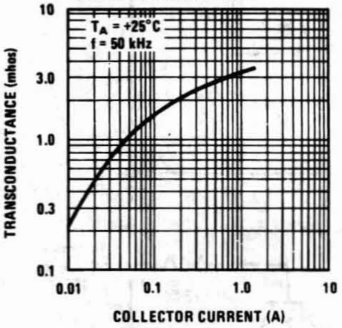
TL/H/6009–7

36V Transfer Function



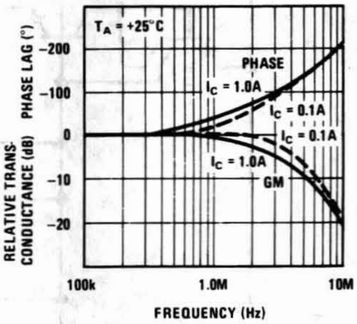
TL/H/6009–8

Transconductance



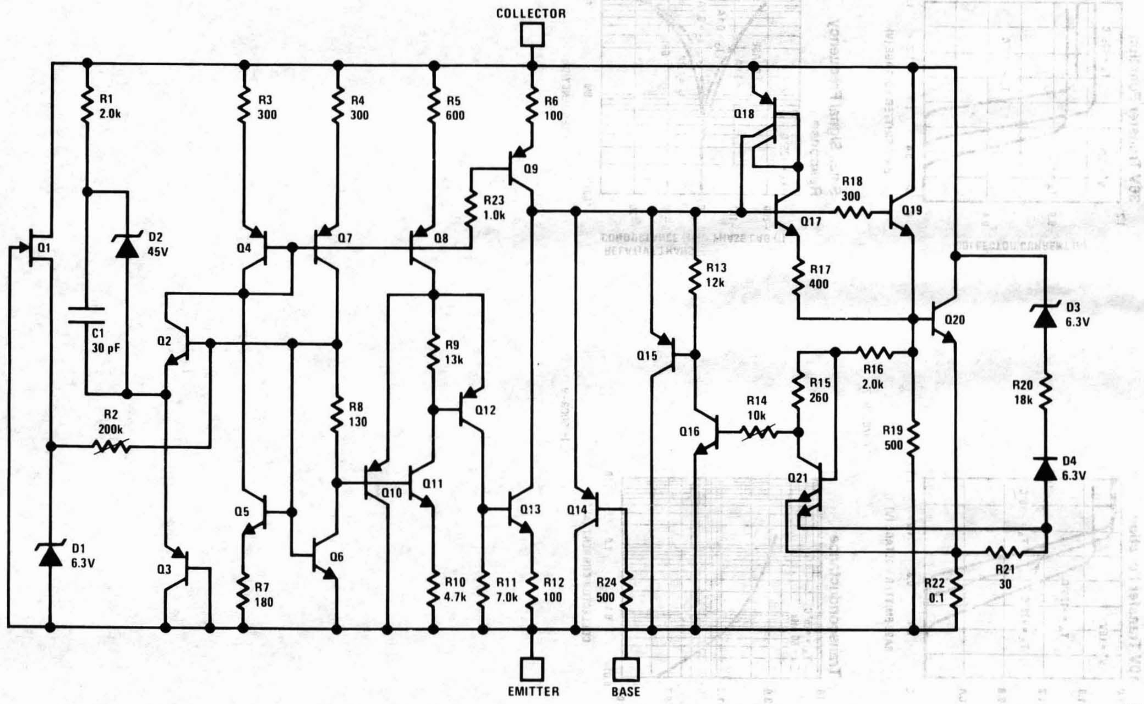
TL/H/6009–9

Small Signal Frequency Response



TL/H/6009–10

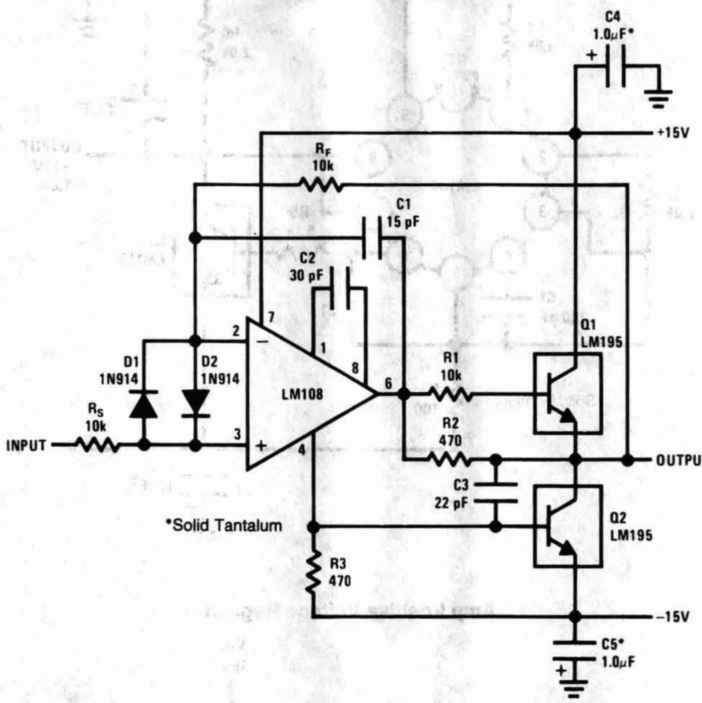
Schematic Diagram


COLLECTOR
EMITTER
BASE
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
R1 2.0k
R2 200k
R3 300
R4 300
R5 600
R6 100
R7 180
R8 130
R9 13k
R10 4.7k
R11 7.0k
R12 100
R13 12k
R14 10k
R15 260
R16 2.0k
R17 400
R18 300
R19 500
R20 18k
R21 30
R22 0.1
R23 1.0k
R24 500
C1 30 pF
D1 6.3V
D2 45V
D3 6.3V
D4 6.3V

TL/H/6009–11

Typical Applications

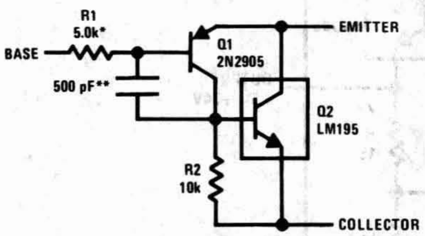
1.0 Amp Voltage Follower


C4
1.0μF*
+15V
R_F
10k
C1
15 pF
C2
30 pF
7
2
1
8
6
3
4
D1
1N914
D2
1N914
R_S
10k
INPUT
LM108
R1
10k
R2
470
Q1
LM195
OUTPUT
C3
22 pF
Q2
LM195
R3
470
−15V
C5*
1.0μF

*Solid Tantalum

TL/H/6009-12

Power PNP

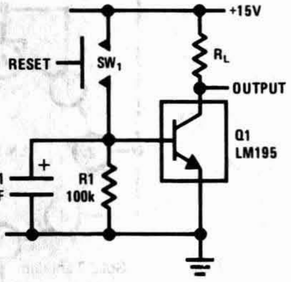

R1
5.0k*
BASE
500 pF**
Q1
2N2905
EMITTER
Q2
LM195
R2
10k
COLLECTOR

TL/H/6009-13

*Protects against excessive base drive

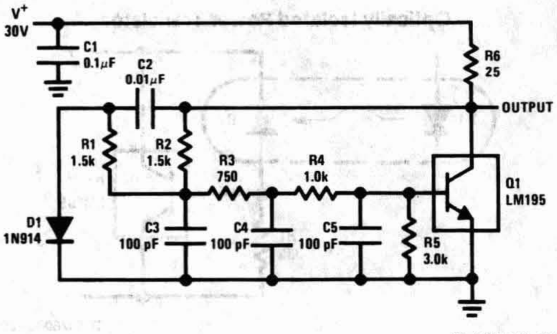
**Needed for stability

Time Delay


+15V
RESET
SW_1
R_L
OUTPUT
Q1
LM195
C1
10μF
R1
100k

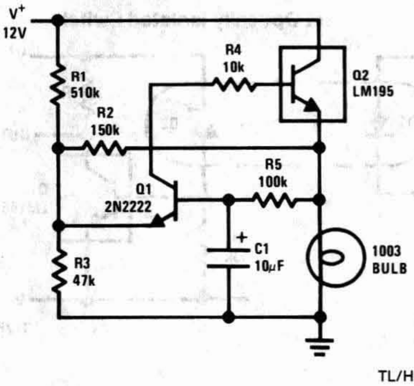
TL/H/6009-14

1.0 MHz Oscillator


V+
30V
C1
0.1μF
C2
0.01μF
R6
25
OUTPUT
R1
1.5k
R2
1.5k
R3
750
R4
1.0k
Q1
LM195
D1
1N914
C3
100 pF
C4
100 pF
C5
100 pF
R5
3.0k

TL/H/6009-15

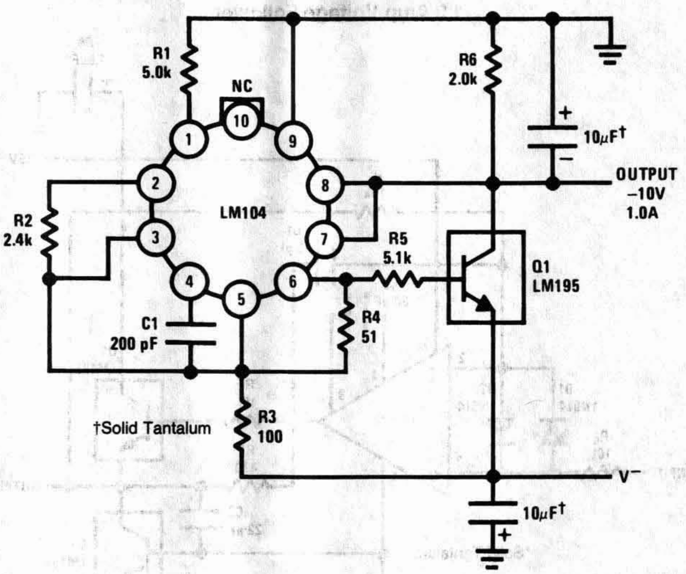
1.0 Amp Lamp Flasher


V+
12V
R4
10k
Q2
LM195
R1
510k
R2
150k
R5
100k
Q1
2N2222
R3
47k
C1
10μF
1003
BULB

TL/H/6009-16

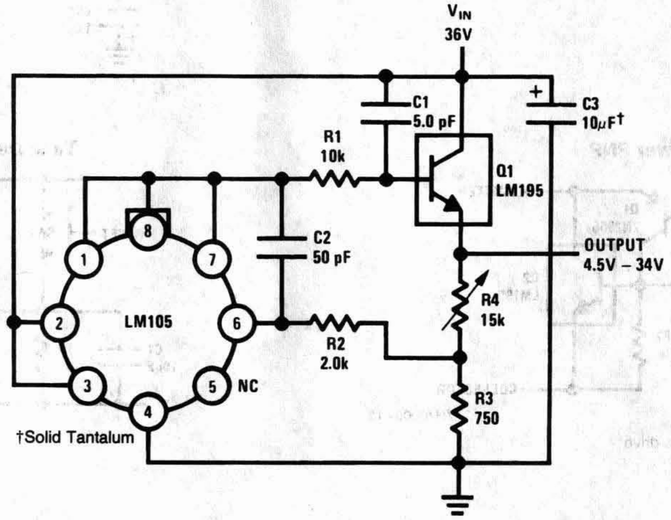
Typical Applications (Continued)

1.0 Amp Negative Regulator


R1
5.0k
NC
10
1
9
2
8
3
7
4
5
6
LM104
R2
2.4k
C1
200 pF
R4
51
R5
5.1k
R3
100
R6
2.0k
10μF†
OUTPUT
−10V
1.0A
Q1
LM195
V−
10μF†
†Solid Tantalum

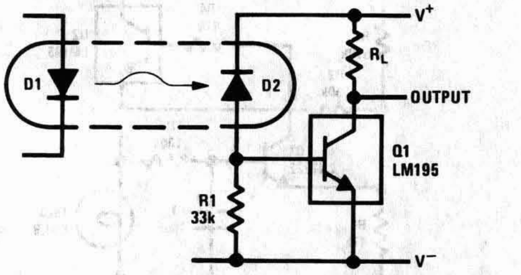
TL/H/6009-17

1.0 Amp Positive Voltage Regulator


V_IN
36V
C1
5.0 pF
C3
10μF†
R1
10k
Q1
LM195
8
1
7
2
6
3
5
4
NC
LM105
C2
50 pF
R2
2.0k
OUTPUT
4.5V – 34V
R4
15k
R3
750
†Solid Tantalum

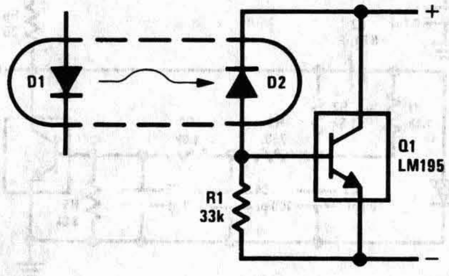
TL/H/6009-18

Fast Optically Isolated Switch


V+
R_L
D1
D2
OUTPUT
Q1
LM195
R1
33k
V−

TL/H/6009-19

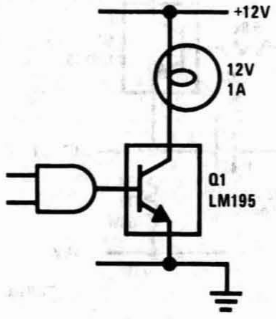
Optically Isolated Power Transistor


+
D1
D2
Q1
LM195
R1
33k
−

TL/H/6009-20

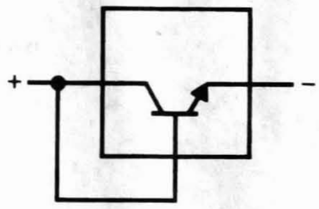
Typical Applications (Continued)

CMOS or TTL Lamp Interface


+12V
12V
1A
Q1
LM195

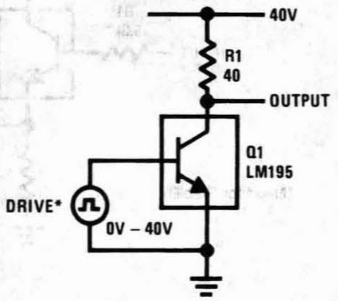
TL/H/6009-21

Two Terminal Current Limiter



TL/H/6009-22

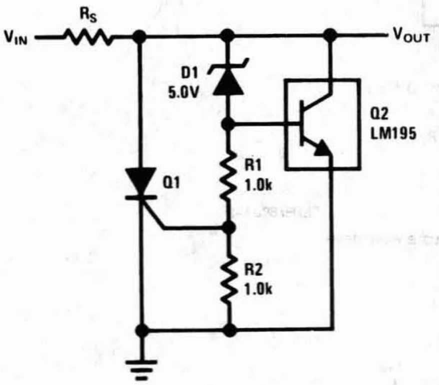
40V Switch


40V
R1
40
OUTPUT
Q1
LM195
DRIVE*
0V – 40V

TL/H/6009-23

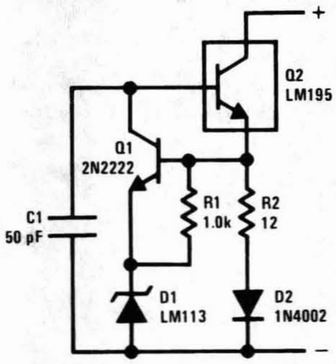
*Drive Voltage 0V to ≥ 10V ≤ 42V

6.0V Shunt Regulator with Crowbar


R$_S$
V$_{IN}$
V$_{OUT}$
D1
5.0V
Q2
LM195
Q1
R1
1.0k
R2
1.0k

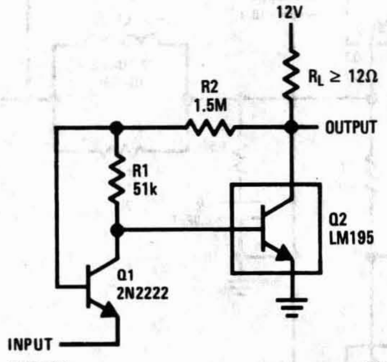
TL/H/6009-24

Two Terminal 100 mA Current Regulator


+
Q2
LM195
Q1
2N2222
R1
1.0k
R2
12
C1
50 pF
D1
LM113
D2
1N4002
−

TL/H/6009-25

Low Level Power Switch

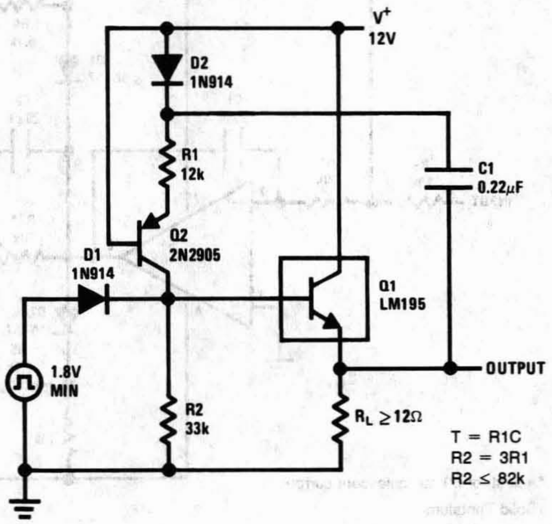

12V
R$_L$ ≥ 12Ω
R2
1.5M
OUTPUT
R1
51k
Q2
LM195
Q1
2N2222
INPUT

Turn ON = 350 mV

Turn OFF = 200 mV

TL/H/6009-26

Power One-Shot


V$^+$
12V
D2
1N914
R1
12k
C1
0.22μF
Q2
2N2905
D1
1N914
Q1
LM195
OUTPUT
1.8V
MIN
R2
33k
R$_L$ ≥12Ω

T = R1C

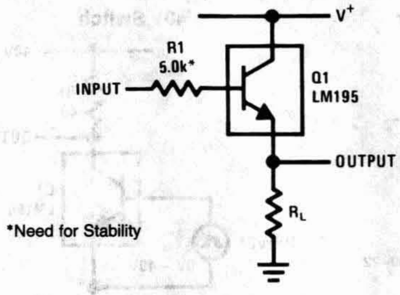
R2 = 3R1

R2 ≤ 82k

TL/H/6009-27

Typical Applications (Continued)

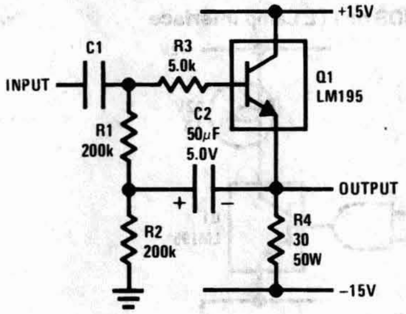
Emitter Follower


V+
R1
5.0k*
INPUT
Q1
LM195
OUTPUT
R_L

*Need for Stability

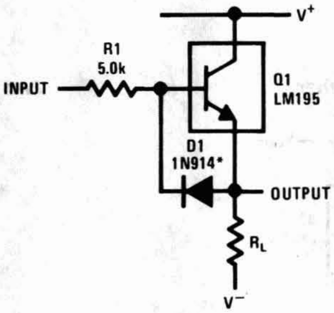
TL/H/6009-28

High Input Impedance AC Emitter Follower


+15V
C1
R3
5.0k
INPUT
Q1
LM195
R1
200k
C2
50μF
5.0V
OUTPUT
R4
30
50W
R2
200k
−15V

TL/H/6009-29

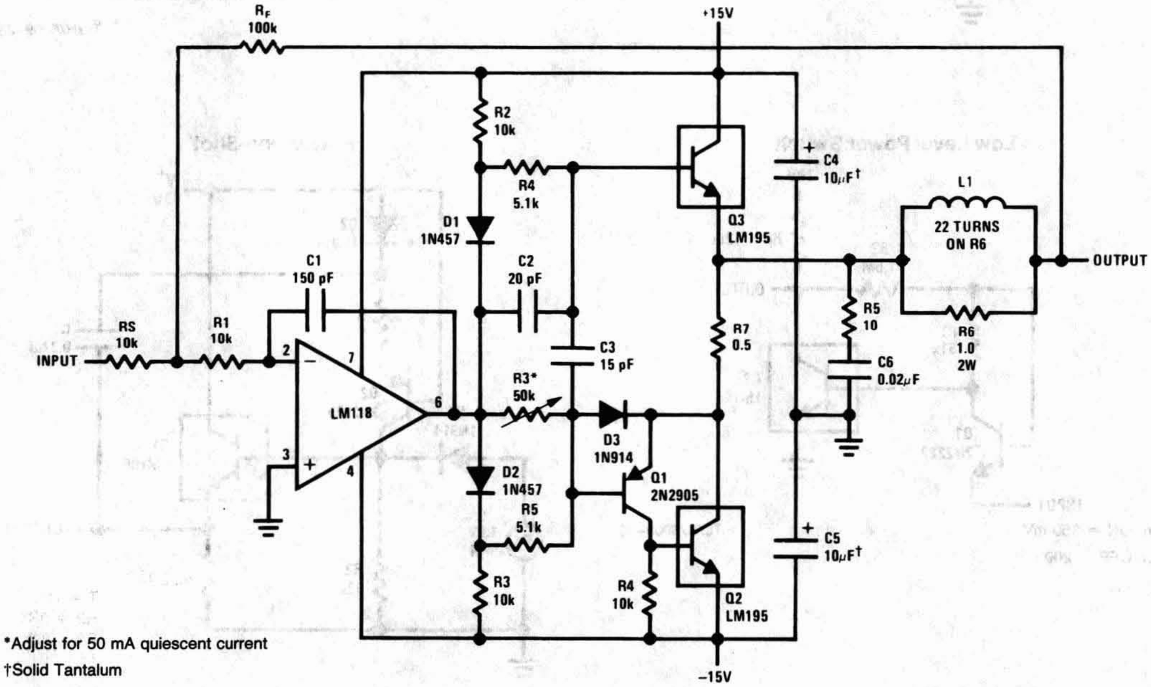
Fast Follower


V+
R1
5.0k
INPUT
Q1
LM195
D1
1N914*
OUTPUT
R_L
V−

TL/H/6009-30

*Prevents storage with fast fall time square wave drive

Power Op Amp


R_F
100k
+15V
R2
10k
R4
5.1k
C4
10μF†
L1
22 TURNS
ON R6
D1
1N457
Q3
LM195
C1
150 pF
C2
20 pF
OUTPUT
R5
10
RS
10k
R1
10k
R7
0.5
R6
1.0
2W
INPUT
C3
15 pF
C6
0.02μF
LM118
R3*
50k
D3
1N914
D2
1N457
Q1
2N2905
R5
5.1k
C5
10μF†
R3
10k
R4
10k
Q2
LM195
−15V
2
7
6
3
4

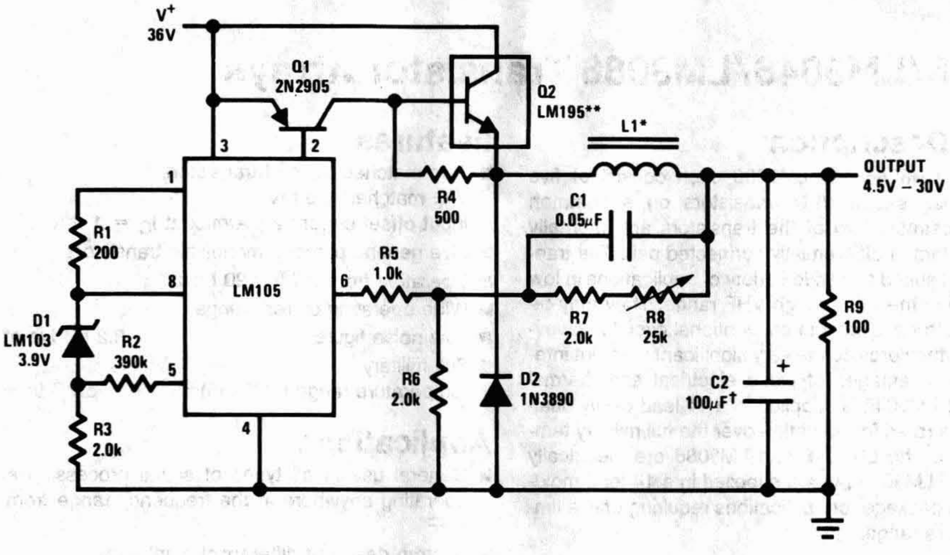
*Adjust for 50 mA quiescent current

†Solid Tantalum

TL/H/6009-31

Typical Applications (Continued)

6.0 Amp Variable Output Switching Regulator


V+
36V
Q1
2N2905
Q2
LM195**
L1*
OUTPUT
4.5V – 30V
3
2
1
R4
500
C1
0.05μF
R1
200
8
R5
1.0k
6
LM105
R7
2.0k
R8
25k
R9
100
D1
LM103
3.9V
R2
390k
5
R6
2.0k
D2
1N3890
C2
100μF†
+
R3
2.0k
4

TL/H/6009–32

*Sixty turns wound on Arnold Type A-083081-2 core.

**Four devices in parallel

†Solid tantalum

National Semiconductor

LM3045/LM3046/LM3086 Transistor Arrays

General Description

The LM3045, LM3046 and LM3086 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3045 is supplied in a 14-lead cavity dual-in-line package rated for operation over the full military temperature range. The LM3046 and LM3086 are electrically identical to the LM3045 but are supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

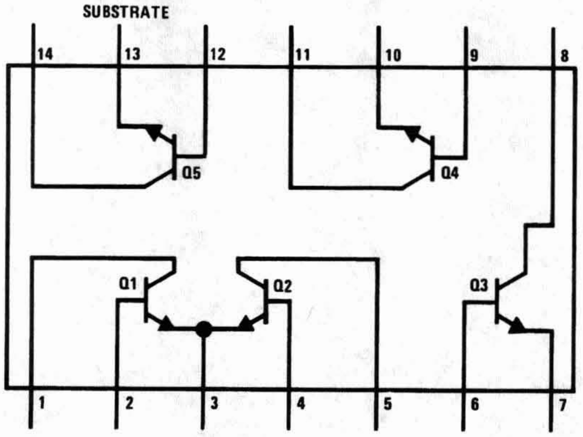
- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 μA max at $I_C = 1$ mA
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz
- Full military temperature range (LM3045) −55°C to +125°C

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Schematic and Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7950–1

Top View

Order Number LM3045J, LM3046M, LM3046N or LM3086N
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings (T_A = 25°C)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM3045		LM3046/LM3086		
	Each Transistor	Total Package	Each Transistor	Total Package	Units
Power Dissipation:					
T_A = 25°C	300	750	300	750	mW
T_A = 25°C to 55°C			300	750	mW
T_A > 55°C			Derate at 6.67		mW/°C
T_A = 25°C to 75°C	300	750			mW
T_A > 75°C	Derate at 8				mW/°C
Collector to Emitter Voltage, V_{CEO}	15		15		V
Collector to Base Voltage, V_{CBO}	20		20		V
Collector to Substrate Voltage, V_{CIO} (Note 1)	20		20		V
Emitter to Base Voltage, V_{EBO}	5		5		V
Collector Current, I_C	50		50		mA
Operating Temperature Range	−55°C to +125°C		−40°C to +85°C		
Storage Temperature Range	−65°C to +150°C		−65°C to +85°C		
Soldering Information					
Dual-In-Line Package Soldering (10 Sec.)	260°C		260°C		
Small Outline Package					
Vapor Phase (60 Seconds)			215°C		
Infrared (15 Seconds)			220°C		

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Parameter	Conditions	Limits LM3045, LM3046			Limits LM3086			Units
		Min	Typ	Max	Min	Typ	Max	
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	I_C = 10 μA, I_E = 0	20	60		20	60		V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	I_C = 1 mA, I_B = 0	15	24		15	24		V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	I_C = 10 μA, I_{CI} = 0	20	60		20	60		V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$)	I_E 10 μA, I_C = 0	5	7		5	7		V
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V, I_E = 0		0.002	40		0.002	100	nA
Collector Cutoff Current (I_{CEO})	V_{CE} = 10V, I_B = 0			0.5			5	μA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	V_{CE} = 3V, I_C = 10 mA		100			100		
	V_{CE} = 3V, I_C = 1 mA	40	100		40	100		
	V_{CE} = 3V, I_C = 10 μA		54			54		
Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{O1} - I_{O2} \rvert$	V_{CE} = 3V, I_C = 1 mA		0.3	2				μA
Base to Emitter Voltage (V_{BE})	V_{CE} = 3V, I_E = 1 mA		0.715			0.715		V
	V_{CE} = 3V, I_E = 10 mA		0.800			0.800		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2} \rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5				mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE3} - V_{BE4} \rvert$, $\lvert V_{BE4} - V_{BE5} \rvert$, $\lvert V_{BE5} - V_{BE3} \rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5				mV
Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		−1.9			−1.9		mV/°C
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	I_B = 1 mA, I_C = 10 mA		0.23			0.23		V
Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{10}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		1.1					μV/°C

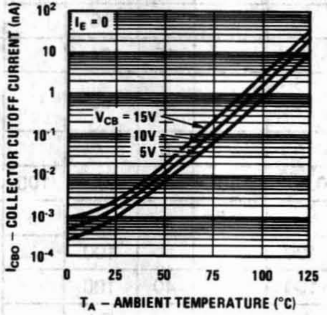
Note 1: The collector of each transistor of the LM3045, LM3046, and LM3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Electrical Characteristics (Continued)

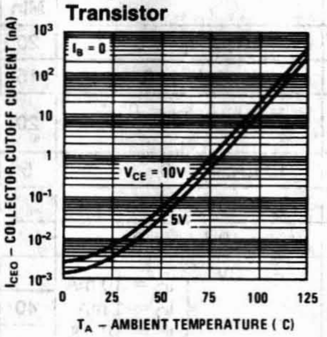
Parameter	Conditions	Min	Typ	Max	Units
Low Frequency Noise Figure (NF)	f = 1 kHz, V_{CE} = 3V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRCUIT CHARACTERISTICS					
Forward Current Transfer Ratio (h_{fe})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		110 (LM3045, LM3046) (LM3086)		
Short Circuit Input Impednace (h_{ie})			3.5		kΩ
Open Circuit Output Impedance (h_{oe})			15.6		μmho
Open Circuit Reverse Voltage Transfer Ratio (h_{re})			1.8×10^{-4}		
ADMITTANCE CHARACTERISTICS					
Forward Transfer Admittance (Y_{fe})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		
Input Admittance (Y_{ie})			0.3 + J 0.04		
Output Admittance (Y_{oe})			0.001 + j 0.03		
Reverse Transfer Admittance (Y_{re})			See Curve		
Gain Bandwidth Product (f_T)	V_{CE} = 3V, I_C = 3 mA	300	550		
Emitter to Base Capacitance (C_{EB})	V_{EB} = 3V, I_E = 0		0.6		pF
Collector to Base Capacitance (C_{CB})	V_{CB} = 3V, I_C = 0		0.58		pF
Collector to Substrate Capacitance (C_{CI})	V_{CS} = 3V, I_C = 0		2.8		pF

Typical Performance Characteristics

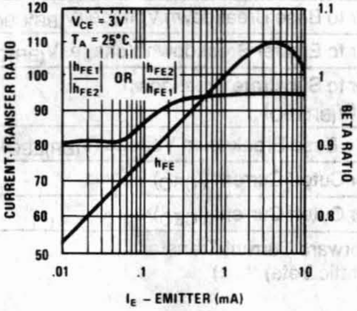
Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor



Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor

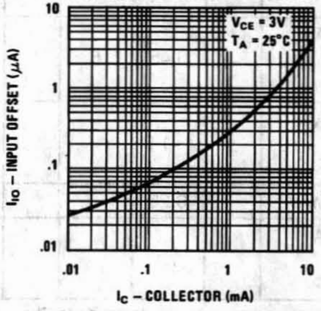


Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current

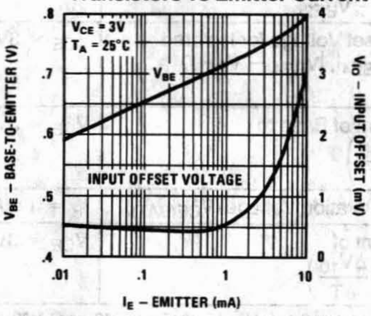


TL/H/7950–2

Typical Input Offset Current for Matched Transistor Pair Q_1 Q_2 vs Collector Current

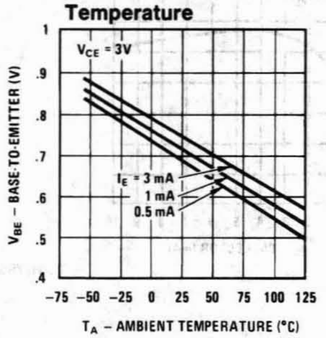


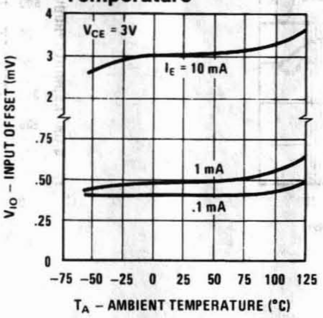
Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current

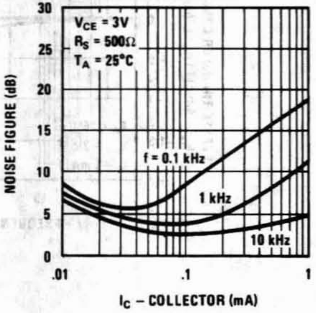


TL/H/7950–3

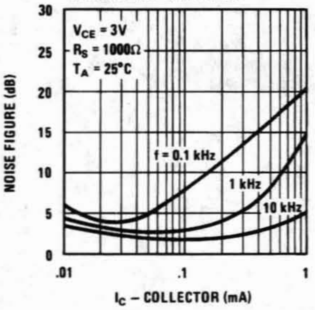
Typical Performance Characteristics (Continued)

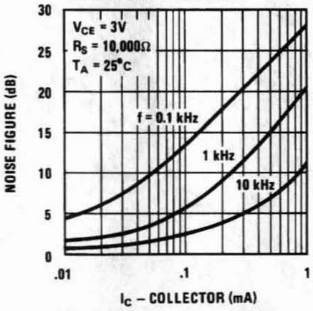

Typical Base To Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

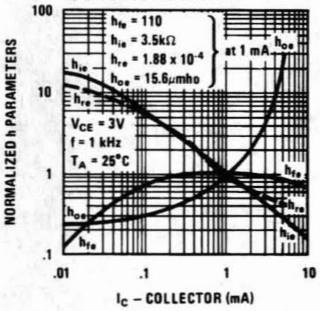

Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature


Typical Noise Figure vs Collector Current

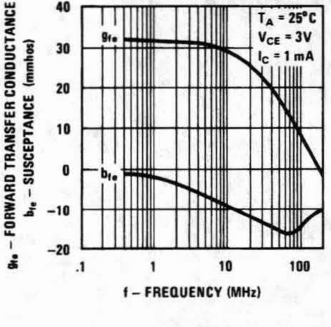
TL/H/7950–4

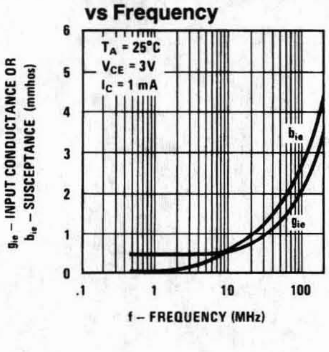

Typical Noise Figure vs Collector Current

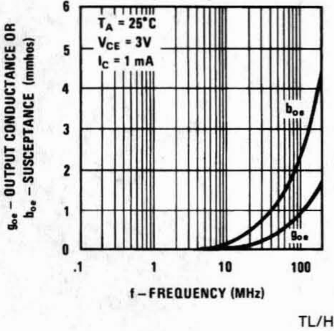

Typical Noise Figure vs Collector Current


Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current

TL/H/7950–5


Typical Forward Transfer Admittance vs Frequency

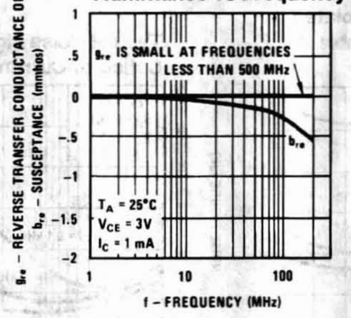

Typical Input Admittance vs Frequency


Typical Output Admittance vs Frequency

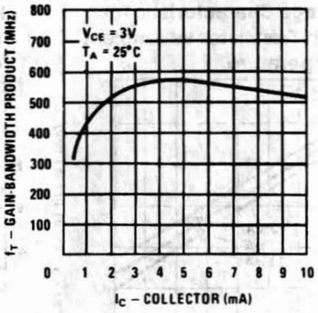
TL/H/7950–6

Typical Performance Characteristics (Continued)

Typical Reverse Transfer Admittance vs Frequency



Typical Gain-Bandwidth Product vs Collector Current



TL/H/7950–7

National Semiconductor

LM3146 High Voltage Transistor Array

General Description

The LM3146 consists of five high voltage general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the dc through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3146 is supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

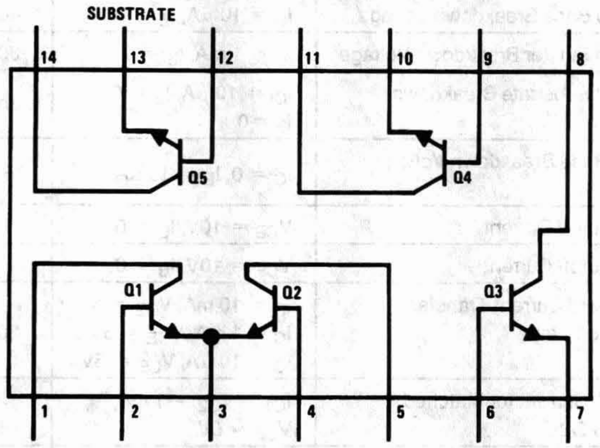
- High voltage matched pairs of transistors, V_{BE} matched ±5 mV, input offset current 2 μA max at $I_C = 1$ mA
- Five general purpose monolithic transistors
- Operation from dc to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from dc to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7959–1

Top View

Order Number LM3146M or LM3146N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LM3146	Units
Power Dissipation: Each transistor		
T_A = 25°C to 55°C	300	mW
$T_A > 55°C$	Derate at 6.67	mW/°C
Power Dissipation: Total Package		
T_A = 25°C	500	mW
$T_A > 25°C$	Derate at 6.67	mW/°C
Collector to Emitter Voltage, V_{CEO}	30	V
Collector to Base Voltage, V_{CBO}	40	V
Collector to Substrate Voltage, V_{CIO} (Note 1)	40	V
Emitter to Base Voltage, V_{EBO} (Note 2)	5	V
Collector to Current, I_C	50	mA
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C

Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics T_A = 25°C

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	$I_C = 10\ \mu A, I_E = 0$	40	72		V
$V_{(BR)CEO}$	Collector to Emitter Breakdown Voltage	$I_C = 1\ mA, I_B = 0$	30	56		V
$V_{(BR)CIO}$	Collector to Substrate Breakdown Voltage	$I_{CI} = 10\ \mu A, I_B = 0, I_E = 0$	40	72		V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage (Note 2)	$I_C = 0, I_E = 10\ \mu A$	5	7		V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 10V, I_E = 0$		0.002	100	nA
I_{CEO}	Collector Cutoff Current	$V_{CE} = 10V, I_B = 0$		(Note 3)	5	μA
h_{FE}	Static Forward Current Transfer Ratio (Static Beta)	$I_C = 10\ mA, V_{CE} = 5V$ $I_C = 1\ mA, V_{CE} = 5V$ $I_C = 10\ \mu A, V_{CE} = 5V$	30	85 100 90		
$I_{B1}-I_{B2}$	Input Offset Current for Matched Pair Q1 and Q2	$I_{C1} = I_{C2} = 1\ mA, V_{CE} = 5V$		0.3	2	μA
V_{BE}	Base to Emitter Voltage	$I_C = 1\ mA, V_{CE} = 3V$	0.63	0.73	0.83	V
$V_{BE1}-V_{BE2}$	Magnitude of Input Offset Voltage for Differential Pair	$V_{CE} = 5V, I_E = 1\ mA$		0.48	5	mV
$\Delta V_{BE}/\Delta T$	Temperature Coefficient of Base to Emitter Voltage	$V_{CE} = 5V, I_E = 1\ mA$		−1.9		mV/°C
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_C = 10\ mA, I_B = 1\ mA$		0.33		V
$\Delta V_{10}/\Delta T$	Temperature Coefficient of Input Offset Voltage	$I_C = 1\ mA, V_{CE} = 5V$		1.1		μV/°C

Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

Note 3: See curve.

AC Electrical Characteristics

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
NF	Low Frequency Noise Figure	f = 1 kHz, V_{CE} = 5V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
f_T	Gain Bandwidth Product	V_{CE} = 5V, I_C = 3 mA	300	500		MHz
C_{EB}	Emitter to Base Capacitance	V_{EB} = 5V, I_E = 0		0.70		pF
C_{CB}	Collector to Base Capacitance	V_{CB} = 5V, I_C = 0		0.37		pF
C_{CI}	Collector to Substrate Capacitance	V_{CI} = 5V, I_C = 0		2.2		pF
Low Frequency, Small Signal Equivalent Circuit Characteristics						
h_{fe}	Forward Current Transfer Ratio	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		100		
h_{ie}	Short Circuit Input Impedance	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		3.5		kΩ
h_{oe}	Open Circuit Output Impedance	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		15.6		μmho
h_{re}	Open Circuit Reverse Voltage Transfer Ratio	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		1.8×10^{-4}		
Admittance Characteristics						
Y_{fe}	Forward Transfer Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		mmho
Y_{ie}	Input Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.3 + j 0.04		mmho
Y_{oe}	Output Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.001 + j 0.03		mmho
Y_{re}	Reverse Transfer Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		(Note 3)		mmho

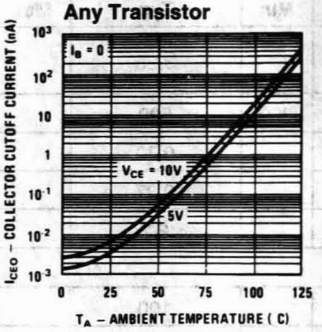
Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

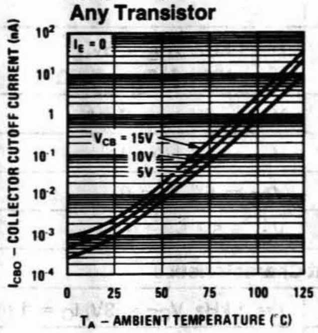
Note 3: See curve.

Typical Performance Characteristics

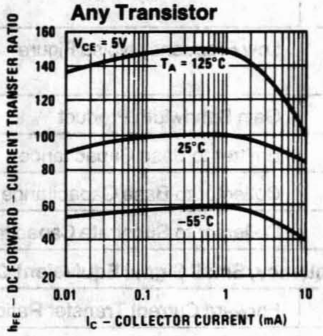
I_{CEO} vs T_A for Any Transistor



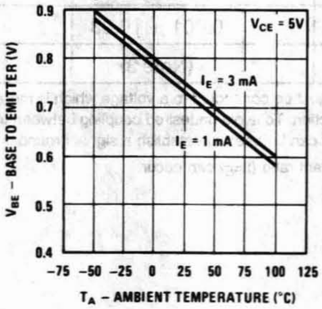
I_{CBO} vs T_A for Any Transistor



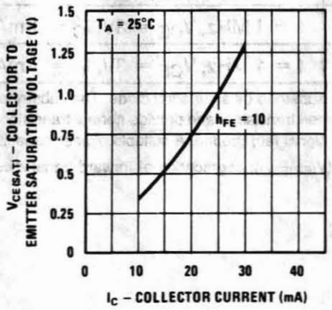
h_{FE} vs I_C for Any Transistor



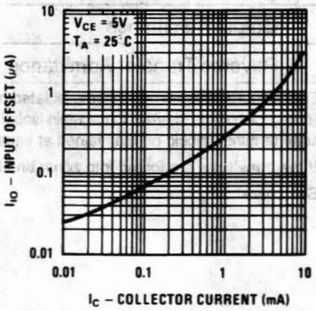
V_{BE} vs T_A for Any Transistor



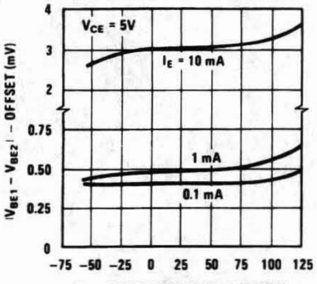
$V_{CE(SAT)}$ vs I_C for Any Transistor



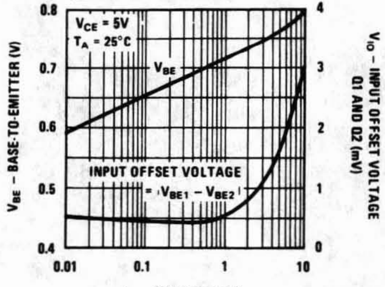
I_{IO} vs I_C (Q1 and Q2)



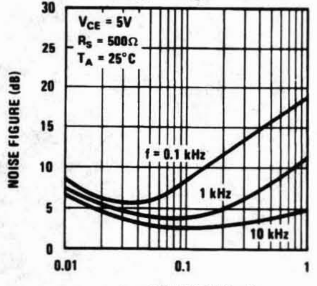
V_{IO} vs T_A for Q1 and Q2



V_{BE} and V_{IO} vs I_E for Q1 and Q2



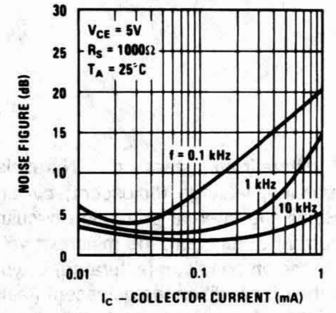
NF vs I_C @ $R_S = 500\Omega$



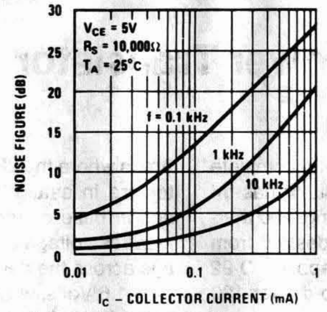
TL/H/7959–2

Typical Performance Characteristics (Continued)

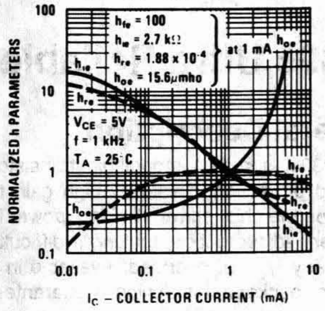
NF vs I_C @ R_S = 1 kΩ



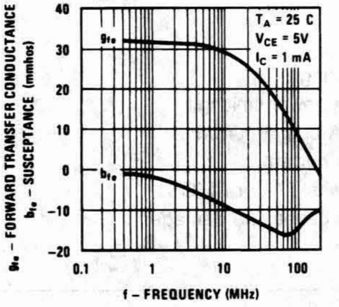
NF vs I_C = R_S = 10 kΩ



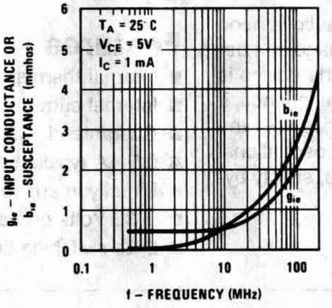
h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C



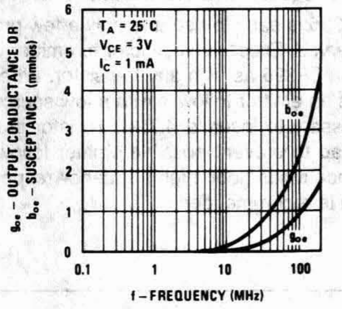
Y_{fe} vs f



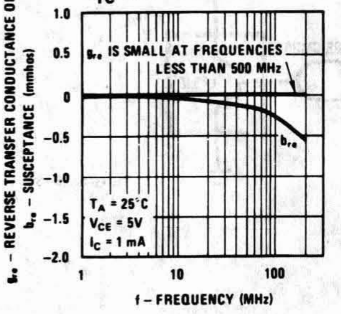
Y_{ie} vs f



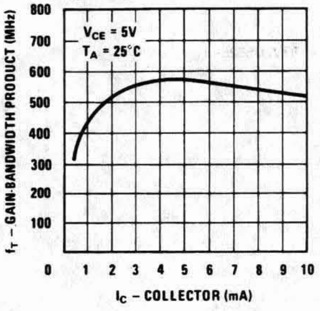
Y_{oe} vs f



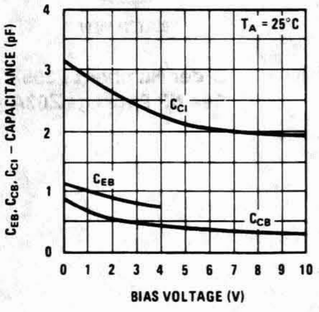
Y_{re} vs f



f_T vs I_C



C_{EB}, C_{CB}, C_{CI} vs Bias Voltage



TL/H/7959-3

National Semiconductor

LP395 Ultra Reliable Power Transistor

General Description

The LP395 is a fast monolithic transistor with complete overload protection. This very high gain transistor has included on the chip, current limiting, power limiting, and thermal overload protection, making it difficult to destroy from almost any type of overload. Available in an epoxy TO-92 transistor package this device is guaranteed to deliver 100 mA.

Thermal limiting at the chip level, a feature not available in discrete designs, provides comprehensive protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive die temperature.

The LP395 offers a significant increase in reliability while simplifying protection circuitry. It is especially attractive as a small incandescent lamp or solenoid driver because of its low drive requirements and blowout-proof design.

The LP395 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LP395 as with any transistor. When the device is used as an emitter follower with a low source impedance, it is necessary to insert a 4.7 kΩ resistor in series with the base lead to prevent possible emitter follower oscillations. Also since it has good high frequency response, supply bypassing is recommended.

Areas where the LP395 differs from a standard NPN transistor are in saturation voltage, leakage (quiescent) current and in base current. Since the internal protection circuitry requires voltage and current to function, the minimum voltage across the device in the on condition (saturated) is typically 1.6 Volts, while in the off condition the quiescent (leakage) current is typically 200 μA. Base current in this device flows out of the base lead, rather than into the base as is the case with conventional NPN transistors. Also the base can be driven positive up to 36 Volts without damage, but will draw current if driven negative more than 0.6 Volts. Additionally, if the base lead is left open, the LP395 will turn on.

The LP395 is a low-power version of the 1-Amp LM195/LM295/LM395 Ultra Reliable Power Transistor.

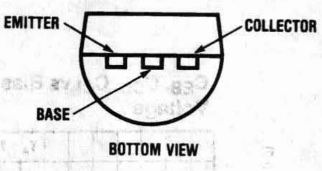
The LP395 is rated for operation over a −40°C to +125°C range.

Features

- Internal thermal limiting
- Internal current and power limiting
- Guaranteed 100 mA output current
- 0.5 μA typical base current
- Directly interfaces with TTL or CMOS
- +36 Volts on base causes no damage
- 2 μs switching time

Connection Diagram

TO-92 Package

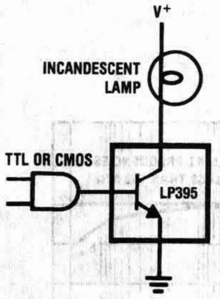


TL/H/5525-1

Order Number LP395Z
See NS Package Z03A

Typical Applications

Fully Protected Lamp Driver



TL/H/5525-3

Absolute Maximum Ratings

Collector to Emitter Voltage	36V	Collector Current Limit	Internally Limited
Collector to Base Voltage	36V	Power Dissipation	Internally Limited
Base to Emitter Voltage (Forward)	36V	Operating Temperature Range	−40°C to +125°C
Base to Emitter Voltage (Reverse)	10V	Storage Temperature Range	−65°C to +150°C
Base to Emitter Current (Reverse)	20 mA	Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics

Symbol	Parameter	Conditions	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limit)
V_{CE}	Collector to Emitter Operating Voltage	$0.5\text{ mA} \leq I_C \leq 100\text{ mA}$		36	**36** (Note 1)	V(Max)
I_{CL}	Collector Current Limit (Note 4)	$V_{BE} = 2V, V_{CE} = 36V$	45	25	**20**	mA(Min)
		$V_{BE} = 2V, V_{CE} = 15V$	90	60	**50**	mA(Min)
		$V_{BE} = 2V, 2V \leq V_{CE} \leq 6V$	130	100	**100**	mA(Min)
I_B	Base Current	$0 \leq I_C \leq 100\text{ mA}$	−0.3	−2.0	**−2.5**	μA(Max)
I_Q	Quiescent Current	$V_{BE} = 0V, 0 \leq V_{CE} \leq 36V$	0.24	0.50	**0.60**	mA(Max)
$V_{CE(SAT)}$	Saturation Voltage	$V_{BE} = 2V, I_C = 100\text{ mA}$	1.82	2.00	**2.10**	V(Max)
BV_{BE}	Base to Emitter Breakdown Voltage (Note 4)	$0 \leq V_{CE} \leq 36V, I_B = 2\ \mu A$		36	**36**	V(Min)
V_{BE}	Base to Emitter Voltage (Note 5)	$I_C = 5\text{ mA}$	0.69	0.79	**0.90**	V(Max)
		$I_C = 100\text{ mA}$ (Note 4)	1.02		**1.40**	V (Max)
t_S	Switching Time	$V_{CE} = 20V, R_L = 200\Omega$ $V_{BE} = 0V, +2V, 0V$	2			μs
θ_{JA}	Thermal Resistance Junction to Ambient	0.4″ leads soldered to printed circuit board	150		**180**	°C/W (Max)
		0.125″ leads soldered to printed circuit board	130		**160**	°C/W (Max)

Note 1: Parameters identified with **boldface type** apply at temp. extremes. All other numbers, unless noted apply at +25°C.

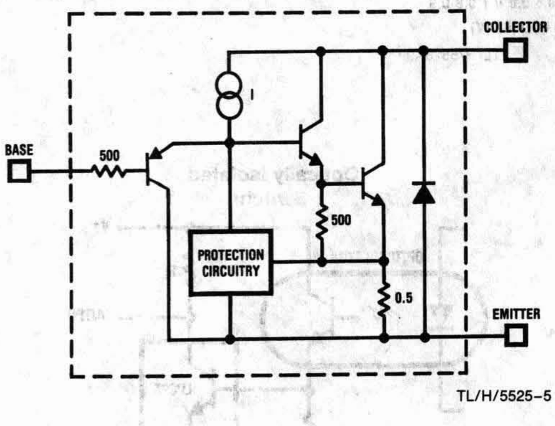
Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: These numbers apply for pulse testing with a low duty cycle.

Note 5: Base positive with respect to emitter.

Simplified Circuit

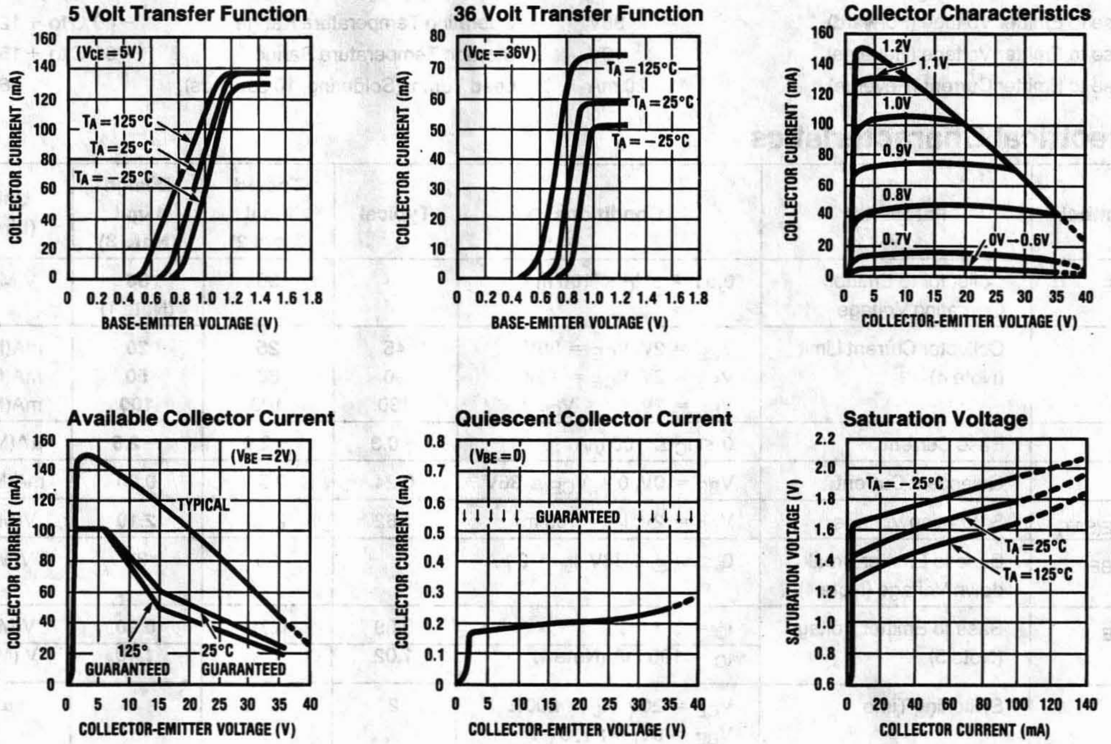


TL/H/5525–5

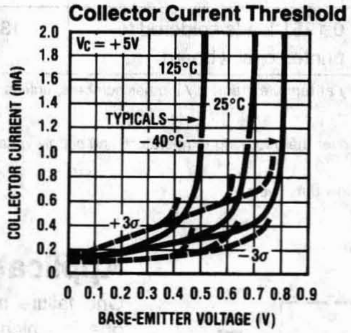
Applications Information

One failure mode incandescent lamps may experience is one in which the filament resistance drops to a very low value before it actually blows out. This is especially rough on most solid-state lamp drivers and in most cases a lamp failure of this type will also cause the lamp driver to fail. Because of its high gain and blowout-proof design, the LP395 is an ideal candidate for reliably driving small incandescent lamps. Additionally, the current limiting characteristics of the LP395 are advantageous as it serves to limit the cold filament inrush current, thus increasing lamp life.

Typical Performance Characteristics



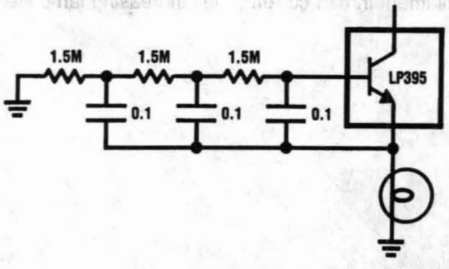
TL/H/5525–4



TL/H/5525–9

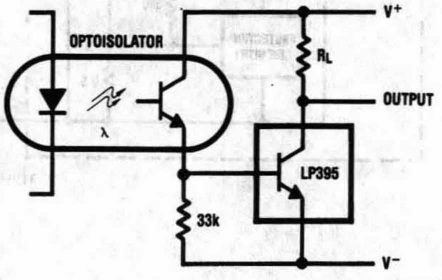
Typical Applications (Continued)

Lamp Flasher (Short Circuit Proof)


V+ ≥ 12V
1.5M
1.5M
1.5M
0.1
0.1
0.1
LP395

TL/H/5525–6

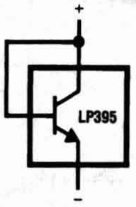
Optically Isolated Switch


OPTOISOLATOR
λ
V+
RL
OUTPUT
LP395
33k
V−

TL/H/5525–7

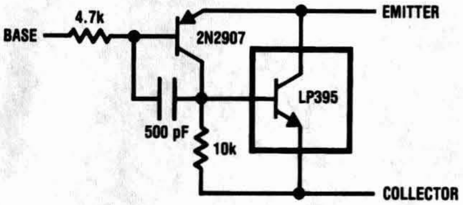
Typical Applications (Continued)

Two Terminal Current Limiter



TL/H/5525–8

Composite PNP


BASE
4.7k
2N2907
EMITTER
500 pF
10k
LP395
COLLECTOR

TL/H/5525–2

Section 6
Surface Mount

Section 6 Contents

Packing Considerations (Methods, Materials and Recycling) 6-3
Board Mount of Surface Mount Components 6-19
Recommended Soldering Profiles—Surface Mount 6-23
AN-450 Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability 6-24
Land Pattern Recommendations 6-35

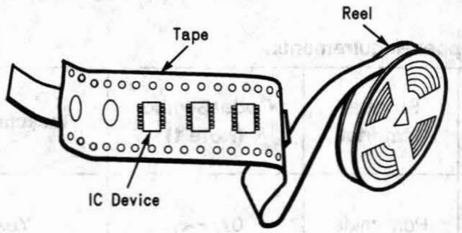
National *Semiconductor*

Packing Considerations (Methods, Materials and Recycling)

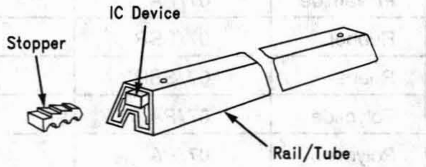
Transport Media

All NSC devices are prepared, inspected and packed to insure proper physical support and to protect during transport and shipment. All assembled devices are packed in one or more of the following container forms—immediate containers, intermediate containers and outer/shipping containers. An example of each container form is illustrated below.

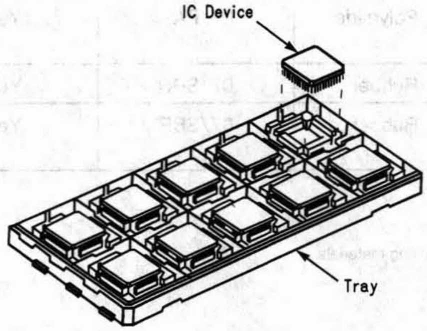
IMMEDIATE CONTAINER


Reel
Tape
IC Device

TL/P/11809-1

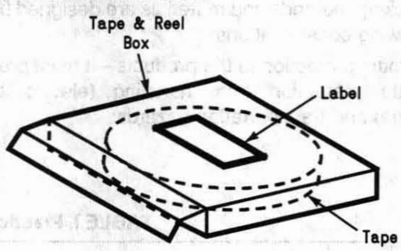

IC Device
Stopper
Rail/Tube

TL/P/11809-2

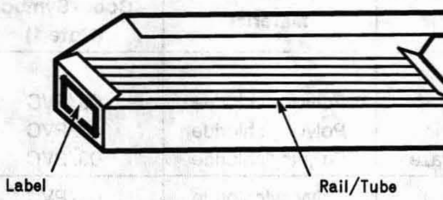

IC Device
Tray

TL/P/11809-3

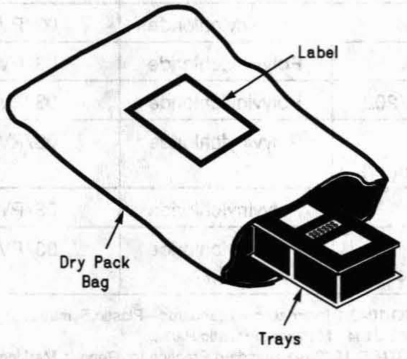
INTERMEDIATE CONTAINER


Tape & Reel
Box
Label
Tape

TL/P/11809-4

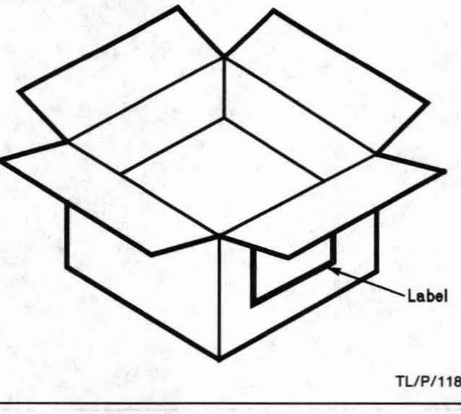

Label
Rail/Tube

TL/P/11809-5


Label
Dry Pack
Bag
Trays

TL/P/11809-6

OUTER/SHIPPING CONTAINER



TL/P/11809-7

Methods of immediate carrier packing include insertion of components into molded trays and rails/tubes, mounting of components onto tape and reel or placement in corrugated cartons. The immediate containers are then packed into intermediate containers (bags or boxes) which specify quantities of trays, rails/tubes or tape and reels. Outer/shipping containers are then filled or partially filled with intermediate containers to meet order quantity requirements and to further insure protection from transportation hazards. Additional dunnage filler material is required to fill voids within the intermediate and outer/shipping containers.

General Packing Requirements

NSC packing methods and materials are designed based on the following considerations:

- Optimum protection to the products—it must provide adequate protection from handling (electrostatic discharge) and transportation hazards;
- Ease of handling—it should be easy to assemble, load and unload products in and from it; and
- Impacts to the environment—it shall be reusable and recyclable.

Levels of Product Packing

IMMEDIATE CONTAINER

The first level of product packing is the immediate container. The immediate container type varies with the product or package being packed. In addition, the materials used in the immediate container depend on the fragility, size and profile of the product. The four types of immediate containers used by NSC are rails/tubes, trays, tape and reel, and corrugated and chipboard containers.

Rails/tubes are generally made of acrylic or polyvinyl chloride (PVC) plastics. The electrical characteristics of the material are altered by either intrinsically adding carbon fillers, and/or topically coating it with antistatic solution. Refer to Table I for rail/tube material and recyclabillty information.

TABLE I. Plastic Rail/Tube and Stopper Requirements

Package Type	Rail		Type	Stopper Material	Code/Symbol (Note 1)	Recyclability
	Material	Code/Symbol (Note 1)				
DIP's						
Plastic	Polyvinylchloride	03/PVC	Pin	Polyamide	07/PA	Yes
Ceramic	Polyvinylchloride	03/PVC	Pin	Polyamide	07/PA	Yes
Sidebraze	Polyvinylchloride	03/PVC	Pin	Polyamide	07/PA	Yes
PLCC	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes
TapePak	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes
Flatpack	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
Cerpack	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
TO-220/202	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
TO-5/8 (in Carrier)	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
SOP	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes
LCC 18L–44L	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes

Note 1: ISO 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D 1972–91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

Molded injection and vacuum formed trays can be either conductive or static dissipative. Molded injection trays are classified as either low-temperature or high-temperature depending on the material type. Vacuum formed trays are only used in ambient room temperature conditions. Refer to Table II for tray material and recyclability information.

TABLE II. Tray Requirements

Package Type	Class	Material	Tray		Binding Type
			Recyclability (Note 1)	Code/Symbol (Note 1)	
PQFP (All)	High Temperature	Polyethersulfone	Yes	07/PES	Wire Tie or Nylon Strap
	Low Temperature	Acrylonitrilebutadiene Styrene	Yes	07/ABS	Wire Tie or Nylon Strap
PGA, LDCC CERQUADs and LCC (48 leads–125 leads)	Low Temperature Only	ABS/PVC	Yes	07/ABS-PVC	Wire Tie
PPGA	Low Temperature Only	Polyarylsulfone	Yes	07/PAS	Wire Tie

Tape and reel is a multi-part immediate container system. The reel is made of either polystyrene (PS) material coated with antistatic solution or chipboard. The embossed or cavity tape is made of either PVC or PS material. The cover tape is made of polyester (PET) and polyethylene (PE) materials. Refer to Table III for tape and reel material and recyclability information.

TABLE III. Tape and Reel Requirements

Package Type	Reel		Cover Type		Carrier Tape		Recyclability (Note 1)
	Material	Code/ Symbol (Note 1)	Material	Code/ Symbol (Note 1)	Material	Code/ Symbol (Note 1)	
TO-92	Chipboard	Resy	N/A		Paper Tape		Yes
SOP-23	Polystyrene Chipboard	06/PS Resy	Polystyrene	06/PS	PVC	03/PVC	Yes
SOP, SSOP and PLCC	Polystyrene Polyethylene	06/PS	Polyester	07/PET-PE	PVC	03/PVC	Yes

Note 1: 150 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D 1972–91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

Corrugated containers are generally constructed with fibreboard facings and a fluted corrugated medium in between the facings. Chipboard containers are comprised of just one fibreboard facing. Facings and corrugated medium are kraft (brown) fibreboard, and generally single wall construction. Refer to Table IV for material and recyclability information.

TABLE IV. Fibreboard Container Requirements

Package Type	Pack Method		Container Type		Recyclability
	Material	Code/ Symbol (Note 1)	Immediate (IMM) Intermediate (INT) Outer or Shipping (SHP)		
TO-92/18, TO-46/5, TO-39, 220, TO-202/126, TO-237	Corrugated (E070 BOX)	Resy	IMM		Yes
All Products	Corrguated	Resy	INT and SHIP		Yes
All Products	3-Ply Paper (Padpak)	Resy	Dunnage		Yes
All Products PLCC	Plastic Bubble Sheet	04/PE	Dunnage		Yes

Note 1: ISO 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D1972-91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

INTERMEDIATE CONTAINERS

The second level of product packing is the intermediate container. Three types on intermediate containers are used by NSC. They are plastic bags, moisture barrier bags and corrugated cartons/boxes.

Two types of plastic bags are used and usage of each type depends on the product or package being packed. Conductive bags are made of polyvinylchloride plastic material. The electrical characteristics of the bag are altered by adding carbon fillers which make the bag black (opaque) in color. Conductive bags are used on products or packages that are packed in static dissipative (SD) rails/tubes. Static shielding bags are made of two layers of SD polyethylene sheets with a metallized film separating the sheets. Refer to Table V for material and recyclability information.

Moisture barrier bags are used on rail/tube, tape and reel, and tray packs for moisture sensitive products. NSC uses National Metallizing's Stratoguard™ 4.6.

TABLE V. Conductive and Static Shielding Bag Requirements

Package Type	Container Type	Material Type	Mat'l and Symbol (Note 1)	Mat'l Recyclability
All Prod. in Rails	Conductive Bag	Polyethlene	04/PE	Yes
TO-92/81, TO-46/5, TO-39/220, TO-202/126, TO-3/237	Static Shielding Bag	Polyethlene Alum. Laminant	N/A	No

TABLE VI. Drypack Bag Requirements

Package Type	Container Type	Material Type	Mat'l and Symbol (Note 1)	Mat'l Recyclability
TapePak PLCC (52-84L) PQFP	Drypack Bag	Stratoguard™ 4.6	N/A	No

Note 1: ISO 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D1972-91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials

Corrugated cartons/boxes are generally constructed with fibreboard facings and a fluted corrugated medium in between the facings. Facings and corrugated medium are kraft (brown) fibreboards, and are generally of single wall construction. Carton style varies with the product that it will contain. For example, packing of a rail/tube will require the use of a carton with a roll end from lock (REFL) design. Other products generally use the regular slotted container (RSC) box. Refer to Table IV for material and recyclability information.

OUTER/SHIPPING CONTAINERS

The third level of product packing is the outer/shipping container. The outer/shipping containers use by NSC are similar to the corrugated containers used for immediate and intermediate packaging, but are heavier in facing thickness. The style generally used is the regular slotted container (RSC) box and can be single, double or triple wall, depending on the total weight of products being transported or shipped. Refer to Table IV for material and recyclability information.

OTHER PACKING MATERIALS

Additional dunnage and void filler materials are required to fill voids within the intermediate and outer/shipping containers. Two types of dunnage/filler material are Padpack and bubble pack. Padpak is a machine processed, 3-ply kraft paper sheet dunnage system. Refer to Table IV for material and recyclability information.

Bubble pack is made of polyethylene plastic sheets with air pockets trapped in between the plastic layers and can be either static dissipative or conductive. Refer to Table IV for material and recyclability information.

Immediate Container Pack Methods

The following table identifies the primary immediate container pack method for all hermetic and plastic packages offered by National Semiconductor. A secondary immediate container pack method is identified where applicable.

Immediate Packing Method for Ceramic Packages

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Sidebrazed Dual-In-Line Package (SB)	D08C	Rail/Tube	35		
	D14D	Rail/Tube	25		
	D16C	Rail/Tube	20		
	D18A	Rail/Tube	20		
	D20A	Rail/Tube	18		
	D20B	Rail/Tube	18		
	D24C	Rail/Tube	15		
	D24H	Rail/Tube	15		
	D24K	Rail/Tube	15		
	D28D	Rail/Tube	13		
	D28G	Rail/Tube	13		
	D28H	Rail/Tube	13		
	D40C	Rail/Tube	9		
	D40J	Rail/Tube	9		
	D48A	Rail/Tube	7		
	D52A	Rail/Tube	7		
Ceramic Leadless Chip Carrier (LCC)	E20A	Rail/Tube	50		
	EA20B	Rail/Tube	50		
	E24B	Tray	25		
	E28A	Tray	28		
	EA028C	Tray	100		
	E32A	Rail/Tube	35		
	E32B	Rail/Tube	35		
	E32C	Rail/Tube	35		
	E40A	Rail/Tube	35		
	E44A	Rail/Tube	25		
	E48A	Tray	25		
	E68B	Tray	48		
	E68C	Tray	48		
	E84A	Tray	42		
	E84B	Tray	42		

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Quad J-Bend (CQJB)	EL28A	Tray	96		
	EL44A	Tray	80		
	EL44B	Tray	80		
	EL44C	Tray	80		
	EL52A	Tray	50		
	EL68A	Tray	44		
	EL68B	Tray	44		
	EL68C	Tray	44		
	EL84A	Tray	42		
Ceramic Quad Flatpack (CQFP)	EL28B	Rail	15		
	EL64A	Box	36		
	EL100A	Tray	12		
	EL116A	Tray	12		
	EL132B	Tray	20		
	EL132C	Tray	20		
	EL132D	Tray	20		
	EL164A	Tray	12		
	EL172B	Tray	12		
	EL172C	Tray	12		
Ceramic Flatpack	F10B	Carrier/Rail	19	Carrier/Box	200
	F14C	Carrier/Rail	19	Carrier/Box	200
	F16B	Carrier/Rail	19	Carrier/Box	200

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Dual-In-Line Package (Cerdip)	J08A	Rail/Tube	40		
	J14A	Rail/Tube	25		
	J16A	Rail/Tube	25		
	J18A	Rail/Tube	20		
	J20A	Rail/Tube	20		
	J22A	Rail/Tube	17		
	J24A	Rail/Tube	15		
	J24AQ	Rail/Tube	15		
	J24B-Q	Rail/Tube	15		
	J24CQ	Rail/Tube	15		
	J24E	Rail/Tube	16		
	J24F	Rail/Tube	15		
	J28A	Rail/Tube	12		
	J28AQ	Rail/Tube	12		
	J28B	Rail/Tube	12		
	J28BQ	Rail/Tube	12		
	J28CQ	Rail/Tube	13		
	J32B	Rail/Tube	11		
	J32AQ	Rail/Tube	11		
	J40A	Rail/Tube	9		
	J40AQ	Rail/Tube	9		
	J40BQ	Rail/Tube	9		
Ceramic Small Outline Package, Wide	MC16A	Rail/Tube	45		
	MC20A	Rail/Tube	36		
	MC20B	Rail/Tube	36		
	MC24A	Rail/Tube	30		
	MC28A	Rail/Tube	26		
	MC28B	Rail/Tube	26		

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Pin Grid Array (CPGA)	U44A	Tray	80		
	U68B	Tray	42		
	U68C	Tray	42		
	U68D	Tray	42		
	U68E	Tray	42		
	U75A	Tray	35		
	U84A	Tray	42		
	U84B	Tray	42		
	U84C	Tray	42		
	U99A	Tray	25		
	U100A	Tray	30		
	U109A	Tray	25		
	U120A	Tray	30		
	U120C	Tray	30		
	U124A	Tray	30		
	U132A	Tray	30		
	U132B	Tray	30		
	U144A	Tray	20		
	U156A	Tray	20		
	U156B	Tray	20		
	U169A	Tray	20		
	U173A	Tray	20		
	U175A	Tray	20		
	U180A	Tray	20		
	U223A	Tray	20		
	U224A	Tray	20		
	U257A	Tray	12		
	U259A	Tray	12		
	U299A	Tray	12		
	U301A	Tray	12		
	U303A	Tray	12		
	U323A	Tray	12		

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Cerpack	W10A	Carrier/Rail	19	Carrier/Box	200
	W14B	Carrier/Rail	19	Carrier/Box	200
	W14C	Carrier/Rail	19	Carrier/Box	200
	W16A	Carrier/Rail	19	Carrier/Box	200
	W20A	Carrier/Rail	19	Carrier/Box	200
	W24C	Carrier/Rail	15	Carrier/Box	80
	W28A	Carrier/Rail	15	Carrier/Box	80
	WA28D	Carrier/Rail	15	Carrier/Box	80
Cerquad	W24B	Rail/Tube	15		
	W56B	Tray	20		
	W64A	Tray	20		
	W68A	Tray	12		
	W84A	Tray	12		
Cerquad, EIAJ	WA80A	Tray	84		
	WA80AQ	Tray	84		
	W120A	Tray	12		
	W144A	Tray	12		
	W144B	Tray	12		
	W160A	Tray	12		
	W208A	Tray	12		

Immediate Packing Method for Metal Cans

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
TO-5	H06C	Tray	100	Carrier/Rail	18
	H08A	Tray	100	Carrier/Rail	18
	H08C	Tray	100	Carrier/Rail	18
	H10C	Tray	100	Cerrier/Rail	18
TO-18	H03C	Box	1800	Tray	100
TO-39	H03A	Tray	100	Carrier/Rail	18
	H03B	Tray	100	Carrier/Rail	18
	HA04E	Tray	100	Carrier/Rail	18
TO-46	H02A	Box	1800	Tray	100
	H03H	Box	1800	Tray	100
	H04A	Box	1800	Tray	100
	H04D	Box	1800	Tray	100
TO-52	H03J	Box	1800	Tray	100
TO-72	H04C	Box	1800	Tray	100

Immediate Packing Method for Plastic Packages

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Small Outline Transistor (SOT-23)	M03A	Tape and Reel	3000/ 10000	Bulk/Bag	500
	M03B	Tape and Reel	3000/ 10000	Bulk/Bag	500
Small Outline Package, JEDEC (SOP)	M08A	Rail/Tube	95	Tape and Reel	2500
	M14A	Rail/Tube	55	Tape and Reel	2500
	M14B	Rail/Tube	50	Tape and Reel	1000
	M16A	Rail/Tube	48	Tape and Reel	2500
	M16B	Rail/Tube	45	Tape and Reel	1000
	M20B	Rail/Tube	36	Tape and Reel	1000
	M24B	Rail/Tube	30	Tape and Reel	1000
	M28B	Rail/Tube	26	Tape and Reel	1000
Small Outline Package, EIAJ (SOP)	M14D	Rail/Tube	47	Tape and Reel	1000
	M16D	Rail/Tube	47	Tape and Reel	1000
	M20D	Rail/Tube	37	Tape and Reel	1000
Shrink Small Outline Package, JEDEC (SSOP)	MQA20	Rail/Tube	54	Tape and Reel	2500
	MQA24	Rail/Tube	54	Tape and Reel	2500
	MS48A	Rail/Tube	29	Tape and Reel	1000
	MS56A	Rail/Tube	25	Tape and Reel	1000
Shrink Small Outline Package, EIAJ (SSOP)	MSA20	Rail/Tube	65	Tape and Reel	1000
	MSA24	Rail/Tube	58	Tape and Reel	1000
	MS40A	Rail/Tube	34	Tape and Reel	1000
Very Small Outline Package (VSOP)	M40A	Rail/Tube	34	Tape and Reel	1000
Thin Small Outline Package, EIAJ (TSOP)	MBH32A	Tray	156		
Thin Shrink Small Outline Package, EIAJ (TSSOP)	MTA20	Tape and Reel	2500		

Immediate Packing Method for Plastic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Molded Dual-In-Line Package (MDIP)	N08E	Rail/Tube	40		
	N14A	Rail/Tube	25		
	N16A	Rail/Tube	20		
	N16E	Rail/Tube	25		
	N16G	Rail/Tube	20		
	N18A	Rail/Tube	20		
	N20A	Rail/Tube	18		
	N22A	Rail/Tube	15		
	N22B	Rail/Tube	15		
	N24A	Rail/Tube	15		
	N24C	Rail/Tube	15		
	N24D	Rail/Tube	15		
	N24E	Rail/Tube	15		
	N28B	Rail/Tube	13		
	N40A	Rail/Tube	9		
	N48A	Rail/Tube	7		
TO-202	P03A	Rail/Tube	45	Box	300
	P03B	Rail/Tube	45	Box	300
	P03C	Rail/Tube	45	Box	300
	P03D	Rail/Tube	45	Box	300
	P03E	Rail/Tube	45	Box	300
	P03F	Rail/Tube	45	Box	300
	P03G	Rail/Tube	45	Box	300
	P03H	Rail/Tube	45	Box	300
	P03J	Rail/Tube	45	Box	300
	P04A	Rail/Tube	45	Box	300
	P11A	Rail/Tube	15		
TO-237	R03A	Box	1500	Tape and Reel	2000
	R03B	Box	1500	Tape and Reel	2000
	R03C	Box	1500	Tape and Reel	2000
	R03D	Box	1500	Tape and Reel	2000
TO-226	RC03A	Box	1500	Tape and Reel	2000
	RC03B	Box	1500	Tape and Reel	2000
	RC03C	Box	1500	Tape and Reel	2000
	RC03D	Box	1500	Tape and Reel	2000

Immediate Packing Method for Plastic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
TO-220	TA02A	Rail/Tube	45	Box	300
	T02D	Rail/Tube	45	Box	300
	TA03A	Rail/Tube	45	Box	300
	TA03B	Rail/Tube	45	Box	300
	TA03D	Rail/Tube	45	Box	300
	T03A	Rail/Tube	45	Box	300
	T03B	Rail/Tube	45	Box	300
	T03D	Rail/Tube	45	Box	300
	T03F	Rail/Tube	45	Box	300
	T05A	Rail/Tube	45	Box	300
	T05B	Rail/Tube	45	Box	300
	T05C	Rail/Tube	45	Box	300
	T05D	Rail/Tube	45	Box	300
	T05E	Rail/Tube	45	Box	300
	T05F	Rail/Tube	45	Box	300
	TA05A	Rail/Tube	45	Box	300
	TA05B	Rail/Tube	45	Box	300
	TA11A	Rail/Tube	20	Box	300
	TA11B	Rail/Tube	20	Box	300
	TA11C	Rail/Tube	20	Box	300
	TA11D	Rail/Tube	20	Box	300
	TA11E	Rail/Tube	20	Box	300
	TA12A	Rail/Tube	20	Box	300
	TA15A	Rail/Tube	20	Box	300
	TA23A	Rail/Tube	15	Box	300
TapePak®	TP40A	Coinstack Tube	100	Flat Rail	25
Plastic Pin Grid Array (PPGA)	UP124A	Tray	30		
	UP159A	Tray	20		
	UP175A	Tray	20		
Plastic Leaded Chip Carrier (PLCC)	V20A	Rail/Tube	40	Tape and Reel	1000
	V28A	Rail/Tube	35	Tape and Reel	750
	V32A	Rail/Tube	30		
	V44A	Rail/Tube	25	Tape and Reel	500
	V52A	Rail/Tube	22	Tape and Reel	500
	V68A	Rail/Tube	18	Tape and Reel	250
	V84A	Rail/Tube	15	Tape and Reel	250

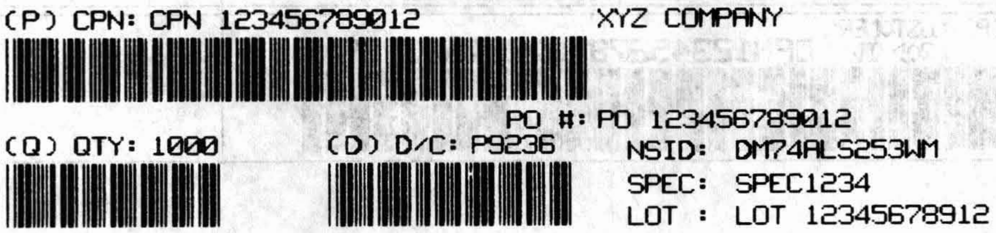
Immediate Packing Method for Plastic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Plastic Quad Flatpack (PQFP)	VEF44A	Tray	96		
	VBG48A	Tray	60		
	VHG80A	Tray	60		
	VJE80A	Tray	84		
	VCC80A	Tray	50/66		
	VCE100A	Tray	84		
	VLJ100A	Tray	50		
	VJG100A	Tray	60		
	VNG144A	Tray	60		
	VUL160A	Tray	24		
	VQL160A	Tray	24		
	VUW208A	Tray	24		
	VF132A	Tray	36		
	VF196A	Tray	21		
TO-92	Z03A	Box	1800	Tape and Reel	2000
	Z03B	Box	1800	Tape and Reel	2000
	Z03C	Box	1800	Tape and Reel	2000
	Z03D	Box	1800	Tape and Reel	2000
	Z03E	Box	1800	Tape and Reel	2000
	Z03G	Box	1800	Tape and Reel	2000
	Z03H	Box	1800	Tape and Reel	2000
	Z03J	Box	1800	Tape and Reel	2000

Labeling

National Semiconductor offers 3 standard bar code labels; reel and intermediate container labels for Tape and Reel; intermediate container label other than for Tape and Reel; and outer/shipping container labels. The tape and reel, and intermediate container labels are National's own format while the outer/shipping container label is based on the EIA-556-A label standard.

NSC Standard Tape and Reel Label



(P) CPN: CPN 123456789012 XYZ COMPANY

PO #: PO 123456789012

(Q) QTY: 1000 (D) D/C: P9236

NSID: DM74ALS253WM

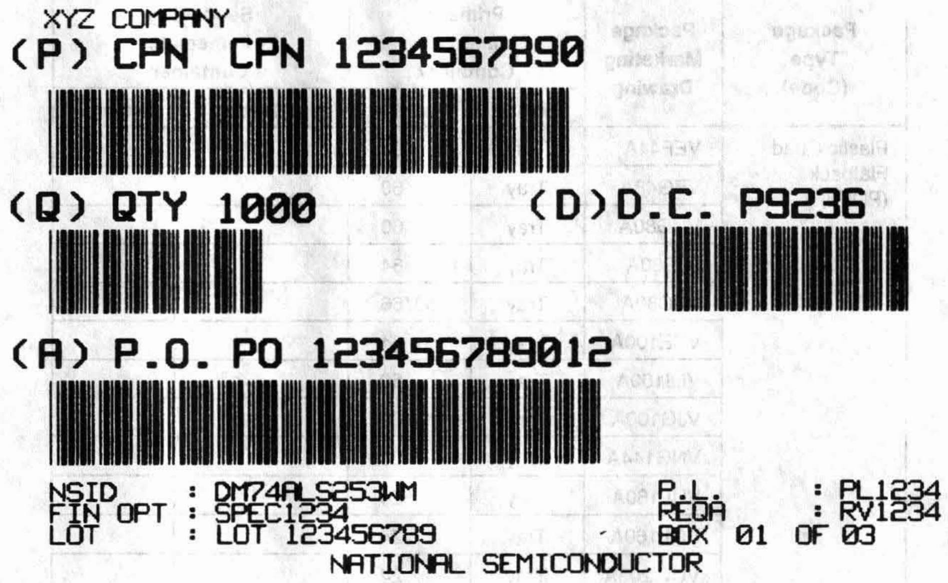
SPEC: SPEC1234

LOT : LOT 12345678912

TL/P/11809-8

This label is placed on the reel (immediate container) as well as on the intermediate box.

NSC Standard Intermediate Container Label



XYZ COMPANY

(P) CPN CPN 1234567890

(Q) QTY 1000

(D) D.C. P9236

(A) P.O. PO 123456789012

NSID : DM74ALS253WM

FIN OPT : SPEC1234

LOT : LOT 123456789

P.L. : PL1234

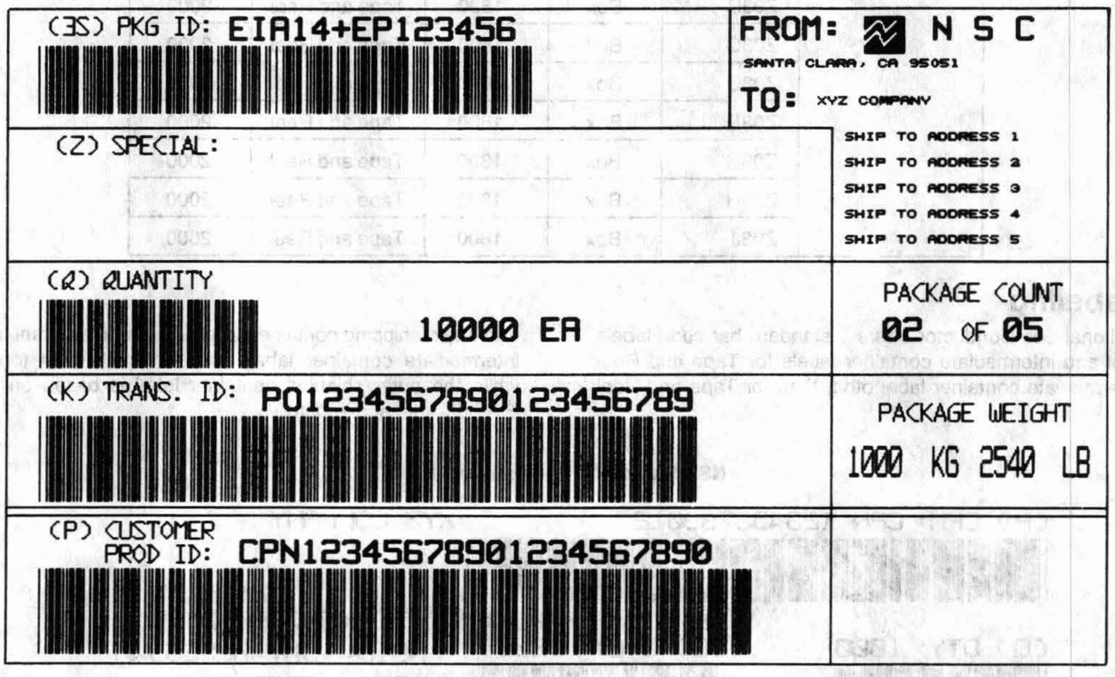
REQA : RV1234

BOX 01 OF 03

NATIONAL SEMICONDUCTOR

TL/P/11809–9

NSC Standard Outer/Shipping Container Label



(3S) PKG ID: EIA14+EP123456

FROM: N S C

SANTA CLARA, CA 95051

TO: XYZ COMPANY

SHIP TO ADDRESS 1

SHIP TO ADDRESS 2

SHIP TO ADDRESS 3

SHIP TO ADDRESS 4

SHIP TO ADDRESS 5

(Z) SPECIAL:

(Q) QUANTITY

10000 EA

PACKAGE COUNT

02 OF 05

(K) TRANS. ID: P01234567890123456789

PACKAGE WEIGHT

1000 KG 2540 LB

(P) CUSTOMER PROD ID: CPN12345678901234567890

TL/P/11809–10

Board Mount of Surface Mount Components

Abstract

In facing the challenges of "Surface Mount Technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this process. However, as the availability of all products as surface mount components is still limited, many have had to mix lead-inserted components with surface mount devices (SMD's). Furthermore, to take advantage of using both sides of the board, some surface mounted components are adhered to the bottom side of the board while the top side is reserved for the conventional lead-insert packages and fine pitch surface mount packages.

There are three surface mount processes in hi-volume use today:

1. **WAVE SOLDER;** the surface mounted components are adhered to the bottom side of the board while the top side is reserved for the lead-inserted packages. The surface mount components are subjected to severe thermal stress when they are immersed into the molten solder.
2. **INFRA-RED** mass reflow; the surface mount components are placed on the solder paste which has been applied to the board, the solder joints are formed when the board is passed thru the reflow media. The surface mount devices are subjected to a controlled thermal environment.
3. **VAPOR PHASE** mass reflow; the surface mount components are placed on the solder paste which has been applied to the board, tbe solder joints are formed when the board is passed thru the reflow media. The surface mount devices are subjected to a controlled thermal environment, more severe than Infra-red but much less than wavesolder.

A discussion of the effect of these processes on the reliability of plastic semiconductor packages follows.

Role of Wave Soldering in Application of SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave soldering machine. The reasons being:

Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.

Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.

Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

PW Board Assembly Procedures

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

a) Whether to mount ICs on one or both sides of the board.

b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or a combination of two or more methods.

The various processes that may be employed are:

A) WAVE SOLDER BEFORE VAPOR/IR REFLOW SOLDER

1. Components on the same side of PW Board. Lead insert standard DIPS onto PW Board Wave solder (conventional). Wash and lead trim. Dispense solder paste on SEM pads. Pick and place SMDs onto PW Board. Bake Vapor phase/IR reflow. Clean.
2. Components on opposite side of PW Board. Lead insert standard DIPs onto PW Board Wave Solder (conventional). Clean and lead trim. Invert PW Board. Dispense drop of adhesive on SMD sites (optional for smaller components). Pick and place SMDs onto board. Bake/Cure. Invert board to rest on raised fixture. Vapor/IR reflow soldering. Clean.

B) VAPOR/IR REFLOW SOLDER THEN WAVE SOLDER

1. Components on the same side of PW Board. Solder paste screened on SMD side of Printed Wire Board. Pick and place SMDs. Bake Vapor/IR reflow. Lead insert on same side as SMD's. Wave solder. Clean and trim underside of PCB.

C) VAPOR/IR REFLOW ONLY

1. Components on the same side of PW Board Trim and form standard DIPs in "gull wing" configuration. Solder paste screened on PW Board. Pick and place SMDs and DIPs. Bake Vapor/IR reflow. Clean.
2. Components on opposite sides of PW Board. Solder paste screened on SMD-side of Printed Wire Board. Adhesive dispensed at central location of each component. Pick and place SMDs. Bake. Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads. Lead insert DIPs. Vapor/IR reflow. Clean and lead trim.

PW Board Assembly Procedures

(Continued)

D) WAVE SOLDERING ONLY

1. Components on opposite sides of PW board. Adhesive dispense on SMD side of PW Board. Pick and place SMDs. Cure adhesive. Lead insert top side with DIPs. Wave solder with SMDs down and into solder bath. Clean and lead trim.

All of the above assembly procedures can be divided into three categories for IC. Reliability considerations:

1) Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
2) Components are subjected to only a vapor phase/IR heat cycle.
3) Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

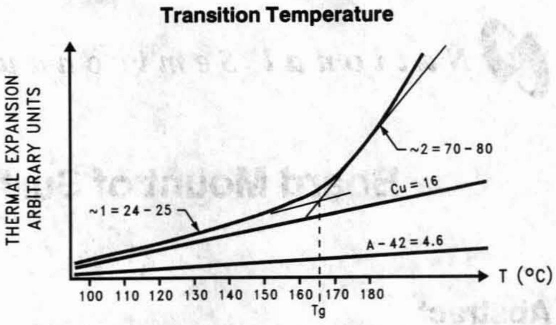
Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a "pallet" where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

Thermal Characteristics of Molded Integrated Circuits

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1.* Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on leadframes, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of leadframe material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal leadframe in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the epoxy-metal interface. However, If the package is subjected to temperature above its glass-transition temperature, the epoxy will expand much faster than the metal and the probability of separation is greatly increased.



TL/P/11828–1

FIGURE 1. Thermal Expansion and Glass

Conventional Wave Soldering

Most wave soldering operations occur at temperatures between 240°C–260°C. Conventional epoxies for encapsulation have glass-transition temperatures between 140°C–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

1. The PW board has a certain amount of heat-sink effort and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120°C–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.
2) In conventional soldering, only the tip of each lead in DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

Effect on Package Performance by Epoxy-Metal Separation

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metalization over time and premature failure of the device in the field.

Vapor Phase/IR Reflow Soldering

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Maximum operating temperatures are 219°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec–60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-leadframe interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

Bias Moisture Test

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a steam chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to faiL

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and 85% relative humidity. One cycle of approximately 100 hours has been shown to be equivalent to 2,000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2,000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

Test Results

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

TABLE IV. Vapor Phase vs. Wave Solder

1. Vapor phase (60 sec. exposure @ 217°C)
   = 9 failures/1723 samples
   = 0.5% (average over 32 sample lots)
2. Wave solder (2 sec total immersion @ 260°C)
   = 16 failures/1201 samples
   = 1.3% (average over 27 sample lots)

Package: SO-14 lead
Test: Bias moisture test 85% R.H.
85°C for 2,000 hours
Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4,000 hours 85/85 test. Results were compared for packages by themselves against packages which were surface-mounted onto a FR-4 printed wire board.

TABLE V. Summary of Wave Solder Results

	Unmounted	Mounted
Control/Vapor Phase 15 sec @ 215°C	0/114	0/84
Solder Dip 4 Sec @ 260°C	2/144 (1.4%)	0/85
Solder Dip 4 Sec @ 260°C	—	0/83
Solder Dip 6 Sec @ 260°C	13/248 (5.2%)	1/76 (1.3%)
Solder Dip 10 Sec @ 260°C	14/127 (11.0%)	3/79 (3.8%)
Package: SO-14 lead Device: LM324M		

Since the package is of very small mass and experiences a rather sharp thermal shock followed by stresses created by the mismatch in expansion, the results show the packages being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6,000 hours in an 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

TABLE VI. U.S. Manufacturing Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Environment)

Package SO-8	Vapor Phase 30 sec	Wave Solder 2 sec	Wave Solder 4 sec	Wave Solder 6 sec	Wave Solder 10 sec
Manuf A	8/30*	1/30*	0/30	12/30*	16/30*
Manuf B	2/30*	8/30*	2/30*	22/30*	20/30*
Manuf C	0/30	0/29	0/29	0/30	0/30
Manuf D	1/30*	12/30*	14/30*	2/30*	
Manuf E	1/30**	0/30	0/30	0/30	
Manuf F	0/30	0/30	0/30	0/30	
NSC	0/30	0/30	0/30	0/30	

*Corrosion failures

**No Visual Defects-Non-corrosion failues

Test Accelerated Bias Moisture Test: 85% R.H./85°C. 6,000 equivalent hours

Summary

Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low T_g compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of the package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

National Semiconductor

Recommended Soldering Profiles—Surface Mount

		Wave Solder	IR Profile	Vapor Phase
Ramp Up °C/sec	Maximum	6°C/sec	4°C/sec	24°C/sec
	Recommended	**4°C/sec***	**2°C/sec***	**2°C/sec**
	Minimum	**	**	**
ΔT	Maximum	135°C	N/A	N/A
	Recommended	**120°C**	**N/A**	**N/A**
	Minimum	110°C	N/A	N/A
Dwell Time ≥ 183°C	Maximum	N/A	85 seconds	85 seconds
	Recommended	**N/A**	**75 seconds***	**75 seconds***
	Minimum	N/A	30 seconds**	**
Solder Temperature	Maximum	260°C	240°C***	219°C
	Recommended	**240°C**	**215°C***	**215°C***
	Minimum	**	**	**
Dwell Time @ Max.	Maximum	4 seconds	10 seconds	75
	Recommended	**3 seconds**	**5 seconds**	**70 seconds**
	Minimum	**	1 second	**
Ramp Down °C/sec	Maximum	No Information	4°C/sec	4°C/sec
	Recommended	**4°C/sec**	**2°C/sec**	**2°C/sec**
	Minimum	No Information	**	**

Note: Temperature in degrees celcius. N/A = Not Applicable.

ΔT = The temperature differential between the final preheat stage and the soldering stage. Temperature measured at the component lead area.

***Will vary depending on board density, geometry, and package type.**

****Will vary depending on package types, and board density.**

*****For plastic packages; ceramic packages maximum may be 250°C.**

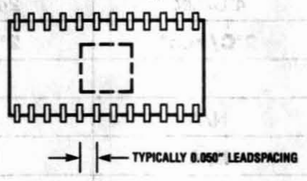
Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliability

National Semiconductor
Application Note 450
Josip Huljev
W. K. Boey

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

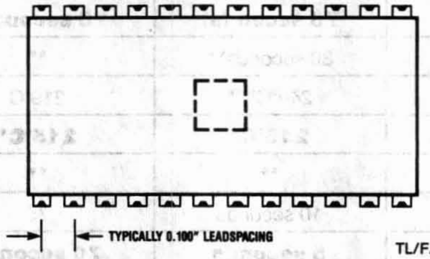
COMPONENT SIZE COMPARISON

S.O. Package



TL/F/8766–1

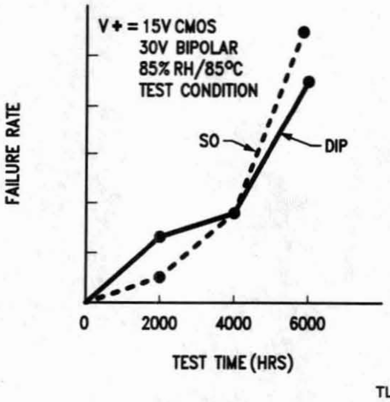
Standard DIP Package



TL/F/8766–2

Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.



TL/F/8766–3

FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

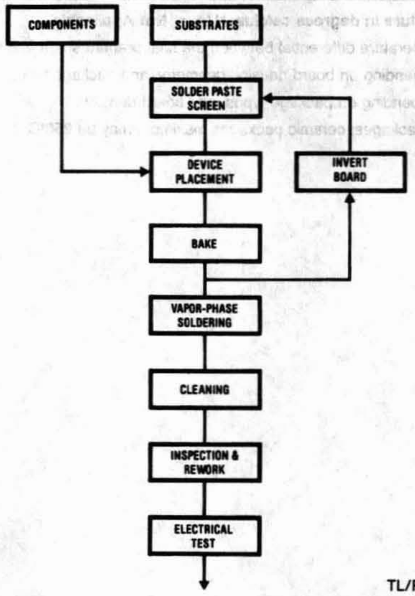
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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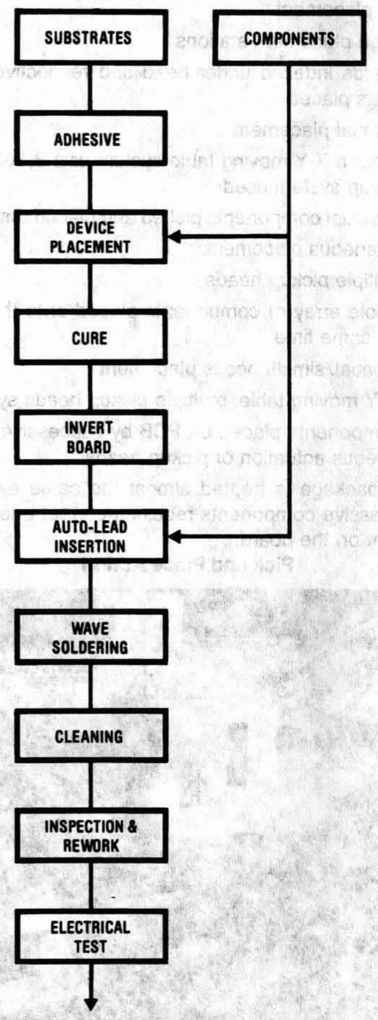
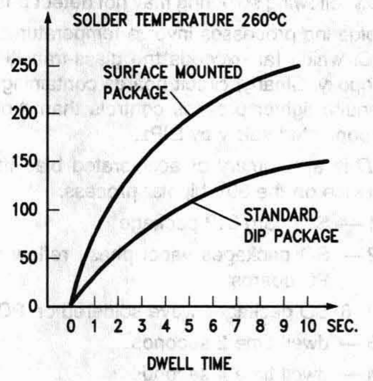
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



TL/F/8766–5

Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).



TL/F/8766–6

FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

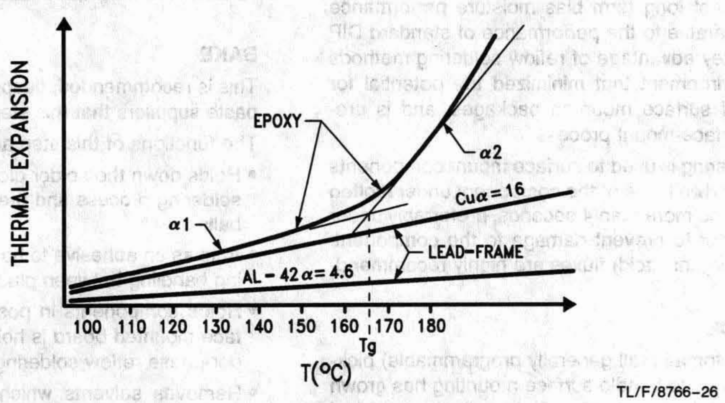


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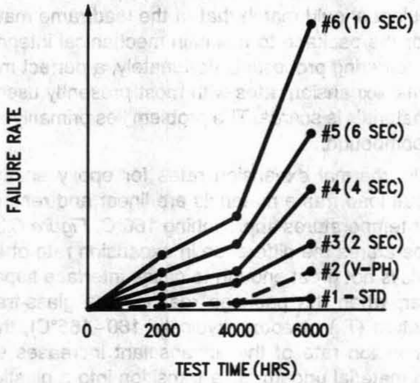
FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package
Group 2 — SO packages vapor-phase reflow soldered on PC boards
Group 3–6 SO packages wave soldered on PC boards
Group 3 — dwell time 2 seconds
4 — dwell time 4 seconds
5 — dwell time 6 seconds
6 — dwell time 10 seconds



TL/F/8766–7

FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement
  - Fixed placement stations
  - Boards indexed under head and respective components placed

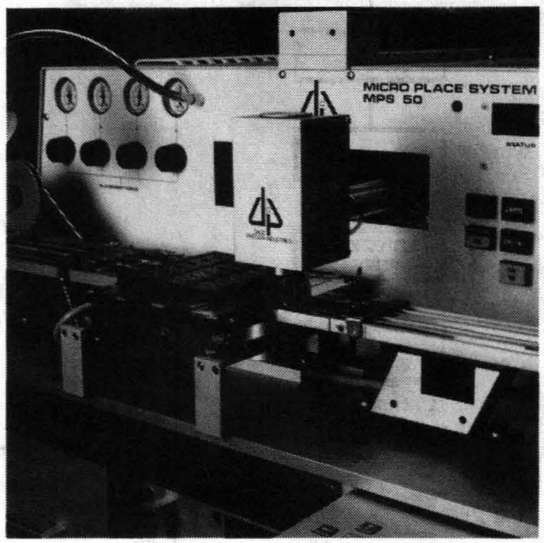
(b) Sequential placement
  - Either a X-Y moving table system or a θ, X-Y moving pickup system used
  - Individual components picked and placed onto boards

(c) Simultaneous placement
  - Multiple pickup heads
  - Whole array of components placed onto the PCB at the same time

(d) Sequential/simultaneous placement
  - X–Y moving table, multiple pickup heads system
  - Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



TL/F/8766–8

BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

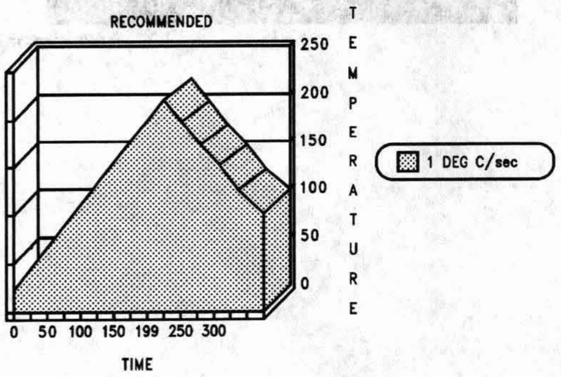
A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

INFRARED REFLOW SOLDERING

Use of an infrared furnace is currently the most popular method to automate mass reflow, the heating is promoted by use of IR lamps or panels. Early objections to this method were that certain materials may heat up at different rates under IR radiation and could result in damage to those components (usually sockets and connectors). This has been minimized by using far-infrared (non-focused) systems and convected air.

Infrared Profile



TL/F/8766–27

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

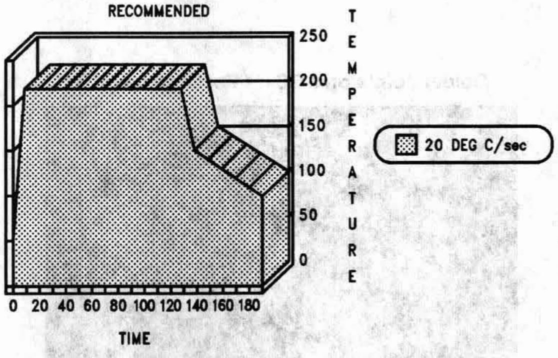
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

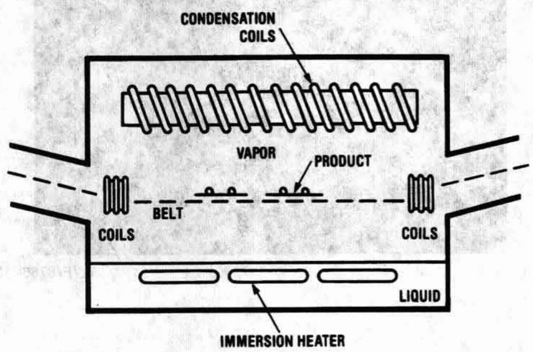
Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

Vapor-Phase Profile



TL/F/8766–28

In-Line Conveyorized Vapor-Phase Soldering



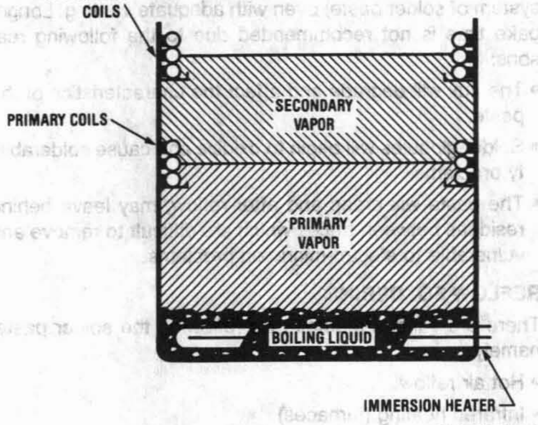
TL/F/8766–9

The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

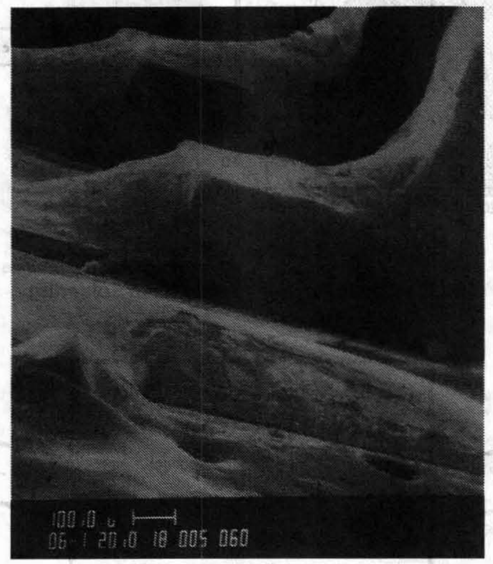
TL/F/8766-10

Batch-Fed Production Vapor-Phase Soldering Unit


SECONDARY COILS
PRIMARY COILS
SECONDARY VAPOR
PRIMARY VAPOR
BOILING LIQUID
IMMERSION HEATER

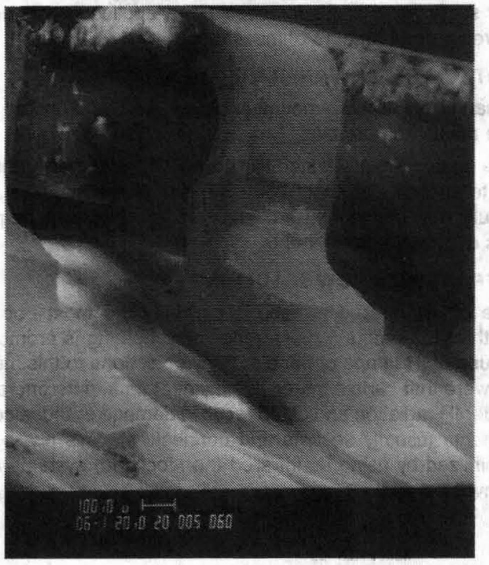
TL/F/8766-11

Solder Joints on a SO-14 Package on PCB


100.0 u
06-1 20.0 18 005 060

TL/F/8766-12

Solder Joints on a SO-14 Package on PCB


100.0 u
06-1 20.0 20 005 060

TL/F/8766-13

PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050" lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005" usually used to achieve a solder paste thickness (wet) of about 0.008" typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed ⅛", to avoid damage to screens and minimize distortion.

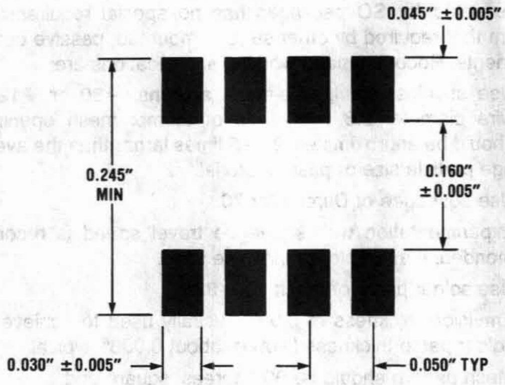
SOLDER PASTE

Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see following photographs). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.
- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

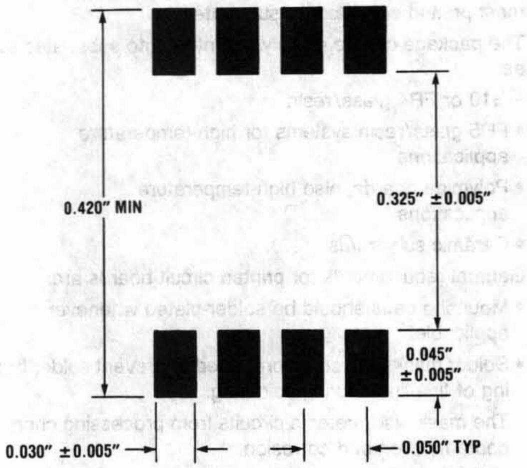
RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16


0.045" ±0.005"
0.245" MIN
0.160" ±0.005"
0.030" ±0.005"
0.050" TYP

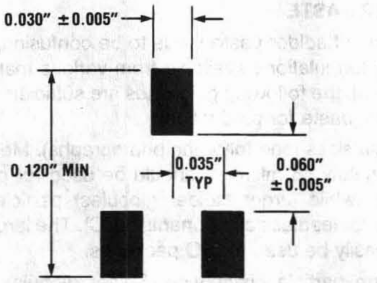
TL/F/8766-14

SO-16L, SO-20


0.420" MIN
0.325" ±0.005"
0.045" ±0.005"
0.030" ±0.005"
0.050" TYP

TL/F/8766-15

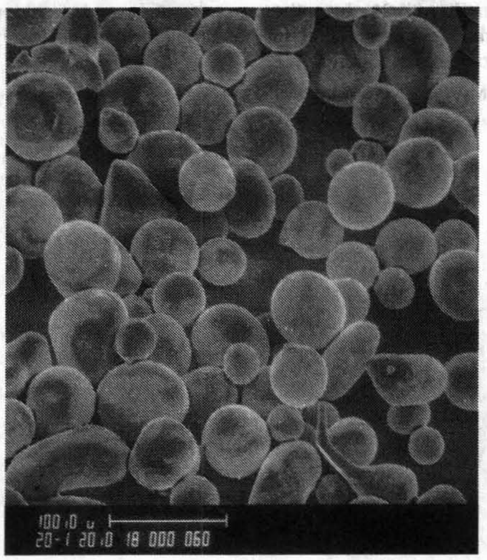
SOT-23


0.030" ±0.005"
0.120" MIN
0.035" TYP
0.060" ±0.005"

TL/F/8766-16

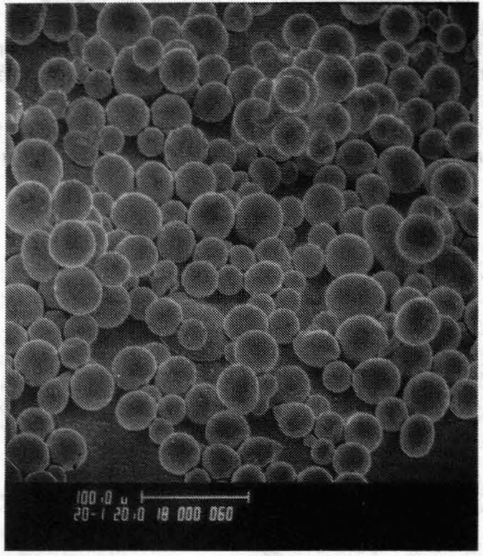
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)


100.0 u
20-1 20.0 18 000 060

TL/F/8766-17

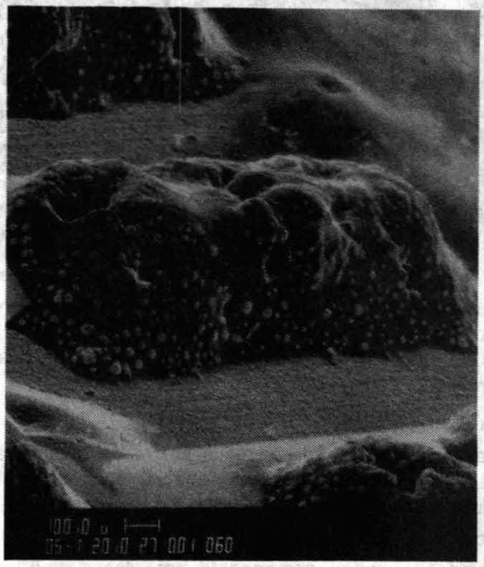
200 × Kester (63/37)


100.0 u
20-1 20.0 18 000 060

TL/F/8766-18

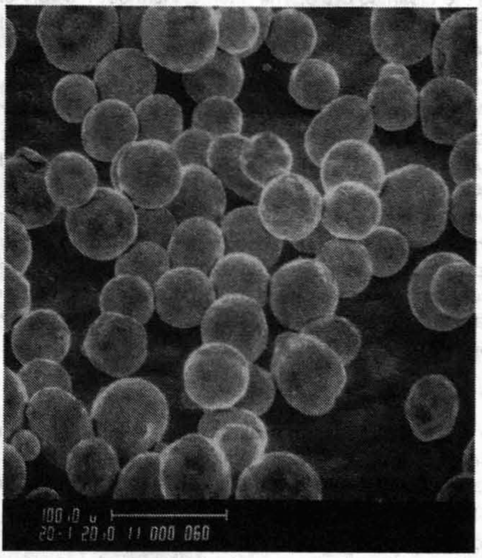
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads


100.0 u
05-1 20.0 21 001 060

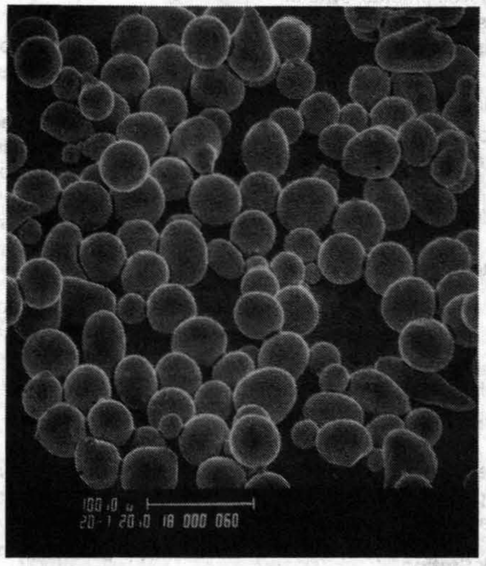
TL/F/8766–19

200 × Fry Metal (63/37)


100.0 u
20-1 20.0 11 000 060

TL/F/8766–20

200 ESL (63/37)


100.0 u
20-1 20.0 18 000 060

TL/F/8766–21

CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. CFC solvents are being phased out as they are hazardous to the environment. Other approaches to cleaning are commercially available and should be investigated on an individual basis considering local and government environmental rules.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

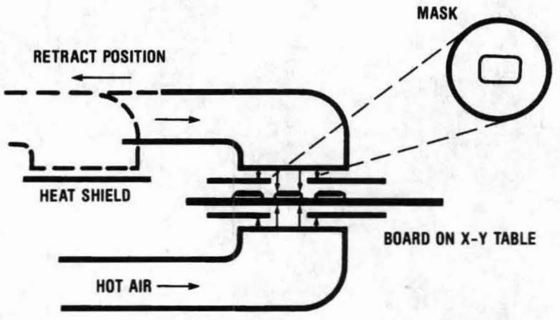
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

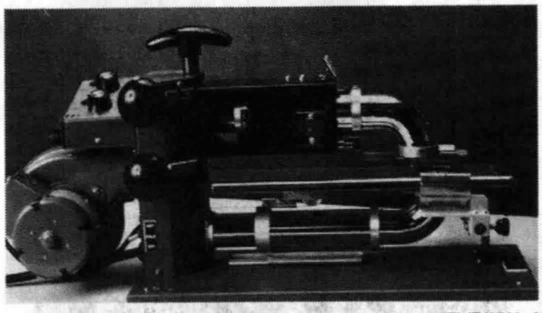
When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



TL/F/8766-22

Hot-Air Rework Machine



TL/F/8766-23

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

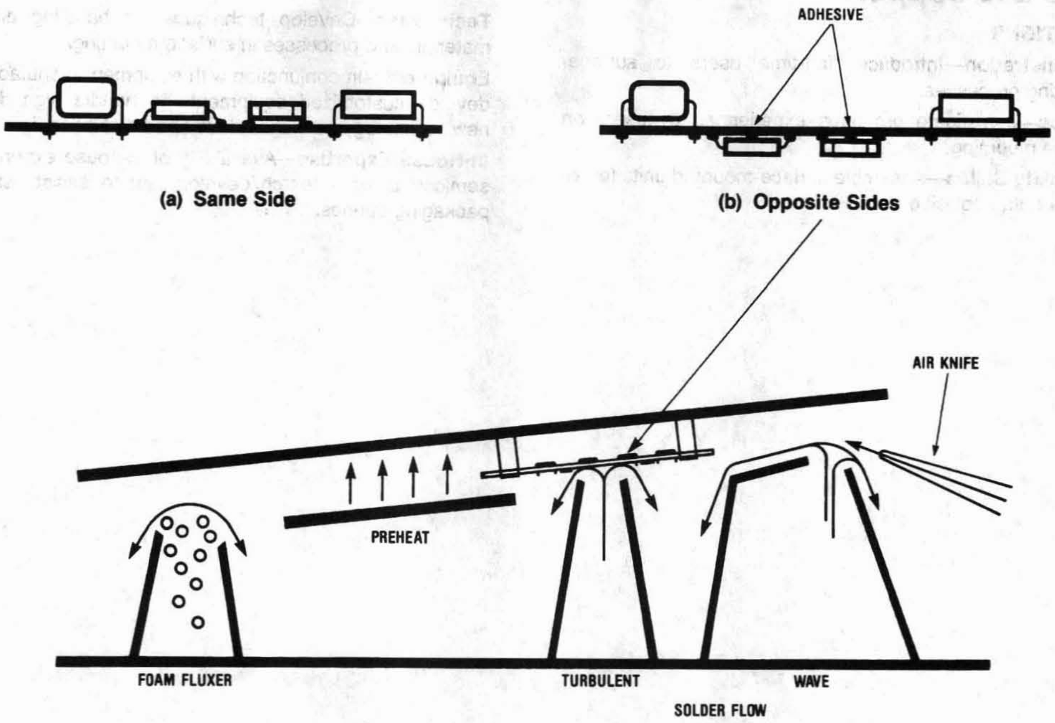
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



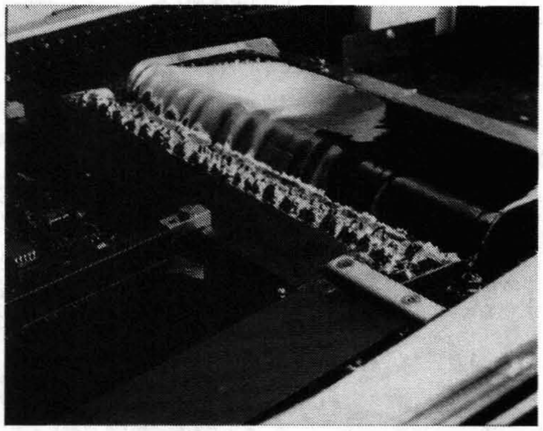
TL/F/8766–24

A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



TL/F/8766–25

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

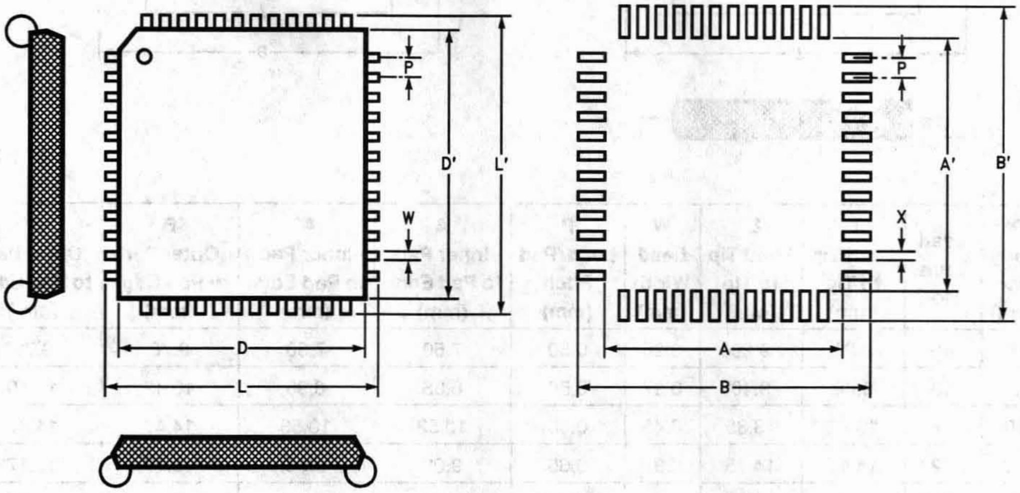
National Semiconductor

Land Pattern Recommendations

The following land pattern recommendations are provided as guidelines for board layout and assembly purposes. These recommendations cover the following National Semiconductor packages: PLCC, PQFP, SOP, SSOP and TSOP.

For SOT-23 (5-Lead) and TO-263 (3- or 5-Lead) packages, refer to land patterns shown in the Physical Dimensions for MA05A and TS3B or TS5B packages, respectively.

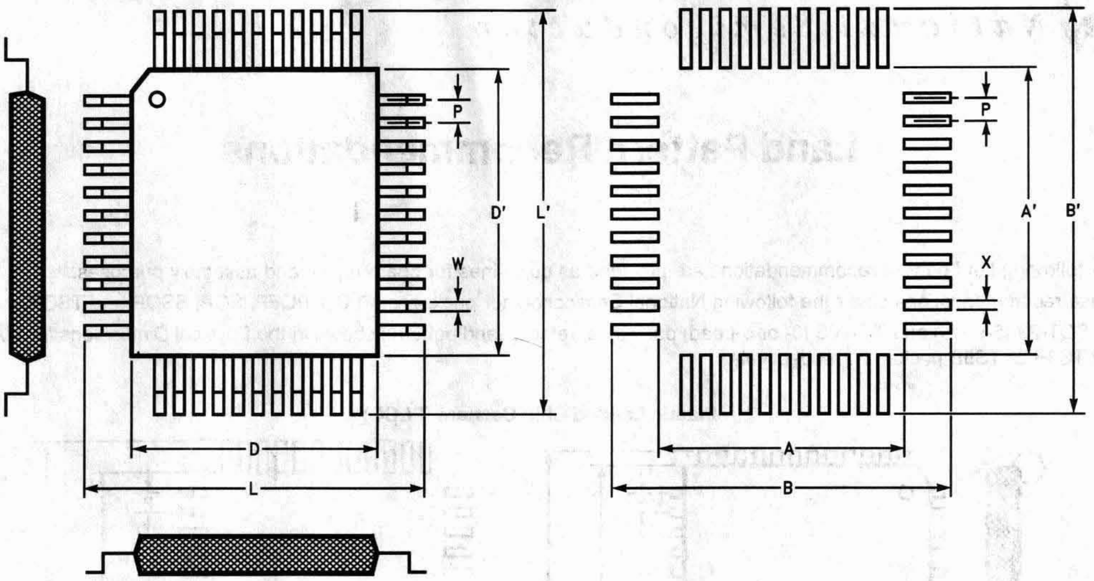
Plastic Leaded Chip Carriers (PLCC)



TL/P/11811-1

D Body Size (mm)	D′ Body Size (mm)	Lead Count No.	L Lead Tip to Tip (mm)	L′ Lead Tip to Tip (mm)	W Lead Width (mm)	P Lead/Pad Pitch (mm)	A Inner Pad to Pad Edge (mm)	A′ Inner Pad to Pad Edge (mm)	B Outer Pad to Pad Edge (mm)	B′ Outer Pad to Pad Edge (mm)	X Land Width (mm)
8.89	8.89	20	10.03	10.03	0.53	1.27	6.73	6.73	10.80	10.80	0.63
11.43	11.43	28	12.57	12.57	0.53	1.27	9.27	9.27	13.34	13.34	0.63
11.43	14.05	32	12.57	15.11	0.53	1.27	9.27	12.00	13.34	16.00	0.63
16.51	16.51	44	17.65	17.65	0.53	1.27	14.35	14.35	18.42	18.42	0.63
19.05	19.05	52	20.19	20.19	0.53	1.27	16.89	16.89	20.96	20.96	0.63
24.13	24.13	68	25.27	25.27	0.53	1.27	21.97	21.97	26.04	26.04	0.63
29.21	29.21	84	30.35	30.35	0.53	1.27	27.05	27.05	31.12	31.12	0.63

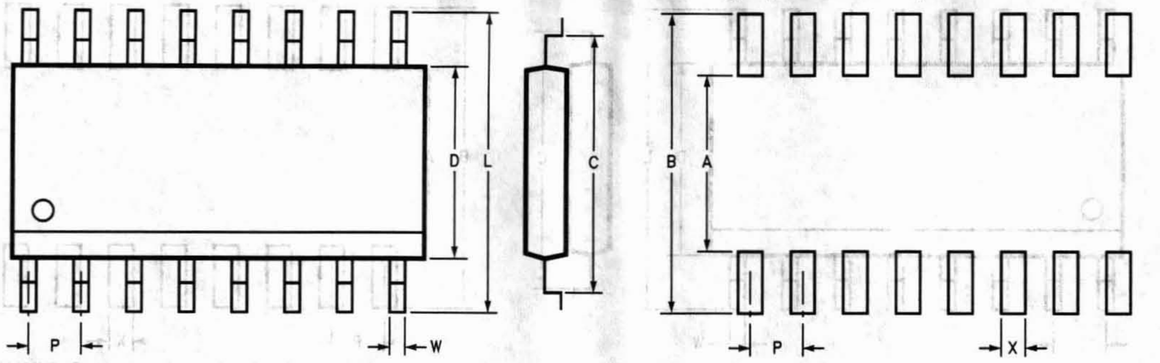
Plastic Quad Flat Packages (PQFP)



TL/P/11811–2

D Body Size (mm)	D′ Body Size (mm)	Lead Count No.	L Lead Tip to Tip (mm)	L′ Lead Tip to Tip (mm)	W Lead Width (mm)	P Lead/Pad Pitch (mm)	A Inner Pad to Pad Edge (mm)	A′ Inner Pad to Pad Edge (mm)	B Outer Pad to Pad Edge (mm)	B′ Outer Pad to Pad Edge (mm)	X Land Width (mm)
7	7	40	9.29	9.29	0.26	0.50	7.50	7.50	9.78	9.78	0.30
7	7	48	9.40	9.40	0.27	0.50	6.88	6.90	10.42	10.40	0.32
10	10	44	13.35	13.35	0.45	0.80	10.53	10.53	14.47	14.47	0.55
10	10	52	14.15	14.15	0.38	0.65	9.08	9.08	15.17	15.17	0.43
12	12	64	14.00	14.00	0.38	0.65	11.48	11.48	15.02	15.02	0.43
14	14	80	18.15	18.15	0.38	0.65	13.08	13.08	19.17	19.17	0.43
14	20	80	17.80	23.80	0.35	0.80	13.50	19.50	18.50	24.50	0.40
14	14	100	17.45	17.45	0.30	0.50	13.08	13.08	18.47	18.47	0.35
14	20	100	17.80	23.80	0.30	0.65	13.50	19.50	18.50	24.50	0.35
20	20	100	24.30	18.30	0.40	0.65	21.28	15.28	25.32	19.32	0.45
24	24	132	24.21	24.21	0.30	0.64	21.67	21.67	25.23	25.23	0.40
28	28	120	32.15	32.15	0.45	0.80	27.88	27.88	33.17	33.17	0.55
28	28	128	31.45	31.45	0.45	0.80	28.03	28.03	32.47	32.47	0.55
28	28	144	32.15	32.15	0.38	0.65	28.03	28.03	33.17	33.17	0.43
28	28	160	32.40	32.40	0.38	0.65	29.48	29.48	33.42	33.42	0.43
28	28	208	30.60	30.60	0.30	0.50	28.08	28.08	31.62	31.62	0.35

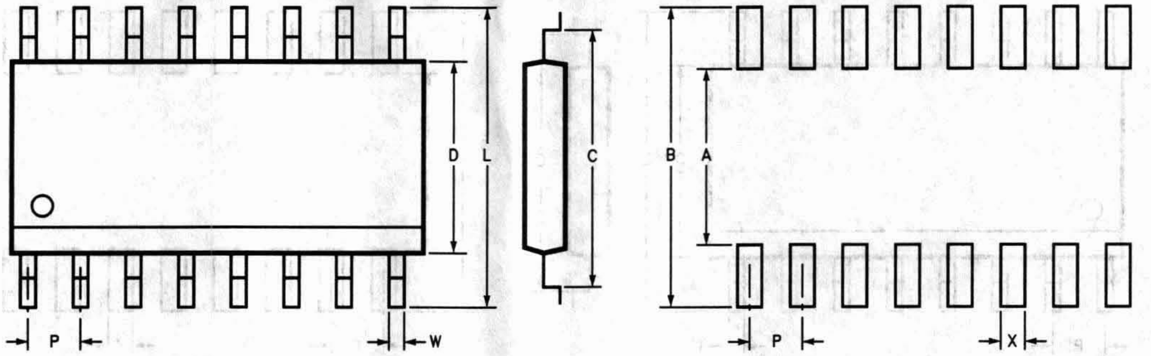
JEDEC Small Outline and Shrink Small Outline Packages (SOP and SSOP)



TL/P/11811-3

D Body Size (in)	Lead Count No.	C Shoulder to Shoulder (in)	L Lead Tip to Tip (in)	W Lead Width (in)	P Lead/Pad Pitch (in)	A Inner Pad to Pad Edge (in)	B Outer Pad to Pad Edge (in)	X Pad Width (in)
SOP								
0.150	8	0.144	0.244	0.020	0.050	0.094	0.294	0.028
0.150	14	0.144	0.244	0.020	0.050	0.094	0.294	0.028
0.150	16	0.144	0.244	0.020	0.050	0.094	0.294	0.028
0.300	14	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	16	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	20	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	24	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	28	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
SSOP								
0.150	20	0.185	0.241	0.010	0.025	0.145	0.281	0.014
0.150	24	0.185	0.241	0.010	0.025	0.145	0.281	0.014
0.300	48	0.340	0.420	0.012	0.025	0.300	0.460	0.016
0.300	56	0.340	0.420	0.012	0.025	0.300	0.460	0.016

EIAJ Small Outline, Shrink Small Outline, and Thin Small Outline Packages (SOP, SSOP and TSOP)



TL/P/11811–4

D Body Size (mm)	Lead Count No.	C Shoulder to Shoulder (mm)	L Lead Tip to Tip (mm)	W Lead Width (mm)	P Lead/Pad Pitch (mm)	A Inner Pad to Pad Edge (mm)	B Outer Pad to Pad Edge (mm)	X Pad Width (mm)
SOP TYPE II								
5.300	14	6.280	8.000	0.400	1.270	5.010	9.270	0.600
5.300	16	6.280	8.000	0.400	1.270	5.010	9.270	0.600
5.300	20	6.280	8.000	0.400	1.270	5.010	9.270	0.600
SSOP TYPE II								
5.300	20	6.600	8.100	0.400	0.650	5.584	9.116	0.451
5.300	24	6.600	8.100	0.400	0.650	5.584	9.116	0.451
SSOP TYPE III								
7.500	40	8.900	10.500	0.350	0.650	7.884	11.516	0.452
TSOP TYPE I								
18.500	32	19.000	20.200	0.250	0.500	17.984	21.216	0.301

Section 7

Appendices/ Physical Dimensions

Section 7 Contents

Appendix A General Product Marking and Code Explanation 7-3
Appendix B Device/Application Literature Cross-Reference 7-4
Appendix C Summary of Commercial Reliability Programs 7-10
Appendix D Military Aerospace Programs from National Semiconductor 7-11
Appendix E Understanding Integrated Circuit Package Power Capabilities 7-21
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Bookshelf
Distributors

Appendix A
General Product Marking & Code Explanation

LF 356 N /A+

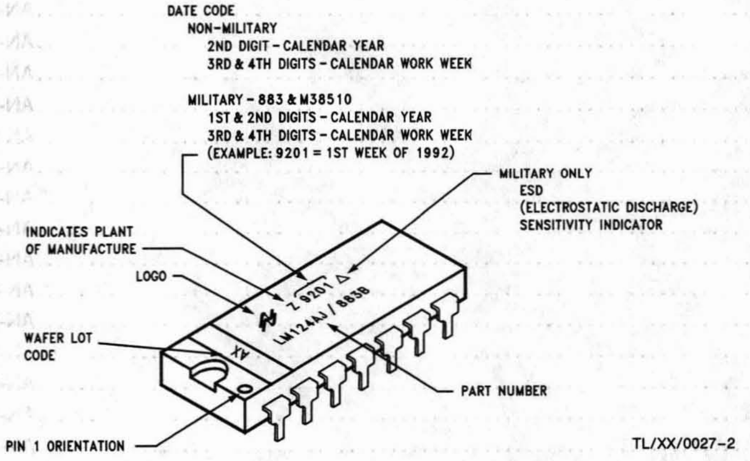
- /A+ — Reliability Program (Optional) (Refer to Appendix C)
- N — Package Type (See Right)
- 356 — Device Number (Generic Type) and Suffix Letter (Optional)
  - A or B: Improved Electrical Specification
  - C, I, E or M: Temperature Range
- LF — Device Family (See Below)

Device Family

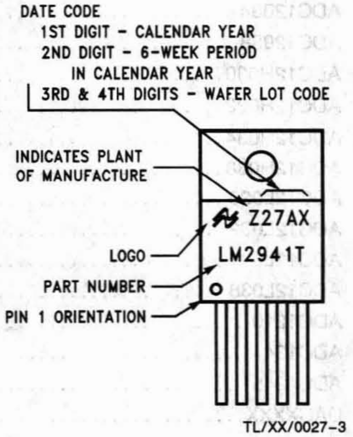
ADC	Data Conversion
AF	Active Filter
AH	Analog Switch (Hybrid)
DAC	Data Conversion
DM	Digital (Monolithic)
HS	Hybrid
LF	Linear (BI-FET™)
LH	Linear (Hybrid)
LM	Linear (Monolithic)
LMC	Linear CMOS
LMD	Linear DMOS
LP	Linear (Low Power)
LPC	Linear CMOS (Low Power)
MF	Linear (Monolithic Filter)
LMF	Linear Monolithic Filter

Package Type

D	Glass/Metal DIP
E	Ceramic Leadless Chip Carrier (LCC)
F	Glass/Metal Flat Pak (¼″ x ¼″)
G	12 Lead TO-8 Metal Can (M/C)
H	Multi-Lead Metal Can (M/C)
H-05	4 Lead M/C (TO-5) } Shipped with Thermal Shield
H-46	4 Lead M/C (TO-46) } Shipped with Thermal Shield
J	Lo-Temp Ceramic DIP
J-8	8 Lead Ceramic DIP ("MiniDIP")
J-14	14 Lead Ceramic DIP (-14 used only when product is also available in -8 pkg).
K	TO-3 M/C in Steel, except LM309K which is shipped in Aluminum
KC	TO-3 M/C (Aluminum)
K Steel	TO-3 M/C (Steel)
M	Small Outline Package
M3	3-Lead Small Outline Package
M5	5-Lead Small Outline Package
N	Molded DIP (EPOXY B)
N-01	Molded DIP (Epoxy B) with Staggered Leads
N-8	8 Lead Molded DIP (Epoxy B) ("Mini-DIP")
N-14	14 Lead Molded DIP (Epoxy B) (-14 used only when product is also available in -8 pkg).
P	3 Lead TO-202 Power Pkg
Q	Cerdip with UV Window
S	3,5,11, & 15 Lead TO-263 Surf. Mt. Power Pkg
T	3,5,11,15 & 23 Lead TO-220 PWR Pkg (Epoxy B)
V	Multi-lead Plastic Chip Carrier (PCC)
W	Lo-Temp Ceramic Flat Pak
WM	Wide Body Small Outline Package


DATE CODE
NON-MILITARY
2ND DIGIT - CALENDAR YEAR
3RD & 4TH DIGITS - CALENDAR WORK WEEK
MILITARY - 883 & M38510
1ST & 2ND DIGITS - CALENDAR YEAR
3RD & 4TH DIGITS - CALENDAR WORK WEEK
(EXAMPLE: 9201 = 1ST WEEK OF 1992)
MILITARY ONLY
ESD
(ELECTROSTATIC DISCHARGE)
SENSITIVITY INDICATOR
INDICATES PLANT
OF MANUFACTURE
LOGO
Z 9201 △
LM124AJ / 883B
WAFER LOT
CODE
AX
PART NUMBER
PIN 1 ORIENTATION

TL/XX/0027-2


DATE CODE
1ST DIGIT - CALENDAR YEAR
2ND DIGIT - 6-WEEK PERIOD
IN CALENDAR YEAR
3RD & 4TH DIGITS - WAFER LOT CODE
INDICATES PLANT
OF MANUFACTURE
Z27AX
LM2941T
LOGO
PART NUMBER
PIN 1 ORIENTATION

TL/XX/0027-3

National Semiconductor

Appendix B
Device/Application Literature Cross-Reference

Device Number	Application Literature
ADCXXXX	AN-156
ADC80	AN-360
ADC0801	AN-233, AN-271, AN-274, AN-280, AN-281, AN-294, LB-53
ADC0802	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0803	AN-233, AN-274, AN-280, AN-281, LB-53
ADC08031	AN-460
ADC0804	AN-233, AN-274, AN-276, AN-280, AN-281, AN-301, AN-460, LB-53
ADC0805	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0808	AN-247, AN-280, AN-281
ADC0809	AN-247, AN-280
ADC0816	AN-193, AN-247, AN-258, AN-280
ADC0817	AN-247, AN-258, AN-280
ADC0820	AN-237
ADC0831	AN-280, AN-281
ADC0832	AN-280, AN-281
ADC0833	AN-280, AN-281
ADC0834	AN-280, AN-281
ADC0838	AN-280, AN-281
ADC1001	AN-276, AN-280, AN-281
ADC1005	AN-280
ADC10461	AN-769
ADC10462	AN-769
ADC10464	AN-769
ADC10662	AN-769
ADC10664	AN-769
ADC12030	AN-929
ADC12032	AN-929
ADC12034	AN-929
ADC12038	AN-929
ADC12H030	AN-929
ADC12H032	AN-929
ADC12H034	AN-929
ADC12H038	AN-929
ADC12L030	AN-929
ADC12L032	AN-929
ADC12L034	AN-929
ADC12L038	AN-929
ADC1210	AN-245
ADC12441	AN-769
ADC12451	AN-769
DACXXXX	AN-156
DAC0800	AN-693
DAC0830	AN-284

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
DAC0831	AN-271, AN-284
DAC0832	AN-271, AN-284
DAC1006	AN-271, AN-275, AN-277, AN-284
DAC1007	AN-271, AN-275, AN-277, AN-284
DAC1008	AN-271, AN-275, AN-277, AN-284
DAC1020	AN-263, AN-269, AN-2293, AN-294, AN-299
DAC1021	AN-269
DAC1022	AN-269
DAC1208	AN-271, AN-284
DAC1209	AN-271, AN-284
DAC1210	AN-271, AN-284
DAC1218	AN-293
DAC1219	AN-693
DAC1220	AN-253, AN-269
DAC1221	AN-269
DAC1222	AN-269
DAC1230	AN-284
DAC1231	AN-271, AN-284
DAC1232	AN-271, AN-284
DAC1280	AN-261, AN-263
DH0034	AN-253
DH0035	AN-49
INS8070	AN-260
LF111	LB-39
LF155	AN-263, AN-447
LF198	AN-245, AN-294
LF311	AN-301
LF347	AN-256, AN-262, AN-263, AN-265, AN-266, AN-301, AN-344, AN-447, LB-44
LF351	AN-242, AN-263, AN-266, AN-271, AN-275, AN-293, AN-447, Appendix C
LF351A	AN-240
LF351B	Appendix D
LF353	AN-256, AN-258, AN-262, AN-263, AN-266, AN-271, AN-285, AN-293, AN-447, LB-44, Appendix D
LF356	AN-253, AN-258, AN-260, AN-263, AN-266, AN-271, AN-272, AN-275, AN-293, AN-294, AN-295, AN-301, AN-447, AN-693
LF357	AN-263, AN-447, LB-42
LF398	AN-247, AN-258, AN-266, AN-294, AN-298, LB-45
LF411	AN-294, AN-301, AN-344, AN-447
LF412	AN-272, AN-299, AN-301, AN-344, AN-447
LF441	AN-301, AN-447
LF13006	AN-344
LF13007	AN-344
LF13331	AN-294, AN-447
LH0002	AN-13, AN-227, AN-263, AN-272, AN-301
LH0024	AN-253
LH0032	AN-242, AN-253
LH0033	AN-48, AN-227, AN-253
LH0063	AN-227
LH0070	AN-301
LH0071	AN-245
LH0094	AN-301
LH0101	AN-261

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LH1605	AN-343
LH2424	AN-867
LM10	AN-211, AN-247, AN-258, AN-271, AN-288, AN-299, AN-300, AN-460, AN-693
LM11	AN-241, AN-242, AN-260, AN-266, AN-271
LM12	AN-446, AN-693, AN-706
LM101	AN-4, AN-13, AN-20, AN-24, LB-42, Appendix A
LM101A	AN-29, AN-30, AN-31, AN-79, AN-241 AN-711, LB-1, LB-2, LB-4, LB-8, LB-14, LB-16, LB-19, LB-28
LM102	AN-4, AN-13, AN-30, LB-1, LB-5, LB-6, LB-11
LM103	AN-110, LB-41
LM105	AN-23, AN-110, LB-3
LM106	AN-41, LB-6, LB-12
LM107	AN-20, AN-31, LB-1, LB-12, LB-19, Appendix A
LM108	AN-29, AN-30, AN-31, AN-79, AN-211, AN-241, LB-14, LB-15, LB-21
LM108A	AN-260, LB-15, LB-19
LM109	AN-42, LB-15
LM109A	LB-15
LM110	LB-11, LB-42
LM111	AN-41, AN-103, LB-12, LB-16, LB-32, LB-39
LM112	LB-19
LM113	AN-56, AN-110, LB-21, LB-24, LB-28, LB-37
LM117	AN-178, AN-181, AN-182, LB-46, LB-47
LM117HV	LB-46, LB-47
LM118	LB-17, LB-19, LB-21, LB-23, Appendix A
LM119	LB-23
LM120	AN-182
LM121	AN-79, AN-104, AN-184, AN-260, LB-22
LM121A	LB-32
LM122	AN-97, LB-38
LM125	AN-82
LM126	AN-82
LM129	AN-173, AN-178, AN-262, AN-266
LM131	AN-210, AN-460, Appendix D
LM131A	AN-210
LM134	LB-41, AN-460
LM135	AN-225, AN-262, AN-292, AN-298, AN-460
LM137	LB-46
LM137HV	LB-46
LM138	LB-46
LM139	AN-74
LM143	AN-127, AN-271
LM148	AN-260
LM150	LB-46
LM158	AN-116
LM160	AN-87
LM161	AN-87, AN-266
LM163	AN-295
LM194	AN-222, LB-21
LM195	AN-110
LM199	AN-161, AN-260
LM199A	AN-161
LM211	LB-39

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM231	AN-210
LM231A	AN-210
LM235	AN-225
LM239	AN-74
LM258	AN-116
LM260	AN-87
LM261	AN-87
LM34	AN-460
LM35	AN-460
LM301A	AN-178, AN-181, AN-222
LM308	AN-88, AN-184, AN-272, LB-22, LB-28, Appendix D
LM308A	AN-225, LB-24
LM309	AN-178, AN-182
LM311	AN-41, AN-103, AN-260, AN-263, AN-288, AN-294, AN-295, AN-307, LB-12, LB-16, LB-18, LB-39
LM313	AN-263
LM316	AN-258
LM317	AN-178, LB-35, LB-46
LM317H	LB-47
LM318	AN-299, LB-21
LM319	AN-828, AN-271, AN-293
LM320	AN-288
LM321	LB-24
LM324	AN-88, AN-258, AN-274, AN-284, AN-301, LB-44, AB-25, Appendix C
LM329	AN-256, AN-263, AN-284, AN-295, AN-301
LM329B	AN-225
LM330	AN-301
LM331	AN-210, AN-240, AN-265, AN-278, AN-285, AN-311, LB-45, Appendix C, Appendix D
LM331A	AN-210, Appendix C
LM334	AN-242, AN-256, AN-284
LM335	AN-225, AN-263, AN-295
LM336	AN-202, AN-247, AN-258
LM337	LB-46
LM338	LB-49, LB-51
LM339	AN-74, AN-245, AN-274
LM340	AN-103, AN-182
LM340L	AN-256
LM342	AN-288
LM346	AN-202, LB-54
LM348	AN-202, LB-42
LM349	LB-42
LM358	AN-116, AN-247, AN-271, AN-274, AN-284, AN-298, Appendix C
LM358A	Appendix D
LM359	AN-278, AB-24
LM360	AN-87
LM361	AN-87, AN-294
LM363	AN-271
LM380	AN-69, AN-146
LM385	AN-242, AN-256, AN-301, AN-344, AN-460, AN-693, AN-777
LM386	LB-54
LM391	AN-272
LM392	AN-274, AN-286

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM393	AN-271, AN-274, AN-293, AN-694
LM394	AN-262, AN-263, AN-271, AN-293, AN-299, AN-311, LB-52
LM395	AN-178, AN-181, AN-262, AN-263, AN-266, AN-301, AN-460, LB-28
LM399	AN-184
LM555	AN-694, AB-7
LM556	AB-7
LM565	AN-46, AN-146
LM566	AN-146
LM604	AN-460
LM628	AN-693, AN-706
LM629	AN-693, AN-694, AN-706
LM709	AN-24, AN-30
LM710	AN-41, LB-12
LM725	LB-22
LM741	AN-79, LB-19, LB-22
LM833	AN-346
LM1036	AN-390
LM1202	AN-867
LM1203	AN-861
LM1204	AN-934
LM1458	AN-116
LM1524	AN-272, AN-288, AN-292, AN-293
LM1558	AN-116
LM1578A	AB-30
LM1823	AN-391
LM1830	AB-10
LM1865	AN-390
LM1886	AN-402
LM1889	AN-402
LM1894	AN-384, AN-386, AN-390
LM2419	AN-861
LM2577	AN-776, AN-777
LM2876	AN-898
LM2889	AN-391, AN-402
LM2907	AN-162
LM2917	AN-162
LM2931	AB-12
LM2931CT	AB-11
LM3045	AN-286
LM3046	AN-146, AN-299
LM3089	AN-147
LM3524	AN-272, AN-288, AN-292, AN-293
LM3525A	AN-694
LM3578A	AB-30
LM3875	AN-898
LM3876	AN-898
LM3886	AN-898
LM3900	AN-72, AN-263, AN-274, AN-278, LB-20, AB-24
LM3909	AN-154
LM3914	AN-460, LB-48, AB-25
LM3915	AN-386
LM3999	AN-161

Device/Application Literature Cross-Reference (Continued)

Device Number	**Application Literature**
LM4250	AN-88, LB-34
LM6181	AN-813, AN-840
LM7800	AN-178
LM12454	AN-906, AN-947, AN-949
LM12458	AN-906, AN-947, AN-949
LM12H454	AN-906, AN-947, AN-949
LM12H458	AN-906, AN-947, AN-949
LM12L458	AN-906, AN-947, AN-949
LM18293	AN-706
LM78L12	AN-146
LM78S40	AN-711
LMC555	AN-460, AN-828
LMC660	AN-856
LMC835	AN-435
LMC6044	AN-856
LMC6062	AN-856
LMC6082	AN-856
LMC6484	AN-856
LMD18200	AN-694, AN-828
LMF40	AN-779
LMF60	AN-779
LMF90	AN-779
LMF100	AN-779
LMF380	AN-779
LMF390	AN-779
LP324	AN-284
LP395	AN-460
LPC660	AN-856
MF4	AN-779
MF5	AN-779
MF6	AN-779
MF8	AN-779
MF10	AN-307, AN-779
MM2716	LB-54
MM54104	AN-252, AN-287, LB-54
MM57110	AN-382
MM74C00	AN-88
MM74C02	AN-88
MM74C04	AN-88
MM74C948	AN-193
MM74HC86	AN-861, AN-867
MM74LS138	LB-54
MM53200	AN-290
2N4339	AN-32

National Semiconductor

Appendix C
Summary of Commercial Reliability Programs

P+ Product Enhancement

The P+ product enhancement program involves dynamic tests that screen out assembly related and silicon defects that can lead to infant mortality and/or reduce the survivability of the device under high stress conditions. This program includes but is not limited to the following power devices:

Device	Package Types					
	TO-3 K STEEL	TO-39 (H)	TO-220 (T)	DIP (N)	SO (M)	TO-263 (S)
LM12	X					
LM109/309	X	X				
LM117/317	X	X	X			X
LM117HV/317HV	X	X				
LM120/320	X	X	X			
LM123/323	X					
LM133/333	X		X			
LM137/337	X	X	X			
LM137HV/337HV	X	X				
LM138/338	X		X			
LM140/340	X		X			
LM145/345	X					
LM150/350	X		X			
LM195/395	X	X	X			
LM2930/2935/2984			X			X
LM2937			X			X
LM2940/2941			X			X
LM2990/2991			X			X
LM2575/2575HV			X	X	X	X
LM2576			X			X
LM2577			X	X	X	X
LMD18200/18201			X			

Appendix D
Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. The process flows and catagories shown below are for general reference only. For further information and availability, please contact the Customer Response Center at 1-800-272-9959, Military/Aerospace Marketing group or your local sales office.

National Semiconductor's Military/Aerospace Program is founded on dedication to excellence. National offers complete support across the broadest range of products with the widest selection of qualification levels and screening flows. These flows include:

Process Flows (Integrated Circuits)	Description
JAN S	QML products processed to MIL-I-38535 Level S or V for Space level applications.
JAN B	QML products processed to MIL-I-38535 Level B or Q for Military applications.
SMD	QML products processed to a Standard Microcircuit Drawing with Table I Electricals controlled by DESC.
883	QML products processed to MIL-STD-883 Level B for Military applications.
MLP	Products processed on the Monitored Line (Program) developed by the Air Force for Space level applications.
-MIL	Similar to MIL-STD-883 with exceptions noted on the Certificate of Conformance.
MSP	Military Screening Products for initial release of advanced products.
MCP	Commercial products processed in a military assembly. Electrical testing performed at 25°C, plus minimum and maximum operating temperature to commercial limits.
MCR	Commercial products processed in a military assembly. Electrical testing performed at 25°C to commercial limits
MRP	Military Ruggedized Plastic products processed to avionics requirements.
MRR	Commercial Ruggedized plastic product processed in a commercial assembly with electrical testing at 25°C.
MPC	Commercial plastic products processed in a commercial assembly with electrical testing at 25°C.

- **QML:** The purpose of the QML program, which is administered by the Defense Electronics Supply Center (DESC), is to provide the military community with standardized products that have been manufactured and screened to the highest quality and reliability standards in facilities that have been certified by the government. To achieve QML status, manufacturers must submit their facilities, quality procedures and design philosophies to a thorough audit aimed at confirming their ability to produce product to the highest design and quality standards. They must be listed on DESC's Qualified Manufacturer List (QML) before devices can be marked and shipped as QML product.

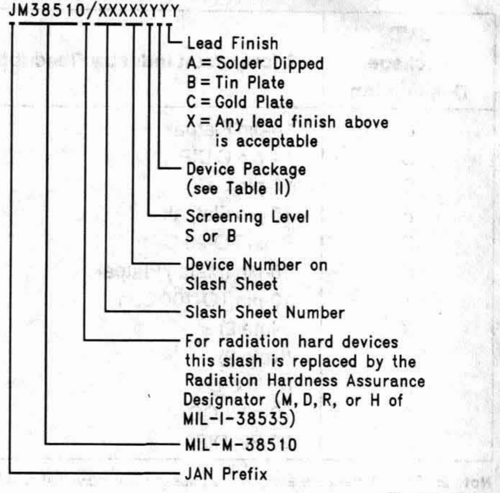
  Two processing levels are specified within MIL-I-38535, the QML standard: Class S (typically specified for space and strategic applications) and Class B (used for tactical missile, airborne, naval and ground systems). The requirements for both classes are defined within MIL-STD-883. National is one of the industry's leading suppliers of both classes.
- **Standard Microcircuit Drawings (SMD).** SMDs are issued to provide standardized versions of devices offered under QML. MIL-STD-883 screening is coupled with tightly controlled electrical test specifications that allow a manufacturer to use his standard electrical tests. Table I explains the marking of JAN devices, and Table II outlines current marking requirements for QML/SMD devices. Copies of MIL-I-38535 and the QML can be obtained from the Naval Publications and Forms Center (5801 Tabor Avenue, Philadelphia, PA 19120, 212/697-2179. A current listing of National's SMD offerings can be obtained from our authorized distributors, our sales offices, our Customer Response Center (Arlington, Texas, 817/468-6300), or from DESC.
- **MIL-STD-883.** Originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-SMD military product. MIL-STD-883 defines the minimum requirements for a device to be marked and advertised as 883-compliant. Design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures are outlined in paragraph 1.1.2 of MIL-STD-883.

  National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

  As with SMDs a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits and test temperatures must be clearly documented. At National Semiconductor, this information is available via our Table I (formerly RETS, Reliability Electrical Test Specification Program). The Table I document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

  Some of National's products are produced on a flow similar to MIL-STD-883. These devices are screened to the same stringent requirements as 883 product, but are marked as **-MIL**; specific reasons for prevention of compliancy are clearly defined in the Certificate of Conformance (C of C) shipped with the product.
- **Monitored Line Program (MLP):** is a non JAN Level S program developed by the Air Force. Monitored Line product usually provides the shortest cycle time, and is acceptable for application in several space level programs. Lockheed Missiles and Space Company in Sunnyvale, California, under an Air Force contract, provides "on-site" monitoring of product processing, and as appropriate, program management. Monitored Line orders generally do not allow "customizing", and most flows do not include quality conformance inspection. Drawing control is maintained by the Lockheed Company.
- **Military Screening Program (MSP):** National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly. Through this program, screened product is made available for prototypes and breadboards prior to or during the QML activities. MSP products receive the 100% screening of Table III, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

TABLE I. JAN S or B Part Marking


JM38510/XXXXXYYY
Lead Finish
A = Solder Dipped
B = Tin Plate
C = Gold Plate
X = Any lead finish above is acceptable
Device Package (see Table II)
Screening Level S or B
Device Number on Slash Sheet
Slash Sheet Number
For radiation hard devices this slash is replaced by the Radiation Hardness Assurance Designator (M, D, R, or H of MIL-I-38535)
MIL-M-38510
JAN Prefix

TL/XX/0030-1

TABLE I-A. JAN Package Codes

JAN Package Designation	Microcircuit Industry Description
A	14-pin ¼″ x ¼″ (Metal) Flatpak
B	14-pin 3⁄16″ x ¼″ (Metal) Flatpak
C	14-pin ¼″ x ¾″ Dual-In-Line
D	14-pin ¼″ x ⅜″ (Ceramic) Flatpak
E	16-pin ¼″ x ⅞″ Dual-In-Line
F	16-pin ¼″ x ⅜″ (Metal or Ceramic) Flatpak
G	8-pin TO-99 Can or Header
H	10-pin ¼″ x ¼″ (Metal) Flatpak
I	10-pin TO-100 Can or Header
J	24-pin ½″ x 1¼″ Dual-In-Line
K	24-pin ⅜″ x ⅝″ Flatpak
L	24-pin ¼″ x 1¼″ Dual-In-Line
M	12-pin TO-101 Can or Header
N	(Note 1)
P	8-pin ¼″ x ⅜″ Dual-In-Line
Q	40-pin 3⁄16″ x 2 1⁄16″ Dual-In-Line
R	20-pin ¼″ x 1 1⁄16″ Dual-In-Line
S	20-pin ¼″ x ½″ Flatpak
T	(Note 1)
U	(Note 1)
V	18-pin ⅜″ x 15⁄16″ Dual-In-Line
W	22-pin ⅜″ x 1⅛″ Dual-In-Line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-terminal 0.350″ x 0.350″ Chip Carrier
3	28-terminal 0.450″ x 0.450″ Chip Carrier

Note 1: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE II. Standard Military Drawing (SMD) Marking

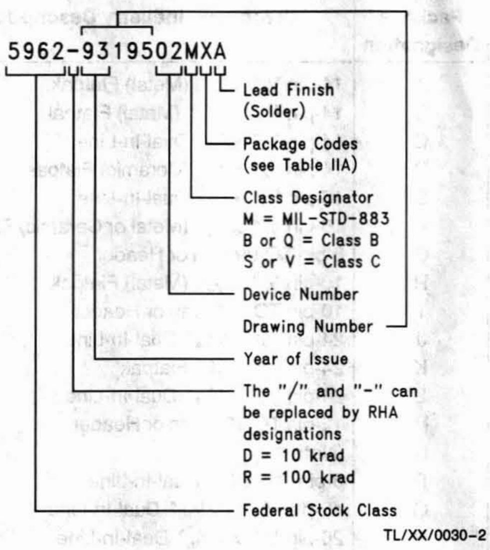

5962-9319502MXA
Lead Finish (Solder)
Package Codes (see Table IIA)
Class Designator
M = MIL-STD-883
B or Q = Class B
S or V = Class C
Device Number
Drawing Number
Year of Issue
The "/" and "-" can be replaced by RHA designations
D = 10 krad
R = 100 krad
Federal Stock Class
TL/XX/0030-2

TABLE II-A. SMD Package Codes

SMD Package Designation	Microcircuit Industry Description
C	14-pin Flatpak
D	14-pin C DIP
E	16-pin C DIP
F	16-pin Flatpak
G	8-pin TO-99 Can
H	10-pin (Metal) Flatpak
I	10-pin TO-100 Can
X	(Note 2)
Y	(Note 2)
P	8-pin C DIP
2	20-pin LCC
R	20-Pin DIP

Note 2: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

	Screen	Class S		Class B	
		Method	Reqmt	Method	Reqmt
1.	Wafer Lot Acceptance	5007	All Lots		
2.	Nondestructive Bond Pull (Note 14)	2023	100%		
3.	Internal Visual (Note 1)	2020, Condition A	100%	2010, Condition B	100%
4.	Stabilization Bake (Note 16)	1008, Condition C, Min 24 Hrs. Min	100%	1008, Condition C, Min 24 Hrs. Min	100%
5.	Temperature Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition E Min Y_1 Orientation Only	100%	2001, Condition E Min Y_1 Orientation Only	100%
7.	Visual Inspection (Note 3)		100%		100%
8.	Particle Impact Noise Detection (PIND)	2010, Condition A (Note 4)	100%		
9.	Serialization	(Note 5)	100%		
10.	Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	
11.	Burn-In Test	1015 240 Hrs. @ 125°C Min (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min	100%
12.	Interim (Post Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 3)	100%		

TABLE III. 100% Screening Requirements (Continued)

	Screen	Class S		Class B	
		Method	**Reqmt**	**Method**	**Reqmt**
13.	Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min (Cond. F Not Allowed)	100%		
14.	Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification	100%
15.	PDA Calculation	5% Parametric (Note 14), 3% Functional	All Lots	5% Parametric (Note 14)	All Lots
16.	Final Electrical Test (Note 15) a) Static Tests 1) 25°C (Subgroup 1, Table I, 5005) 2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005) b) Dynamic Tests or Functional Tests 1) 25°C (Subgroup 4 or 7) 2) Max and Min Rated Operating Temp. (Subgroups 5 and 6 or 8, Table I, 5005) c) Switching Tests 25°C (Subgroup 9, Table I, 5005)	Per Applicable Device Specification	 100% 100% 100% 100% 100%	Per Applicable Device Specification	 100% 100% 100% 100% 100%
17.	Seal Fine, Gross	1014	100% (Note 8)	1014	100% (Note 9)
18.	Radiographic (Note 10)	2012 Two Views	100%		
19.	Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20.	External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock Method 1011, Test Condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-I-38585 paragraph 40.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separately or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g., flatpaks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 9.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005.

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and record is required at steps 10 and 12 only for those parameters for which post-burn-in delta measurements are specified. All parameters shall be read and recorded at step 14.

Note 14: The PDA shall apply to all subgroup 1 parameters at 25°C and all delta parameters.

Note 15: Only one view is required for flat packages and leadless chip carriers with leads on all four sides.

Note 16: May be performed at any time prior to step 10.

Military Analog Products Available from National Semiconductor

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
HIGH PERFORMANCE AMPLIFIERS AND BUFFERS				
LF147	D, J	Wide BW Quad JFET Op Amp	SMD/JAN	/11906
LF155A	H	JFET Input Op Amp	883	—
LF156	H	JFET Input Op Amp	883	—
LF156A	H	JFET Input Op Amp	883	—
LF157	H	JFET Input Op Amp	883	—
LF157A	H	JFET Input Op Amp	883	—
LF411M	H	Low Offset, Low Drift JFET Input	883/JAN	/11904
LF412M	H, J	Low Offset, Low Drift JFET Input-Dual	883/JAN	/11905
LF441M	H	Low Power JFET Input	883	—
LF442M	H	Low Power JFET Input-Dual	883	—
LF444M	D	Low Power JFET Input-Quad	883	—
LH0002	H	Buffer Amp	"-MIL"	—
LH0021	K	1.0 Amp Power Op Amp	"-MIL"	—
LH0024	H	High Slew Rate Op Amp	"-MIL"	—
LH0032	G	Ultra Fast FET-Input Op Amp	"-MIL"	—
LH0041	G	0.2 Amp Power Op Amp	"-MIL"	—
LH0101	K	Power Op Amp	"-MIL"	—
LM10	H	Super-Block™ Micropower Op Amp/Ref	883/SMD	5962-87604
LM101A	J, H, W	General Purpose Op Amp	883/JAN	/10103
LM108A	J, H, W	Precision Op Amp	883/JAN	/10104
LM118	J, H	Fast Op Amp	883/JAN	/10107
LM124	J, E, W	Low Power Quad Op Amp	883/JAN	/11005
LM124A	J, E, W	Low Power Quad	883/JAN	/11006
LM146	J	Quad Programmable Op Amp	883	—
LM148	J, E	Quad 741 Op amp	883/JAN	/11001
LM158A	J, H	Low Power Dual Op Amp	883/SMD	5962-8771002
LM158	J, H	Low Power Dual Op Amp	883/SMD	5962-8771001
LM611AM	J	Super-Block Op Amp/Reference	883/SMD	—
LM613AM	J, E	Super-Block Dual Op Amp/Dual Comp/Ref	883/SMD	—
LM614AM	J	Super-Block Quad Op Amp/Ref	883/SMD	—
LM709A	H, J, W	General Purpose Op Amp	883/SMD	7800701
LM741	J, H, W	General Purpose Op Amp	883/JAN	/10101
LM747	J, H	General Purpose Dual Op Amp	883/JAN	/10102
LM6118	J, E	VIP Dual Op Amp	883/SMD	5962-91565
LM6121	H, J	VIP Buffer	883/SMD	5962-90812
LM6125	H	VIP Buffer with Error Flag	883/SMD	5962-90815
LM6161	J, E, W	VIP Op Amp (Unity Gain)	883/SMD	5962-89621
LM6162	J, E, W	VIP Op Amp ($A_V > 2, -1$)	883/SMD	5962-92165
LM6164	J, E, W	VIP Op Amp ($A_V > 5$)	883/SMD	5962-89624
LM6165	J, E, W	VIP Op Amp ($A_V > 25$)	883/SMD	5962-89625
LM6181AM	J	VIP Current Feedback Op Amp	883/SMD	5962-9081802
LM6182AM	J	VIP Current Feedback Dual Op Amp	883/SMD	5962-9460301
LMC660AM	J	Low Power CMOS Quad Op Amp	883/SMD	5962-9209301
LMC662AM	J	Low Power CMOS Dual Op Amp	883/SMD	5962-9209401
LPC660AM	J	Micropower CMOS Quad Op Amp	883/SMD	5962-9209302
LPC662AM	J	Micropower CMOS Dual Op Amp	883/SMD	5962-9209402
LMC6482AM	J	Rail to Rail CMOS Dual Op Amp	883/SMD	5962-9453401
LMC6484AM	J	Rail to Rail CMOS Quad Op Amp	883/SMD	5962-9453402
OP07	H	Precision Op Amp	883	—

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
COMPARATORS				
LF111	H	Voltage Comparator	"-MIL"	—
LH2111	J, W	Dual Voltage Comparator	883/JAN	/10305
LM106	H, W	Voltage Comparator	883/SMD	8003701
LM111	J, H, E, W	Voltage Comparator	883/JAN	/10304
LM119	J, H, E, W	High Speed Dual Comparator	883/JAN	/10306
LM139	J, E, W	Quad Comparator	883/JAN	/11201
LM139A	J, E, W	Precision Quad Comparator	883/SMD	5962-87739
LM160	J, H	High Speed Differential Comparator	883/SMD	8767401
LM161	J, H, W	High Speed Differential Comparator	883/SMD	5962-87572
LM193	J, H	Dual Comparator	883	—
LM193A	J, H	Dual Comparator	883/JAN	/11202
LM612AM	J	Dual-Channel Comparator/Reference	883/SMD	5962-93002
LM613AM	J, E	Super-Block Dual Comparator/ Dual Op Amp/Adj Reference	883/SMD	5962-93003
LM615AM	J	Quad Comparator/Adjustable Reference	883	—
LM710A*	J, H, W	Voltage Comparator	883/JAN	/10301
LM711A*	J, H, W	Dual LM710	883/JAN	/10302
LM760	J, H	High Speed Differential Comparator	883/SMD	5962-87545

*Formerly manufactured by Fairchild Semiconductor as part numbers μA710 and μA711.

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
LINEAR REGULATORS				
Positive Voltage Regulators				
LM105	H	Adjustable Voltage Regulator	883/SMD	5962-89588
LM109	H	5V Regulator, $I_o = 20$ mA	883/JAN	/10701BXA
LM109	K	5V Regulator, $I_o = 1$A	883/JAN	/10701BYA
LM117	H, E, K	Adjustable Regulator	883/JAN	/11703, /11704
LM117HV	H	Adjustable Regulator, $I_o = 0.5$A	883/SMD	7703402XA
LM117HV	K	Adjustable Regulator, $I_o = 1.5$A	883/SMD	7703402YA
LM123	K	3A Voltage Regulator	883	—
LM138	K	5A Adjustable Regulator	"-MIL"	—
LM140-5.0	H	0.5A Fixed 5V Regulator	883/JAN	/10702
LM140-6.0	H	0.5A Fixed 6V Regulator	883	—
LM140-8.0	H	0.5A Fixed 8V Regulator	883	—
LM140-12	H	0.5A Fixed 12V Regulator	883/JAN	/10703
LM140-15	H	0.5A Fixed 15V Regulator	883/JAN	/10704
LM140-24	H	0.5A Fixed 24V Regulator	883	—
LM140A-5.0	K	1.0A Fixed 5V Regulator	883	—
LM140A-12	K	1.0A Fixed 12V Regulator	883	—
LM140A-15	K	1.0A Fixed 15V Regulator	883	—
LM140K-5.0	K	1.0A Fixed 5V Regulator	883/JAN	/10706
LM140K-12	K	1.0A Fixed 12V Regulator	883/JAN	/10707
LM140K-15	K	1.0A Fixed 15V Regulator	883/JAN	/10708
LM140LAH-5.0	H	100 mA Fixed 5V Regulator	883	—
LM140LAH-12	H	100 mA Fixed 12V Regulator	883	—
LM140LAH-15	H	100 mA Fixed 15V Regulator	883	—
LM150	K	3A Adjustable Power Regulator	883	—
LM2940-5.0	K	5V Low Dropout Regulator	883/SMD	5962-89587
LM2940-8.0	K	8V Low Dropout Regulator	883/SMD	5962-90883
LM2940-12	K	12V Low Dropout Regulator	883/SMD	5962-90884
LM2940-15	K	15V Low Dropout Regulator	883/SMD	5962-90885
LM2941	K	Adjustable Low Dropout Regulator	883/SMD	TBD
LM431	H, K	Adjustable Shunt Regulator	883	—
LM723	H, J, E	Precision Adjustable Regulator	883/JAN	/10201
LP2951	H, E, J	Adjustable Micropower LDO	883/SMD	5962-38705
LP2953AM	J	250 mA Adj. Micropower LDO	883/SMD	5962-9233601

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
LINEAR REGULATORS (Continued)				
Negative Voltage Regulators				
LM120-5.0	H	Fixed 0.5A Regulator, $V_{OUT} = -5V$	883/JAN	/11501
LM120-8.0	H	Fixed 0.5A Regulator, $V_{OUT} = -8V$	883	—
LM120-12	H	Fixed 0.5A Regulator, $V_{OUT} = -12V$	883/JAN	/11502
LM120-15	H	Fixed 0.5A Regulator, $V_{OUT} = -15V$	883/JAN	/11503
LM120-5.0	K	Fixed 1.0A Regulator, $V_{OUT} = -5V$	883/JAN	/11505
LM120-12	K	Fixed 1.0A Regulator, $V_{OUT} = -12V$	883/JAN	/11506
LM120-15	K	Fixed 1.0A Regulator, $V_{OUT} = -15V$	883/JAN	/11507
LM137A	H	Precision Adjustable Regulator	883/SMD	7703406XA
LM137A	K	Precision Adjustable Regulator	883/SMD	7703406YA
LM137	H, K	Adjustable Regulator	883/JAN	/11803, /11804
LM137HV	H	Adjustable (High Voltage) Regulator	883/SMD	7703404XA
LM137HV	K	Adjustable (High Voltage) Regulator	883/SMD	7703404YA
LM145-5.0	K	Negative 3 Amp Regulator	883/SMD	5962-90645
LM145-5.2	K	Negative 3 Amp Regulator	883	—
SWITCHING REGULATORS				
LM1575-5	J, K	Simple Switcher™ Step-Down, $V_{OUT} = 5V$	883/SMD	5962-9167201
LM1575-12	J, K	Simple Switcher Step-Down, $V_{OUT} = 12V$	883/SMD	5962-9167301
LM1575-15	J, K	Simple Switcher Step-Down, $V_{OUT} = 15V$	883/SMD	5962-9167401
LM1575-ADJ	J, K	Simple Switcher Step-Down, Adj V_{OUT}	883/SMD	5962-9167101
LM1575HV-5	K	Simple Switcher Step-Down, $V_{OUT} = 5V$	883	—
LM1575HV-12	K	Simple Switcher Step-Down, $V_{OUT} = 12V$	883	—
LM1575HV-15	K	Simple Switcher Step-Down, $V_{OUT} = 15V$	883	—
LM1575HV-ADJ	K	Simple Switcher Step-Down, Adj V_{OUT}	883	—
LM1577-12	K	Simple Switcher Step-Up, $V_{OUT} = 12V$	883/SMD	5962-9216701
LM1577-15	K	Simple Switcher Step-Up, $V_{OUT} = 15V$	883/SMD	5962-9216801
LM1577-ADJ	K	Simple Switcher Step-Up, Adj V_{OUT}	883/SMD	5962-9216601
LM1578	H	750 mA Switching Regulator	883/SMD	5962-89586
LM78S40*	J	Universal Switching Regulator Subsystem	883/SMD	5962-88761
*Formerly manufactured by Fairchild Semiconductor as the μA78S40DMQB.				
VOLTAGE REFERENCES				
LM103-3.0	H	Reference Diode, BV = 3.0V	883/SMD	7702806
LM103-3.3	H	Reference Diode, BV = 3.3V	883/SMD	7702807
LM103-3.6	H	Reference Diode, BV = 3.6V	883/SMD	7702808
LM103-3.9	H	Reference Diode, BV = 3.9V	883/SMD	7702809
LM113	H	Reference Diode with 5% Tolerance	883/SMD	5962-8671101
LM113-1	H	Reference Diode with 1% Tolerance	883/SMD	5962-8671102
LM113-2	H	Reference Diode with 2% Tolerance	883/SMD	5962-8671103
LM129A	H	Precision Reference, 10 ppm/°C Drift	883/SMD	5962-8992101XA
LM129B	H	Precision Reference, 20 ppm/°C Drift	883/SMD	5962-8992102XA
LM136A-2.5	H	2.5V Reference Diode, 1% V_{OUT} Tolerance	883	—
LM136A-5.0	H	5V Reference Diode, 1% V_{OUT} Tolerance	883/SMD	8418001
LM136-2.5	H	2.5V Reference Diode, 2% V_{OUT} Tolerance	883	—
LM136-5.0	H	5V Reference Diode, 2% V_{OUT} Tolerance	883	—

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
VOLTAGE REFERENCES (Continued)				
LM169	H	10V Precision Reference, Low Tempco 0.05% Tolerance	883	—
LM185B	H, E	Adjustable Micropower Voltage Reference	883/SMD	5962-9041401
LM185BX2.5	H	2.5V Micropower Reference Diode, Ultralow Drift	883/SMD	5962-8759404
LM185BY	H	Adjustable Micropower Voltage Reference	883	—
LM185BY1.2	H	1.2V Micropower Reference Diode, Low Drift	883/SMD	5962-8759405
LM185BY2.5	H	2.5V Micropower Reference Diode, Low Drift	883/SMD	5962-8759406
LM185-1.2	H, E	1.2V Micropower Reference Diode, Low Drift	883/SMD	5962-8759401
LM185-2.5	H, E	2.5V Micropower Reference Diode, Low Drift	883/SMD	5962-8759402
LM199	H	Precision Reference, Low Tempco	883/SMD	5962-8856102
LM199A	H	Precision Reference, Ultralow Tempco	883/SMD	5962-8856101
LM199A-20	H	Precision Reference, Ultralow Tempco	883	—
LM611AM	J	Super-Block Op Amp/Reference	883	
LM612AM	J	Super-Block Dual-Channel Comparator/Reference	883/SMD	5962-9300201
LM613AM	J, E	Super-Block Dual Op Amp/DualComp/Dual Ref	883/SMD	5962-9300301
LM614AM	J	Super-Block Quad Op Amp/Reference	883/SMD	5962-9300401
LM615AM	J	Super-Block Quad Comparator/Reference	883/SMD	TBD
LH0070-0	H	Precision BCD Buffered Reference	"-MIL"	—
LH0070-1	H	Precision BCD Buffered Reference	"-MIL"	—
LH0070-2	H	Precision BCD Buffered Reference	"-MIL"	—
DATA ACQUISITION				
ADC08020L	J	8-Bit μP-Compatible	883/SMD	5962-90966
ADC0851	J	8-Bit Analog Data Acquisition & Monitoring System	883/SMD	TBD
ADC0858	J	8-Bit Analog Data Acquisition & Monitoring System	883/SMD	TBD
ADC08061CM	J	8-Bit Multistep ADC	883/SMD	TBD
ADC10061CM	J	10-Bit Multistep ADC	883/SMD	TBD
ADC10062CM	J	10-Bit Multistep ADC w/Dual Input Mutiplexer	883/SMD	TBD
ADC10064CM	J	10-Bit Multistep ADC w/Quad Input Multiplexer	883/SMD	TBD
ADC1241CM	J	12-Bit Plus Sign Self-Calibrating with Sample/Hold Function	883/SMD	5962-9157801
ADC12441CM	J	Dynamically-Tested ADC1241	883/SMD	5962-9157802
ADC1251CM	J	12-Bit Plus Sign Self-Calibrating with Sample/Hold Function	883/SMD	5962-9157801
ADC12451CM	J	Dynamically-Tested ADC1251	883/SMD	TBD
DAC0854CM	J	Quad 8-Bit D/A Converter with Read Back	883/SMD	TBD
DAC1054CM	J	Quad 10-Bit D/A Converter with Read Back	883/SMD	TBD
LM12458M	EL, W	12-Bit Data Acquisition System	883/SMD	5962-9319501
LM12H458M	EL, W	12-Bit Data Acquisition System	883/SMD	5962-9319502

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
DATA ACQUISITION SUPPORT				
Switched Capacitor Filters				
LMF60CMJ50	J	6th Order Butterworth Lowpass	883/SMD	5962-90967
LMF60CMJ100	J	6th Order Butterworth Lowpass	883/SMD	5962-90967
LMF90CM	J	4th Order Elliptic Notch	883/SMD	5962-90968
LMF100A	J, E	Dual 2nd Order General Purpose	883/SMD	5962-9153301
Sample and Hold				
LF198	H	Monolithic Sample and Hold	SMD/JA	5962-87608 /12501
Motion Control				
LMD18200-2	D	Dual 3A, 55V H-Bridge	883/JAN	5962-9232501

Note 1: D: Side-Brazed DIP
E: Leadless Ceramic Chip Carrier
G: Metal Can (TO-8)
H: Metal Can (TO-39, TO-5, TO-99, TO-100)
J: Ceramic DIP
K: Metal Can (TO-3)
W: Flatpak

Note 2: Process Flows
JAN = JM38510, Level B
SMD = Standard Military Drawing
883 = MIL-STD-883 Rev C
-MIL = Exceptions to 883C noted on Certificate of Conformance

Note 3: Please call your local sales office to determine price and availability of space-level products. All "LM" prefix products in this guide are availble with space-level processing.

National Semiconductor

Appendix E
Understanding Integrated Circuit Package Power Capabilities

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

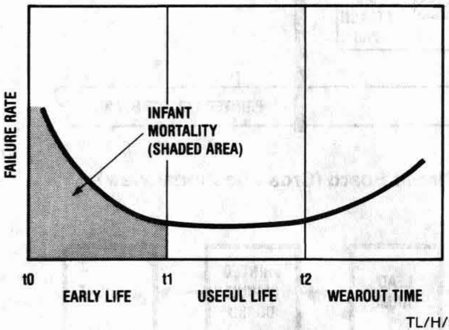


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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: $X1$ = Failure rate at junction temperature $T1$
$X2$ = Failure rate at junction temperature $T2$
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

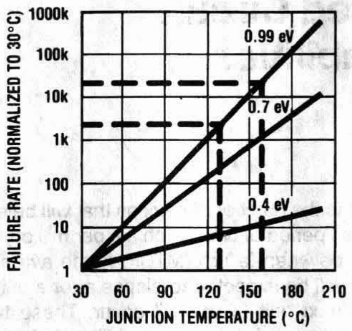

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D\,(\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using IC components.

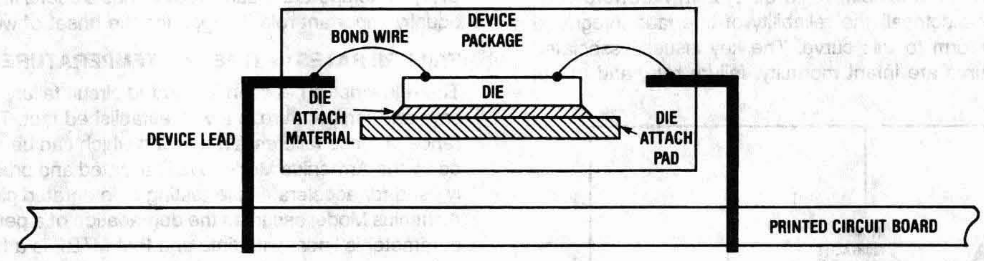

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

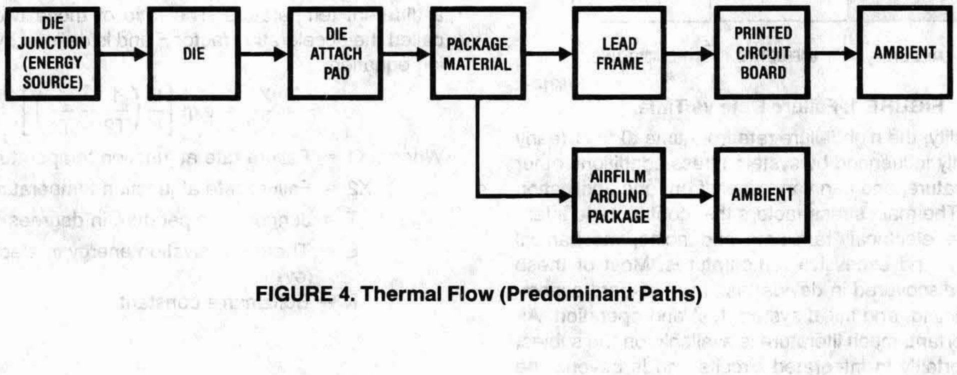

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, $T_A(\text{max})$, the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D \text{ @ } 25°C = \frac{T_J(\text{max}) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

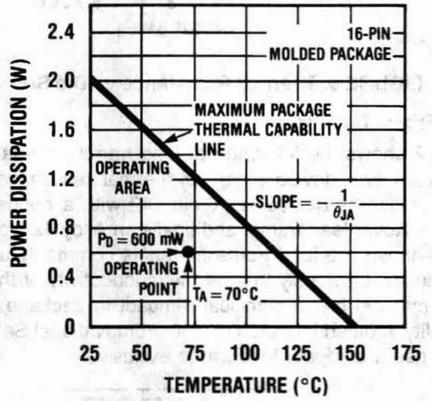

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all integrated circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

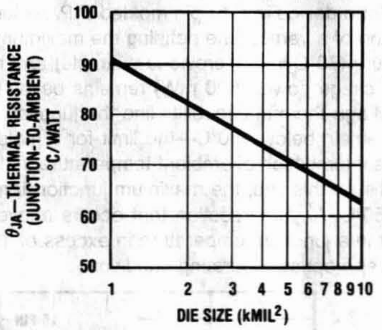

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

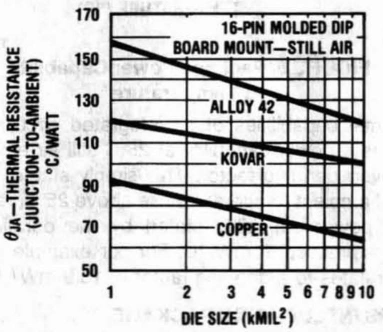

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

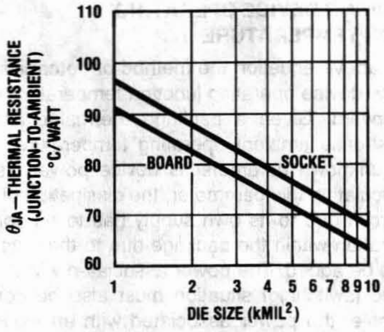

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

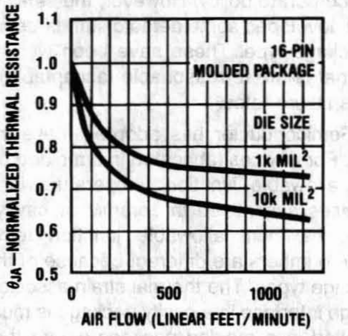

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

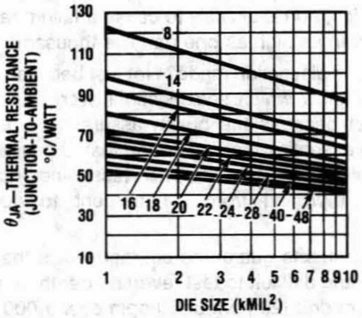
NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Linear Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTEGRATED CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Linear Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the linear data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

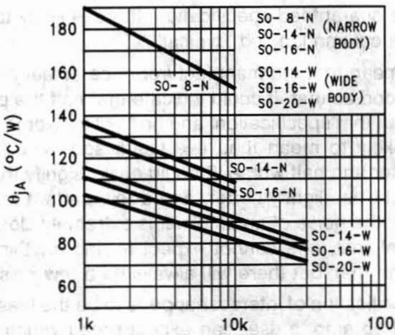
Molded (N Package) DIP*
Copper Leadframe—HTP
Die Attach Board Mount—
Still Air



*Packages from 8- to 20-pin 0.3 mil width TL/H/9312-10
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Surface Mount (M, MW Packages),
Board Mount, Still Air



TL/H/9312-12

FIGURE 12. Thermal Resistance for "SO" Packages (Board Mount)

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

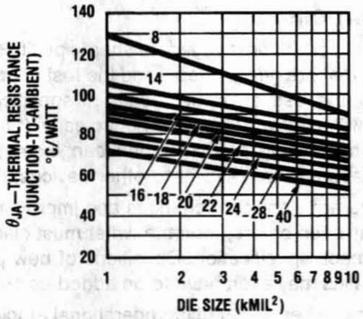
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D \text{ @ } 70^\circ C = 1476\text{ mW} - (11.8\text{ mW}/^\circ C) \times (70^\circ C - 25^\circ C) = 945\text{ mW}$$

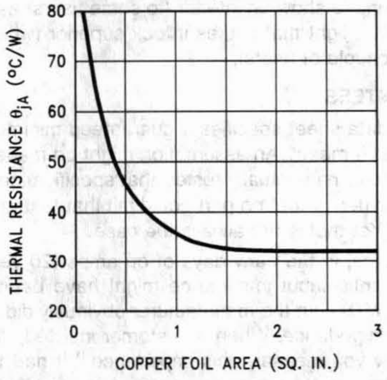
Cavity (J Package) DIP*
Poly Die Attach Board
Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width TL/H/9312-11
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

TO-263 (S Package)
Board Mount, Still Air



TL/H/9312-13

*For products with high current ratings (>3A), thermal resistance may be lower. Consult product datasheet for more information.

FIGURE 13. Thermal Resistance (typ.*) for 3-, 5-, and 7-L TO-263 packages mounted on 1 oz. (0.036mm) PC board foil

National Semiconductor

APPENDIX F
How to Get the Right Information From a Data Sheet

Not All Data Sheets Are Created Alike, and False Assumptions Could Cost an Engineer Time and Money

By Robert A. Pease

When a new product arrives in the marketplace, it hopefully will have a good, clear data sheet with it.

The data sheet can show the prospective user how to apply the device, what performance specifications are guaranteed and various typical applications and characteristics. If the data-sheet writer has done a good job, the user can decide if the product will be valuable to him, exactly how well it will be of use to him and what precautions to take to avoid problems.

SPECIFICATIONS

The most important area of a data sheet specifies the characteristics that are guaranteed—and the test conditions that apply when the tests are done. Ideally, all specifications that the users will need will be spelled out clearly. If the product is similar to existing products, one can expect the data sheet to have a format similar to other devices.

But, if there are significant changes and improvements that nobody has seen before, then the writer must clarify what is meant by each specification. Definitions of new phrases or characteristics may even have to be added as an appendix.

For example, when fast-settling operational amplifiers were first introduced, some manufacturers defined settling time as the time after slewing before the output finally enters and stays within the error-band; but other manufacturers included the slewing time in their definition. Because both groups made their definitions clear, the user was unlikely to be confused or misled.

However, the reader ought to be on the alert. In a few cases, the data-sheet writer is playing a specsmanship game, and is trying to show an inferior (to some users) aspect of a product in a light that makes it look superior (which it may be, to a couple of users).

GUARANTEES

When a data sheet specifies a guaranteed minimum value, what does it mean? An assumption might be made that the manufacturer has actually tested that specification and has great confidence that no part could fail that test and still be shipped. Yet that is not always the case.

For instance, in the early days of op amps (20 years ago), the differential-input impedance might have been guaranteed at 1 MΩ—but the manufacturer obviously did not measure the impedance. When a customer insisted, "I have to know how you measure this impedance," it had to be explained that the impedance was not measured, but that the base current was. The correlation between I_b and Z_{in} permitted the substitution of this simple dc test for a rather messy, noisy, hard-to-interpret test.

Every year, for the last 20 years, manufacturers have been trying to explain, with varying success, why they do not measure the Z_{in} *per se*, even though they do guarantee it.

In other cases, the manufacturer may specify a test that can be made only on the die as it is probed on the wafer, but cannot be tested after the die is packaged because that signal is not accessible any longer. To avoid frustrating and confusing the customer, some manufacturers are establishing two classes of guaranteed specifications:

- The tested limit represents a test that cannot be doubted, one that is actually performed directly on 100 percent of the devices, 100 percent of the time.
- The design limit covers other tests that may be indirect, implicit or simply guaranteed by the inherent design of the device, and is unlikely to cause a failure rate (on that test), even as high as one part per thousand.

Why was this distinction made? Not just because customers wanted to know which specifications were guaranteed by testing, but because the quality-assurance group insisted that it was essential to separate the tested guarantees from the design limits so that the AQL (assurance-quality level) could be improved from 0.1 percent to down below 100 ppm.

Some data sheets guarantee characteristics that are quite expensive and difficult to test (even harder than noise) such as long-term drift (20 ppm or 50 ppm over 1,000 hours).

The data sheet may not tell the reader if it is measured, tested or estimated. One manufacturer may perform a 100-percent test, while another states, "Guaranteed by sample testing." This is not a very comforting assurance that a part is good, especially in a critical case where only a long-term test can prove if the device did meet the manufacturer's specification. If in doubt, question the manufacturer.

TYPICALS

Next to a guaranteed specification, there is likely to be another in a column labeled "typical".

It might mean that the manufacturer once actually saw one part as good as that. It could indicate that half the parts are better than that specification, and half will be worse. But it is equally likely to mean that, five years ago, half the parts were better and half worse. It could easily signify that a few parts might be slightly better, and a few parts a lot worse; after all, if the noise of an amplifier is extremely close to the theoretical limit, one cannot expect to find anything much better than that, but there will always be a few noisy ones.

If the specification of interest happens to be the bias current (I_b) of an op amp, a user can expect broad variations. For example, if the specification is 200 nA maximum, there might be many parts where I_b is 40 nA on one batch (where the beta is high), and a month later, many parts where the I_b is 140 nA when the beta is low.

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Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temperature,	
TO-46 Package	−76°F to +356°F
TO-92 Package	−76°F to +300°F

Lead Temp. (Soldering, 4 seconds) *	
TO-46 Package	+300°C
TO-92 Package	+260°C
Specified Operating Temp. Range (Note 2)	
	T_{MIN} to T_{MAX}
LM34, LM34A	−50°F to +300°F
LM34C, LM34CA	−40°F to +230°F
LM34D	+32°F to +212°F

DC Electrical Characteristics (Note 1, **Note 6**)

Parameter	Conditions	LM34A			LM34CA			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	$T_A = +77°F$	±0.4	±1.0		±0.4	±1.0		°F
	$T_A = 0°F$	±0.6			±0.6		±2.0	°F
	$T_A = T_{MAX}$	±0.8	±2.0		±0.8	±2.0		°F
	$T_A = T_{MIN}$	±0.8	±2.0		±0.8		±3.0	°F
Nonlinearity (Note 8)	$T_{MIN} \leq T_A \leq T_{MAX}$	±**0.35**		±**0.7**	±**0.30**		±**0.6**	°F
Sensor Gain (Average Slope)	$T_{MIN} \leq T_A \leq T_{MAX}$	+**10.0**	+**9.9,**		+**10.0**		+**9.9,**	mV/°F, min
			+**10.1**				+**10.1**	mV/°F, max
Load Regulation (Note 3)	$T_A = +77°F$	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \leq T_A \leq T_{MAX}$	±**0.5**		±**3.0**	±**0.5**		±**3.0**	mV/mA
	$0 \leq I_L \leq 1$ mA							
Line Regulation (Note 3)	$T_A = +77°F$	±0.01	±0.05		±0.01	±0.05		mV/V
	$5V \leq V_S \leq 30V$	±**0.02**		±**0.1**	±**0.02**		±**0.1**	mV/V
Quiescent Current (Note 9)	$V_S = +5V, +77°F$	75	90		75	90		μA
	$V_S = +5V$	**131**		**160**	**116**		**139**	μA
	$V_S = +30V, +77°F$	76	92		76	92		μA
	$V_S = +30V$	**132**		**163**	**117**		**142**	μA
Change of Quiescent Current (Note 3)	$4V \leq V_S \leq 30V, +77°F$	+0.5	2.0		0.5	2.0		μA
	$5V \leq V_S \leq 30V$	+**1.0**		**3.0**	**1.0**		**3.0**	μA
Temperature Coefficient of Quiescent Current		+**0.30**		+**0.5**	+**0.30**		+**0.5**	μA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1,* $I_L = 0$	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	$T_j = T_{MAX}$ for 1000 hours	±0.16			±0.16			°F

Note 1: Unless otherwise noted, these specifications apply: $-50°F \leq T_j \leq +300°F$ for the LM34 and LM34A; $-40°F \leq T_j \leq +230°F$ for the LM34C and LM34CA; and $+32°F \leq T_j \leq +212°F$ for the LM34D. $V_S = +5$ Vdc and $I_{LOAD} = 50$ μA in the circuit of *Figure 2;* +6 Vdc for LM34 and LM34A for $230°F \leq T_j \leq 300°F$. These specifications also apply from +5°F to T_{MAX} in the circuit of *Figure 1*.

Note 2: Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

Note 10: Contact factory for availability of LM34CAZ.

* * **Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

A Point-By-Point Look

Let's look a little more closely at the data sheet of the National Semiconductor LM34, which happens to be a temperature sensor.

Note 1 lists the nominal test conditions and test circuits in which all the characteristics are defined. Some additional test conditions are listed in the column "Conditions", but Note 1 helps minimize the clutter.

Note 2 gives the thermal impedance, (which may also be shown in a chart or table).

Note 3 warns that an output impedance test, if done with a long pulse, could cause significant self-heating and thus, error.

Note 6 is intended to show which specs apply at all rated temperatures.

Note 7 is the definition of the "Accuracy" spec, and Note 8 the definition for non-linearity. Note 9 states in what test circuit the quiescent current is defined. Note 10 indicates that one model of the family may not be available at the time of printing (but happens to be available now), and Note 11 is the definition of Absolute Max Ratings.

* Note—the "4 seconds" soldering time is a new standard for plastic packages.

** Note—the wording of Note 11 has been revised—this is the best wording we can devise, and we will use it on all future datasheets.

APPLICATIONS

Another important part of the data sheet is the applications section. It indicates the novel and conventional ways to use a device. Sometimes these applications are just little ideas to tweak a reader's mind. After looking at a couple of applications, one can invent other ideas that are useful. Some applications may be of no real interest or use.

In other cases, an application circuit may be the complete definition of the system's performance; it can be the test circuit in which the specification limits are defined, tested and guaranteed. But, in all other instances, the performance of a typical application circuit is not guaranteed, it is only typical. In many circumstances, the performance may depend on external components and their precision and matching. Some manufacturers have added a phrase to their data sheets:

"Applications for any circuits contained in this document are for illustration purposes only and the manufacturer makes no representation or warranty that such applications will be suitable for the use indicated without further testing or modification."

In the future, manufacturers may find it necessary to add disclaimers of this kind to avoid disappointing users with circuits that work well, much of the time, but cannot be easily guaranteed.

The applications section is also a good place to look for advice on quirks—potential drawbacks or little details that may not be so little when a user wants to know if a device will actually deliver the expected performance.

For example, if a buffer can drive heavy loads and can handle fast signals cleanly (at no load), the maker isn't doing anybody any favors if there is no mention that the distortion goes sky-high if the rated load is applied.

Another example is the application hint for the LF156 family: "Exceeding the negative common-mode limit on either input will cause a reversal of the phase to output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and, thus the amplifier, in a normal operating mode."

That's the kind of information a manufacturer should really give to a data-sheet reader because no one could ever guess it.

Sometimes, a writer slips a quirk into a characteristic curve, but it's wiser to draw attention to it with a line of text. This is because it's better to make the user sad before one gets started, rather than when one goes into production. Conversely, if a user is going to spend more than 10 minutes using a new product, one ought to spend a full five minutes reading the entire data sheet.

FINE PRINT

What other fine print can be found on a data sheet? Sometimes the front page may be marked "advance" or "preliminary." Then on the back page, the fine print may say something such as:

"This data sheet contains preliminary limits and design specifications. Supplemental information will be published at a later date. The manufacturer reserves the right to make changes in the products contained in this document in order to improve design or performance and to supply the best possible products. We also assume no responsibility for the use of any circuits described herein, convey no license under any patent or other right and make no representation that the circuits are free from patent infringement."

In fact, after a device is released to the marketplace in a preliminary status, the engineers love to make small improvements and upgrades in specifications and characteristics, and hate to degrade a specification from its first published value—but occasionally that is necessary.

Another item in the fine print is the manufacturer's telephone number. Usually it is best to refer questions to the local sales representative or field-applications engineer, because they may know the answer or they may be best able to put a questioner in touch with the right person at the factory.

Occasionally, the factory's applications engineers have all the information. Other times, they have to bring in product engineers, test engineers or marketing people. And sometimes the answer can't be generated quickly—data have to be gathered, opinions solidified or policies formulated before the manufacturer can answer the question. Still, the telephone number is the key to getting the factory to help.

ORIGINS OF DATA SHEETS

Of course, historically, most data sheets for a class of products have been closely modeled on the data sheet of the forerunner of that class. The first data sheet was copied to make new versions.

That's the way it happened with the UA709 (the first monolithic op amp) and all its copies, as well as many other similar families of circuits.

Even today, an attempt is made to build on the good things learned from the past and add a few improvements when necessary. But, it's important to have real improvements, not just change for the sake of change.

So, while it's not easy to get the format and everything in it exactly right to please everybody, new data sheets are continually surfacing with new features, applications ideas, specifications and aids for the user. And, if the users complain loudly enough about misleading or inadequate data sheets, they can help lead the way to change data sheets. That's how many of today's improvements came about—through customer demand.

Who writes data sheets? In some cases, a marketing person does the actual writing and engineers do the checking. In other companies, the engineer writes, while marketing people and other engineers check. Sometimes, a committee seems to be doing the writing. None of these ways is necessarily wrong.

For example, one approach might be: The original designer of the product writes the data sheet (inside his head) at the same time the product is designed. The concept here is, if one can't find the proper ingredients for a data sheet—good applications, convenient features for the user and nicely tested specifications as the part is being designed—then maybe it's not a very good product until all those ingredients are completed. Thus, the collection of raw materials for a good data sheet is an integral part of the design of a product. The actual assembly of these materials is an art which can take place later.

WHEN TO WRITE DATA SHEETS

A new product becomes available. The applications engineers start evaluating their application circuits and the test engineers examine their production test equipment.

But how can the users evaluate the new device? They have to have a data sheet—which is still in the process of being written. Every week, as the data sheet writer tries to polish and refine the incipient data sheet, other engineers are reporting, "These spec limits and conditions have to be revised," and, "Those application circuits don't work like we thought they would; we'll have one running in a couple of days." The marketing people insist that the data sheet must be finalized and frozen right away so that they can start printing copies to go out with evaluation samples.

These trying conditions may explain why data sheets always seem to have been thrown together under panic conditions and why they have so many rough spots. Users should be aware of the conflicting requirements: Getting a data sheet "as completely as possible" and "as accurately as possible" is compromised if one wants to get the data sheet "as quickly as possible."

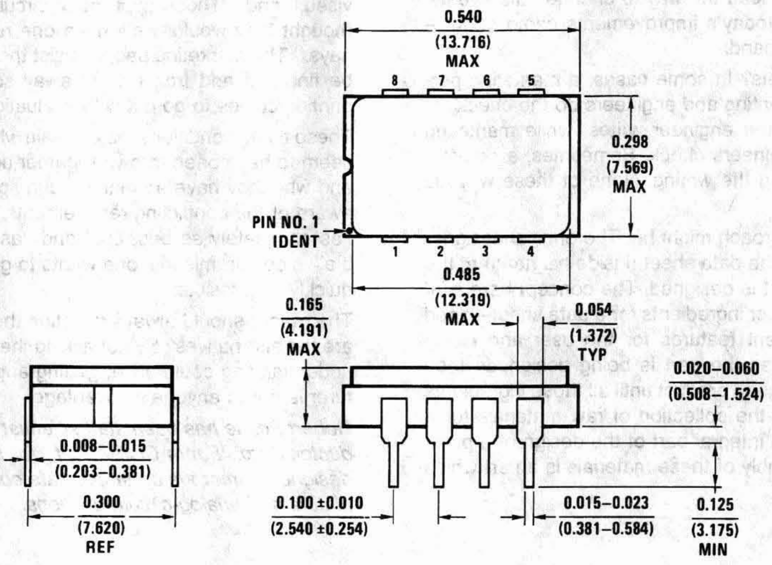
The reader should always question the manufacturer. What are the alternatives? By not asking the right question, a misunderstanding could arise; getting angry with the manufacturer is not to anyone's advantage.

Robert Pease has been staff scientist at National Semiconductor Corp., Santa Clara, Calif., for eleven years. He has designed numerous op amps, data converters, voltage regulators and analog-circuit functions.

National Semiconductor

8 Lead Ceramic Sidebrazed Dual-in-Line Package NS Package Number D08C

All dimensions are in inches (millimeters)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(13.716)
MAX
8
7
6
5
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MAX
PIN NO. 1
IDENT
1
2
3
4
0.485
(12.319)
MAX
0.165
(4.191)
MAX
0.054
(1.372)
TYP
0.020–0.060
(0.508–1.524)
0.008–0.015
(0.203–0.381)
0.300
(7.620)
REF
0.100 ±0.010
(2.540 ±0.254)
0.015–0.023
(0.381–0.584)
0.125
(3.175)
MIN

D08C (REV C)

14 Lead Ceramic Sidebrazed Dual-in-Line Package NS Package Number D14D

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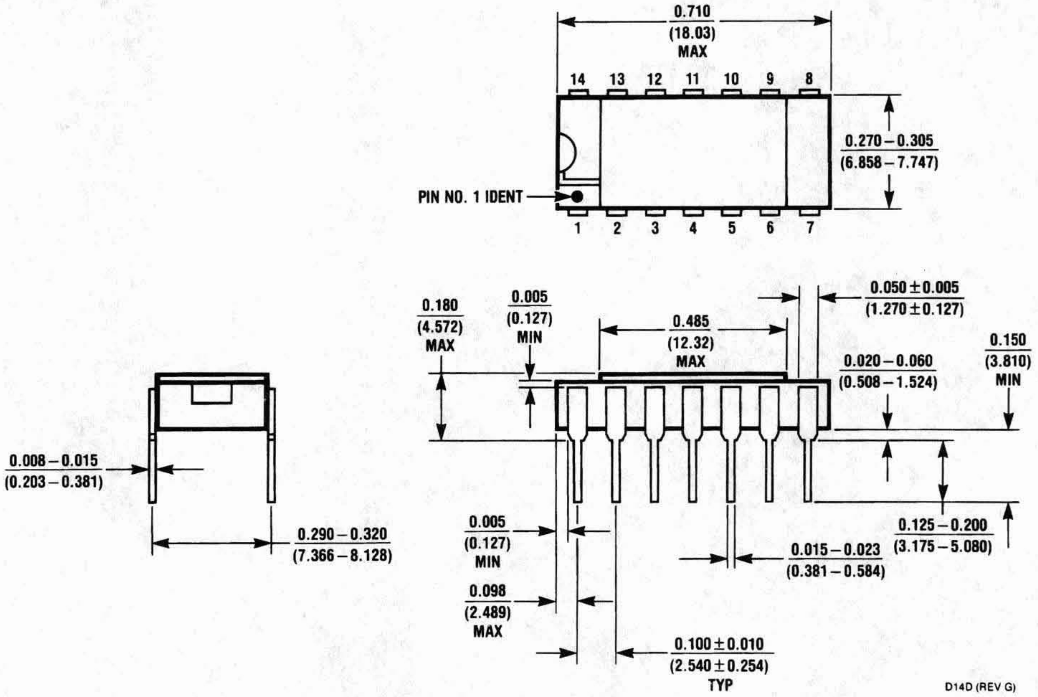
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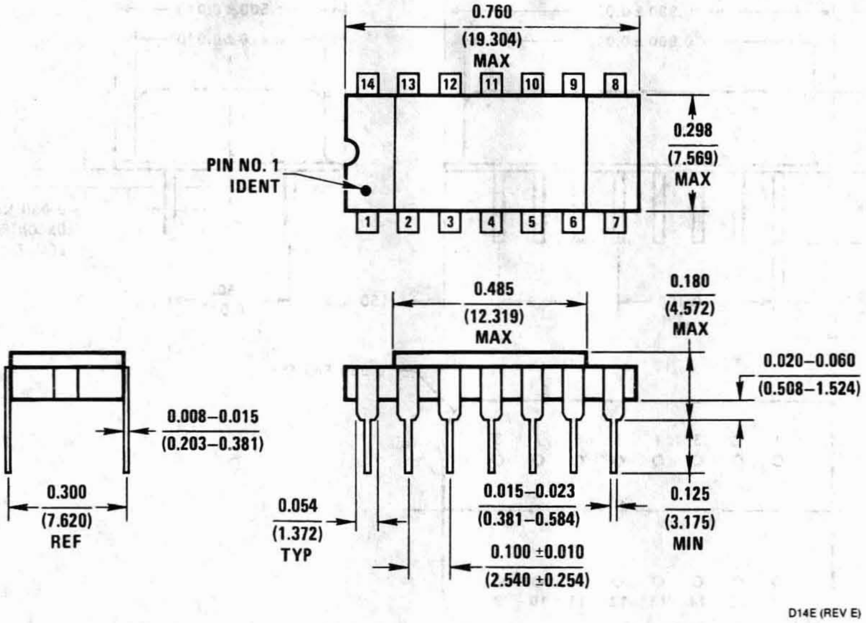
(18.03)
MAX
14
13
12
11
10
9
8
0.270 – 0.305
(6.858 – 7.747)
PIN NO. 1 IDENT
1
2
3
4
5
6
7
0.180
(4.572)
MAX
0.005
(0.127)
MIN
0.485
(12.32)
MAX
0.050 ± 0.005
(1.270 ± 0.127)
0.020 – 0.060
(0.508 – 1.524)
0.150
(3.810)
MIN
0.008 – 0.015
(0.203 – 0.381)
0.290 – 0.320
(7.366 – 8.128)
0.005
(0.127)
MIN
0.125 – 0.200
(3.175 – 5.080)
0.015 – 0.023
(0.381 – 0.584)
0.098
(2.489)
MAX
0.100 ± 0.010
(2.540 ± 0.254)
TYP

D14D (REV G)

14 Lead Hermetic Dual-in-Line Package
NS Package Number D14E

All dimensions are in inches (millimeters)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MAX
0.485
(12.319)
MAX
0.180
(4.572)
MAX
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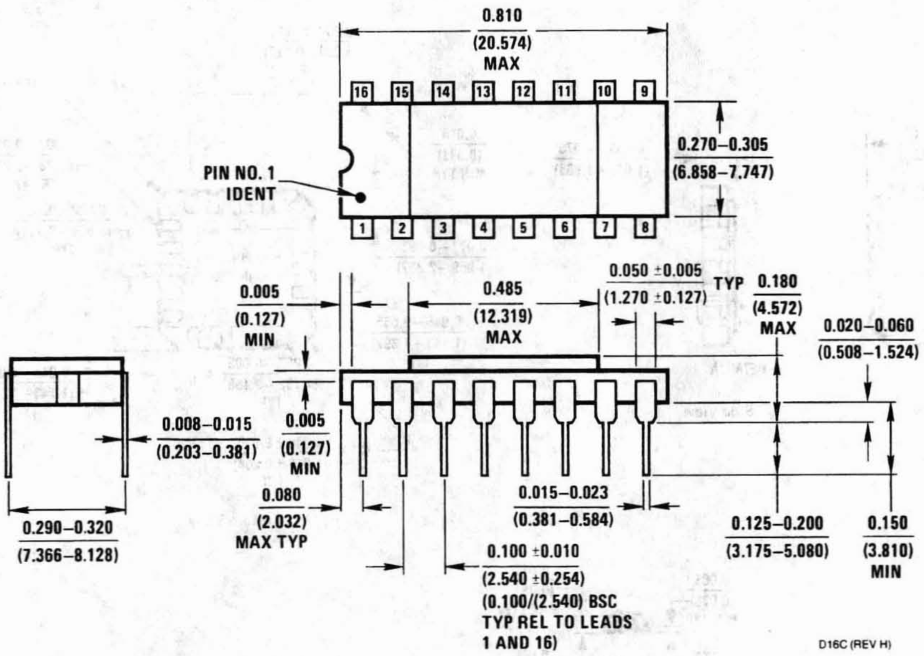
(0.508–1.524)
0.008–0.015
(0.203–0.381)
0.300
(7.620)
REF
0.054
(1.372)
TYP
0.015–0.023
(0.381–0.584)
0.125
(3.175)
MIN
0.100 ±0.010
(2.540 ±0.254)
D14E (REV E)

16 Lead Ceramic Sidebrazed Dual-in-Line Package
NS Package Number D16C

All dimensions are in inches (millimeters)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IDENT
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(6.858–7.747)
0.005
(0.127)
MIN
0.485
(12.319)
MAX
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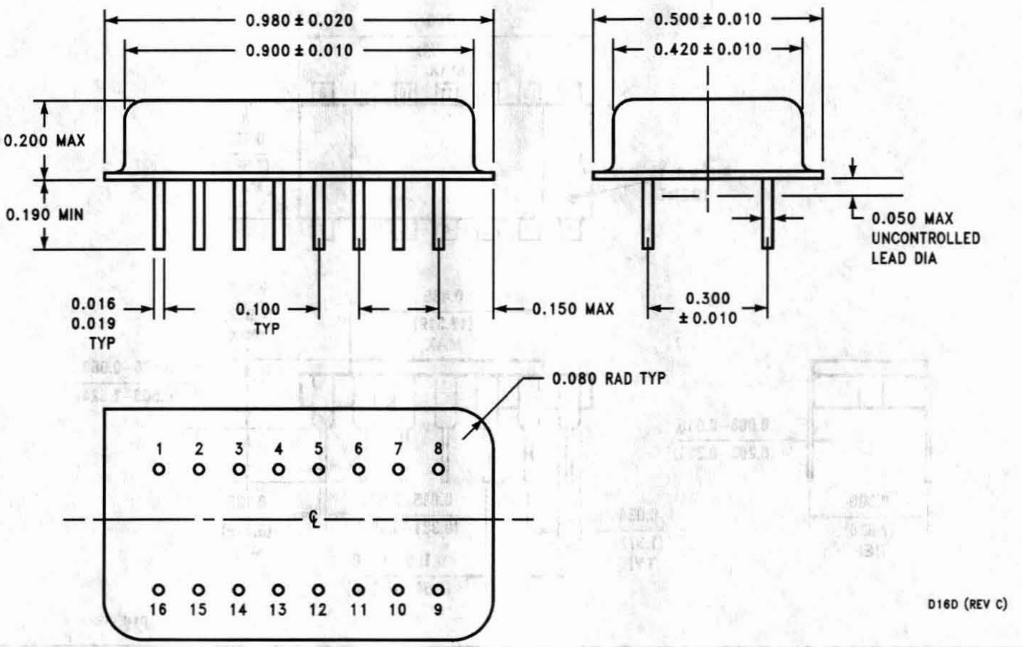
(1.270 ±0.127)
TYP
0.180
(4.572)
MAX
0.020–0.060
(0.508–1.524)
0.008–0.015
(0.203–0.381)
0.005
(0.127)
MIN
0.080
(2.032)
MAX TYP
0.015–0.023
(0.381–0.584)
0.290–0.320
(7.366–8.128)
0.100 ±0.010
(2.540 ±0.254)
(0.100/(2.540) BSC
TYP REL TO LEADS
1 AND 16)
0.125–0.200
(3.175–5.080)
0.150
(3.810)
MIN
D16C (REV H)

16 Lead Hybrid Metal Can Dual-in-Line Package NS Package Number D16D

All dimensions are in inches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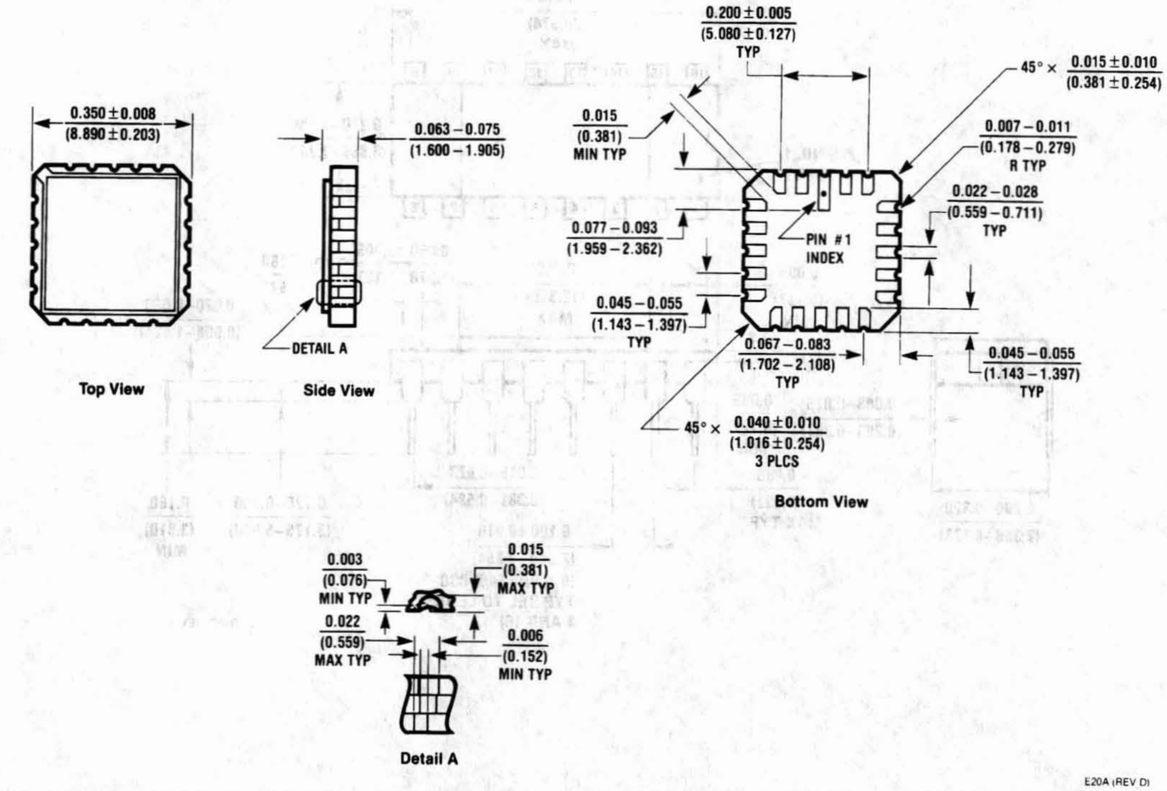
LEAD DIA
0.016
0.019
TYP
0.100
TYP
0.150 MAX
0.300
± 0.010
0.080 RAD TYP
1 2 3 4 5 6 7 8
℄
16 15 14 13 12 11 10 9
D16D (REV C)

20 Lead Ceramic Leadless Chip Carrier, Type C NS Package Number E20A

All dimensions are in inches (millimeters)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(8.890 ± 0.203)
Top View
0.063 – 0.075
(1.600 – 1.905)
DETAIL A
Side View
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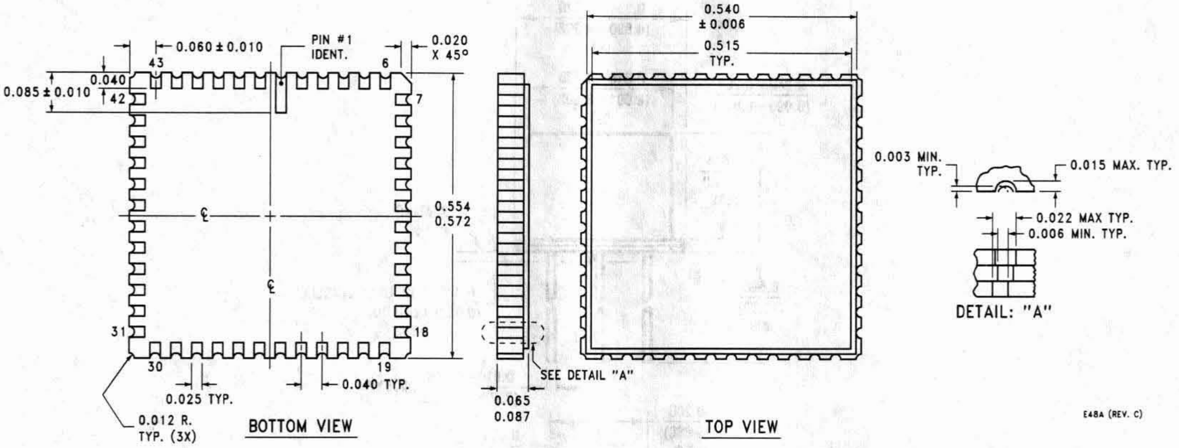
(5.080 ± 0.127)
TYP
45° × 0.015 ± 0.010
(0.381 ± 0.254)
0.015
(0.381)
MIN TYP
0.007 – 0.011
(0.178 – 0.279)
R TYP
0.022 – 0.028
(0.559 – 0.711)
TYP
0.077 – 0.093
(1.959 – 2.362)
PIN #1
INDEX
0.045 – 0.055
(1.143 – 1.397)
TYP
0.067 – 0.083
(1.702 – 2.108)
TYP
0.045 – 0.055
(1.143 – 1.397)
TYP
45° × 0.040 ± 0.010
(1.016 ± 0.254)
3 PLCS
Bottom View
0.003
(0.076)
MIN TYP
0.015
(0.381)
MAX TYP
0.022
(0.559)
MAX TYP
0.006
(0.152)
MIN TYP
Detail A
E20A (REV D)

48 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E48A

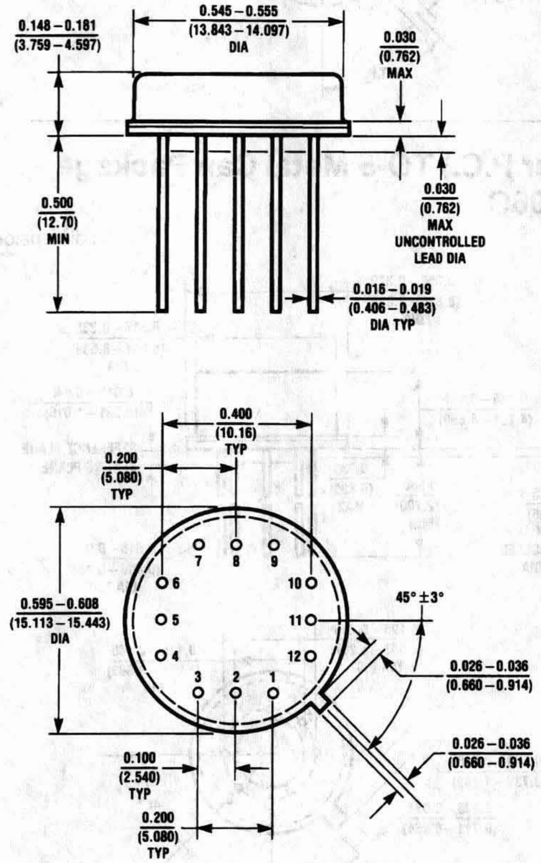
All dimensions are in inches


0.060 ± 0.010
PIN #1
IDENT.
0.020
X 45°
43
6
0.040
42
0.085 ± 0.010
7
℄
℄
0.554
0.572
31
18
30
19
0.025 TYP.
0.040 TYP.
0.012 R.
TYP. (3X)
BOTTOM VIEW
SEE DETAIL "A"
0.065
0.087
0.540
± 0.006
0.515
TYP.
TOP VIEW
0.003 MIN.
TYP.
0.015 MAX. TYP.
0.022 MAX TYP.
0.006 MIN. TYP.
DETAIL: "A"

E48A (REV. C)

12 Lead (0.400″ Square Pattern) TO-8 Metal Can Package
NS Package Number G12B

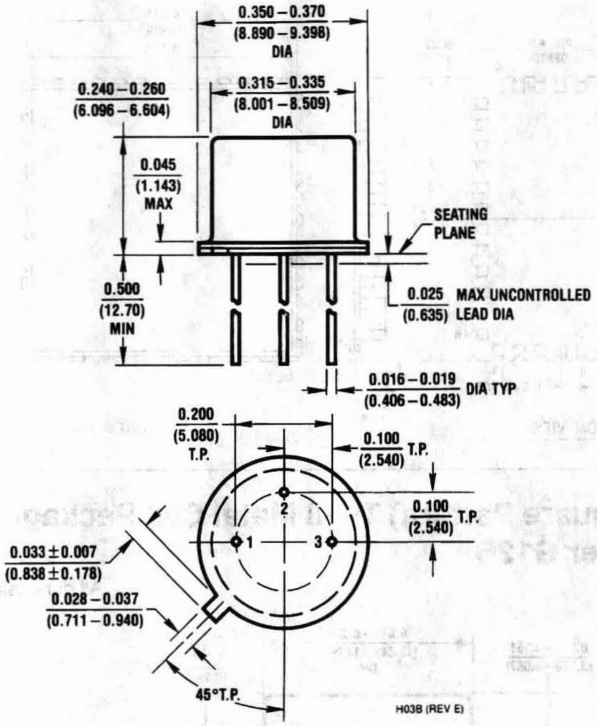
All dimensions are in inches (millimeters)


0.148 – 0.181
(3.759 – 4.597)
0.545 – 0.555
(13.843 – 14.097)
DIA
0.030
(0.762)
MAX
0.500
(12.70)
MIN
0.030
(0.762)
MAX
UNCONTROLLED
LEAD DIA
0.016 – 0.019
(0.406 – 0.483)
DIA TYP
0.400
(10.16)
TYP
0.200
(5.080)
TYP
7
8
9
6
10
5
11
4
12
3
2
1
0.595 – 0.608
(15.113 – 15.443)
DIA
45° ±3°
0.026 – 0.036
(0.660 – 0.914)
0.026 – 0.036
(0.660 – 0.914)
0.100
(2.540)
TYP
0.200
(5.080)
TYP

G12B (REV C)

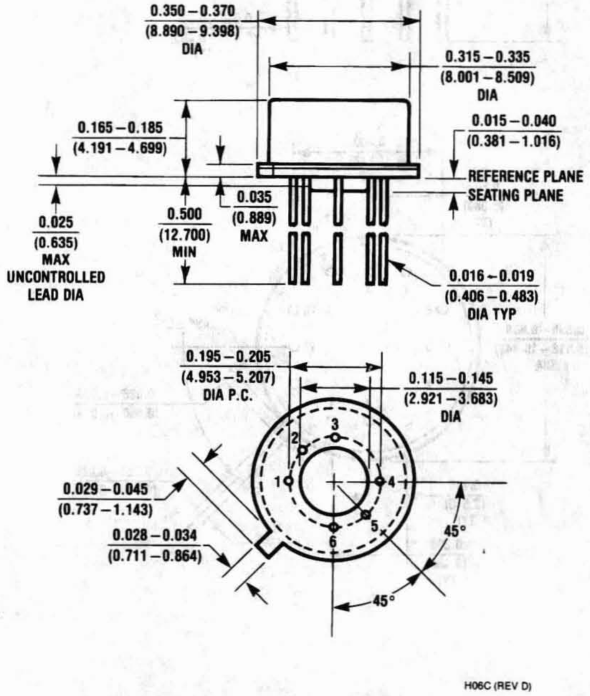
3 Lead (0.200″ Diameter P.C.) TO-39 Metal Can Package, High Profile NS Package Number H03B

All dimensions are in inches (millimeters)


0.350 – 0.370
(8.890 – 9.398)
DIA
0.240 – 0.260
(6.096 – 6.604)
0.315 – 0.335
(8.001 – 8.509)
DIA
0.045
(1.143)
MAX
SEATING PLANE
0.500
(12.70)
MIN
0.025 MAX UNCONTROLLED
(0.635) LEAD DIA
0.016 – 0.019
(0.406 – 0.483) DIA TYP
0.200
(5.080)
T.P.
0.100
(2.540) T.P.
0.100
(2.540) T.P.
2
1
3
0.033 ± 0.007
(0.838 ± 0.178)
0.028 – 0.037
(0.711 – 0.940)
45°T.P.
H03B (REV E)

6 Lead (0.200″ Diameter P.C.) TO-5 Metal Can Package NS Package Number H06C

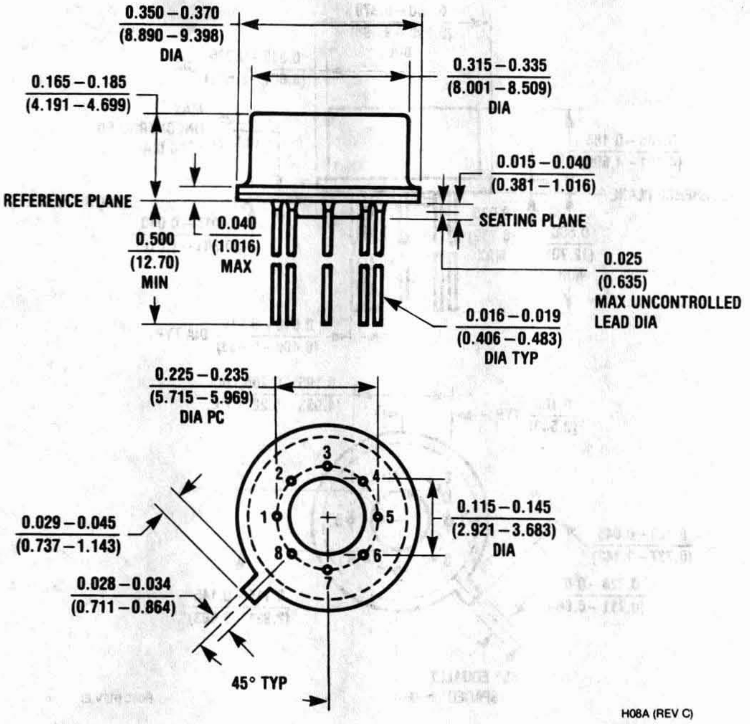
All dimensions are in inches (millimeters)


0.350 – 0.370
(8.890 – 9.398)
DIA
0.315 – 0.335
(8.001 – 8.509)
DIA
0.165 – 0.185
(4.191 – 4.699)
0.015 – 0.040
(0.381 – 1.016)
REFERENCE PLANE
SEATING PLANE
0.035
(0.889)
MAX
0.025
(0.635)
MAX
UNCONTROLLED
LEAD DIA
0.500
(12.700)
MIN
0.016 – 0.019
(0.406 – 0.483)
DIA TYP
0.195 – 0.205
(4.953 – 5.207)
DIA P.C.
0.115 – 0.145
(2.921 – 3.683)
DIA
3
2
1
4
5
6
0.029 – 0.045
(0.737 – 1.143)
0.028 – 0.034
(0.711 – 0.864)
45°
45°

H06C (REV D)

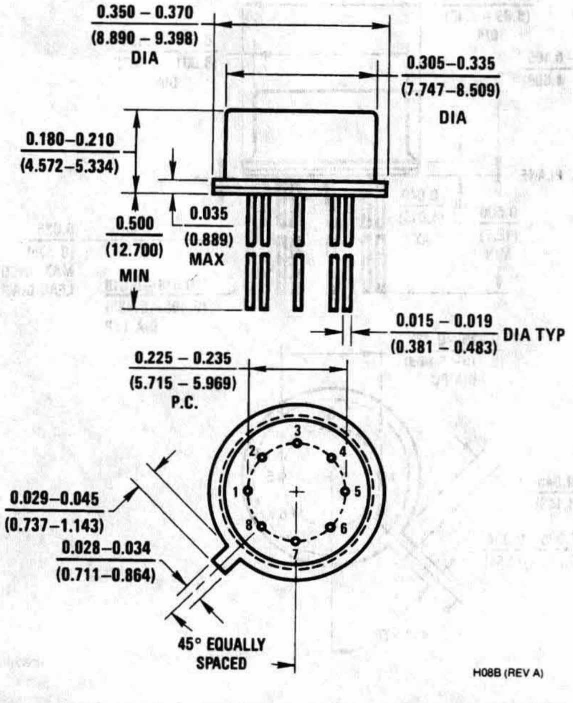
8 Lead (0.230″ Diameter P.C.) TO-5 Metal Can Package
NS Package Number H08A

All dimensions are in inches (millimeters)


0.350 – 0.370
(8.890 – 9.398)
DIA
0.315 – 0.335
(8.001 – 8.509)
DIA
0.165 – 0.185
(4.191 – 4.699)
0.015 – 0.040
(0.381 – 1.016)
REFERENCE PLANE
SEATING PLANE
0.040
(1.016)
MAX
0.500
(12.70)
MIN
0.025
(0.635)
MAX UNCONTROLLED
LEAD DIA
0.016 – 0.019
(0.406 – 0.483)
DIA TYP
0.225 – 0.235
(5.715 – 5.969)
DIA PC
1
2
3
4
5
6
7
8
0.115 – 0.145
(2.921 – 3.683)
DIA
0.029 – 0.045
(0.737 – 1.143)
0.028 – 0.034
(0.711 – 0.864)
45° TYP
H08A (REV C)

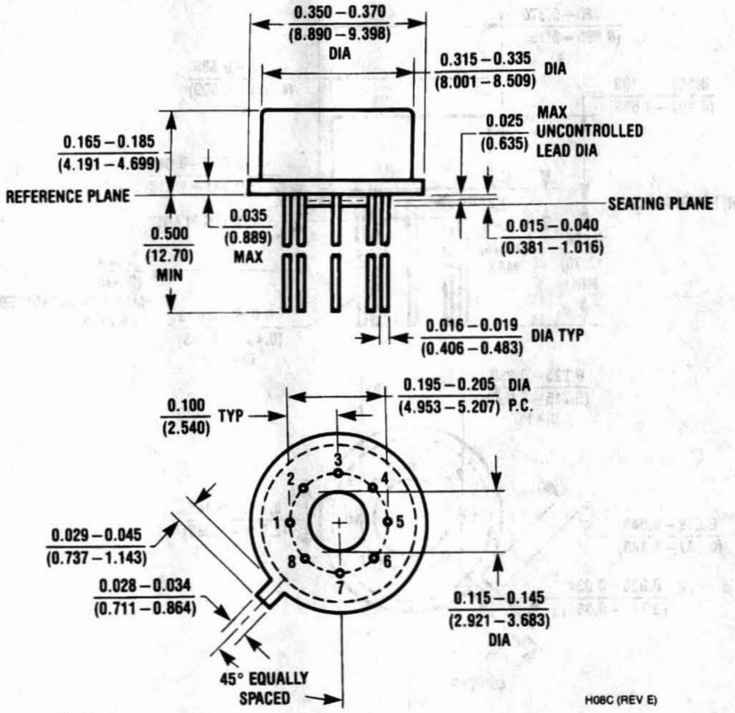
8 Lead (0.230″ Diameter P.C.) Metal Can Package
NS Package Number H08B

All dimensions are in inches (millimeters)


0.350 – 0.370
(8.890 – 9.398)
DIA
0.305–0.335
(7.747–8.509)
DIA
0.180–0.210
(4.572–5.334)
0.035
(0.889)
MAX
0.500
(12.700)
MIN
0.015 – 0.019
(0.381 – 0.483)
DIA TYP
0.225 – 0.235
(5.715 – 5.969)
P.C.
1
2
3
4
5
6
7
8
0.029–0.045
(0.737–1.143)
0.028–0.034
(0.711–0.864)
45° EQUALLY
SPACED
H08B (REV A)

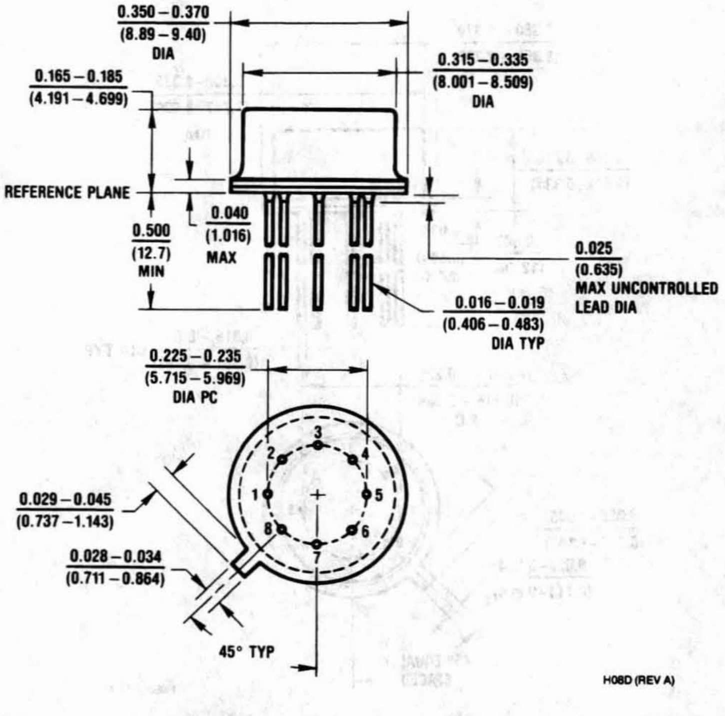
8 Lead (0.200″ Diameter P.C.) TO-5 Metal Can Package NS Package Number H08C

All dimensions are in inches (millimeters)


0.350 – 0.370
(8.890 – 9.398)
DIA
0.315 – 0.335
(8.001 – 8.509)
DIA
0.025
(0.635)
MAX
UNCONTROLLED
LEAD DIA
0.165 – 0.185
(4.191 – 4.699)
REFERENCE PLANE
SEATING PLANE
0.035
(0.889)
MAX
0.500
(12.70)
MIN
0.015 – 0.040
(0.381 – 1.016)
0.016 – 0.019
(0.406 – 0.483)
DIA TYP
0.195 – 0.205
(4.953 – 5.207)
DIA
P.C.
0.100
(2.540)
TYP
1
2
3
4
5
6
7
8
0.029 – 0.045
(0.737 – 1.143)
0.028 – 0.034
(0.711 – 0.864)
0.115 – 0.145
(2.921 – 3.683)
DIA
45° EQUALLY
SPACED
H08C (REV E)

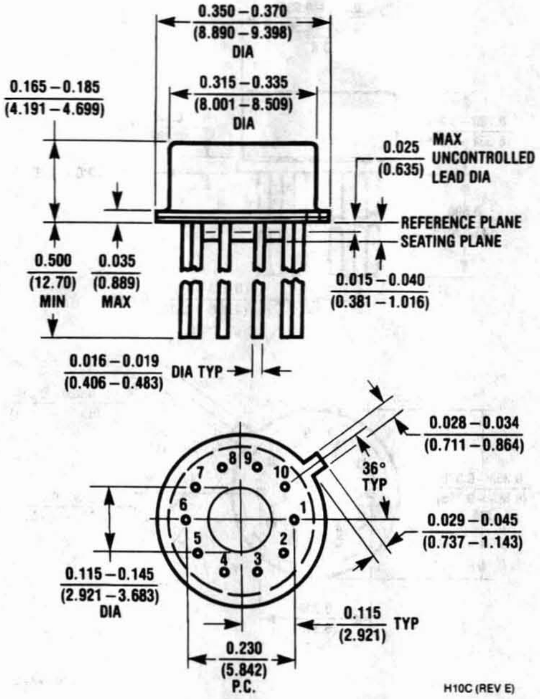
8 Lead (0.230″ Diameter P.C.) Metal Can Package NS Package Number H08D

All dimensions are in inches (millimeters)


0.350 – 0.370
(8.89 – 9.40)
DIA
0.315 – 0.335
(8.001 – 8.509)
DIA
0.165 – 0.185
(4.191 – 4.699)
REFERENCE PLANE
0.040
(1.016)
MAX
0.500
(12.7)
MIN
0.025
(0.635)
MAX UNCONTROLLED
LEAD DIA
0.016 – 0.019
(0.406 – 0.483)
DIA TYP
0.225 – 0.235
(5.715 – 5.969)
DIA PC
1
2
3
4
5
6
7
8
0.029 – 0.045
(0.737 – 1.143)
0.028 – 0.034
(0.711 – 0.864)
45° TYP
H08D (REV A)

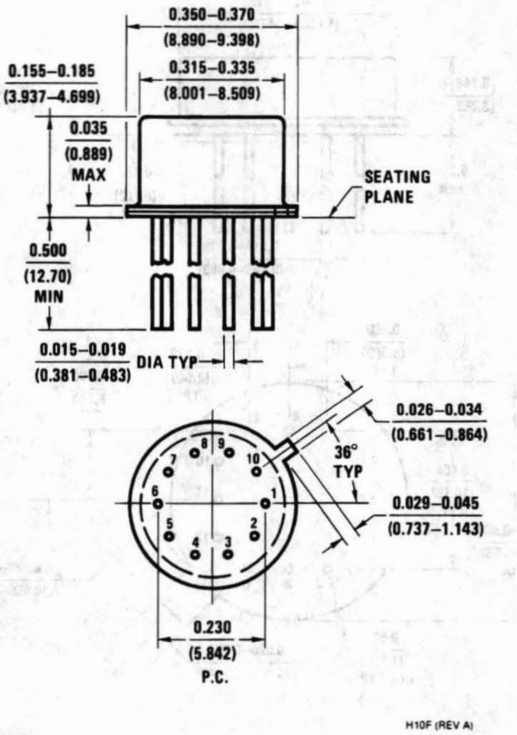
10 Lead (0.230″ Diameter P.C.) TO-5 Metal Can Package NS Package Number H10C

All dimensions are in inches (millimeters)


0.350 – 0.370
(8.890 – 9.398)
DIA
0.165 – 0.185
(4.191 – 4.699)
0.315 – 0.335
(8.001 – 8.509)
DIA
0.025 (0.635) MAX UNCONTROLLED LEAD DIA
REFERENCE PLANE
SEATING PLANE
0.500 (12.70) MIN
0.035 (0.889) MAX
0.015 – 0.040 (0.381 – 1.016)
0.016 – 0.019 (0.406 – 0.483) DIA TYP
0.028 – 0.034 (0.711 – 0.864)
36° TYP
0.029 – 0.045 (0.737 – 1.143)
0.115 – 0.145 (2.921 – 3.683) DIA
0.115 (2.921) TYP
0.230 (5.842) P.C.
1
2
3
4
5
6
7
8
9
10
H10C (REV E)

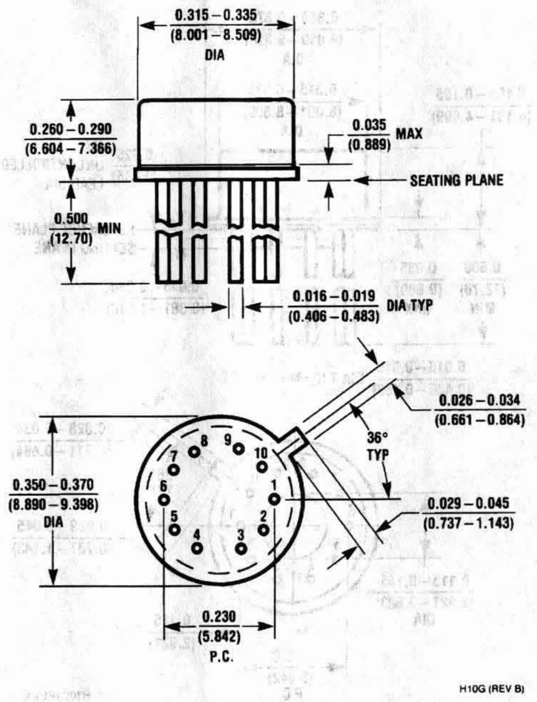
10 Lead (0.230″ Diameter P.C.) Metal Can Package NS Package Number H10F

All dimensions are in inches (millimeters)


0.350–0.370
(8.890–9.398)
0.155–0.185
(3.937–4.699)
0.315–0.335
(8.001–8.509)
0.035 (0.889) MAX
SEATING PLANE
0.500 (12.70) MIN
0.015–0.019 (0.381–0.483) DIA TYP
0.026–0.034 (0.661–0.864)
36° TYP
0.029–0.045 (0.737–1.143)
0.230 (5.842) P.C.
1
2
3
4
5
6
7
8
9
10
H10F (REV A)

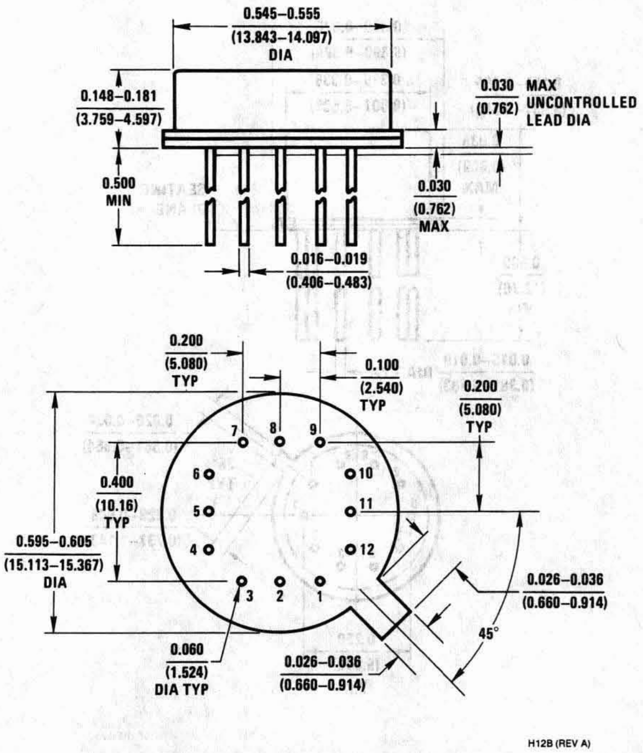
10 Lead (0.230″ Diameter P.C.) Metal Can Package
NS Package Number H10G

All dimensions are in inches (millimeters)


0.315 – 0.335
(8.001 – 8.509)
DIA
0.260 – 0.290
(6.604 – 7.366)
0.035 (0.889) MAX
SEATING PLANE
0.500 (12.70) MIN
0.016 – 0.019 (0.406 – 0.483) DIA TYP
0.026 – 0.034
(0.661 – 0.864)
36° TYP
0.350 – 0.370
(8.890 – 9.398)
DIA
0.029 – 0.045
(0.737 – 1.143)
0.230
(5.842)
P.C.
1
2
3
4
5
6
7
8
9
10
H10G (REV B)

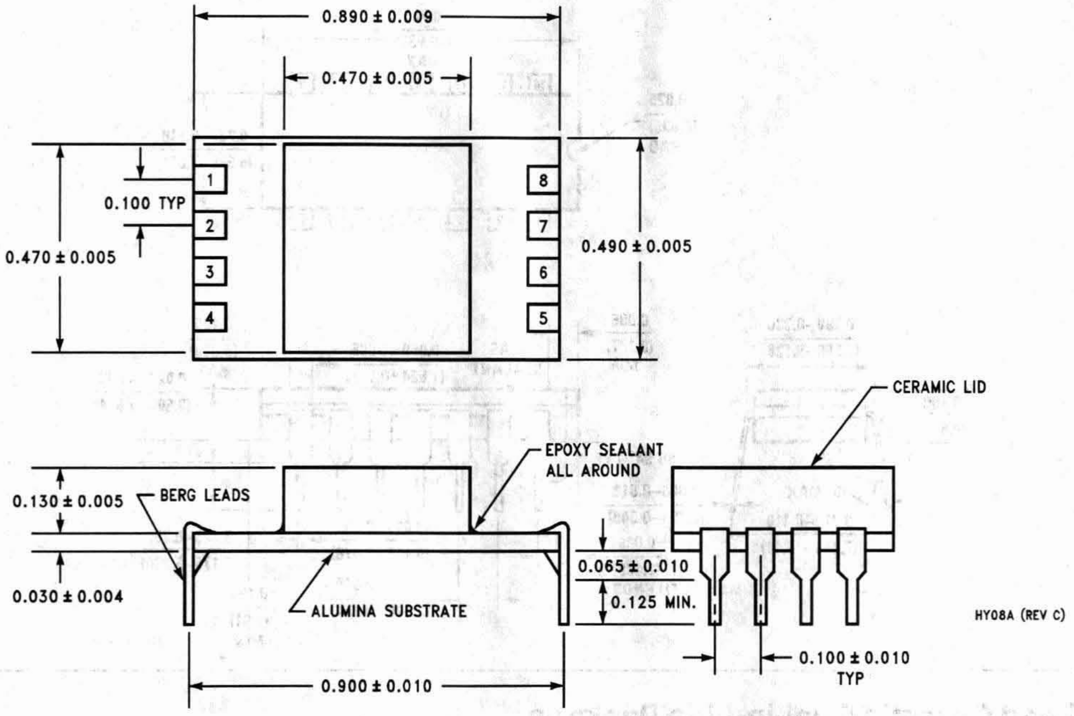
12 Lead (0.400″ Square Pattern) Metal Can Package
NS Package Number H12B

All dimensions are in inches (millimeters)


0.545–0.555
(13.843–14.097)
DIA
0.148–0.181
(3.759–4.597)
0.030 (0.762) MAX UNCONTROLLED LEAD DIA
0.500 MIN
0.030 (0.762) MAX
0.016–0.019
(0.406–0.483)
0.200 (5.080) TYP
0.100 (2.540) TYP
0.200 (5.080) TYP
0.400 (10.16) TYP
0.595–0.605
(15.113–15.367)
DIA
0.026–0.036
(0.660–0.914)
45°
0.060 (1.524) DIA TYP
0.026–0.036
(0.660–0.914)
1
2
3
4
5
6
7
8
9
10
11
12
H12B (REV A)

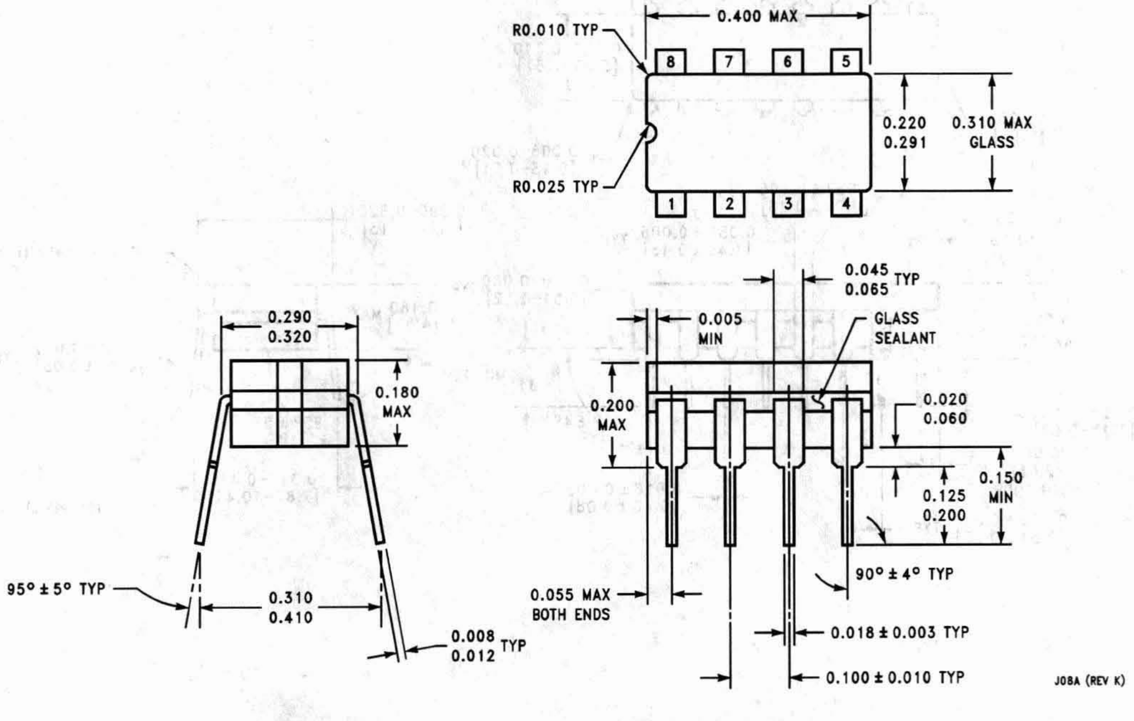
8 Lead Dual-in-Line Hybrid Package
NS Package Number HY08A

All dimensions are in inches


0.890 ± 0.009
0.470 ± 0.005
0.100 TYP
0.470 ± 0.005
0.490 ± 0.005
1
2
3
4
8
7
6
5
CERAMIC LID
EPOXY SEALANT
ALL AROUND
0.130 ± 0.005
BERG LEADS
0.030 ± 0.004
ALUMINA SUBSTRATE
0.065 ± 0.010
0.125 MIN.
0.100 ± 0.010
TYP
0.900 ± 0.010
HY08A (REV C)

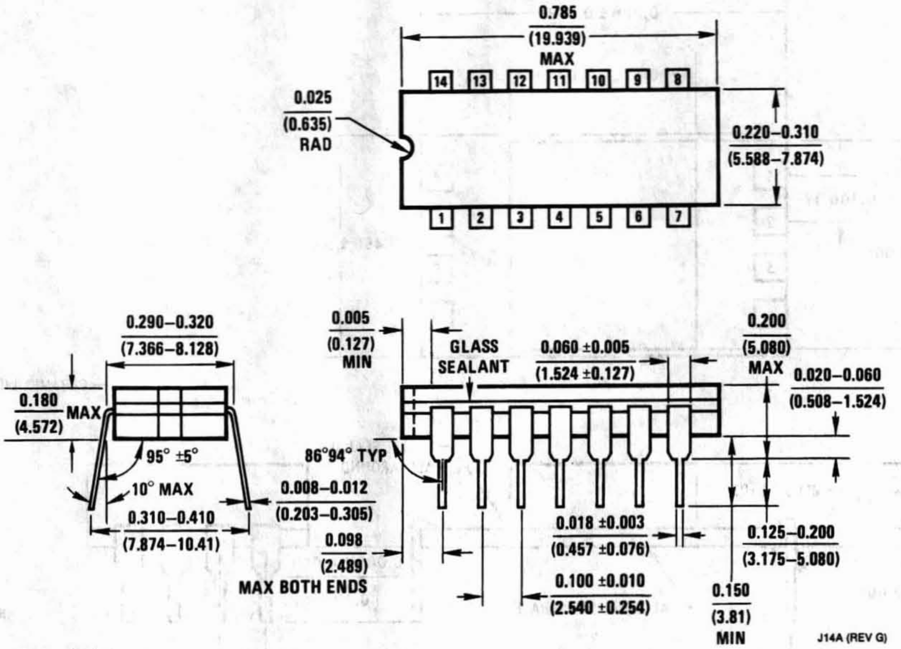
8 Lead Ceramic Dual-in-Line Package
NS Package Number J08A

All dimensions are in inches


R0.010 TYP
0.400 MAX
8
7
6
5
1
2
3
4
0.220
0.291
0.310 MAX
GLASS
R0.025 TYP
0.045
0.065 TYP
0.005
MIN
GLASS
SEALANT
0.290
0.320
0.180
MAX
0.200
MAX
0.020
0.060
0.150
MIN
0.125
0.200
90° ± 4° TYP
95° ± 5° TYP
0.310
0.410
0.008
0.012 TYP
0.055 MAX
BOTH ENDS
0.018 ± 0.003 TYP
0.100 ± 0.010 TYP
J08A (REV K)

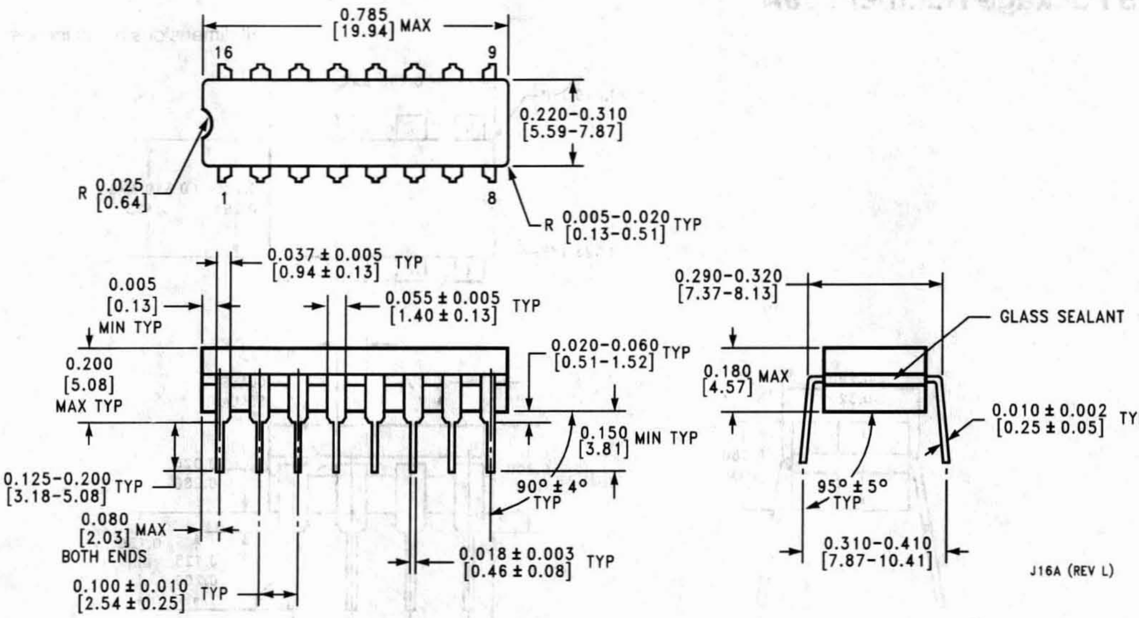
14 Lead Ceramic Dual-in-Line Package
NS Package Number J14A

All dimensions are in inches (millimeters)


0.785
(19.939)
MAX
14
13
12
11
10
9
8
0.025
(0.635)
RAD
0.220–0.310
(5.588–7.874)
1
2
3
4
5
6
7
0.290–0.320
(7.366–8.128)
0.180
(4.572)
MAX
95° ±5°
10° MAX
0.310–0.410
(7.874–10.41)
0.005
(0.127)
MIN
GLASS
SEALANT
0.060 ±0.005
(1.524 ±0.127)
0.200
(5.080)
MAX
0.020–0.060
(0.508–1.524)
86°94° TYP
0.008–0.012
(0.203–0.305)
0.098
(2.489)
MAX BOTH ENDS
0.018 ±0.003
(0.457 ±0.076)
0.100 ±0.010
(2.540 ±0.254)
0.125–0.200
(3.175–5.080)
0.150
(3.81)
MIN
J14A (REV G)

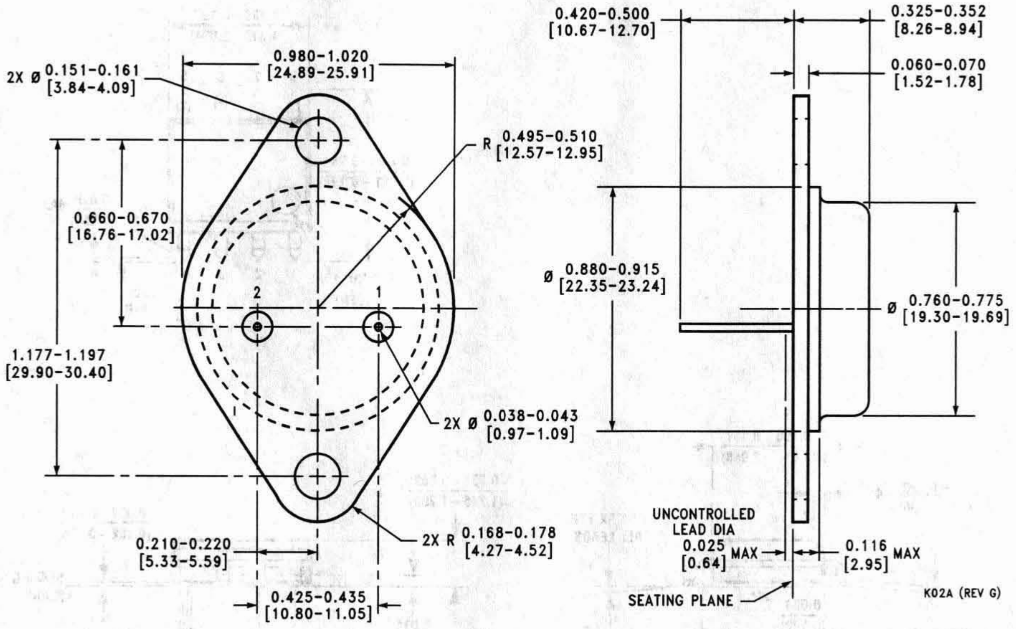
16 Lead Ceramic Dual-in-Line Package
NS Package Number J16A

All dimensions are in inches [millimeters]


0.785
[19.94] MAX
16
9
0.220-0.310
[5.59-7.87]
R 0.025
[0.64]
1
8
R 0.005-0.020
[0.13-0.51] TYP
0.037 ± 0.005
[0.94 ± 0.13] TYP
0.005
[0.13]
MIN TYP
0.055 ± 0.005
[1.40 ± 0.13] TYP
0.200
[5.08]
MAX TYP
0.020-0.060
[0.51-1.52] TYP
0.150
[3.81] MIN TYP
0.125-0.200
[3.18-5.08] TYP
90° ± 4°
TYP
0.080
[2.03] MAX
BOTH ENDS
0.018 ± 0.003
[0.46 ± 0.08] TYP
0.100 ± 0.010
[2.54 ± 0.25] TYP
0.290-0.320
[7.37-8.13]
GLASS SEALANT
0.180
[4.57] MAX
0.010 ± 0.002
[0.25 ± 0.05] TYP
95° ± 5°
TYP
0.310-0.410
[7.87-10.41]
J16A (REV L)

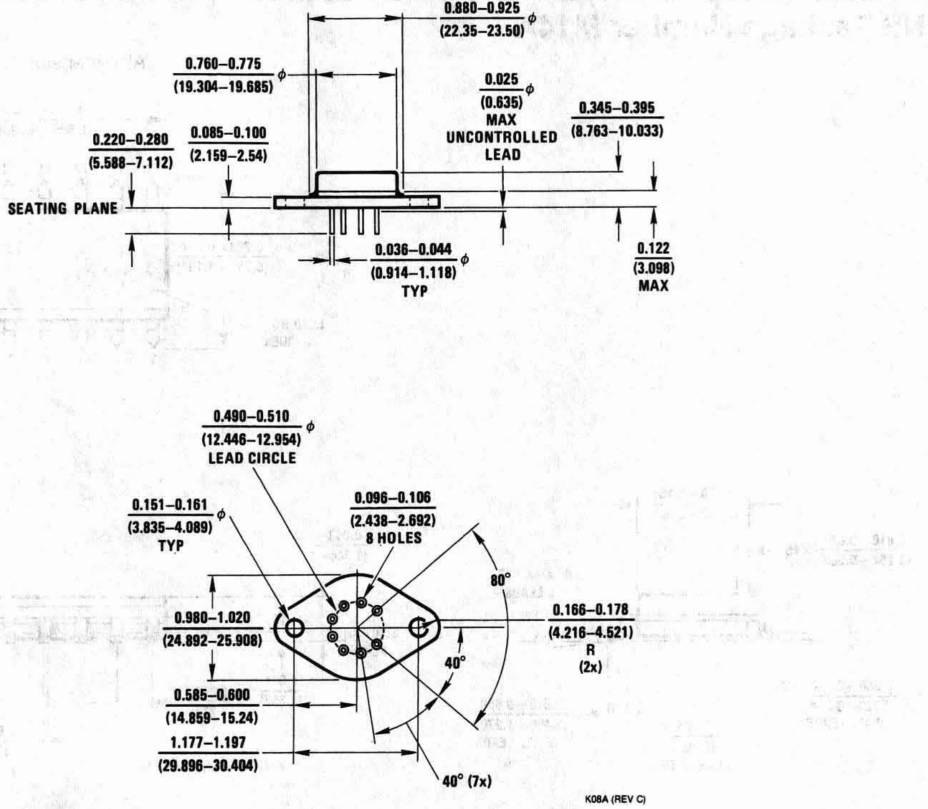
2 Lead TO-3 Metal Can Package
NS Package Number K02A

All dimensions are in inches [millimeters]


0.420-0.500
[10.67-12.70]
0.325-0.352
[8.26-8.94]
0.060-0.070
[1.52-1.78]
2X Ø 0.151-0.161
[3.84-4.09]
0.980-1.020
[24.89-25.91]
R 0.495-0.510
[12.57-12.95]
0.660-0.670
[16.76-17.02]
Ø 0.880-0.915
[22.35-23.24]
2
1
Ø 0.760-0.775
[19.30-19.69]
1.177-1.197
[29.90-30.40]
2X Ø 0.038-0.043
[0.97-1.09]
UNCONTROLLED
LEAD DIA
0.025
[0.64] MAX
0.116
[2.95] MAX
0.210-0.220
[5.33-5.59]
2X R 0.168-0.178
[4.27-4.52]
0.425-0.435
[10.80-11.05]
SEATING PLANE
K02A (REV G)

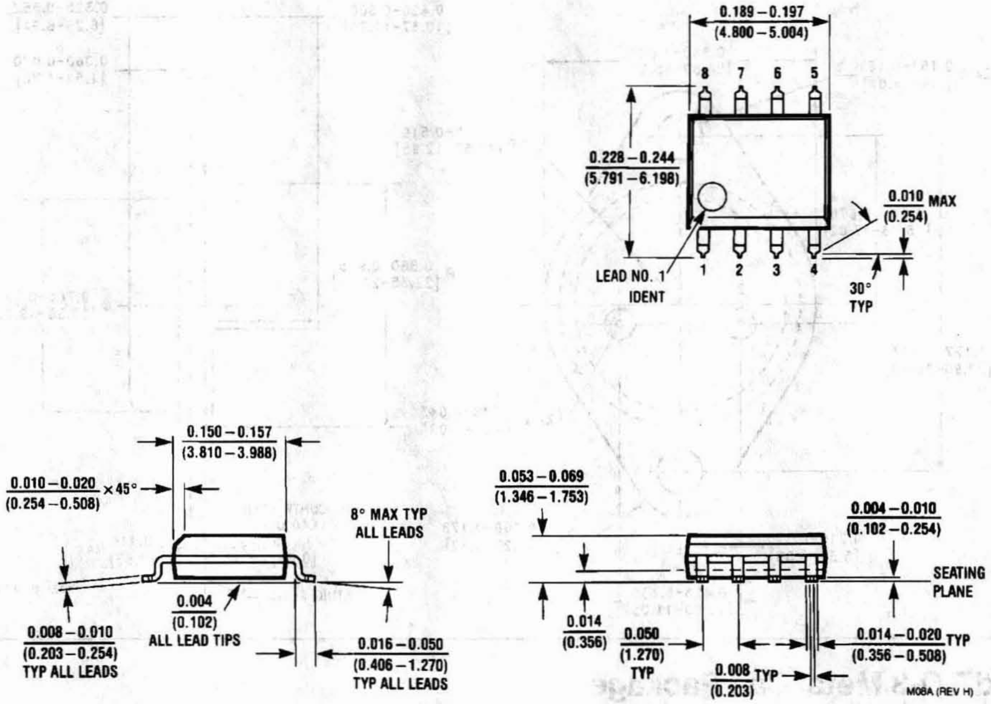
8 Lead TO-3 Metal Can Package
NS Package Number K08A

All dimensions are in inches (millimeters)


0.880–0.925 ϕ
(22.35–23.50)
0.760–0.775 ϕ
(19.304–19.685)
0.025 ϕ
(0.635)
MAX
UNCONTROLLED
LEAD
0.345–0.395
(8.763–10.033)
0.220–0.280
(5.588–7.112)
0.085–0.100
(2.159–2.54)
SEATING PLANE
0.036–0.044 ϕ
(0.914–1.118)
TYP
0.122
(3.098)
MAX
0.490–0.510 ϕ
(12.446–12.954)
LEAD CIRCLE
0.151–0.161 ϕ
(3.835–4.089)
TYP
0.096–0.106
(2.438–2.692)
8 HOLES
80°
0.980–1.020
(24.892–25.908)
0.166–0.178
(4.216–4.521)
R
(2x)
40°
0.585–0.600
(14.859–15.24)
1.177–1.197
(29.896–30.404)
40° (7x)
K08A (REV C)

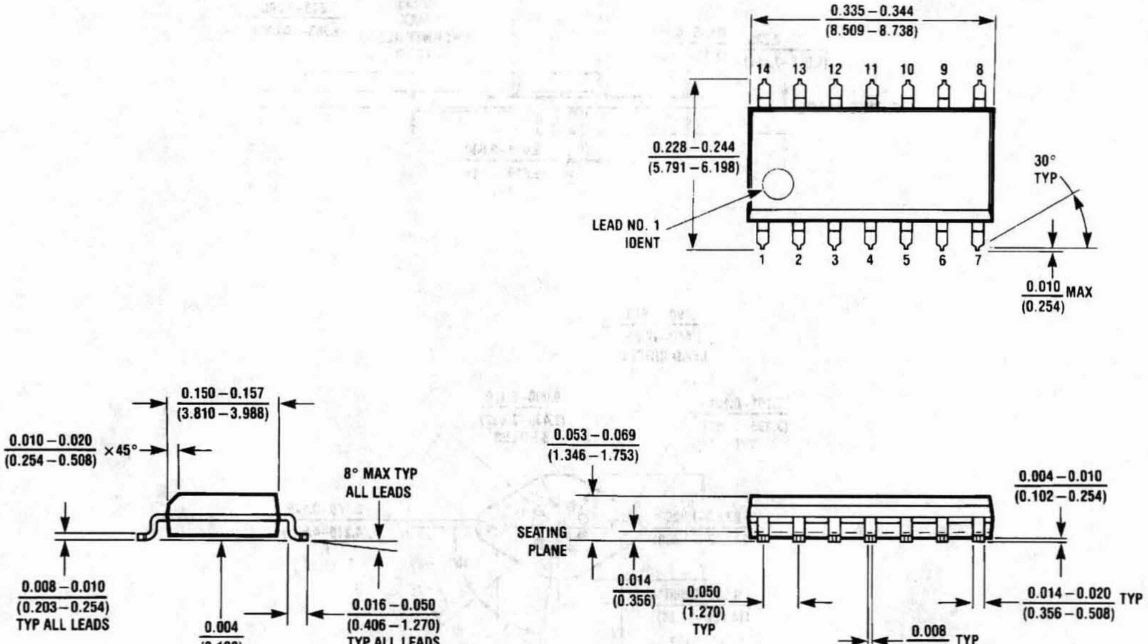
8 Lead (0.150″ Wide) Molded Small Outline Package, JEDEC NS Package Number M08A

All dimensions are in inches (millimeters)


0.189 – 0.197
(4.800 – 5.004)
8 7 6 5
0.228 – 0.244
(5.791 – 6.198)
0.010 MAX
(0.254)
LEAD NO. 1
IDENT
1 2 3 4
30°
TYP
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508)
× 45°
8° MAX TYP
ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.014 – 0.020 TYP
(0.356 – 0.508)
0.008 TYP
(0.203)
M08A (REV H)

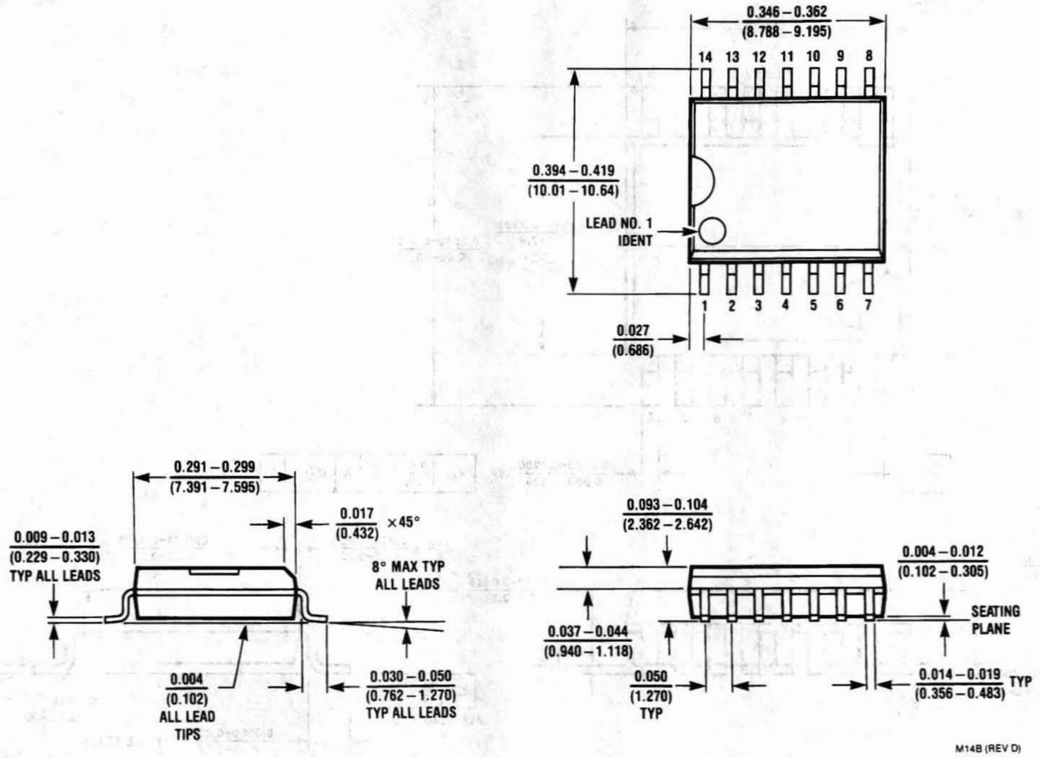
14 Lead (0.150″ Wide) Molded Small Outline Package, JEDEC NS Package Number M14A

All dimensions are in inches (millimeters)


0.335 – 0.344
(8.509 – 8.738)
14 13 12 11 10 9 8
0.228 – 0.244
(5.791 – 6.198)
30°
TYP
LEAD NO. 1
IDENT
1 2 3 4 5 6 7
0.010 MAX
(0.254)
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508)
× 45°
8° MAX TYP
ALL LEADS
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.014 – 0.020 TYP
(0.356 – 0.508)
0.008 TYP
(0.203)
M14A (REV H)

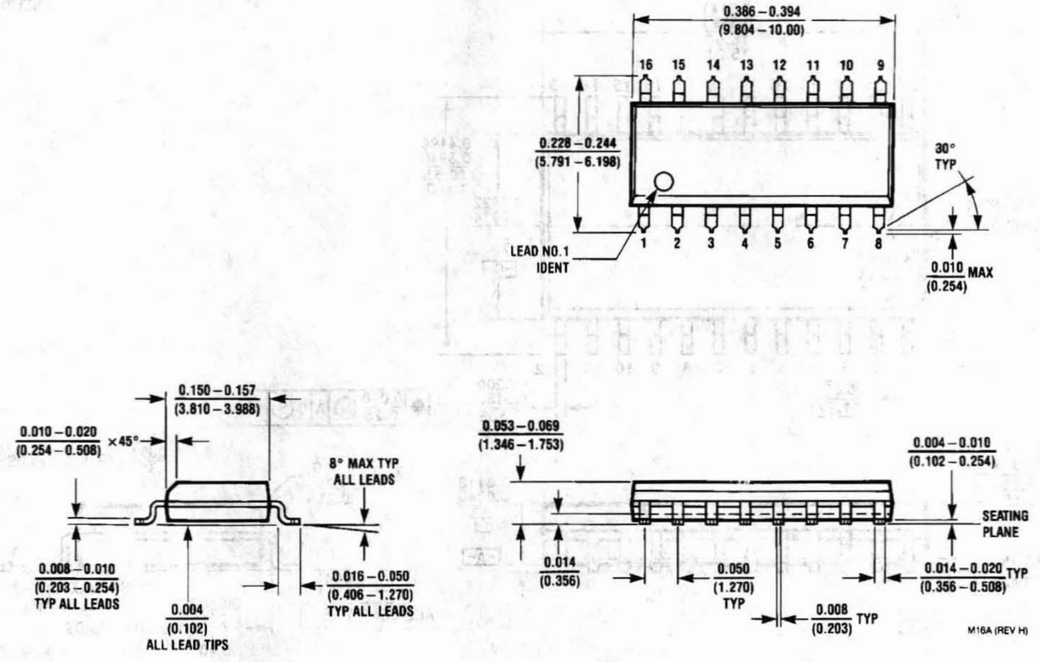
14 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14B

All dimensions are in inches (millimeters)


0.346 – 0.362
(8.788 – 9.195)
14 13 12 11 10 9 8
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432) ×45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
8° MAX TYP
ALL LEADS
0.004
(0.102)
ALL LEAD
TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
SEATING
PLANE
0.037 – 0.044
(0.940 – 1.118)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483) TYP
M14B (REV D)

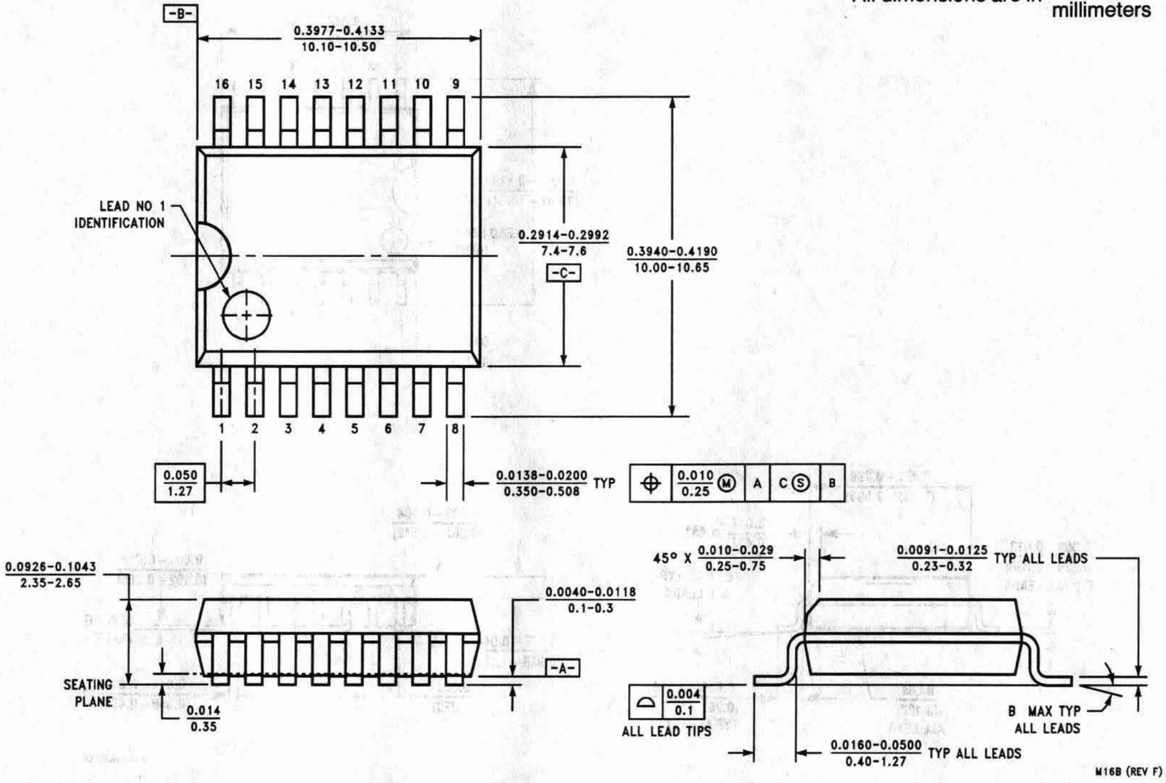
16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A

All dimensions are in inches (millimeters)


0.386 – 0.394
(9.804 – 10.00)
16 15 14 13 12 11 10 9
0.228 – 0.244
(5.791 – 6.198)
30°
TYP
LEAD NO. 1
IDENT
1 2 3 4 5 6 7 8
0.010 MAX
(0.254)
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508) ×45°
8° MAX TYP
ALL LEADS
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.008
(0.203) TYP
0.014 – 0.020
(0.356 – 0.508) TYP
M16A (REV H)

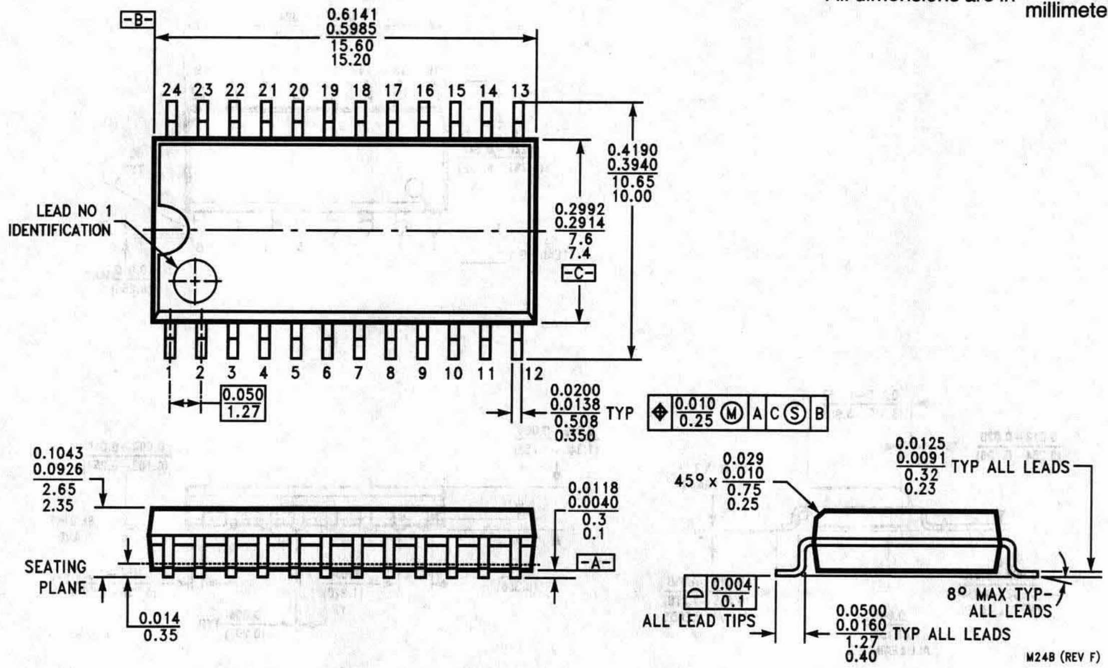
16 Lead (0.300″ Wide) Molded Small Outline Package, JEDEC NS Package Number M16B

All dimensions are in $\frac{\text{inches}}{\text{millimeters}}$


-B-
0.3977-0.4133
10.10-10.50
16 15 14 13 12 11 10 9
LEAD NO 1 IDENTIFICATION
0.2914-0.2992
7.4-7.6
-C-
0.3940-0.4190
10.00-10.65
1 2 3 4 5 6 7 8
0.050
1.27
0.0138-0.0200
0.350-0.508
TYP
0.010 M A C S B
0.25
0.0926-0.1043
2.35-2.65
0.0040-0.0118
0.1-0.3
-A-
SEATING PLANE
0.014
0.35
45° X 0.010-0.029
0.25-0.75
0.0091-0.0125
0.23-0.32
TYP ALL LEADS
0.004
0.1
ALL LEAD TIPS
8° MAX TYP
ALL LEADS
0.0160-0.0500
0.40-1.27
TYP ALL LEADS
M16B (REV F)

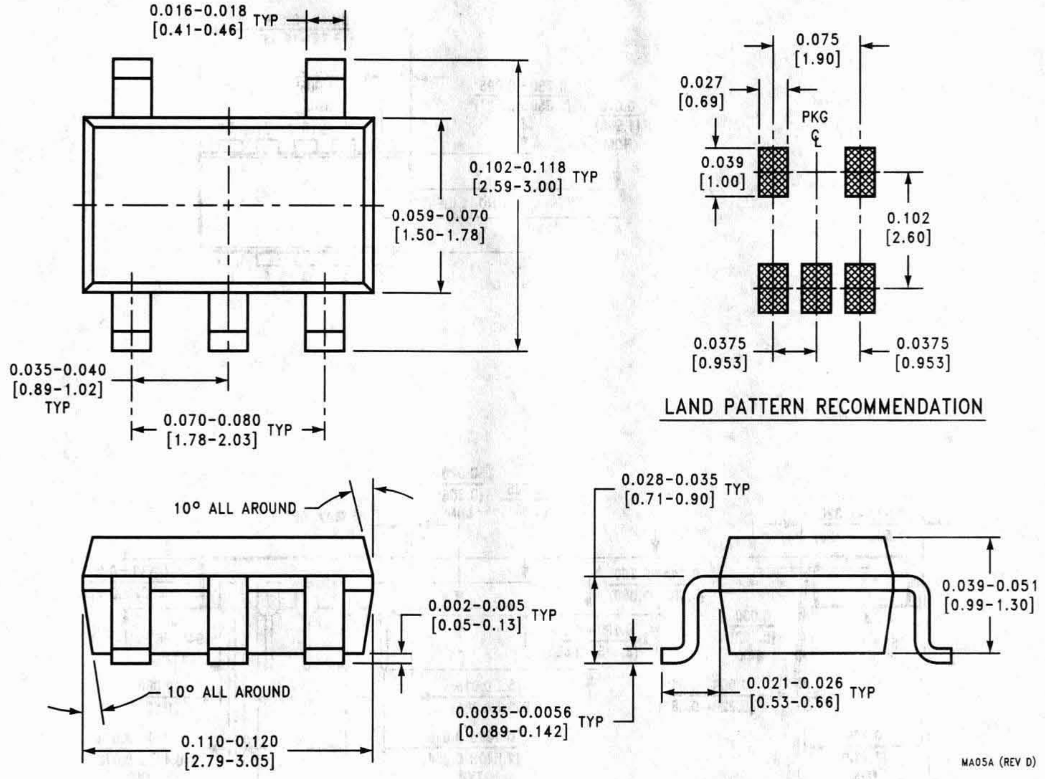
24 Lead (0.300″ Wide) Molded Small Outline Package, JEDEC NS Package Number M24B

All dimensions are in $\frac{\text{inches}}{\text{millimeters}}$


-B-
0.6141
0.5985
15.60
15.20
24 23 22 21 20 19 18 17 16 15 14 13
0.4190
0.3940
10.65
10.00
LEAD NO 1 IDENTIFICATION
0.2992
0.2914
7.6
7.4
-C-
1 2 3 4 5 6 7 8 9 10 11 12
0.050
1.27
0.0200
0.0138
0.508
0.350
TYP
0.010 M A C S B
0.25
0.1043
0.0926
2.65
2.35
0.0118
0.0040
0.3
0.1
-A-
SEATING PLANE
0.014
0.35
45° x 0.029
0.010
0.75
0.25
0.0125
0.0091
0.32
0.23
TYP ALL LEADS
0.004
0.1
ALL LEAD TIPS
8° MAX TYP
ALL LEADS
0.0500
0.0160
1.27
0.40
TYP ALL LEADS
M24B (REV F)

5 Lead Molded SOT-23-5
NS Package Number MA05A

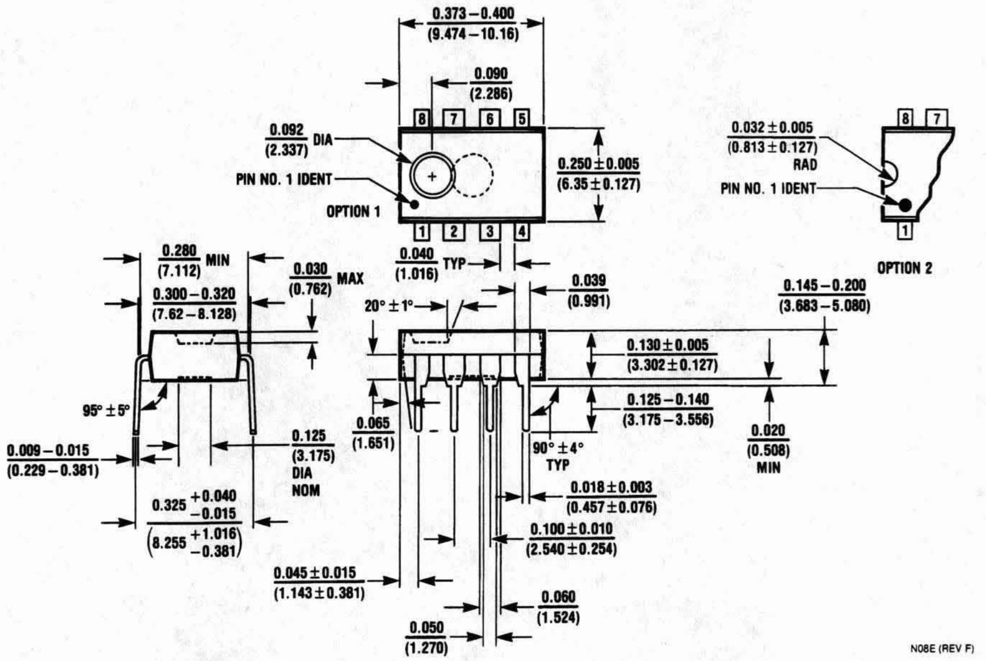
All dimensions are in inches [millimeters]


0.016-0.018 [0.41-0.46] TYP
0.102-0.118 [2.59-3.00] TYP
0.059-0.070 [1.50-1.78]
0.035-0.040 [0.89-1.02] TYP
0.070-0.080 [1.78-2.03] TYP
0.075 [1.90]
0.027 [0.69]
PKG ℄
0.039 [1.00]
0.102 [2.60]
0.0375 [0.953]
0.0375 [0.953]
LAND PATTERN RECOMMENDATION
10° ALL AROUND
0.002-0.005 [0.05-0.13] TYP
10° ALL AROUND
0.110-0.120 [2.79-3.05]
0.0035-0.0056 [0.089-0.142] TYP
0.028-0.035 [0.71-0.90] TYP
0.039-0.051 [0.99-1.30]
0.021-0.026 [0.53-0.66] TYP

MA05A (REV D)

8 Lead (0.300″ Wide) Molded Dual-in-Line Package
NS Package Number N08E

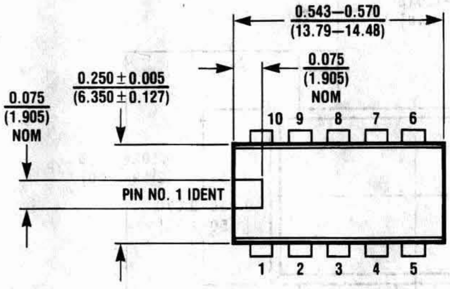
All dimensions are in inches (millimeters)

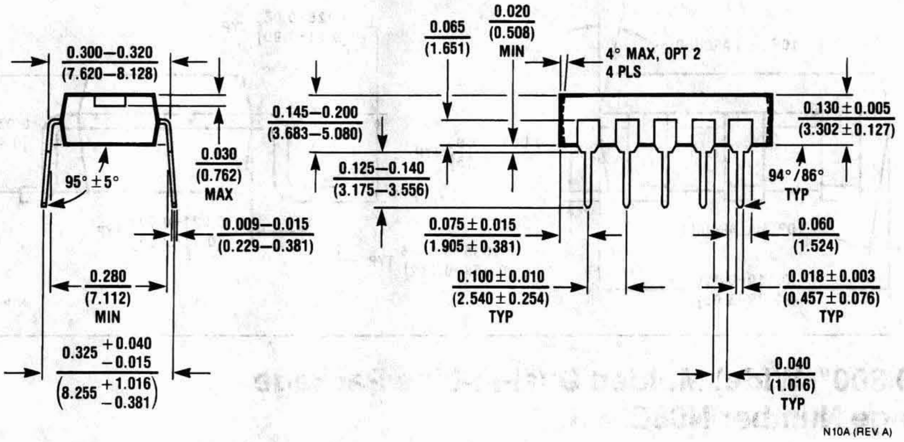

0.373 – 0.400 (9.474 – 10.16)
0.090 (2.286)
8 7 6 5
0.092 (2.337) DIA
PIN NO. 1 IDENT
OPTION 1
0.250 ± 0.005 (6.35 ± 0.127)
1 2 3 4
0.032 ± 0.005 (0.813 ± 0.127) RAD
PIN NO. 1 IDENT
8 7
1
OPTION 2
0.280 (7.112) MIN
0.300 – 0.320 (7.62 – 8.128)
0.030 (0.762) MAX
0.040 (1.016) TYP
0.039 (0.991)
20° ± 1°
0.145 – 0.200 (3.683 – 5.080)
0.130 ± 0.005 (3.302 ± 0.127)
0.125 – 0.140 (3.175 – 3.556)
0.020 (0.508) MIN
95° ± 5°
0.009 – 0.015 (0.229 – 0.381)
0.125 (3.175) DIA NOM
0.065 (1.651)
90° ± 4° TYP
0.325 +0.040 −0.015 (8.255 +1.016 −0.381)
0.018 ± 0.003 (0.457 ± 0.076)
0.100 ± 0.010 (2.540 ± 0.254)
0.045 ± 0.015 (1.143 ± 0.381)
0.060 (1.524)
0.050 (1.270)

N08E (REV F)

10 Lead Molded Dual-in-Line Package NS Package Number N10A

All dimensions are in inches (millimeters)

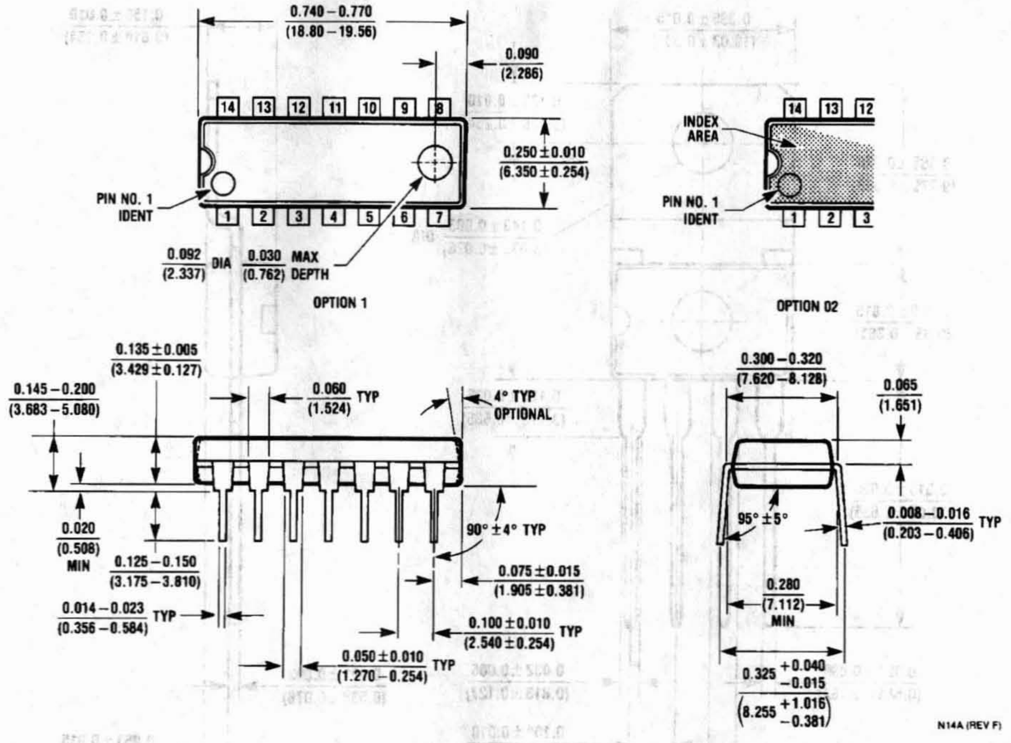

0.543—0.570
(13.79—14.48)
0.075
(1.905)
NOM
0.250 ± 0.005
(6.350 ± 0.127)
0.075
(1.905)
NOM
10 9 8 7 6
PIN NO. 1 IDENT
1 2 3 4 5


0.300—0.320
(7.620—8.128)
95° ± 5°
0.030
(0.762)
MAX
0.009—0.015
(0.229—0.381)
0.280
(7.112)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.145—0.200
(3.683—5.080)
0.125—0.140
(3.175—3.556)
0.065
(1.651)
0.020
(0.508)
MIN
4° MAX, OPT 2
4 PLS
0.130 ± 0.005
(3.302 ± 0.127)
94°/86°
TYP
0.075 ± 0.015
(1.905 ± 0.381)
0.060
(1.524)
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.018 ± 0.003
(0.457 ± 0.076)
TYP
0.040
(1.016)
TYP

N10A (REV A)

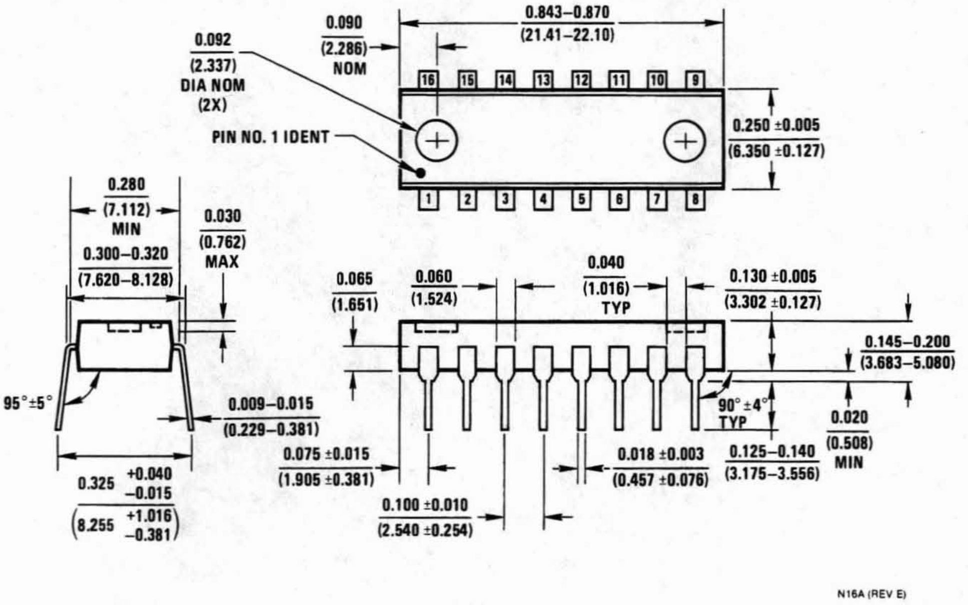
14 Lead (0.300″ Wide) Molded Dual-in-Line Package NS Package Number N14A

All dimensions are in inches (millimeters)


0.740 – 0.770
(18.80 – 19.56)
0.090
(2.286)
14
13
12
11
10
9
8
0.250 ± 0.010
(6.350 ± 0.254)
PIN NO. 1
IDENT
1
2
3
4
5
6
7
0.092
(2.337)
DIA
0.030 MAX
(0.762) DEPTH
OPTION 1
INDEX
AREA
14
13
12
PIN NO. 1
IDENT
1
2
3
OPTION 02
0.135 ± 0.005
(3.429 ± 0.127)
0.145 – 0.200
(3.683 – 5.080)
0.060
(1.524)
TYP
4° TYP
OPTIONAL
0.020
(0.508)
MIN
0.125 – 0.150
(3.175 – 3.810)
0.014 – 0.023
(0.356 – 0.584)
TYP
90° ± 4° TYP
0.075 ± 0.015
(1.905 ± 0.381)
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.050 ± 0.010
(1.270 – 0.254)
TYP
0.300 – 0.320
(7.620 – 8.128)
0.065
(1.651)
95° ± 5°
0.008 – 0.016
(0.203 – 0.406)
TYP
0.280
(7.112)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
N14A (REV F)

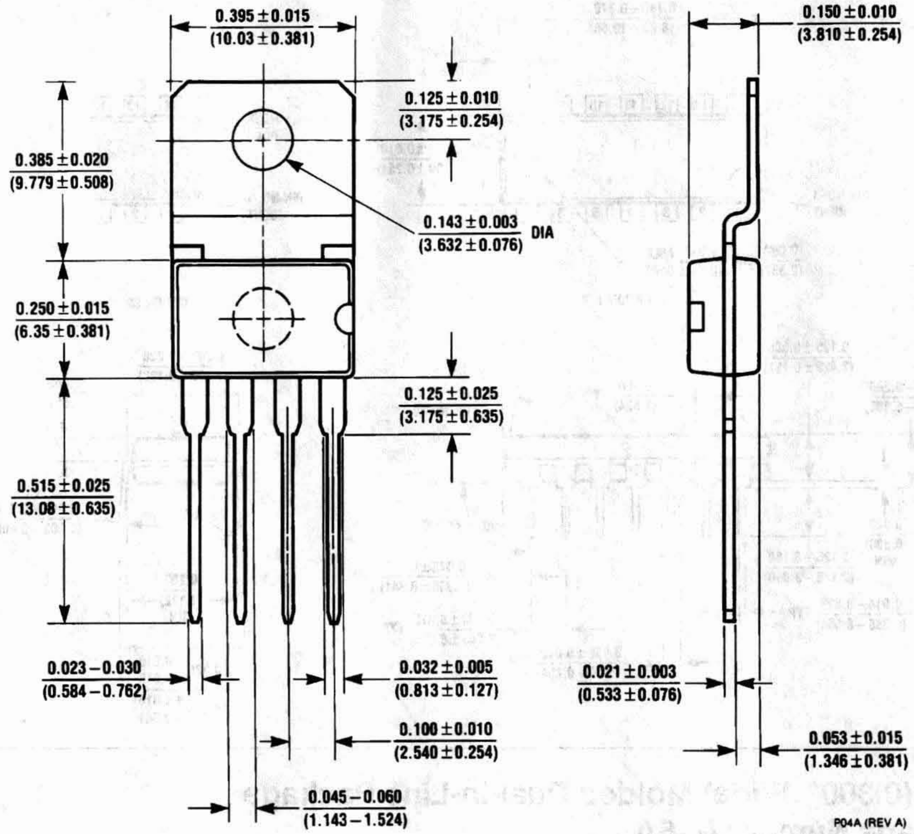
16 Lead (0.300″ Wide) Molded Dual-in-Line Package NS Package Number N16A

All dimensions are in inches (millimeters)


0.843–0.870
(21.41–22.10)
0.090
(2.286)
NOM
0.092
(2.337)
DIA NOM
(2X)
PIN NO. 1 IDENT
16
15
14
13
12
11
10
9
0.250 ±0.005
(6.350 ±0.127)
1
2
3
4
5
6
7
8
0.280
(7.112)
MIN
0.030
(0.762)
MAX
0.300–0.320
(7.620–8.128)
95°±5°
0.009–0.015
(0.229–0.381)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.065
(1.651)
0.060
(1.524)
0.040
(1.016)
TYP
0.130 ±0.005
(3.302 ±0.127)
0.145–0.200
(3.683–5.080)
90° ±4°
TYP
0.020
(0.508)
MIN
0.125–0.140
(3.175–3.556)
0.018 ±0.003
(0.457 ±0.076)
0.075 ±0.015
(1.905 ±0.381)
0.100 ±0.010
(2.540 ±0.254)
N16A (REV E)

4 Lead Molded TO-202
NS Package Number P04A

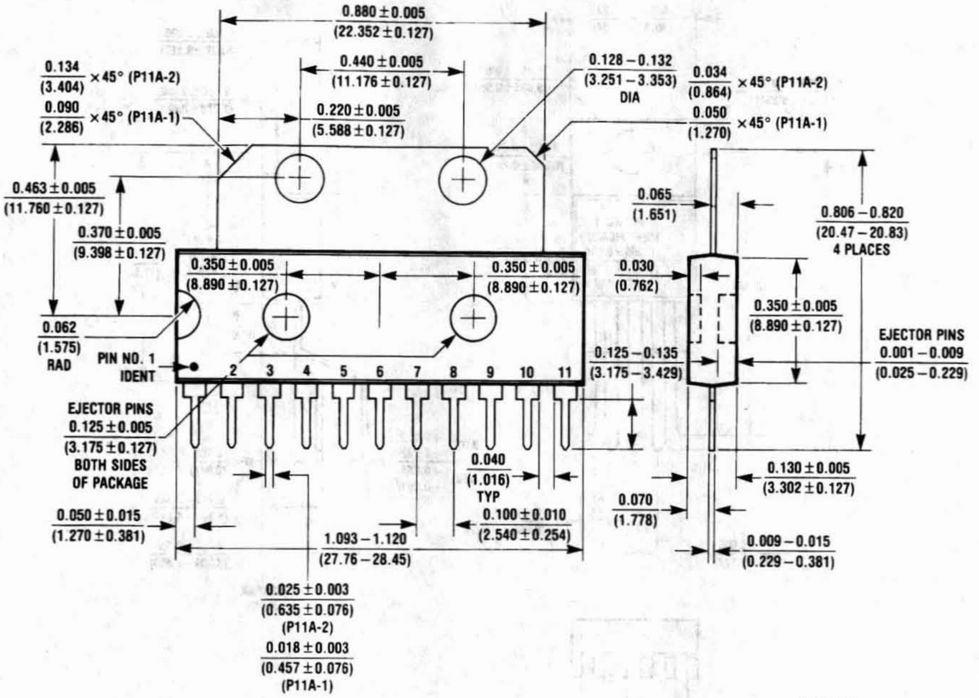
All dimensions are in inches (millimeters)


0.395 ± 0.015
(10.03 ± 0.381)
0.125 ± 0.010
(3.175 ± 0.254)
0.385 ± 0.020
(9.779 ± 0.508)
0.143 ± 0.003
(3.632 ± 0.076)
DIA
0.250 ± 0.015
(6.35 ± 0.381)
0.125 ± 0.025
(3.175 ± 0.635)
0.515 ± 0.025
(13.08 ± 0.635)
0.023 – 0.030
(0.584 – 0.762)
0.032 ± 0.005
(0.813 ± 0.127)
0.100 ± 0.010
(2.540 ± 0.254)
0.045 – 0.060
(1.143 – 1.524)
0.150 ± 0.010
(3.810 ± 0.254)
0.021 ± 0.003
(0.533 ± 0.076)
0.053 ± 0.015
(1.346 ± 0.381)

P04A (REV A)

11 Lead Molded TO-202
NS Package Number P11A

All dimensions are in inches (millimeters)

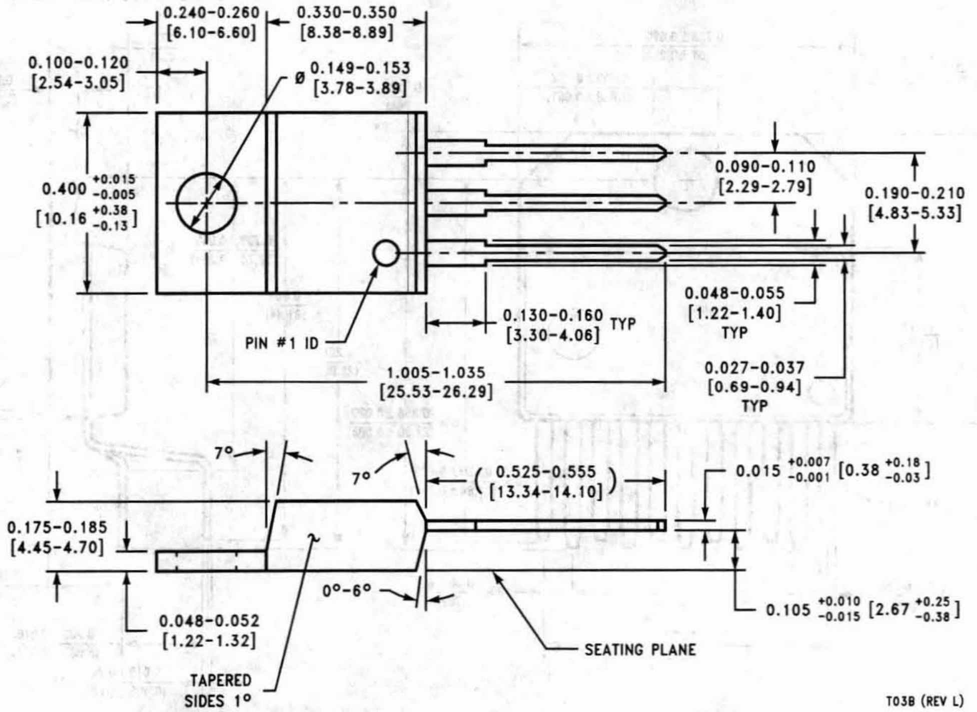


0.880 ± 0.005 (22.352 ± 0.127)
0.440 ± 0.005 (11.176 ± 0.127)
0.220 ± 0.005 (5.588 ± 0.127)
0.134 (3.404) × 45° (P11A-2)
0.090 (2.286) × 45° (P11A-1)
0.128 – 0.132 (3.251 – 3.353) DIA
0.034 (0.864) × 45° (P11A-2)
0.050 (1.270) × 45° (P11A-1)
0.463 ± 0.005 (11.760 ± 0.127)
0.370 ± 0.005 (9.398 ± 0.127)
0.350 ± 0.005 (8.890 ± 0.127)
0.350 ± 0.005 (8.890 ± 0.127)
0.065 (1.651)
0.806 – 0.820 (20.47 – 20.83) 4 PLACES
0.030 (0.762)
0.350 ± 0.005 (8.890 ± 0.127)
EJECTOR PINS 0.001 – 0.009 (0.025 – 0.229)
0.062 (1.575) RAD
PIN NO. 1 IDENT
2 3 4 5 6 7 8 9 10 11
0.125 – 0.135 (3.175 – 3.429)
EJECTOR PINS 0.125 ± 0.005 (3.175 ± 0.127) BOTH SIDES OF PACKAGE
0.040 (1.016) TYP
0.130 ± 0.005 (3.302 ± 0.127)
0.070 (1.778)
0.050 ± 0.015 (1.270 ± 0.381)
0.100 ± 0.010 (2.540 ± 0.254)
1.093 – 1.120 (27.76 – 28.45)
0.009 – 0.015 (0.229 – 0.381)
0.025 ± 0.003 (0.635 ± 0.076) (P11A-2)
0.018 ± 0.003 (0.457 ± 0.076) (P11A-1)

P11A (REV F)

3 Lead Molded TO-220
NS Package Number T03B

All dimensions are in inches [millimeters]

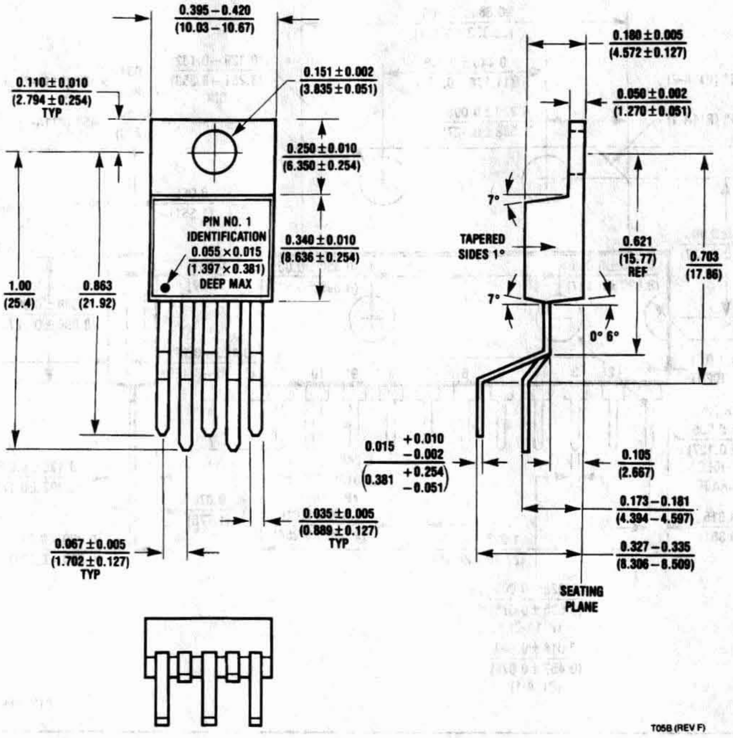


0.240-0.260 [6.10-6.60]
0.330-0.350 [8.38-8.89]
0.100-0.120 [2.54-3.05]
Ø 0.149-0.153 [3.78-3.89]
0.400 +0.015 -0.005 [10.16 +0.38 -0.13]
0.090-0.110 [2.29-2.79]
0.190-0.210 [4.83-5.33]
0.048-0.055 [1.22-1.40] TYP
0.130-0.160 [3.30-4.06] TYP
PIN #1 ID
1.005-1.035 [25.53-26.29]
0.027-0.037 [0.69-0.94] TYP
7°
7°
(0.525-0.555 [13.34-14.10])
0.015 +0.007 -0.001 [0.38 +0.18 -0.03]
0.175-0.185 [4.45-4.70]
0°-6°
0.105 +0.010 -0.015 [2.67 +0.25 -0.38]
0.048-0.052 [1.22-1.32]
SEATING PLANE
TAPERED SIDES 1°

T03B (REV L)

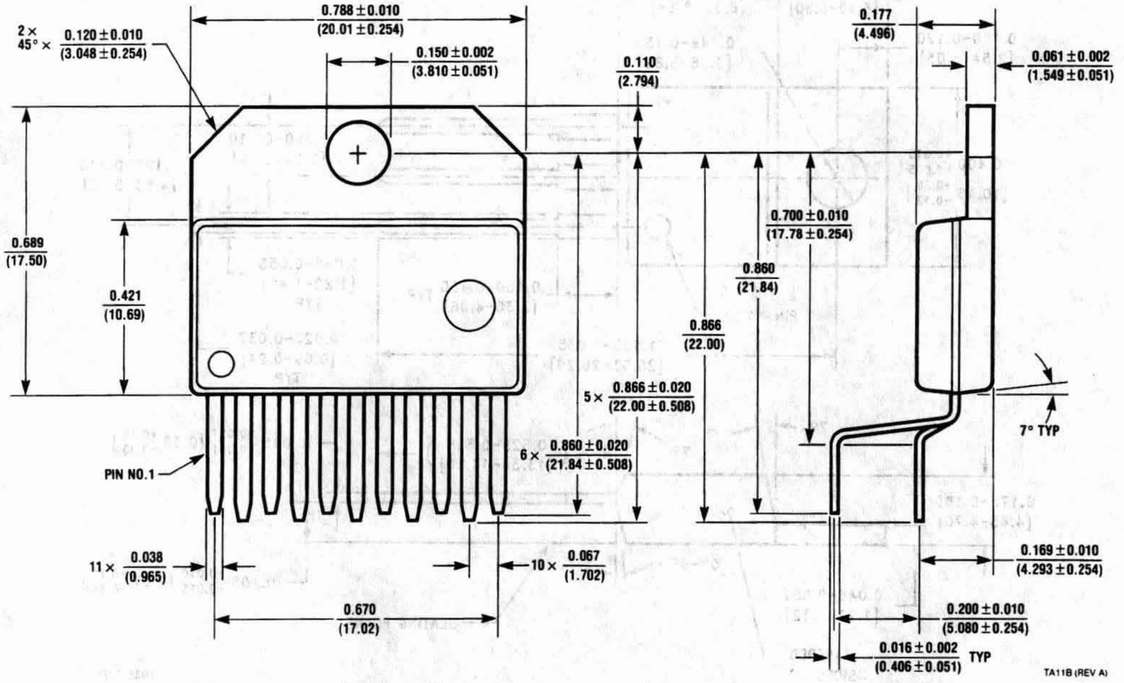
5 Lead Molded TO-220
NS Package Number T05B

All dimensions are in inches (millimeters)


0.395 – 0.420
(10.03 – 10.67)
0.110 ± 0.010
(2.794 ± 0.254)
TYP
0.151 ± 0.002
(3.835 ± 0.051)
0.250 ± 0.010
(6.350 ± 0.254)
PIN NO. 1
IDENTIFICATION
0.055 × 0.015
(1.397 × 0.381)
DEEP MAX
0.340 ± 0.010
(8.636 ± 0.254)
1.00
(25.4)
0.863
(21.92)
0.035 ± 0.005
(0.889 ± 0.127)
TYP
0.067 ± 0.005
(1.702 ± 0.127)
TYP
0.180 ± 0.005
(4.572 ± 0.127)
0.050 ± 0.002
(1.270 ± 0.051)
7°
TAPERED
SIDES 1°
0.621
(15.77)
REF
0.703
(17.86)
7°
0° 6°
0.015 +0.010 −0.002
(0.381 +0.254 −0.051)
0.105
(2.667)
0.173 – 0.181
(4.394 – 4.597)
0.327 – 0.335
(8.306 – 8.509)
SEATING
PLANE
T05B (REV F)

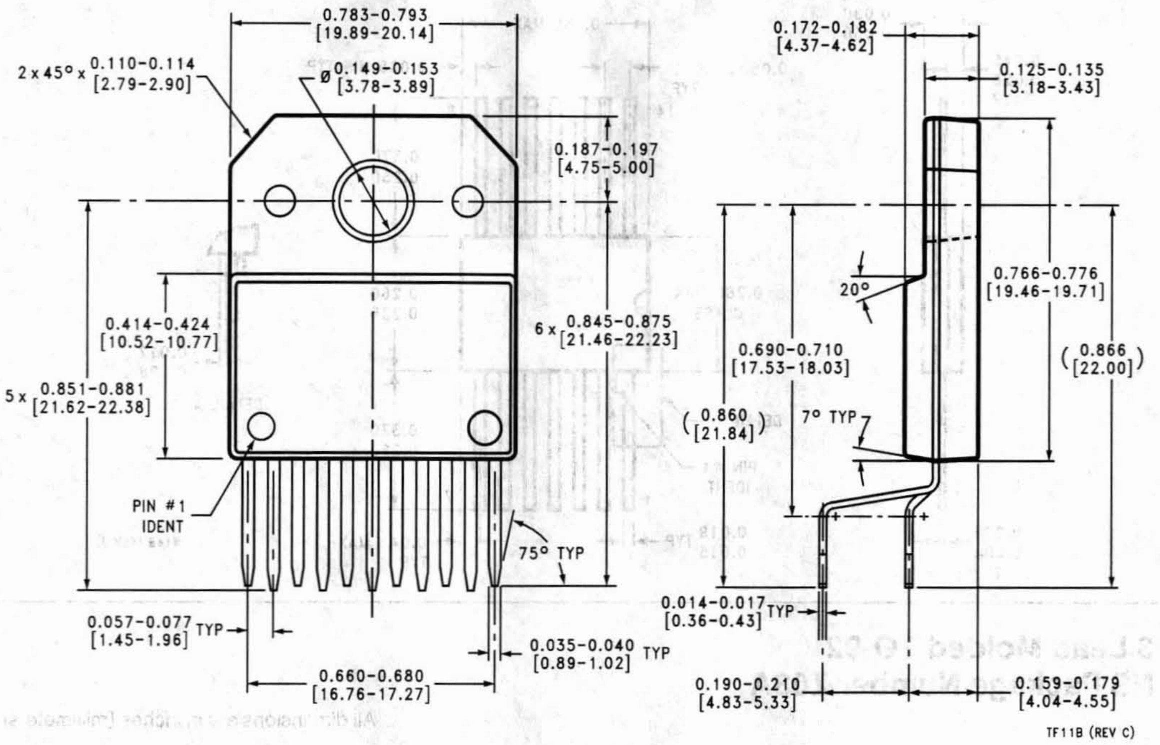
11 Lead Molded TO-220
NS Package Number TA11B

All dimensions are in inches (millimeters)


0.788 ± 0.010
(20.01 ± 0.254)
2 × 45° × 0.120 ± 0.010
(3.048 ± 0.254)
0.150 ± 0.002
(3.810 ± 0.051)
0.110
(2.794)
0.177
(4.496)
0.061 ± 0.002
(1.549 ± 0.051)
0.689
(17.50)
0.421
(10.69)
0.700 ± 0.010
(17.78 ± 0.254)
0.860
(21.84)
0.866
(22.00)
5 × 0.866 ± 0.020
(22.00 ± 0.508)
6 × 0.860 ± 0.020
(21.84 ± 0.508)
7° TYP
PIN NO.1
11 × 0.038
(0.965)
10 × 0.067
(1.702)
0.670
(17.02)
0.169 ± 0.010
(4.293 ± 0.254)
0.200 ± 0.010
(5.080 ± 0.254)
0.016 ± 0.002
(0.406 ± 0.051)
TYP
TA11B (REV A)

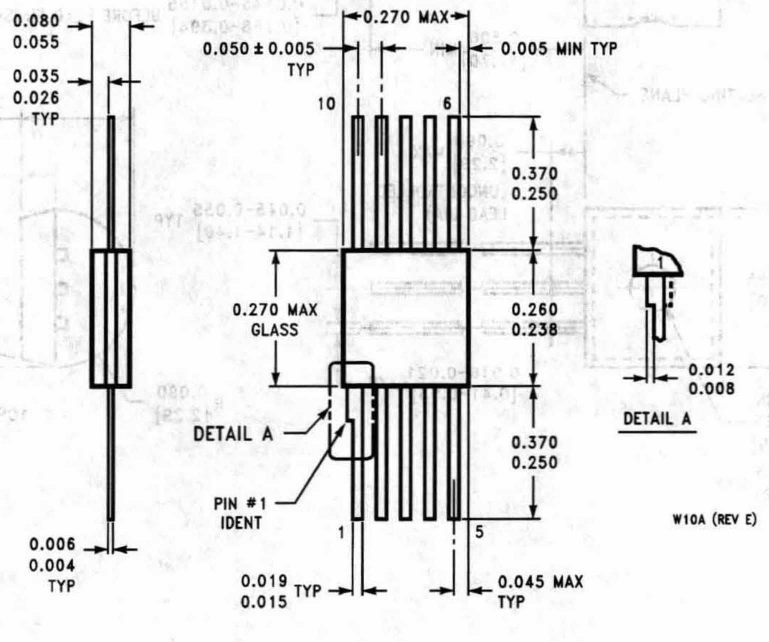
11 Lead Molded TO-220
NS Package Number TF11B

All dimensions are in inches [millimeters]


0.783–0.793
[19.89–20.14]
2 x 45° x 0.110–0.114
[2.79–2.90]
Ø 0.149–0.153
[3.78–3.89]
0.187–0.197
[4.75–5.00]
0.414–0.424
[10.52–10.77]
6 x 0.845–0.875
[21.46–22.23]
5 x 0.851–0.881
[21.62–22.38]
PIN #1
IDENT
75° TYP
0.057–0.077
[1.45–1.96] TYP
0.035–0.040
[0.89–1.02] TYP
0.660–0.680
[16.76–17.27]
0.172–0.182
[4.37–4.62]
0.125–0.135
[3.18–3.43]
20°
0.766–0.776
[19.46–19.71]
0.690–0.710
[17.53–18.03]
(0.866
[22.00])
(0.860
[21.84])
7° TYP
0.014–0.017
[0.36–0.43] TYP
0.190–0.210
[4.83–5.33]
0.159–0.179
[4.04–4.55]
TF11B (REV C)

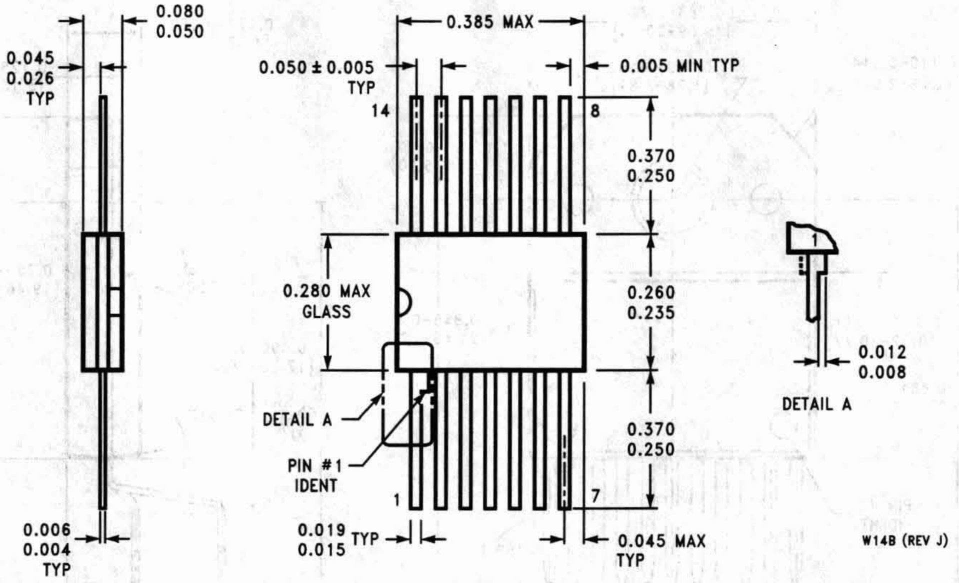
10 Lead Cerpack
NS Package Number W10A

All dimensions are in inches


0.080
0.055
0.035
0.026
TYP
0.006
0.004
TYP
0.270 MAX
0.050 ± 0.005
TYP
0.005 MIN TYP
10
6
0.370
0.250
0.270 MAX
GLASS
0.260
0.238
DETAIL A
0.370
0.250
PIN #1
IDENT
1
5
0.019
0.015 TYP
0.045 MAX
TYP
0.012
0.008
DETAIL A
W10A (REV E)

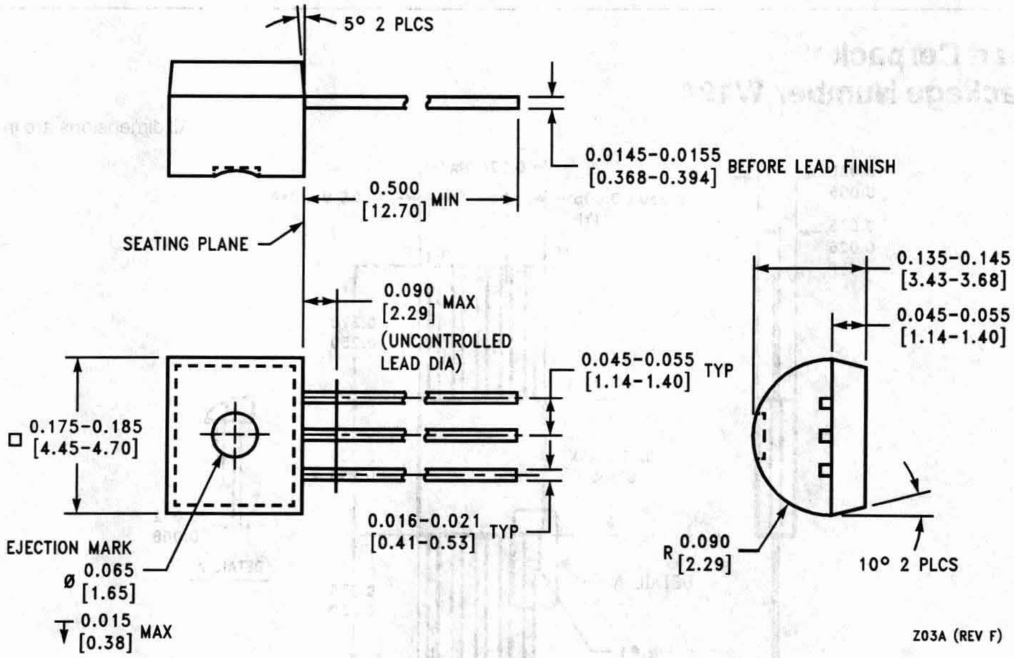
14 Lead Ceramic Flatpack
NS Package Number W14B

All dimensions are in inches


0.080
0.050
0.045
0.026
TYP
0.006
0.004
TYP
0.385 MAX
0.050 ± 0.005
TYP
0.005 MIN TYP
14
8
0.370
0.250
0.280 MAX
GLASS
0.260
0.235
DETAIL A
PIN #1
IDENT
0.370
0.250
1
7
0.019
0.015
TYP
0.045 MAX
TYP
1
0.012
0.008
DETAIL A
W14B (REV J)

3 Lead Molded TO-92
NS Package Number Z03A

All dimensions are in inches [millimeters]


5° 2 PLCS
0.0145-0.0155
[0.368-0.394]
BEFORE LEAD FINISH
0.500
[12.70]
MIN
SEATING PLANE
0.090
[2.29]
MAX
(UNCONTROLLED
LEAD DIA)
0.045-0.055
[1.14-1.40]
TYP
□ 0.175-0.185
[4.45-4.70]
0.016-0.021
[0.41-0.53]
TYP
EJECTION MARK
ø 0.065
[1.65]
0.015
[0.38]
MAX
0.135-0.145
[3.43-3.68]
0.045-0.055
[1.14-1.40]
R 0.090
[2.29]
10° 2 PLCS
Z03A (REV F)

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